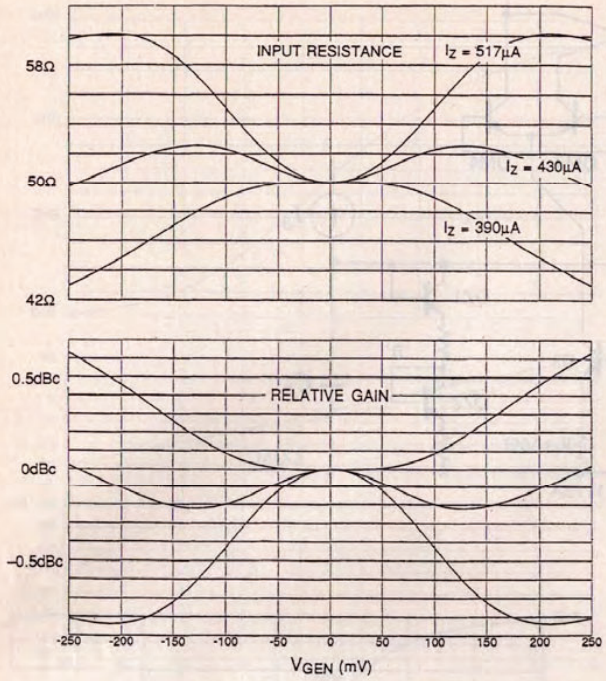


Fig. 9. Incremental gain and R_{IN} for various other padding conditions.

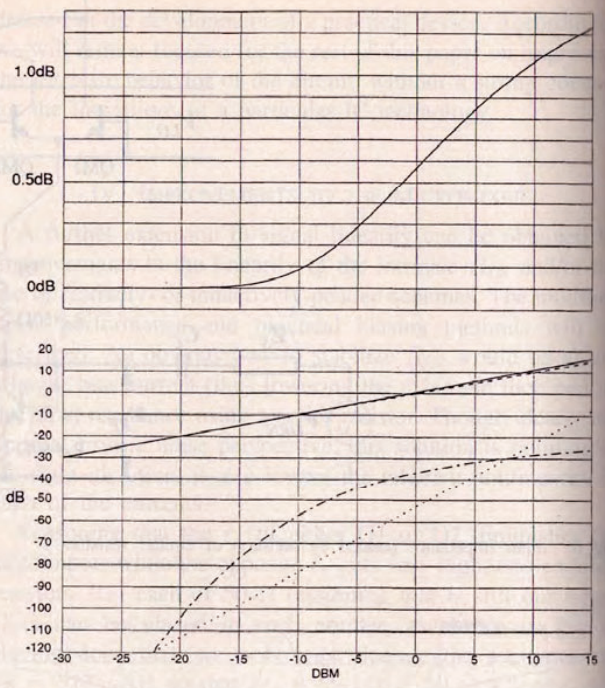


Fig. 10. Harmonic signature $I_Z = 390$ μAP, $R_P = 34$ Ω. Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

Thus for a 50-Ω input, this optimal solution occurs at $I_Z = 1.5\,I_{Z0} = 387.75$ μAP and $R_P = 33.33$ Ω. In practice, slightly higher bias levels will result in a useful improvement in *large-signal* linearity.

Fig. 9 shows the incremental R_{IN} for $I_Z = 390$ μAP ($R_P = 34$ Ω) and 430 μAP ($R_P = 40$ Ω) over the range -250 mV $\leq V_{GEN} \leq +250$ mV, which for a sinusoidal input would correspond to a loaded input power of -8 dBm; the previous result is also shown for comparison. The small-signal linearity is near-optimal using $I_Z = 390$ μAP, while it remains flatter over more of this input range when using $I_Z = 430$ μAP (maximum deviation of +2.5 Ω). Note that the incremental gain follows a predictable inverse relationship to the sum of R_S and R_{IN}. For $I_Z = 430$ μAP, it varies by 0.22 dB over this input range, and by only 0.003 dB over -50 mV $\leq V_{GEN} \leq +50$ mV for $I_Z = 390$ μAP.

The harmonic signature for $I_Z = 390$ μAP is shown in Fig. 10. Again there is no 1 dB gain compression point; instead, the gain increases to +1.2 dB at +15 dBm and is 0.57 dB high at 0 dBm. The H_3 is extremely low, being -98 dBc at -22 dBm, resulting in a PH_3 of +27 dBm. An unwelcome artifact of this response is that over the signal range -22 dBm to +7.5 dBm the H_3 now lies *above* the extrapolated line. Fig. 11 shows the results for $I_Z = 430$ μAP. The fundamental output is even more constant, dropping by only -0.12 dB at -9 dBm and rising to +0.63 dB at +15 dBm. The H_3 remains very low, now -78 dBc at -30 dBm, resulting in a PH_3 of +9 dBm. Furthermore, now both the H_2 (not shown) and H_3 always remain below the extrapolations, and the H_3 is notably lower than for the last case at high signal levels, being only -42 dBc at an input power of +15 dBm.

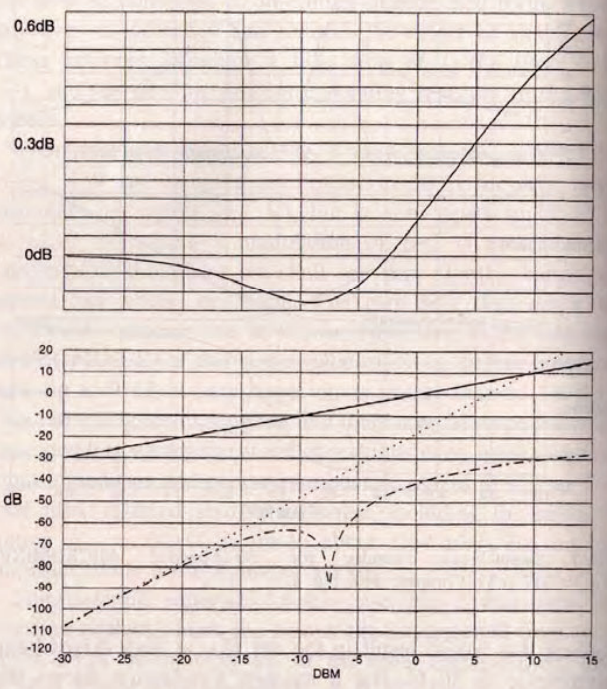


Fig. 11. Harmonic signature $I_Z = 430$ μAP, $R_P = 40$ Ω. Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

Numerous simulation studies have been carried out to explore the intermodulation properties of this cell using a two-tone test input. Using the "optimal" bias of 390 μAP, test tones of 320 MHz and 340 MHz and a transistor with a TF of

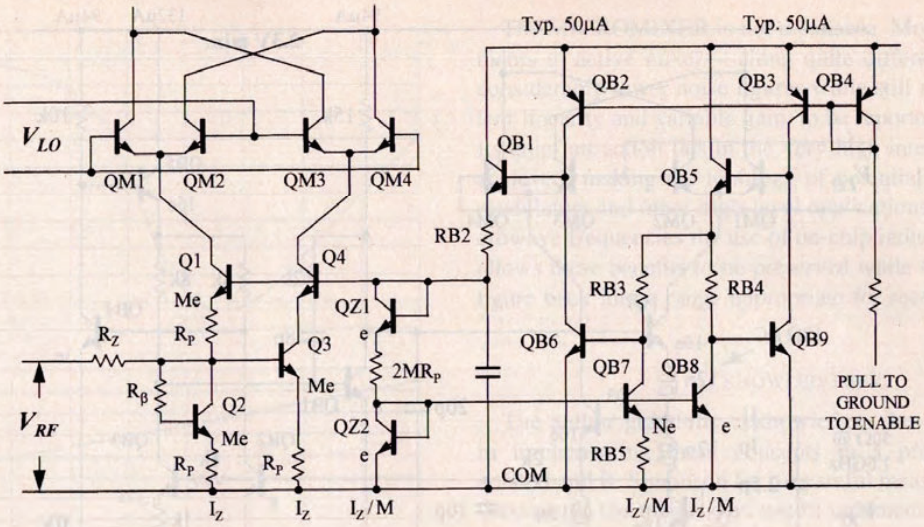


Fig. 12. The T-padded form and bias details.

10 ps (f_T = 16 GHz) the side-tone powers using test levels of −30 dBm are −92.8 dB below the wanted signals; I2P3 thus evaluates to $-30 + (92.8/2) = 16.5$ dBm. As always, caution is needed in interpreting results based on simplified simulations, which nevertheless usefully serve to *bound* the best-possible performance.

The variation of input noise as a function of the bias current has been explored over a wide range using an algorithmic value of $R_F = 2R_{IN} - V_T/I_Z$. For the 50-Ω case, a useful approximation for the total noise spectral density, referred to the generator, including that of the source resistance, real resistors for R_F, and collector shot noise, but excluding base resistance or base shot noise, is

$$E_N = \left\{1 + \frac{2}{9}(1 - \exp\xi) + \frac{1}{24}\left(1 - \exp\frac{\xi}{24}\right)\right\} \times 1.44 \text{ nV}/\sqrt{\text{Hz}} \quad (18)$$

where $\xi = (I_Z - I_{Z0})/I_{Z0}$. The value is within ±0.02 nV/$\sqrt{\text{Hz}}$ for all bias currents above I_{Z0}.

B. The Tee-Padded MICROMIXER

A further refinement to the design results when the padding scheme just described is augmented with a series-connected input resistor. The left-hand side of Fig. 12 shows this simple modification. The addition of R_Z alters the required value of R_P. Having chosen R_Z, considerable latitude remains in the choice of I_Z. Thus, the optimization space is rather large. The cascode Q4 is added to equalize the V_{CE} of Q2 and Q3; it also reduces the amount of LO voltage appearing at the emitters of QM3 and QM4 that couples back to the input. In practice, however, the incidental inequality of V_{CE} may help to recover some of the current gain in the mirror lost by reason of its finite ac beta, and the cascode may be contraindicated.

The approach used in studying this circuit has been to choose combinations that result in a null in the derivative $\partial G/\partial V_{GEN}$ at $V_{GEN} = 0$, that is, in flat gain versus instantaneous input voltage for small signals. Table I lists some

TABLE I

R_Z Ω	R_P Ω	I_Z μAP	PH_3 dBm (−30dBm)	I2P3 dBm (−30dBm)	SSB NF dB	R_{IN} Ω (V_{RF} = ±100mV)	ΔG dB
0	33.33	388	16.3	15.5	9.64	49.00	0.088
2	32.14	405	16.7	16.6	9.75	49.23	0.067
4	30.71	422	17.4	17.0	9.87	49.31	0.060
6	29.35	441	18.0	17.5	10.00	49.42	0.051
8	28	462	18.6	18.2	10.14	49.52	0.042
10	26.67	485	19.3	18.8	10.30	49.61	0.034
15	23.33	554	21.1	20.6	10.75	49.80	0.020
20	**20**	**647**	**23.3**	**22.4**	**11.25**	**49.90**	**0.008**
25	16.67	776	24.5	25.3	11.90	49.95	0.004
30	13.33	970	27.1	28.5	12.75	49.98	0.001

combinations and various performance criteria. In all cases an input match to 50 Ω (and thus a 0-dB relative gain) at $V_{GEN} = 0$ is provided. The I2P3 was determined for test signals of 320 MHz and 340 MHz, each of either −30 dBm (±10 mV at the RF input) or −10 dBm (±100 mV), in this particular case using a transistor having an effective f_T of 16 GHz.

From the point of view of realizability and robustness, we are especially interested in solutions resulting in resistor combinations that are integer multiples of a unit element. One in particular stands out, namely, I_Z = 647 μAP, $R_Z = R_P$ = 20 Ω. For this case, R_{IN} varies from 50 Ω at $V_{GEN} = 0$ and falls only slightly to 49.9 Ω at $V_{GEN} = \pm 200$ mV ($V_{RF} = \pm 100$ mV); the gain theoretically varies by only 0.008 dB. This points toward very linear performance as a mixer, as evidenced by the excellent two-tone (320/340 MHz) results. The noise figure in SSB full-mixing mode is a moderate 11.25 dB.

A practical biasing system is also shown on the right of Fig. 12. It is based on an all-NPN delta-V_{BE} (PTAT) cell [7] tightly integrated into the RF stage, resulting in precise biasing. In an optimal realization, all resistors would be thin-film, having good absolute accuracy and near-zero temperature-coefficient, for excellent control of R_{IN}. The core of this cell is

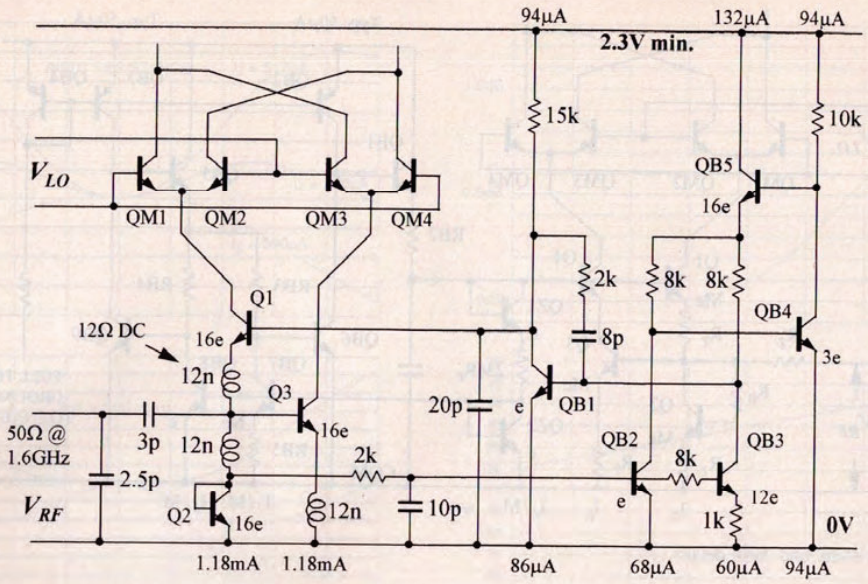


Fig. 13. L-band mixer using inductive degeneration.

QB7, QB8, and RB5. Loads RB3 and RB4 are equal. The dual-loop amplifier establishes $I_{C7} = I_{C8} = (V_T \log N)/R_{B5}$. The current-density in QB8 is replicated in QZ2, and becomes M times larger in Q1–Q4. Thus, $R_{IN} = R_Z + \{R_{B5}/M \log(N) + R_P\}/2$. The PNP transistors QB2–QB4 provide a cell-enable feature. They are entirely noncritical, operating at low currents, and may be lateral devices; they may be optionally replaced by resistors if the enable feature is not required.

Many subtle design issues remain. For example, we have noted the importance of cancellation of the individual nonlinearities of the two output currents I_1 and I_3, but not yet addressed the effect of the finite ac beta (which is often very low, being roughly f/f_T), particularly in the current mirror section. This is addressed in the circuit shown in Fig. 12 by the inclusion of the resistor R_β in the base of Q2, whose theoretical value should be $2V_T/I_Z$. This restores the overall unity ratio of the mirror, while it also slightly raises the input impedance of the mirror section, particularly at high frequencies, which has the further useful effect of compensating for the finite alpha of Q1. However, there is a significant noise penalty, and a lower value may be necessary to achieve a compromise between a reduction of beta-sensitivity and the increase in noise.

C. Microwave Variants

The use of monolithic inductors in place of the degeneration resistors R_F is clearly a useful alternative in microwave applications. A low Q is not a disadvantage here. Using typical metallization technologies, the series resistance is of the order of 1 Ω per nanohenry. Thus, the inductive reactance and resistance have the same magnitude at a frequency which is the solution of the equation $2\pi f x\ (\text{nH}) = x\ (\Omega)$, or, $f \approx 160$ MHz. Accordingly, these components remain essentially inductive above about 1 GHz. Note in passing that the metallization resistance is roughly PTAT, so the Johnson noise increases in direct proportion to temperature, not as the square root.

The component values shown in Fig. 13 provide a purely resistive input impedance of 50 Ω at 1.6 GHz, for the optimum bias current of 1.18 mAP, at which current-density the transistors used in these experiments exhibit an f_T of about 18 GHz. In this bias scheme the current in Q2 is set up by using it as the current-sensor in the loop enclosing the delta-V_{BE} cell, QB2–QB3. This method eliminates the effect of the inductor resistance. An RF filter (2 kΩ/10 pF) and beta compensation (the 8 kΩ in the base of QB3) are included. The bias loop needs special attention to HF compensation. This bias system can operate at supply voltages of under 2.5 V.

Slight compression is evident in the harmonic signature (Fig. 14): the fundamental dips to −0.93 dB at an input of about −2 dBm before rising again. The input-referred single-tone third-order intercept is at +10.2 dBm, and the noise-spectral-density is 1.22 nV/$\sqrt{\text{Hz}}$ for an amplifier-mode noise-figure of 2.6 dB.

Precise linearity matching of the separate sections handling the positive and negative input excursions will always be a critical factor in any Class-AB RF structure. It will be obvious that two of these RF stages may be combined in a differential manner to effect further improvement in linearity through a cancellation process based on symmetry and component matching. The input impedance—now measured between the two "floating" input nodes—may be readjusted to any desired value; the input port must now be driven differentially, typically using a balun. Both the noise spectral density and the signal handling capacity will increase. Further considerations relate to embedding this cell into an integrated circuit package, which brings with it numerous important complications arising from lead inductances and their mutual coupling, and the many parasitic capacitances associated with the input path, including those due to ESD devices. These and other issues lie

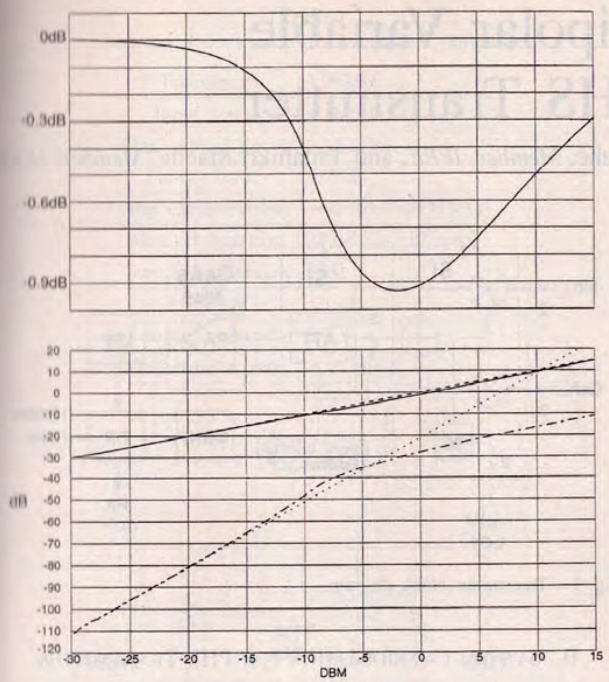


Fig. 14. Harmonic signature for the L-band variant ($I_Z = 1.18$ mA). Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

beyond the primary objective of this paper, which has been to outline the general conceptual and theoretical framework of the MICROMIXER and point to some new areas for development.

V. Conclusion

The MICROMIXER topology provides an accurate input impedance, high intermodulation intercepts, and an almost unlimited signal capacity at its input, arising from the use of a Class-AB topology, while maintaining acceptable noise performance. This paper has provided a brief overview of its potential. The results are based largely on simple models of the devices, in order to better compare the variants on a similar basis, without the coloration introduced by complex dynamic effects, and as an aid to the development of insights leading to improved topologies. It is clear that if the fundamentals are not right, there is little benefit in proceeding to the later steps of adding the greater realism captured in the full transistor model.

Nonetheless, for modern low-inertia transistors (that is, having few-picosecond transit times and few-femtofarad capacitances) operating at sensible bias currents, the "low frequency" predictions are reliable out to many hundreds of megahertz and still useful as a comparative tool in the microwave range. In practice, package parasitics, biasing-current errors, and instrumentation issues will have a much greater impact on determining mixer performance at microwave frequencies, provided that due care is taken in the design and layout of the monolithic circuit.

The MICROMIXER is not a panacea. More recent developments in active mixers—along quite different lines—provide considerably lower noise figures while still maintaining excellent linearity and variable gain, to be reported at a future time. Its chief attraction lies in the very high intercepts that can be achieved, making the topology of potential value in transmit modulators and other high-level applications. However, at microwave frequencies the use of on-chip inductive degeneration allows these benefits to be preserved while lowering the noise figure back into a range appropriate for receiver applications.

Acknowledgment

The author gratefully acknowledges the work of G. Dawe in implementing these concepts in a practical monolithic context and R. Simonson for his careful measurements on early versions of the mixer. The useful comments of the reviewers have also been noted.

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Barrie Gilbert (M'62–SM'71–F'84) was born in 1937 in Bournemouth, England.

He pursued an early interest in solid-state devices at Mullard Ltd., working on first-generation planar IC's. Emigrating to the United States in 1964, he joined Tektronix, Beaverton, OR, where he developed the first electronic knob-readout system and other advances in instrumentation. Between 1970–1972 he was Group Leader at Plessey Research Laboratories. He joined Analog Devices Inc., Beaverton, OR, in 1972 and was appointed as ADI Fellow in 1979. He manages the development of communications IC's at the NW Labs in Beaverton.

For work on merged logic Dr. Gilbert received the IEEE "Outstanding Achievement Award" (1970) and the IEEE Solid-State Circuits Council "Outstanding Development Award" (1986). He was Oregon Researcher of the Year in 1990 and received the Solid-State Circuits Award (1992) for "Contributions to Nonlinear Signal Processing." He has five times received the ISSCC Outstanding Paper Award and has been issued over 40 patents. He holds an Honorary Doctorate from Oregon State University.

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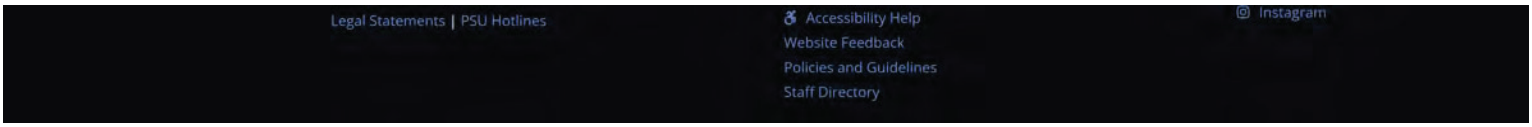
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Appendix GALTON02

Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement

Ian Galton, *Fellow, IEEE*, and Colin Weltin-Wu, *Member, IEEE*

(Invited Paper)

***Abstract*— Precision oscillators are ubiquitous in modern electronic systems, and their accuracy often limits the performance of such systems. Hence, a deep understanding of how oscillator performance is quantified, simulated, and measured, and how it affects the system performance is essential for designers. Unfortunately, the necessary information is spread thinly across the published literature and textbooks with widely varying notations and some critical disconnects. This paper addresses this problem by presenting a comprehensive one-stop explanation of how oscillator error is quantified, simulated, and measured in practice, and the effects of oscillator error in typical oscillator applications.**

***Index Terms*— Oscillator phase error, phase noise, jitter, frequency stability, Allan variance, frequency synthesizer, crystal, phase-locked loop (PLL).**

I. Introduction

ELECTRONIC oscillators are in nearly all electronic devices. They make it possible to modulate and demodulate wireless signals, clock both digital and sampled-data analog circuits, and measure time intervals. Moreover, they are astonishingly precise. For example, present-day mobile telephone transceivers incorporate several highly-tunable multi-GHz oscillators whose output signals have integrated jitter of less than a few hundred femtoseconds. Nevertheless, oscillator precision is often a limiting factor in high-performance applications such as modern wireless and wireline communications, radar, and high-speed digital circuits. Accordingly, it is critical for engineers to understand how oscillator performance is quantified, simulated, and measured, and how oscillator error affects application performance.

Unfortunately, acquiring this knowledge is not easy. The information is spread thinly across the published literature, and there are fundamental disconnects between much of the published information and actual practice. One disconnect is that most textbooks and papers define oscillator error in terms of sinusoidal oscillator signals, but most practical circuits use squared-up versions of such oscillator signals that approximate square waves. A related disconnect is that most communication textbooks define a mixer as performing multiplication by a sinusoidal oscillator signal whereas most practical mixer circuits perform multiplication by squared-up oscillator signals. Fundamental questions typically are left unanswered such as: How does the squaring-up process change the oscillator error? How does multiplying by a squared-up oscillator signal instead of a sinusoidal signal change a mixer's behavior and response to oscillator error?

Another obstacle to learning the material is that there are three distinct oscillator error metrics in common use: phase error, jitter, and frequency stability. Each metric offers advantages in certain applications, so it is important to understand how they relate to each other, yet with the exception of [1], the authors are not aware of prior publications that provide this information directly.

The goal of this tutorial is to comprehensively and systematically present this information. There are many publications that describe and model the circuit-level mechanisms of oscillator error, e.g., [2]–[9], so this material is not covered here. Instead, the paper describes how to evaluate, simulate, and measure oscillator error, and the system-level effects of oscillator error in typical circuit applications.

II. Phase Error

A. Sinusoidal Oscillator Signal Model

Oscillator accuracy is critical in so many electronics applications that the recommended quantities with which to quantify it have been specified in an IEEE standard [10]. As with most other papers and textbooks that touch on the subject, the IEEE standard starts from the premise that an ideal oscillator is purely sinusoidal. It expresses the instantaneous output of a non-ideal oscillator as

$$v(t) = [V_0 + \varepsilon(t)] \sin(\omega_0 t + \phi(t)), \tag{1}$$

where V_0 is the nominal peak amplitude, $\varepsilon(t)$ is the *amplitude error*, ω_0 is the nominal frequency, and $\phi(t)$ is the *phase error*. The amplitude error represents the oscillator's deviation from the nominal amplitude, and the phase error represents the oscillator's deviation from the ideal phase, $\omega_0 t$. It is assumed that $|\varepsilon(t)| < V_0$ for all t and $\omega_0 t + \phi(t)$ monotonically increases with t, which are reasonable assumptions given that the purpose of the model is to characterize precision oscillators.

The oscillator signal's zero-crossing times, i.e., the values of t for which $v(t) = 0$, are of particular importance. Throughout this paper, the zero-crossing times are denoted as t_n and ordered such that $t_n > t_{n-1}$ for all integers n, so t_n is an increasing sequence that comprises all values of t at which

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I. Galton is with the University of California at San Diego, La Jolla, CA 92093 USA (e-mail: galton@ucsd.edu).

C. Weltin-Wu is with Analog Devices, Inc., San Jose, CA 95134 USA.

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$v(t) = 0$. It follows from (1) and the $|\varepsilon(t)| < V_0$ assumption that, for each integer n,

$$\phi(t_n) = \pi n - \omega_0 t_n. \tag{2}$$

Samples of the phase error at the zero-crossing times, i.e., $\phi(t_n)$ for every integer n, can be measured directly from $v(t)$ by substituting the nth time at which $v(t)$ crosses zero into (2). In this sense, the $\phi(t_n)$ values are uniquely determined by $v(t)$.

However, $\phi(t)$ is not uniquely determined by $v(t)$ for values of t that are not zero-crossing times, because at such times there are an infinite number of $\varepsilon(t)$ and $\phi(t)$ functions that yield the same value of $v(t)$. This can be verified by observing that whenever $t \neq t_n$, the right side of (1) can be written as $[V_0 + \varepsilon_1(t)]\ \sin(\omega_0 t + \phi_1(t))$, where

$$\varepsilon_1(t) = [V_0 + \varepsilon(t)] \frac{\sin(\omega_0 t + \phi(t))}{\sin(\omega_0 t + \phi_1(t))} - V_0 \tag{3}$$

and $\phi_1(t)$ is any function for which $\omega_0 t + \phi_1(t)$ is not an integer multiple of π.

Furthermore, $\varepsilon(t)$ is not uniquely determined by $v(t)$ for *any* value of t. This follows directly from the argument above for each t that is not a zero-crossing time. For each t that is a zero-crossing time, it follows because the sine function in (1) evaluates to zero, so $\varepsilon(t)$ can take on any value.

These ambiguities generally make it impossible to separate the effects of $\phi(t)$ from those of $\varepsilon(t)$ on the performance of a circuit driven by $v(t)$. Yet it is often the case in practice that the effects of $\varepsilon(t)$ on circuits driven by oscillators are negligible compared to those of $\phi(t)$. One reason is that the mean squared value of $\varepsilon(t)$ is often very small for practical oscillators. Another reason is that typical circuits driven by oscillators only change state when $v(t)$ is relatively close to zero where the magnitude of the sinusoid in (1) is small, so it attenuates the effect of $\varepsilon(t)$. In such cases, $\phi(t)$ represents the oscillator's only significant non-ideal behavior, so the above-mentioned ambiguities are avoided.

B. Squared-Up Oscillator Signal Model

Oscillator signals that switch as abruptly as possible between $\pm V_0$ at each zero-crossing are often used instead of the sinusoidal oscillator signal given by (1). Such oscillator signals are sometimes generated by amplifying and clipping sinusoidal oscillator signals, so they are often called *squared-up* oscillator signals. Squared-up oscillator signals are widely used in practice, because, as described shortly, they offer practical benefits when used to drive circuits that are only sensitive to the oscillator signals near their zero-crossings.

In analogy with (1), a squared-up oscillator signal can be modelled as

$$v(t) = [V_0 + \varepsilon(t)]\, r\left(\omega_0 t + \phi(t)\right), \tag{4}$$

where $r(\theta)$ is a 2π-periodic function which is as close as possible to a unit square wave given by

$$r_{ideal}(\theta) = \begin{cases} 1, & \text{if } \sin(\theta) > 0, \\ 0, & \text{if } \sin(\theta) = 0, \\ -1, & \text{if } \sin(\theta) < 0. \end{cases} \tag{5}$$

Thus, $\phi(t_n)$ is still given by (2). In cases where the squared-up oscillator signal is obtained by amplifying and clipping a sinusoidal oscillator signal, the $\phi(t)$ and $\varepsilon(t)$ associated with the squared-up oscillator signal are generally different from those associated with the sinusoidal oscillator signal. However, to the extent that the amplifying and clipping circuitry has negligible noise and input offset voltage, the zero-crossing times, t_n, and the phase error sampled at the zero-crossing times, $\phi(t_n)$, are not altered by the squaring up process.

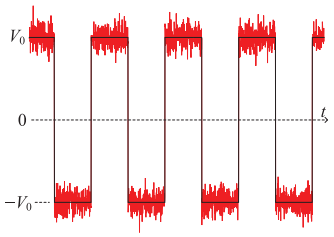


Fig. 1. Superimposed squared-up oscillator signals with and without amplitude noise.

It is convenient to rewrite the squared-up oscillator signal model as

$$v(t) = V_0 r\left(\omega_0 t + \phi(t)\right) + e(t), \tag{6}$$

which is equivalent to (4) when $e(t) = \varepsilon(t) r(\omega_0 t + \phi(t))$ but emphasizes that $\varepsilon(t)$ can be viewed as a type of additive error. Practical oscillator circuits typically introduce other types of additive error as well, and error introduced by the circuits they drive often can be modeled as input-referred error added to the oscillator signal. Therefore, $e(t)$ is more realistically modelled as $e(t) = \varepsilon(t) r(\omega_0 t + \phi(t)) + e_a(t)$, where $e_a(t)$ is all additive error other than $\varepsilon(t) r(\omega_0 t + \phi(t))$.

To the extent that $r(\theta)$ approximates (5), $v(t)$ is only near zero at its zero-crossing times, a consequence of which is that $e(t)$ only has a significant effect on the oscillator signal when the magnitude of $v(t)$ is large. This phenomenon is illustrated in Fig. 1, wherein the oscillator signal was generated by (6) with an $r(\theta)$ that well-approximates (5). Two versions of the waveform are superimposed: an ideal version in which $e(t)$ is zero, and a non-ideal version in which $e(t)$ is a noise waveform. The two waveforms are nearly identical except when their magnitudes are much greater than zero. If such an oscillator signal drives a circuit that is insensitive to the oscillator signal when its magnitude is far from zero, $e(t)$ has little effect on the circuit's behavior.

The common practice of using squared-up oscillator signals to drive such circuits renders even relatively strong amplitude and additive error negligible in terms of circuit performance. Nevertheless, as described in Sections VI and VII, care must be taken to prevent $e(t)$ from corrupting phase error simulations and laboratory measurements.

Unlike $e(t)$, phase error cannot be neglected in practical circuits. However, as explained shortly, it is not the phase error waveform itself, but the phase error sampled at times t_n, i.e., $\phi(t_n)$, that matters, and this sampling process leads to several practical issues because of aliasing.

C. Reconciliation of the Two Oscillator Signal Models

For the reasons described above, it is neither common, nor desirable in many cases, for oscillator signals to be sinusoidal in practical circuits. Yet the official IEEE definition and most communication system textbooks describe oscillator signals as sinusoidal. As shown in this subsection, these two viewpoints can be reconciled to an extent by observing that the sinusoidal

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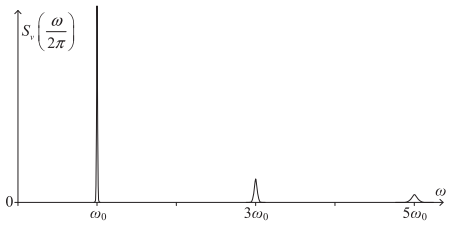


Fig. 2. Power spectrum of the first three terms of the squared-up oscillator signal given by (8).

and squared-up oscillator signal models often have nearly equivalent spectra for frequencies from 0 to well above ω_0.

Given that $r(\theta)$ in (6) is a 2π-periodic real function, it can be expressed as a Fourier series. Substituting the Fourier series representation of $r(\theta)$ into (6) yields

$$v(t) = V_0 \sum_{n=0}^{\infty} \rho_n \sin\left(n\omega_0 t + n\phi(t) + \theta_n\right) + e(t), \qquad (7)$$

where ρ_n and θ_n are constants that depend on the Fourier series coefficients. For the case where $r(\theta) = r_{ideal}(\theta)$, (7) reduces to

$$v(t) = \frac{4}{\pi} V_0 \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin\left(n\omega_0 t + n\phi(t)\right) + e(t). \qquad (8)$$

Except for the $4/\pi$ constant scale factor, the $n = 1$ term of (8) is identical to the right side of (1) in the absence of amplitude error. The remaining terms are therefore the only significant differences between the sinusoidal and squared-up oscillator signal models in this case.

The nth term of (8) for $n > 1$ is a sinusoid with phase modulation $n\phi(t)$, so Carson's rule suggests that its bandwidth is approximately n times larger than that of the first term [11]. However, the power spectrum of the nth term is centered n times further away from zero than that of the first term. Furthermore, its power is $1/n^2$ times that of the first term. Consequently, it is reasonable to expect that the terms in (8) for $n > 1$ are negligible at frequencies from 0 to well above ω_0, as illustrated conceptually in Fig. 2.

This phenomenon is particularly relevant to frequency translation via mixers in communication systems. The classic communication system textbook definition of a mixer is a circuit that multiplies an input signal by a sinusoidal oscillator signal and filters the result. An example of such a mixer that translates the center frequency of a bandpass signal from a non-zero frequency, ω_1, to another non-zero frequency, $\omega_1 - \omega_0$, is shown in Fig. 3.

In most practical situations, the sinusoidal oscillator signal in the communication system textbook version of a mixer could be replaced by a squared-up oscillator signal without significantly changing the output of the mixer. For example, consider the mixer of Fig. 3 except with the sinusoidal oscillator signal replaced by a squared-up oscillator signal. It is straightforward to verify that each of the $n > 1$ terms in (8) contribute signal components that lie outside the passband of the filter provided the bandwidths of the mixer's input signal and bandpass filter are sufficiently narrow. In this case, only the $n = 1$ term in (8) significantly affects the output of the mixer, and this term is identical to the sinusoidal oscillator

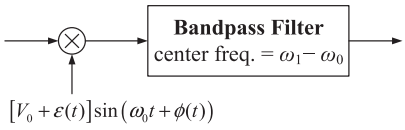


Fig. 3. Communication system textbook version of a mixer with the addition of oscillator phase and amplitude error.

signal model in the absence of amplitude error except for a scale factor of $4/\pi$.†

This behavioral equivalence between sinusoidal and squared-up oscillator signals in mixers provides some rationale for the persistence of the sinusoidal oscillator signal model despite the widespread use of squared-up oscillator signals. Mixers are of great importance in communication systems so they are taught early at the undergraduate level, and it is easier to explain the basic operation of communication system textbook style mixers with sinusoidal oscillator signals than with squared-up oscillator signals. Mixers of one type or another have been in use for over a century [13], [14], and for the first several decades they were the primary application of oscillators. Moreover, early mixers did approximate multiplication by sinusoidal oscillator signals, and this remains so in very high-frequency (e.g., millimeter wave) applications wherein parasitic capacitances and other electronic device nonidealities make squared-up oscillator signals impractical.

Nevertheless, as described in more detail below, the rationale breaks down somewhat with typical present-day mixers. Furthermore, in other oscillator applications, such as sampling and clocking, the sinusoidal oscillator model is not particularly useful. These applications use the zero-crossing times of oscillator signals to initiate specific events, so there is no benefit to thinking of the oscillator signals as being sinusoidal in such cases.

D. Circuit Applications of Oscillators

This subsection describes the types of analog and mixed-signal circuits commonly driven by oscillators. A comprehensive description of this subject could easily fill a textbook, so it is far beyond the scope of this paper. Instead, the goal is to provide qualitative descriptions that explain the practical reasons which underlie the statements made above regarding squared-up oscillator signals and why the circuits driven by them usually are insensitive to $e(t)$.

1) Mixers: As described in Section II-C, communication system textbooks describe mixers as ideal multipliers followed by filters. In contrast, circuit design textbooks typically consider just the multiplier to be the mixer. Filtering is always performed following the multiplier, but it is not considered by most circuit designers to be part of the mixing operation.

Practical mixers do not implement true multiplication. Instead, as depicted in Fig. 4 a practical mixer usually can be modelled as a device that multiplies the input signal, $x(t)$, by a strongly nonlinearly distorted and limited version of the oscillator signal, i.e., $f(v(t))$. The nonlinearity, $f(v)$, is monotonic and is limited in the sense that $f(v) \cong 1$ when $v > V_{s+}$ and $f(v) \cong -1$ when $v < V_{s-}$, where V_{s+} and V_{s-}

†An exception occurs if the mixer input has unwanted signal components at $\omega_1 - k\omega_0$, for any $k = 3, 5, \ldots$, in which case the unwanted components corrupt the desired component in the mixer's output. A harmonic rejection mixer that consists of multiple conventional mixers with squared-up oscillator signals of different phases can be used to avoid this problem if necessary [12].

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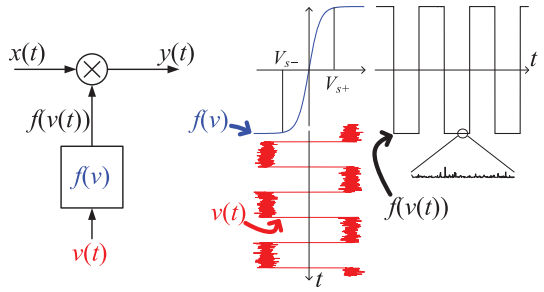


Fig. 4. Model of a practical mixer with an example that demonstrates how $f(v)$ suppresses the squared-up oscillator signal's $e(t)$ error.

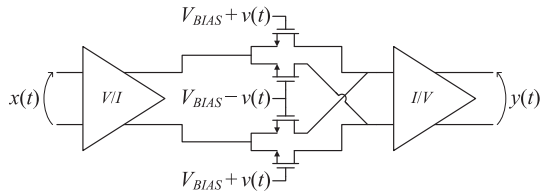


Fig. 5. Simplified diagram of a passive mixer circuit.

denote the approximate values of v where $f(v)$ saturates at 1 and -1, respectively. The limiting causes the mixer to be nearly insensitive to $v(t)$ when $v(t) < V_{s-}$ or $v(t) > V_{s+}$.

Suppose $v(t)$ is the squared-up oscillator signal given by (6) with an $r(\theta)$ that well-approximates $r_{ideal}(\theta)$, and V_0 is large enough that $V_0+e(t) > V_{s+}$ and $-V_0+e(t) < V_{s-}$. In this case $v(t)$ is nearly independent of $e(t)$ when $V_{s-} < v(t) < V_{s+}$ for the reasons described in Section II-B. While $v(t)$ does depend on $e(t)$ when $v(t) < V_{s-}$ or $v(t) > V_{s+}$, these are the regions over which the mixer is insensitive to $v(t)$. Consequently, the mixer output is insensitive to $e(t)$ for all values of $v(t)$. Given that the oscillator signal is only in the range $V_{s-} < v(t) < V_{s+}$ very near the oscillator signal's zero-crossing times, the mixer output is also insensitive to the nonlinearity imposed by $f(v)$. It follows that under these circumstances the behavior of the mixer is nearly identical to that of an ideal multiplier with the important and beneficial exception that it practically ignores $e(t)$. Specifically, the mixer's output under these circumstances well approximates

$$y(t) = \frac{4}{\pi} \sin\left(\omega_0 t + \phi(t)\right) x(t). \tag{9}$$

A practical example of such a mixer is shown in Fig. 5. The figure shows the general structure of a MOS transistor based mixer of the type currently used in mobile telephone receivers [15], [16]. The mixer consists of a differential voltage to current (V/I) converter, four MOS transistors controlled by the oscillator signal, and a differential current-to-voltage (I/V) converter.

Each of the four transistor gates is driven by $V_{BIAS}+v(t)$ or $V_{BIAS}-v(t)$, where V_{BIAS} is a constant bias voltage and $v(t)$ is the squared-up oscillator signal. The circuit is designed such that the four transistors approximate switches which connect the differential outputs of the V/I converter to the differential inputs of the I/V converter directly when $v(t)$ is sufficiently greater than zero and with swapped polarity when $v(t)$ is sufficiently less than zero.

Although the on-resistances of the transistors are never zero, the low differential input impedance of the I/V converter combined with the much higher differential output impedance

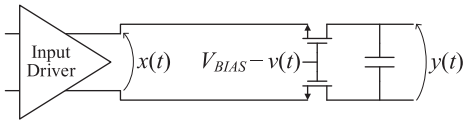


Fig. 6. Simplified diagram of an ADC's sampling circuit.

of the V/I converter causes the mixer's behavior to be fairly insensitive to non-zero transistor on-resistance. In this context, V_{s-} and V_{s+} are voltage levels such that $v(t) < V_{s-}$ and $v(t) > V_{s+}$ are the ranges of $v(t)$ over which the on-resistance of the transistors is sufficiently low to negligibly affect mixer performance. By design, the value of V_{BIAS} is chosen to cause $V_{s-} \cong -V_{s+}$ and V_0 is chosen large enough to ensure $V_0 + e(t) > V_{s+}$ and $-V_0 + e(t) < V_{s-}$ for all t, so the mixer is insensitive to $e(t)$ for the reasons described above.

2) Oscillators as Clocks in Non-Mixer Applications: In most other applications, the oscillator signal is used as a clock to mark a set of times, τ_n for $n = \ldots, -1, 0, 1, 2, \ldots$, that are as close to being uniformly spaced as possible. The zero-crossing times of a squared-up oscillator are ideal for this purpose. Typically, only the positive-going zero-crossings or only the negative-going zero-crossings are used to mark τ_n in any given application, so the oscillator signal's duty cycle can deviate from 50% without causing timing errors. In the following, without loss of generality τ_n is taken to be the nth positive-going zero-crossing time of the oscillator signal.

Ideally, $\tau_n = nT_0$, where $T_0 = 2\pi/\omega_0$ is the oscillator signal's nominal period, but oscillator phase error causes deviations from this ideal. It follows from (2) that $\tau_n = t_{2n} = [2\pi n - \phi(t_{2n})]/\omega_0$. This can be rewritten as

$$\tau_n = nT_0 + \Delta\tau_n, \quad \text{where } \Delta\tau_n = -\frac{\phi(\tau_n)}{\omega_0}. \tag{10}$$

Thus, $\Delta\tau_n$ is the deviation of τ_n from its ideal value of nT_0, and it is proportional to the oscillator signal's phase error sampled at τ_n. It is often called *absolute jitter* or *aperture jitter* and it is described further in Section V.

3) Analog-to-Digital Converters: A typical ADC uses a squared-up oscillator signal, $v(t)$, as a clock to mark the times, τ_n, at which to sample its input signal, $x(t)$. It converts the resulting sequence of sampled values, $x(\tau_n)$, to a digital output sequence. The sampling circuitry is designed to be insensitive to the clock signal, $v(t)$, except near its positive-going zero-crossings, so ADCs, like mixers, are insensitive to $e(t)$.

There are several types of ADC sampling circuits, but the circuit shown in Fig. 6 is representative of the core operation performed by most of them. The gates of the MOS transistors are driven by $V_{BIAS} - v(t)$, where V_{BIAS} is a constant bias voltage and $v(t)$ is the squared-up oscillator signal given by (6) with an $r(\theta)$ that well-approximates $r_{ideal}(\theta)$. When $v(t)$ is close to $-V_0$ the transistors are turned on, and the voltage across the capacitor tracks $x(t)$. At the positive-going zero-crossing of the oscillator signal, $v(t)$ rapidly transitions toward V_0 which abruptly turns off the transistors, thereby freezing the voltage stored on the capacitor until the subsequent negative-going zero-crossing time.

The circuit is designed such that $V_{BIAS} - V_0 - e(t) < V_{off}$ and $V_{BIAS} + V_0 - e(t) > V_{on}$ for all t, where V_{off} and V_{on} are voltage levels for which the transistors have high-enough off-resistance when $V_{BIAS} - v(t) < V_{off}$ and low-enough on-resistance when $V_{BIAS} - v(t) > V_{on}$ so as not to degrade performance. Hence, the use of a squared-up oscillator signal

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for $v(t)$ ensures that $V_{BIAS} - v(t)$ is only between V_{off} and V_{on} very near the zero-crossing times of $v(t)$. One consequence is that $e(t)$ can be neglected much like in the case of the mixer described above. Another consequence is that each transistor's nonlinear transition between its on and off states has little effect on the sampling circuit's performance. Hence, the frozen voltage stored on the capacitor when $v(t)$ is close to V_0 well-approximates $x(\tau_n)$.

4) Other Clocking Applications: Oscillators are also used to clock a wide range of other analog, mixed-signal, and digital circuits including DACs, frequency dividers, phase-frequency detectors (PFDs), time-to-digital converters (TDCs), digital-to-time converters (DTCs), timers, and synchronous digital logic. In most cases, the components within these circuits that are clocked by the oscillator signals are edge-triggered latches or flip-flops.

The clock input of each such edge-triggered latch or flip-flop is driven by a clock signal of the form $V_{BIAS} + v(t)$, where, once again, V_{BIAS} is a constant bias voltage and $v(t)$ is a squared-up oscillator signal. By design, the edge-triggered circuit only changes its state when $v(t)$ is in a narrow range of values about its midpoint, and V_0 is large enough that that $-V_0 + e(t)$ and $V_0 + e(t)$ are outside this range for all t. Therefore, by exactly the same reasoning described above for mixers and sampling circuits, such circuits are insensitive to $e(t)$.

E. Phase Error Versus Phase Noise

An oscillator signal's phase error, $\phi(t)$, usually contains both a random component and a deterministic component. The random component is caused by device noise, such as thermal and flicker noise, introduced by the transistors and other components that make up the oscillator circuit. The deterministic component is the result of deterministic disturbances that are inadvertently generated within or parasitically coupled into the oscillator circuitry. For example, the deterministic component of $\phi(t)$ in a PLL-based oscillator inevitably contains spurious tones, also known as spurs, that are not harmonics of the oscillator frequency.

In this paper, $\phi(t)$ is called *phase error* and the random component of $\phi(t)$ is called *phase noise*. This choice was made to avoid confusion because the word *noise* is considered by many people to denote purely random phenomena. It is also consistent with much of the published literature, e.g., most papers that report the measured performance of PLL-based oscillators refer to phase noise and spurious tones as distinct types of phase error. Unfortunately, the literature is not consistent in this respect. For instance, in the IEEE standard $\phi(t)$ is called *phase fluctuations* and, somewhat confusingly, the term *phase noise* is reserved exclusively for a function $\mathcal{L}(f)$ (pronounced "script-ell of f") equal to half the one-sided time average power spectrum of $\phi(t)$ [10].

F. Time Average Power Spectra

Laboratory measurements and circuit simulations of power spectra inevitably estimate time average power spectra as opposed to statistical power spectra [17]. The two-sided time average power spectrum of a real-valued continuous-time signal, in this case $\phi(t)$, is defined as

$$S_{\phi\phi}(f) = \lim_{T\to\infty} \frac{1}{T} |FT\{\phi_T(t)\}|^2 \text{ for } -\infty < f < \infty \quad (11)$$

provided the limit exists, where f has units of Hz, and $FT\{\phi_T(t)\}$ is the Fourier transform of $\phi(t)$ restricted to the interval $0 \le t \le T$. Specifically,

$$FT\{\phi_T(t)\} = \int_{-\infty}^{\infty} \phi_T(t) e^{-j2\pi f t} dt \quad (12)$$

where

$$\phi_T(t) = \begin{cases} \phi(t), & \text{if } 0 \le t \le T, \\ 0, & \text{otherwise.} \end{cases} \quad (13)$$

As is well known and can be verified from the definition above, $S_{\phi\phi}(f)$ for any value of f can be interpreted as $1/\Delta f$ times the time average power of $\phi(t)$ in the frequency band between $f$and $f + \Delta f$ in the limit as $\Delta f \to 0$. Hence, each value of $S_{\phi\phi}(f)$ represents a *power density* per Hz. In this case, $\phi(t)$ has units of radians, so $S_{\phi\phi}(f)$ has units of radians^2 per Hz.

Replacing $|FT\{\phi_T(t)\}|^2$ in (11) by the product of the right side of (12) and the complex conjugate of the right side of (12) and rearranging the result yields

$$S_{\phi\phi}(f) = \int_{-\infty}^{\infty} R_{\phi\phi}(\tau) e^{-j2\pi\tau f} d\tau, \quad (14)$$

where $R_{\phi\phi}(\tau)$ is given by

$$R_{\phi\phi}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T \phi(t)\phi(t+\tau) dt \quad (15)$$

and is called the *time average autocorrelation* of $\phi(t)$. Equation (14) implies that $S_{\phi\phi}(f)$ is the Fourier transform of the time average autocorrelation. Applying the inverse Fourier transform to (14) gives

$$R_{\phi\phi}(\tau) = \int_{-\infty}^{\infty} S_{\phi\phi}(f) e^{j2\pi\tau f} df. \quad (16)$$

It follows from (15) that the time average power of $\phi(t)$ is $R_{\phi\phi}(0)$, so (16) implies that the time average power of $\phi(t)$ is the integral of $S_\phi(f)$ over all frequencies.

The Fourier transform of any real-valued function is conjugate symmetric, and $|c| = |c^*|$ for any complex number c, so (11) implies that $S_{\phi\phi}(f) = S_{\phi\phi}(-f)$. Consequently, the one-sided time average power spectrum of $\phi(t)$, defined as

$$S_\phi(f) = 2S_{\phi\phi}(f) \text{ for } f \ge 0, \quad (17)$$

is often used. The factor of 2 ensures that the time average power of $\phi(t)$ is the integral of $S_\phi(f)$ over all positive frequencies.[‡]

As described above,

$$\mathcal{L}(f) = \frac{1}{2} S_\phi(f) \quad (18)$$

by definition. This definition is important because $\mathcal{L}(f)$ is what laboratory phase noise measurement instruments estimate. For reasons explained in Section III-A, when $\mathcal{L}(f)$ is expressed in decibels (dB), i.e., $10\log_{10}(\mathcal{L}(f))$, its units are *defined* to be dBc/Hz.

[‡]For the remainder of the paper, all *time average power spectra* are referred to as just *power spectra* for brevity.

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G. Spurious Tones

A signal or its power spectrum is said to contain a spur at a frequency f_m if the signal's power spectrum contains a Dirac delta function at f_m. The power of a phase error spur at frequency f_m is therefore given by

$$P_{spur} = \lim_{\varepsilon \to 0} \int_{f_m - |\varepsilon|}^{f_m + |\varepsilon|} S_{\phi\phi}(f) df \tag{19}$$

with units of radians^2.

Due to the symmetry of $S_{\phi\phi}(f)$ about $f = 0$, its spurs appear in pairs, e.g., a sinusoidal component $B\sin(2\pi f_m t)$ in $\phi(t)$ gives rise to two $B^2/4$-powered spurs, at frequencies f_m and $-f_m$. Nevertheless, the power of each spur is quantified separately by (19), a justification for which is explained in the next section.

As shown in Section IV, spurs are especially detrimental to the performance of wireless systems, so spur mitigation techniques in PLL-based oscillators are an active research topic [18]–[21].

III. Oscillator Signal Power Spectrum

A. Relationship to Phase Error Spectrum

As described in Section II, it is usually the case in practice that only the fundamental term of an oscillator signal (e.g., the $n = 1$ term in (8)) contributes to the oscillator signal's power spectrum in a wide bandwidth around $f = \omega_0/(2\pi)$, and in many applications $e(t)$ can be neglected. In these cases, the oscillator signal of interest has the form

$$v(t) = A\sin(\omega_0 t + \phi(t)) \tag{20}$$

where A is a constant amplitude.

Applying the angle sum trigonometric identity to (20) gives

$$v(t) = A\sin(\omega_0 t)\cos(\phi(t)) + A\cos(\omega_0 t)\sin(\phi(t)). \tag{21}$$

If $|\phi(t)| << 1$ for all t as is often the case for oscillators, applying the sine and cosine small angle approximations to (21) results in

$$v(t) \cong A\sin(\omega_0 t) + A\cos(\omega_0 t)\,\phi(t). \tag{22}$$

The first and second terms on the right side of (22) are the ideal oscillator signal and an additive noise term caused by oscillator phase error, respectively.

The power spectrum of $v(t)$ and its properties are given by (11)-(17) except with ϕ replaced by v. Given that the ideal oscillator signal term in (22) has zero bandwidth, the one-sided power spectrum of $v(t)$ for $f \neq \omega_0/(2\pi)$ only depends on the noise term. It follows from well-known Fourier transform properties and the power spectrum definition that the one-sided power spectrum of $v(t)$ can be written as

$$S_v(f) \cong \frac{A^2}{4} S_\phi\left(\left|f - \frac{\omega_0}{2\pi}\right|\right) \quad \text{for } f \neq \frac{\omega_0}{2\pi}. \tag{23}$$

This can be rearranged and combined with (18) to give

$$\mathcal{L}(f) \cong \frac{S_v\left(\frac{\omega_0}{2\pi} + f\right)}{A^2/2} \quad \text{for } f > 0. \tag{24}$$

The right side of (24) used to be the *definition* of $\mathcal{L}(f)$ [22]. When this was the case, (18) followed from this definition as an approximation. The old definition had the advantage that it was a proxy for $S_\phi(f)/2$ that could easily be measured directly from an oscillator signal's power spectrum. Unfortunately, the simple relationship between the old definition of $\mathcal{L}(f)$ and $S_\phi(f)$ breaks down unless $|\phi(t)| << 1$. Given that practical cases of interest exist for which $|\phi(t)| << 1$ does not hold, the definition was eventually changed to (18) [10].

The error term in (22) caused by oscillator phase error can be viewed as an amplitude modulated (AM) waveform with *carrier signal* $A\cos(\omega_0 t)$ and modulation signal $\phi(t)$. The time average power of the carrier signal is $A^2/2$, and for $f \neq \omega_0/(2\pi)$ the one-sided power spectrum of the AM waveform is $S_v(f)$. The portion of an AM waveform's power spectrum on either side of the carrier frequency is traditionally called a *sideband* of the signal. Therefore (24) implies that $\mathcal{L}(f)$ is approximately equal to the power density per Hz in a sideband of $v(t)$ at an offset of f from the carrier divided by the power of the carrier.[§]

It follows that 10 times the logarithm of the right side of (24) can be interpreted as having units of dBc/Hz, i.e., the power density per Hz in a sideband relative to the power of the carrier in dB. Therefore, with the old definition of $\mathcal{L}(f)$, the units of $10\log_{10}(\mathcal{L}(f))$ are dBc/Hz. This is not strictly true for the current definition of $\mathcal{L}(f)$, but for consistency, and because (24) holds approximately with the current definition, the units of $10\log_{10}(\mathcal{L}(f))$ are *defined* to be dBc/Hz.

If $S_\phi(f)$ contains a spur at f_m, the argument above can be repeated while integrating both sides of (23) over an ε-interval around $f_0 + f_m$ and applying (19). This shows that P_{spur} is equal to the power of the spur in $S_v(f)$ at $f_0 + f_m$, divided by the power of the carrier. Hence, the units of $10\log_{10}(P_{spur})$ are *defined* to be dBc.

By the symmetry of $S_{\phi\phi}(f)$, if $S_v(f)$ has a spur at $f_0 + f_m$ caused by oscillator phase error, it also has a spur of the same power at $f_0 - f_m$. Therefore, it might seem redundant to evaluate the power of each spur individually, e.g., as in (19). However, for reasons explained in Section VII, measurements of oscillator signal power spectra are seldom perfectly symmetric for frequency offsets above and below f_0, and therefore evaluating the power of each spur separately is not redundant in practice.

B. Continuous-Time Versus Discrete-Time Paradox

It is argued in Section II that only the samples of a squared-up oscillator signal's phase error at the oscillator signal's zero-crossing times, i.e., $\phi(t_n)$, affect the oscillator output waveform in the absence of $e(t)$ error. Yet it is argued in Section III-A that in many cases of interest the power spectrum of the fundamental term of such an oscillator signal is a function of the power spectrum of the continuous-time phase error waveform, $\phi(t)$. This apparent contradiction can be resolved as follows.

As described in Section II-C, a squared-up oscillator signal can be used in place of a sinusoidal oscillator signal provided the power spectra of the terms in the squared-up signal centered at integer multiples of $f_0 = \omega_0/(2\pi)$ do not overlap the power spectrum of the fundamental term centered at f_0. This requires that $S_{\phi\phi}(f)$ be bandlimited to a bandwidth that is lower than $f_0/2$. In such cases the definition of $S_{\phi\phi}(f)$ given by (11)-(13) implies that $FT\{\phi_T(t)\}$ is also bandlimited with this bandwidth in the limit as $T \to \infty$. It follows from the sampling theorem that $FT\{\phi_T(t)\}$ in (11) can be replaced

[§] Older literature often shows phase noise as $\mathcal{L}(\Delta f)$ to underscore this fact.

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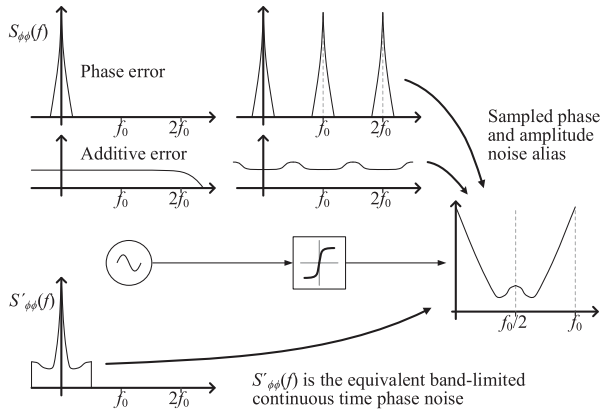


Fig. 7. Sampling behavior of the limiting amplifier on the oscillators phase and additive error.

by T_0 times the discrete-time Fourier transform of $\phi(nT_0)$ for $|f| < f_0/2$. Hence, in such cases

$$S_{\phi\phi}(f) = \begin{cases} \lim_{T\to\infty} \frac{T_0^2}{T} \left| \sum_{n=-\infty}^{\infty} \phi_T(nT_0)\, e^{-j2\pi f n T_0} \right|^2, & \text{if } |f| < \frac{f_0}{2}, \\ 0, & \text{otherwise.} \end{cases} \tag{25}$$

Provided the bandwidth of $S_{\phi\phi}(f)$ is sufficiently low, (10) implies that $\phi(\tau_n) \cong \phi(nT_0)$ to a high degree of accuracy. In such cases, it follows from (25) that $S_{\phi\phi}(f)$ can be expressed as a function of $\phi(t)$ sampled at the oscillator signal's positive-going zero-crossing times. A nearly identical argument shows that it can also be expressed as a function of $\phi(t)$ sampled at the oscillator signal's negative-going zero-crossing times. Thus, provided $|\phi(t)| << 1$, it follows from (17), (23), and (25) that $S_v(f)$ can be expressed as a function of $\phi(t_n)$ instead of $\phi(t)$.

C. Sampled Phase Error

The assumption that $S_{\phi\phi}(f) = 0$ for $|f| \geq f_0/2$, which led to (25), is usually acceptable in wireless transceivers, because the various signal paths in wireless transceivers typically have bandwidths much less than $f_0/2$ by design. In contrast, the assumption is rarely valid in clocked systems which generally lack equivalent band-limiting circuits. In such cases, (25) does not hold because sampling the phase error at a rate of f_0 causes aliasing.

A common approach to avoid this problem is to replace the actual phase error power spectrum, $S_{\phi\phi}(f)$, with a conceptual modified phase error power spectrum, $S'_{\phi\phi}(f)$, equal to the right side of (25). Even though $S'_{\phi\phi}(f) \neq S_{\phi\phi}(f)$ when $S_{\phi\phi}(f)$ is not bandlimited to $|f| < f_0/2$, $S'_{\phi\phi}(f)$ is bandlimited to $|f| < f_0/2$ and already contains all content that would have aliased into the frequency band $|f| < f_0/2$ had $S_{\phi\phi}(f)$ been sampled at a rate of f_0. Accordingly, $S'_{\phi\phi}(f)$ can be used in place of $S_{\phi\phi}(f)$ in all of this paper's results that relate the phase error power spectrum to f_0-rate samples of the phase error or, by extension, to absolute jitter.

Fig. 7 shows how this approach can be extended to handle broadband additive error that gets converted to phase error when a sinusoidal oscillator signal is amplified and clipped by a limiting amplifier to generate a squared-up oscillator signal. Both the broadband phase and the broadband additive error are sampled at the zero crossings of the oscillator signal. The limiting amplifier's wide bandwidth typically causes aliasing of many bands of broadband noise into the $|f| < f_0/2$ frequency band.

The conversion of additive error to phase error also affects the clock buffers which follow the limiting amplifier. The purpose of a clock buffer is to maintain the squared-up edges of the clock signal over long transmission distances, and therefore is susceptible to the same error-sampling effect discussed for limiting amplifiers. While each clock buffer may only contribute a small amount of phase error, in ICs such as network routers or FPGAs where GHz clocks are distributed several centimeters, their cumulative error usually dominates the oscillator's intrinsic phase error [23], [24].

The simulation methodology described in Section VI-A ensures that the sampling and conversion effects described above are properly captured, so that any amplitude error on the resulting squared-up clock signal can usually be ignored, as explained in Section II-B. The phase error power spectrum of this squared-up clock signal can then be "input-referred" as shown in Fig. 7 to generate the equivalent band-limited $S'_{\phi\phi}(f)$ which contains all the sampled noise.

Throughout the remainder of the paper, $S_{\phi\phi}(f)$ is used in equations that relate the phase error power spectrum to samples of the phase error or, equivalently, to jitter, as a proxy for either the actual phase error power spectrum or $S'_{\phi\phi}(f)$. In cases where the actual phase error is bandlimited to $|f| < f_0/2$, the reader should view $S_{\phi\phi}(f)$ as denoting the power spectrum of the actual phase error. Otherwise, the reader should view $S_{\phi\phi}(f)$ as denoting $S'_{\phi\phi}(f)$. In this way, the quantity denoted by $S_{\phi\phi}(f)$ in such equations is bandlimited to $|f| < f_0/2$ by definition.

D. Why $S_{\phi\phi}(f)$ Increases With Oscillator Frequency

As can be seen from (1) and (6), oscillator frequency, ω_0, and phase error, $\phi(t)$, are separate variables in both the sinusoidal and squared-up oscillator signal models. This separation obscures an implicit dependency of phase error on oscillator frequency that arises because phase error represents the oscillator's timing error as a fraction of its period but its period is inversely proportional to its frequency. For example, (10) implies that changing an oscillator's frequency by X dB without changing the mean squared value of its absolute jitter would increase its phase error power by $2X$ dB.

Indeed, it has been shown for many different types of oscillators that the effect of circuit noise on absolute jitter is relatively independent of the frequency to which a given oscillator is tuned [25]–[28]. In such cases, changing the oscillator's frequency does not significantly change the mean squared value of its absolute jitter.

This effect can cause confusion when comparing the phase noise performance of oscillators tuned to different frequencies. The confusion can be avoided by *normalizing* the phase noise of the oscillators to a common frequency prior to comparing their phase noise spectra. The phase noise of an oscillator normalized to a frequency ω_n is $(\omega_n/\omega_0)^2 S_{\phi\phi}(f)$ where ω_0 is the nominal frequency and $S_{\phi\phi}(f)$ is the phase noise spectrum of the oscillator. In general, the phase noise of two oscillators normalized to the same frequency will be approximately equal if they have equivalent jitter performance. For example, two oscillators, one with frequency ω_0 and phase error power spectrum $S_{\phi\phi}(f)$ and one with frequency $2\omega_0$ and phase error

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power spectrum $4S_{\phi\phi}(f)$ would have the same normalized phase noise power spectrum. Normalizing the phase noise spectra of different oscillators to a common frequency in this fashion allows for a fair phase noise performance comparison.

A commonly-used oscillator figure of merit (FOM) that implicitly performs this normalization is

$$FOM = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{\mathcal{L}(\Delta f)\,P}\right] \tag{26}$$

where $f_0 = \omega_0/(2\pi)$, Δf is any frequency offset, and P is the oscillator's power consumption in mW [25]. For instance, if an oscillator's frequency is doubled (increased by 3 dB) without changing its phase noise or power consumption, its *FOM* increases by 6 dB, which is consistent with the above discussion.

IV. Effects of Phase Error on Mixing

In wireless receivers, a mixer's input signal, $x(t)$, usually consists of a *desired signal* plus multiple unwanted signals at other frequencies called *interferers* or *blockers*. The interferers not only arise from unwanted signals received through the antenna, but they can also result from non-ideal circuit behavior. For example, in frequency division duplex (FDD) transceivers it is not possible to fully isolate the receiver from the transmitted signal, so a partially attenuated version of the transmitted signal appears to the receiver as an interferer.

Ideally, the mixer frequency-translates $x(t)$ such that the desired signal resides within the passband of the filter following the mixer, and the interferers are either suppressed by the filter or subsequently suppressed by digital filtering after analog-to-digital conversion. Unfortunately, oscillator phase error mixes with the interferers which can result in error that ends up in the same frequency range as the desired signal, thereby corrupting the desired signal and reducing the sensitivity of the receiver. This phenomenon is known as *reciprocal mixing*.

It follows from (9), (20), and (22) that the output of a typical mixer in the band of interest can be written as

$$y(t) = \frac{4}{\pi}\sin(\omega_0 t)\,x(t) + \frac{4}{\pi}\cos(\omega_0 t)\,\phi(t)x(t). \tag{27}$$

The first term on the right side of (27) represents the ideal behavior of the mixer, and the second term represents the effect of oscillator phase error. The sine and cosine factors in the two terms both perform the same frequency translations; the sine factor frequency-translates $x(t)$ by both $\omega_0/(2\pi)$ and $-\omega_0/(2\pi)$ Hz, and the cosine factor frequency-translates $\phi(t)x(t)$ by both $\omega_0/(2\pi)$ and $-\omega_0/(2\pi)$ Hz. Therefore, any portion of the power spectrum of $\phi(t)x(t)$ that overlaps the power spectrum of the desired signal portion of $x(t)$ causes reciprocal mixing error.

For example, suppose $x(t)$ contains a desired signal component centered at frequency f_d and an interferer centered at frequency f_i, and suppose $\phi(t)$ contains a spurious tone given by $B\sin[2\pi(f_d - f_i)t]$ where B is a constant. The spurious tone causes $\phi(t)x(t)$ in the second term of (27) to contain a copy of the interferer scaled by $B/2$ and centered at frequency f_d, which corrupts the desired signal component unless the power spectrum of the interferer times $B^2/4$ is sufficiently small that it can be neglected.

More generally, multiplication in the time domain is equivalent to convolution in the frequency domain, so the power spectrum of $\phi(t)x(t)$ has a non-zero component in the frequency range $f_d - \Delta f/2$ to $f_d + \Delta f/2$ if an interferer with bandwidth Δf is centered at frequency f_i and $S_{\phi\phi}(f - f_d)$ is non-zero for $f_i - \Delta f \le |f| \le f_i + \Delta f$. This component is centered on and therefore corrupts the desired signal component of $x(t)$. As illustrated in Fig. 8, if the interferer has a high-enough power relative to the desired signal, the reciprocal mixing error can be significant even when $S_{\phi\phi}(f - f_d)$ is small for $f_i - \Delta f \le |f| \le f_i + \Delta f$.

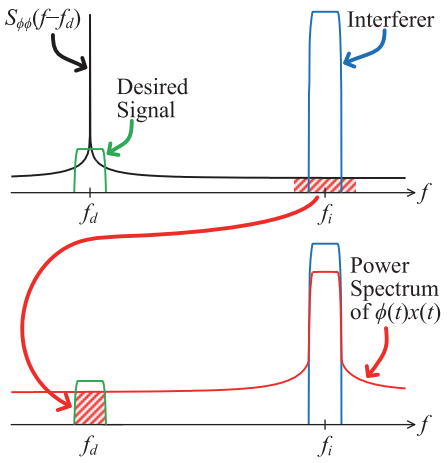


Fig. 8. Power spectra on a dBc/Hz scale of: the desired signal and an interferer in $x(t)$, $\phi(t)$ (frequency-shifted by f_d), and $\phi(t)x(t)$. Hash marks show a portion of $\phi(t)$ that causes reciprocal mixing error (top plot) and the resulting reciprocal mixing error (bottom plot).

Thus, reciprocal mixing error is caused by phase error mixing with interferers via the $\phi(t)x(t)$ term in (27), and the corresponding signal-to-noise ratio (SNR) over the desired signal band decreases with increasing interferer power. This often places stringent restrictions on the phase error, because interferers can be extremely powerful relative to the desired signal in typical wireless receivers.** For example, in LTE cellular handset receivers, interferers with $|f_i - f_d| \ge$ 10 MHz can be up to 87 dB more powerful than the desired signal [29].

Of course, the phase error also mixes with the desired signal component via the $\phi(t)x(t)$ term, and this causes error in the desired signal band too. In applications such as GSM handset receivers wherein the required SNR over the signal band is modest, this error is less problematic than reciprocal mixing error because the SNR does not decrease with increasing signal power. However, in receivers for high-order modulation formats, such as 256 QAM in LTE handset receivers, the required SNR over the signal band is high enough that close-in oscillator phase error, i.e., phase error below several MHz, becomes one of the most challenging oscillator specifications to meet [21].

Oscillator phase error also causes mixing error in wireless transmitters. Mixers are used in a wireless transmitter to frequency-translate the desired signal to the RF transmit frequency. As in receivers, each mixer behaves according to (27); it performs the same frequency translations on both its input signal, $x(t)$, and the phase error term, $\phi(t)x(t)$. After frequency translation, these signals have spectral shapes comparable to the interferer and $\phi(t)x(t)$ power spectra,

**Typically, large interferers occur relatively far from f_d, so they place stringent requirements on the *far-out* phase error, i.e., on the phase error power spectrum above at least several MHz.

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respectively, shown in the bottom plot of Fig. 8, except in this case f_i corresponds to the transmit frequency.

The combined signals are passed through a power amplifier and then bandpass filtered. Typically, the bandpass filter is a SAW filter or duplexer which attenuates the out-of-band portion of $\phi(t)x(t)$ by about 50 dB, but the amplification prior to filtering is often so high that the residual out-of-band emission from the term corresponding to $\phi(t)x(t)$ can still be significant. For example, in FDD transceivers, its overlap with the receive band can desensitize the receiver. This out-of-band emission phenomenon generally dictates the maximum far-out phase error that can be tolerated in a given application.

The close-in phase error results in the portion of the error power spectrum arising from $\phi(t)x(t)$ that overlaps the desired transmitted signal. As in receivers, this term can be problematic in applications that use high-order modulation formats such as the 256 QAM option in LTE handset receivers unless the close-in phase error is kept very low.

V. Jitter

In mixers it is convenient for the reasons described above to represent non-ideal oscillator behavior in terms of continuous-time phase error, $\phi(t)$. In most other applications, it is more useful to represent the non-ideal behavior in terms of the absolute jitter, $\Delta\tau_n$, as defined in (10), or quantities derived from the absolute jitter.

Like phase error, jitter typically consists of random and deterministic components. Accordingly, the modifiers *random* or *deterministic* are applied to jitter metrics in cases where the metrics represent only the effects of the random or deterministic components, respectively. The modifier *total* is also often used to indicate when a jitter metric represents the effects of both components, e.g., total absolute jitter is comprised of random absolute jitter and deterministic absolute jitter. Without a modifier, the total quantity is usually implied.

A. Jitter Density

In many clocked systems, the clock signal undergoes several frequency multiplications and divisions between its source and each circuit that it drives. In such cases, phase error is an inconvenient metric, because, as discussed in Section III-D, it increases with clock frequency. To avoid the tedium of scaling phase error after every frequency translation, a normalized power spectrum called jitter density and defined as

$$J(f) = \frac{1}{\omega_0^2} S_\phi(f) \tag{28}$$

is often used in place of the phase error power spectrum when analyzing such systems. Jitter density is so-named because for $f < f_0/2$ it is proportional to the single-sided discrete-time power spectrum of the absolute jitter sequence, $\Delta\tau_n$. This can be seen by dividing both sides of (25) by ω_0^2, and using (10) and the symmetry property (17). The units of $\Delta\tau_n$ are seconds, so the units of $J(f)$ are seconds^2 per Hz.

The jitter densities of oscillator signals at different nominal frequencies do not need to be normalized to a common frequency for comparison as would be necessary for the corresponding phase error power spectra, because the normalization is built into the definition of jitter density. This property simplifies many practical computations as demonstrated in the following sections.

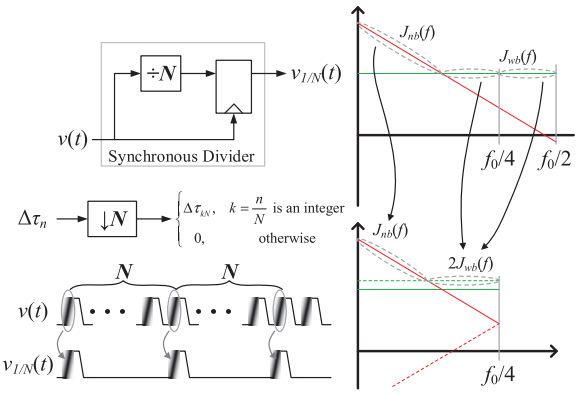


Fig. 9. Divide-by-N circuit block diagram and effect on input clock jitter.

B. Jitter of Divided Clocks

A clock divider that reduces the frequency of its input clock by an integer factor, N, is a fundamental building block in many clocked systems. As shown in Fig. 9, such a clock divider typically consists of edge-selection logic, i.e., an N-fold digital divider driven by the oscillator signal, $v(t)$, followed by a retiming flip-flop. The retiming operation renders the absolute jitter of the output clock signal insensitive to noise and other non-ideal circuit behavior within the edge-selection logic, thereby isolating the jitter-contributing circuitry to just the retiming flip-flop. To the extent that the absolute jitter added by the retiming flip-flop is negligible, the output clock signal's absolute jitter is approximately equal to a sub-sampled version of the input clock signal's absolute jitter.

The jitter density of a typical clock signal has regions with different slopes [30]. The top right plot in Fig. 9 shows the jitter density of the divider's input clock, where the sloped regions have been simplified into a single low-frequency (close-in) sloped region with jitter density $J_{nb}(f)$, and a broadband (far-out) flat region with jitter density $J_{wb}(f)$. The bottom right plot in Fig. 9 shows the jitter density of the divider's output clock signal for the case of division by 2 (i.e., $N = 2$). In this example, the power of the input clock signal's close-in jitter density falls far below the power of the far-out jitter density in the frequency band $[f_0/4,\ f_0/2)$, so the aliased contribution of the close-in jitter density to the jitter density of the output clock signal is negligible. The far-out jitter density of the output clock signal is, however, doubled in power because of aliasing introduced by the sub-sampling.

Generalizing this example to N-fold division, the output clock's close-in jitter density remains that of the input clock, whereas its far-out jitter density is N times that of the input clock. In theory, it is possible for the division ratio, N, to be large enough that aliasing of the close-in jitter density is non-negligible, but this rarely happens in practical low-jitter circuits.

C. Integrated Jitter

In some applications, the mean squared value of the absolute jitter, i.e., the time average of $(\Delta\tau_n)^2$, is of interest. This can usually be related to the phase error spectrum as shown below.

Equation (25) can be rearranged as

$$S_{\phi\phi}(f) = T_0 \sum_{k=-\infty}^{\infty} R_{\phi\phi}[k] e^{-j2\pi f k T_0}, \quad \text{for } |f| < \frac{f_0}{2} \tag{29}$$

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where

$$R_{\phi\phi}[k] = \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} \phi\left(nT_0\right) \phi\left(\left(n+k\right) T_0\right). \quad (30)$$

The summation on the right side of (29) has the form of a discrete-time Fourier transform. Applying the inverse discrete-time Fourier transform equation gives

$$R_{\phi\phi}[k] = \int_{-\infty}^{\infty} S_{\phi\phi}\left(f\right) e^{j2\pi f k T_0} df. \quad (31)$$

It follows from (30) that the mean squared value of $\phi(nT_0)$ is $R_{\phi\phi}[0]$, so (31) implies that the mean squared value of $\phi(nT_0)$ is equal the integral of $S_{\phi\phi}(f)$ over all frequencies. To the extent that $\phi(\tau_n) \cong \phi(nT_0)$, this with (10) implies that the mean-squared value of the absolute jitter is given by

$$\sigma_{abs}^2 = \frac{1}{\omega_0^2} \int_{-\infty}^{\infty} S_{\phi\phi}\left(f\right) df = \frac{1}{\omega_0^2} \int_{0}^{\infty} S_{\phi}\left(f\right) df. \quad (32)$$

This and other mean-squared quantities derived from the absolute jitter that are defined in the next section are often stated as their square-root equivalents, i.e., the root-mean-squared (rms) absolute jitter σ_{abs}.

Section III-C defined the use of $S_\phi(f)$ in this paper as a proxy for either the one-sided power spectrum of the continuous-time phase error, or $S'_\phi(f)$, the conceptual modified power spectrum. As explained in that section, clocked circuits tend to contain sources of broadband noise which result in broadband jitter, and the applications which they serve also tend to have wide bandwidths. For these reasons, it is almost always $S'_\phi(f)$ that is used in applications that specify jitter. Irrespective of whether $S_\phi(f)$ or $S'_\phi(f)$ is appropriate, both are bandlimited to the frequency range [0, f_0/2). Therefore, (32) can be rewritten as

$$\sigma_{abs}^2 = \frac{1}{\omega_0^2} \int_{0}^{f_0/2} S_{\phi}(f) df = \int_{0}^{f_0/2} J(f) df. \quad (33)$$

Actually integrating the jitter density down to $f = 0$ would yield an unbounded result in practice, because oscillator phase error power spectra (and correspondingly, jitter density) tend to be unbounded at low frequencies [30]. Usually this is not a practical concern, though, as many clocked systems are designed to be insensitive to low-frequency jitter density. For example, transmitter-receiver pairs in serial communication links use PLL-based oscillators and clock and data recovery (CDR) circuits configured in a manner that effectively bandpass-filters the transmitter clock jitter density before it reaches timing-sensitive circuits in the receiver [31].

Hence, in practice the integration limits of 0 and f_0/2 in (33) are usually replaced by limits that are greater than 0 and less than f_0/2, respectively. In particular, integration limits of 12 kHz to 20 MHz are widely used. These limits were first seen in the specifications for the PLL-based oscillators designed for the synchronous optical network (SONET) [32]. They have since proliferated to applications where they no longer have any architectural significance, but because most PLL-based oscillators have qualitatively similar phase error power spectra, they provide a useful means by which to quickly compare the performance of different PLL-based oscillators.

In some applications, it is of interest to evaluate the contribution of a phase error spur at a particular frequency to σ_{abs}^2. It follows from (33) that this contribution can be written as

$$\sigma_{abs-spur}^2 = \frac{1}{\omega_0^2} \lim_{\varepsilon\to 0} \int_{f_m-|\varepsilon|}^{f_m+|\varepsilon|} S_{\phi}(f) df \quad (34)$$

where f_m is the frequency of the spur. Hence, (17) and (19) imply that

$$\sigma_{abs-spur}^2 = \frac{2}{\omega_0^2} P_{spur} = \frac{2}{\omega_0^2} 10^{P_{dBc}/10} \quad (35)$$

where P_{dBc} is the spur power in units of dBc, obtained through measurements as described in Section VII.

D. Other Jitter-Based Metrics

In typical clocked digital circuits, multiple flip-flops whose inputs and outputs are interconnected through combinational logic are driven by the same clock signal. Each timing path in such a digital circuit is defined as a path that begins at the output of a flip-flop, passes through combinational logic, and ends at the input of a flip-flop. Correct functionality of the overall digital circuit requires that the maximum delay among all such timing paths, which is called the *critical path delay*, is less than the minimum clock period. The minimum clock period depends on the jitter: the higher the jitter the lower the minimum clock period and, therefore, the lower the maximum possible clock frequency of the digital circuit.

In particular the variation of a clock signal's period from its nominal value, i.e., $\Delta\tau_n - \Delta\tau_{n-1}$, is the jitter metric of interest. It is called *period jitter*, and is frequently used in place of absolute jitter to specify the performance of clock signals for digital circuits.

The concept of period jitter can be generalized to *accumulated jitter*, which is also known as *N-cycle*, or *long-term jitter*. Accumulated jitter is defined as the variation of the time interval spanned by a clock edge and the Nth edge preceding it minus N times the nominal period, so it can be expressed as $\Delta\tau_n - \Delta\tau_{n-N}$. Thus, accumulated jitter for $N = 1$ is just period jitter.

By definition, accumulated jitter is equivalent to absolute jitter passed through a discrete-time filter with transfer function $1 - z^{-N}$, so its mean squared value can be written as

$$\sigma_{acc}^2(N) = \int_{0}^{f_0/2} \left|1 - e^{-j2\pi N f/f_0}\right|^2 J(f) df. \quad (36)$$

E. Effects of Jitter on Analog to Digital Conversion

A common use of precision oscillators is the clocking of ADCs. The operation of many ADCs can be abstracted into two sequential operations. The first operation is sampling the continuous-time, continuous-valued input signal, $x(t)$, at a discrete set of times defined by the oscillator, τ_n. The second operation is quantizing the sequence of continuous-valued samples, $x(\tau_n)$, into a sequence of digital codes. In many ADC architectures, the second operation is insensitive to clock jitter, so only the initial sampling operation is analyzed here [33].

Fig. 6 shows a simplified input sampling circuit. Ignoring all non-idealities except clock jitter, the nth sample of the input voltage is given by $y[n] = x(nT_0 + \Delta\tau_n)$. Equation (10) implies that the $|\phi(t)| << 1$ assumption made in previous sections is equivalent to $|\Delta\tau_n| << T_0$. Assuming $x(t)$ is bandlimited to prevent aliasing, the sampling error caused by

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jitter can be approximated as $y[n] \cong x(nT_0) + x'(nT_0) \cdot \Delta\tau_n$, where $x'(t)$ is the first derivative of $x(t)$.

Even with these assumptions and approximation, the jitter-induced error, $x'(nT_0) \cdot \Delta\tau_n$, is hard to analyze without simulation. Textbooks typically consider a worst-case scenario in which $x(t)$ is a maximum-frequency, maximum-amplitude sinusoid, $x(t) = A_{max} \sin(\omega_x t)$ [33]. In this case, the sampled voltage error is approximately $A_{max}\omega_x \Delta\tau_n \cos(\omega_x\, nT_0)$. Thus, prior to quantization, this jitter-induced error already sets an upper bound on the maximum achievable SNR given by

$$SNR_{max} = 10\log_{10}\left(\frac{\frac{1}{2}A_{max}^2}{\frac{1}{2}A_{max}^2\omega_x^2\sigma_{abs}^2}\right) = 10\log_{10}\left(\frac{1}{\omega_x^2\sigma_{abs}^2}\right). \tag{37}$$

Restricting $x(t)$ to be a single sinusoid makes the analysis tractable, but it has been shown empirically that the SNRs of ADCs with broadband input signals achieve much higher performance than the single-tone result would suggest [34]. Yet (37) remains useful as pessimistic performance bound.

Moreover, σ_{abs}, the clock quality metric on which SNR_{max} depends, is often used instead of $S_\phi(f)$ to stipulate the required ADC clock quality in applications. When an ADC's input signal, $x(t)$, is broadband, the error caused by jitter, i.e., $x(nT_0 + \Delta\tau_n) - x(nT_0)$, tends to be spread across the Nyquist band in a way that does not depend strongly on the shape of $S_\phi(f)$, so σ_{abs} is a more convenient metric. Notable exceptions are software-defined and reconfigurable radios in which ADCs capture broad spectrum signals, but the constituent desired signals and interferers each occupy relatively narrow bandwidths [35]. In such cases, $S_\phi(f)$ is required to characterize the full radio performance [36].

F. Jitter Histograms

Equation (33) provides a means with which to calculate σ_{abs} from $J(f)$, but it is possible to approximate σ_{abs} without knowing $J(f)$ by plotting a histogram of the $\Delta\tau_n$ sequence. The histogram provides an estimate of the probability distribution of $\Delta\tau_n$ from which σ_{abs} can be calculated directly. This is useful in applications like ADC clocking wherein $J(f)$ is not particularly useful. Furthermore, with reasonable assumptions on the sources of the random and deterministic absolute jitter contributions to the total absolute jitter, it is possible to estimate the relative magnitudes of their contributions [37].

For many clocked systems, jitter histograms are also a useful visualization of clock signal phase error. For example, in a serial communication receiver there is a circuit which samples incoming data at time intervals controlled by a sampling clock. As described in Section VII-C, it is usually possible to observe the waveforms of the data and sampling clock in the time domain. Knowing the histogram of the sampling clock jitter shows the distribution of when the data is sampled in time, which is usually informative because realistic absolute jitter histograms are non-Gaussian. In contrast, simply calculating σ_{abs} by integrating $J(f)$ would give no information on the distribution of $\Delta\tau_n$.

VI. Phase Error Simulation

In principle, an oscillator's phase error could be estimated via transistor-level transient simulations. However, this is rarely practical, even with present-day high-performance computers. The difficulty arises from the large timescales necessary to capture phase error quantities of interest. For example, to measure the phase error of a 1 GHz oscillator down to 1 kHz would require running a transient simulation for one million oscillator periods just to capture a single period of a 1-kHz phase error component.

For the past few decades, simulation methods have been available that greatly accelerate the analysis of relatively simple circuits that generate and process periodic signals, such as oscillators and clock buffers. While such methods are much faster than direct transient simulation, they have limitations, as described below, which make them generally inapplicable to the simulation of larger systems such as PLL-based oscillators.

For larger systems, it is more common to use the data generated in block transistor-level simulations to develop behavioral models, which are then used to simulate the complete system in an event-driven simulator. As explained below, event-driven simulators are ideally suited for simulating large systems that process discrete events, such as an oscillator's zero crossings.

A. Transistor-Level Simulation

To perform a phase noise or random jitter simulation, the simulator must first compute the circuit's periodic steady state, which is comprised of the periodic waveforms at the various circuit nodes after all transient settling effects have died out. For example, when an oscillator with a high-Q resonator is started, it usually takes many cycles for the oscillation envelope to stabilize. In contrast, a clock buffer driven by an external clock signal may only need a few cycles to stabilize [38]. There are two main techniques used to compute this solution: *shooting* and *harmonic balance* [39]–[41].

The shooting method is a time-domain approach wherein the circuit is iteratively simulated over a time interval equal to the expected period. After each iteration, the differences between the circuit's initial and final states are measured, and the initial state for the next iteration is modified. This process continues until the circuit's final state is equal to its initial state, indicating the periodic solution is achieved [39]. The majority of the computation time is spent on transient simulations, so this method is especially effective for circuits with short periodicities, e.g., multi-GHz RF oscillators. Moreover, as the waveforms are computed in the time-domain, sharp transitions resulting in broadband frequency-domain content, such as occur in ring oscillators and CMOS clock buffers, are not problematic [42].

In contrast, harmonic balance is considered a frequency-domain method. The circuit is first divided into two partitions, one containing all the linear elements, and another containing the nonlinear elements. The simulator iteratively solves for the voltages at, and current through, the nodes at the interface between these two partitions. Given an initial guess at the node voltages, the currents into the linear partition are solved in the frequency domain, which are computed using simple matrix multiplications. This is much faster than a transient simulation which requires iteratively solving differential equations. The currents into the nonlinear partition are solved by first applying the Inverse-Fast-Fourier Transform (IFFT) to the node voltages, computing the currents in the time domain, then returning them to the frequency domain via the FFT. By Kirchoff's current law, the current into the linear partition must equal the current leaving the nonlinear partition, so the simulator iterates until this condition is satisfied.

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The computation of the nonlinear currents is cumbersome, but the huge speed advantage gained in the frequency-domain computation of the linear currents gives the harmonic balance method an overall advantage for circuits which are weakly nonlinear, only have a few nonlinear elements, or have extremely long periodicities. For weakly nonlinear circuits, the overhead of the FFT and IFFT operations is modest because the circuit solution can be represented by only a few harmonics in the frequency domain, and by having few nonlinear elements, the quantity of time-domain computations is reduced. For circuits with long periodicities, to achieve a given accuracy the harmonic balance method is usually more efficient than the shooting method because it does not suffer from accumulated numerical noise which plagues long transient simulations. Ideal candidates for harmonic balance analysis are low-noise, extremely high-Q systems such as crystal oscillators [42].

Regardless of how the circuit's periodic steady state solution is calculated, the second step in a phase noise or random jitter simulation is to use this solution to compute how the different circuit noise sources contribute to voltage noise on the periodic signal at a chosen node. This method takes advantage of the periodicity of the signals within the circuit so that the effect of very low frequency circuit noise can be analyzed using only a single period of the circuit's behavior [43], [44].

The distinctions made in the above discussion regarding the types of circuits best suited to either the shooting or harmonic balance methods were more critical when these methods were first developed. However, the rapid improvement in simulation and computer technology over the intervening decades has blurred this separation. While there do still exist specialized problems which are better served by one or the other method, there are now general-purpose industry-standard simulation tools based on both methods, as well as hybrid methods [45], [46].

Moreover, while early incarnations of these simulators only estimated the raw signal power spectrum, present-day simulators are able to estimate both phase and amplitude error power spectra, and decompose the spectra into upper- and lower-sideband contributions [47]. Furthermore, provided the necessary information, they can accurately compute the modified phase error power spectrum resulting from sampling and/or noise folding, as discussed in Section III.C [48].

Simulation technology has reached a level of maturity where the simulator tool is typically no longer the design bottleneck. Rather, assuming the device models are accurate, most analysis errors are the result of improper or incomplete simulation methodology. For example, a complete clock distribution system comprised of an oscillator, limiting amplifier, and clock buffers is usually still too large to be simulated efficiently in one circuit. Rather, it is partitioned into sections which are simulated independently. Unfortunately, oscillators and buffers tend to be extremely sensitive to the circuits they drive, and buffers additionally tend to be sensitive to the circuits that drive them [49], [50]. Therefore, realistic driving and loading conditions must be included when simulating each partition.

In particular, the oscillator and its limiting amplifier is a critical combination, as the interface between them is especially susceptible to broadband additive noise to phase noise conversion. When simulating the jitter of an oscillator and its limiting amplifier, the clock buffer following the limiting amplifier should be included. This only serves as a realistic load, for reasons described above, as the simulation analysis is performed on the clock signal at the output of the limiting amplifier.

In spite of the advancements in simulator technology, there are still situations where simulating the combined oscillator and limiting amplifier can cause the simulator to have convergence issues. For example, this often occurs when simulating a high-Q crystal oscillator driving a CMOS limiting amplifier. For the reasons discussed above, the oscillator and its limiting amplifier are optimally simulated using the harmonic balance and shooting methods, respectively, so their combination is challenging for either simulator. In this situation, what is often done is to perform separate simulations on each block, while loading the oscillator with an approximation of the CMOS buffer load, and driving the CMOS buffer with an approximation of the oscillator's sinusoidal output. The two results are then added in power to represent the total phase noise at the CMOS buffer's output.

When simulating clock buffer chains, their layout strongly influences the clock signal waveforms, which in turn influences their jitter performance. It is therefore important to electromagnetically model the interconnect between the clock buffers, including both the signal and ground return path, to account for potential transmission-line effects that are not accurately captured in RC parasitic extractors [51]. The results from electromagnetic simulators are invariably high-order frequency-domain models in the form of s- or y-parameters. Such models are most efficiently simulated in their native form using the harmonic balance method. Alternatively, their dominant effects can usually be captured in lumped element models to be used with transient-based simulators, and some simulators can automatically perform this conversion [46], [47].

Clock buffer chains are also highly sensitive to their power supplies and power distribution networks. This includes the interconnect between the clock buffers' voltage regulators, the voltage regulators themselves, and even the package models. Clock buffer supply current waveforms usually have broadband content at frequencies well beyond a voltage regulator's bandwidth. At these high frequencies, there are often parasitic resonances. Therefore, accurate clock buffer simulations require not only the circuits and their drivers and loads, but electromagnetic models of their complete on-chip environment, and their supply circuitry as well [52]–[54].

B. Behavioral Simulation

There are two major obstacles to using the simulation methods described above for more complicated systems such as PLL-based oscillators. The first obstacle is that a periodic steady-state solution must exist and be computed [42]. This precludes the simulation of fractional-N type PLL-based oscillators, as well as systems which use digitally-generated pseudorandom dither, because such circuits tend to have extremely long periods (e.g., several days) [48]. The second obstacle is that even in cases where the period is relatively small, the complexity of a complete PLL-based oscillator imposes impractical processing and memory requirements, and even when these resources are available, computing the periodic steady-state solution can still take days. This simulation methodology would provide little utility during the design phase, where many iterations usually are required.

A more practical method for simulating PLL-based oscillators is to use behavioral event-driven simulations [55]–[57]. These simulations offer a huge speed advantage over transient

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transistor-level simulations, because behavioral event-driven simulations only capture the relevant functionality of circuits rather than all of the voltages and currents of every node with very small time steps. For example, a transistor-level oscillator simulation iteratively solves differential equations to compute many points per period of the oscillator waveform. Yet, as has been argued throughout this paper, many circuits driven by an oscillator signal are insensitive to the oscillator signal at times other than its zero crossings. Therefore, PLL-based oscillators are almost always behaviorally-modeled by generating the sequence of their rising or falling zero-crossing times, τ_n. This sequence can be processed using (10) and (25) to generate the conceptual band-limited phase error power spectrum, $S'_{\phi\phi}(f)$. Even though the shape of the oscillator signal waveform is lost in a behavioral simulation, many non-idealities such as noise and nonlinearity can still be accurately modeled [55]–[59].

The main drawback of behavioral event-driven simulations is that their results are only as accurate as their behavioral models of the circuit's sub-blocks. Care is therefore required to continually cross-verify the behavioral models against transistor-level simulations of the corresponding circuit sub-blocks.

Mixed-signal simulators, or *co-simulators*, bridge the gap between the speed of behavioral event-driven simulators and the functional accuracy of transistor-level simulators [60]. A co-simulator can efficiently simulate a system comprised of transistor circuits, behaviorally-modeled circuits, and fully-digital circuits. The behavioral models are written in a mixed-signal language such as Verilog-AMS, while the digital circuits can be described in Verilog. The co-simulator partitions the system into its different types, and runs simulators optimized for each type in lock-step. Data between the simulated partitions is continually communicated, so that the whole system is simulated in unison.

The power of a co-simulation is that a design can start with all behavioral models, and then transistor-level circuit blocks can be used in place of the corresponding behavioral models as they are designed. As different combinations of transistor-level circuits and behavioral models can be run, this implicitly improves the behavioral model verification. Unfortunately, because the analog portions of the system are simulated with a transistor-level simulator, co-simulations still take orders of magnitude more simulation time than fully behavioral simulations.

VII. Phase Error Measurement

A. Spectrum Analyzers

A spectrum analyzer performs the equivalent of passing its input signal through a bandpass filter whose center frequency is swept across a user-defined range of frequencies, called the *span*.[††] This frequency-swept bandpass filter is called the *equivalent bandpass filter*. The power of the equivalent bandpass filter's output signal is measured, and this power is plotted on the spectrum analyzer display's vertical axis on a dB scale against the equivalent bandpass filter's center frequency on the horizontal axis. The bandwidth of the equivalent bandpass filter is called the *resolution bandwidth* (RBW), and the time it takes for the equivalent bandpass filter's center frequency to traverse the span is called the *sweep time*.

If the spectrum analyzer input is driven by an oscillator signal, then the displayed power on the spectrum analyzer at a frequency f is equal to the power of the oscillator signal in the frequency band $(f - \text{RBW}/2, f + \text{RBW}/2)$. This is proportional to an estimate of the power spectrum of the oscillator signal, $S_v(f)$, as described in Section II-F. The accuracy of this estimate improves as the RBW decreases.

If the assumptions that $\varepsilon(t) \cong 0$ and $|\phi(t)| << 1$ made in Section III-A are valid, then (23) can be used to estimate $S_\phi(f)$ from $S_v(f)$. As oscillator phase error power spectra tend to rise at low frequencies, this approximation becomes invalid at very low offsets from the carrier [61]. Extremely low frequency oscillator phase error is indistinguishable from frequency drift, which can also corrupt spur measurements, as explained shortly.

Most spectrum analyzers have modes specifically for phase *noise* measurement which perform the carrier power normalization and apply any instrument-specific correction factors automatically. Examples of correction factors include accounting for the exact transfer function of the equivalent bandpass filter, and accounting for non-idealities in the power detector that follows the equivalent bandpass filter [62], [63].

If amplitude error is not negligible, then replacing A with $[A+\varepsilon(t)]$ in (20) results in an extra additive term $\varepsilon(t)\sin(\omega_0 t)$ in (22). Furthermore, any additive error on the oscillator signal will also appear in its power spectrum. Therefore, the oscillator signal power spectrum contains both amplitude error as well as additive error, and these errors are indistinguishable from phase error in $S_v(f)$. This results in a pessimistic estimate of $S_\phi(f)$ from $S_v(f)$.

The full form of the right side of (22) including amplitude modulation is the carrier signal plus $\varepsilon(t)\sin(\omega_0 t) + A\cos(\omega_0 t)\phi(t)$, where $\varepsilon(t)$ and $A\phi(t)$ can be viewed as complex modulation of the carrier. Therefore, when the oscillator signal has both phase and amplitude error, the sidebands of its power spectrum are no longer symmetric, in contrast to the case of pure phase error described in Section III-A. Parasitic coupling in both the circuit as well as the measurement setup can result in amplitude modulation of the oscillator signal, leading to such asymmetries. This effect is often noticeable in the spurious tones of PLL-based oscillators.

As explained in Section III-A, the power of a spur in the oscillator phase error power spectrum at frequency f_m is equal to the power of the spur in the oscillator signal power spectrum at frequency f_0+f_m, divided by the power of the carrier. Thus, the phase error spur power in dBc can be read from a dB-scale oscillator signal power spectrum as the difference between the values of the power spectrum at $f_0 + f_m$ and f_0.

However, there is a caveat to this spur measurement technique. As described above, the value of the spectrum analyzer measurement at frequency $f_0 + f_m$ is the power at the output of the conceptual RBW-bandwidth bandpass filter centered at frequency $f_0 + f_m$. Therefore, the measured power is approximately the sum of the spur power plus the oscillator signal noise power density integrated over the band $(f_0+f_m-\text{RBW}/2,\ f_0 + f_m + \text{RBW}/2)$. As the power of the spur of interest decreases, the RBW must be decreased so that the measured power at that frequency is dominated by the spur power, not the integrated noise power.

The left plot in Fig. 10 shows a PLL-based oscillator's signal measured power spectrum over a 100 kHz span centered at the 2.4 GHz carrier frequency, measured by a Rohde & Schwarz FSW13 spectrum analyzer. Symmetric spurs are visible at

[††]This is a behavioral description, not an explanation of how spectrum analyzers are implemented (a good explanation of which can be found in [17]).

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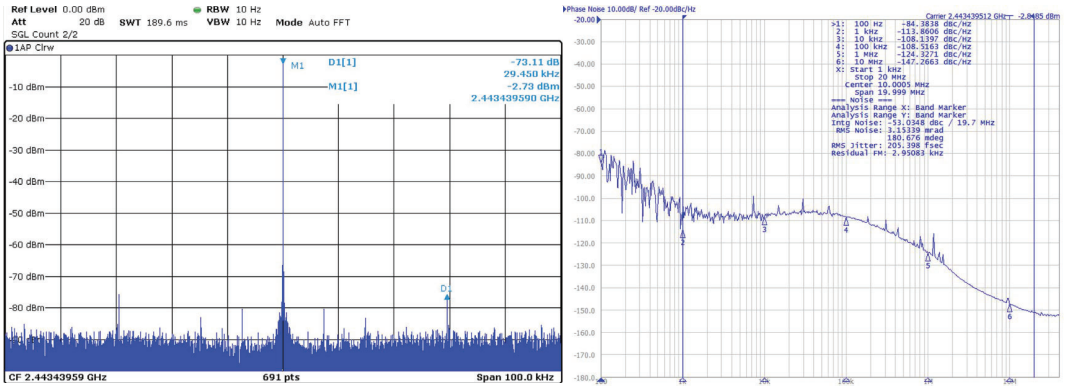


Fig. 10. Measured power spectra of a PLL-based oscillator signal (left) and its phase noise (right).

approximately 7.4, 14.7, and 29.5 kHz offsets from the carrier, with the largest shown by the delta marker as −73 dBc. The phase noise of this PLL-based oscillator in the 10 kHz to 100 kHz region is known to be −108 dBc/Hz. However, because this measurement was taken with a 10 Hz RBW and without averaging, any spur below about −80 dBc would become indistinguishable from the noise, so to resolve a lower-power spur would require a narrower RBW.

Unfortunately, narrow RBWs can complicate spur measurements and lead to erroneously optimistic results, because the time it takes for the spectrum analyzer to measure the power at the output of the equivalent bandpass filter increases as the RBW decreases. Oscillator frequency drift may cause the spur frequency to drift in the measurement. Often, this has the effect of spreading the spur power across a range of frequencies that can extend beyond the bandwidth of the spectrum analyzer's conceptual bandpass filter, thereby underestimating the spur power. Moreover, because frequency drift varies randomly over time, its effect on a spur may differ from its effect on the carrier, as they are measured at different points during the sweep time. These effects can cause spur power measurement to be optimistic, often by several dB.

The above discussion also explains why it is necessary to disable spectrum analyzer averaging when measuring spurs. Spectrum analyzer averaging causes the instrument to average the results of multiple sequentially captured measurements. This mode is useful for increasing the precision of noise measurements. Unfortunately, oscillator frequency drift causes the spur to appear at different frequencies across different measurement sweeps. When these results are averaged, the resulting spur power is reduced as it is averaged with noise, and just as explained above, the averaging may affect the spur power and carrier power differently, due to any randomness in the frequency drift.

Most spectrum analyzers implement the conceptual bandpass filtering operation described above by either downconverting the input signal to a fixed intermediate frequency and passing the result through a fixed-frequency bandpass filter, or digitizing the input signal and performing fast Fourier transform (FFT) based spectrum estimation [17]. Either way, the accuracy of the center frequency of the conceptual bandpass filter depends on the accuracy of the spectrum analyzer's local oscillator frequency, which, in turn, depends on the accuracy of the spectrum analyzer's reference oscillator frequency. Most spectrum analyzers offer the option of using an external reference oscillator signal. When measuring PLL-based oscillator phase error spurs, this feature makes it possible to lock the spectrum analyzer's local oscillator to the PLL-based oscillator's reference oscillator [62]. In this case, the spectrum analyzer's local oscillator has the same frequency drift as the PLL-based oscillator, which avoids the spur-measurement problem described above.

B. Phase Noise Analyzers

The lowest-noise phase noise measurements are made with phase noise analyzers, which are also called signal source analyzers depending on the manufacturer. Phase noise analyzers are essentially extremely sensitive receivers, and are capable of differentiating between the amplitude and phase noise components of an oscillator signal over a limited bandwidth [64].

Two different measurement techniques are commonly used, homodyne phase discrimination and heterodyne frequency discrimination [65]. The phase discrimination method is typically called narrowband-optimized mode, as it is optimized for measuring the close-in phase noise of oscillators with very little frequency drift, such as crystal oscillators and PLL-based oscillators locked to crystal oscillators. The frequency discriminator method is often called wideband-optimized mode, and is better-suited to measure the phase noise of oscillators with relatively high low-frequency phase noise or frequency drift, such as free-running voltage-controlled oscillators. Both of these measurement methods are further improved by correlation techniques, which essentially average out the uncorrelated noise between multiple identical measurement channels inside the instrument [66]. The total added noise from these instruments can be less than 10 femtoseconds of integrated jitter.

The right side of Fig. 10 shows the phase noise plot of the same PLL-based oscillator discussed in the previous subsection, as measured by a Keysight E5052B signal source analyzer. For the reasons given in the previous section, the averaging techniques used by this instrument to improve the noise measurement precision adversely affects its ability to resolve spurs. For example, the spurs at 7.4, 14.7, and 29.5 kHz in the left-side power spectrum are also visible in the phase noise plot, but their powers are not directly readable as they are spread over a range of frequencies.

C. Time-Domain Methods

For serial communication applications, phase error is usually measured in the time domain with high-speed digitizing oscilloscopes, as they can make measurements that would

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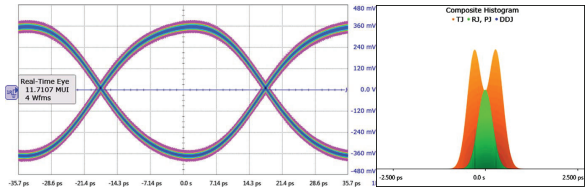


Fig. 11. Measured 14 GHz clock eye diagram and jitter histogram.

be impossible with other instruments [67]. Digitizing oscilloscopes fall into two categories, *realtime* and *sampling* (also called equivalent-time). A realtime oscilloscope operates like a digital version of a traditional analog oscilloscope, in that continuous segments of the input signal are digitized and displayed onscreen. The maximum bandwidth of the input signal is limited by the sample-rate of the ADC, which is currently up to well over 100 GS/s [68].

Realtime oscilloscopes often have internal configurable zero-crossing detectors, so that finite-duration segments of the oscillator signal absolute jitter can be extracted. An absolute jitter sequence can be processed via an FFT, which, by (25), gives an estimate of the oscillator phase error's modified conceptual power spectrum. An absolute jitter sequence can also be viewed as a histogram, and by analyzing the histogram as described in Section V-F, various aspects of the type and magnitude of the jitter can be inferred.

Fig. 11 shows measurement results for a 14 GHz clock signal via a Keysight DSAZ634A realtime oscilloscope. The clock signal was generated by a 28 Gb/s serial transmitter, transmitting a repetitive "01" sequence. The left plot in Fig. 11 is comprised of over 11 million segments of the measured clock waveform shifted and overlaid atop one another, in a plot known as an eye diagram [69]. The right plot in Fig. 11 shows the histogram of the clock signal's zero crossings. It shows the total jitter, random jitter, and two additional terms: periodic jitter (PJ) and data-dependent jitter (DDJ). The complete categorization of jitter used by this instrument is described in [70].

A realtime oscilloscope's unique ability to debug circuit problems in the time domain is particularly valuable in that it makes it possible to compare, edge by edge, the absolute jitter on a clock signal against other signals in the system. For example, in a serial transmitter circuit, coupling may cause transitions in the data being transmitted to disturb the edges of its PLL-based oscillator signal [31]. By viewing the clock and data signals simultaneously on a realtime oscilloscope, it is possible to verify this effect, whereas if the clock signal were viewed on a spectrum analyzer, a spur would be visible with no indication of its phase.

In contrast to the Nyquist-rate sampling in a realtime oscilloscope, a sampling oscilloscope sub-samples its input signal at a much lower rate, usually below 1 MHz [67]. On the other hand, its maximum input frequency is no longer limited by the sampling rate, but by the bandwidth of the analog frontend and sampling circuitry. Furthermore, as the sampling oscilloscope's ADC has more time to process each sample, it can achieve higher voltage resolution. Currently, realtime oscilloscopes have 8-10 bits of resolution, whereas sampling oscilloscopes typically have over 12 bits of resolution [67].

Due to its sub-sampling behavior, a sampling oscilloscope cannot be used to generate phase error power spectra, but it can generate jitter histograms, and its ability to debug time-domain issues is only slightly limited compared to a realtime oscilloscope. For example, a serial transmitter can be configured to transmit a repeating data sequence. Provided the duration of each data sequence transmission is slower than the maximum sub-sampling rate of the sampling oscilloscope, it is possible to sub-sample a very high-speed clock signal relative to the start time of each repeated data sequence. The full clock signal can then be slowly reconstructed in the time domain, hence the "equivalent-time" name for this instrument. The limitation of this method stems from the instrument's sub-sampling behavior, in that any periodic disturbances in the oscillator signal not harmonically-related to the sub-sampling rate can corrupt the measurement.

A drawback of time-domain measurement instruments is caused by their wide analog bandwidths. The analog circuitry present in both types of oscilloscopes prior to their ADCs adds broadband thermal noise to the oscillator signal, and this additive noise corrupts the oscillator signal via the mechanism described in Section III-C. Therefore, even the highest-performance realtime and sampling oscilloscopes have integrated jitter floors well above those of phase noise analyzers.

VIII. Frequency Stability

In the preceding sections, oscillator error was analyzed in the frequency domain via phase error and jitter power spectra, $S_\phi(f)$ and $J(f)$. There exist, however, a broad class of problems in fields such as astronomy [71], satellite navigation [72], and precision metrology [73], [74] in which oscillator error is usually characterized in the time-domain with a quantity called the Allan variance, $\sigma_y^2(\tau)$, which is described in this section. The main utility of the Allan variance and its variants is that they allow for simple characterization of very long-term oscillator behavior (days to years). For example, they are useful in analyzing the behavior of a system where the frequency of a low-precision oscillator is periodically re-calibrated with a high-precision oscillator, a situation which frequently occurs in mobile devices [75]. The development of the time-domain approach to oscillator error was primarily driven by the invention of the atomic clock, whereas the phase error frequency-domain approach was motivated by the development of Doppler radar [76], [77].

This section considers only the phase noise component of phase error. Spurious tones and deterministic modulation in the oscillator phase error have been extensively analyzed within this framework [78], [79], but they require special consideration which is beyond the scope of this tutorial.

A. Frequency Fluctuations

The instantaneous frequency, $\omega(t)$, of the oscillator signal given by (1) is defined as the derivative of the argument of the sine term, i.e., $\omega(t) = \omega_0 + \phi'(t)$ [80]. The *frequency fluctuations* function is defined as $\omega(t) - \omega_0$, i.e., the deviation of the instantaneous frequency from its nominal value. The *fractional frequency fluctuations* function, $y(t)$, is the frequency fluctuations function normalized by ω_0, i.e., $y(t) = \phi'(t)/\omega_0$.

The use of frequency rather than phase as the variable of interest stems from early research characterizing oscillators by counting its cycles [81]. A digital counter can be used to approximately measure sequences of time averages of $y(t)$ of the form

$$\bar{y}_k = \int_{\lambda_k}^{\lambda_k+\tau} \frac{y(t)}{\tau} dt = \frac{\phi(\lambda_k+\tau) - \phi(\lambda_k)}{\omega_0 \tau}, \qquad (38)$$

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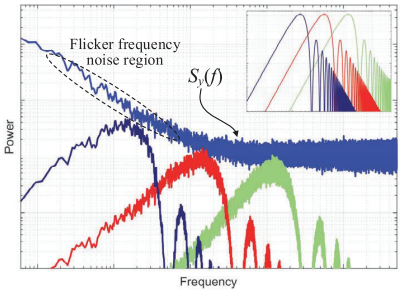


Fig. 12. Frequency-domain signal processing of the Allan variance. Inset shows the equivalent bandpass filter transfer function.

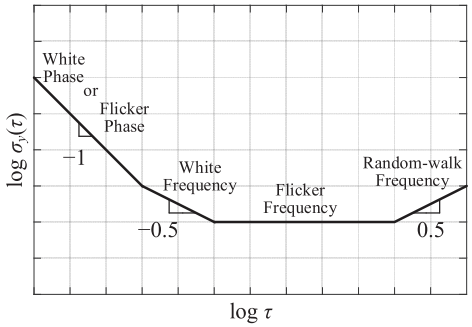


Fig. 13. The σ-τ plot, annotated with the slopes of different regions indicating the different noise type contributions.

where λ_k denotes the time of the kth measurement, and τ is the duration of the average, also known as the counter gating interval, or stride [82]. It follows from (38) that the $\bar{y}_k$ sequence is generated by sampling the result of a τ-width moving average filter applied to $y(t)$, which is a type of lowpass filter. Hence, $\bar{y}_k$ can be interpreted as samples of the continuous time sequence whose power spectrum is a lowpass-filtered version of $S_y(f)$.

Counters only measure the zero crossings of a clock, so the measurement of (38) incurs quantization noise. Laboratory frequency counters use various methods to improve the measurement accuracy of $\bar{y}_k$, especially for short gating intervals relative to the clock period [83], [84]. However, for the types of problems where Allan variance is a useful metric, the values of τ of interest are typically many orders of magnitude larger than the clock period, so this quantization error can often be ignored. However, there are other non-idealities within the measurement instrument such as drift and noise in its internal time base. These cannot be ignored, and must be considered as part of the uncertainty in the measurement [85].

B. Allan Variance

A focus of early research on precision oscillators was characterizing flicker frequency noise, which manifests as the low-frequency region of $S_y(f)$ that decays at -10 dB/decade [86], shown in Fig. 12. Unlike other types of noise, such as white frequency noise (flat in $S_y(f)$) or white phase noise ($+20$ dB/decade in $S_y(f)$), measurement uncertainty due to flicker frequency noise cannot be removed by averaging, which leads to an accuracy limitation for measurements that depend on averaging over time intervals. Its measurement also defies characterization by the variance, because the integral over positive frequencies including 0 of a lowpass-filtered $S_y(f)$ is unbounded, due to the divergence of the integral of $1/f$ at $f = 0$ [87].

The divergence of the flicker noise model at low frequencies is shown to be accurate over extremely long observation intervals, well beyond practical measurement durations [88], [89]. One method to bound the integral of $S_y(f)$ is to use arguments similar to those in Section V-C, where a restricted jitter density integration interval is used to bound the calculation of absolute jitter. However, there is no unique interval of frequency noise integration for the characterization of oscillators that would be applicable in all scenarios [86]. Therefore, a different metric is needed that is both generally applicable and practically measurable.

The problem with computing the variance of $\bar{y}_k$ occurs because the integral of $S_y(f)$ diverges at $f = 0$, so the most straightforward solution is to take the variance of the first difference of $\bar{y}_k$. The Allan variance, or two-sample variance, is thus defined as

$$\sigma_y^2(\tau) = \frac{1}{2} E\left[(\bar{y}_2 - \bar{y}_1)^2\right]. \tag{39}$$

Hence, the value $\sigma_y^2(\tau)$ is equal to the variance of the difference between two adjacent τ-duration average frequency measurements, normalized to the nominal frequency. This may seem contrived, but it has an intuitive interpretation in relation to timekeeping, which is explained in the next sub-section.

Taking the first difference in the time domain is equivalent to a highpass filter in the frequency domain, so the combined response of the first difference and the τ-width moving average filter is equivalent to a bandpass filter applied to $S_y(f)$ [90]. The behavior of this filter is shown in Fig. 12, for three different values of τ. The bandwidth and center frequency of this filter is proportional to $1/\tau$, so it has a constant logarithmic bandwidth. As flicker noise has constant integrated power over logarithmic bandwidths, $\sigma_y^2(\tau)$ is constant when the value of τ places the filter's center frequency in regions of $S_y(f)$ dominated by flicker frequency noise.

The square root of the Allan variance, $\sigma_y(\tau)$, is called the Allan deviation. This is typically plotted on a log-log scale versus τ, in what is called a σ-τ plot, shown in Fig. 13. Like a phase noise plot, different regions of the σ-τ plot are dominated by different types of noise. A typical σ-τ plot shows, for increasing τ, a downward sloping region, a flat region, and an upward sloping region. As indicated, all but the upward-sloping region (random-walk frequency) can be attributed to the intrinsic noise processes encountered in IC design. The random-walk frequency region tends to be dominated by external effects, such as random temperature fluctuations.

The value of τ required to measure the upward sloping region depends on the type of oscillator. For example, precision temperature-compensated crystal oscillators (TCXO) can show this region after τ's of minutes or hours, whereas the Rubidium oscillators in GPS satellite clocks require a τ of several days [91]! It is important to note that, as τ (and hence measurement duration) becomes large, it becomes increasingly difficult to isolate the performance of the oscillator under test from the measurement environment. In addition to temperature fluctuations, issues such as physical vibration due to office foot traffic, power surges causing equipment failure, or failure of the oscillator itself can all be considered random events that tend to manifest during long-term measurements.

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C. Interpretation and Comparison With Phase Noise

Mobile devices such as cellular phones and GPS receivers contain circuits called realtime clocks (RTC). An RTC contains an internal oscillator tuned to a known nominal frequency. By counting the oscillator's cycles, a sense of time is kept. The frequency stability of the mobile device RTC oscillator is typically poor, so the RTC is periodically recalibrated using the base station time as described below.

Every τ seconds, the base station transmits its time to the mobile device. The mobile device updates its internal time to the received time, but also computes the error between the RTC's measurement of the τ-second interval and the actual interval as defined by the base station. The mobile device then uses this measured error to correct the RTC's prediction of the subsequent τ-second interval.

In this manner, the mobile device's time error from the base station time is reset to 0 every τ seconds, but its time error grows as time elapses from the most recent reset up to the next reset. In this scenario, the standard deviation of the mobile device's time error immediately before each recalibration is closely approximated by $\tau\sigma_y(\tau)$. While this idealized example ignores practical challenges faced by such systems, e.g., temperature fluctuations between recalibrations, it illustrates how the Allen variance is a useful tool to characterize the precision of time measurements based on the performance of the underlying oscillator used to measure the time interval.

Using a σ-τ plot in the above example, if the chosen τ falls in the -1 sloped region, then $\tau\sigma_y(\tau)$ is a constant with respect to τ. If τ falls in the flat region, then $\tau\sigma_y(\tau)$ grows linearly with τ, and if τ falls in the rising region, then $\tau\sigma_y(\tau)$ grows at a much higher rate. From the σ-τ plot, it is also easy to calculate the maximum allowable time between recalibrations given a maximum time error standard deviation requirement. In contrast, such information is not evident from a plot of either $S_\phi(f)$ or $J(f)$.

The time between the negative-slope region and the flat region in a σ-τ plot is of particular interest. This time, called τ_0, corresponds to the time after which averaging a frequency measurement longer than τ_0 seconds does not increase the measurement precision. Thus, the *flicker noise floor* of frequency stability is a critical specification of precision oscillators for metrology applications. Recent publications have reported reaching a frequency stability of below 1.5×10^{-18} with just 30 minutes of averaging [92]. For a point of scale, this is equivalent to measuring the diameter of the earth to a precision of less than the width of a hydrogen atom [93]!

The Allen variance is a convenient metric not only because it is simple to estimate through measurement, but also because its estimate converges for all the commonly encountered power-law noise types. There exist several other types of variances that offer advantages over the Allen variance. For example, the modified Allan variance (MVAR) introduces a τ-dependent scale factor to the Allan variance that gives the white phase and flicker phase noise regions different slopes on the σ-τ plot [94]. The total variance (TVAR) is another Allan variance like metric that has better convergence of the estimator sequences for long τ in the presence of effects such as linear frequency drift [95]. Another metric is the Hadamard variance which has a sharp frequency selectivity and can estimate very high order frequency noise, namely flicker walk frequency (-50 dB/dec phase noise) and flicker run frequency (-60 dB/dec phase noise) noise [96]. This was needed to analyze the Rubidium oscillators in GPS satellites that exhibit complex frequency drift behavior [91].

The approach to selecting a type of variance is similar to the choice of window type for power spectrum estimation. The different types emphasize (or obscure) different aspects of the signal, and depending on the features of interest one may be more appropriate than another. The references [90], [97], [98] provide more details on many commonly-used types of variance.

IX. Conclusion

Oscillators and the clock signals they generate are ubiquitous in modern electronic systems. Due to their wide range of applications, different disciplines have each developed their own metrics and methods by which to characterize oscillator non-idealities, each uniquely suited to their particular application. Wireless systems are predominantly concerned with the oscillator's phase error power spectrum. Digital clocked circuits, and wireline communication systems are more frequently analyzed using time-domain jitter calculations. Metrology and physics applications frequently employ the Allan variance. Although these metrics, and the instruments used to measure them, appear very different, as explained in this tutorial they are all just different perspectives on oscillator phase error.

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Ian Galton (F'11) received the Sc.B. degree from Brown University in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology in 1989 and 1992, respectively, all in electrical engineering. Since 1996, he has been a Professor of electrical engineering with the University of California, San Diego, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters and phase-locked loops.



Colin Weltin-Wu (M'15) received the B.S. degree in math and the M.E. degree in electrical engineering from the Massachusetts Institute of Technology and the Ph.D. degree from Columbia University. He spent 15 months, starting in 2014, collaborating with I. Galton at the University of California at San Diego. He is currently involved in high-performance phase-locked loops at Analog Devices, Inc.

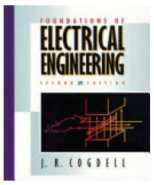
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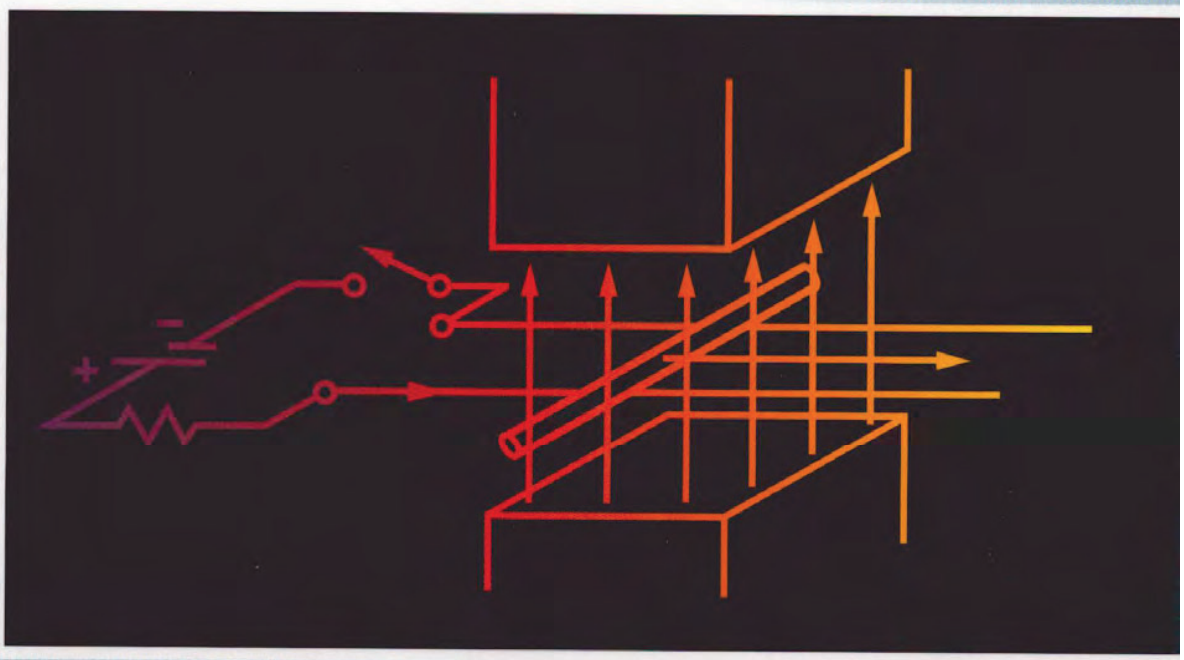
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3 The Dynamics of Circuits
4 The Analysis of AC Circuits
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$$L_{eq} = L_1 \parallel L_2 = \frac{1}{1/L_1 + 1/L_2} \text{ (parallel inductors)} \tag{3.9}$$

Capacitor Basics

Physical capacitors. Electric (electrostatic) forces arise from interactions between separated charges, and the associated energy is called electric energy. To store electric energy, we must separate charges, as in Fig. 3.9.

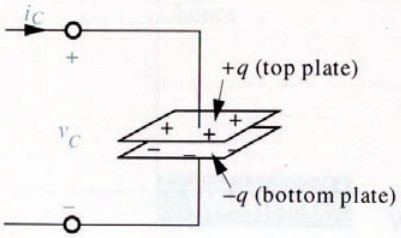


Figure 3.9 Structure having capacitance.

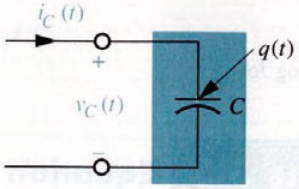


Figure 3.10 Circuit symbol for capacitance.

OBJECTIVE 2

To understand the properties of capacitors and to be able to find the capacitor voltage from the capacitor current and vice versa

Circuit-theory definition of a capacitor. Figure 3.10 shows the circuit symbol for a capacitance. Capacitance is defined as the constant relating charge and voltage in a structure that supports a charge separation. If q is the charge on the + side of the capacitor and the voltage is v_C, as shown in Fig. 3.9, the capacitance, C, is defined as

$$q = Cv_C \tag{3.10}$$

Chapter 13 discusses the physics of capacitance. For every charge arriving at the + side of the capacitor, a charge of like sign will depart from the − side and the structure as a whole will remain charge-neutral. Thus, KCL will be obeyed because charge flowing into the + terminal side is matched by charge flowing out of the − terminal, as for a resistor. If current is positive into the + terminal, positive charge will accumulate there and will be increasing in proportion to the current. From the definition of current, we can relate the charge in Eq. (3.10) and current as follows:

$$i_C = \frac{dq(t)}{dt} \tag{3.11}$$

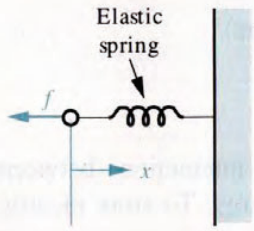
where $q(t)$ is the charge in the + side of the capacitor. Thus, we may define the relationship between current and voltage for a capacitor as

$$i_C = \frac{d}{dt} Cv_C(t) = C\frac{dv_{C(t)}}{dt} \tag{3.12}$$

where the last form of Eq. (3.12) is valid if the capacitance is constant. Note that we have used a load set in Fig. 3.10 for the voltage and current variables.

farad, microfarad, nanofarad, picofarad

Units of capacitance. The unit of capacitance is the coulomb/volt, but to honor Michael Faraday (1791–1867), we use the name *farad* (F). Realistic capacitor values come small and usually are specified in microfarads (10^{-6} F, or μF), nanofarads (10^{-9} F, or nF), or picofarads (10^{-12} F, or pF). When a capacitor is constructed from parallel



$f = Kx$ (reaction)

$u = \frac{dx}{dt} = \frac{1}{K}\frac{df}{dt}$

Figure 3.11
Mechanical analog for capacitance.

plates, as in Fig. 3.9, the capacitance depends on the area, separation, and material (if any) between the plates.

Mechanical analog of capacitance. The mechanical analog of a capacitor is a spring, as shown in Fig. 3.11. The analog of velocity is current and thus displacement of the spring is analogous to charge. The voltage across a capacitor is analogous to the force produced by the spring. Comparison of the second equation in Fig. 3.11 with Eq. (3.12) shows that capacitance corresponds to the inverse of the stiffness constant, K, and thus capacitance is analogous to the compliance of a spring.

EXAMPLE 3.3 Equation of RC circuit

Derive the equation for the current in Fig. 3.12(a). Assume $v_C(0) = 0$.

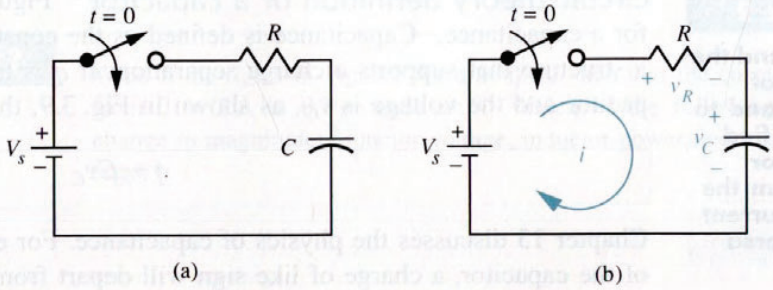


Figure 3.12 (a) Closing the switch will cause a momentary current. (b) The same circuit with variables defined.

SOLUTION:
Figure 3.12(b) defines the capacitor and resistor voltages in a load-set convention. With the switch closed, KVL is

$$-V_s + v_R(t) + v_C(t) = 0 \tag{3.13}$$

We may express both voltages in terms of the current if we differentiate Eq. (3.13):

$$0 + \frac{d}{dt}Ri(t) + \frac{dv_C(t)}{dt} = R\frac{di(t)}{dt} + \frac{i(t)}{C} = 0 \tag{3.14}$$

The last form in Eq. (3.14) is readily manipulated to the form

$$\frac{di}{i} = -\frac{1}{RC}dt \Rightarrow \ln i = -\frac{t}{RC} + \ln A \Rightarrow i(t) = Ae^{-t/RC} \tag{3.15}$$

where A is a constant. The current will charge the capacitor until the capacitor voltage is equal to the battery voltage. Equation (3.16) equates the final charge on C to the integral of the current.

$$q - q(0) = CV_s = \int_0^\infty i(t)\,dt = \frac{Ae^{-t/RC}}{-1/RC}\bigg|_0^\infty = A(RC) \tag{3.16}$$

Because $v_C(0) = 0$, $q(0) = 0$, and

$$A = \frac{V_s}{R} \tag{3.17}$$

hence

$$i(t) = \frac{V_s}{R} e^{-t/RC} \tag{3.18}$$

WHAT IF?

What if the switch is opened after being closed a long time? What would happen to the capacitor voltage?[4]

Integral *i–v* equation. Equation (3.12) is useful in determining the current through a capacitor, given the voltage as a function of time. If we know the current and wish to determine the voltage, we must integrate. Let us consider that we know the capacitor voltage at some time, say, $t = 0$, and wish to determine the voltage at a later time, t. We can integrate Eq. (3.12) from 0 to t, with the result

$$v_C(t) = v_C(0) + \frac{1}{C}\int_0^t i_C(t')\,dt' \tag{3.19}$$

We have used t' as the dummy variable of the integration process because t is one limit of the integral.

EXAMPLE 3.4 Capacitor discharge and charge

As an example of the use of Eq. (3.19), consider a capacitor with current, as shown in Fig. 3.13.

Here we know the voltage at the beginning time, $v_C(0) = -2$ V, and the current through the capacitor. We wish to compute the voltage for all $t > 0$. We will use Eq. (3.19), noting that we must divide the integration into several regions due to the piecewise nature of the current function. During interval I, $0 < t < 1$ ms, the current is zero; hence, the voltage does not change. During interval II, the slope of the current is 0.1 A/1 ms = 100 A/s; hence, the current is

[4] No current could flow after the switch opened, and according to Eq. (3.12), the voltage would remain constant. A real capacitor would discharge over time due to leakage current.

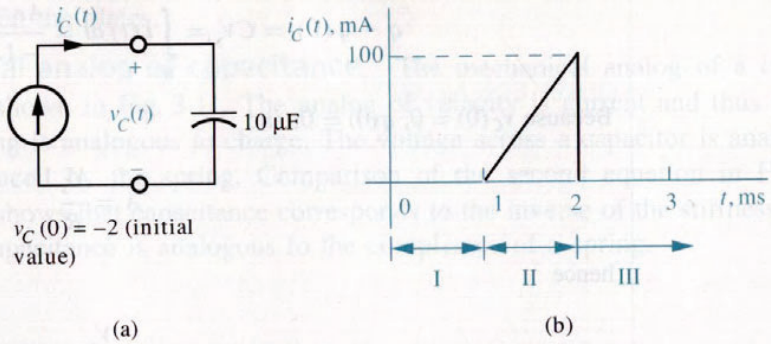


Figure 3.13 (a) The capacitor has an initial voltage. (b) Current into the capacitor for positive time.

$$i_C(t) = 100(t - 1\text{ ms})\text{ A}, \qquad 1\text{ ms} < t < 2\text{ ms} \tag{3.20}$$

Thus, during interval II, the voltage will be

$$v_C(t) = -2.0 + \frac{1}{10\mu\text{F}} \int_{1\text{ ms}}^{t} 100\,(t' - 1\text{ms})\,dt'\Big|_{\text{II: } 1 < t < 2\text{ ms}}$$

$$= -2.0 + \frac{10^{+5} \times 100\,(t - 1\text{ms})^2}{2}\text{ V} \tag{3.21}$$

which indicates a parabolic increase, as shown in Fig. 3.14. The final value at $t = 2$ ms is $+3$ V, which is easily checked from the area under the current curve:

$$\Delta v_C = \frac{\Delta q}{C} = \frac{\text{area under current curve}}{C} = \frac{\frac{1}{2} \times 1\text{ms} \times 100\text{ mA}}{10\ \mu\text{F}} = +5\text{ V} \tag{3.22}$$

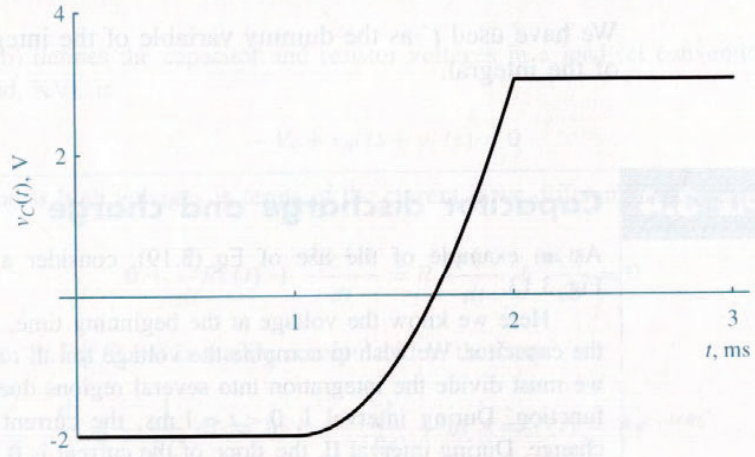


Figure 3.14 Capacitor voltage for positive time.

After the current pulse, the capacitor voltage remains constant because the current is zero. This

constant voltage would hold for an ideal capacitor; a physical capacitor would discharge eventually due to leakage current.

WHAT IF? What if the current were constant at 100 mA for 1 ms $< t <$ 2 ms? What then would be the final value?[5]

Mechanical analogy. The process of integrating current through a capacitor to determine voltage is analogous to integrating velocity to determine change in force in a spring problem. The only difference is that the value of the capacitance scales the integral of the current, whereas the scale factor depends on K, the spring constant, in the mechanical analog.

Stored energy in a capacitor. The charge separation in a capacitor stores electric energy. This energy is analogous to potential energy stored in a stressed spring. We may derive the stored electric energy in a capacitor by integrating the power into the capacitor,

$$W_e = \int p_C \, dt = \int v_C \times C \frac{dv_C}{dt} dt = \int d\left(\frac{1}{2} C v_C^2\right) = \frac{1}{2} C v_C^2 = \frac{1}{2} \frac{q^2}{C} \tag{3.23}$$

where p_C is the power into the capacitor and W_e is the stored electric energy in the capacitor. The constant of integration must be zero because the uncharged capacitor stores no energy. We see from Eq. (3.23) that the stored energy depends uniquely on the voltage, or the charge, and the capacitance. For example, if we take a 10-μF capacitor and connect it briefly to a 12.6-V battery, the capacitor will receive $0.5 \times 10^{-5}(12.6)^2 = 7.94 \times 10^{-4}$ J from the battery. Although this is not much energy, it would take only about 1 μs to charge the capacitor. Hence, the rate of energy flow would be rather high, about 800 W.

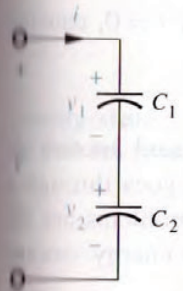


Equivalent Circuits

Capacitors in series and parallel. Figure 3.15 shows two capacitors in series. KVL yields

$$v(t) = v_1 + v_2 = \frac{1}{C_1}\int_0^t i \, dt + \frac{1}{C_2}\int_0^t i \, dt = \frac{1}{C_{eq}}\int_0^t i \, dt \tag{3.24}$$

Figure 3.15
Capacitors in series add like resistors in parallel: $C_{eq} = C_1 \parallel C_2$.



where

$$C_{eq} = C_1 \| C_2 = \frac{1}{1/C_1 + 1/C_2} \quad \text{(series capacitors)}$$

Thus, capacitors connected in series combine numerically like resistors in parallel. Similarly, we can easily show that capacitors in parallel add like resistors in series, that is,

$$C_{eq} = C_1 + C_2 \quad \text{(parallel capacitors)} \tag{3.25}$$

Mechanical analog for resistance. A mechanical analog for a resistance is frictional loss of a special type. Voltage is analogous to force, and current analogous to ve-

[5] +8 V.

TABLE 3.1 Summary of Mechanical and Electrical Analogs

Mechanical	Electrical
Force	Voltage
Velocity	Current
Displacement	Charge
Mass	Inductance
Spring compliance	Capacitance
Shock absorber	Resistance

locity. Voltage/current, or resistance, would thus imply a force that is proportional to velocity. We experience such a force when we try to move underwater. A common mechanical component having this property would be an automotive shock absorber. Table 3.1 summarizes the analogies between mechanical and electrical quantities.



Check Your Understanding

1. An inductor has a stored energy of 5 J and an inductance of 0.1 H. What is the current through the inductor?
2. If an ideal 10-V battery were connected for 1 s to an ideal 1-H inductor, how much energy would be given to the inductor?
3. A capacitor has a stored energy of 500 μJ and a capacitance of 0.15 μF. What is the voltage across this capacitor?
4. What is the mechanical analog of an inductor?

Answers. **(1)** 10 A; **(2)** 50.0 J; **(3)** 81.6 V; **(4)** mass.

3.2 FIRST-ORDER TRANSIENT RESPONSE OF *RL* AND *RC* CIRCUITS

transients, first-order transient

First-order transients. In the major part of this chapter, we show how to analyze an important class of circuit problems. Typical situations are shown in Fig. 3.16. These circuits are characterized by having the following:

- A single energy storage element, one capacitor or inductor
- Loss, represented by one or more resistors
- DC sources
- A switch[6] that either opens or closes at a known time, usually $t = 0$, causing a sudden change in the circuit
- Only linear components.

In all cases, the circuit will have one dc state before the switch action and another dc state long after the switch action. Consequently, the state of the circuit goes through a transition. Because this transition lasts for a brief period of time, these problems are often called *transient* problems. We consider primarily circuits with one energy storage element, which lead to *first-order transients*.

[6]The pulse in Fig. 3.16(c) can be considered a voltage switched ON, then OFF.

mately 10–12 pulses/second and relays counted the pulses at the exchange to route the call. The ring signal was about 90 to 100 V ac at approximately 20 Hz.

The modern system used a tone system to transmit switching information and semiconductor switching computers have replaced the relays. The "ring" signal is commonly a tone that activates an audible device in the telephone receiver.



Digital Information

The local exchange switches up to 10^4 lines with the signal at the base band with a 4-kHz bandwidth. Between exchanges, the voice information is modulated with signal sideband plus carrier into groups of 12 adjacent channels between 60 and 108 kHz. These groups, 12 channels, are then placed into a supergroup of 60 channels between 312 and 552 kHz, and finally 10 supergroups, 600 channels, are placed into a mastergroup between 564 and 3084 kHz. For long distance, the voice channels are modulated to yet higher frequency for transmission by coaxial cable, line-of-sight microwave, or satellite link. Currently digital systems using optical fibers are replacing traditional analog systems.

Noise in Receivers

noise, interference

Importance of noise. When we spoke of op amps in Chapter 9, we asserted that gain is cheap. With radio receivers, gain is not as cheap as with op amps, but we can still achieve as high a gain as we wish by adding more stages of amplification. We might suppose, therefore, that we can successfully detect any input RF signal, no matter how weak, simply by having adequate gain in the receiver. This is not true, however, because the sensitivity of a radio receiver is limited by random noise. *Noise*, by definition, is any undesired signal in the system, whether natural or man-made. Man-made noise is called *interference*; Chapter 10 showed techniques to reduce its effects.

blackbody radiation, shot noise, flicker noise

Sources of natural noise. Natural noise in communication systems comes from two sources. Some noise comes into the receiver from the antenna; for example, in an AM receiver, we can hear a sporadic crackling noise from lightning during storms. Other sources of noise that enter the system through the antenna are atmospheric gases (thermal noise) and extraterrestrial objects such as the sun and our galaxy (cosmic noise).

The second source of noise is the receiver itself. Just as any body radiates *blackbody radiation* due to the thermal motion of its atomic constituents, so also resistors radiate their own type of thermal noise into the circuits of which they are a part. We investigate resistor noise in what follows. Transistors add, in addition to thermal noise, *shot noise* due to the discrete charges that carry the current across the *pn* junctions, and *flicker* or $1/f$ noise, due to slow changes in device properties from aging, temperature, and other physical changes.



Equivalent Circuits



The Frequency Domain

Thermal noise. The thermal radiation of resistors plays an important role in the description of noise because resistors provide a simple calibration for noise signals. Figure 11.16(a) shows a resistor, R, and indicates the noise voltage generated by the thermal motion of the carriers in the resistor. The Thévenin equivalent circuit in Fig. 11.16(b) separates the noise voltage from the resistance, which here is noise-free. The power spectrum of the noise voltage in volts^2/hertz is shown in Fig. 11.16(c),

$$S_n(f) = 4kTR \text{ V}^2/\text{Hz} \tag{11.14}$$

white noise

with k = Boltzmann's constant of 1.38×10^{-23} J/K. We note the following:

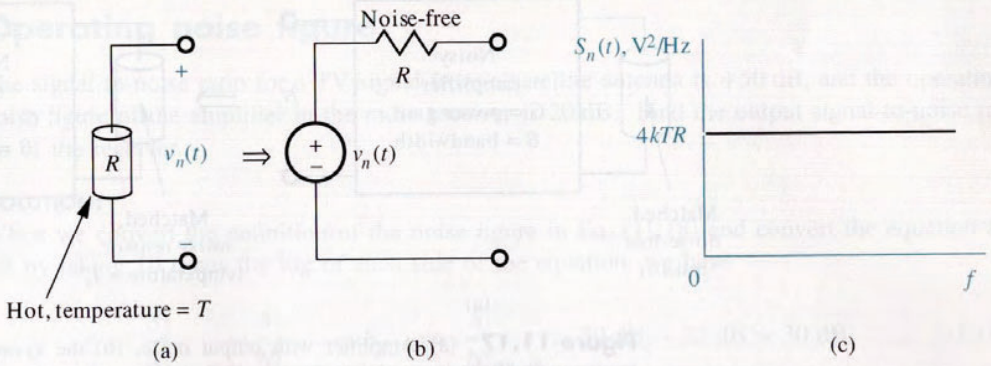


Figure 11.16 (a) A noisy resistor; (b) Thévenin equivalent circuit of a noisy resistor; (c) power spectrum of thermal noise.

- The noise spectrum is *white noise*, meaning that all frequencies are present equally, at least throughout the radio spectrum. Thus, a resistor produces a noise power that is proportional to the bandwidth of the circuit.
- The intensity of the power spectrum is proportional to the temperature of the resistor. For sensitive amplifiers, we may measure the noise of the system by comparing system noise to the noise from a resistor of known temperature.
- The intensity of the power spectrum is proportional to the resistance. For this reason, large values of resistance are avoided in sensitive electronic amplifiers.

available power

The *available power* out of a circuit is the maximum power that the circuit is capable of delivering into a matched load (see Chapter 2, page 69). The available power spectrum from the circuit in Fig. 11.16(b) is.

$$S_{av}(f) = \frac{S_n(f)}{4R} = kT \text{ W/Hz} \tag{10.15}$$

where $S_{av}(f)$ is the available power spectrum in watts/hertz. Thus, the total power a noisy resistor will contribute to a matched circuit is

$$P = kTB \text{ W} \tag{11.16}$$

where B is the bandwidth in hertz. Equation (11.16) is useful in determining the signal-to-noise ratio in a communication circuit, once we have defined the noise figure and system temperature of an amplifier.

system temperature

System temperature. The noise originating in the resistors and semiconductors in a radio amplifier is generally broadband or white noise, at least over the bandwidth of the radio. Thus, we may represent the noise *as if* it originated in a resistor at the input of the radio. Figure 11.17(a) shows the true situation: An amplifier with a power gain of G and a bandwidth of B has internal noise sources that produce N_s watts of noise at its output. In Fig. 11.17(b) we show an equivalent amplifier, assumed to be noise-free, with the same noise at its output *attributed* to a noisy resistor at the input. The *system temperature* is defined as the temperature the resistor required in Fig. 11.17(b) to produce the same amount of output noise as in Fig. 11.17(a). Using Eq. (11.16), we can express

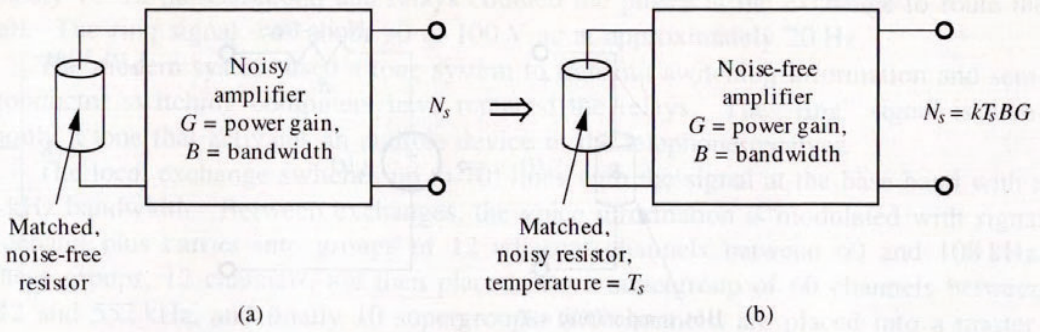


Figure 11.17 (a) Amplifier with output noise; (b) the system temperature is the temperature of the input resistor to give the same output noise.

the output noise as

$$N_s = kT_sGB \Rightarrow T_s = \frac{N_s}{kGB} \text{ K} \tag{11.17}$$

where T_s is the system temperature and N_s is the output noise produced by the amplifier. All the internally generated noise is *referred to the input* of the receiver and then expressed as a temperature. The system temperature describes the sensitivity of the amplifier; the lower the system temperature, the more sensitive the amplifier.

operating noise figure

Noise figure. The *operating noise figure* is defined as the input signal-to-noise ratio divided by the output signal-to-noise ratio. Figure 11.18 shows an amplifier with input signal and noise, S_{in} and N_{in}, and output signal and noise, S_{out} and N_{out}. The *operating noise figure* is defined to be

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{N_{out}}{N_{in}G} = \frac{N_{in}G + N_s}{N_{in}G} = 1 + \frac{N_s/G}{N_{in}} = 1 + \frac{T_s}{T_{in}} \tag{11.18}$$

where F is the operating noise figure of the amplifier and is often expressed in decibels: $F_{dB} = 10 \log F$ and T_{in} is the input noise expressed as a temperature. The first form on the right side of Eq. (11.18) is the definition of operating noise figure. The second form introduces the gain, $G = S_{out}/S_{in}$, and the third form breaks the output noise into two components, the amplified input noise and the internally generated noise. The last form shows that the noise figure depends on the internally generated noise, referred to the input of the amplifier, compared with the input noise. Thus, the operating noise figure depends in part on the input noise and not on the amplifier only. The operating noise figure is useful in performing signal-to-noise calculations in a communication system.

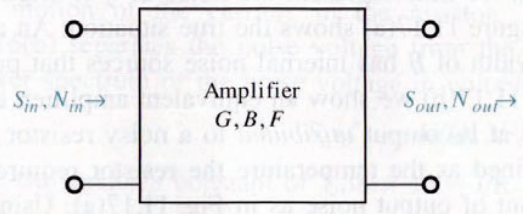


Figure 11.18 Amplifier with signal and noise at input and output.

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Appendix WITTMANN02

Brief Papers

Trimless High Precision Ratioed Resistors in D/A and A/D Converters

Reimund Wittmann, Werner Schardein, Bedrich J. Hosticka, Gert Burbach, and Juergen Arndt

Abstract—**Investigations into realization of high precision ratioed resistors in standard CMOS and BiCMOS processes have been carried out. The results indicate that the layout of the resistors can be optimized with respect to area and matching requirements to yield relative accuracy better than 0.25%. Using an intermeshed ladder architecture, fast converters with resolution up to 10 b are realizable without trimming.**

I. Introduction

In recent years, A/D and D/A converters based on the use of resistor-strings have gained great popularity. The characteristics of such converters include inherent monotonicity, temperature insensitivity, low matching requirements on components, and relative simplicity, making resistor strings useful for high-speed ADC's and DAC's with moderate resolution requirements. Since the resistors in resistive converters are usually arranged as regular arrays, and the same resistor core can be used for both A/D and D/A conversion (Fig. 1), flexible layout generators can be easily realized.

A critical aspect of the resistive concept is the size of layout and component matching requirements. Increasing the resolution by one bit causes the number of resistors in the string to be doubled. But this may not always be a disadvantage, especially in applications where more than one converter is needed, e.g., in a video processor for the red, blue, and green components. For such applications, one resistor core can be used for realizing a high speed multichannel converter with excellent matching behavior because of accessing the same resistor string.

The upper limit of achievable resolution is not only given by how many resistors can be arranged in a defined area but also by precision limits due to lithography errors and process control. Any variation leads to a spread in resistance and can be caused either by gradient or statistical errors. Optimization strategies for resistors that minimize the effects limiting precision are rare and standard approaches (named in the following section) are not applicable to converter designs in which resistor values are fixed owing to speed and power requirements and where the large number of resistors limits the area.

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R. Wittmann, W. Schardein, B. J. Hosticka, and G. Burbach are with the Fraunhofer Institute of Microelectronic Circuits and Systems, 47057 Duisburg, Germany.

J. Arndt is with TEMIC Telefunken Microelectronic, 74072 Heilbronn, Germany.

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This paper presents a new optimization technique for resistor matching in resistive dividers that reduces the effects limiting precision and is intended for design of resistive D/A and A/D converters featuring high speed and moderate resolution.

II. Effects Limiting Matching Precision

To realize a resistive n-bit converter, a string of 2^n well matched resistors must be available. The matching behavior of those resistors, which are arranged in an array, is influenced by several important parameters. These parameters are the spread in sheet resistance, lithography and etching errors, bend effects, contact resistance, and alignment errors.

Lithography and etching errors lead to statistical and deterministic deviations of resistor ratios from the desired value. The precision of converters based on the string principle is independent of the design center resistance value, which is defined as the averaged resistance of all matched resistors in one converter. The absolute value can fluctuate in a range of about 30% from one wafer to another. Statistical deviations from this value are large for small structures and become smaller if structure size increases. Increasing the resistor size, however, must be carried out with care because of the increasing influence of deterministic deviations for larger structures. Thus, gradient errors with respect to the resistor core depend on height, orientation, and slope of the spread in sheet resistance. An optimal geometry for resistor layout has to be found, which reduces the statistical errors to minimum, assuming the statistical errors still dominate when compared with gradient errors.

In hand-crafted analog design it is usual to design well-matched resistors without any bends. In a flexible layout generator for different resolutions (2^n resistors), the resistors must contain bends or the area requirements would become excessive. Effects that decrease matching due to deterministic errors caused by bends, lithography, and etching are minimized by using an identical basic resistor cell for all matched resistors.

Another critical problem stems from contacts interconnecting the array resistors. Their resistance varies widely and can degrade matching behavior. Especially in converters featuring higher resolution in which low-valued resistors ($< 10\ \Omega$) are used, contact resistance can easily dominate over the string resistance. Also, mask tolerances can lead to contact alignment errors. To avoid these problems, the resistors are arranged in groups in which no contacts are used in the current path.

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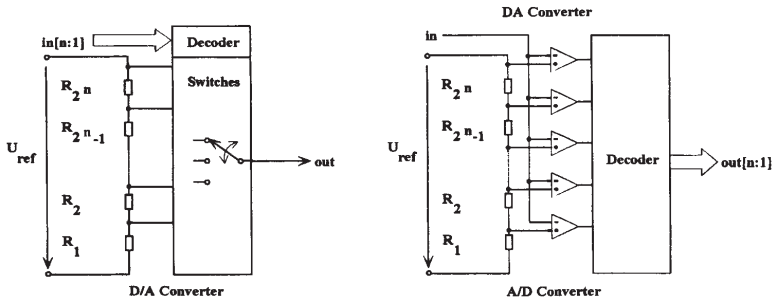


Fig. 1. Parallel resistor-string D/A and A/D converter.

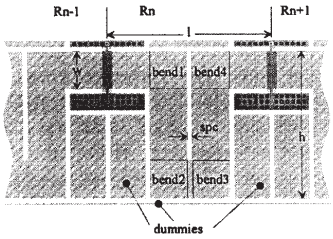


Fig. 2. Layout of basic resistor cell.

The resistors are interconnected without leaving the resistor layer. At the end of each resistor chain, where contacts are unavoidable, arrays of contacts are used for interconnection.

III. Resistor Cell

A flexible resistor layout generator (Fig. 2) has been developed that takes into account all aspects considered before. The resistor generator has been developed for use in a D/A and A/D converter compiler. Independent parameters are the length l, the resistance r, the width w, the spacing spc, and the material with the sheet resistance Rs of the resistor. Dependent parameters are the resulting height h and the number of foldings n.

The contacts for each voltage tap are set outside the reference current path and connected with the resistor layer to the voltage tap. This kind of connection is insensitive to alignment tolerance of the contacts. The use of two symmetrical contact arrays for each tap decreases the tap interconnection resistance and increases speed, since charge time for parasitic capacitances has been reduced. This principle is described in detail in [1]. The spacing between resistor meanders is kept constant. In case of missing meanders from a neighboring resistor, dummy polygons are used instead.

IV. Measurement of Matching Behavior

To investigate the influence of resistor parameters on matching behavior independent of technology, several test circuits with a string of 11 identical resistors were realized in a 0.8 μm-BiCMOS technology [2] and a 1.5 μm-HT-SIMOX process [3]. The resistor type used in converters with moderate resolution (9–12 b) has to have a low sheet resistance (< 50 Ω/square). Resistors in the SIMOX process were fabricated in polysilicon and exhibited 18 Ω/square. In the BiCMOS technology, an additional process step (silicide) decreased the sheet resistance of polysilicon to 1.2 Ω/square. Because of this additional process step in the BiCMOS technology, a better matching behavior for the SIMOX resistors was expected. The process modules used for resistor fabrication in the SIMOX process were the same as in a standard CMOS process. Fig. 3 summarizes the measured results of the test circuits.

The measurement of test structures yielded several important results described below. The maximum of measured relative accuracy exceeded values known from open literature. The maximum of measured relative accuracy was found to be 0.24% for SIMOX and 0.32% for BiCMOS technology (for untrimmed resistors). Values known from literature vary in the range of 0.5–1%, but these are based mostly only on paired resistors and have high area requirements ($w > 25$ μm [4]). In the measured range, the number of bends (varied between 4 and 20) had no influence on matching behavior. Matching behavior was found independent from the current density in the evaluated range of 40–1500 μA per μm line width (Fig. 3). Meander spacing in the range of 2–4 μm had also no effect on accuracy.

A direct dependence of the relative accuracy on resistor area was confirmed. The measurements corroborate our statement made above. Statistical errors dominate the resistors mismatch for small structures and deterministic errors due to gradients dominate in the case of large structures, so that an optimum can be easily determined. Thus, in the range below the maximum accuracy ($a < a_{crit}$, $\approx 10\,000$ μm^2 in BiCMOS), where statistical deviations dictate the matching behavior of resistors, a heavy dependence between matching error p and design area a is apparent (Fig. 4). In the double logarithmic diagram, all resistor types exhibit the same slope but different offsets for different fabrication processes. This behavior is almost independent of the realized resistance; only the area determines the precision and not the resistor width in cases where statistical errors dominate the resistor mismatch. Measurement results lead to a simple equation, which allows modeling of the statistical precision errors (1). This yields an area optimization procedure for the resistor core with respect

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Type	Technology	Material	R	l/h	Area	No. of bends	spc	w	Current density	Matching * error p *	Standard deviation
		(Ω/□)	(Ω)		(μm²)		(μm)	(μm)	(μA/μm)	σ_m , 11 res.	σ , 15 str.
1	BiCMOS	Silicide (1.2)	10	2	1220	4	2	8	1500	0.90 %	0.143 %
2	BiCMOS	Silicide (1.2)	10	1.4	2568	4	2	12	1025	0.60 %	0.112 %
3	BiCMOS	Silicide (1.2)	10	1.1	4340	4	2	16	750	0.51 %	0.165 %
4	BiCMOS	Silicide (1.2)	100	2.4	2640	20	2	4	300	0.56 %	0.116 %
5	BiCMOS	Silicide (1.2)	100	0.7	9040	12	2	8	160	0.32 %	0.070 %
6	BiCMOS	Silicide (1.2)	100	0.5	12960	8	2	8	160	0.34 %	0.070 %
7	BiCMOS	Silicide (1.2)	100	0.1	51288	4	2	16	75	0.63 %	0.422 %
8	SIMOX	Poly (18)	500	1.5	572	8	2	2.6	140	0.66 %	0.117 %
9	SIMOX	Poly (18)	500	1.1	1778	8	2	5	64	0.38 %	0.100 %
10	SIMOX	Poly (18)	500	1	4330	8	2	8	40 , 370	0.25 %	0.046 %
11	SIMOX	Poly (18)	500	1	4330	8	3	8	40	0.24 %	0.058 %
12	SIMOX	Poly (18)	500	1	4330	8	4	8	40	0.24 %	0.050 %

* averaged over 15 structures consisting of 11 resistors each

Fig. 3. Matching behavior of different types of resistors.

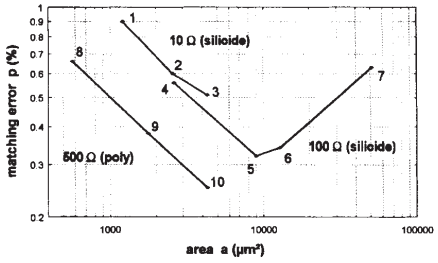


Fig. 4. Measurement results.

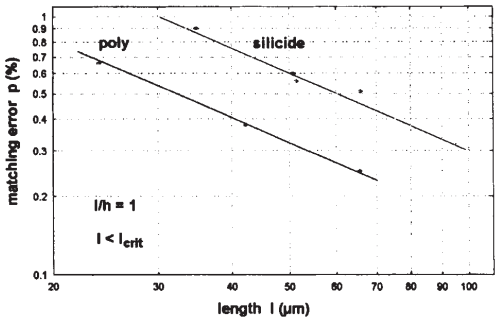


Fig. 5. Modeling of statistical errors.

to precision requirements for a defined converter resolution

$$p = \frac{1}{\sqrt{a'}}$$

$$a' = \frac{a}{a_{ref}}$$

and

$$a \leq a_{crit} \tag{1}$$

with

- p expected matching error in percent,
- a' normalized area of single resistor,
- a area of single resistor,
- a_{ref} reference resistor area (1% target precision) (SIMOX: $a_{ref} = 260\ \mu\text{m}^2$, BiCMOS: $a_{ref} = 900\ \mu\text{m}^2$).

In the range $a \leq a_{crit}$, the matching behavior is dominated by statistical mismatch, and the matching precision can be doubled by quadrupling the area of the resistors. Since this equation is valid for l/h ratios from 0.7–2.4, measurement results can be transformed to squared resistors ($l/h = 1$). In this case, the matching precision is proportional to the edge l of the resistor (Fig. 5). For $a > a_{crit}$, gradient errors degrade matching behavior. This area range should be avoided.

V. Resistor Core

Next, precision requirements imposed on resistors to be used in the core of an n-bit A/D or D/A converter will be analyzed to estimate the achievable resolution of conversion with this type of resistor. The matching tolerance $tol(Rx)$ can be defined as the relative error according to the average value Rm of all resistors of a string

$$tol(R_i) = \frac{R_i - \overline{R}}{\overline{R}} \cdot 100\%$$

with

$$\overline{R} = \frac{1}{j} \cdot \sum_{i=1}^{j} R_i \quad j\text{: number of resistors in a string.} \tag{2}$$

Only the matching tolerance decreases matching behavior, not a shift of Rm. The voltage at each node of a n-bit converter resistor string is found as

$$V_x = \frac{\sum_{i=1}^{x} R_i}{\sum_{i=1}^{2^n} R_i} \cdot V_{ref} = \frac{x + \sum_{i=1}^{x} \frac{tol(R_i)}{100\%}}{2^n} \cdot V_{ref} \quad 1 \leq x \leq 2^n. \tag{3}$$

The difference between V_x and $V_{x,ideal}[tol(Ri) = 0]$ has to be less than $\pm$ 0.5 LSB at all nodes of the string to meet specification.

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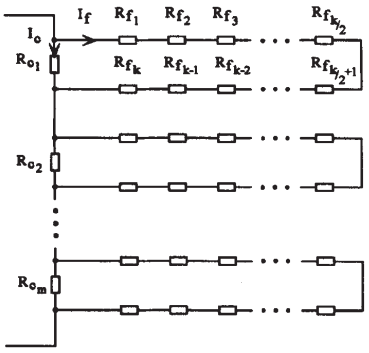


Fig. 6. Intermeshed ladder.

In a first approach worst case precision, requirements based on sensitivity analyses [9] are compared, which allow analysis of the influence of small parameter variations on the operating point of a circuit. The influence of correlated small resistor variations on the critical node of a resistor-string (center of the string) can determined with (4)

$$\Delta V_{crit} = \left|\frac{\partial V_{crit}}{\partial R_1}\cdot\frac{R_1}{100\%}\cdot tol(R_1)\right| + \left|\frac{\partial V_{crit}}{\partial R_2}\cdot\frac{R_2}{100\%}\cdot tol(R_2)\right| + \cdots + \left|\frac{\partial V_{crit}}{\partial R_2^n}\cdot\frac{R_2^n}{100\%}\cdot tol(R_2^n)\right| \le \frac{V_{ref}}{2^{n+1}}. \quad (4)$$

With use of the same type of resistor (same layout) for all resistors in the string, (4) results in

$$tol(R_{string}) \le \frac{100}{2^n}\% \quad (2^n \text{ resistors}). \quad (5)$$

Equation 5 defines the precision requirement for an n-bit string converter in which all 2^n resistors are connected in series. A limitation of the string principle is the area required for the resistor layout. Each additional bit requires doubling of the number of resistors. Also, the accuracy requirements imposed on the resistors are doubled, which considerably increases the area of each resistor (Fig. 4).

Chip size requirements can be relaxed by using an intermeshed resistor ladder [5]–[8]. The use of a small number of additional coarse resistors (Fig. 6) decreases precision requirements on the ladder resistors (6), which are arranged in decoupled groups of fine resistors. The intermeshed ladder architecture allows building of smaller and faster converters (owing to decreasing parasitic capacitances) than converters featuring the same resolution and using standard string structure.

The intermeshed ladder consists of two critical nodes. The first is found in the center of the coarse ladder on which the sensitivity for variation of the coarse resistors is maximal, and the second is found in the center of one of the direct neighbored fine-strings on which the sensitivity for variation of the fine resistors is maximal. With respect to the sensitivities of those critical nodes on deviations of the coarse resistors

Concept	Components for Core	Additonal Parameters	Matching Requirements	Area for Resistors
a) 7 bit				
string	128 Rs	-	tol (R) 0.8%	0.077 mm²
interm. ladder	4 Rc, 128 Rf	r=10, m=4	tol (Rc) 0.6% tol (Rf) 0.8%	0.061 mm²
b) 8 bit				
string	256 Rs	-	tol (R) 0.4%	0.512 mm²
interm. ladder	8 Rc; 256 Rf	r = 10; m=8	tol (Rc) 0.26% tol (Rf) 0.80%	0.151 mm²

Fig. 7. Comparison of matching requirements.

Rc and the fine resistors Rf, precision requirements can be estimated by

$$\frac{r}{r+1}\,tol(R_c) + \frac{1+\frac{r}{m}}{r+1}\,tol(R_f) \le \frac{100}{2^n}\% \quad (2^n \text{ resistors } Rf,\ m \text{ resistors} Rc) \quad (6)$$

with

- n resolution,
- $tol(x)$ matching tolerance of x,
- m number of coarse resistors,
- k number of fine resistors attached to one coarse resistor,
- $m * k = 2^n$,
- $r = Ic/If = k * Rf/Rc$.

The table in Fig. 7 allows a comparison of the presented concepts. Based on matching measurements given in the previous section and the worst case considered (i.e., 100% yield), the achievable resolution for each concept is shown. Thus, considering the worst case, a resolution of 8 b can be realized using an intermeshed ladder.

Since statistical errors in matching precision dominate for the applied resistors, matching requirements are excessive for the worst case. For the string converter, the worst case has been found for all resistors in the upper half of the string being increased by the worst case tolerance and in the lower half being decreased by the worst case tolerance (or vice versa). The error at the node in the center of the string has to be below $\pm\frac{1}{2}$ LSB to reach the desired resolution. In reality, higher resolutions can be obtained considering the measured degree of matching. Measurements have shown that the matching error has a Gaussian distribution along the design center value. Therefore, a second approach was made that is based on statistical analysis of the resistor core and seems to be the more realistic one. Nevertheless, the statistical approach may be too optimistic for a higher number of coarse resistors ($m \ge 32$) in the intermeshed ladder architecture since the influence of gradients increases.

Monte Carlo simulations have been carried out using the simulator Pspice modeling, the matching error of the intermeshed ladder with a Gaussian distribution function. The simulations were restricted to the coarse resistors only ($m = 16$) because of their dominant matching requirements. In the case of a desired resolution of 10 b, the fine resistors have to match only within a 6-b precision. All error-sensitive nodes

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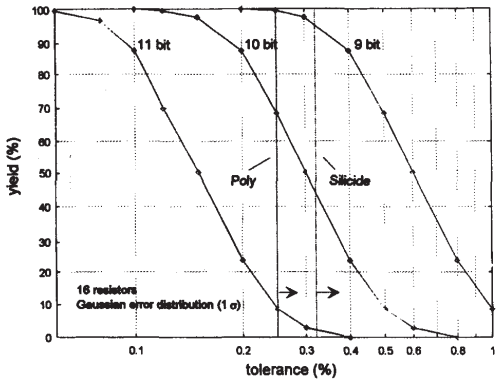


Fig. 8. Yield dependence on matching of resistors (Monte Carlo simulation).

(15) were monitored. A string was considered acceptable, if all nodes had an error below $\pm\frac{1}{2}$ LSB. The yield dependence for converters (9–11 b) on the degree of matching (Gaussian distribution 1σ) was analyzed, and the result is shown in Fig. 8. It can be seen that the measured precision can be realized for resistive converters with up to 10-b resolution with an acceptable yield.

VI. Conclusion

Based on the known effects limiting precision of resistor matching, methods for realizing high precision ratioed resistors in standard processes have been presented. Several test structures have been realized in a 1.5 μm HT-SIMOX and a 0.8 μm BiCMOS technology. The evaluation of dependence of matching behavior on resistor size showed that statistical errors dominate the resistor mismatch for small structures, while gradient (i.e., deterministic) errors dominate the mismatch for large resistors. Hence, an optimum size for resistor arrays can be found, which yields an optimum precision. In the SIMOX process [3], a matching precision of 0.25% was reached. It was found that bending had no measured influence on resistor precison. A worst case analysis showed that a converter resolution of 8 b can be reached using the intermeshed ladder principle. With a more realistic statistical analysis the intermeshed ladder converter can reach 10-b resolution with the SIMOX technology and 65% yield.

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949 a| QC176.A1I3 SC.18 1983 w| LCPER c| 1 i| 26090101001 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 001

949 a| QC176.A1I3 SC.19 1984 w| LCPER c| 1 i| 26090101002 d| 3/8/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 002

949 a| QC176.A1I3 SC.20 no.1-2 1985 w| LCPER c| 1 i| 26090101003 d| 2/1/2007 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 003

949 a| QC176.A1I3 SC.20 no.3-6 1985 w| LCPER c| 1 i| 26090101004 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 004

949 a| QC176.A1I3 SC.21 no.1-3 1986 w| LCPER c| 1 i| 26090101005 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 005

949 a| QC176.A1I3 SC.21 no.4-6 1986 w| LCPER c| 1 i| 26090101006 d| 2/3/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 006

949 a| QC176.A1I3 SC.22 no.1-3 1987 w| LCPER c| 1 i| 26090101007 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 007

949 a| QC176.A1I3 SC.22 no.4-6 1987 w| LCPER c| 1 i| 26090101008 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 008

949 a| QC176.A1I3 v.23 no.1-3 1988 w| LCPER c| 1 i| 26090101009 d| 1/16/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 009

949 a| QC176.A1I3 v.23 no.4-6 1988 w| LCPER c| 1 i| 26090101010 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 010

949 a| QC176.A1I3 v.24 no.1-3 1989 w| LCPER c| 1 i| 26090101011 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 011

949 a| QC176.A1I3 v.24 no.4-6 1989 w| LCPER c| 1 i| 26090101012 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 012

949 a| QC176.A1I3 v.25 no.4-6 1990 w| LCPER c| 1 i| 26090101014 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 014

949 a| QC176.A1I3 v.25 no.1-3 1990 w| LCPER c| 1 i| 26090101013 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 013

949 a| QC176.A1I3 v.26 no.4-6 1991 w| LCPER c| 1 i| 26090101016 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 016

949 a| QC176.A1I3 v.26 no.1-3 1991 w| LCPER c| 1 i| 26090101015 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 015

949 a| QC176.A1I3 v.26 no.7-9 1991 w| LCPER c| 1 i| 26090101017 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 017

949 a| QC176.A1I3 v.26 no.10-12 1991 w| LCPER c| 1 i| 26090101018 d| 5/24/2024 e| 5/14/2024 l| CATO-PARK m| UP-ANNEX n| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 018

949 a| QC176.A1I3 v.27 no.4-6 1992 w| LCPER c| 1 i| 26090101020 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 020

949 a| QC176.A1I3 v.27 no.7-10 1992 w| LCPER c| 1 i| 26090101021 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 021

949 a| QC176.A1I3 v.27 no.11-12 1992 w| LCPER c| 1 i| 26090101022 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 022

949 a| QC176.A1I3 v.28 no.1-6 1993 w| LCPER c| 1 i| 26090101023 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 023

949 a| QC176.A1I3 v.28 no.7-12 1993 w| LCPER c| 1 i| 26090101024 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 024

949 a| QC176.A1I3 v.29 no.1-6 1994 w| LCPER c| 1 i| 26090101025 d| 7/3/2019 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 025

949 a| QC176.A1I3 v.29 no.7-12 1994 w| LCPER c| 1 i| 26090101026 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 026

949 a| QC176.A1I3 v.30 no.1-6 1995 w| LCPER c| 1 i| 26090101027 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 027

949 a| QC176.A1I3 v.30 no.7-12 1995 w| LCPER c| 1 i| 26090101028 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 028

949 a| QC176.A1I3 v.31 no.1-6 1996 w| LCPER c| 1 i| 26090101029 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 029

949 a| QC176.A1I3 v.31 no.7-9 1996 w| LCPER c| 1 i| 26090101030 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 030

949 a| QC176.A1I3 v.31 no.10-12 1996 w| LCPER c| 1 i| 26090101031 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 031

949 a| QC176.A1I3 v.32 no.1-6 1997 w| LCPER c| 1 i| 26090101032 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 032

949 a| QC176.A1I3 v.32 no.7-12 1997 w| LCPER c| 1 i| 26090101033 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 033

949 a| QC176.A1I3 v.33 no.1-6 1998 w| LCPER c| 1 i| 26090101034 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 034

949 a| QC176.A1I3 v.33 no.7-12 1998 w| LCPER c| 1 i| 26090101035 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 035

949			a| QC176.A1I3 v.34 no.1-6 1999 w| LCPER c| 1 i| 26090101036 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 036
949			a| QC176.A1I3 v.34 no.7-12 1999 w| LCPER c| 1 i| 26110101017 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2611 0| 0101 1| 017
949			a| QC176.A1I3 v.35 no.1-6 2000 w| LCPER c| 1 i| 26110101018 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2611 0| 0101 1| 018
949			a| QC176.A1I3 v.35 no.7-12 2000 w| LCPER c| 1 i| 26110101019 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 11/1/2001 x| D z| 2611 0| 0101 1| 019
949			a| QC176.A1I3 v.36 no.1-6 2001 w| LCPER c| 1 i| 26110101020 d| 6/28/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 7/18/2002 x| D z| 2611 0| 0101 1| 020
949			a| QC176.A1I3 v.36 no.7-12 2001 w| LCPER c| 1 i| 26110101021 d| 6/28/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 7/18/2002 x| D z| 2611 0| 0101 1| 021
949			a| QC176.A1I3 v.37 no.1-6 2002 w| LCPER c| 1 i| 26110101022 d| 12/19/2024 e| 11/14/2024 l| CATO-PARK m| UP-ANNEX n| 2 q| 1 r| Y s| Y t| PERIODICAL u| 3/4/2003 x| D z| 2611 0| 0101 1| 022
949			a| QC176.A1I3 v.37 no.7-12 2002 w| LCPER c| 1 i| 26110101023 d| 12/17/2024 e| 11/14/2024 l| CATO-PARK m| UP-ANNEX n| 2 q| 1 r| Y s| Y t| PERIODICAL u| 3/4/2003 x| D z| 2611 0| 0101 1| 023
949			a| QC176.A1I3 v.38 no.1-6 2003 w| LCPER c| 1 i| 26110101024 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/5/2003 x| D z| 2611 0| 0101 1| 024
949			a| QC176.A1I3 v.38 no.7-12 2003 w| LCPER c| 1 i| 26110101025 d| 11/29/2004 e| 9/23/2004 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 9/7/2004 x| D z| 2611 0| 0101 1| 025
949			a| QC176.A1I3 v.39 no.1-6 2004 w| LCPER c| 1 i| 26110101026 d| 11/29/2004 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 9/7/2004 x| D z| 2611 0| 0101 1| 026
949			a| QC176.A1I3 v.39 no.7-9 2004 w| LCPER c| 1 i| 26110101027 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 027
949			a| QC176.A1I3 v.39 no.10-12 2004 w| LCPER c| 1 i| 26110101028 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 028
949			a| QC176.A1I3 v.40 no.1-3 2005 w| LCPER c| 1 i| 26110101029 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 029
949			a| QC176.A1I3 v.40 no.4-6 2005 w| LCPER c| 1 i| 26110101030 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 030
949			a| QC176.A1I3 v.40 no.7-9 2005 w| LCPER c| 1 i| 26110101031 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/25/2006 x| D z| 2611 0| 0101 1| 031
949			a| QC176.A1I3 v.40 no.10-12 2005 w| LCPER c| 1 i| 26110101032 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/25/2006 x| D z| 2611 0| 0101 1| 032
949			a| QC176.A1I3 v.41 no.1-3 2006 w| LCPER c| 1 i| 26060201001 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/25/2006 x| D z| 2606 0| 0201 1| 001
949			a| QC176.A1I3 v.41 no.4-6 2006 w| LCPER c| 1 i| 26060201002 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/25/2006 x| D z| 2606 0| 0201 1| 002
949			a| QC176.A1I3 v.41 no.7-9 2006 w| LCPER c| 1 i| 26060201003 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2006 x| D z| 2606 0| 0201 1| 003
949			a| QC176.A1I3 v.41 no.10-12 2006 w| LCPER c| 1 i| 26060201004 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/14/2006 x| D z| 2606 0| 0201 1| 004
949			a| QC176.A1I3 v.27 no.1-3 1992 w| LCPER c| 1 i| 26090101019 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 019
852	0	1	a| PSt b| UP-ANNEX c| CATO-PARK h| QC176.A1 i| I3
866		0	8| 0 a| SC.1(1966)-SC.22(1987); v.23(1988)-v.41(2006)
852	8		a| PSt b| HARRISBURG c| MICROS-HB h| Microfiche
866		0	8| 0 a| v.15(1980)-v.34(1999)
852	8		a| PSt b| HARRISBURG c| PERIOD-HB h| Periodical
866		0	8| 0 a| v.1(1966)-v.14(1979)

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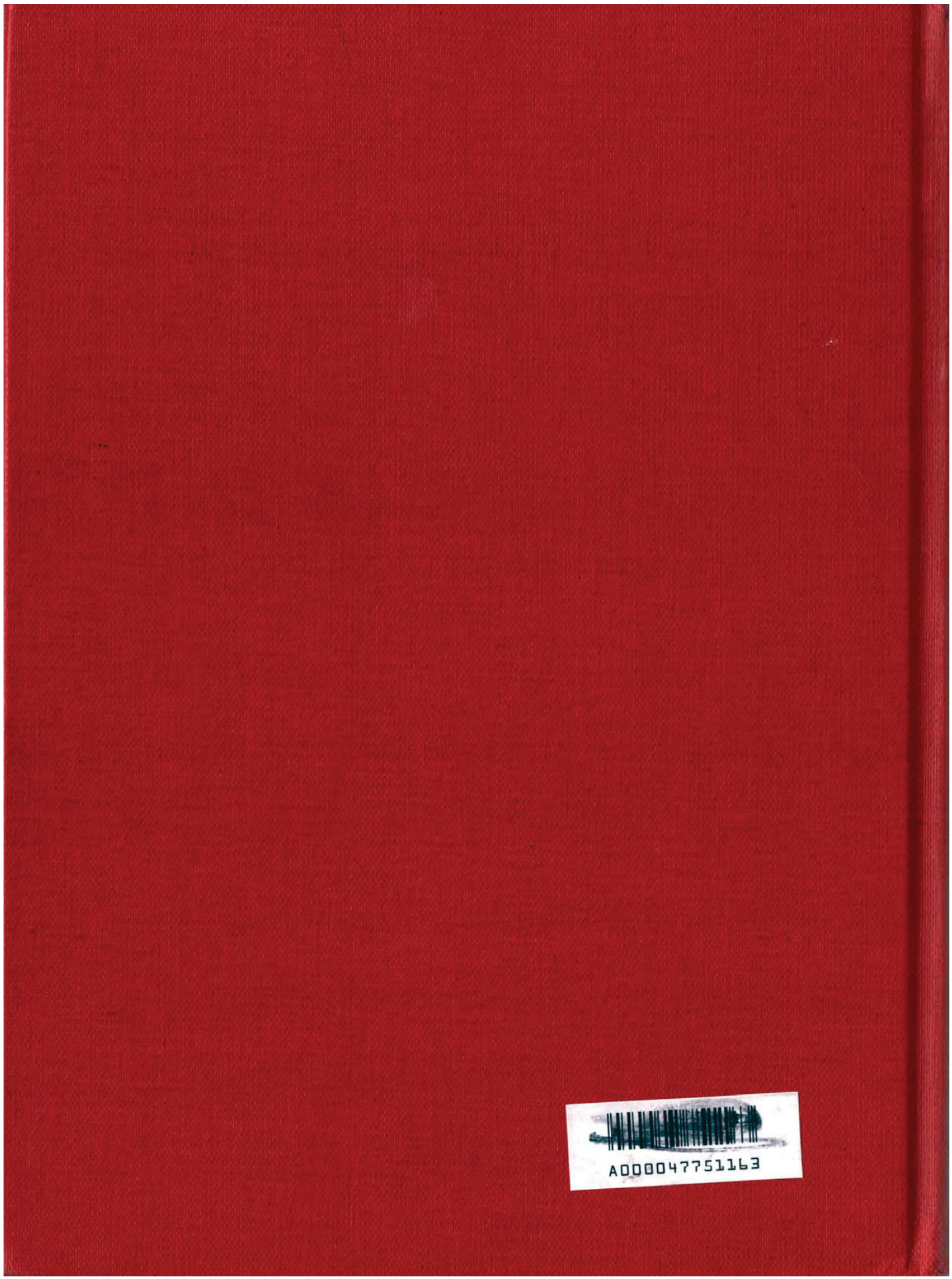
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A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications

Jacques C. Rudell, *Student Member, IEEE*, Jia-Jiunn Ou, *Student Member, IEEE*, Thomas Byunghak Cho, *Member, IEEE*, George Chien, *Student Member, IEEE*, Francesco Brianti, Jeffrey A. Weldon, *Student Member, IEEE*, and Paul R. Gray, *Fellow, IEEE*

***Abstract*— A monolithic 1.9-GHz, 198-mW, 0.6-μm CMOS receiver which meets the specifications of the Digital Enhanced Cordless Telecommunications (DECT) standard is described. All of the RF, IF, and baseband receiver components, with the exception of the frequency synthesizers, have been integrated into a single chip solution. A description is given of a wide-band IF with double conversion architecture which eliminates the need for the discrete-component noise and IF filters in addition to facilitating the eventual integration of the frequency synthesizer blocks with on-chip VCO's. The prototype device utilizes a 3.3-V supply and includes a low noise amplifier, an image-rejection mixer, and two quadrature baseband signal paths each of which includes a second-order Sallen and Key anti-alias filter, an eighth-order switched-capacitor filter network followed by a 10-b pipelined analog-to-digital converter (ADC). The experimental device has a measured receiver reference sensitivity of −90 dBm, an input referred IP3 of −7 dBm, a $P_{-1\,\mathrm{dB}}$ of −24 dBm, and an image-rejection ratio of −55 dBc across the DECT bands.**

***Index Terms*— Analog-to-digital converters, anti-alias filters, CMOS RF, Digital Enhanced Cordless Telecommunications, image-rejection mixers, low noise amplifiers, mixers, monolithic, radio architectures, radio receivers, switched-capacitor filters, wide-band IF double conversion, wireless communications.**

I. Introduction

THE proliferation of cellular, cordless, and PCS applications has driven the demand for portable communication systems which share the common requirement of a low-cost, low-power, small form-factor transceiver [1]. To address this need, recent research has been focused toward the development of a monolithic transceiver using a low-cost CMOS technology [2]–[7]. A single-chip CMOS transceiver requires the exploration of new systems and circuit design techniques which facilitate the highest levels of receiver and transmitter integration.

Commensurate with this trend toward integration is the evolution of numerous RF standards which define the specifications of any given transceiver. A single future portable communication system may well require the ability to utilize both the services provided by multiple RF standards and the flexibility afforded through multimodal operation. This consequently will demand the capability by a *single* transceiver to operate on standards with various carrier frequencies, channel bandwidths, sensitivity, and selectivity requirements. The increased functionality offered by a large high-integration system will be well suited to address the needs of a multimodal transceiver.

This paper describes a receiver system that achieves high levels of integration while exhibiting features potentially allowing operation on multiple RF standards. A prototype device based on this new wide-band IF double conversion (WBIFDC) architecture was realized in a 0.6-μm double-poly, triple-metal CMOS process and runs off of a 3.3-V supply. The experimental receiver, designed for specifications of the Digital Enhanced Cordless Telecommunications (DECT) standard, operates on a 1.9-GHz carrier and has the capability of detecting a signal amplitude of a microvolts at the low noise amplifier (LNA) input and generating a 10-b digital representation of the desired baseband channel. All of the required components to convert the desired signal from RF to baseband, with the exception of the frequency synthesizers, are integrated onto the prototype device which includes an LNA, an image-rejection mixer, two baseband filter stages, and two analog-to-digital converters (ADC).

Section II provides a brief review of two well-known receiver systems and introduces the wide-band IF with double conversion architecture. Section III provides an extended description of the wide-band IF system examining the merits and nonidealities of this architecture. Section IV discusses CMOS implementation issues of the wide-band IF system for the DECT standard. Finally, Section V presents test results obtained from the prototype device followed by a few concluding comments.

II. Receiver Architectures

Many issues are involved when attempting to translate a discrete-component receiver into an integrated form. To understand some of the barriers to integration, a review is given of a traditional superheterodyne system. Then two approaches to integration, a homodyne receiver and the wide-band IF with double conversion architectures are evaluated. Although there have been many recently proposed integrated architectures [6], [8], for the sake of brevity, only direct

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J. C. Rudell, J.-J. Ou, G. Chien, J. A. Weldon, and P. R. Gray are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA.

T. B. Cho is with San Francisco Telecom/Level One Communications, San Francisco, CA 94105 USA.

F. Brianti is with SGS Thomson, San Jose, CA 95110 USA.

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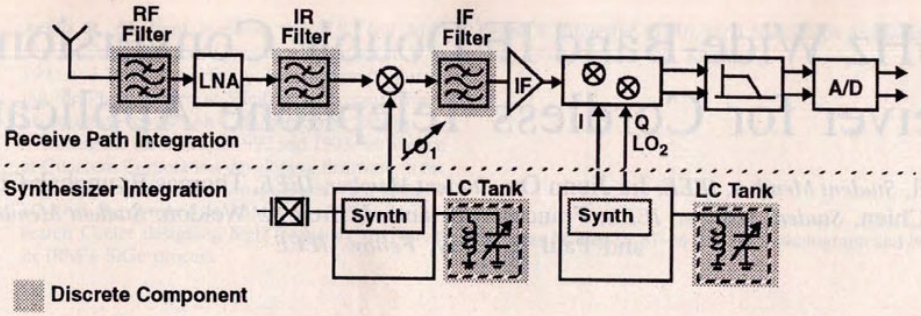


Fig. 1. Conventional superheterodyne receiver architecture.

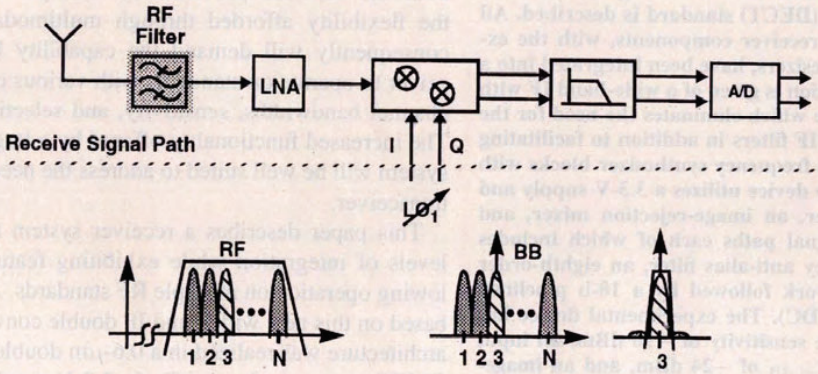


Fig. 2. Direct conversion receiver architecture.

conversion and wide-band IF with double conversion will be considered.

A. Conventional Superheterodyne Receiver

Most RF communication transceivers manufactured today utilize a conventional superheterodyne approach. In this system, shown in Fig. 1, implementation is achieved with a collection of discrete-component filters and various technologies such as gallium arsenide, silicon bipolar, and CMOS. The discrete-component RF front-end filter serves to remove out-of-band energy and perform rejection of image-band signals. The noise or image-rejection filter, which follows the LNA, further attenuates the undesired signals present at the image frequencies. An RF channel-select frequency synthesizer tunes the desired band to a fixed IF where a discrete-component filter performs a first-order attenuation of alternate channel energy. The IF filter, typically in combination with a variable gain amplifier, reduces the distortion and dynamic range requirements of the subsequent receiver blocks. High-performance, low phase-noise voltage controlled oscillators (VCO) are typically realized with discrete-component high-Q inductors and varactor diodes.

The high-Q associated with the discrete components found on a superheterodyne receiver is difficult and somewhat impractical to realize at high frequency as an integrated solution. A superior performance with respect to *selectivity*, a measure of a receiver's ability to separate the desired band about the carrier from signals received at other frequencies, and *sensitivity*, the minimal signal at the receiver input such that there is a sufficient signal-to-noise ratio at the receiver output [9], [10], can only be achieved with the use of high-Q discrete components found on a superheterodyne receiver. However, using these components runs contrary to the goal of high integration required by modern portable communication systems.

The challenge of fully integrating a receiver is to replace the functions traditionally implemented with the high performance, high-Q discrete components with integrated on-chip solutions. Problems associated with full integration of the receiver can be separated into two categories. First, the integration of the receive signal path requires the elimination of the noise or image-rejection filter and the discrete-component IF filter (see Fig. 1). Second, a fully integrated low-phase noise channel-select synthesizer must be realized using the relatively low-Q and poor phase-noise performance associated with on-chip VCO's. Two architectures which address the issues related to integration will now be discussed.

B. Direct Conversion Receiver (Homodyne)

One receiver architecture that eliminates many off-chip components in the receive signal path is the direct conversion, or homodyne architecture. In this approach, shown in Fig. 2, all of the in-band potential channels are frequency translated from the carrier directly to baseband using a single mixer stage. Energy from undesired channels is easily removed with on-chip filtering at baseband. In a direct conversion receiver, the IF stage is eliminated as is the need for image-rejection filtering.

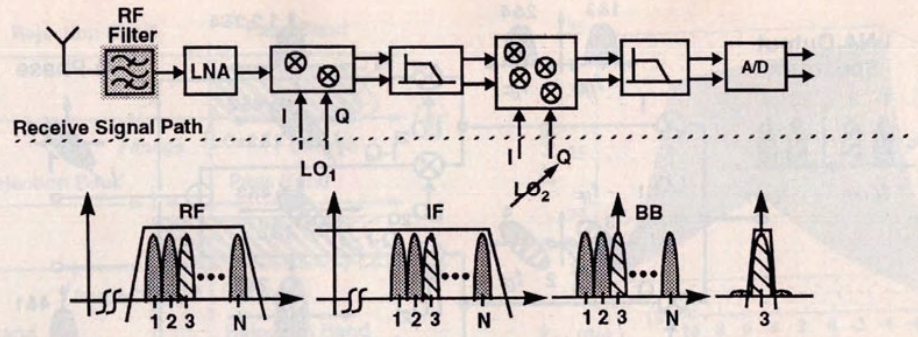


Fig. 3. Wide-band IF with double conversion receiver architecture.

TABLE I
RELATIVE COMPARISON OF RECEIVER ARCHITECTURE

Receiver Architecture	Required Discrete Filters	Channel Select Synthesizer	Potential for Multi-modal use	Channel Filtering	Image-Rejection
Superheterodyne	RF, Noise, IF	RF	Low	IF	RF & Noise Filter
Direct Conversion	RF	RF	High	Baseband	N/A
Wide-Band IF	RF	IF	High	Baseband	RF Filter &IR Mixer

Although the direct conversion receiver allows for higher levels of integration than a superheterodyne system, problems are associated with this architecture. Because the local oscillator (LO) is at the same frequency as the RF carrier, the potential exists for LO leakage to either the mixer input or to the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect off of nearby objects and be "re-received," consequently self-mixing with the local oscillator resulting in a time-varying or "wandering" dc offset at the output of the mixer [11]. This time-varying dc offset together with inherent circuit offsets significantly reduces the dynamic range of the receiver. In addition, a direct conversion receiver requires a high-frequency, low phase-noise, channel-select frequency synthesizer, which is difficult to achieve with a relatively low-Q integrated VCO.

C. Wide-Band IF with Double Conversion Receiver

An alternative architecture well suited for integration of the entire receiver is wide-band IF with double conversion [7]. Shown in Fig. 3, this receiver system takes all of the potential channels and frequency translates them from RF to IF using a mixer with a single frequency local oscillator. A simple low-pass filter is used at IF to remove any upconverted frequency components, allowing all channels to pass to the second stage of mixers. All of the channels at IF are then frequency translated directly to baseband using a tunable, channel-select frequency synthesizer. Alternate channel energy is then removed with a baseband filtering network where variable gain may be provided. This approach is similar to a superheterodyne receiver architecture in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscillator frequency translates all of the receive channels, maintaining a large bandwidth signal at IF. The channel selection is then realized with the lower frequency tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multistandard-capable receiver features.

In summary, Table I provides a high level comparison between the three receiver architectures discussed. Clearly, the highest performance receiver with respect to sensitivity and selectivity is the conventional superheterodyne architecture. However, the superior performance of this system is provided only with discrete-component solutions. In addition, the narrow-band discrete-component channel filters of the superheterodyne receiver tailor the particular implementation to a specific standard. Moreover, future portable transceivers will require smaller form factors which can be provided only through integrated solutions.

With respect to the two integrated architectures discussed, both direct conversion and wide-band IF perform channel filtering at baseband, allowing the possibility of a programmable integrated channel filter for multistandard receiver applications. In addition, as discussed in Section III, the wide-band IF architecture facilitates the integration of the synthesizer section of the receiver and provides a programmable image-rejection mixer.

III. WIDE-BAND IF ARCHITECTURE: EXTENDED DISCUSSION

The wide-band IF architecture offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The most important advantage is the fact that the channel tuning is performed using the second

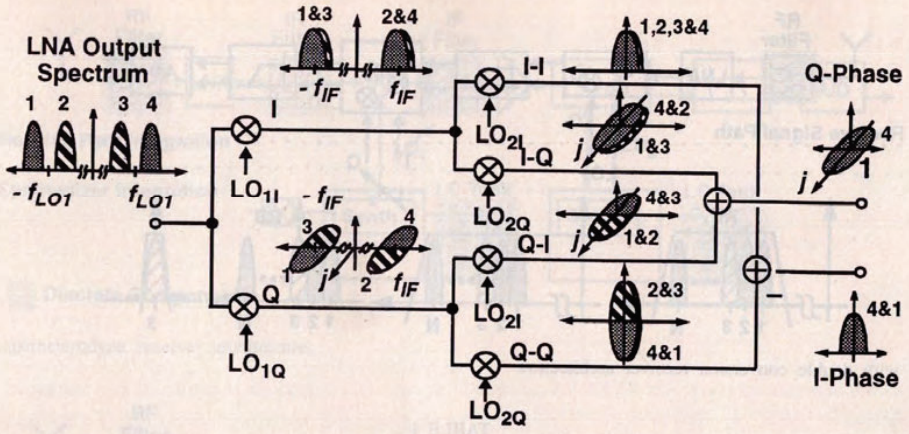


Fig. 4. Frequency domain interpretation of the wide-band IF image-rejection mixer. Low-pass filters not shown for simplicity.

lower-frequency, or IF, local oscillator but not the first, or RF, synthesizer. Consequently, the RF local oscillator can be implemented as a fixed-frequency crystal-controlled oscillator where several techniques may be utilized which allow the realization of low phase noise in the local oscillator output with low-Q on-chip components. One such approach is the use of wide phase-locked loop (PLL) bandwidth in the synthesizer to suppress the VCO contribution to phase noise near the carrier [12]–[14].

In addition, since channel tuning is performed with the IF local oscillator, operating at a lower frequency, a reduction in the required divider ratio of the phase-locked loop necessary to perform channel selection results. The noise generated by the reference oscillator, phase detector, and divider circuits of a PLL all contribute to the phase noise performance of a frequency synthesizer. With a lower divider ratio, the contribution to the frequency synthesizer output phase noise from the reference oscillator, phase detector, and divider circuits can be significantly reduced. Moreover, a lower divider ratio implies a reduction in spurious tones generated by the PLL [15], [16].

Another advantage associated with the wide-band IF architecture is that there are no local oscillators which operate at the same frequency as the incoming RF carrier. This eliminates the potential for the LO retransmission problem that plagues a direct conversion system and results in *time-varying* dc offsets. Although the second local oscillator is at the same frequency of the IF desired carrier in the wide-band IF system, the offset which results at baseband from self mixing is relatively constant and may be cancelled using one of the proposed methods described in [17] and [18].

A. Image-Rejection in the Wide-Band IF System

In the wide-band IF receiver, the signal is mixed to a finite IF; therefore, the image problem is reintroduced in this system. However, because the two frequency translations occur in cascade, the architecture used lends itself to easy implementation of the image-reject function using a six-mixer configuration. This image-rejection mixer which shares a similarity to the Weaver technique [19] is best understood with a frequency domain interpretation for a real valued input signal (Fig. 4). The RF carrier is first multiplied by in-phase and quadrature local oscillators and converted to IF. The spectrum at IF is the result of a convolution in the frequency domain of the RF carrier with both a sine and cosine. At IF, there exists a known phase relationship between the image and desired frequency bands. This phase relationship is further exploited with a complex mixing from IF to baseband. If the upconverted terms from the mixer are removed by low-pass filtering at IF and baseband, then by properly adding the four baseband channels in pairs, the image frequencies can be made to cancel while the desired band adds constructively for both the I and Q channels. This image-rejection mixer has the property that any incoming frequency below the frequency of the first local oscillator ideally is rejected, while any frequency above the first LO is passed. If the IF is made high enough, additional image rejection may be obtained from the RF front-end filter.

This particular image-rejection mixer topology has several advantages. First, lossy passive phase-shifting filters are not required in the signal path to generate the correct phase between the image and desired bands. Second, assuming again that the upconverted terms are removed, the image-rejection is very wide-band. It can be further shown that the edge of the image-attenuation band is set by the frequency of the first local oscillator (LO1) which leads to the third advantage. If it is assumed that a multistandard capable receiver is built where the frequency of LO1 can perform a coarse adjustment to accommodate the carrier frequency of a different standard, then the image rejection will follow the first LO, or it can be thought of as a self-aligning image-rejection mixer. Two hypothetical LO1 frequencies, labeled f_{LO1a} and f_{LO1b}, necessary to properly frequency translate the carrier of two different standards are shown in Fig. 5(a) and (b). Both the passband and the rejection band as a function of the frequency referred to the mixer input are aligned to LO1. Assuming that the desired band is above LO1 in frequency, the image-rejection will be self aligned. Further flexibility using this mixer configuration may be obtained by reversing the polarity of the four baseband channels before they are summed together at the mixer output. This has the effect of retaining the lower

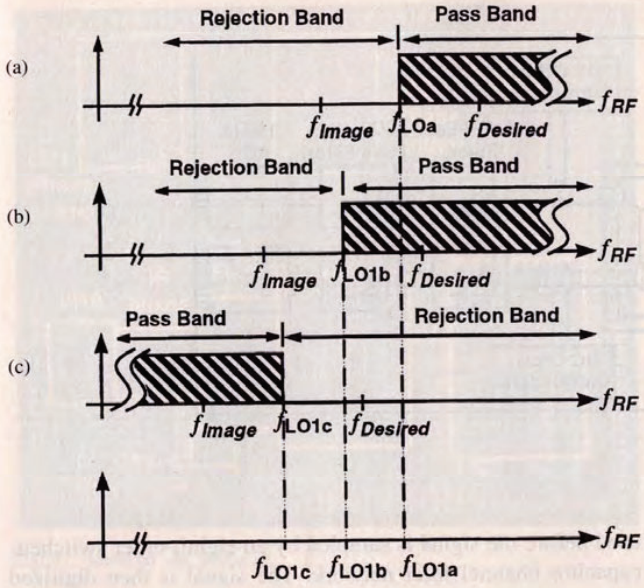


Fig. 5. Self-aligning image-rejection mixer. (a) f_{LO1a} and (b) f_{LO1b} two different LO1 frequencies and their relationship to the rejection and pass band of the image-rejection mixer. (c) f_{LO1c} case when the polarity of the baseband channels are reversed before the summation.

sideband about LO1 while rejecting the upper sideband. This concept is illustrated in Fig. 5(c).

B. Nonidealities of the Wide-Band IF Double Conversion System

Although the wide-band IF system has advantages with respect to high integration, certain nonidealities limit the overall receiver performance. These are now discussed.

Because the first local oscillator is fixed in frequency, all of the channels must pass through the IF stage and the desired channel is selected with the second LO. This has two problematic implications. First, as a result of moving the channel selection to a lower frequency, the IF synthesizers require a VCO with the capability of tuning across a broader frequency range as a percentage of the nominal operating frequency. Second, by removing the channel select filter at IF, strong adjacent channel interferers are now a concern for the second mixer stage as well as the baseband blocks. This implies a higher dynamic range requirement of these latter receiver stages. In addition, spurious tones generated by the IF local oscillator can mix with undesired IF channels creating in-band interference at the output of the second mixer stage. Additional care must be taken when developing a frequency plan to guard against digital baseband clock signals and their harmonics falling within the range of the desired IF channels.

As with conventional image-rejection mixer systems [20]–[24], the magnitude of the image attenuation in the wide-band IF architecture is a function of the phase mismatch between both the I and Q phase of the first and second local oscillators and the gain matching between the signal paths. A detailed derivation for the image-rejection performance as a function of phase and gain mismatch is given in Appendix A.

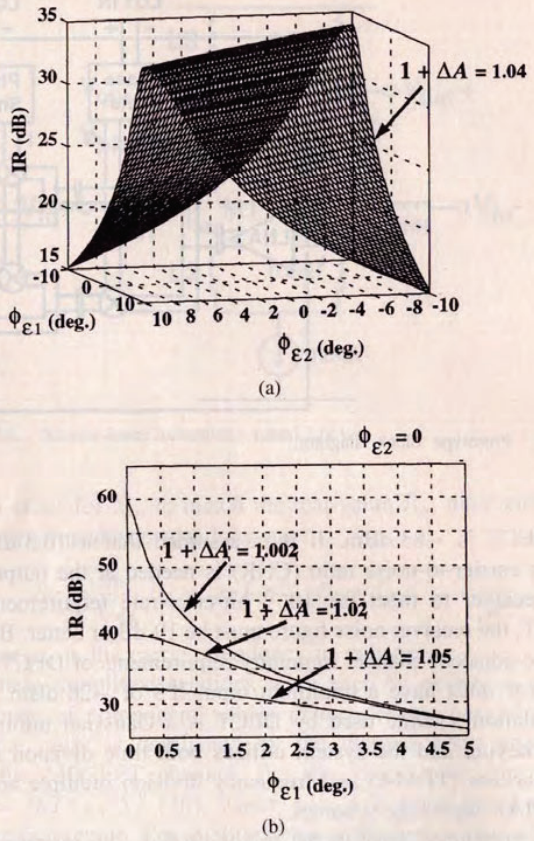


Fig. 6. Image rejection as a function of LO phase mismatch. (a) Illustrating IR dependence on $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$. (b) IR as a function of $\phi_{\varepsilon 1}$ and gain mismatch, $\phi_{\varepsilon 2} = 0$.

The image rejection as a function of the mismatch is given by

$$IR(\text{dB}) = 10 \cdot \log \left[\frac{1 + (1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})} \right] \quad (1)$$

where $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ represent the deviation of the local oscillators from quadrature in the first and second LO's, respectively, while ΔA is the aggregate gain error along the I and Q signal paths. A plot of (1) is given in Fig. 6. With a sufficiently high intermediate frequency, the image-rejection may be performed with a combination of the RF front-end filter and this image-rejection mixer. Using this approach, most applications will require better than 35 dB of image-rejection from the six-mixer configuration. Under prefect gain matching, the phase error of the local oscillator can be no great than 2° while with perfect phase matching the gain error between any two of the four signal paths must be less than 3.6%.

IV. DECT Prototype Receiver

A prototype receiver utilizing the wide-band IF architecture was designed to meet the specifications of the DECT standard [25]. In DECT, there are ten channels which are 1.728 MHz wide with carrier frequencies that range from 1.881–1.897 GHz. The required receiver reference sensitivity

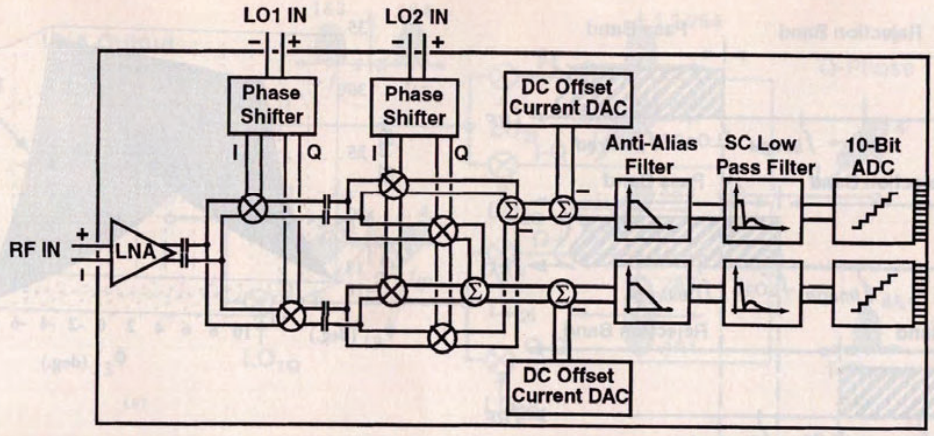


Fig. 7. Prototype block diagram.

of DECT is −83 dBm. If it is assumed that a 10.3 dB or better carrier-to-noise ratio (CNR) is needed at the output of the receiver to meet the 10^{-3} bit-error-rate requirement of DECT, the receiver noise figure must be 19 dB or better. Based on the adjacent channel immunity requirements of DECT, the receiver must have a minimum input IP3 of −26 dBm. The modulation scheme used by DECT is a Gaussian minimum shift keying and the system utilizes both time division multiple access (TDMA) and frequency division multiple access (FDMA) duplexing schemes.

As mentioned later in the mixer section, the intermediate frequency for the desired carriers reside from 181–197 MHz. Given that the carrier frequency is at 1.89 GHz, the image signals fall in the 1.503–1.519 GHz band. In DECT, the receiver is required to properly detect a −80 dBm carrier in the presence of an out-of-band blocker −23 dBm below 1.78 GHz [25]. Therefore, to obtain the required CNR in the presence of the 1.5 GHz out-of-band blocker, the image-rejection can be expressed as

$$IR(\mathrm{dB}) = CNR(dB) + (Blocker_{1.5\ \mathrm{GHz}}(dBm) - DesiredCarrier(dBm)). \quad (2)$$

Therefore, for this particular receiver implementation of DECT, approximately 70 dB or more of image-rejection is required.

A. Prototype Description

A diagram of all the blocks included on the prototype chip is shown in Fig. 7. At the RF and LO signal ports of the receiver, a single-ended-to-differential conversion takes place with an external balun allowing the higher frequency signals to be brought on-chip differentially. To reduce the impact of coupling between blocks in the receiver, the entire signal path across the chip was made fully differential. The LNA is ac-coupled to the input of the RF mixers, while the first mixer stage is ac-coupled to the second set of mixers. At baseband, two offset current digital-to-analog converters (DAC's) are used to mitigate any effect due to LO self-mixing in the second mixer stage. A Sallen and Key anti-aliasing filter is used before the signal is sampled by an eighth-order switched-capacitor channel filter network. The signal is then digitized using a 10-b, 10 MS/s ADC. The digital output is driven off-chip using source-coupled logic to reduce the effects of digital substrate noise coupling. Quadrature LO's are realized with a second-order polyphase filter before being applied to the mixer input [24]. The wide-band IF architecture is intended to be eventually integrated with the frequency synthesizer. Therefore, the polyphase filters found on this prototype are for testing purposes only.

All circuits on this chip use a 3.3-V supply. All pads are electrostatic discharge (ESD) protected with reversed-biased PN diodes including the LNA input. To further reduce the possibility of coupling effects due to parasitic bondwire inductances, a self-biased on-chip current source is replicated throughout the RF and IF sections of the receiver. This bias circuit which includes an adjustable current DAC is further described in [26] and [27]. All bias circuits, gain control for the RF, and baseband sections, as well as the ADC clocking frequency and various other options are controlled by two sets of 50-b serial-input shift registers.

A die photo is shown in Fig. 8. The chip was fabricated in a 0.6-μm double-poly, triple-metal CMOS process. The die size is 7.5 mm by 6.5 mm while the active chip area is 15 mm^2. A description of each circuit block in the receiver chain will now be given starting with the LNA.

B. Low Noise Amplifier (LNA)

Essential requirements of the LNA are low noise, high linearity, moderate gain, and low power consumption. Since the linearity performance is dominated by the stages which follow the LNA, the primary goal in this LNA design is to minimize the power consumption for the required noise figure. In a standard 0.6-μm CMOS process, the device f_T is typically below 10 GHz when biased at 0.5 V ($V_{gs}-V_t$). This makes the conventional wide-band approach somewhat impractical and a narrow-band design an attractive alternative. In addition, the bandpass frequency response of a narrow-band LNA helps to perform some image-attenuation and increases the immunity of the front-end to low-frequency digital baseband signals. To

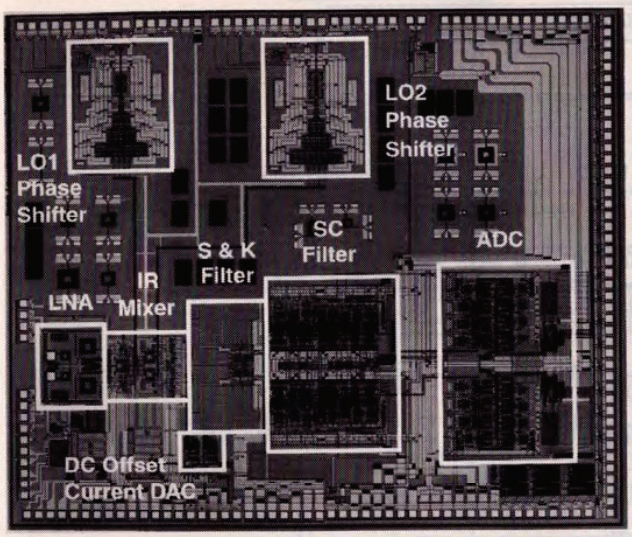


Fig. 8. Receiver die photo

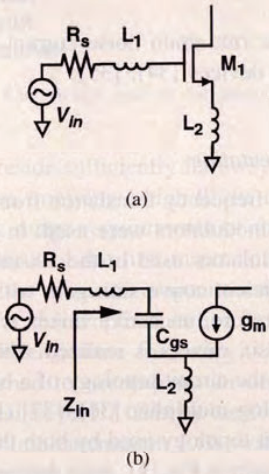


Fig. 9. Inductor-degenerated common-source LNA: (a) topology and (b) small signal model.

realize this approach, an inductively degenerated common-source amplifier topology [28], [29] was selected, as shown Fig. 9(a). This configuration has the advantage that it provides both current gain and voltage gain, thus reducing the noise contribution of the following stages. Moreover, by utilizing inductive degeneration, a real-part impedance matching is achieved without the use of a physical resistor, which would degrade the LNA's noise figure.

The actual noise performance of the LNA is heavily influenced by nonidealities in devices and passive components, which are difficult to fully model. However, some insight can be obtained from an ideal circuit model, shown in Fig. 9(b), where C_{gd} is neglected and R_s is the source impedance. The input impedance may now be expressed as

$$Z_{\text{in}} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_2. \tag{3}$$

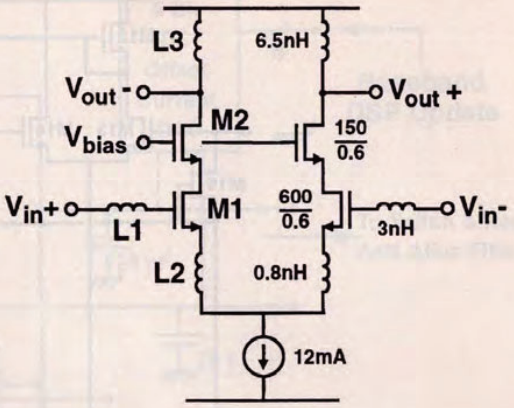


Fig. 10. Narrow-band inductively tuned LNA.

In order for Z_{in} to match the real-value R_s, the conditions for this impedance matching are

$$R_s = \frac{g_m}{C_{gs}} L_2 = \omega_T L_2; \quad (L_1 + L_2)C_{gs} = \frac{1}{\omega_c^2} \tag{4}$$

where ω_c is the carrier frequency in radians/s.

These simplified relations were used to obtain an initial estimate of component values in the design. Assuming the device noise is dominated by the thermal noise produced by the MOSFET channel, the rms drain noise current is $\overline{i_d^2} = 4kT\gamma g_m \Delta f$ [30], where $\gamma = 2/3$ when based in the saturation region. The quality factor of the entire input network is

$$Q_{\text{in}} = \frac{1}{R_s} \frac{1}{\omega_c C_{gs}} = \frac{1}{R_s} \omega_c (L_1 + L_2). \tag{5}$$

Now the input-referred noise figure (NF) under a matched condition can be expressed as

$$\text{NF} = 1 + \gamma \frac{1}{R_s} \frac{1}{g_m} \frac{1}{Q_{\text{in}}^2}. \tag{6}$$

Equation (6) shows that the NF can be reduced by increasing Q_{in}, breaking the classical tradeoff between noise figure and power consumption of the LNA. This now allows the LNA linearity to be traded-off with the noise figure for a given power consumption.

The complete implementation of the LNA is shown in Fig. 10. A differential configuration was selected to improve the common-mode rejection of spurious digital noise and substrate noise coupling. Cascode device M_2 provides better reverse isolation and alleviates the effect of C_{gd} of M_1. The relatively high-Q parasitic inductance associated with the LNA input bondwires were used to realize L_1. However, due to the differential configuration along with the desire to integrate all elements of the LNA, L_2 was implemented as an on-chip low-Q spiral inductor.

A key advantage associated with this highly integrated receiver architecture is that the 50-Ω matching is not required at the LNA output. Therefore, a spiral inductor L_3 was used at the LNA output to tune out the capacitance associated with the mixer input. This results in an enhancement of the output impedance and LNA voltage gain.

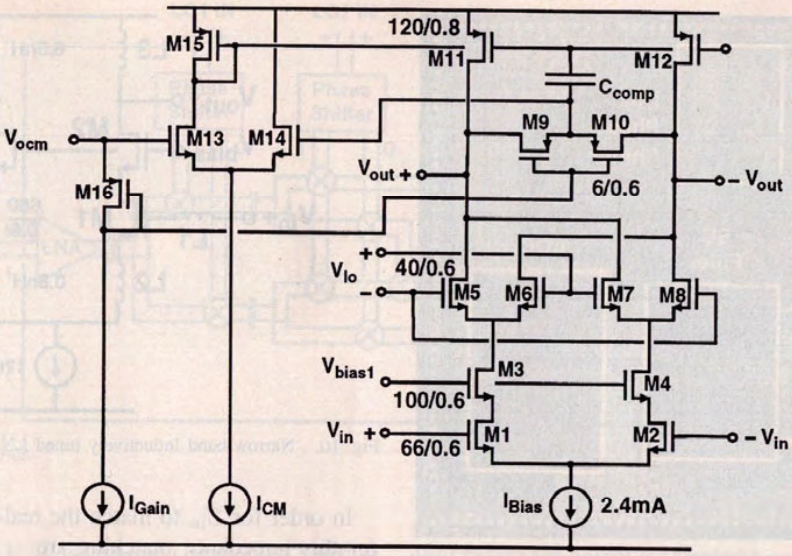


Fig. 11. One of two mixers used to translate the RF signal to IF. CMOS variant of the Gilbert cell multiplier.

On-chip spiral inductors [32] were created with the top two layers of metal, while the bottom layer of metal was used as the bridge connecting the center of the spiral to an outside terminal. Greenhouse formulas [33] were used for the initial design while EM, a commercial software package by Sonnet, performed a $2\frac{1}{2}$-dimension electromagnetic simulation to confirm the final design. The result was transformed to a simple π model which was then used for the final circuit simulation in SPICE.

Actual LNA performance is different from the idealized model because of the nonidealities in active and passive components. As the operating frequency approaches the device f_T, the assumption of the MOSFET quasi-static behavior no longer holds. A first-order nonquasi-static (NQS) model can be applied to the circuit simulation by adding a resistor in series with the gate terminal, $R_{\rm nqs} = 1/(5g_m)$ [31]. To improve the LNA noise figure, $Q_{\rm in}$ can be increased by decreasing the input device size which reduces C_{gs}. However, if the device size is too small, $R_{\rm nqs}$ becomes significant, increasing the overall noise figure. Ideally, an optimal $Q_{\rm in}$ can be achieved by balancing between the noise from the MOSFET channel and the noise which results from the NQS behavior. However, increasing $Q_{\rm in}$ implies large values of inductors. For this design, both on-chip spiral and bondwire inductors limited $Q_{\rm in}$ to approximately two to three.

In addition to the noise contribution of device M_1, the overall noise figure is further degraded by the cascode device M_2 and a finite Q of the inductors. The noise from M_2 is nonnegligible because at high frequency the impedance looking into the drain of M_1 is low. Simulation results show the noise contribution from M_2 is approximately 2/3 of the noise contribution from M_1.

Compared to a simulated NF of 3.5 dB, the observed noise figure of the individual LNA testing chip is 5 dB. This discrepancy mainly results from the inadequate thermal noise model of the short channel MOSFET devices. The assumption of $\gamma = 2/3$ in the rms drain noise current may not be valid for short-channel devices [34], [35].

C. Mixer Implementation

To perform the frequency translation from RF to baseband, down-conversion modulators were used. In addition to image rejection, the modulators used in the six-mixer configuration must provide sufficient conversion gain with a minimal noise contribution. Therefore, an active mixer was selected. Each of the individual six mixers is realized with a CMOS active mixer resembling the circuit topology of a bipolar Gilbert cell four-quadrant analog multiplier [36], [37] (Fig. 11).

The basic circuit topology used by both the first and second mixer stages is shown in Fig. 11, with the exception that triode region devices M_9 and M_{10} are replaced with p^+ diffusion resistors in the second mixer stage. The input transconductance stage consists of a simple differential pair M_1 and M_2. The cascode devices M_3 and M_4 provide better LO-to-RF isolation. M_5–M_8 act as switches in the mixer. Triode region devices M_9 and M_{10} are used to set both the load and the gain which may be modulated on-chip by varying the current through diode-connected device M_{16}. Common-mode feedback is achieved with devices M_{13}, M_{14}, M_{15}, and the current source consisting of M_{11} and M_{12}. Compensation for the common-mode feedback loop is provided with $C_{\rm comp}$. To remove any dc offsets from the first mixer and accommodate a level shift between the output of the first mixer stage and the input to the LO2 mixers, a 2.6-pF coupling capacitor was used (see Fig. 12).

Selection of the local oscillator and IF frequencies involves several tradeoffs. Gain and phase mismatch within the signal paths of the mixer limit the practical image attenuation to 35 dB. Therefore, to meet the image-rejection requirement of 70 dB, some filtering must be performed by the front-end RF filter. However, to make full use of this filter, the

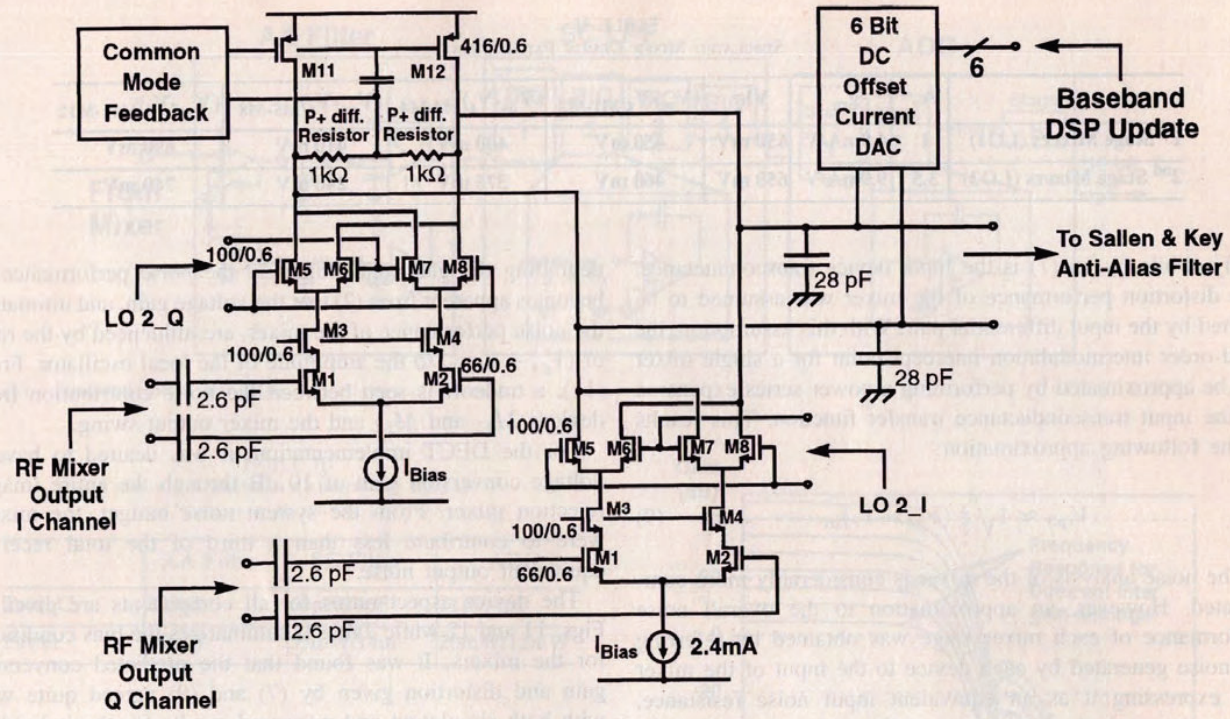


Fig. 12. Two of the four mixers used in the second mixer stage using LO2.

image-band must reside sufficiently far away from the desired carrier in frequency, implying a high IF. In addition, a high IF reduces the tuning range requirements of the IF synthesizer. In contrast, the output of the first mixer is a high impedance node. Therefore, the parasitic capacitance and the silicon technology used for this implementation set an upper bound on the allowable intermediate frequency. Originally, the RF mixers were designed to accompany an on-chip synthesizer where LO1 was limited to 1.7 GHz by the 0.6-μm technology. Therefore, in this implementation LO1 was set to 1.7 GHz requiring LO2 to range from 181–197 MHz.

To remove the upconverted terms, a low-pass filter is required at the IF node. The output resistance of the RF mixers in combination with the parasitic capacitance at the IF node together create the required RC time constant. Unfortunately, a problem associated with this particular implementation of the wide-band IF system is that at the first mixer output, the 3 dB frequency is 160 MHz which is much lower than desired. At IF, the desired channels range from 181–197 MHz which implies a significant gain penalty for the RF mixers. Using a 0.6-μm CMOS technology, the drain junction capacitance of the switches and the current source at the output of the first mixer, the gate capacitance of the input devices of the second mixer stage, and the parasitic capacitance of the ac-coupling capacitor severely limit the bandwidth and the gain of the mixer.

The output current from two of the four IF-to-baseband mixers are added together to correctly sum the signals for image cancellation, as shown in Fig. 12. A pair of 6-b dc offset current DAC's are then used to mitigate the effects of any LO2 self-mixing and to compensate for dc offset in the subsequent baseband switched-capacitor filter stages. The offset current DAC on this chip can be updated with a baseband DSP using an algorithm as described in [17] and [18]. At the current summing node, the first pole of the anti-alias filter is created with the mixer output resistance loaded by a 28-pF capacitor. The low-pass filter created at the output of the first mixer stage in combination with the Sallen and Key filter serve a dual purpose, to remove the upconverted IF mixer components and perform anti-alias filtering for the subsequent switched-capacitor blocks.

Similar to the LNA, physical insight may be gained when designing each of the individual mixer cells by creating an idealized model. Simplified expressions for the voltage conversion gain, input referred voltage IP3, and equivalent input noise contribution from each device in the mixer are given with (8)–(11). These relationships were used to make initial estimates before simulation in SPICE.

Assuming a square-law MOSFET device, the conversion gain of an individual mixer can be approximated by averaging the gain over one period of the local oscillator, as shown in Appendix B. This results in the following analytical expression:

$$A_v \approx g_m R_L \left(\frac{2}{\pi}\right)\left(1 - \frac{\sqrt{2}(V_{gs}-V_t)_{\rm sw}}{\pi V_{LO}}\right) \quad (7)$$

or

$$A_v \approx \frac{I_{\rm Bias}}{(V_{gs}-V_t)_{\rm in}} R_L \left(\frac{2}{\pi}\right)\left(1 - \frac{\sqrt{2}(V_{gs}-V_t)_{\rm sw}}{\pi V_{LO}}\right) \quad (8)$$

where $(V_{gs}-V_t)_{\rm in}$ and $(V_{gs}-V_t)_{\rm sw}$ are the $(V_{gs}-V_t)$ of the input devices M_1 and M_2 and the switches M_5–M_8, respec-

TABLE II
SIMULATED MIXER DESIGN PARAMETERS

	A_v	g_m	Vlo	$(V_{gs}-V_t)_{M1-M2}$	$(V_{gs}-V_t)_{M3-M4}$	$(V_{gs}-V_t)_{M5-M8}$	$(V_{gs}-V_t)_{M11-M12}$
1st Stage Mixers (LO1)	1	4.9mA/V	650 mV	450 mV	400 mV	410 mV	690 mV
2nd Stage Mixers (LO2)	3.5	9.9mA/V	650 mV	460 mV	375 mV	240 mV	740 mV

tively, while g_m in (7) is the input device transconductance. The distortion performance of the mixer was assumed to be limited by the input differential pair. With this assumption, the third-order intermodulation intercept point for a single mixer can be approximated by performing a power series expansion on the input transconductance transfer function. This results in the following approximation:

$$V_{ip3} \approx 4\sqrt{\tfrac{2}{3}}\,(V_{gs}-V_t)_{\text{in}}. \tag{9}$$

The noise analysis of the mixer is considerably more complicated. However, an approximation to the overall noise performance of each mixer stage was obtained by referring the noise generated by each device to the input of the mixer and expressing it as an equivalent input noise resistance, where the equivalent input rms noise voltage is given by $\overline{v_{\text{eqin}}^2} = 4kTR_{\text{eqin}}\Delta f$.

Noise generated by the LNA in the image-band will to first-order be cancelled when going through the image-rejection mixer. Devices M_1–M_8 in the first mixer stage add noise which is uncorrelated as the noise passes through the image-rejection mixer. Therefore, devices M_1–M_8 in the first mixer stage are single sideband (SSB) noise sources, while all other devices in the receive path are double sideband (DSB) noise sources.

The equivalent input noise resistance generated by devices M_1 and M_2 is described as

$$R_{\text{eqin}} \approx 2\left(\gamma \cdot \frac{(V_{gs}-V_t)}{I_Bias}\right) \cdot k \tag{10}$$

where $k = 2$ (SSB) for the first mixer stage (LO1) and $k = 1$ (DSB) for the second mixer stage (LO2). I_{Bias} is the mixer tail current. The equivalent input noise resistance due to the active current source and the load resistance can be referred to the input as

$$R_{\text{eqLOAD}} \approx \frac{R_L^2}{A_v^2}\left(\frac{1}{R_L} + \frac{I_{\text{Bias}}/2}{(V_{gs}-V_t)_{\text{Load}}}\right) \cdot 2 \tag{11}$$

where A_v is the voltage conversion gain given by (8). R_L is the load resistance from either the triode devices M_9 and M_{10} or the p^+ diffusion resistor in the second mixer stage, while $(V_{gs}-V_t)_{\text{Load}}$ is the $(V_{gs}-V_t)$ of M_{11} and M_{12} in Fig. 11. The noise analysis from the switches is considerably more complicated and can be analyzed using the approach given in [38].

Equations (7)–(11) reveal the classic tradeoff between gain, noise, and distortion. Essentially, a higher $(V_{gs}-V_t)$ for the input devices improves the distortion performance while degrading the gain and ultimately the noise performance. It becomes apparent from (7) that the voltage gain, and ultimately the noise performance of the mixer, are influenced by the ratio of $(V_{gs}-V_t)_{\text{sw}}$ to the amplitude of the local oscillator. From (11), a tradeoff is seen between the noise contribution from devices M_{11} and M_{12} and the mixer output swing.

For the DECT implementation, it was desired to have a voltage conversion gain of 10 dB through the entire image-rejection mixer. From the system noise budget, the mixers were to contribute less than a third of the total receiver equivalent output noise.

The device aspect ratios for all components are given in Figs. 11 and 12 while Table II summarizes the bias conditions for the mixers. It was found that the predicted conversion gain and distortion given by (7) and (9) agreed quite well with both simulation and measured results for the individual mixers and the entire image-rejection configuration. However, the measured noise performance was significantly more than predicted. The difference is believed to be related to the inadequate device noise model. A $\gamma = \frac{2}{3}$ was assumed for the thermal noise calculations, which may not have been accurate. In addition, the unity conversion gain limitation of the first mixer stage results in a significant noise penalty.

To minimize the mismatch between the different mixer and LO signal paths, exceptional care was taken during layout. Common centroid techniques were used throughout the image-rejection mixer. The quadrature local oscillator signals used by the mixer were generated using a polyphase filter described by [24].

D. Baseband Filters and ADC

Similar to a direct conversion receiver, the wide-band IF front-end downconverts all channels to baseband before any filtering is performed. The primary objective of the baseband filter section is to remove all of the alternate channel energy while adjusting the amplitude of the desired signal which results in a reduced dynamic range requirement for the ADC. The baseband filter and ADC utilized by this receiver have been previously described [39]–[42]. A description of the baseband filter and ADC as they relate to the DECT receiver will now be outlined. A block diagram of the baseband section is given in Fig. 13.

E. Sallen and Key Anti-Alias Filter

Before the signal is sampled by the switched-capacitor filter, an anti-alias filter must be used. The objective is to filter any energy that could potentially alias into the band of the desired signal as a result of sampling. This is of particular concern in highly integrated receivers where it is possible to have a

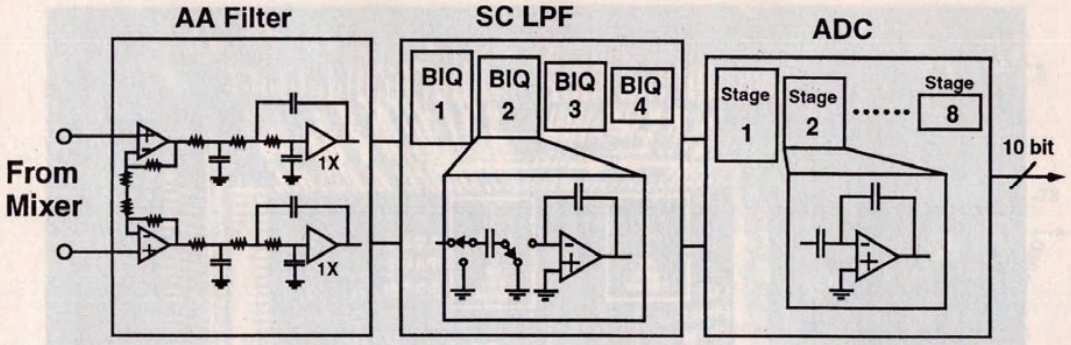


Fig. 13. Baseband filters and ADC.

TABLE III
COMPARISON BETWEEN CAPACITIVELY SCALED AND NONSCALED BASEBAND SECTIONS

	AA Filter	SC Filter	ADC
Total C	200pF	60pF/24pF	11pF/4pF
Power	10mW	35mW/14m	20mW/12mW

weak desired signal in the presence of large adjacent channel interferers which see little if any attenuation before the anti-aliasing filter. For the DECT receiver, a sampling frequency of 31.1 MS/s was selected for the switched-capacitor sampled data circuits which follow the Sallen and Key filter. The 3-dB bandwidth of the desired signal is 700 kHz. Therefore, the blocking requirements at 30.4 MHz (31.1–700 kHz) define the required anti-alias filtering at this frequency. For DECT, a −80-dBm desired carrier must be received with an adequate CNR in the presence of a blocker potentially −23 dBm 30.4 MHz away from the carrier. Thus, on the order of 70 dB of attenuation is required by a combination of the RF front-end filter and the anti-alias filter before sampling may occur at baseband.

Anti-alias filtering for the baseband sampled-data filters is performed by a series of cascaded poles. The output impedance of the IF-to-baseband mixers is in parallel with a 28-pF capacitance to form the first pole (see Fig. 12). A noninverting amplifier is then used with resistive feedback to create a 2× gain stage which reduces the noise contribution from the subsequent filter blocks. A second pole is then introduced at the output of the 2× gain stage. This is then followed by a second-order Sallen and Key filter. The 3-dB frequency of the composite continuous time filter is 1.5 MHz, which provides more than 70 dB of rejection 30.4 MHz away from the carrier. Additional attenuation in this band will also be provided by the RF front-end filter. P^+ diffusion resistors were used with poly-poly capacitors to create the filter poles. The filter was designed to have an adequate frequency response for DECT performance over all process corners.

F. Switched-Capacitor Channel-Select Filter

After the anti-alias filter, the signal is sampled and put through an eighth-order switched-capacitor filter, which performs channel filtering and provides variable gain from 0–42 dB in 6-dB increments. The switched-capacitor filter has an equiripple frequency response. After filtering and gain control, the dynamic range requirements of the ADC are now reduced to 10 b.

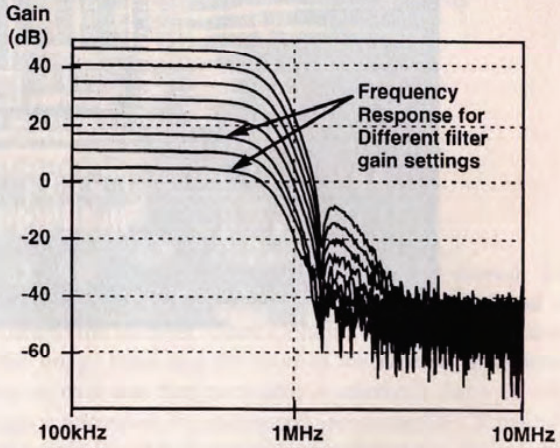


Fig. 14. Measured filter response, stand-alone baseband filters.

The switched-capacitor filter is comprised of four biquad stages. The first three biquad stages perform channel filtering, while the last stage equalizes the phase response of the desired signal for a constant group delay to compensate for delay added by the Sallen and Key and switched-capacitor filters. In the first few switched-capacitor stages, the desired signal's amplitude may be relatively small, however, as the signal passes down the filter, gain is provided and the noise floor (predominantly from kT/C) can rise for a constant carrier-to-noise ratio. Therefore, capacitor scaling techniques were employed to optimize the overall filter configuration for the lowest power consumption. A comparison of total capacitance used by the filters and ADC is given in Table III. It was estimated that by scaling the capacitance, a reduction of 40% in the switched-capacitor filter's power consumption may be obtained. This technique is further described in [39].

A stand-alone filter section which included both the Sallen and Key and switched-capacitor filters was fabricated as a separate die on the same reticle as the receiver prototype. Fig. 14 shows the measured frequency response for all the baseband gain filter settings on the stand-alone chip.