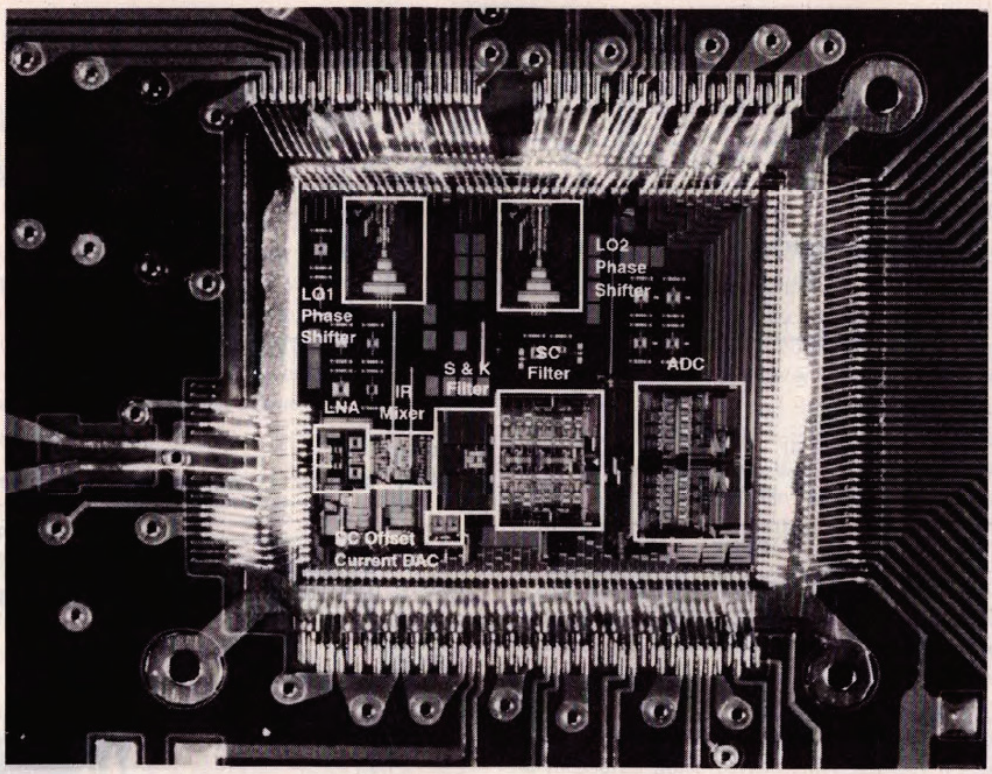
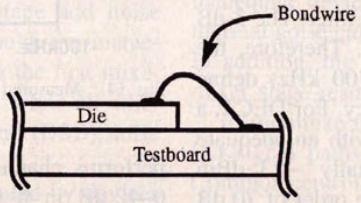


(a)



(b)

Fig. 15. Chip-on-board (COB) assembly. (a) Chip assembled with the board. (b) Sideview of a single bondwire.

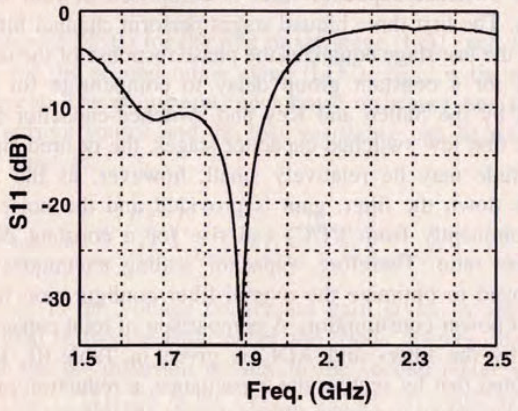


Fig. 16. Measured S11 at the receiver input.

G. Analog-to-Digital Conversion

After filtering, the signal then passes through a 10-b, 10 MS/s pipelined ADC. Similar to the switched-capacitor filter stages, the sampling and feedback capacitors utilized by the ADC were scaled to minimize the overall power consumption. This work has been previously described in [40]–[42].

V. Receiver Test Results

The prototype receiver was assembled with the testboard using a chip-on-board packaging technology. Fig. 15 shows that the backside of the die is glued directly to a gold-plated landing zone found on the testboard which provides an excellent ground plane to the chip substrate. The bondwires run from the chip pads to landing zones found directly on the testboard. This is done to reduce the effects of parasitic lead inductance that otherwise would have been associated with a packaged part. With the testboard assembled, the S11 looking into the receiver input port was measured before testing began; this is shown in Fig. 16.

To test the receiver's immunity to strong adjacent channel signals, a modified version of the two-tone test was used. First, a single tone was applied to the receiver input such that

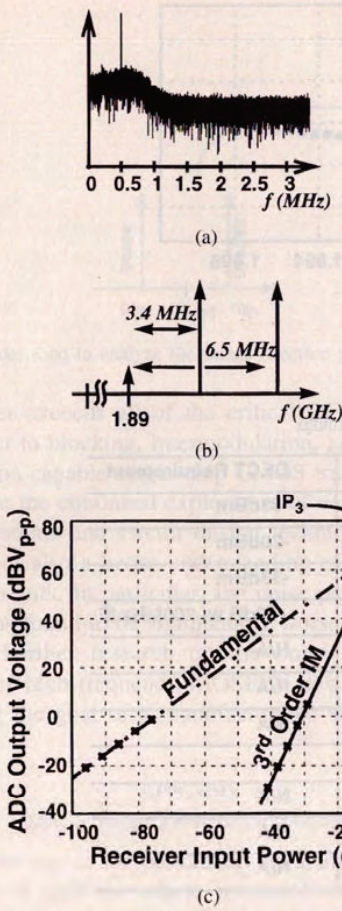


Fig. 17. Two-tone third-order intermodulation test. (a) FFT of the receiver output with a single tone input. (b) Tones applied two and four DECT channels away from the carrier. (c) Third-order IM plot showing intercept point.

when it was frequency translated to baseband, it fell within the bandwidth of the channel filter, as shown in Fig. 17(a). The power of the input signal was then varied and the linear response of the receiver was obtained. Then as outlined in the DECT specification [25], two tones were applied to the receiver two and four DECT channels away from the carrier such that when downconverted to baseband, their third-order intermodulation product fell within the pass-band of the baseband filters. The magnitude of the two input tones was varied and a third-order intermodulation intercept point of −7 dBm referred to the input of the LNA was extrapolated from Fig. 17(c)

To test the receiver's blocking performance, a −73 dBm desired signal was applied to the input in accordance with the test conditions outlined in the DECT standard. Simultaneously, a blocker was applied in the adjacent DECT channel and increased in magnitude until the CNR at the output of the receiver dropped to 10.3 dB [43], [44]. The test was repeated with a blocker in each of the DECT channels. Fig. 18 shows the magnitude of the measured blockers which resulted in a 10.3 dB CNR of the desired carrier. The shaded area in Fig. 18 represents the blocking requirements of DECT which are well below that measured on the prototype device.

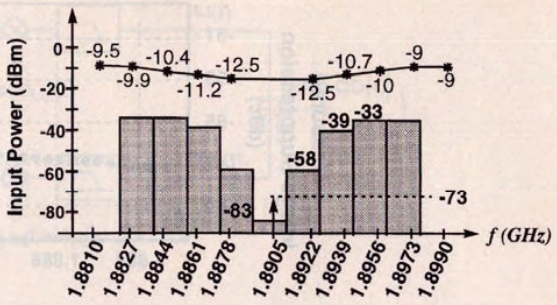


Fig. 18. Blocking performance of the DECT receiver.

TABLE IV
BREAKDOWN OF THE RECEIVER COMPONENTS CONTRIBUTING TO IMAGE REJECTION

Balun	**2dB**
LNA	**8dB**
IR Mixer	**45dB**
Total IR	**55dB**

To test the receiver's immunity to signals present within the image-band, a series of tones in the DECT band were applied to the receiver. Corresponding tones were then applied in the image band and the ratio of the receiver's response to these signals was then recorded. A relatively flat −55 dBc of image suppression was measured across the DECT band. This is shown in Fig. 19. It should be noted that the phase between the quadrature local oscillators was tuned to give maximum image suppression. However, no tuning was provided to adjust the gain between the signal paths. A breakdown of the receiver components which contribute to image rejection is shown in Table IV. The RF filter which was not a part of the test set-up can easily provide an additional 30 dB of image attenuation. Therefore, this receiver under a tuned condition could attain 85 dB of image rejection, which is well above the requirement for the DECT standard with a ~190 MHz intermediate frequency.

The receiver's reference sensitivity was measured at −90 dBm which corresponds to a noise figure of 14 dB. The overall receiver's power consumption is 198 mW. A breakdown of the rms noise voltage referenced to the output of the receiver can be found in Fig. 20(a), while the contribution of each block to the overall power consumption is shown in Fig. 20(b). From Fig. 20 it can be inferred that although the first mixer contributes almost 40% of the output noise power, it dissipates less than 9% of the overall receiver's power consumption.

Although the prototype meets the sensitivity requirement of DECT, it is insufficient for other standards with more aggressive noise figure requirements. From Fig. 20 it can be seen that the noise contribution of the first mixer stage could have been traded-off with the mixer power consumption to improve the noise performance of the overall receiver. In addition, as mentioned previously, the voltage conversion gain of the first mixer was limited to unity by the parasitic capacitance at the first mixer output with the constraint of

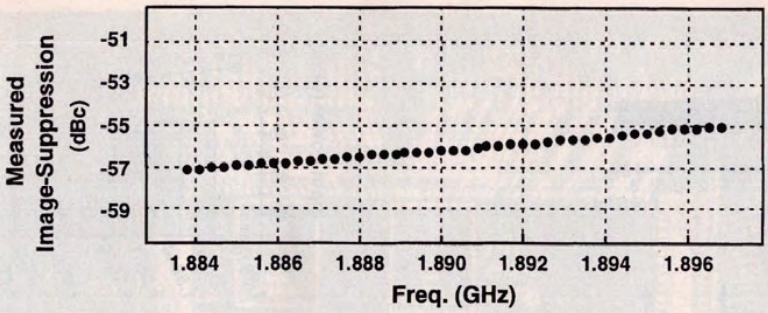


Fig. 19. Measured image suppression for the receiver.

TABLE V
RECEIVER PERFORMANCE, BOTH MEASURED AND REQUIRED

	Receiver Measurement	DECT Requirement
Sensitivity	-90dBm	-83dBm
Input IP3 (Max. gain setting)	-7dBm	-26dBm
P_{-1dB} (Min gain setting)	-24dBm	-33dBm
Receiver Image Rejection	~85dB w/ RF Filter	~70dB w/ 200MHz IF
P_{ob3dB} (Max. gain setting)	-33dBm @ 2MHz	N/A
Max. Receiver Gain	78dB	N/A
Min. Receiver Gain	26dB	N/A
Die Size	7.5mm x 6.5mm	
Active Chip Area	$15mm^2$	N/A
Power Supply	3.3v	N/A
Silicon Technology	0.6μm DPTM CMOS	N/A

the first mixer gain equal to one, the noise contribution from the second mixer stage becomes increasingly important. The IF bandwidth limitation problem can be more adequately addressed with an improved silicon technology with a finer feature size as is currently available with 0.35 and 0.25-μm CMOS processes. The receiver's linearity performance is set by the input stage of the first mixer. Because the input referred IP3 of the receiver was significantly above the requirement for DECT, the first mixer's linearity could have been traded-off to improve the RF mixer and receiver's noise performance.

A summary of other key receiver measurements can be found in Table V.

VI. CONCLUSION

A proposed receiver architecture, wide-band IF with double conversion, was presented in this paper. The relative merits of this system were discussed as they relate to the goal of a highly integrated receiver. The wide-band IF architecture holds promise with respect to integrating one of the more challenging components in a transceiver system, the frequency synthesizers. Moreover, the wide-band IF receiver removes the need for the discrete-component IF filter while the image-rejection mixer presented eliminates the need for the discrete-component noise filter after the LNA. In addition, the proposed architecture has features which potentially enable a single receiver to be used by multiple RF standards. A prototype

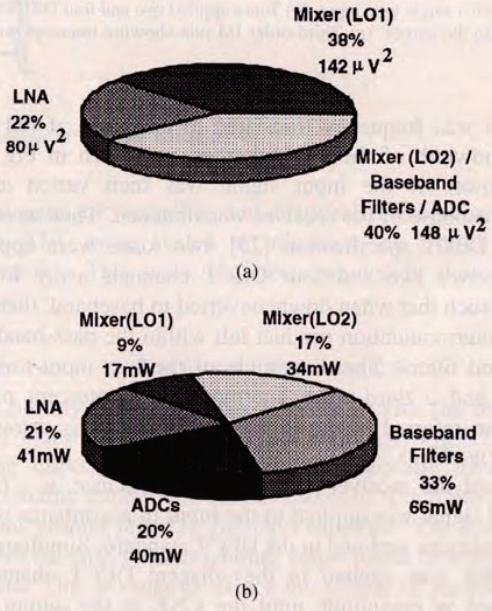


Fig. 20. (a) Breakdown of the output rms noise voltage and (b) breakdown of the receiver's power consumption.

receiver based on the wide-band IF concept was implemented in a 0.6-μm CMOS process and designed to meet the specifications of the DECT standard. Measured results indicate that

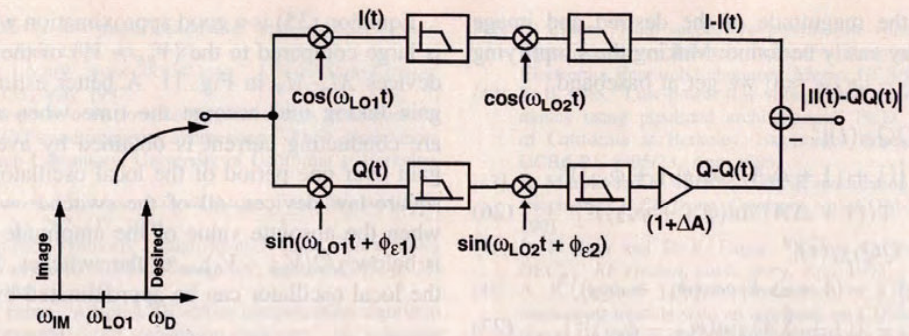


Fig. 21. Model used to analyze the image-rejection performance as a function of LO phase and gain path matching.

this receiver exceeds all of the critical DECT specifications with respect to blocking, intermodulation, and sensitivity.

Production capable single-chip CMOS transceivers will not only require the continued exploration of new transmitter and receiver systems and circuit design techniques [3], [4], [6], [8], [46], but also a better understanding of the devices used by these circuits. In particular, the noise performance of this receiver was found to be significantly worse than that initially predicted. Further research on the noise performance and modeling of high-frequency MOSFET devices is paramount to reaching the goal of a manufacturable single-chip CMOS receiver.

Appendix A
Image Rejection with Mismatch

The following is an outline of an analysis to determine the effects of gain and phase mismatch on image-rejection performance. The matching error is modeled as shown in Fig. 21. The phase mismatch between both the I and Q first and second local oscillators are defined as $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$, respectively, which defines the deviation from ideal quadrature. For example, 91° phase difference between the I and Q LO1 would be represented by $\phi_{\varepsilon 1} = 1°$. ΔA represents the composite gain mismatch between two of the four image-rejection channels.

The analysis is carried out by applying an image and deisred signal denoted $D(t)$ and $IM(t)$ both equally spaced in the frequency domain from the first local oscillator as shown in Fig. 21. Both the image and desired signal will be tracked as they move through the mixer to the baseband II and QQ channels where they are summed. A solution for the image-rejection ratio is found with the magnitude of the desired and image signals after summation of the II and QQ channels

$$D(t) = \cos(\omega_D t) + j\sin(\omega_D t) \tag{12}$$

$$IM(t) = \cos(\omega_{IM} t) + j\sin(\omega_{IM} t). \tag{13}$$

Assuming an idealized sinusoidal LO, the two input signals $D(t)$ and $IM(t)$ are multiplied by the I and Q local oscillators, the resulting signals at IF can be expressed as

$$I_D(t) = \tfrac{1}{2}\left[\cos((\omega_D - \omega_{\mathrm{LO1}})t) + \cos((\omega_D + \omega_{\mathrm{LO1}})t)\right] + \frac{j}{2}\left[\sin((\omega_D + \omega_{\mathrm{LO1}})t) + \sin((\omega_D - \omega_{\mathrm{LO1}})t)\right] \tag{14}$$

$$I_{IM}(t) = \tfrac{1}{2}\left[\cos((\omega_{IM} - \omega_{\mathrm{LO1}})t) + \cos((\omega_{IM} + \omega_{\mathrm{LO1}})t)\right] + \frac{j}{2}\left[\sin((\omega_{IM} + \omega_{\mathrm{LO1}})t) + \sin((\omega_{IM} - \omega_{\mathrm{LO1}})t)\right] \tag{15}$$

$$Q_D(t) = \tfrac{1}{2}\left[\sin((\omega_D + \omega_{LO1})t + \phi_{\varepsilon 1}) - \sin((\omega_D - \omega_{\mathrm{LO1}})t - \phi_{\varepsilon 1})\right] + \frac{j}{2}\left[\cos((\omega_D + \omega_{\mathrm{LO1}})t - \phi_{\varepsilon 1}) - \cos((\omega_D + \omega_{\mathrm{LO1}})t + \phi_{\varepsilon 1})\right] \tag{16}$$

$$Q_{IM}(t) = \tfrac{1}{2}\left[\sin((\omega_{IM} + \omega_{LO1})t + \phi_{\varepsilon 1}) - \sin((\omega_{IM} - \omega_{\mathrm{LO1}})t - \phi_{\varepsilon 1})\right] + \frac{j}{2}\left[\cos((\omega_{IM} + \omega_{\mathrm{LO1}})t - \phi_{\varepsilon 1}) - \cos((\omega_{IM} + \omega_{\mathrm{LO1}})t + \phi_{\varepsilon 1})\right]. \tag{17}$$

Assuming the upconverted terms are removed through low-pass filtering and substituting in $\omega_{\mathrm{IF}} = \omega_D - \omega_{\mathrm{LO1}} = \omega_{\mathrm{LO1}} - \omega_{IM}$ results in

$$I_D(t) = \frac{1}{2}\cos(\omega_{\mathrm{IF}} t) + \frac{j}{2}\sin(\omega_{\mathrm{IF}} t) \tag{18}$$

$$I_{IM}(t) = \frac{1}{2}\cos(\omega_{\mathrm{IF}} t) - \frac{j}{2}\sin(\omega_{\mathrm{IF}} t) \tag{19}$$

$$Q_D(t) = -\frac{1}{2}\sin(\omega_{\mathrm{IF}} t - \phi_{\varepsilon 1}) + \frac{j}{2}\cos(\omega_{\mathrm{IF}} t - \phi_{\varepsilon 1}) \tag{20}$$

$$Q_{IM}(t) = \frac{1}{2}\sin(\omega_{\mathrm{IF}} t) + \phi_{\varepsilon 1}) + \frac{j}{2}\cos(\omega_{\mathrm{IF}} t + \phi_{\varepsilon 1}). \tag{21}$$

Multiplying (18)–(21) by the second set of quadrature LO's and again removing the upconverted terms, the following expression may be obtained for image and desired signal present in the II and QQ baseband channels:

$$II_D(t) = \tfrac{1}{4}\left[\cos((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t) + j\sin((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t)\right] \tag{22}$$

$$II_{IM}(t) = \tfrac{1}{4}\left[\cos((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t) - j\sin((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t)\right] \tag{23}$$

$$QQ_D(t) = \tfrac{1}{4}(1+\Delta A)[-\cos((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t - (\phi_{\varepsilon 1} + \phi_{\varepsilon 2})) - j\sin((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t - (\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))] \tag{24}$$

$$QQ_{IM}(t) = \tfrac{1}{4}(1+\Delta A)[\cos((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t + (\phi_{\varepsilon 1} + \phi_{\varepsilon 2})) - j\sin((\omega_{\mathrm{IF}} - \omega_{\mathrm{LO2}})t + (\phi_{\varepsilon 1} - \phi_{\varepsilon 2}))]. \tag{25}$$

From (22)–(25) the magnitude of the desired and image baseband signals may easily be found. Making the simplifying assumption that $\omega_{\rm IF} - \omega_{\rm LO2} \approx 0$ we get at baseband

$$|II_D(t) - QQ_D(t)|^2 = \tfrac{1}{16}\left[(1+(1+\Delta A)\cos(\phi_{\varepsilon 1}+\phi_{\varepsilon 2}))^2 + ((1+\Delta A)\sin(\phi_{\varepsilon 1}+\phi_{\varepsilon 2}))^2\right] \quad (26)$$

$$|II_{IM}(t) - QQ_{IM}(t)|^2 = \tfrac{1}{16}\left[(1-(1+\Delta A)\cos(\phi_{\varepsilon 1}+\phi_{\varepsilon 2}))^2 + ((1+\Delta A)\sin(\phi_{\varepsilon 1}-\phi_{\varepsilon 2}))^2\right]. \quad (27)$$

By taking the ratio (26) and (27), the image-rejection ratio in (dB) is given by

$$IRR(\text{dB}) = 10 \cdot \log \cdot \left[\frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon_1}+\phi_{\varepsilon 2})}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})}\right]. \quad (28)$$

Equation (28) is identical to the result given in [20] and [45] for more conventional image-rejection mixer configurations.

Appendix B
Mixer Voltage Conversion Gain

First take the idealized model where the desired signal is represented as a cosine, $V_{\rm rf}(t)$, multiplied by an ideal squarewave local oscillator, $V_{\rm LO}(t)$, which is represented with height ± 1

$$V_{\rm rf}(t) = g_m R_L V_{\rm rf}\cos(\omega_{\rm rf} t) \quad (29)$$

$$V_{\rm LO}(t) = \left(\frac{4}{\pi}\right)\sum_{k=1}^{\infty}\left[\frac{\sin(k\pi/2)}{k}\cdot\cos(k\omega_{\rm LO}t)\right]. \quad (30)$$

In this model, take (29) and multiply by (30). This gives

$$V_o(t) = V_{\rm rf}(t)\cdot V_{\rm LO}(t) \quad (31)$$

$$V_o(t) = g_m R_L\left(\frac{4}{\pi}\right)[\cos(\omega_{\rm LO}t) - \cos(3\omega_{\rm LO}t)\cdots] \cdot V_{\rm rf}\cos(\omega_{\rm rf}t). \quad (32)$$

Ignoring the harmonics of the LO and multiplying the fundamental by the RF sinewave results in

$$V_o(t) = g_m \cdot R_L\left(\frac{4}{\pi}\right)\left(\frac{1}{2}\cos((\omega_{\rm rf}-\omega_{\rm LO})t) + \frac{1}{2}\cos((\omega_{\rm rf}+\omega_{\rm LO})t)\right). \quad (33)$$

Eliminating the upconverted term, the resulting desired signal at the mixer output is then

$$V_o(t) \approx g_m R_L\left(\frac{2}{\pi}\right)\cos((\omega_{rf}-\omega_{\rm LO})t). \quad (34)$$

Therefore, assuming a perfect squarewave LO, the voltage conversion gain through the mixer is given by the well-know expression [47], [38], [5]

$$A_v = g_m R_L\left(\frac{2}{\pi}\right). \quad (35)$$

Equation (35) is a good approximation when the LO voltage is large compared to the $(V_{gs}-V_t)$ of the switching devices, devices M_4-M_8 in Fig. 11. A better estimate of the voltage gain taking into account the time when all of the switches are conducting current is obtained by averaging the voltage gain over one period of the local oscillator. Again, assuming square-law devices, all of the switches will conduct current when the absolute value of the amplitude of the LO voltage is below $\sqrt{2}(V_{gs}-V_t)_{\rm sw}$ of the switches. Assuming now that the local oscillator can be approximated by a sinewave as

$$V_{\rm LO}(t) = V_{\rm LO}\sin(\omega_{\rm LO}t). \quad (36)$$

Defining the time that the switches move from the balanced state (all switches conducting), denoted $t_{\rm BAL}$, to the unbalanced state (only two of the four devices are conducting) may be determined by the following relationship:

$$V_{\rm LO}(t) = \sqrt{2}(V_{gs}-V_t)_{\rm sw} = V_{\rm LO}\sin(\omega_{\rm LO}t_{\rm BAL}). \quad (37)$$

Assuming $\sin(x) \approx x$ for small x, this gives

$$t_{\rm BAL} = \frac{\sqrt{2}(V_{gs}-V_t)_{\rm sw}}{V_{\rm LO}\omega_{\rm LO}}. \quad (38)$$

The gain is then averaged over one period of the LO assuming that the instantaneous gain increases linearly from zero conversion gain to the gain given (35) at time $t_{\rm BAL}$. Averaging over one period of the LO results in

$$A_v \approx g_m R_L\left(\frac{2}{\pi}\right)\left(1 - \frac{\sqrt{2}(V_{gs}-V_t)_{\rm sw}}{\pi V_{\rm LO}}\right). \quad (39)$$

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Jacques C. Rudell (S'94) was born in Grand Rapids, MI, on July 13, 1965. In 1989, he received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor. In 1991, he returned to graduate school at the University of California at Berkeley. There he completed the M.S.E.E. degree focusing on high-speed, low-power digital adaptive equalization techniques for magnetic disk drive channels employing class IV partial response. He is currently completing the Ph.D. degree in the area of integrated RF architectures and CMOS mixer implementation techniques for multistandard applications.

After receiving the B.S. degree, he spent two years as an IC Designer and Project Manager at Delco Electronics, Kokomo, IN. While at Delco, his work focused mainly on bipolar analog circuits for automotive applications.

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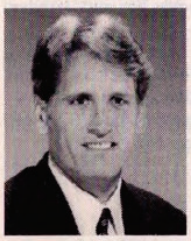
Since August 1993, he has been a Graduate Student Researcher at the University of California, Berkeley. During the summer of 1993, he worked at IBM Storage System Division where he was involved in 3-1/2" hard disk drive electronic development. During the summer of 1994, he worked at Micro Linear Corporation designing a set of IC's which are being used in undergraduate microelectronics labs at universities. During the summer of 1995, he worked at Hewlett-Packard Labs Solid State Technology Lab characterizing InP devices at 60-GHz range. He is currently working toward the Ph.D. degree in the area of analog integrated circuit design for mixed-signal and RF applications.

Mr. Chien is a member of Tau Beta Pi and Eta Kappa Nu.



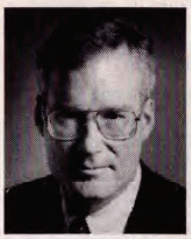
Francesco Brianti was born in Piacenza, Italy, in 1969. He graduated from the University of Pavia with a degree in electrical engineering in 1993.

In 1994, he joined SGS-Thomson working as an Analog Designer on continuous time filters and analog transversal equalizers for PRML read channels. In 1995, he was a Visiting Industrial Fellow at the University of California at Berkeley working on an integrated CMOS receiver for cordless telephone applications. He is now responsible for hard disk drivers at SGS-Thomson, San Jose, CA.



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Paul R. Gray (S'65–M'69–SM'76–F'80) was born in Jonesboro, AR, on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

In 1969 he joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, CA, where he was involved in the application of new technologies for analog integrated circuits, including power integrated circuits and data conversion circuits. In 1971 he joined the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley as a Professor. His research interests during this period have included bipolar and MOS circuit design, electro-thermal interactions in integrated circuits, device modeling, telecommunications circuits, and analog-digital interfaces in VLSI systems. He is the co-author of a widely used college textbook on analog integrated circuits. During year-long industrial leaves of absence from Berkeley, he served as Project Manager for Telecommunications Filters at Intel Corporation, Santa Clara, CA, in 1977–78, and as Director of CMOS Design Engineering at Microlinear Corporation, San Jose, CA, in 1984–85. At Berkeley he has held several administrative posts including Director of the Electronics Research Laboratory (1985–86), Vice-Chairman of the EECS Department for Computer Resources (1988–90), and Chairman of the Department of Electrical Engineering and Computer Sciences (1990–93). He is currently the Dean of the College of Engineering and is the Roy W. Carlson Professor of Engineering.

Dr. Gray has been co-recipient of best-paper awards at the International Solid State Circuits Conference, the European Solid-State Circuits Conference, and was co-recipient of the IEEE R. W. G. Baker Prize in 1980, the IEEE Morris K. Liebman award in 1983, and the IEEE Circuits and Systems Society Achievement Award in 1987. In 1994 he received the IEEE Solid-State Circuits award. He served as Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1977 through 1979 and as Program Chairman of the 1982 International Solid State Circuits Conference. He served as President of the IEEE Solid-State Circuits Council from 1988 to 1990. He is a member of the National Academy of Engineering.

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Appendix CHANG01

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Appendix CHANG02

A CMOS Channel-Select Filter for a Direct-Conversion Wireless Receiver

Paul J. Chang, Ahmadreza Rofougaran, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*— A highly selective and linear switched-capacitor channel-select filter is fabricated in 1-μm CMOS for a direct-conversion wireless receiver operating in the 902–928 MHz ISM band. The filter selects a 230-kHz wide channel and attenuates by at least 50 dB from 320 kHz to 57 MHz. The input IP3 is +30 dBm, the input-referred noise in the passband is 70 nV/$\sqrt{\text{Hz}}$, and the circuit takes 4.6 mA from a 3.3 V supply. Direct subsampling of the 915 MHz RF input signal by the filter front-end is also demonstrated with only a small degradation in linearity. The input noise voltage is halved in a redesign while keeping the current drain unchanged.**

***Index Terms*— Biquadratic filters, CMOS analog integrated circuits, elliptic filters, frequency shift keying, low-pass filters, surface acoustic wave filters, switched capacitor circuits, switched capacitor filters, UHF radio communication, UHF receiver.**

I. Introduction

RECENT research shows the feasibility of CMOS RF circuit blocks in the 1 GHz frequency range [1]–[8]. These elementary RF building blocks have recently been assembled into subcircuits such as a receiver front-end and a spread-spectrum transmitter [9]. On-chip filtering remains key to a totally integrated wireless receiver, and this is one of the first reports on a CMOS filter for a wireless receiver.

The channel-select filter must satisfy some exacting requirements. The first and most important is *selectivity*. A filter with a sharp cutoff should select the desired channel and attenuate all other adjacent users. An active implementation of the filter must itself be *low noise* so as not to degrade the overall receiver noise figure, and it must have *wide dynamic range* so that out-of-band interferers, prior to filtration, do not create intermodulation distortion which falls in the passband. Passive filters admirably meet these requirements and are therefore widely used in wireless receivers today. However, they take up precious volume on the circuit board. The receiver IC must also drive small signals at a low characteristic impedance into the filter, often at very high frequencies. The off-chip buffers required to do so dissipate additional power, and the off-chip interconnections may also pickup noise.

For at least three reasons, active filters have made little impact in superheterodyne receivers, where a *bandpass* filter with high-Q poles selects the desired channel at some intermediate frequency (IF). First, the power dissipation of an active bandpass filter rises proportionally to the center frequency and the required dynamic range [10]. Second, it is increasingly difficult because of parasitic effects to accurately realize high-Q poles at high center frequencies. Third, it is difficult to meet the specifications on distortion because the filter must handle signals and interferers which are *amplified* by the front-end. For these reasons, ceramic and surface acoustic wave (SAW) filters tuned to frequencies from 100's of kHz to 100's of MHz are used in vast numbers in production broadcast radio receivers and conventional cellular telephone handsets. In the case of the popular 10.7 MHz IF used in FM receivers, it is difficult to meet receiver specifications with even the best reported continuous-time filters [11], although bandpass delta-sigma modulators may prove a viable alternative [12].

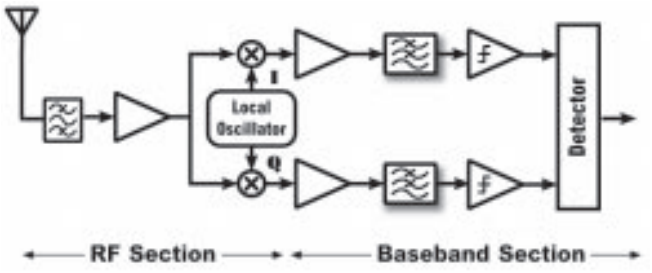


Fig. 1. Direct-conversion frequency shift keying (FSK) receiver. Low-pass channel-select filter is highlighted.

However, it has always been one of the attractions of a direct-conversion, or zero-IF, receiver that a low-pass filter with poles of a modest Q selects the desired channel, and that this filter may be integrated with the rest of the receiver [13] (Fig. 1). Some active channel-select filters have been developed for this purpose [14]–[17]. These bipolar continuous-time filters usually trade off large-signal handling against noise. Recently, attention has turned to CMOS switched-capacitor (SC) filters [18]–[21], which are better suited to handle large signals. It is now possible with the appropriate filter architecture and good circuit design to preserve the dynamic range of the receiver frontend. A CMOS continuous-time baseband filter has also been published, with a noise and dynamic range comparable to the best SC filter results [22]. This shows that aside from the additional overhead of self-tuning, the performance of a continuous-time filter is on a par with an SC implementation.

II. Filter Specifications

The SC channel-select filter described in this paper is designed for use in a frequency-hopped spread-spectrum direct-conversion receiver operating in the 902–928 MHz ISM band

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[23]. Data at 160 kb/s is transmitted by quaternary frequency shift keying (FSK) modulation, where each pair of data bits offsets the carrier frequency by one of the amounts −160, −80, +80, or +160 kHz. The modulated spectrum, therefore, lies within ±200 kHz of the carrier, which hops pseudorandomly once every four symbols across 50 slots in the 26 MHz-wide ISM band. The RF preselect filter at the front of the receiver passes the entire ISM band, and an agile local oscillator synchronized to the hopping pattern of a particular transmitter (the desired user) downconverts the ISM band to center the sought channel at dc.

The specifications of the required channel-select filter are illustrated in Fig. 2. The filter passband encompasses the spectrum of four FSK tones at ±80 and ±160 kHz, modulated in continuous-phase by pseudorandom data. The filter must suppress all the other signals populating the downconverted ISM band, particularly the adjacent user whose carrier frequency is 480 kHz above and below the desired user. The sidelobes of each quaternary tone at a baud rate of 80 kHz occupy a 6-dB signal bandwidth of ±40 kHz around the tone frequency, which means that the spectrum of the tones at 160 kHz extends to ±200 kHz. The filter passband is 230 kHz wide. System level simulations show that a passband ripple of 1 dB or so does not adversely affect the detector's ability to discriminate between the four tones. Ultimately, the correlating detector [24] sets the overall receiver noise bandwidth to 160 kHz. The stopband edge is placed at the closest tone generated by the adjacent user, 320 kHz, where the stopband loss is 50 dB. One sidelobe of this tone, however, lies in the filter transition band, and is therefore not attenuated as much. The worst case occurs at the −6 dB down frequency of the sidelobe, where the transition band loss is only 24 dB. There, the filter attenuates the adjacent user's spectrum by only 30 dB, compared to 50 dB at 320 kHz and beyond. The partial passage of the adjacent channel energy does not measurably degrade receiver sensitivity.

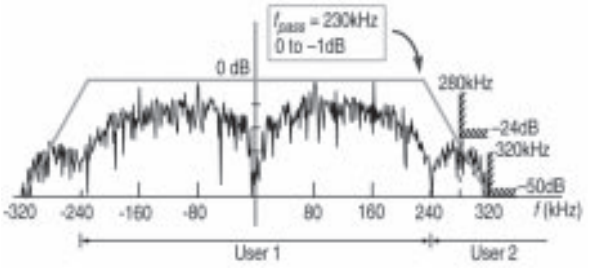


Fig. 2. Channel-select filter specification for reception of quaternary FSK. Frequency spectrum of 4-FSK modulated pseudorandom shown in passband.

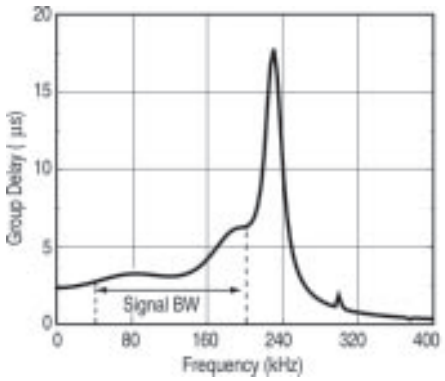


Fig. 3. Group delay variation of elliptic filter.

III. Filter Architecture

A. Main Channel-Select Filter

The channel-select filter must implement a sharp transition from 230 to 320 kHz. Since the order of the filter determines the number of opamps, a low-order realization is sought to reduce size and power consumption. A *sixth-order elliptic* filter fulfills the magnitude specification, given the sharp transition band. The group delay, however, changes somewhat across the elliptic filter's passband. This happens to be not very important for FSK detection, where the detector is sensitive only to frequency and not to phase. The group delay of the elliptic filter varies by 3 μs across the range of the signal frequency spectrum (Fig. 3), which is ±10% of the 12.5 μs symbol period. This degrades the received SNR by at most 0.5 dB. In this application, the main impairment arises at a carrier frequency hop, when the sudden change in phase upon a new frequency propagating through the wireless channel from the transmitter to receiver stimulates a time-domain transient in the receiver's channel-select filter.

The sixth-order elliptic channel-select filter is implemented with a cascade of three switched-capacitor biquadratic sections. Although the filter characteristics of a ladder are less sensitive to element-value variations, a cascade of biquads with distributed gain gives the circuit designer more flexibility to optimize dynamic range. The nonlinearity of the filter, which is covered more in detail in a later section, is measured by how well it handles overload caused by large off-channel interferers. By interspersing amplification with filtering, the desired signal progressively grows through the filter while the interferers diminish, so that at the later stages of the filter where the signal swing is largest, the interferers are substantially attenuated.

Nonlinearity defines the upper end of the dynamic range, and filter noise the lower end. The input-referred noise spectrum rises as the frequency approaches the passband edge. This phenomenon is well understood to arise from the noise contributions of the high-Q filter sections. Similarly, at low frequencies the noise spectrum rises because of flicker noise. In case the spectral density of the input-referred noise is unequal at the frequencies of the two baseband FSK tones, then the higher level of the two determines the filter dynamic range.

The three biquad sections are cascaded in an order set by their Q-factors [25]. The low-Q section appears first, to attenuate high frequency out-of-band signals and input noise, and to ease the requirements on any antialiasing filter prior to the SCF. The high-Q section follows, so the gain of the previous stage lessens the noise this section contributes to the filter input, particularly near the passband edge where the input-referred noise spectrum rises. The medium-Q section is placed last.

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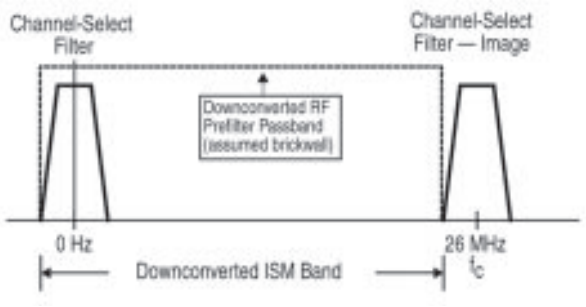


Fig. 4. Minimum clock rate for SC channel-select filter. Assumes brickwall RF preselect filter.

For convenience, the sampling frequency of the elliptic SC filter is derived by dividing down the receiver's fixed LO frequency, f_{LO}, by a power-of-two. It follows from fundamental considerations that for a fixed filter cutoff, the higher the sampling frequency, the larger the spread in filter capacitance [25]. Assume, initially, a perfect RF preselect filter with brickwall band edges that passes only the ISM band. Now, if the desired channel hops to one edge of the ISM band, the channel-select filter must attenuate all ISM users populating the 26 MHz-wide spectrum to the other edge of the band. The RF preselect filter removes all signals outside the ISM band. Therefore, a sample rate of at least 26 MHz forces all the images of the channel-select filter's transition band and passband to lie outside the ISM band, where the RF preselect filter removes all out-of-band signals (Fig. 4).

However, a practical RF preselect filter is not perfect. For instance, the transition band of a sixth-order 902–928 MHz dielectric resonator filter spans 50 MHz, and its stopband loss is only about 40 dB. Therefore, a non-ISM band interferer in the transition band of the RF preselect filter will, after only mild attenuation, fall in the image passband of the channel-select filter. It is impractical to push out the image into the preselect filter's stopband by raising the channel filter's clock rate, because the capacitor spread will then grow excessively. A multirate filter cascade works much better, where a *low-order prefilter* clocked at a high rate suppresses signals lying at the images of the higher-order channel-select filter's passband [25]. The channel-select filter subsamples, or decimates, the prefilter's output. The following section discusses the prefilter design in greater detail.

B. Prefilter

A prefilter is designed whose passband extends beyond that of the main filter, so that it does not contribute a measurable droop or ripple in the main filter passband. However, its stopband edge is placed at a considerably higher frequency, f_C–f_{STOP}, where f_C is the main (channel) filter's clock frequency, and f_{STOP} is its stopband frequency. The prefilter is clocked at some integer multiple, N, of f_C, preferably a power-of-two for convenient frequency division. Thus, the first $N-1$ images of the main filter passband lie in the prefilter's stopband, and when N is sufficiently large, the first passband image of the prefilter itself, at Nf_C, lies well in the stopband of the RF preselect filter.

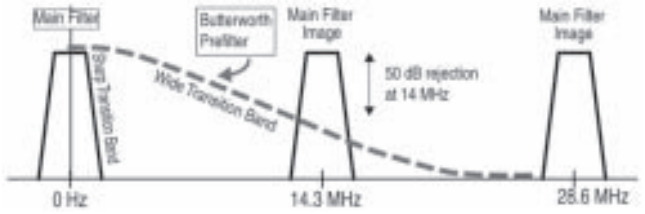


Fig. 5. Cascade of low-order prefilter and high-order main filter. Prefilter suppresses images of main filter while controlling capacitor spread and power dissipation.

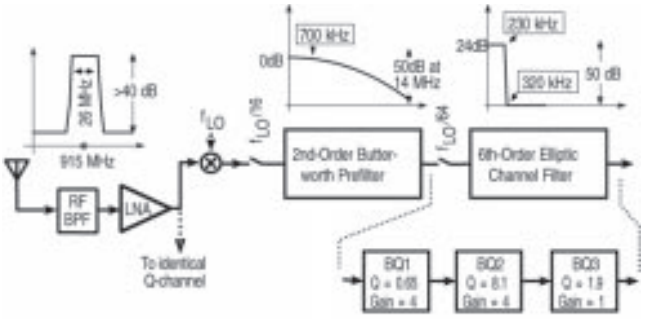


Fig. 6. Final filter, in the context of entire receiver.

Here we use $f_C = f_{\mathrm{LO}}/64 = 14.3$ MHz, and $N = 4$, so the prefilter samples its continuous-time input at 57.2 MHz. The first passband image of the prefilter at 57.2 MHz lies in the stopband of the RF preselect filter, and well beyond the output cutoff frequency at a few MHz of the conventional downconversion mixer which precedes it in the receiver. A second-order Butterworth low-pass section realizes the prefilter, with a -3-dB frequency of 700 kHz, and more than 50 dB rejection at 14.3 MHz (Fig. 5). The maximally flat passband of the Butterworth filter adds only 0.1 dB of droop within the 240 kHz-wide passband of the channel-select filter.

The final filter comprises a cascade of four biquad blocks (Fig. 6). The first block implements the second-order Butterworth prefilter, and the following three blocks make up the sixth-order elliptic channel-select filter.

IV. Circuit Design

The circuit diagram of the SC biquads used in the filter is shown in Fig. 7. Appropriate biquad architectures [25] implement the low-$Q(=0.65)$ and the high-$Q(=1.9, 8.1)$ pairs of poles in the main filter. The capacitors are fabricated as polysilicon plates over gate-oxide, with a heavily-doped N-type layer underneath. The smallest capacitor in the circuit, 215 fF, consists of two unit capacitors in antiparallel.

A. Filter as Subsampling Mixer

The received signal may be downconverted to baseband by a continuous-time mixer, or alternatively by subsampling. The well-known continuous-time mixer is implemented with a Gilbert analog multiplier or some variant. Downconversion by subsampling, on the other hand, makes use of the generalized sampling theorem, which states that no information in the

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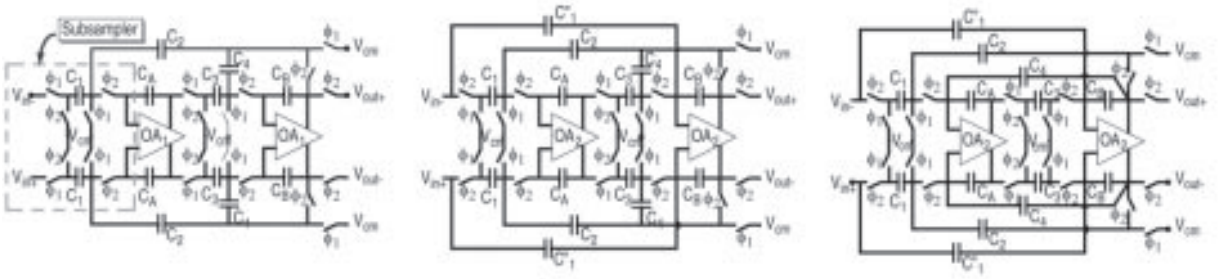


Fig. 7. SC biquads used in prefilter, low-Q section, and high-Q sections, respectively.

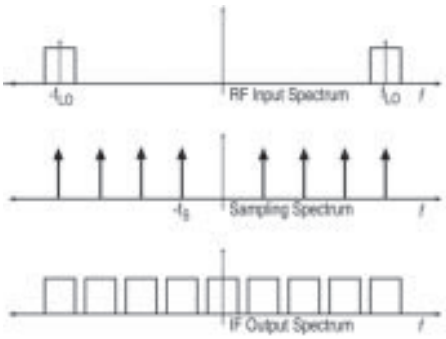


Fig. 8. Downconversion by subsampling, represented in the frequency domain.

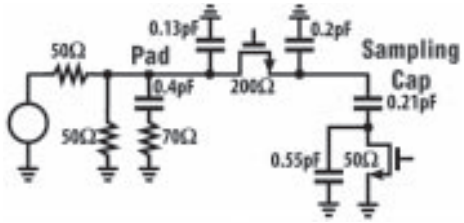


Fig. 9. Equivalent circuit of prefilter input designed to track 900 MHz RF. The various parasitic capacitors and resistors are shown.

original signal is lost if the signal is sampled at a rate greater than twice the *signal bandwidth*. The narrowband RF channel is sampled at a rate much lower than the carrier frequency, but at more than twice the channel bandwidth. When the sample rate equals the carrier frequency divided by an integer, the modulation is translated to dc (Fig. 8) [2]. A track-and-hold (T/H) consisting of MOS switches, two sampling capacitors, and a balanced differential operational amplifier is well-suited to subsampling. The time constant of the switch resistance and sampling capacitor is chosen for a wide acquisition bandwidth, but the opamp clocks at the low sample rate.

As an experiment, the input switched-capacitor and the first opamp in the Butterworth biquad were designed to downconvert the input by subsampling. A minimum-size capacitor of 215 fF samples the input, and the switch size is chosen to minimize the ON-resistance without overloading the low-noise amplifier (LNA) preceding the filter. The equivalent circuit is carefully designed to track the RF input on the sampling capacitor (Fig. 9).

We emphasize that this is not how the filter is finally used in the receiver. Downconversion by subsampling suffers from the fundamental disadvantage of a high noise figure, because in sampling a narrowband signal at RF, the mixer also acquires *wideband noise* extending from dc to RF and aliases it into the much lower Nyquist bandwidth. For white noise, this raises the noise spectral density by the subsampling factor, as has been verified in previous reports on downconversion by subsampling [2], [19]. Therefore, downconversion by subsampling is not to be recommended at the RF frontend, although it may have its uses in the IF section of a receiver, where it no longer aliases noise which has been bandpass-filtered to less than half the sample rate in preceding stages. Here we examine the feasibility of a merged mixer and filter as an object of scientific curiosity.

B. Gain Assignment

For two good reasons, both to do with lower noise, this filter must also amplify the signal. First, with amplification in the first stage of the filter cascade, later stages contribute less to the overall noise. Second, for a given feedback capacitor, gain in the first biquad requires use of a larger sampling capacitor, which therefore also contributes a lower kT/C noise.

Gain is assigned to each block in the cascade to balance signal amplification and lower noise on the one hand, and on the other hand to preserve good large signal handling. That is, with too high a gain in the blocks, the filter input noise becomes so small that it is overwhelmed by the noise of the preceding stages, but now a small input signal to the filter clips the output and compromises the overall receiver dynamic range.

Various gain assignments were considered to optimize the dynamic range of the filter, and finally a gain of $4\times$ is assigned to both the low-Q and high-Q biquad sections, to obtain a total filter gain of $16\times$, or 24 dB. The capacitors C_1 and C_1'' set the gain of the biquads in the main filter (Fig. 7). In addition to improving dynamic range, this distribution of gains flattens the input noise spectrum across the passband. The prefilter biquad on this test chip is designed to subsample a 900 MHz input unity gain, so its input capacitor is minimum size, resulting in unity gain in the biquad.

The capacitance spread, that is, the ratio of the largest to the smallest capacitors in the circuit, is approximately set by the ratio between the sampling rate and the corner frequency

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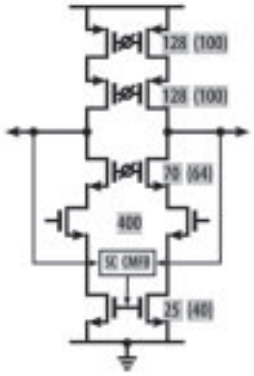


Fig. 10. Opamp circuit. FET widths in μm shown for low clock rate opamp OA 2 (widths for high clock rate opamp OA 1 in parentheses).

of the filter [25]. This predicts a spread of roughly 60 in this elliptic filter. However, larger internal capacitors lower noise, so the final spread for the entire filter is 110.

C. Transconductance Amplifier Design

The opamp determines filter linearity and power consumption. Of the eight opamps in the filter, the first two clock at 57.2 MHz and the rest at 14.3 MHz. The current drain of the two versions is 0.59 mA and 0.47 mA, respectively, and the transconductance is 4.6 mS and 3.9 mS, respectively. These are optimum for the intended operating frequency.

Due to finite dc gain in the opamp, the realized Q of the complex-conjugate poles will deviate from the designed value, leading to either ripple or droop in the filter passband. However, the detector following the filter is insensitive to the resulting slightly unequal amplitudes of the FSK tones. A simple differential single-cascode opamp with SC common-mode feedback (Fig. 10) provides adequate dc gain to satisfy this requirement. As is described below, incomplete settling at the opamp output is the larger source of error.

The opamp is designed for high-frequency operation. Generally, low-power design results in low g_m, while high-frequency operation requires high g_m. Increasing the input transistor size at a given power consumption raises g_m—doubling the transistor size raises g_m by about $\sqrt{2}$. However, the junction capacitance at the drain of the input FET also gets larger with the FET size and lowers the frequency of the second pole, eventually causing instability. Therefore, the input transistor is sized up to the point that the opamp retains a sufficient phase margin.

The output of the opamp clips at a differential voltage swing of ± 2.2 V.

V. Experimental Results

The test chip of the channel-select filter is implemented as a fully balanced circuit in a single-poly, double-metal 1-μm CMOS process and occupies an active area of 2.1×2.4 mm^2 (Fig. 11). A total of 200 pF on-chip capacitance takes up about 60% of the area. The input leads of the IC package are terminated in 50 Ω. The balanced outputs, taken off-chip through source follower buffers, are converted to single-ended in a passive power combiner. A balanced input is applied to the filter IC through an off-chip passive power splitter. The filter is tested with a baseband input, and then with an RF input which the filter downconverts by subsampling at the first stage. The results of both these tests are now presented.

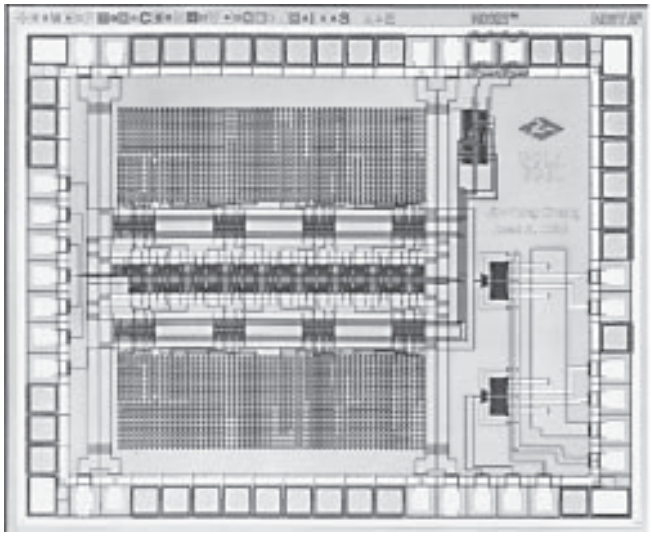


Fig. 11. Chip photograph.

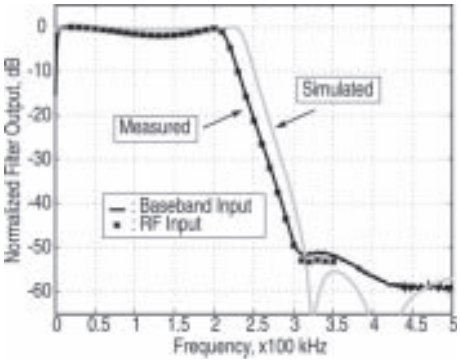


Fig. 12. Measured frequency response. Passband details with baseband and RF inputs.

A. Filter Frequency Response

The measured filter passband response corresponds very well to the expected response as shown in Fig. 12, except for an additional 1 dB droop in the passband attributed to incomplete settling in the opamps of the high-gain biquads. The corner frequency is at 215 kHz, and the stopband starts at 300 kHz. The frequency response remains unchanged when the prefilter subsamples a frequency offset from 915 MHz, accomplishing downconversion and filtering.

Fig. 13 shows the stopband of the filter measured on a large frequency scale. As expected, the Butterworth prefilter suppresses the first three images of the elliptic filter passband, in effect extending the stopband to 57 MHz. Interferers beyond this frequency lie in the stopband of the RF preselect filter, which suppresses, for instance, the passband image at 57 MHz by an additional 35 dB. The measured stopband attenuation is at least 50 dB up to 57 MHz, and limited to at most 65 dB by parasitic effects such as on-chip signal feedthrough.

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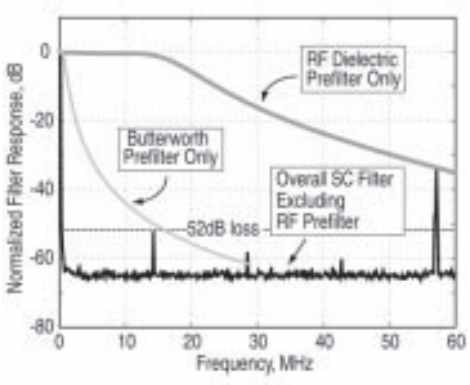


Fig. 13. Measured frequency response. Stopband measured on large frequency scale.

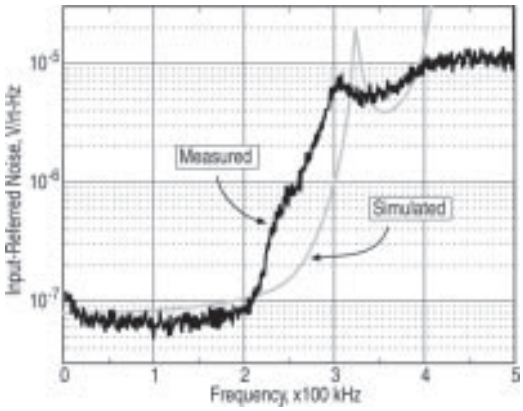


Fig. 14. Measured input-referred noise spectrum.

The overall filter response measurement shows that when used in a quadrature receiver (Fig. 1), this filter selects a 480 kHz-wide channel from a band hundreds of MHz wide, while rejecting out-of-band signals by at least 50 dB. The RF test proves that this filter can also downconvert by subsampling without any degradation in its frequency response.

B. Filter Noise and Receiver Performance

The input-referred noise plot is obtained by dividing the noise spectral density at the output by the measured frequency response of the filter (Fig. 14). A flat input-referred noise level of about 70 nV/$\sqrt{\text{Hz}}$ is obtained in the passband, as expected from the simulation, which shows that the gain distribution indeed suppresses high-frequency noise peaking in the high-Q biquad. The flicker noise corner lies below 20 kHz. The slight discrepancy between the measured and simulated noise spectra in the transition band is the same as the difference between the measured and simulated filter response. Noise is simulated on SPICE by replacing every switched capacitor, C, in the circuit with the equivalent continuous-time resistor $1/(f_cC)$, where f_c is the clock frequency. In addition, the prefilter noise level is multiplied by the decimation factor of 4× to capture the effect of noise aliasing in the main filter.

As the received signal in a direct-conversion receiver is only amplified by 20 or 30 dB in the RF front-end before it enters the baseband section, noise in the baseband circuits can easily further degrade the signal-to-noise ratio. This reflects as a lower receiver sensitivity, or, equivalently, a higher input-referred noise figure. The total filter input-referred noise of 70 nV/$\sqrt{\text{Hz}}$, or −130 dBm/Hz referenced to a hypothetical 50 Ω resistor, implies that with 30 dB of conversion gain in the RF frontend, the receiver noise figure due to the *filter noise* alone is 13.6 dB. This is not acceptable. The filter noise must be lowered. In a redesign, the input-referred noise is halved to 35 nV/$\sqrt{\text{Hz}}$ by merely redistributing the gain in the various filter blocks. As the filter in its final version is not to be used as a downconversion mixer, a larger sampling capacitor is used in the prefilter biquad, which results in a gain of 4× and suppresses the noise contributions of all the later filter blocks. Then, a gain of 2× is assigned to both the first and second biquad of the elliptic filter to suppress the noise contributions, as well as peaking in the input-referred noise spectrum at the filter band-edge. The final filter gain remains 16×, or 24 dB. This redistribution of gains does not change the total current drain of the filter.

C. Filter Nonlinearity

An active filter's ability to handle large signals with little intermodulation distortion is of special interest, as its inevitable inferiority to a passive filter in this one respect may disqualify its use in a wireless receiver. There are no standards on how to evaluate this feature of a filter. The sources of distortion which matter in a particular receiver must be identified and then characterized in a way linked to the receiver's intended performance.

Nonlinearity in a balanced baseband circuit is measured by the third-harmonic distortion, or in the case of a bandpass circuit, by the third-order intermodulation created by two in-band tones. Harmonics of a single FSK-tone at 160 kHz in this filter lie in the stopband and are further rejected in the correlating detector [24]. Therefore, harmonic distortion is unimportant in the intended use. Similarly, in the unlikely event that an extraneous interferer appears in the filter passband, the receiver will grossly malfunction because the detector cannot discriminate the interferer from the legitimate FSK tone. Therefore, intermodulation distortion between the two is inconsequential.

On the other hand, it is more likely that third-order intermodulation between certain combinations of two tones in the *stopband* produces spurious products in the passband at the frequency of one of the expected FSK tones (Fig. 15). This nonlinearity is characterized by plotting the third-order intermodulation between 320 and 480 kHz at the filter output on the same scale as its response to a single 160 kHz tone, and extrapolating the intercept point from this data. The measured input IP3 is 30 dBm (Fig. 16). This plot of third-order intermodulation is unlike an amplifier in that it includes filtering of the input tones. The two tones at 320 kHz and 480 kHz are significantly attenuated by the filter while the 160 kHz tone is not. The experiment is repeated by translating all these frequencies by 915 MHz, which the prefilter biquad downconverts to baseband. The IP3 is now lowered to 21 dBm. The measured input IP3 of a previously reported unity-gain subsampling mixer [2] is also about 22 dBm, which suggests

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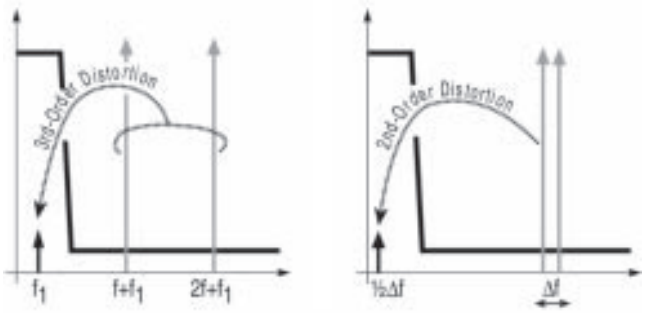


Fig. 15. Two likely sources of distortion in filter. Intermodulation between out-of-band signals (left) and AM detection of out-of-band signal (right).

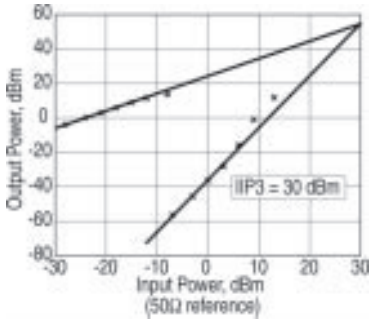


Fig. 16. Measured third-order intermodulation due to out-of-band signals, and intercept point.

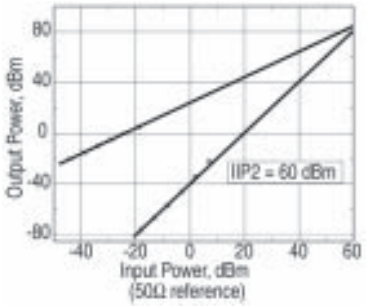


Fig. 17. Measured second-order envelope detection of out-of-band signal and intercept point.

that this may be the limit to attainable linearity in a 3.3 V subsampling front-end.

Second-order distortion in the filter frontend affects receiver performance in a different way, by detecting the time-varying envelope of an AM signal in the stopband and translating it to baseband (Fig. 15). This is shown by the following trigonometric relation, where a carrier frequency, f_0, is amplitude-modulated at index ε by the tone f_m, and only the baseband term is retained on the right-hand side

$$[(1+\varepsilon \sin \omega_m t) \sin \omega_0 t]^2 \rightarrow \varepsilon \cos \omega_m t.$$

If f_m lies at one of the expected FSK tones, it triggers a spurious response in the detector. The second-order AM detection is measured with a 1 MHz carrier amplitude-modulated by 50 kHz at a 100% index applied to the filter input. The input IP2 is about 60 dBm (Fig. 17). This shows a very small second-order nonlinearity, chiefly due to the strong rejection of second harmonic by a balanced circuit.

The filter's input intercept point due to both the third-order intermodulation and the second-order AM detection is higher than the 28 dBm output intercept point of a previously published RF front-end [26], which means that when the two are cascaded in a receiver, the filter will preserve the dynamic range of the front-end. The high linearity of the active filter results from careful gain distribution among the various stages.

D. Current Drain

The circuit operates at a 3.3 V power supply. The filter drains 4.6 mA of current as expected from the simulation, which corresponds on average to 0.58 mA/pole, including the two prefilter poles. The clock divider logic drains another 1.3 mA. The filter current is lower than the extrapolated current drain of previously published continuous-time bipolar channel-select filters when they are scaled to the same noise level. For instance, a 7.5 kHz sixth-order elliptic low-pass filter for a paging receiver [14] will dissipate 8 mA after scaling, while a 172 kHz third-order Butterworth filter will require 30 mA [16]. Neither filter's stopband has been evaluated to 57 MHz, nor are they capable of handling large signals as well as this CMOS circuit. A BiCMOS RF frontend switched capacitor filter using biquads [19] dissipates a total power of 112 mW from a 3.3 V supply including the clock generator, and offers a minimum stopband attenuation of 38 dB with input IP3 of -23 dBm.

A more germane comparison is with the aforementioned 600 kHz 0.6-μm CMOS continuous-time channel-select low-pass filter [22]. That filter operates at 3 V, its IP3 of 34 dBm is comparable to ours, its input-referred noise is 42 nV/$\sqrt{\text{Hz}}$ slightly higher than 35 nV/$\sqrt{\text{Hz}}$ in our redesign, and it drains 0.5 mA/pole, whereas our redesigned filter, which includes a prefilter with two poles of its own, drains 0.58 mA/pole. It is noteworthy that for this building block, two different design approaches lead to a remarkably similar total performance.

E. DC Offset

The nonautozeroed integrators in the filter contribute dc offset, which is amplified and may saturate the subsequent limiting amplifier. The measured output offset ranges from 80–200 mV. Owing to a dc biasing feedback in the limiting amplifier which is decoupled by an off-chip capacitor, an input offset of ± 100 mV may be absorbed with little loss of dynamic range [5]. A higher offset will require on-chip ac coupling of the signal. Therefore, filter offset is not a limiting factor in this receiver.

VI. Conclusion and Discussion

The portable wireless transceiver of the future requires a high level of integration and low-power dissipation. The filter block, however, has traditionally not been amenable to integration.

This work successfully demonstrates a highly selective and highly linear channel-select filter using a switched-capacitor circuit in 1-μm CMOS technology. In concert with standard

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RF preselection, this filter is capable of selecting a 480 kHz-wide baseband channel out of a bandwidth of over hundreds of MHz. Its low noise and exceptional linearity make it a suitable choice for this application. A zero-IF receiver makes it easier to attain these very useful attributes in the active filter.

As an exercise to enable comparison with filters for well-known wireless standards, this filter has been modified in simulation to satisfy the GSM channel-selection specifications in a direct-conversion receiver, such as the one from Alcatel [27]. The key requirements are for a 300 kHz-wide passband whose gain varies by less than 1 dB and group delay by less than 1 μs, a transition band of 250 kHz, and a stopband rejection of 35 dB. Although a fifth-order Butterworth filter satisfies all requirements, a sixth-order filter is designed here to avail the existing design tools. With a passband gain of 24 dB, the input-referred filter noise spectral density is 20 nV/$\sqrt{\text{Hz}}$, and there are no high-Q stages to raise this noise near the passband edge. Extrapolating now to a fifth-order implementation preceded by a second-order prefilter, this GSM channel-select filter will drain only 4.1 mA. Assuming a 34 dB conversion gain in the front-end, it also meets the GSM specifications on receiver noise figure and IIP3.

This filter is the final linear block in the receive chain to realize a single-chip 900 MHz direct-conversion wireless receiver in 1-μm CMOS.

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Asad A. Abidi (S'75–M'80–SM'95–F'96), for a photograph and biography, see p. 311 of the March 1997 issue of this JOURNAL.

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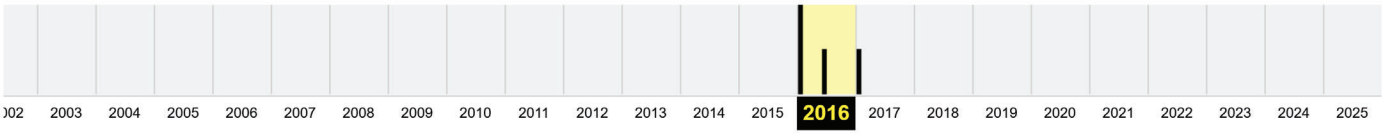
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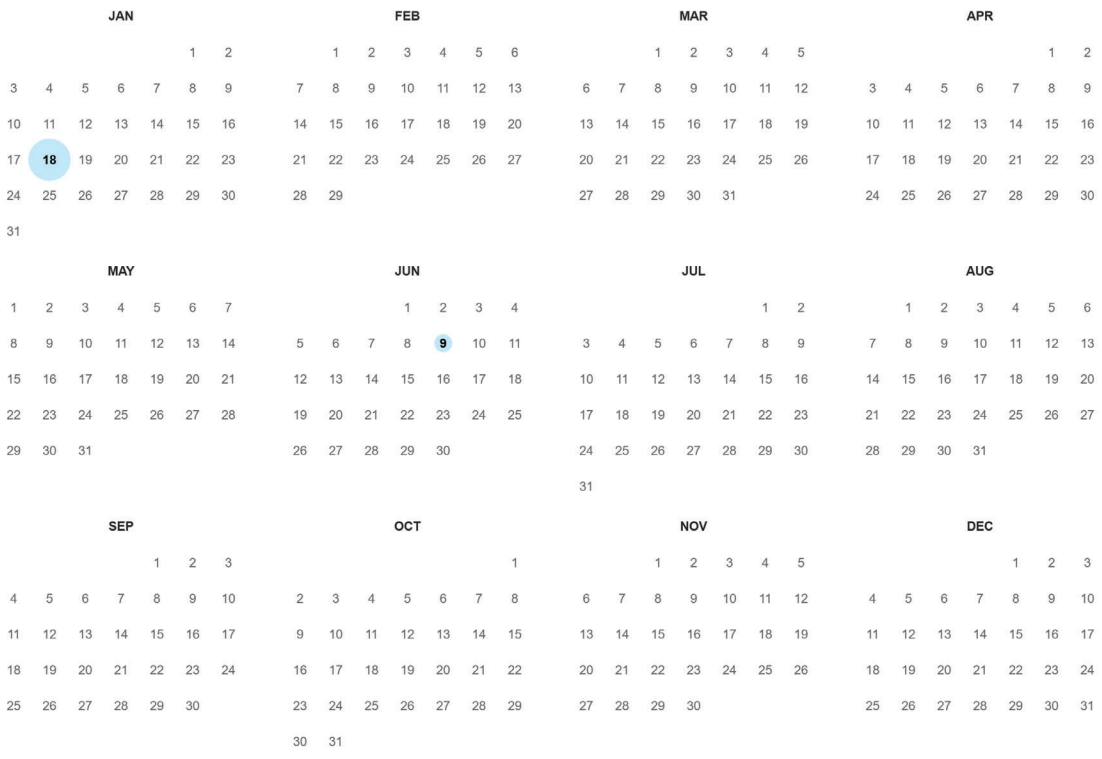
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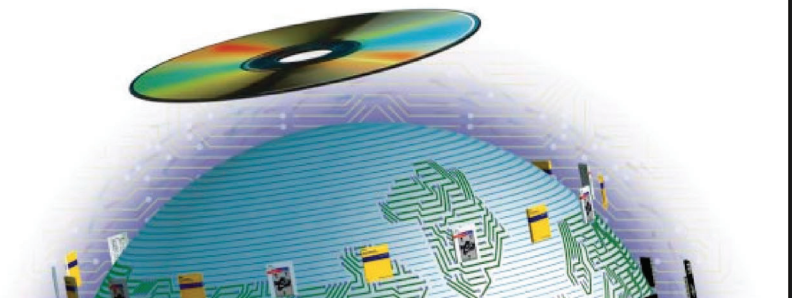
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TEXAS INSTRUMENTS

WORLD LEADER IN LOGIC PRODUCTS

Logic Selection Guide

August 1998



TEXAS INSTRUMENTS

WORLD LEADER IN LOGIC PRODUCTS

Logic Selection Guide

August 1998



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LOGIC SELECTION GUIDE

AUGUST 1998

TEXAS INSTRUMENTS

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http://www.ti.com/sc/logic

TI DATA SHEETS
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Texas Instruments (TI™) offers a full spectrum of logic functions and technologies from the mature to the advanced, including bipolar, BiCMOS, and CMOS. TI's process technologies offer the logic performance and features required for the most modern logic designs, while maintaining support for more traditional logic products. TI's offerings include products in the following process technologies:

- AC, ACT, AHC, AHCT, ALVC, HC, HCT, LV, LVC
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- BTA, CBT, CBTLV, FB, FIFO, GTL, JTAG
- ALS, AS, F, LS, S, TTL

TI offers specialized, advanced logic products that improve overall system performance and address design issues, including testability, low skew requirements, bus-termination memory drivers, and low-impedance drivers.

TI offers a wide variety of packaging options, including advanced surface-mount packaging, such as the plastic thin quad flatpack (TQFP), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP). These packages deliver high performance and allow the designer to double input/output density in the same circuit board area or to reduce the board area by one-half, compared to standard packaging technology.

For further information on TI logic families, refer to the list of current TI logic technical documentation provided in this preface. For an overview of TI logic, see Section 1. Sections 2, 3, and 4 are a functional index, functional cross-reference, and device selection guide, respectively. These sections list the functions offered, package availability, and applicable literature numbers for each device. The literature number shown is for the current data sheet (as of publication date). Copies of data sheets can be ordered through your local sales office or TI authorized distributor, or downloaded from the internet at http://www.ti.com. Please see the back cover of this selection guide for additional information.

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CURRENT TI LOGIC TECHNICAL DOCUMENTATION

Listed below is the current collection of TI logic technical documentation. These documents can be ordered through a TI representative or authorized distributor by referencing the appropriate literature number.

Document	Literature Number
ABT Logic Advanced BiCMOS Technology Data Book (1997)	SCBD002C
AC/ACT CMOS Logic Data Book (1997)	SCAD001D
Advanced Bus-Interface SPICE I/O Models Data Book (1995)	SCBD004A
AHC/AHCT Logic Advanced High-Speed CMOS Data Book (1997)	SCLD003A
AHC/AHCT Designer's Guide (1998)	SCLA013
ALS/AS Logic Data Book (1995)	SDAD001C
ALVC Advanced Low-Voltage CMOS Data Book (1998)	SCED006
BCT BiCMOS Bus-Interface Logic Data Book (1994)	SCBD001B†
Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book (1997)	SCTD002A
IEEE Std 1149.1 (JTAG) Testability Primer (1997)	SSYA002C
CBT (5-V) and CBTLV (3.3-V) Bus Switches Data Book (1998)	SCDD001B
Design Considerations for Logic Products Application Book (1997)	SDYA002
F Logic Data Book (1994)	SDFD001B†
GTL, BTL, and ETL Logic Data Book (1997)	SCED004
HC/HCT Logic High-Speed CMOS Data Book (1997)	SCLD001D
LVC and LV Low-Voltage CMOS Logic Data Book (1998)	SCBD152A
LVT Logic Low-Voltage Technology Data Book (1998)	SCBD154
Semiconductor Group Package Outlines Reference Guide (1998)	SSYU001D

CD-ROM	Literature Number
Logic Selection Guide and Data Book (September 1997)	SCBC001A‡

† See www.ti.com/sc/docs/psheets/pids2.htm for current data sheets.
‡ See www.ti.com/sc/docs/asl/cdrom.htm for online update.

Example:



1 Standard Prefix

Example: SNJ – Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 – Military
74 – Commercial

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/
Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALB – Advanced Low-Voltage BiCMOS
ALS – Advanced Low-Power Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
AS – Advanced Schottky Logic
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CBTLV – Low-Voltage Crossbar Technology
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transceiver Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage CMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Logic
SSTL – Stub Series-Terminated Logic

4 Special Features

Examples: Blank = No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G – Single Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

7 Function

Examples: 244 – Noninverting Buffer/Driver
374 – D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A–Z

9 Packages

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBQ – Quarter-Size Outline Package (QSOP)
DBV, DCK – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier (LCCC)
FN – Plastic Leaded Chip Carrier (PLCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
PAG, PAH, PCA, PCB, PM, PN, PZ –
Thin Quad Flat Package (TQFP)
PH, PQ, RC – Quad Flat Package (QFP)
W, WA, WD – Ceramic Flat Package (CFP)

10 Tape and Reel

All new or changed devices in the DB and PW package types include the R designation for reeled product. Existing products designated as LE presently maintain that designation, but will be converted to R in the future.

Nomenclature Examples:
For an Existing Device – SN74LVTxxxDBLE
For a New or Changed Device – SN74LVTxxxADBR

LE – Left Embossed (valid for DB and PW packages only)
R – Standard (valid for all surface-mount packages except existing DB and PW devices)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

LOGIC SYMBOLIZATION GUIDELINES

The logic symbolization guidelines are intended to minimize confusion concerning package symbolization on logic devices. Table 1 provides the user with a name rule and useful TI package designator information. Table 2 uses the name rule from Table 1 and applies it across all logic families.

Example: Suppose you have a 48-pin TVSOP with the symbolization VH***. Locate the 48-pin TVSOP (DGV) package in Table 1 and read across to the third column. Note that this package utilizes name rule C. Proceed to Table 2 and search down the *Name Rule C* column for VH***. The most-complete device number, SN74ALVCH16***, is located in the *Name Rule A* column.

Table 1. Name Rule Decision Tree

PACKAGE	NO. OF PINS	NAME RULE	PACKAGE DESIGNATOR
PDIP	8	A	P
	14, 16, 20	A	N
	24, 28	A	NP, NT
PLCC	28	A	FN
	44	B	FN
QSOP	16, 20, 24	B	DBQ
SOIC	1, 14, 16	B	D
	16, 20, 24, 28	B	DW
QFP	52	B	RC
	80	A	PH
	100, 132	A	PQ
SSOP	14, 16, 20, 24, 28, 30, 38	C	DB
	28, 48, 56	B	DL
TSSOP	8, 14, 16, 20, 24, 28	C	PW
	48, 56, 64	B	DGG
TVSOP	14, 16, 20, 24, 48, 56	C	DGV
	80, 100	B	DBB
TQFP	52	B	PAH
	64	B	PAG, PM
	80	B	PN
	100	B	PZ, PCA
	120	B	PCB

Table 2. Typical Logic Package Symbolization Guidelines

NAME RULE A	NAME RULE B	NAME RULE C
74AC***	AC***	AC***
74AC11***	AC11***	AE***
74ACT***	ACT***	AD***
74ACT1***	ACT1***	AU***
74ACT11***	ACT11***	AT***
SN64BCT***	DCT***	DT***
SN64BCT2***	DCT2***	DA***
SN64BCT25***	DCT25***	DC***
SN64BCT29***	DCT29***	DD***
SN74ABT***	ABT***	AB***
SN74ABT16***	ABT16***	AH***
SN74ABT162***	ABT162***	AH2***
SN74ABT18***	ABT18***	AJ***
SN74ABT2***	ABT2***	AA***
SN74ABT5***	ABT5***	AF***
SN74ABT8***	ABT8***	AG***
SN74ABTE16***	ABTE16***	AN***
SN74ABTH***	ABTH***	AK***
SN74ABTH16***	ABTH16***	AM***
SN74ABTH162***	ABTH162***	AM2***
SN74ABTH18***	ABTH18***	AL***
SN74ABTR2***	ABTR2***	AR***
SN74ACT8***	ACT8***	
SN74AHC***	AHC***	HA***
SN74AHC16***	AHC16***	HE***
SN74AHC16H***	AHCH16***	HH***
SN74AHCT***	AHCT***	HB***
SN74AHCT16***	AHCT16***	HF***
SN74AHCTH16***	AHCTH16***	HG***
SN74AHCU***	AHCU***	HD***
SN74ALB16***	ALB16***	AV***
SN74ALS***	ALS***	G***
SN74ALVC***	ALVC***	VA***
SN74ALVCH***	ALVCH***	VB***
SN74ALVCH16***	ALVCH16***	VH***
SN74ALVCH162***	ALVCH162***	VH2***
SN74ALVCHR16***	ALVCHR16***	VR***
SN74ALVCHR162***	ALVCHR162***	VR2***
SN74AS***	AS***	AS***
SN74BCT***	BCT***	BT***
SN74BCT11***	BCT11***	BB***
SN74BCT2***	BCT2***	BA***
SN74BCT25***	BCT25***	BC***

NAME RULE A	NAME RULE B	NAME RULE C
SN74BCT29***	BCT29***	BD***
SN74BCT8***	BCT8***	BG***
SN74CBT***	CBT***	CT***
SN74CBT16***	CBT16***	CY***
SN74CBT3***	CBT3***	CU***
SN74CBT6***	CBT6***	CV***
SN74CBTD***	CBTD***	CD***
SN74CBTD16***	CBTD16***	CYD***
SN74CBTD3***	CBTD3***	CC***
SN74CBTLV16***	CBTLV16***	CN***
SN74CBTLV3***	CBTLV3***	CL***
SN74CBTS***	CBTS***	CS***
SN74CBTS16***	CBTS16***	CYS***
SN74CBTS3***	CBTS3***	CR***
SN74F***	F***	F***
SN74H***	H***	H***
SN74HC***	HC***	HC***
SN74HCT***	HCT***	HT***
SN74HCU***	HCU***	(U)***
SN74HCU***	HCU***	HU***
SN74LS***	LS***	LS***
SN74LV***	LV***	LV***
SN74LVC***	LVC***	LC***
SN74LVC16***	LVC16***	LD***
SN74LVC2***	LVC2***	LE***
SN74LVC4***	LVC4***	LJ***
SN74LVCC3***	LVCC3***	LH***
SN74LVCC4***	LVCC4***	LG***
SN74LVCH***	LVCH***	LCH***
SN74LVCH16***	LVCH16***	LDH***
SN74LVCH162***	LVCH162***	LN2***
SN74LVCHR162***	LVCHR162***	LR2***
SN74LVCR2***	LVCR2***	LER***
SN74LVCU***	LVCU***	LCU***
SN74LVT***	LVT***	LX***
SN74LVT18***	LVT18***	
SN74LVTH***	LVTH***	LXH***
SN74LVTH16***	LVTH16***	LL***
SN74LVTH162***	LVTH162***	LL2***
SN74LVTH2***	LVTH2***	LK***
SN74LVU***	LVU***	LU***
SN74S***	S***	S***

5-Pin Single-Gate Packages (SOT-5)

Due to their small size, Microgate logic (DBV) and PicoGate Logic packages require more complex symbolization rules than other surface-mount packages.

Table 3 lists the four-character name rule for TI's Microgate logic offerings. The first character denotes the AHC sub-family, AHC1G, AHCT1G, AHCU1G, or the CBT family. The second and third characters denote device function, and the fourth character denotes a wafer fab/assembly site code for internal tracking (designated here by x).

Example: A Microgate logic device with package code A00x is an SN74AHC1G00DBV.

PicoGate Logic utilizes a three-character name rule. The first character denotes device technology, the second character denotes device function, and the third character denotes a wafer fab/assembly site code for internal tracking (designated here by x) (see Table 4).

Example: A PicoGate Logic device with package code HAx is an SN74HC1G00DCK.

Table 3. Microgate Logic (DBV) Package Symbolization Codes

DEVICE NAME	CODE
SN74AHC1G**	A**x
SN74AHCT1G**	B**x
SN74AHCU1G**	U**x
SN74CBT1G**	S**x

** Denotes the two-number function of the device (00, 04, 10, etc.). The 125 function is shown as 25.

Table 4. PicoGate Logic (DCK) Package Symbolization Codes

TECHNOLOGY	CODE
AHC	A
AHCT	B
ALV	E
ALVC	G
ALVCH	J
CBT	S
LVC	L

FUNCTION	CODE
00	A
02	B
04	C
U04	D
08	E
14	F
32	G
75	K
79	R
86	H
125	M
126	N
4066	L

x

Package Breakout by Levels

LEVEL 1	
PACKAGE	NO. OF PINS
D	8, 14, 16
DB	14, 16, 20, 24
DBQ	16, 20, 24
DBV	5
DGV	14, 16
DL	28, 48, 56
DW	16, 20, 24, 28
FN	20, 28
N	14, 16, 20
NS	14, 16, 20, 24
NT	24, 28
PW	8, 14, 16

LEVEL 2	
PACKAGE	NO. OF PINS
DBB	80, 100
DGG	64
DGV	20, 24, 48, 56
FN	44, 68, 84
PAG	64
PAH	52
PCA	100
PCB	120
PN	80
PW	20, 24
PZ	100
RC	52

LEVEL 3	
PACKAGE	NO. OF PINS
DGG	48, 56
PH	80
PPM	208
PQ	132

LEVEL 4	
PACKAGE	NO. OF PINS
PM	64

Level 1: Not moisture sensitive, dry pack not required
Levels 2–4: Moisture sensitive, dry pack required

Moisture-Sensitivity Levels (Per QSS 009-138, Rev D)

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS	
	CONDITIONS	TIME (hours)	CONDITIONS	TIME (hours)
1	≤ 30°C/90% RH	Unlimited	85°C/85% RH	168
2	≤ 30°C/60% RH	1 year	85°C/60% RH	168
				X + Y = Z†
3	≤ 30°C/60% RH	168	30°C/60% RH	24 + 168 = 192
4	≤ 30°C/60% RH	72	30°C/60% RH	24 + 72 = 96
5	≤ 30°C/60% RH	24	30°C/60% RH	24 + 24 = 48
6	≤ 30°C/60% RH	6	30°C/60% RH	0 + 6 = 6

RH = Relative humidity
† X + Y = Z, where:
X = Default value of time between bake and bag. If the actual time exceeds this value, use the actual time and adjust the soak time (Z). For levels 3–6, X may be standardized at 24 hours so long as the actual time does not exceed this value.
Y = Floor life of package after it is removed from dry-pack bag
Z = Total soak time for the evaluation

For more information, see:

Packaging Material Standards for Moisture-Sensitive Items, EIA Std EIA-583

Symbol and Labels for Moisture-Sensitive Devices, EIA/JEDEC Publication EIA/JEP113-A

Guidelines for the Packaging, Handling, and Repacking of Moisture-Sensitive Components, EIA/JEDEC Publication EIA/JEP124

PACKAGING CROSS-REFERENCE

	NO. OF PINS	BODY WIDTH (in./mm)	LEAD PITCH (in./mm)	PACKAGE				
				TI	PHILIPS	FAIRCHILD	TOSHIBA	MOTOROLA
PDIP	14, 16, 18, 20	0.31/7.87	0.1/2.54	N	N	N	P	P, N
	24	0.31/7.87	0.1/2.54	NT	N		P	N
QSOP	16, 20, 24	0.157/3.99	0.025/0.64	DBQ		MQA		
SOIC	8, 14, 16	0.157/4	0.05/1.27	D	D	M/S	FN	D
	16, 20, 24	0.299/7.59	0.05/1.27	DW	D	WM	FW	DW
SSOP	14, 16, 20, 24	0.22/5.6	0.025/0.65	DB	DB	MSA	FS	SD
	48, 56	0.299/7.59	0.025/0.635	DL	DL	MEA		
TSSOP	8, 14, 16, 20, 24	0.177/4.5	0.025/0.65	PW	PW	MTC	FT	DT
	48, 56, 64	0.251/6.4	0.019/0.5	DGG	DGG	MTD		
TVSOP	14, 16, 20, 24, 48, 56	0.177/4.5	0.016/0.4	DGV				
	80	0.33/8.4	0.016/0.4	DBB				
Single gate	5	1.8 mm	0.95 mm	DBV			F	
Tape and reel				LE/R		X		R2

TI Packages

D, DW – Small-Outline Integrated Circuit (SOIC)

DB, DL – Shrink Small-Outline Package (SSOP)

DBB, DGV – Thin Very Small-Outline Package (TVSOP)

DBQ – Quarter-Size Outline Package (QSOP)

DBV, DCK – Small-Outline Transistor Package (SOT)

DGG, PW – Thin Shrink Small-Outline Package (TSSOP)

FK – Leadless Ceramic Chip Carrier (LCCC)

FN – Plastic Leaded Chip Carrier (PLCC)

GB – Ceramic Pin Grid Array (CPGA)

HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)

J, JT – Ceramic Dual-In-Line Package (CDIP)

N, NP, NT – Plastic Dual-In-Line Package (PDIP)

PAG, PAH, PCA, PCB, PM, PN, PZ – Thin Quad Flat Package (TQFP)

PH, PQ, RC – Quad Flat Package (QFP)

W, WA, WD – Ceramic Flat Package (CFP)

SLL Devices

Tube Quantities

	PIN COUNT										
	8	**14**	**16**	**20**	**24**	**28**	**40**	**44**	**48**	**56**	**68**
DIP	50	25	25	20	15	13	9	N/A	N/A	N/A	N/A
SOIC	75	50	40	25	25	20	N/A	N/A	N/A	N/A	N/A
PLCC	N/A	N/A	N/A	46	N/A	37	N/A	26	N/A	N/A	18
SSOP	N/A	N/A	NS	N/A	N/A	40	N/A	N/A	25	20	N/A

NOTE: QSOP (DBQ) and EIAJ devices (DB, PW, and NS packages) are not available in tubes.

Reel Quantities

		PACKAGE DESIGNATOR	UNITS PER REEL
SOIC	14/16 pin	DR	2500
	Widebody 16 pin	DWR	2000
	20/24 pin	DWR	2000
	28 pin	DWR	1000
PLCC	28 pin	FNR	750
	44 pin	FNR	500
QSOP	16/20/24 pin	DBQR	2500
SSOP	48/56 pin	DLR	1000
EIAJ surface mount		DBR/DBLE, NSR/NSLE, PWR/PWLE	2000
TSSOP		DGGR	2000
TQFP	64 pin	PMR	1000

Box Quantities

		PACKAGE DESIGNATOR	UNITS PER BOX
DIP		N	1000
		NT	750
		NP	700
SOIC		D, DW	1000
SSOP	48/56 pin	DL	1000

Tray Quantities

		PACKAGE DESIGNATOR	UNITS PER TRAY
TQFP	64 pin	PM	160

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LOGIC OVERVIEW

SECTION 1
LOGIC OVERVIEW

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TEXAS INSTRUMENTS

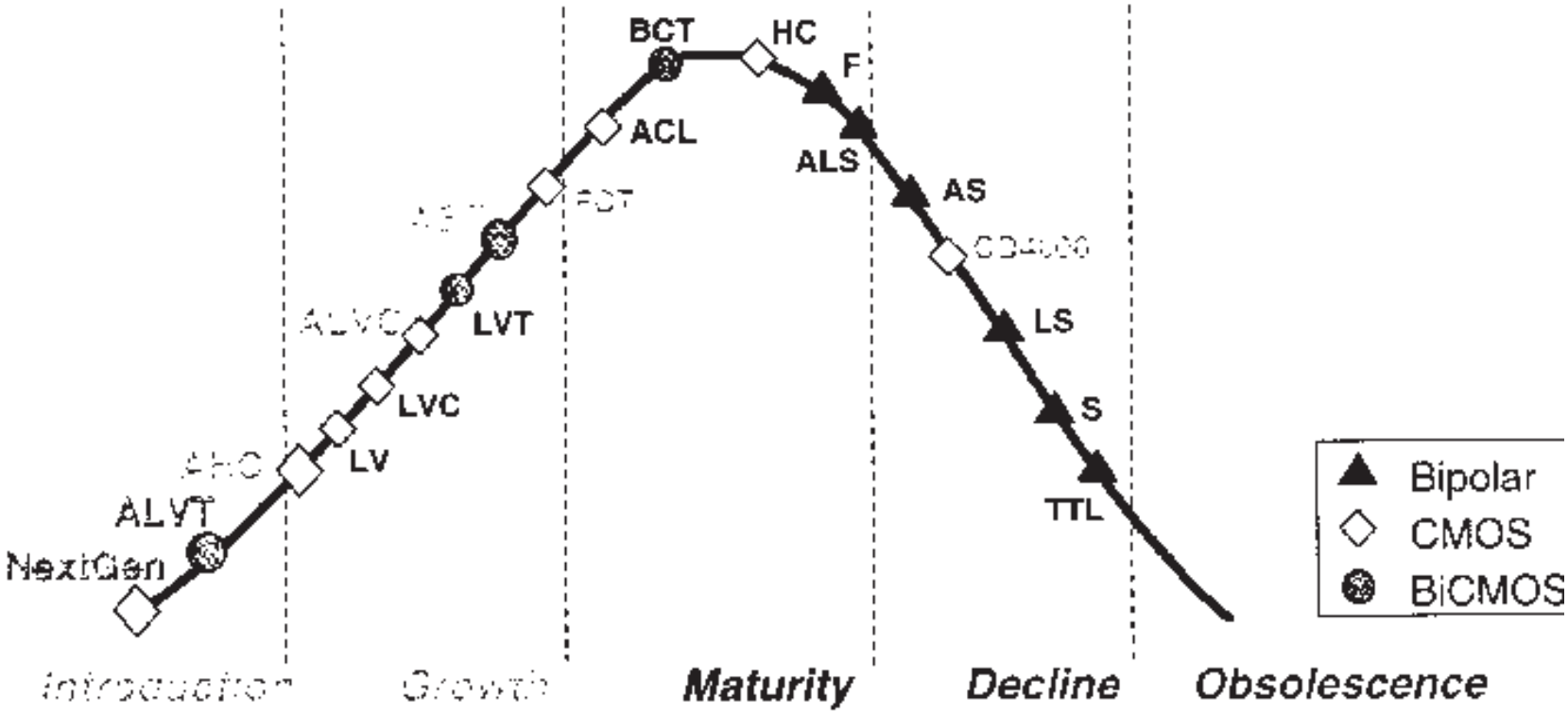
1998 Logic Priorities

- AHC/AHCT Conversion From HCMOS
- Continue Success of ABT Over FCT
- Continue Low-Voltage-Logic Dominance

One-Stop Logic Shop!

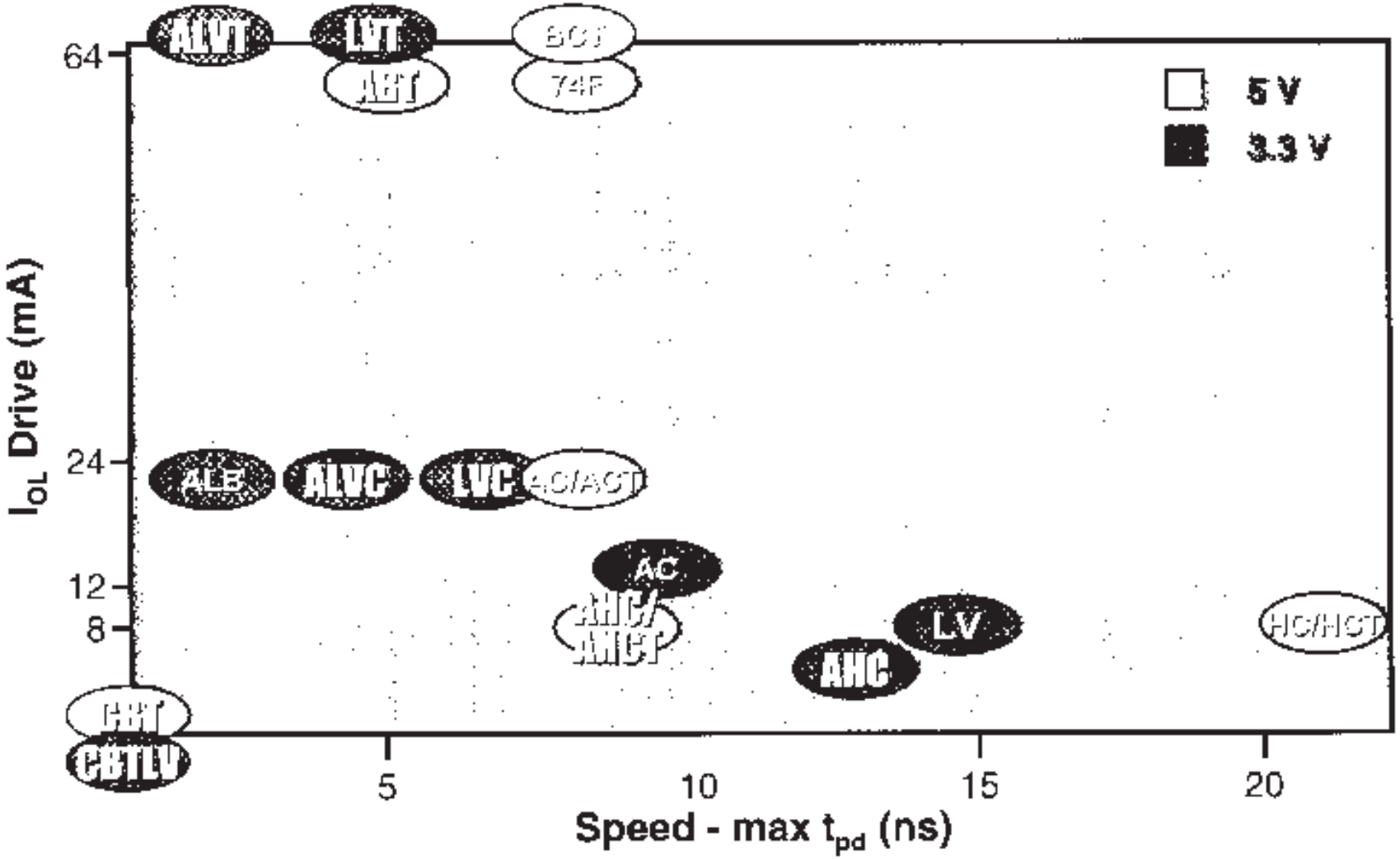
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Product Life Cycle



- TI remains committed to be the last supplier in the older families.
- Investment levels for new products are at an all time high while end equipment requirements are accelerating new product introduction.

Family Performance Positioning



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HCMOS Market Analysis

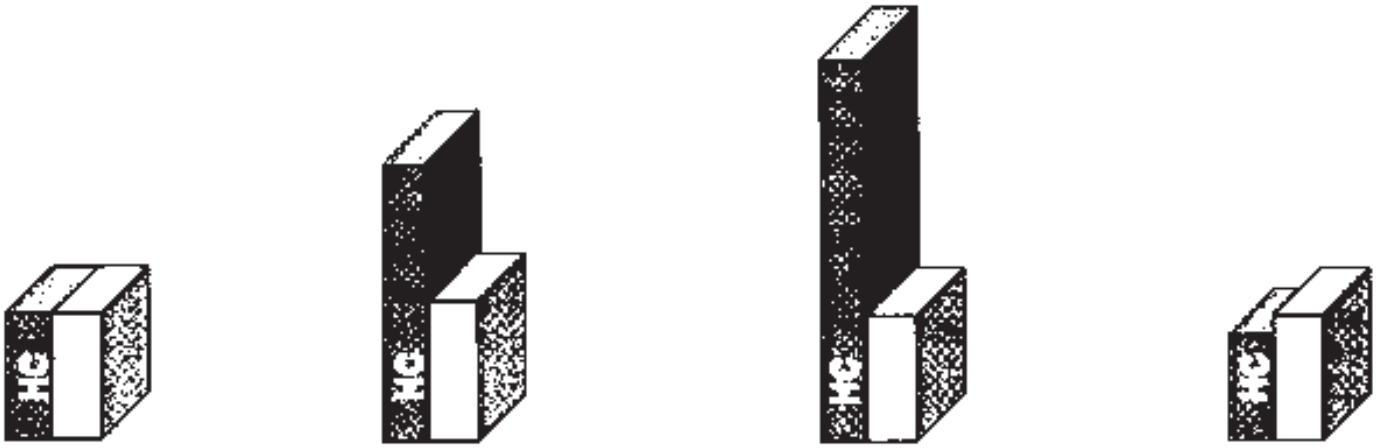
- **Data Indicates DESIGNERS prefer HCMOS due to:**
  - Low Noise
  - Low Power
  - Low Price
- **Requested Improvements**
  - Improve Output Current
  - Improve Power Consumption
  - Improve Package Offering
  - 5V Signal Tolerance
  - Better Availability
  - Higher Speed



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AHC/AHCT: Advanced HCMOS

A Reliable and Effortless Migration Path for HCMOS Users



Ground Bounce (V_{OLP}) | **Static Power Consumption** | **Propagation Delay** | **Drive - I_{OL}**

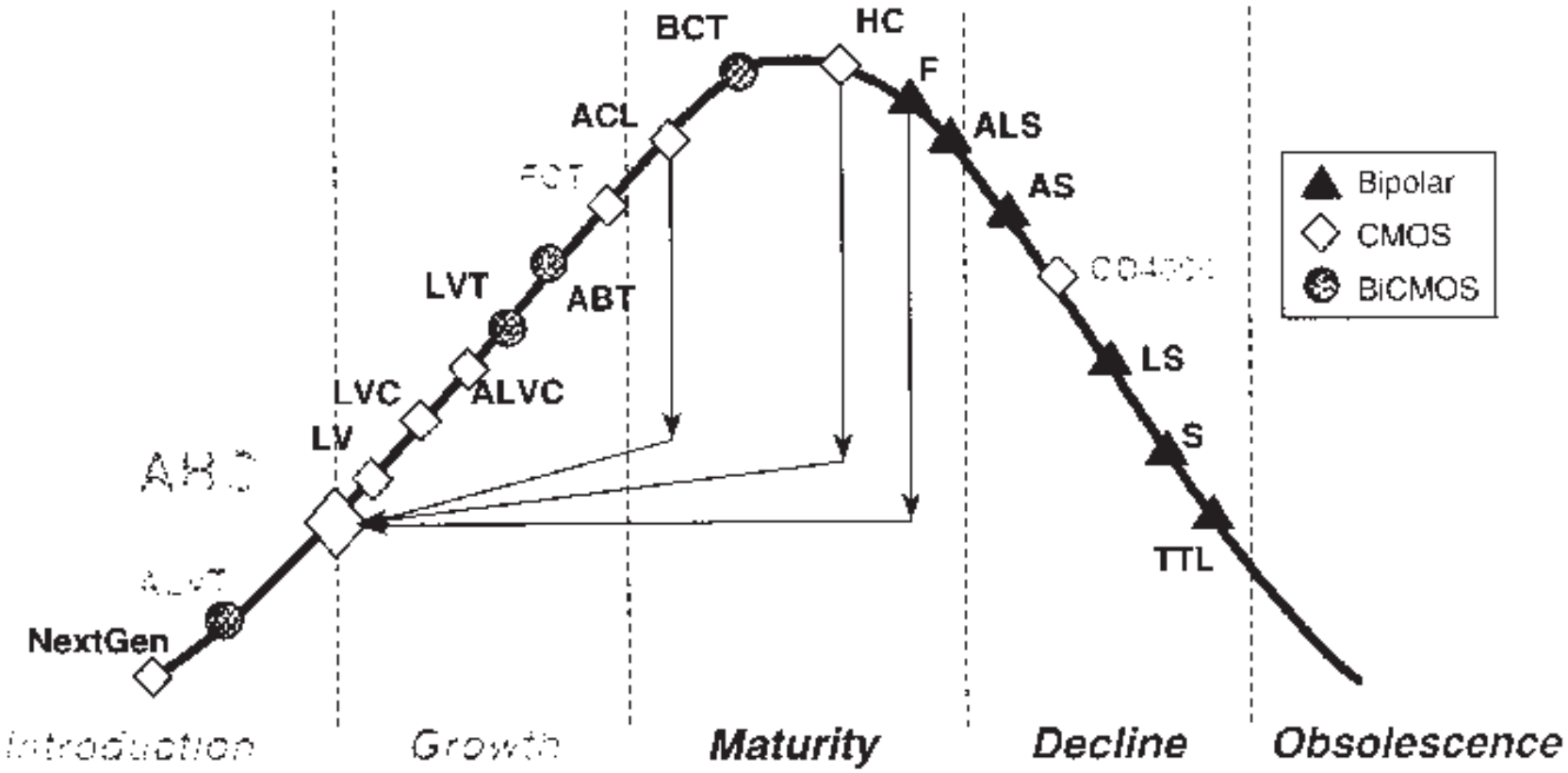
at the current market price as hcmos!

Plus:

- Output Edge Control (OEC™)
- Improved Package Offering: TVSOP, TSSOP, SSOP, SOIC, PDIP
- Widebus™ (16-Bit), Single gate (Single-bit) options available
- 5V Input Tolerance (AHC specified in data sheet at both 5V and 3.3V. Input diode to V_{CC} removed!)
- Highest availability of any logic family on the market! - 5 Worldwide Sources
- TI is the #1 Worldwide Logic Source (1996 - Doubled CMOS and fine pitch package capacity)

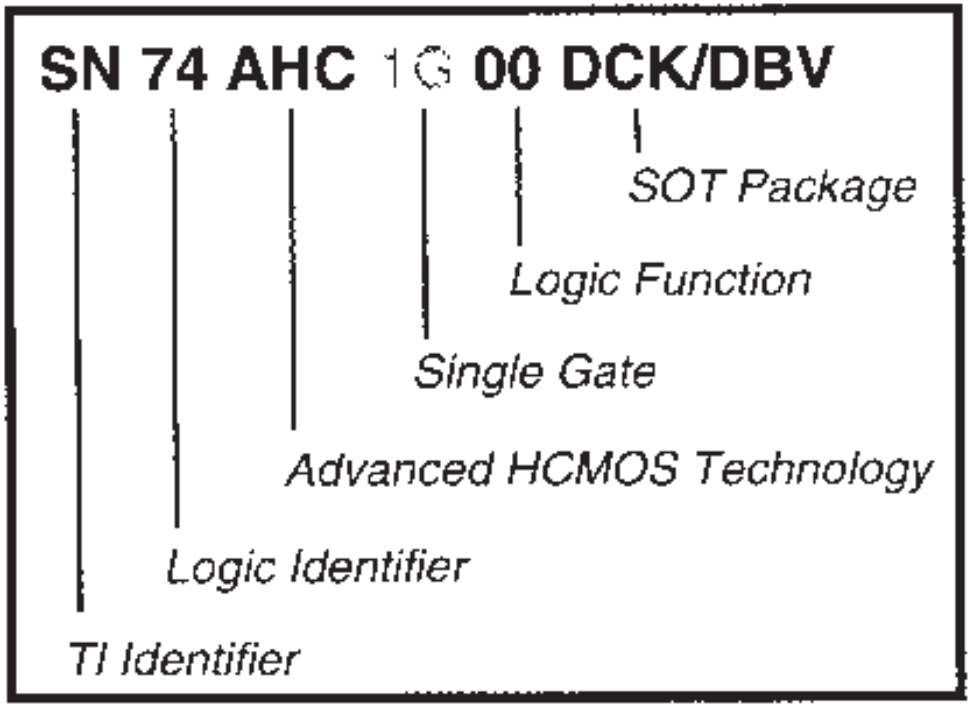
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A Reliable and Effortless Migration Path for HCMOS Users



For HCMOS, AC/ACT, and 74F upgrades, AHC is the family of choice!

AHC/AHCT Single-Gate Logic



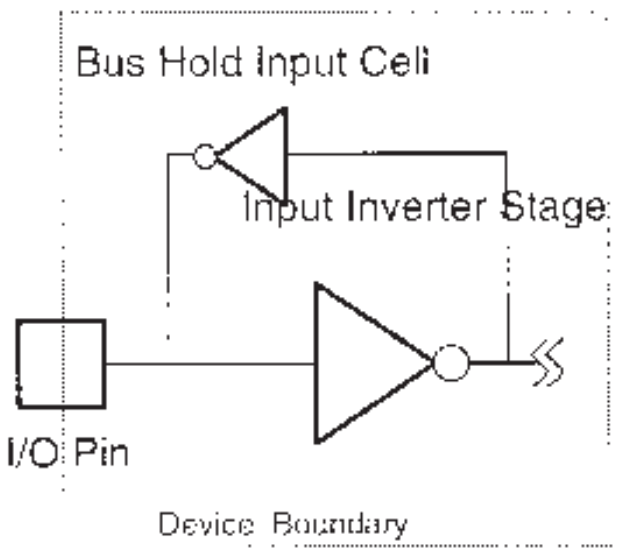
- Simplifies circuit routing
- ASIC modification
- Industry's smallest logic package reduces board space requirement
- Alternate source by Philips
- CMOS Compatible (AHC) and TTL Compatible (AHCT) versions
- Compatible with Toshiba's TC7SH/SETxx series and Fairchild's NC7SH/NC7ST series
- Samples available: now

Cross-Reference (examples)

Texas Instruments	Toshiba	Fairchild
SN74AHC1G00DBV	TC7SH00F	NC7SH00M5
SN74AHCT1G000DBV	TC7ST00F	NC7ST00M5
SN74AHCU1GU04DBV	TC7SHU04F	NC7SU04M5

Texas Instruments	Toshiba	Fairchild
SN74AHC1G00DCK	TC7SH00FU	NC7SH00P5
SN74AHCT1G00DCK	TC7SHT00FU	NC7ST00P5
SN74AHC1GU04DCK	TC7SHU04FU	NC7SU04P5

Bus-Hold Input Characteristics



Bus hold input cell replaces pullup resistor

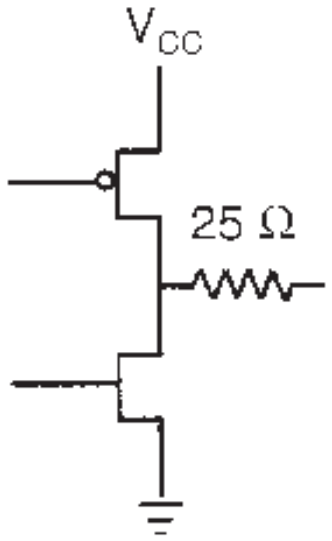
- Holds the last known state of the input
- $I_{I(HOLD)}$ ± 75 µA min holding current at 0.8 and 2V
- Bus hold current does NOT load down the driving output at valid logic levels
- Eliminates the need for external resistors on unused or floating input/output pins
- The "H" in the device name indicates bus-hold

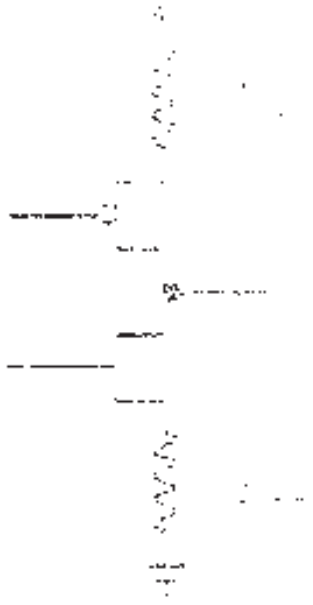
Device	ABT	LV	LVC	ALVC	LVT
Bus Hold versions	✘ *		✘	✘	✘
Non-Bus Hold versions	✘	✘	✘ *	✘ *	

* select functions only

Standard linear & logic

Damping Resistors





TI's Series-Damping Resistor Option

- Limits the current thereby reducing noise from undershoot/overshoot
- Helps in line termination (reduces ringing/line reflection to improve signal quality)

Competitor's Balanced Drive

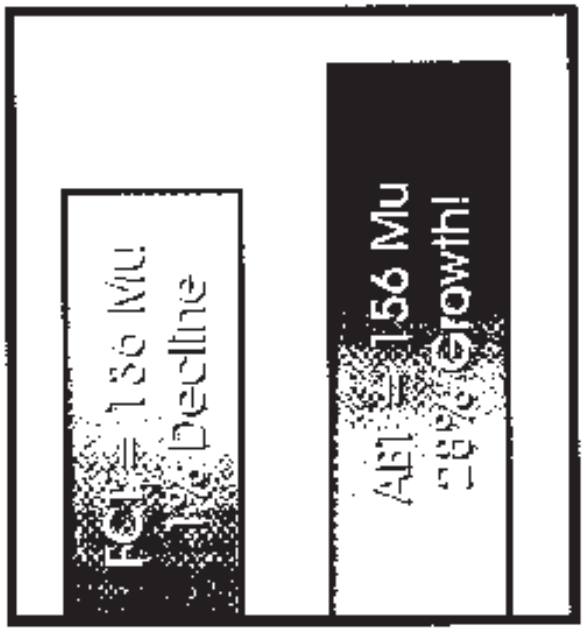
e.g.: 'ABT2245
'ABT162245 → **Extra "2" in device name indicates damping resistor**

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Continued Logic Leadership
ABT vs. FCT

ABT is the undisputed WINNER in the ABT/FCT battle

- FCT TAM at $147M
- ABT TAM at $200M
- TI dominates the ABT market: 80% market share



ABT is the Clear Winner!

Source: Insight Onsite

ABT Offers the Complete 5-V Solution

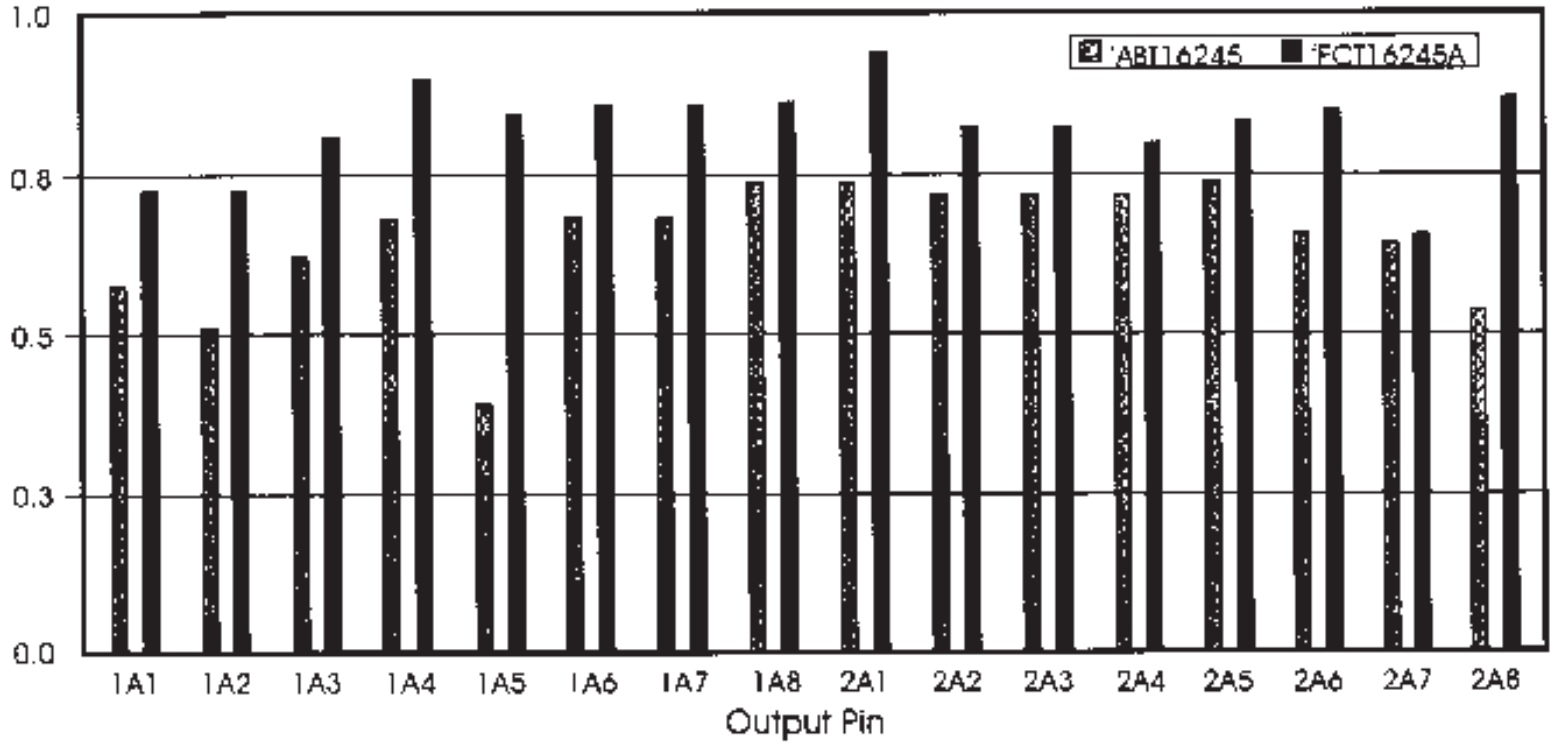
Product Features	ABT	FCT
High-Performance	✓	✓
I_{off} Specification(Live Insertion)	✓	✓
Competitive Pricing	✓	✓
Bus Hold(Selected Functions)	✓	✓
Lowest Ground Bounce	✓	
True Series Damping Resistor Options	✓	
Power-Up 3-State	✓	
Strongest Supplier Base	✓	
JTAG Options Available	✓	
Low-Voltage Migration Path	✓	

Standard
Smart
Logic

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ABT Has Lower Ground Bounce!

V_{OLP}

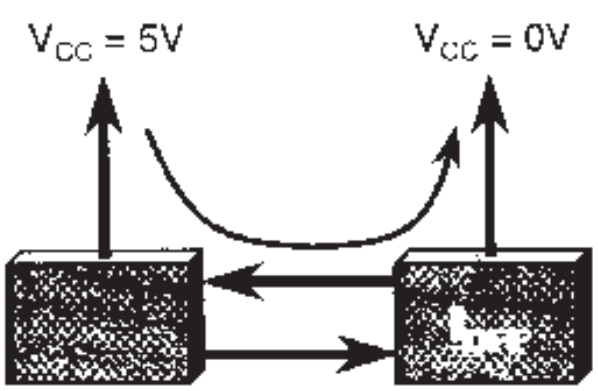


V_{CC} = 5.5V V, C_L = 50 pF, R_L = 500Ω, 15 Outputs Switching,
Freq = 1 MHz, T_A = 25°C, V_{INL} = 0.5V, V_{INH} = 2.5V

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Partial Power-Off

System Function/Capability

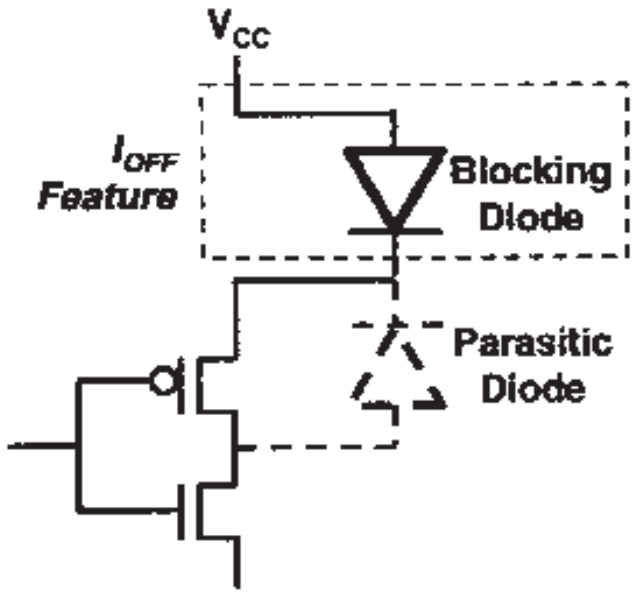


Supporting Chip Spec.

I_{OFF}

Circuit Implementation/Mod.

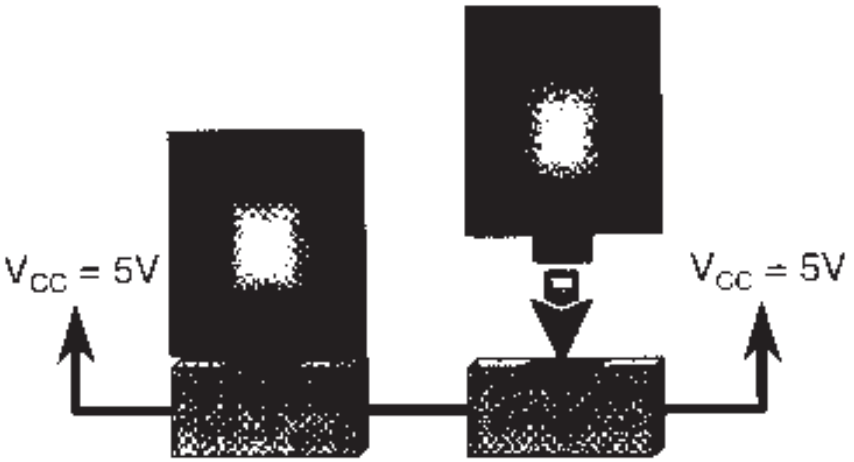
I_{OFF} Circuit



When V_{CC} = 0, I_{PIN} = 0 for V_{PIN} = min to max.

Hot Insertion

System Function/Capability

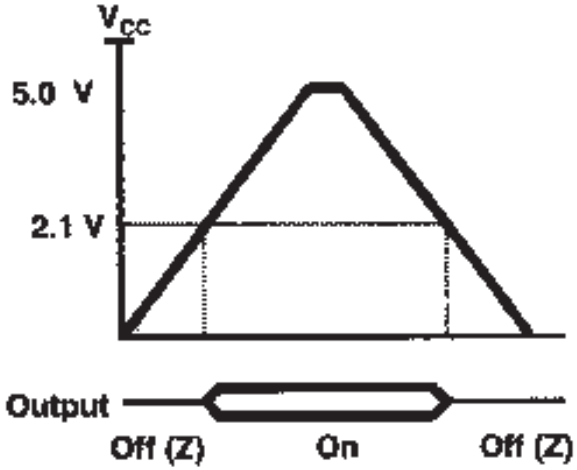


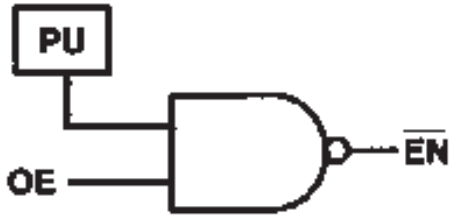
Supporting Chip Spec

I_{OFF}
I_{OZPU}
I_{OZPD}

Circuit Implementation/Mod.

PU3S Circuit



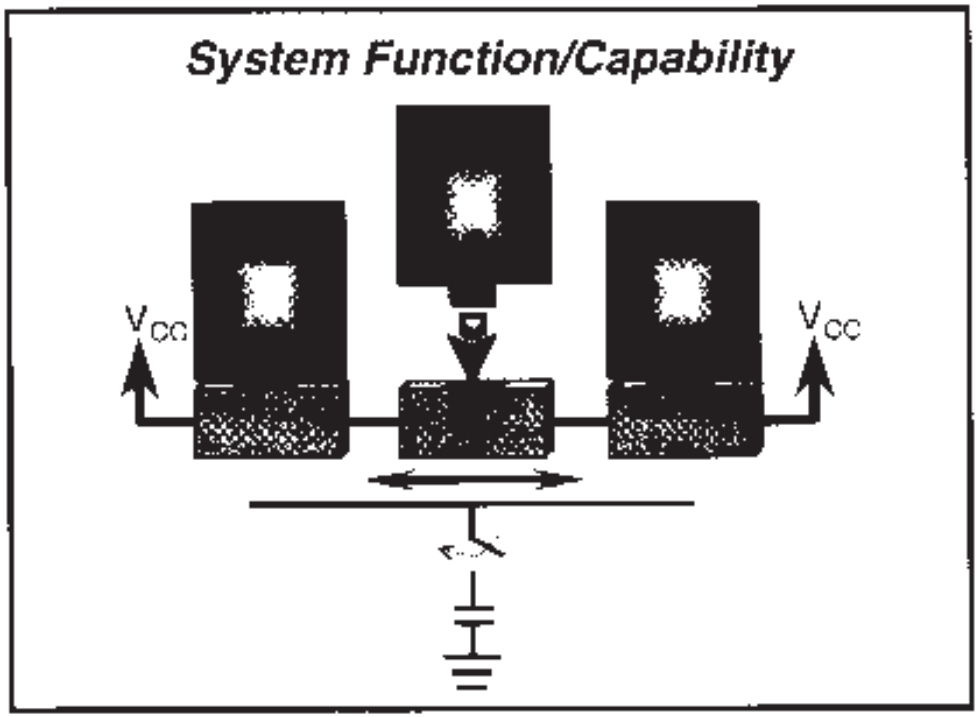


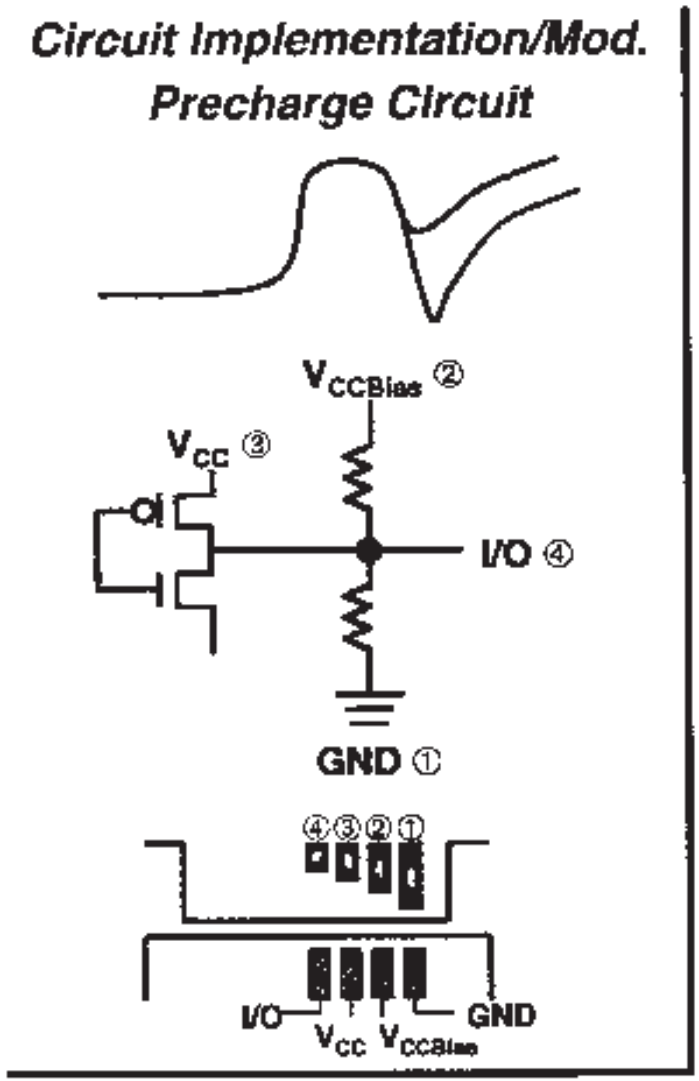
PU = 1 → $\overline{EN}$ = $\overline{OE}$

PU = 0 → $\overline{EN}$ = 1 → Z

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Live Insertion



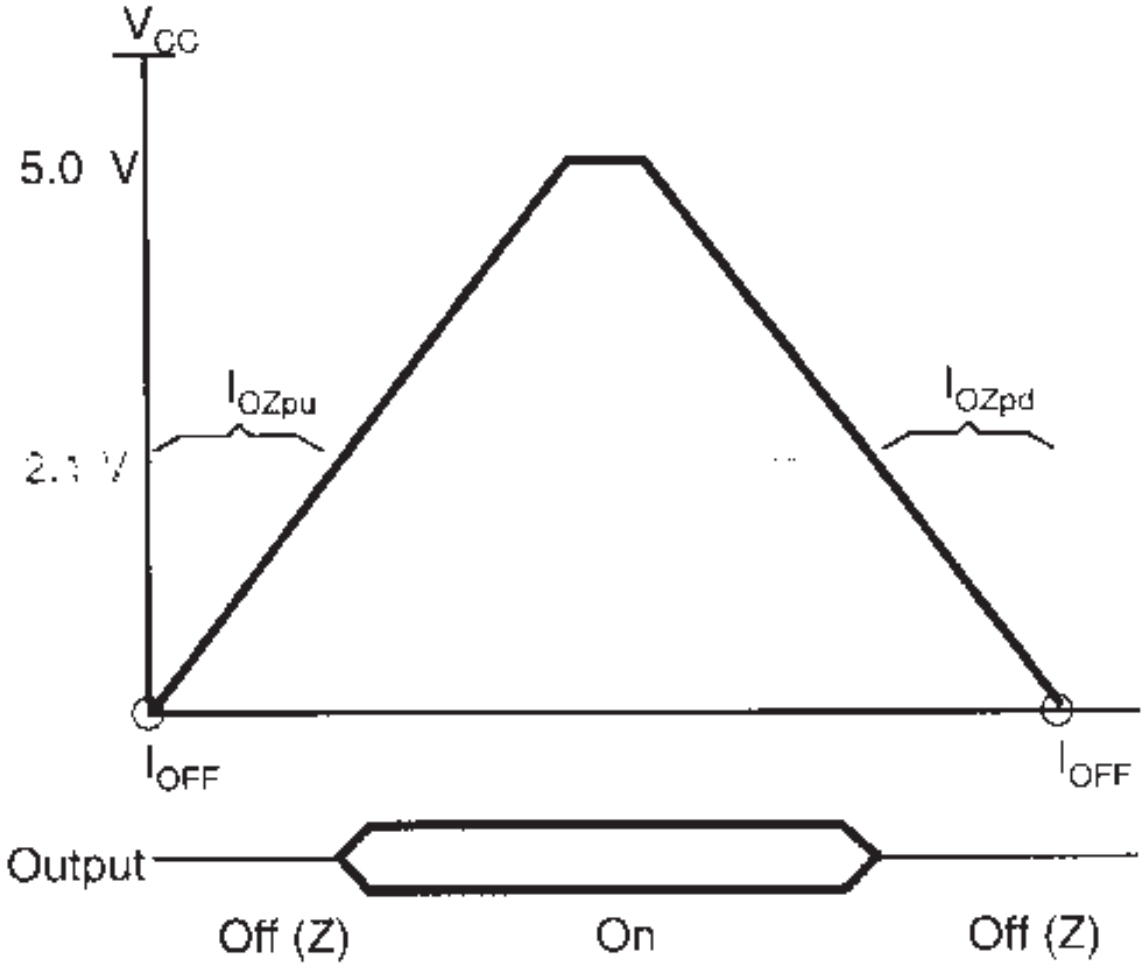


Supporting Chip Spec

I_{OFF}
I_{OZPU}
I_{OZPD}
V_O, V_{CC} = 0, V_{CCBIAS} = min to max

Standard linear & logic

ABT Has Power-Up 3-State!

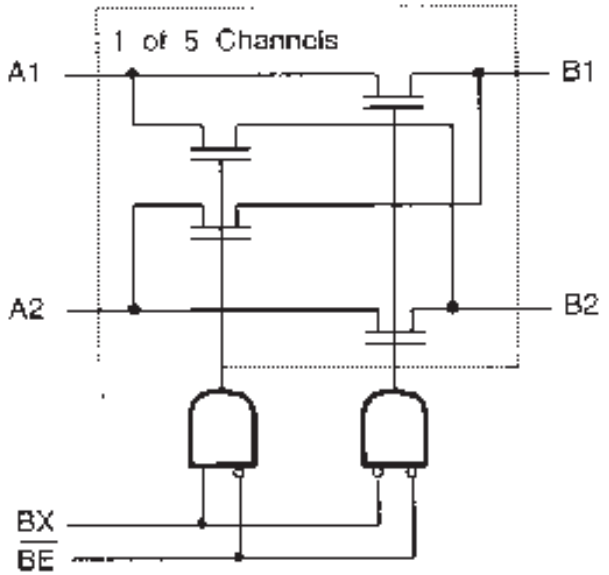


- To ensure valid output levels during power up/power down
  - I_{OZpu}, I_{OZpd} on data sheet
- To ensure high Z on output during power off
  - I_{OFF} on data sheet

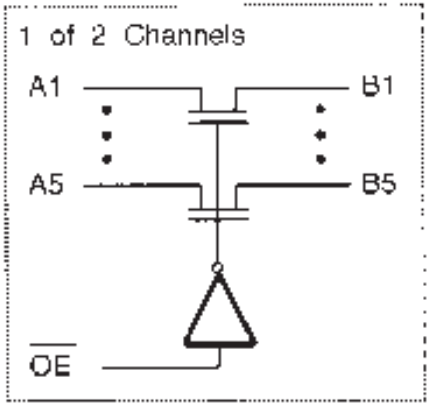
Standard Linear & Logic

CBT Bus-Exchange Switches

CBT3383 BUS EXCHANGER



'CBT3384A BUS SWITCH



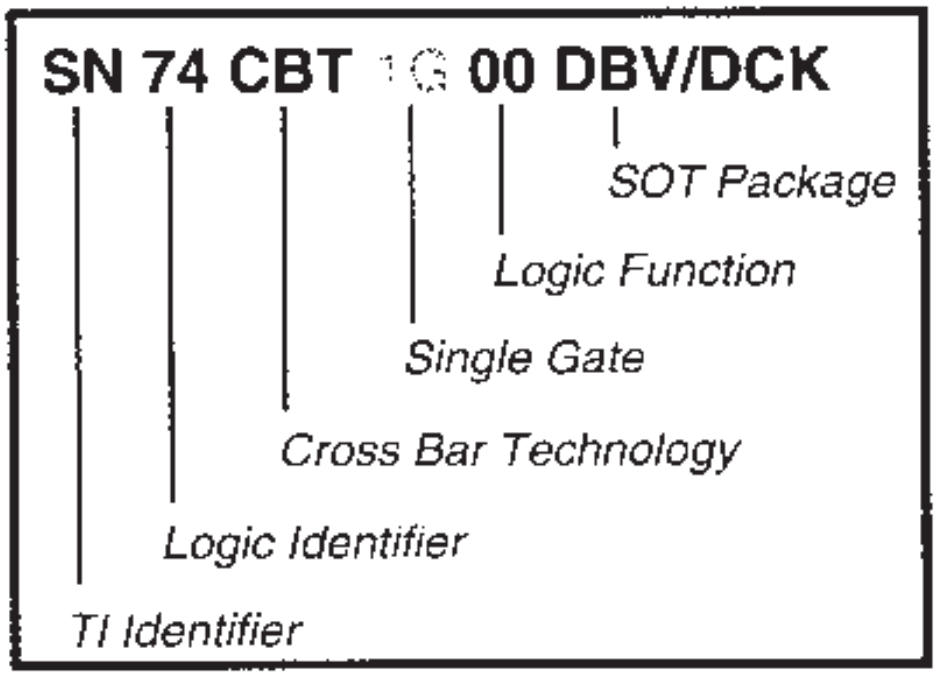
- Simple FET Switches
- Functionally Equivalent To: QS3383 and QS3384
- Industry Standard Pinouts ('244, '245)
- Widebus™ Functions Available
- Fine Pitch Packaging Options (SOIC, SSOP, TSSOP, Widebus, Shrink Widebus™)
- Octals and Widebus available NOW!

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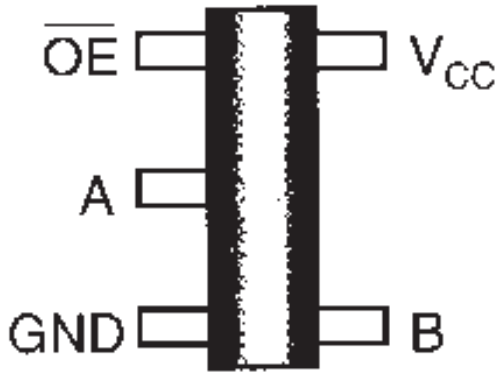
Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated

Standard Linear & Logic

CBT Single-Gate Logic

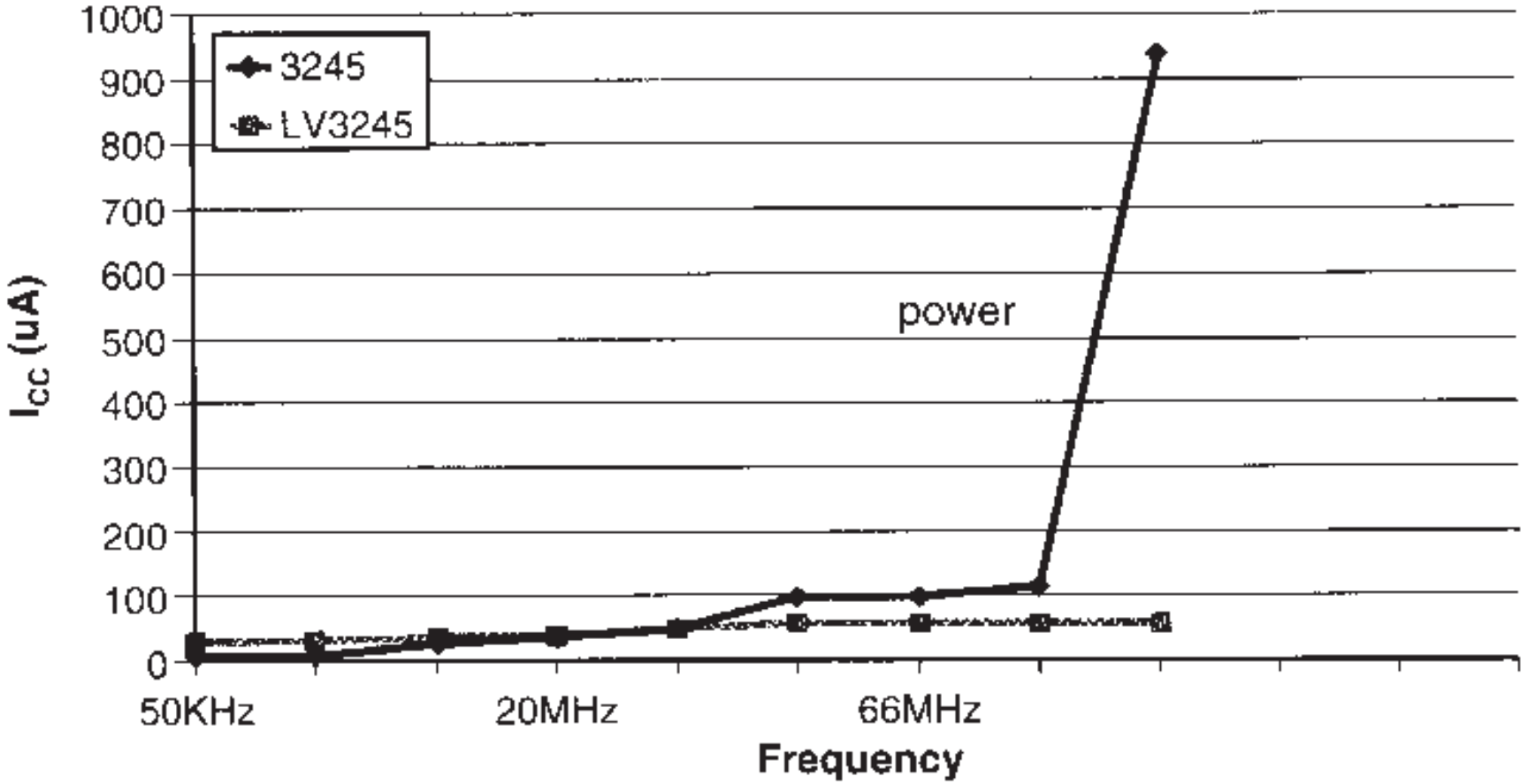


- Simplifies circuit routing
- 250 ps propagation delay
- Low on-state resistance (5Ω)
- Ideal for control signal isolation



1106

CBT Versus CBTLV



	50KHz	1MHz	10MHz	20MHz	33MHz	50MHz	66MHz	100MHz	150MHz
3245	9	9	25	35	48	99	99	113	939
LV3245	29	32	36	40	48	57	58	58	58

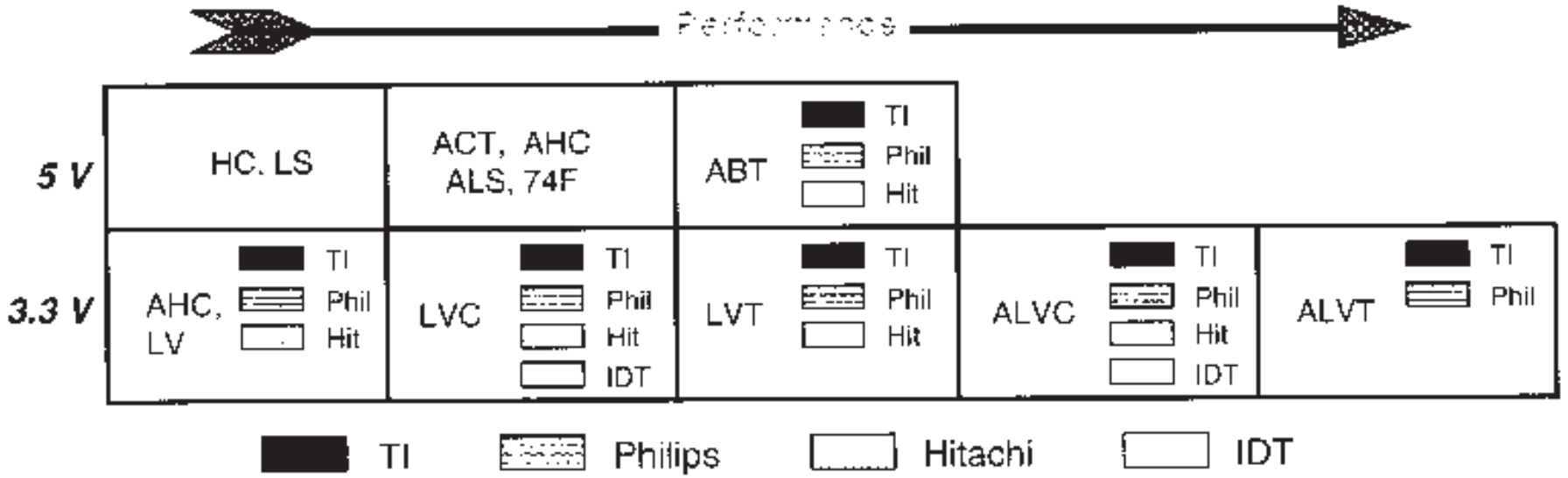
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CBT/CBTLV Product Offering

- Multiple package offerings
- CBTDs with integrated V_{CC} diode for 5V-to-3.3V level translation
- CBTSs with integrated Schottky diodes on inputs/outputs to clamp negative undershoots
- Broad product offering
- 1st to market with CBTLV family

Standard Linear & Logic

Complete Low-Voltage Market Coverage and Standardization



AHC
- ✔8.5 ns speed(5 V)
- ✔13.5 ns speed(3.3 V)
- ✔-8/8 mA drive (5 V)
- ✔-4/4 mA drive(3.3 V)
- ✔5 V or 3.3 V Vcc
- ✔5 V input tolerant
- ✔4 WW sources

LVC
- ✔6.5 ns speed
- ✔-24/24 mA drive
- ✔Ultra-low (20 µA) standby power
- ✔3 WW sources
- ✔Bus hold
- ✔5 V tolerant
- ✔Gate functions
- ✔Live insertion

LVT
- ✔4 ns speed
- ✔-32/64 mA drive
- ✔Low (90 µA) standby power
- ✔3 WW sources
- ✔Bus hold
- ✔5 V tolerant
- ✔Live insertion

ALVC
- ✔3 ns speed
- ✔-24/24 mA drive
- ✔Ultra-low (40 µA) standby power
- ✔3 WW sources
- ✔Bus hold

ALVT
- ✔-32/64 mA drive
- ✔2 WW sources
- ✔Bus hold
- ✔5 V tolerant
- ✔Live insertion

Standard Linear & Logic

Advanced Low-Voltage CMOS - ALVC

Circuit Features

- Bus hold ($I_{I(HOLD)}$)
- Drive capability
  (-24/24 mA @ 3.3 V V_{CC})
  (-6 /12 mA @ 2.5 V V_{CC})
- Low noise
- Damping resistor options
- ESD protection
- Spec'd for 3.3 V and 2.5 V operation

Advantages

- Performance leadership product
- Marketing and applications support
- SPICE models
- Internal and external second sources
- Wide product portfolio
- Specialized memory interface functions available for SDRAMs

Standard Linear & Logic

Low-Voltage BiCMOS - LVT

Circuit Features

- Mixed mode 5 V TTL compatible $V_{I/O}$ 7 V max
- Live insertion (I_{OFF})
- Bus hold ($I_{I(HOLD)}$)
- Drive capability -32/64 mA
- Low noise
- Power on demand
- Damping resistor options
- ESD protection

Advantages

- Largest selling low voltage
- Marketing and applications support
- SPICE models
- Internal and external second sources
- Wide product portfolio

1111

Low-Voltage CMOS - LVC

Circuit Features

- 5 V tolerant
- Live insertion (I_{OFF})
- Bus hold option($I_{I(HOLD)}$)
- Drive capability (-24/24 mA at 3.3 V V_{CC})
- Low noise
- Damping resistor options
- ESD protection

Advantages

- Price/performance
- Second sources
- Broad product offering
- Marketing and applications support
- SPICE models
- Gates
- No bus-hold/damping resistors with competitor (LCX)

Stub Series-Terminated Logic - SSTL

Characteristics:

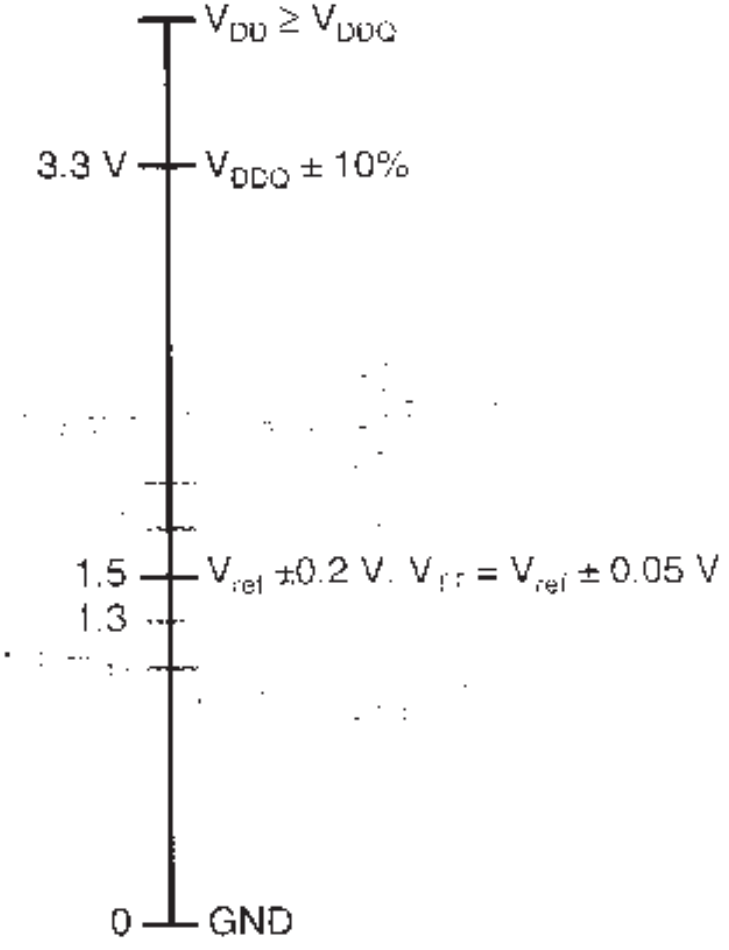
- Supports SSTL_3 and LVTTL signal inputs and outputs
- Input threshold = $V_{REF} \pm 0.2$ $V_{REF} = 1.5V$
- Drive = ± 20 mA
- Interfaces with next generation SDRAM

Benefits:

- Allows higher system clock rate
  - point-to-point communication speeds of 200 MHz

Considering for next device:

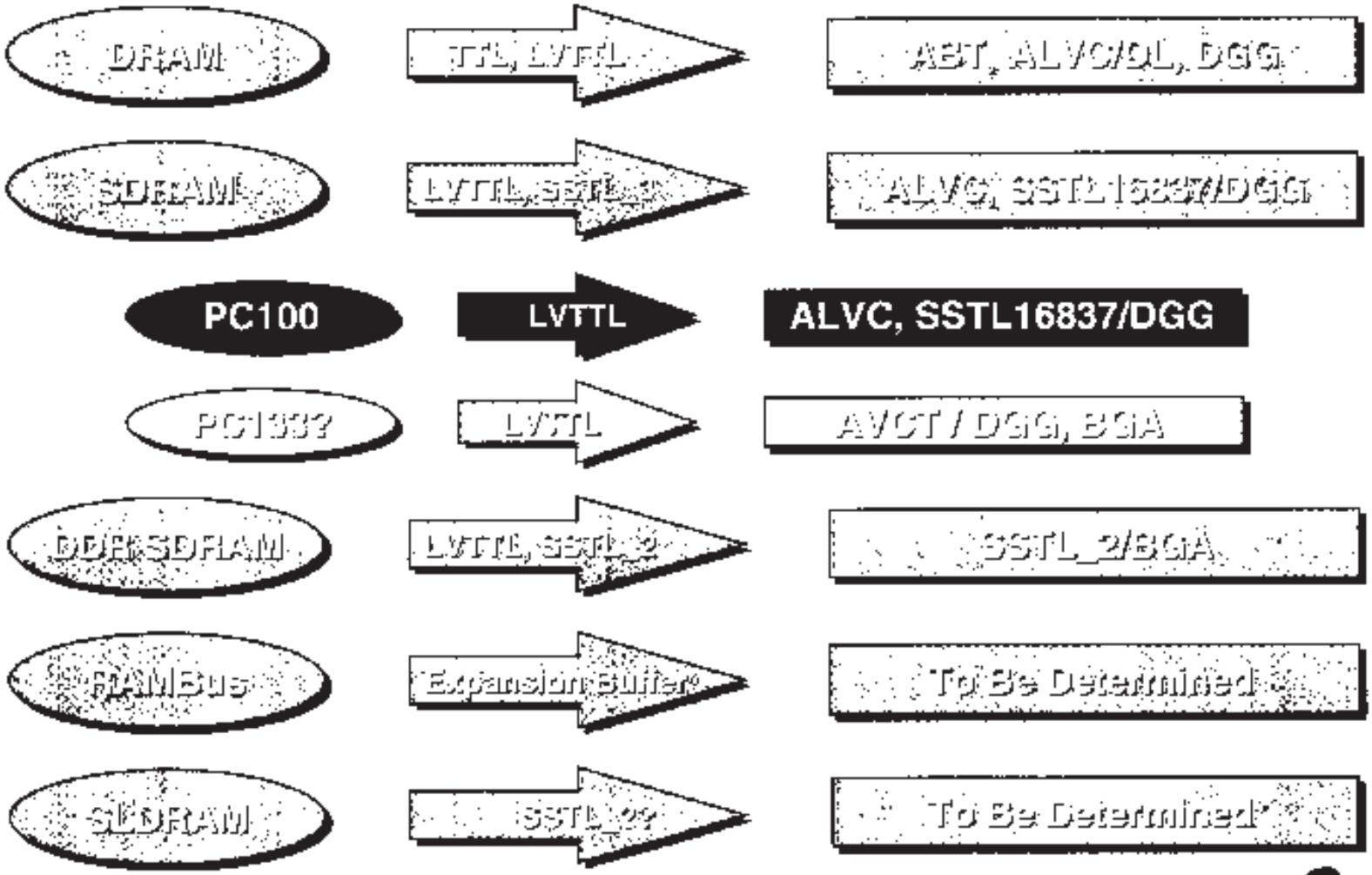
- SSTL Universal Bus Transceivers for data bus
- SSTL registered data multiplexer/exchanger



SSTL_3

Standard Linear & Logic

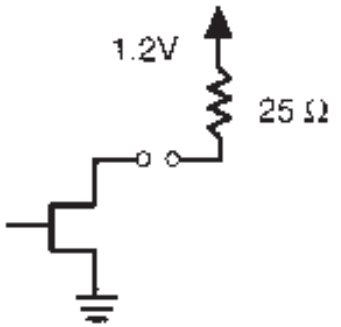
Memory Roadmap with Compatible Logic Families



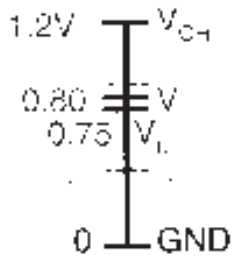
Standard Linear & Logic

What Is GTL?

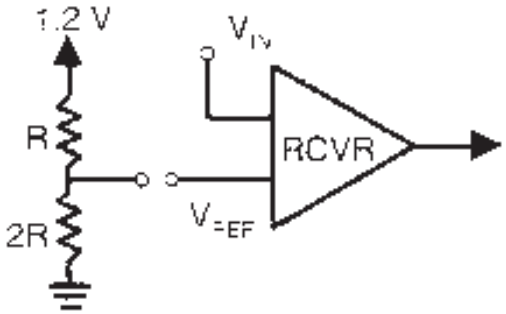
- Driver is an open drain n-channel CMOS transistor



- Reduced voltage swing reduces power and allows integration into VLSI CMOS



- Receiver stage is a differential input with external V_{REF} set at 0.8V. V_{REF} is derived from simple R/2R voltage divider of 1.2V pull-up.



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Advantages of GTL

Noise: External V_{REF} provides common-mode noise immunity (derived from 1.2V pull-up).

Low signal amplitude reduces EMI

Speed: Absence of Reflections Allows Higher System Clock Rate
- Very high speed point-to-point communication (100+ MHz)
- Backplane speeds over 60 MHz

Power: High speed, low power backplane alternative to BTL or ECL

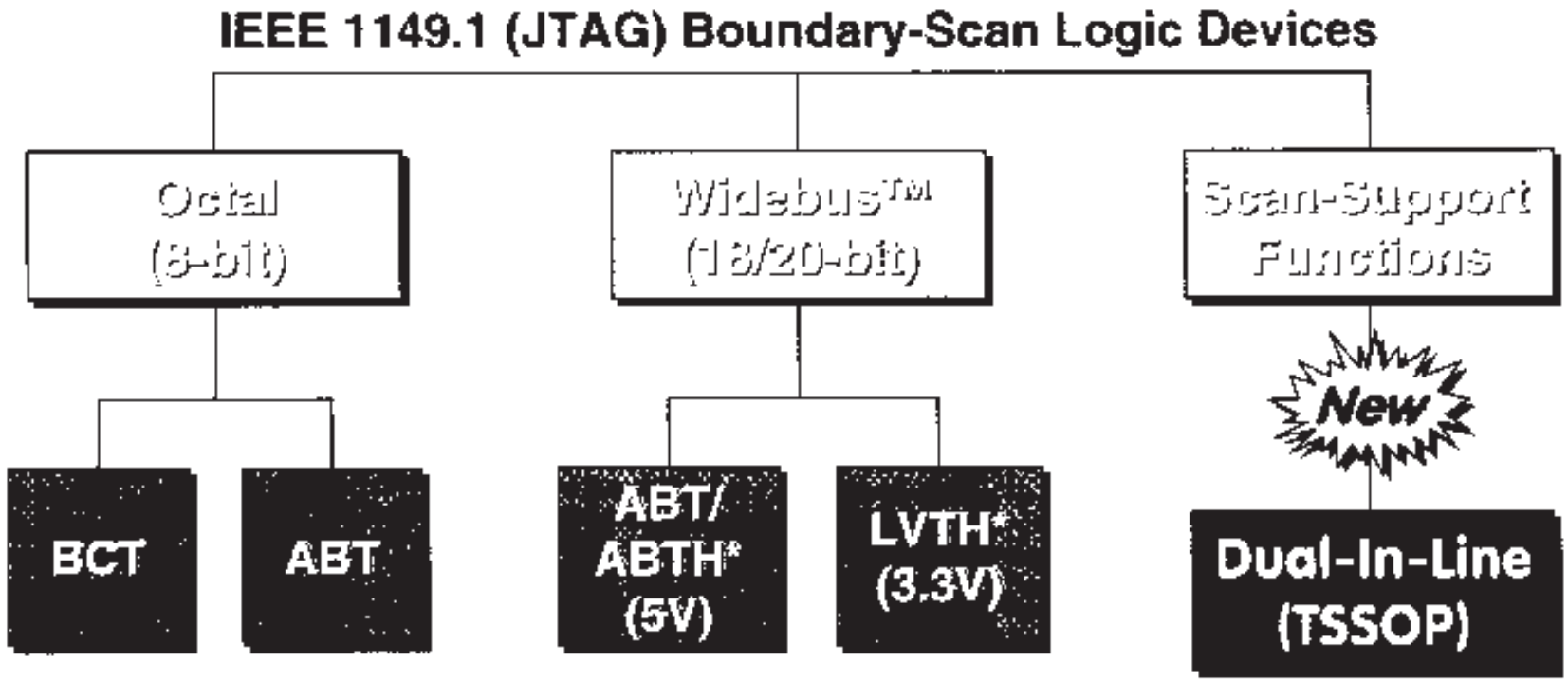
Power Comparison (160 active I/Os)

Technology	Power (watts)	Termination
ECL 10K	20	25 Ω to 3.0V
BTL	11	16.5 Ω to 2.0V
GTL	1.5	50 Ω to 1.2V

Cost: GTL transceivers are less than half the cost per bit as BTL drivers of comparable speeds.

What Does TI Offer in IEEE 1149.1 (JTAG) Silicon Solutions?

40+ commercially released devices

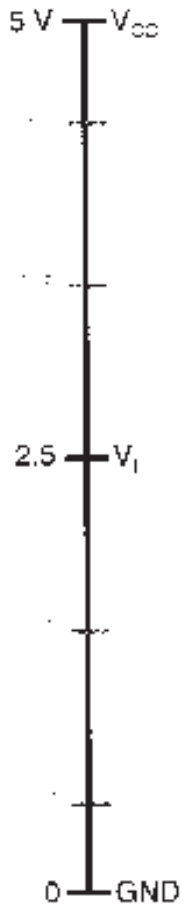


* Bus Hold option

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IC Basics

Comparison of Switching Standards



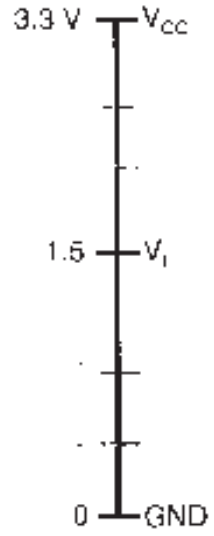
5V CMOS
Rail-to-Rail 5V
HC, AHC, AC



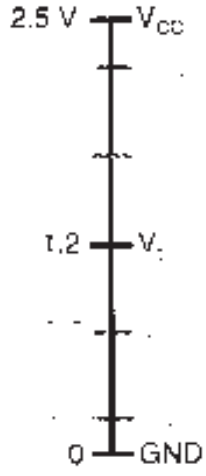
ETL
Larger Noise
Margins - ABTE



5V TTL
Standard TTL - ABT,
AHCT, HCT, ACT, Bipolar



LVTTL
LVT, LVC,
ALVC, LV

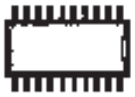


2.5V CMOS
ALVC

Standard Linear & Logic

1118

Packaging Options

8 Bits SOIC	8 Bits SSOP	8 Bits TSSOP	16/18 Bits Widebus™	16/18 Bits TSSOP	16/18 Bits TVSOP
					
20-Pin SOIC (DW) Area = 137 mm² Height = 2.65 mm Lead Pitch = 1.27 mm	**20-Pin SSOP (DB)** Area = 62 mm² Height = 2.0 mm Lead Pitch = 0.65 mm	**20-Pin TSSOP (PW)** Area = 46 mm² Height = 1.1 mm Lead Pitch = 0.65 mm	**48-Pin SSOP (DL)** Area = 171 mm² Height = 2.74 mm Lead Pitch = 0.635 mm	**48-Pin TSSOP (DGG)** Area = 108 mm² Height = 1.1 mm Lead Pitch = 0.5 mm	**48-Pin TVSOP (DGV)** Area = 63 mm² Height = 1.2 mm Lead Pitch = 0.4 mm

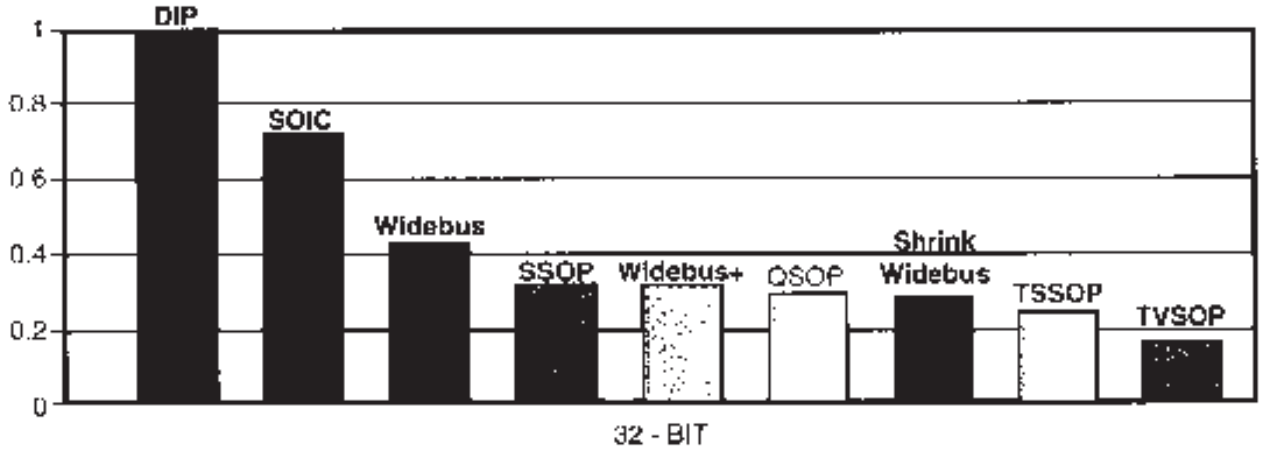
Single Gate



5-Pin SOT (DBV)
Area = 8.12mm²
Height = 1.2mm
Lead Pitch = 0.95 mm



5-Pin SOT (DCK)
Area = 4.2mm²
Height = 1.0 mm
Lead Pitch = 0.65 mm



Bold indicates TI TTL/CMOS logic packages.

(TI package designators)

Widebus, Widebus+ and Shrink Widebus are trademarks of Texas Instruments Incorporated

Standard Linear & Logic

Logic CD-ROM Features

- Easy-to-use navigator and search engine
- Device data sheets and mechanical drawings
- Application reports
- Device models
- Press announcements/product spotlights
- Vendor cross-reference
- Glossary, worldwide contacts, and FAQs
- Literature number SCBC001

Standard Linear & Logic

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FUNCTIONAL INDEX

SECTION 2
FUNCTIONAL INDEX

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BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																			
			ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Single	3S	'1G125														✢	✢	✢				✢	
		'1G126														✢	✢	✢				✢	
Quad	3S	'125	✓			✓	✓			✓	✓					✓	✓	✢	✓	✓	✓	✓	
		'126	✓			✓				✓	✓		✶			✓	✓	✢	✓		✓	✓	
Noninverting Hex	3S	'365									✓		✶						✓				
	3S	'367									✓		✓			✢	✢		✓				
Inverting Hex	3S	'368									✓		✓						✓				
Noninverting Octal	3S	'241				✓	✓	✓	✓	✓	✓	✓		✓	✓				✓			✢	
		'244	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓	✓	✢	✓	✓	✓	✓	
		'1244						✓															
		'541	✓			✓		✓		✓	✓					✓	✓		✓	✓		✓	
	OC	'757							✓														
		'760				✓		✓	✓														
Inverting Octal	3S	'240	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓	✓		✓	✓	✓	✓	
		'540	✓			✓		✓			✓					✓	✓		✓	✓		✓	
	OC	'756				✓			✓														
Inverting and Noninverting Octal	3S	'230							✓														
Octal With Series Resistors on Output	3S	'2240	✓			✓		✓															
		'2241	✓																				
		'2244	✓			✓				✓												✓	
		'2541						✓															
Noninverting 10 Bit	3S	'827	✓																			✓	
		'29827				✓		✓															
Inverting 10 Bit	3S	'828																				✓	
		'29828						✓															
10 Bit With Series Resistors	3S	'2827	✓			✓																	
		'2828				✓																	

OC = open collector OD = open drain 3S = 3-state

✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✢ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

Buffers/Drivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																				
			ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
11 Bit With Series Resistors	3S	'5400	✓																				
		'5401	✓																				
12 Bit With Series Resistors	3S	'5402	✓																				
		'5403	✓																				
Noninverting 16 Bit	3S	'16241	✓				✛								✓			✛				✛	
		'16244	✓	✓	✛		✓							✓	✓	✓	✓	✓				✓	
		'16541	✓				✛								✓	✓	✓	✛				✓	
Inverting 16 Bit	3S	'16240	✓		✛		✛							✓	✓	✓	✓	✓				✓	
		'16540	✓												✓	✓	✓	✛				✓	
		'16828																	✛				
16 Bit With Series Resistors	3S	'162240					✓											✛					
		'162241					✓																
		'162244	✓		✛		✓											✓				✓	
		'162541					✓																
17 Bit IEEE P1284	3S	'161284																				✓	
Noninverting 18 Bit	3S	'16825	✓												✓			✓					
		'16835					✓											✓					
18 Bit With Series Resistors	3S	'162825	✓																				
Noninverting 20 Bit	3S	'16827	✓		✛										✓			✓					
20 Bit With Series Resistors	3S	'162827	✓															✓					
1-to-2 Address Drivers	3S	'16830																✛					
1-to-2 Address Drivers With Series Resistors	3S	'162830																✛					✓ALVCHS
1-to-4 Address Drivers	3S	'16344																✓					
		'16831																✓					
		'16832																✓					

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✶ Product available as a military device only * Product planned as a military device

Buffers/Drivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																				
			ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
1-to-4 Address Drivers With Series Resistors	3S	'162831																✓					
		'162832																✓					

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																				
			ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Noninverting Quad	3S	'243						✓		✓	✓												
Noninverting Octal	3S	'245	✓			✓	✓	✓	✓	✓	✓			✓•*	✓•	✓	✓	+	✓	✓	✓	✓	+LVTR
		'1245						✓															
		'25245	✓			✓																	
		'442									✓												
		'466									✓												
		'645						✓	✓		✓								✓	✓			
		'1645						✓															
	OC	'621						✓		✶													
		'641						✓	✓		✓												
	OC/3S	'639						✓	✓														
Inverting Octal	3S	'620	✓					✓															
		'623	✓				✓			✓	✓								✓	✓			
		'640	✓				✓	✓	✓		✓								✓				
		'1640						✓															
	OC	'642						✓			✓												
	OC/3S	'638						✓															
Octal With Series Resistors on B Port	3S	'2245					✓			✓												+	✓LVCR ✓ABTR
Octal 3.3-V-to-5-V Level Shifter	3S	'4245																				✓	✓LVCC
Noninverting Octal With Adjustable Output Voltage	3S	'3245																					✓LVCC

OC = open collector OD = open drain 3S = 3-state

✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Noninverting 9 Bit	3S	'863	✓																			✓	
		'29863				✓		✓															
Noninverting 10 Bit	3S	'861	✓																			✓	
Noninverting 16 Bit	3S	'16245	✓	✓	✢		✓							✓	✓	✢	✓	✓				✓	✓ABTE
		'16623	✓												✓								
16 Bit With Series Resistors	3S	'162245	✓		✢		✓											✓					✓LVCR
Noninverting 16-Bit 3.3-V-to-5-V Level Shifter	3S	'164245																✓					
Inverting 16 Bit	3S	'16640	✓											✓	✓								
		'16620												✓	✓								
Noninverting 18 Bit	3S	'16863	✓												✓			✓					
Inverting 18 Bit	3S	'16864													✓								
Noninverting 20 Bit	3S	'16861													✓								

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✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✢ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

Bus Transceivers With Registers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																				
			ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Noninverting Octal Registered	3S	'543	✓			✓	✓			✓					•							✓
		'544																				+
		'646	✓			✓	✓	✓	✓		✓								✓	✓		+
		'647						✓			✓											
		'652				✓	✓	✓	✓		✓			•	•				✓	✓		✓
	OC/3S	'653						✓														
		'654						✓														
Inverting Octal Registered	3S	'648						✓	✓		✓											
		'651	✓					✓	✓													
Noninverting 16 Bit Registered	3S	'16470	✓												✓							
		'16543	✓		+		✓							✓	✓			✓				✓
		'16646	✓				✓							✓	✓							✓
		'16652	✓		+		✓							✓	✓			+				✓
Inverting 16 Bit Registered	3S	'16544													✓							
		'16648													✓							
		'16651													✓							
		'16952	✓				✓								✓			+				✓
Noninverting 18 Bit Registered	3S	'16474													✓							
		'16524																✓				
		'16525																✓				
Noninverting 18 Bit Registered With Series Resistors	3S	'162525																✓				

Bus Transceivers With Latches

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																			
			ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Noninverting Octal Registered	3S	'2952	✓			✓															✓
Inverting Octal Registered	3S	'2953			✓																

OC = open collector OD = open drain 3S = 3-state
✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated
✶ Product available as a military device only * Product planned as a military device

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY							
			ABT	ALVT	BCT	LVT	LV	LVC	ALVC	OTHER
Noninverting 9-Bit 4-Port UBE	3S	'16409							✓	
Noninverting 9-Bit 4-Port UBE With Series Resistors	3S	'162409							✓	
16-Bit Universal Bus Drivers	3S	'16334							✓	
16-Bit Universal Bus Drivers With Series Resistors on B Port	3S	'162334							✓	
Noninverting 18-Bit UBT	3S	'16500	✓			✓			✓	
		'16501		✛		✓			✓	
		'16600	✓						✓	
		'16601	✓	✛					✓	
		'16834							✛	
		'16835				✓			✓	
Noninverting 36-Bit UBT	3S	'32501	✓							
Noninverting 16-Bit Tri-Port UBE	3S	'32316	✓							
Noninverting 18-Bit Tri-Port UBE	3S	'32318	✓							
18-Bit UBT With Series Resistors on B Port	3S	'162500	✓							
		'162501	✓							
		'162601	✓						✓	
		'162835							✓	
18-Bit UBT With Input and Output Series Resistors on A and B Port	3S	'162601								✓ALVCHR
Noninverting 18-Bit UBT With Parity Generators/Checkers	3S	'16901							✓	
18- to-36-Bit Registered Bus Exchanger With Series Resistors	3S	'162282							✓	
20-Bit Universal Bus Drivers With Series Resistors	3S	'162836							✓	

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✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✛ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

Parity Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																		
			ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Octal	3S	'656												✓								
		'657	✓																			
8-Bit to 9-Bit Bus	3S	'833	✓																			
8/9 Bit With Parity Checkers/ Generators	3S	'853	✓																			
	3S/OC	'29833					✓															
		'29834			✓																	
		'29854			✓																	
16 Bit	3S	'16657	✓											✓								
Dual 8-Bit to 9-Bit Bus	3S	'16833	✓											✓								
		'16853	✓																			

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✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✛ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

Non-TTL Transceivers/Latches

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY
7-Bit TTL/BTL Transceivers	OC	'2041	✓FB
8-Bit TTL/BTL Transceivers	OC	'2040	✓FB
8-Bit TTL/BTL Registered Transceivers	OC	'2033	✓FB
9-Bit TTL/BTL Competition Transceivers	OC	'2032	✓FB
9-Bit TTL/BTL Address/Data Transceivers	OC	'2031	✓FB
11-Bit Incident Wave Switching Transceivers	OC	'16246	✓ABTE
14-Bit HSTL-to-LVTTL Memory Address Latches		'162822	✓HSTL
14-Bit SSTL_2/3 Universal Bus Drivers	3S	'16857	✢SSTL
16-Bit LVTTL-to-GTL UBT With Live Insertion	OD	'1655	✓GTL
Noninverting 16-Bit Transceivers	OC	'16245	✓ABTE
17-Bit LVTTL-to-BTL Universal Storage Transceivers With Buffered Clock Lines	OC	'1653	✓FB
17-Bit TTL/BTL Universal Storage Transceivers	OC	'1651	✓FB
Noninverting 17-Bit UBT With Buffered Clock Outputs and Output Edge Control (OEC™)	OD	'16616	✓GTL
18-Bit TTL/BTL Universal Storage Transceivers	OC	'1650	✓FB
18-Bit LVTTL-to-GTL/GTL+ Registered Transceivers	OC	'16622	✓GTL
		'16923	✓GTL
Noninverting 18-Bit UBT With Output Edge Control (OEC™)	OD	'16612	✓GTL
20-Bit SSTL_3 Universal Bus Drivers	3S	'16837	✓SSTL

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✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✢ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

FLIP-FLOPS AND LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																		
			ABT	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Single D-Type	3S	'1G79															✢				✢
Dual J-K Edge Triggered	3S	'73								✓											
		'107								✓											
		'109					✓	✓	✓	✓								✓			
		'112					✓		✓	✓	✓							✓			✓
Dual D-Type		'74					✓	✓	✓	✓	✓	✓	✓•	✓•	✓	✓	✢	✓	✓	✓	✓
Dual 4 Bit D-Type Edge Triggered	3S	'876					✓	✓													
Quad D-Type		'175					✓	✓	✓	✓	✓	✓						✓			
Quad D-Type With Clock Enable		'379								✓											
Quad J-K		'276										✓									
		'376										✓									
Hex D-Type		'174					✓	✓	✓	✓	✓				✢	✢		✓		✓	
		'378								✶											
Octal D-Type True Data	3S	'374	✓		✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓	✓	✢	✓	✓	✓	✓
		'574	✓		✓	✓	✓	✓	✓				✓	✓	✓	✓		✓	✓	✓	✓
Octal D-Type True Data With Clear		'273	✓			✓	✓			✓					✓	✢		✓	✓	✓	
	3S	'575					✓	✓													
		'874					✓	✓													
Octal D-Type True Data With Clock Enable		'377	✓						✓	✓								✓	✓		
Octal D-Type Inverting	3S	'534	✓				✓						✓	✓				✓			
		'564					✓						✓	✓							
		'576					✓	✓													
Octal Dual Ranked True Data	3S	'4374						✓													
Octal Inverting With Clear	3S	'577					✓														

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Flip-Flops (continued)

DESCRIPTION	OUTPUT	TYPE	ABT	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Octal True Data	3S	'825						✓													
9 Bit True Data	3S	'823	✓					✓													✓
		'29823			✓		✶														
10 Bit Noninverting	3S	'16820															✓				
10 Bit True Data	3S	'821	✓					✓													✓
		'29821			✓		✓														
16 Bit Noninverting	3S	'16374		✢		✓							✓	✓	✓	✓	✓				✓
16 Bit D-Type With Series Resistors	3S	'162374				✓											✓				
18 Bit Noninverting	3S	'16823	✓										✓	✓			✓				
18 Bit Bus Interface With Series Resistors	3S	'162823	✓																		
20 Bit With Dual Outputs and Series Resistors	3S	'162820															✓				
20 Bit Noninverting	3S	'16721															✓				
		'16821	✓	✢										✓			✓				
20 Bit Noninverting With Series-Damping Resistors	OD	'162721															✓				
		'162821															✢				

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Latches

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY																	
				ABT	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
D-Type Edge Triggered Inverting and Noninverting	8	3S	'996					✓														
D-Type Transparent Readback, True	8	3S	'990					✓														
	9	3S	'992					✓														
	10	3S	'994					✓														
D-Type Transparent With Clear, True Outputs	8	3S	'666					✓														
D-Type Transparent With Clear, Inverting Outputs	8	3S	'667					✓														
D-Type Transparent True	8	3S	'373	✓		✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓*	✓*	+	✓	✓	✓	✓
			'2373	✓						✓												
			'573	✓		✶	✓	✓	✓	✓				✓	✓	✓*	✓*		✓	✓	✓	✓
	16	3S	'16373	✓	+		✓							✓	✓	✓	✓	✓				✓
D-Type Dual 4 Bit Transparent True	8	3S	'873					✓	✓													
D-Type Transparent Inverting	8	3S	'533	✓				✓	✓					✓	✓							
			'563					✓						✓	✓				✓			
			'580					✓														
Addressable	8	2S	'259					✓			✓								✓			
D-Type True Inputs	8	3S	'845					✓														
	9	3S	'843	✓				✓														+
			'29843			✓																
	10	3S	'841	✓				✓														✓
			'29841			✓		✓														
	18	3S	'16843	✓														+				
	20	3S	'16841	✓											✓			✓				

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FLIP-FLOPS AND LATCHES

Latches (continued)

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY																	
				ABT	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
D-Type True Inputs With Series Resistors	20	3S	'162841	✛											✛			✓				
D-Type Inverting Inputs	10	3S	'842					✓														
D-Type	4		'75								✓											
Quad Set/Reset			'279								✓		✶									
Bistable	4		'375								✓											
4 × 4 Register File			'670								✓											
Dual 16 Word × 4 Bits		3S	'870					✓														
D-Type With Series Resistors	16	3S	'162373				✛															

BUS-TERMINATION ARRAYS

Bus-Termination Arrays

DESCRIPTION	TYPE	TECHNOLOGY		
		F	S	ACT
10 Bit	'1071			✓
16 Bit	'1073			✓
8 Bit Schottky Barrier Diode	'1050		✓	
	'1056	✓	✓	
12 Bit Schottky Barrier Diode	'1051		✓	
16 Bit Schottky Barrier Diode	'1016	✓		
	'1052		✓	
	'1053		✓	

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BUS SWITCHES

Bus Switches

DESCRIPTION	TYPE	TECHNOLOGY				
		CBT	CBTS	CBTD	CBTLV	OTHER
Single Bus Switches	'1G125	✓			✢	
	'1G384	✢	✢	✢		
Quad Bus Switches	'3125	✓			✢	
	'3126	✓			✢	
Dual 4-Bit Bus Switches With '244 Pinout	'3244	✓				
8-Bit Bus Switches With '245 Pinout	'3245	✓			✓	
Dual 4-Bit-to-1-Bit FET Multiplexers/Demultiplexers	'3253	✓			✢	
8-Bit-to-1-Bit Multiplexers/Data Selectors	'3251	✓			✢	
Quad 2-to-1-Bit FET Multiplexers/Demultiplexers	'3257	✓			✢	
Dual Bus Switches	'3306	✓	✓	✓		
8-Bit Bus Switches	'3345	✓				
10-Bit Bus-Exchange Switches	'3383	✓			✢	✢CBTH
10-Bit Bus Switches	'3384	✓	✓	✓	✢	
	'3861	✢		✢	✢	
10-Bit Bus-Exchange Switches With Extended Voltage Range	'3386	✢				
Quad Bilateral Analog Switches	'4066					✢AHC, ✓HC
10 Bit Bus Switches With Precharged Outputs for Live Insertion	'6800	✓				
18-Bit Bus-Exchange Switches With Flow-Through Pinout	'16209	✓				
20-Bit Bus Switches With Flow-Through Pinout and Level Shifting	'16210	✓		✓	✓	
24-Bit Bus-Exchange Switches	'16211	✓	✢	✢	✓	✢CBTH
	'16212	✓	✢	✓	✓	✢CBTH
	'16213	✓	✢			
12-Bit 3-to-1 Bus Selects	'16214	✓				
20-Bit FET Bus Switches With Precharged Outputs	'16215				✢	
Synchronous 16-Bit-to-32-Bit FET Multiplexers	'16232	✓				
16-Bit-to-32-Bit FET Multiplexers/Demultiplexers	'16233	✓				
	'16235				✢	
20-Bit Bus Switches With Flow-Through Pinout and Level Shifting	'16240			✢		
16-Bit Bus Switches	'16244	✓*				

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BUS SWITCHES

Bus Switches (continued)

DESCRIPTION	TYPE	TECHNOLOGY				
		CBT	CBTS	CBTD	CBTLV	OTHER
12-Bit 1-to-2 FET Multiplexers/Demultiplexers	'16292	✓			+	
	'162292	✓			+	
16-Bit 1-to-2 Bus Switches	'16390	+			+	
20-Bit FET Bus Switches With Precharged Outputs	'16800				+	

COUNTERS

Synchronous Counters - Positive Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY									
			ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT
4 Bit Decade Up/Down	Sync	'568	✓									
4 Bit Binary	Sync	'161	✓	✓	✓	✓					✓	
		'163	✓	✓	✓	✓	✓	✶			✓	
		'561	✓									
4 Bit Binary Up/Down	Sync	'93				✓						
		'169	✓	✓	✓	✓	✓					
		'569	✓									
		'191	✓			✓		✶			✓	
		'193	✓			✓		✓			✓	
8 Bit Up/Down	Sync	'697				✓						
	Sync Clear	'869	✓	✓								
	Async Clear	'867	✓	✓								

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Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY									
			ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT
Dual 4 Bit Binary	None	'390				✓						
		'393				✓		✶			✓	
12 Bit Binary	Async	'4040							+		✓	
14 Bit Binary	Async	'4020									✓	
		'4060									✓	

Other Counters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY									
			ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT
4 Bit Up/Down	3S	'669				✓						
Binary With Input Register	3S	'592				✓						
Decade	3S	'90				✓		✶				
Divide By 12	3S	'92				✓		✶				
16 Bit Programmable	3S	'294				✓						
31 Bit Programmable	3S	'292				✓						
Parallel Register Outputs	3S	'590				✓					✓	
Parallel Register Inputs	3S	'593				✓						

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Shift Registers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY										
				LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	LV
Octal Storage Registers	8		'396					✓						
Octal Serial In With Output Storage Latches	8		'596					✓						
Parallel In, Parallel Out, Bidirectional	4		'194			✓		✓	✓					
	8		'299		✓		✓	✓	✓					
			'323		✓			✓						
Parallel In, Parallel Out	4		'195					✓	✓	✶				
Serial In, Parallel Out	8		'164		✓			✓		✶			✓	✓
Parallel In, Serial Out	8		'165		✓			✓					✓	
			'166		✓			✓		✶			✓	
Serial In, Parallel Out With Input Latches	8		'597					✓						
	8		'598					✓						
Serial In, Parallel Out With Output Latches	8	3S	'594					✓			✛	✛	✓	
			'595					✓			✛	✛	✓	
	8		'599					✓						
Noninverting	8	3S	'299		✓		✓	✓	✓					
	9	3S	'29823	✓	✶									
16 Bit Serial In With Output Storage Registers	16		'673					✓						
16 Bit Serial Out	16		'674					✓						

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ENCODERS, DATA SELECTORS/MULTIPLEXERS, AND BUS EXCHANGERS

Encoders, Data Selectors/Multiplexers, and Bus Exchangers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY															
			ABT	ALS	ALVT	AS	F	LS	S	TTL	ACT	AHC	AHCT	ALVC	HC	HCT	LVC	OTHER
Data Selectors/Multiplexers		'150								✓								
Triple 2-to-1 Analog Multiplexers/Demultiplexers	Analog	'4053										✛						
Quad 2-to-1		'157		✓		✓	✓	✓	✓	✓		✓	✓		✓	✓	✓	
		'158		✓		✓	✓	✓	✓			✓	✓				✛	
		'298				✓		✓		✶								
	3S	'257		✓		✓	✓	✓	✓		•	✛	✛		✓	✓	✓	
		'258		✓		✓	✓	✓	✶			✛	✛				✛	
Quad 2-Input Multiplexers		'399						✓										
Hex 2-to-1	3S	'857		✓														
Dual 4-to-1		'153		✓		✓	✓	✓	✓	✶					✓			
	3S	'253		✓		✓	✓	✓							✓			
		'353				✓												
4-to-1 Registered Transceivers	3S	'16460	✓															
Cascadable Octals		'148						✓		✓					✓			
8-to-1		'151		✓		✓	✓	✓	✓						✓			
	3S	'251		✓			✓	✓	✓	✶					✓			
8-to-1 Analog Multiplexers/Demultiplexers	Analog	'4051										✛						
8-to-3 Line Encoders		'348						✓										
9-Bit 4-Port Universal Bus Exchangers		'16409	✓											✓				
12-to-24 Multiplexed	3S	'16260			✛									✓				
12-to-24 Registered Bus Exchangers	3S	'16269												✓				✓ALVCHR
		'16270												✓				
12-to-24 Multiplexed Bus Exchangers	3S	'16271												✛				
		'16272												✛				
16-to-1	3S	'250				✓												

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ENCODERS, DATA SELECTORS/MULTIPLEXERS, AND BUS EXCHANGERS

Encoders, Data Selectors/Multiplexers, and Bus Exchangers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY															
			ABT	ALS	ALVT	AS	F	LS	S	TTL	ACT	AHC	AHCT	ALVC	HC	HCT	LVC	OTHER
18-to-36 Registered Bus Exchangers		'16282												✓				
18-to-36 Registered Bus Exchangers With Series Resistors		'162282												✓				
32-to-16 VL Bus Multiplexers		'16254									✓							

DECODERS/DEMULTIPLEXERS AND OSCILLATORS

Decoders/Demultiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY													
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC	OTHER
Dual 2-to-4		'139	✓			✓	✓		•	•	✓	✓	✓	✓		✓	
	OC	'156	✓			✓		✓									
3-to-8		'138	✓	✓	✓	✓	✓		•		✓	✓	✓	✓	✓	✓	
3-to-8 With Address Registers		'137	✓	✓		✓										✢	
4-to-10 BCD-to-Decimal		'42				✓							✓				

Oscillators

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY	
			LS	S
Voltage Controlled	2S	'124		✓
		'624	✓	
		'628	✓	
		'629	✓	
Crystal Controlled	2S	'321	✓	

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COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

INPUT	DESCRIPTION							TYPE	TECHNOLOGY					
	P=Q	$\overline{P=Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	ENABLE		ALS	AS	F	LS	S	HC
4 Bit Binary	No	Yes	No	No	No	2S	Yes	'85				✓	✓	
8 Bit With 20-kΩ Pullup	No	Yes	No	No	No	2S	Yes	'520	✓					
	No	Yes	No	Yes	No	2S	No	'682				✓		✓
8 Bit Standard	No	Yes	No	No	No	2S	Yes	'521	✓		✓			
	No	Yes	No	Yes	No	2S	No	'684				✓		✓
	No	Yes	No	No	No	2S	Yes	'686				✓		
	No	Yes	No	No	No	2S	Yes	'688	✓			✓		✓
8 Bit Latched P	No	No	Yes	No	Yes	2S	Yes	'885		✓				

Parity Generators/Checkers

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY						
			ALS	AS	F	LS	S	ACT	
Odd/Even	9	'280	✓	✓	✓	✓	✓		
		'286		✓				•	

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+ New product planned in technology indicated

ARITHMETIC CIRCUITS

Adders

DESCRIPTION	TYPE	TECHNOLOGY		
		F	LS	S
4 Bit	'283	✓	✓	✓

Arithmetic Logic Units

DESCRIPTION	TYPE	TECHNOLOGY		
		AS	LS	S
4 Bit	'181	✓	✶	✶
	'381			✓
	'382		✓	

Dividers/Multipliers

DESCRIPTION	TYPE	TECHNOLOGY	
		LS	TTL
Binary Rate Multipliers	'97		✓
Digital Phase Lock Loop	'297	✓	

Monostable Multivibrators

DESCRIPTION	TYPE	TECHNOLOGY			
		LS	TTL	AHC	AHCT
1 Shot	'121		✓		
1-Shot Multivibrators	'122	✓			
Dual	'123	✓		✢	✢
	'221	✓			
Retriggerable	'423	✓			

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GATES

Positive-AND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY													
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Single 2 Input		'1G08									✓	✓	✢				✢
Quad 2 Input	OC	'09	✓			✓	✓										
		'7001												✓			
Dual 4 Input		'21	✓	✓	✓	✓								✓			
Triple 3 Input		'11	✓	✓	✓	✓	✓		✓	✓				✓			
Quad 2 Input		'08	✓	✓	✓	✓	✓		✓•	✓•	✓	✓	✢	✓	✓	✓	✓
		'1008		✓													
Hex 2 Input		'808		✓													
		'1808		✓													

Positive-NAND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY													
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Single 2 Input		'1G00									✓	✓	✢				✢
8 Input		'30	✓	✓	✓	✓	✓	✓									
13 Input		'133	✓				✓										
Dual 4 Input		'20	✓	✓	✓	✓	✓							✓			
Triple 3 Input		'10	✓	✓	✓	✓	✓		✓	✓			✢	✓			✓
Quad 2 Input		'00	✓	✓	✓	✓	✓	✓	✓•	✓*	✓	✓	✢	✓	✓	✓	✓
	OC	'01				✓											
		'03	✓			✓	✶							✓			
	3S	'26				✓											
		'37	✓			✓	✓	✓									
	OC	'38	✓		✓	✓	✓	✓									
		'1000		✓													
Quad 2 Input With Schmitt Trigger		'132				✓	✓	✓			✢	✢		✓			
Hex 2 Input		'804	✓	✓													
		'1804		✓													

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Positive-OR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY																
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Single 2 Input		'1G32									✓	✓	✢				✢
Quad 2 Input		'32	✓	✓	✓	✓	✓	✓	✓•	✓•*	✓	✓	✓	✓	✓	✓	✓
		'1032		✓													
	3S	'7032												✓			
Hex 2 Input		'832	✓	✓													
		'1832		✓													

Positive-NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY														
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Single 2 Input		'1G02									✓	✓				✢
Dual 5 Input		'260			✓		✓									
Triple 3 Input		'27	✓	✓	✓	✓		✶					✓			
Quad 2 Input		'02	✓	✓	✓	✓	✓	✶			✓	✓	✓	✓	✓	✓
	OC	'33	✶			✓										
		'7002											✓			
Hex 2 Input		'805	✓	✓												
		'1805		✓												

XOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY													
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Single 2 Input		'1G86									✓	✓				✢
Quad 2 Input		'86	✓		✓	✓	✶	✶	✓•	✓	✓	✓	✓			✓
	OC	'136				✓										

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XNOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY														
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC	
Quad 2 Input	OD	'266				✓							✓				

AND/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY														
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC	
Dual 3 Input		'51				✓	✓										

OC = open collector OD = open drain 3S = 3-state
✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated
★ Product available as a military device only * Product planned as a military device

HEX INVERTERS/NONINVERTERS AND DELAY ELEMENTS

Hex Inverters/Noninverters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY														
			ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Hex Inverters		'04	✓	✓	✓	✓	✓	✓	✓•	✓•	✓	✓	+	✓	✓	✓	✓
		'U04									✓			✓		✓	✓
		'1G04									✓	✓	+				+
		'1GU04									✓						
	OC	'05	✓			✓	✓	✓			+	+		✓			
		'1G05															+
		'06				✓		✓									✓
		'16						✓									
		'1004	✓	✓													
		'1005	✓														
Hex Inverters With Schmitt Trigger		'14				✓		✓	✓	✓*	✓	✓	+	✓		✓	✓
		'1G14									✓	✓	+				+
		'19				✓											
Hex Noninverters	OC	'07				✓		✓									✓*
		'17						✓									
	OC	'35	✓														
		'128						✓									
		'140					✓										
		'1034	✓	✓													
	OC	'1035	✓														

Delay Elements

DESCRIPTION	TYPE	TECHNOLOGY													
		ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Hex	'31				✓										

OC = open collector OD = open drain 3S = 3-state

✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

IEEE 1149.1 (JTAG) Widebus™ With Dual-Sided Terminals

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				ABT	BCT	LVT	ACT	OTHER
Noninverting Transceivers	18	3S	'18245	✓				
Inverting Transceivers	18	3S	'18640	✓				
UBT	18	3S	'18512			✓		✓ Bus Hold
			'18516			✛		✛ Bus Hold
	20	3S	'18514			✓		✓ Bus Hold
UBT With Series Resistors on B Port	18	3S	'182512			✓		✓ Bus Hold
			'182516			✛		✛ Bus Hold
	20	3S	'182514			✛		✛ Bus Hold

IEEE 1149.1 (JTAG) Widebus™ With Quad-Sided Terminals

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				ABT	BCT	LVT	ACT	OTHER
Registered Transceivers	18	3S	'18646	✓		✓		✓ Bus Hold
			'18652	✓		✓		✓ Bus Hold
Registered Transceivers With Series Resistors on B Port	18	3S	'182646	✓		✓		✓ Bus Hold
			'182652	✓		✓		✓ Bus Hold
UBT	18	3S	'18502	✓		✓		✓ Bus Hold
	20	3S	'18504	✓		✓		✓ Bus Hold
UBT With Series Resistors on B Port	18	3S	'182502	✓		✓		✓ Bus Hold
	20	3S	'182504	✓		✓		✓ Bus Hold

OC = open collector OD = open drain 3S = 3-state
✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✛ New product planned in technology indicated
✶ Product available as a military device only * Product planned as a military device

IEEE 1149.1 (JTAG) Octal Bus Interface

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				ABT	BCT	LVT	ACT	OTHER
Inverting Buffers/Drivers	8	3S	'8240		✓			
Noninverting Buffers/Drivers	8	3S	'8244		✓			
Transceivers	8	3S	'8245	✓	✓			
Registered Transceivers	8	3S	'8543	✓				
			'8646	✓				
			'8652	✓				
			'8952	✓				
D-Type Transparent Latches	8	3S	'8373		✓			
D-Type Flip-Flops	8	3S	'8374		✓			

IEEE 1149.1 (JTAG) Scan Support

DESCRIPTION	TYPE	TECHNOLOGY				
		ABT	BCT	LVT	ACT	OTHER
Test Bus Controllers	'8980			✓		
	'8990				✓	
Digital Bus Monitors	'8994				✓	
Addressable Scan Port Devices	'8996	✓		✢		
Scan-Path Linkers	'8997				✓	
Scan-Path Selectors	'8999				✓	

OC = open collector OD = open drain 3S = 3-state

✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✢ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

FIFO MEMORIES

First-In, First-Out (FIFO) Memories

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY					
SIZE	TYPE			ABT	ALS	LS	S	ACT	ALVC
16 × 4 Bits	U	3S	'224			✓			
			'232		✓				
16 × 5 Bits	U	3S	'225				✓		
			'233		✓				
64 × 4 Bits	U		'236		✓				
64 × 18 Bits	U, C	3S	'7813					✓	✓
	U	3S	'7814					✓	✓
64 × 36 Bits	B, C	3S	'3612	✓					
			'3614	✓					
	U, C	3S	'3611	✓					
			'3613	✓					
Dual 64 × 1	C	3S	'2226					✓	
			'2227					✓	
Dual 256 × 1	C	3S	'2228					✓	
			'2229					✓	
256 × 18 Bits	U, C	3S	'7805					✓	✓
	U	3S	'7806					✓	✓
256 × 36 × 2 Bits	B, C	3S	'3622					✓	
512 × 18 Bits	U, C	3S	'7803					✓	✓
	U	3S	'7804					✓	✓
	B, C	3S	'7819	✓					
	B	3S	'7820	✓					
512 × 32 Bits	B, C	3S	'3638					✓	
512 × 36 Bits	U, C	3S	'3631					✓	
	B, C	3S	'3632					✓*	
1K × 9 Bits	B	3S	'2235					✓	

OC = open collector OD = open drain 3S = 3-state
✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated
★ Product available as a military device only * Product planned as a military device

U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized

First-In, First-Out (FIFO) Memories (continued)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY					
SIZE	TYPE			ABT	ALS	LS	S	ACT	ALVC
1K × 18 Bits	U, C	3S	'7811					✓	
			'7881					✓	
	U	3S	'7802					✓	
1K × 36 Bits	U, C	3S	'3641					✓	
2K × 9 Bits	U, C	3S	'7807					✓	
	U	3S	'7808					✓	
2K × 18 Bits	C	3S	'7882					✓	
2K × 36 Bits	U, C	3S	'3651					✓	

OC = open collector OD = open drain 3S = 3-state

✓ Product available in technology indicated • Product available in reduced-noise advanced CMOS (11000 series) ✛ New product planned in technology indicated

✶ Product available as a military device only * Product planned as a military device

U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized

LOGIC OVERVIEW 1

FUNCTIONAL INDEX 2

FUNCTIONAL CROSS-REFERENCE 3

DEVICE SELECTION GUIDE 4

SECTION 3
FUNCTIONAL CROSS-REFERENCE

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'1G00														✓	✓	✛				✛	
'1G02														✓	✓						✛	
'1G04														✓	✓	✛					✛	
'1GU04														✓								
'1G05																					✛	
'1G08														✓	✓	✛					✛	
'1G14														✓	✓	✛					✛	
'1G32														✓	✓	✛					✛	
'1G79																✛					✛	
'1G86														✓	✓						✛	
'1G125														✛	✛	✛					✛	✓CBT ✓CBTLV
'1G126														✛	✛	✛					✛	
'1G384																						✛CBT,D,S
'00						✓	✓	✓	✓	✓	✓	✓•	✓*	✓	✓	✛	✓	✓	✓	✓	✓	
'01									✓		✶											
'02						✓	✓	✓	✓	✓	✶			✓	✓		✓	✓	✓	✓	✓	
'03						✓			✓	✶							✓					
'04						✓	✓	✓	✓	✓	✓	✓•	✓•	✓	✓	✓	✓	✓	✓	✓	✓	
'U04														✓			✓		✓	✓	✓	
'05						✓			✓	✓	✓			✛			✓					
'06									✓		✓										✓	
'07									✓		✓										✓	
'08						✓	✓	✓	✓	✓		✓•	✓•	✓	✓	✛	✓	✓	✓	✓	✓	
'09						✓			✓	✓												
'10						✓	✓	✓	✓	✓		✓	✓			✛	✓			✓	✓	
'11						✓	✓	✓	✓	✓		✓	✓				✓					
'14									✓		✓	✓	✓*	✓	✓	✛	✓	✶	✓	✓	✓	
'16											✓											
'17											✓											
'19									✓													

✓ Product available in technology indicated
✶ Product available as a military device only
• Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✛ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'20						✓	✓	✓	✓	✓							✓				
'21						✓	✓	✓	✓								✓				
'26									✓												
'27						✓	✓	✓	✓		✶						✓				
'30						✓	✓	✓	✓	✓	✓										
'31									✓												
'32						✓	✓	✓	✓	✓	✓	✓•	✓•	✓	✓	✢	✓	✓	✓	✓	
'33						✶			✓												
'35						✓															
'37						✓				✓	✓										
'38						✓		✓	✓	✓	✓										
'42									✓								✓				
'45											✓										
'47									✓		✓										
'51									✓	✓	✶										
'73									✓												
'74						✓	✓	✓	✓	✓	✓	✓•	✓•	✓	✓	✢	✓	✓	✓	✓	
'75									✓												
'85									✓	✓											
'86						✓	✶	✓	✓	✶	✶	✓•	✓	✓	✓		✓			✓	
'90									✓		✶										
'92									✓		✶										
'93									✓												
'97											✓										
'107									✓		✶										
'109						✓	✓	✓	✓								✓				
'112						✓		✓	✓	✓							✓			✓	
'121											✓										
'122									✓		✶										
'123									✓		✓			✢	✢						

✓ Product available in technology indicated
✶ Product available as a military device only
• Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✢ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'124										✓											
'125	✓			✓	✓			✓	✓					✓	✓*	✛	✓	✓	✓	✓	
'126	✓			✓				✓	✓		✶			✓*	✓*	✛	✓		✓	✓	
'128											✓										
'132									✓	✓	✓			✛	✛		✓				
'133						✓				✓											
'136									✓												
'137						✓	✓		✓											✛	
'138						✓	✓	✓	✓	✓		•		✓	✓			✓	✓	✓	
'139						✓			✓	✓		•	•	✓	✓		✓	✓		✓	
'140										✓											
'145									✓		✓										
'148									✓		✓						✓				
'150											✓										
'151						✓	✓	✓	✓	✓							✓				
'153						✓	✓	✓	✓	✓	✶						✓				
'154											✓										
'155									✓		✶										
'156						✓			✓		✓										
'157						✓	✓	✓	✓	✓	✓			✓	✓		✓	✓		✓	
'158						✓	✓	✓	✓	✓				✓	✓					✛	
'159											✓										
'161						✓	✓	✓	✓								✓				
'163						✓	✓	✓	✓	✓	✶						✓				
'164						✓			✓		✶						✓		✓		
'165						✓			✓								✓		✓		
'166						✓			✓		✶						✓				
'169						✓	✓	✓	✓	✓											
'173									✓		✶										
'174						✓	✓	✓	✓	✓				✛	✛		✓		✓		

✓ Product available in technology indicated
✶ Product available as a military device only
● Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✛ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'175						✓	✓	✓	✓	✓	✓						✓				
'181							✓		✶	✶											
'191						✓			✓		✶						✓				
'193						✓			✓		✓						✓				
'194							✓		✓	✓											
'195									✓	✓	✶						✶				
'221									✓		✶										
'224									✓												See FIFO
'230							✓														
'232						✓															See FIFO
'233						✓															See FIFO
'236						✓															See FIFO
'240	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓	✓		✓	✓	✓	✓	
'241	✓			✓	✓	✓	✓	✓	✓	✓		✓	✓				✓			✢	
'243						✓		✓	✓												
'244	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓*	✓	✓	✓	✓	✓	✓	
'245	✓			✓	✓	✓	✓	✓	✓			✓•*	✓•*	✓*	✓	✢	✓	✓	✓	✓	
'247									✓												
'250							✓														
'251						✓		✓	✓	✓	✶						✓				
'253						✓	✓	✓	✓								✓				
'257						✓	✓	✓	✓	✓			•	✢	✢		✓	✓		✓	
'258						✓	✓	✓	✓					✢	✢						✢
'259						✓			✓								✓				
'260								✓		✓											
'266									✓								✓				
'273	✓					✓			✓					✓	✢		✓	✓	✓		
'276											✓										
'279									✓		✶										
'280						✓	✓	✓	✓	✓											

✓ Product available in technology indicated
✶ Product available as a military device only
• Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✢ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'283								✓	✓	✓											
'286							✓						•								
'292									✓												
'294									✓												
'297									✓												
'298							✓		✓		✶										
'299						✓		✓	✓	✓											
'321									✓												
'323						✓			✓												
'348									✓												
'353							✓														
'365									✓		✶						✓				
'367									✓		✓			÷	÷		✓				
'368									✓		✓						✓				
'373	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓*	✓*	÷	✓	✓	✓	✓	
'374	✓			✓	✓	✓	✓	✓	✓	✓		✓•	✓•	✓*	✓*	÷	✓	✓	✓	✓	
'375									✓												
'376											✓										
'377	✓							✓	✓								✓	✓			
'378									✓												
'379									✓												
'381										✓											
'382									✓												
'390									✓												
'393									✓		✶						✓				
'396									✓												
'399									✓												
'423									✓												
'442									✓												
'465									✓												

✓ Product available in technology indicated
✶ Product available as a military device only
• Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
÷ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'466									✓												
'520						✓															
'521						✓		✓													
'533	✓					✓	✓					✓	✓								
'534	✓					✓						✓	✓				✓				
'540	✓			✓		✓			✓					✓*	✓*		✓	✓		✓	
'541	✓			✓		✓		✓	✓					✓*	✓*		✓	✓		✓	
'543	✓			✓	✓			✓					•							✓	
'544																				✢	
'561						✓															
'563						✓						✓	✓				✓				
'564						✓						✓	✓								
'568						✓															
'569						✓															
'573	✓			✶	✓	✓	✓	✓				✓	✓	✓*	✓*		✓	✓	✓	✓	
'574	✓			✓	✓	✓	✓	✓				✓	✓	✓*	✓*		✓	✓	✓	✓	
'575						✓	✓														
'576						✓	✓														
'577						✓															
'580						✓															
'590									✓								✓				
'592									✓												
'593									✓												
'594									✓					✢	✢		✓				
'595									✓					✢	✢		✓				
'596									✓												
'597									✓												
'598									✓												
'599									✓												
'620	✓			✶		✓															

✓ Product available in technology indicated
✶ Product available as a military device only
• Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✢ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'621						✓		✶													
'623	✓			✓		✓		✓	✓								✓	✓			
'624									✓												
'628									✓												
'629									✓												
'638						✓															
'639						✓	✓														
'640	✓			✓		✓	✓		✓								✓				
'641						✓	✓		✓												
'642						✓			✓												
'645						✓	✓		✓								✓	✓			
'646	✓			✓	✓	✓	✓		✓								✓	✓			✓
'647									✓												
'648						✓	✓		✓												
'651	✓					✓	✓														
'652	✓			✓	✓	✓	✓		✓			•	•				✓	✓		✓	
'653						✓															
'654						✓															
'656													•								
'657	✓																				
'666						✓															
'667						✓															
'669									✓												
'670									✓												
'673									✓												
'674									✓												
'682									✓								✓				
'684									✓								✓				
'686									✓												
'688						✓			✓								✓				

✓ Product available in technology indicated
✶ Product available as a military device only
● Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✢ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'697									✓												
'756				✓			✓														
'757							✓														
'760				✓		✓	✓														
'804						✓	✓														
'805						✓	✓														
'808							✓														
'821	✓						✓													✓	
'823	✓						✓													✓	
'825							✓														
'827	✓																			✓	
'828																				✓	
'832						✓	✓														
'833	✓																				
'841	✓					✓														✓	
'842						✓															
'843	✓					✓														✛	
'845						✓															
'853	✓																				
'857						✓															
'861	✓																			✓	
'863	✓																			✓	
'867						✓	✓														
'869						✓	✓														
'870						✓															
'873						✓	✓														
'874						✓	✓														
'876						✓	✓														
'885							✓														
'990						✓															

✓ Product available in technology indicated
✶ Product available as a military device only
● Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✛ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'992						✓															
'994						✓															
'996						✓															
'1000							✓														
'1004						✓	✓														
'1005						✓															
'1008							✓														
'1016								✓													
'1032							✓														
'1034						✓	✓														
'1035						✓															
'1050										✓											
'1051										✓											
'1052										✓											
'1053										✓											
'1056								✓		✓											
'1071													✓								
'1073													✓								
'1244						✓															
'1245						✓															
'1284													✓								
'1640						✓															
'1645						✓															
'1650																					✓FB+
'1651																					✓FB+
'1653																					✓FB+
'1655																					✓GTL
'1804							✓														
'1805							✓														
'1808							✓														

✓ Product available in technology indicated
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✢ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR					CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'1832							✓														
'2031																					✓FB+
'2032																					✓FB+
'2033																					✓FB+
'2040																					✓FB+
'2041																					✓FB+
'2226													✓								See FIFO
'2227													✓								See FIFO
'2228													✓								See FIFO
'2229													✓								See FIFO
'2235													✓								See FIFO
'2240	✓			✓		✓															
'2241	✓																				
'2244	✓			✓				✓												✓	
'2245				✓	✓			✓												+	✓ABTR ✓LVCR +LVTR
'2373								✓													
'2541						✓															
'2827	✓			✓																	
'2828				✓																	
'2952	✓				✓															✓	
'2953				✓																	
'3125																					✓CBT +CBTLV
'3126																					✓CBT +CBTLV
'3244																					✓CBT
'3245																					✓CBT +CBTLV ✓LVCC

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DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'3251																					✓CBT ✛CBTLV
'3253																					✓CBT ✛CBTLV
'3257																					✓CBT ✛CBTLV
'3306																					✓CBT,D,S
'3345																					✓CBT
'3383																					✓CBT ✛CBTLV
'3384																					✓CBT,D,S ✛CBTLV
'3386																					✛CBT
'3611	✓																				See FIFO
'3612	✓																				See FIFO
'3613	✓																				See FIFO
'3614	✓																				See FIFO
'3622													✓								See FIFO
'3631													✓								See FIFO
'3632													✓*								See FIFO
'3638													✓								See FIFO
'3641													✓*								See FIFO
'3861																					✛CBT,D ✛CBTLV
'4020																	✓				
'4040														✛			✓				
'4051														✛							
'4053														✛							
'4060																	✓				
'4066														✛			✓				
'4245																				✓	✓LVCC
'4374							✓														

✓ Product available in technology indicated
✶ Product available as a military device only
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DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'5400	✓																				
'5401	✓																				
'5402	✓																				
'5403	✓																				
'6800																					✓CBT
'7001																	✓				
'7002																	✓				
'7032																	✓				
'7802													✓								See FIFO
'7803													✓			✓					See FIFO
'7804													✓			✓					See FIFO
'7805													✓			✓					See FIFO
'7806													✓			✓					See FIFO
'7807													✓								See FIFO
'7808													✓								See FIFO
'7811													✓								See FIFO
'7813													✓			✓					See FIFO
'7814													✓			✓					See FIFO
'7819	✓																				See FIFO
'7820	✓																				See FIFO
'7881													✓								See FIFO
'7882													✓								See FIFO
'8240				✓																	
'8244				✓																	
'8245	✓			✓																	See JTAG
'8373				✓																	
'8374				✓																	
'8543	✓																				See JTAG
'8646	✓																				See JTAG
'8652	✓																				See JTAG

✓ Product available in technology indicated
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DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'8952	✓																				See JTAG
'8980					✓																See JTAG
'8990													✓								See JTAG
'8994													✓								See JTAG
'8996	✓				✢																See JTAG
'8997													✓								See JTAG
'8999													✓								See JTAG
'11000												✓									
'11004												✓	✓								
'11008												✓	✓								
'11032												✓	✓								
'11074												✓	✓								
'11086												✓									
'11138												✓									
'11139												✓	✓								
'11240												✓	✓								
'11244												✓	✓								
'11245												✓	✓								
'11257												✓	✓								
'11286													✓								
'11373												✓	✓								
'11374												✓	✓								
'11652												✓	✓								
'16209																					✓CBT
'16210																					✓CBT,D ✓CBTLV
'16211																					✓CBT,D,S,H ✓CBTLV
'16212																					✓CBT,S ✓CBTLV
'16213																					✓CBT,S

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DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'16214																					✓CBT
'16215																					✛CBTLV
'16232																					✓CBT
'16233																					✓CBT
'16235																					✛CBTLV
'16240	✓		✛		✓							✓	✓	✓	✓	✓				✓	
'16241	✓				✓								✓							✛	
'16244	✓	✓	✛		✓							✓	✓	✓	✓	✓				✓	✓*CBT
'16245	✓	✓	✛		✓							✓	✓	✓	✓	✓				✓	✓ABTE
'16246																					✓ABTE
'16254													✓								
'16260	✓		✛									✓				✓					
'16269																✓					
'16270																✓					
'16271																✓					
'16282																✓					
'16292																					✛CBT ✛CBTLV
'16334																✓					
'16344																✓					
'16373	✓		✛		✓							✓	✓	✓	✓	✓				✓	
'16374	✓		✛		✓							✓	✓	✓	✓	✓				✓	
'16390																					✛CBT ✛CBTLV
'16409																✓					
'16460	✓																				
'16470	✓												✓								
'16472												✓									
'16474													✓								
'16475													✓								
'16500	✓				✓											✓					

✓ Product available in technology indicated
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DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'16501	✓		✢		✓											✓					
'16524																✓					
'16525																✓					
'16540	✓												✓	✓	✓					✓	
'16541	✓				✢								✓	✓	✓					✓	
'16543	✓		✢		✓							✓	✓			✓				✓	
'16544													✓								
'16600	✓															✓					
'16601	✓		✢													✓					
'16612																					✓GTL
'16616																					✓GTL
'16620												✓	✓								
'16622																					✓GTL
'16623	✓												✓								
'16640	✓											✓	✓								
'16646	✓				✓							✓	✓							✓	
'16648													✓								
'16651													✓								
'16652	✓		✢		✓							✓	✓							✓	
'16657	✓												✓								
'16721																✓					
'16800																					✓CBTLV
'16820																✓					
'16821	✓		✢										✓			✓					
'16823	✓											✓	✓			✓					
'16825	✓												✓			✓					
'16827	✓		✢										✓			✓					
'16831																✓					
'16832																✓					
'16833	✓												✓								

✓ Product available in technology indicated
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* Product planned as a military device
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DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'16834																+					
'16835					✓											✓					
'16837																					✓SSTL
'16841	✓												✓			✓					
'16843	✓																				
'16847																					+SSTL
'16853	✓																				
'16857																					+SSTL
'16861													✓								
'16863	✓												✓			✓					
'16864													✓								
'16901																✓					
'16923																					✓GTL
'16952	✓				✓*								✓			✓				✓	
'18245	✓																				See JTAG
'18502	✓				✓																See JTAG
'18504	✓				✓																See JTAG
'18512					✓																See JTAG
'18514					✓																See JTAG
'18516					+																See JTAG
'18640	✓																				See JTAG
'18646	✓				✓																See JTAG
'18652	✓				✓																See JTAG
'25245	✓			✓																	
'29821				✓		✓															
'29823				✓		✶															
'29827				✓		✓															
'29828						✓															
'29833						✓															
'29834				✓																	

✓ Product available in technology indicated
✶ Product available as a military device only
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* Product planned as a military device
+ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS								OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'29841				✓		✓															
'29843				✓																	
'29854				✓																	
'29863				✓		✓															
'32245	✓																				
'32316	✓																				
'32318	✓																				
'32501	✓																				
'32543	✓																				
'161284																				✓	See JTAG
'162240					✓											✓					
'162241					✓																
'162244	✓		✦		✓											✓				✓	✓LVCR
'162245	✓		✦		✓															✓	
'162260	✓															✓					
'162268																✓					
'162269																✓					✓ALVCHR
'162280																✓					
'162292																					✓CBT ✦CBTLV
'162334																✓					
'162344																✓					
'162373					✦																
'162374					✓											✓					
'162409																✓					
'162460	✓																				
'162500	✓																				
'162501	✓																				
'162525																✓					
'162541					✓																
'162601	✓															✓					

✓ Product available in technology indicated
✶ Product available as a military device only
● Product available in reduced-noise advanced CMOS (11000 series)
* Product planned as a military device
✦ New product planned in technology indicated

DEVICE	BiCMOS					BIPOLAR						CMOS							OTHER
	ABT	ALB	ALVT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	
'162721																✓					
'162820																✓					
'162822																					✓HSTL
'162823	✓																				
'162825	✓																				
'162827	✓															✓					
'162830																✓					✓ALVCHS
'162831																✓					
'162832																✓					
'162835																✓					
'162836																✓					
'162841	✓												✢			✓					
'164245																✓					
'182502	✓				✓																See JTAG
'182504	✓				✓																See JTAG
'182512					✓																See JTAG
'182514					✢																See JTAG
'182516					✢																See JTAG
'182646	✓				✓																See JTAG
'182652	✓				✓																See JTAG

✓ Product available in technology indicated
✶ Product available as a military device only
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✢ New product planned in technology indicated

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SECTION 4
DEVICE SELECTION GUIDE

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Refer to the following for MIL column entries:

military package description and availability

CDIP (ceramic dual-in-line package)
J = 14/16/20 pins
JT = 24/28 pins

CFP (ceramic flat package)
WA = 14 pins (small outline)
W = 14/16/20 pins
WD = 48/56 pins

CPGA (ceramic pin grid array)
GB = 68/84/120 pins

CQFP (ceramic quad flat package)
HV = 68 pins
HT = 84 pins
HS = 100 pins
HFP = 132 pins

LCCC (leadless ceramic chip carrier)
FK = 20/28 pins

schedule

✓ = Now
✢ = Planned
★ = Please see the corresponding device data sheet for correct military nomenclature or visit http://www.ti.com/sc/docs/military for TI military product information.

ABT
Advanced BiCMOS Technology

The ABT family is TI's second-generation family of BiCMOS bus-interface products. It is manufactured using the latest 0.8-μ BiCMOS process and provides high drive up to 64 mA and propagation delays below the 5-ns range, while maintaining very low power consumption. ABT products are well suited for live-insertion applications with an I_{off} specification of 0.1 mA.

To reduce transmission-line effects, the ABT family has series-damping resistor options. Furthermore, there are special ABT parts that provide extremely high-current drive (180 mA) to transmit down to 25-Ω transmission lines. Advanced bus functions, such as universal bus transceivers (UBT™) emulate a wide variety of bus-interface functions. Multiplexing options for memory interleaving and bus upsizing or downsizing also are provided.

The ABT devices can be purchased in octal, Widebus™, or Widebus+™. The Widebus and Widebus+ packages feature higher performance with reduced noise and flow-through pinout for easier board layout. In addition, the Widebus+ devices have bus-hold circuitry on the inputs to eliminate the need for external pullup resistors for floating inputs.

For ABT data sheets, see the 1997 *ABT Logic Advanced BiCMOS Technology Data Book*, literature number SCBD002C.

DEVICE SELECTION GUIDE

ABT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	
SN74ABT125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓	✓	✓			SCBS182E
SN74ABT126	14	Quad Bus Buffer Gate (OE)		✓	✓	✓	✓			SCBS183C
SN74ABT240A	20	Octal Buffer/Driver	★	✓	✓	✓	✓			SCBS098H
SN74ABT241A	20	Octal Buffer/Driver	★	✓	✓	✓	✓			SCBS184D
SN74ABT244A	20	Octal Buffer/Driver	★	✓	✓	✓	✓	✢		SCBS099I
SN74ABT245B	20	Octal Bus Transceiver	★	✓	✓	✓	✓	✓		SCBS081H
SN74ABTH245	20	Octal Bus Transceiver	✢	✓	✓	✓	✓	✓		SCBS663C
SN74ABT273	20	Octal D-Type Flip-Flop With Clear	✓	✓	✓	✓	✓			SCBS185B
SN74ABT373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓			SCBS155D
SN74ABT374A	20	Octal D-Type Flip-Flop	★	✓	✓	✓	✓			SCBS111G
SN74ABT377A	20	Octal D-Type Flip-Flop With Clock Enable	✓	✓	✓	✓	✓			SCBS156E
SN74ABT533A	20	Octal D-Type Transparent Latch	★	✓	✓	✓	✓			SCBS186D
SN74ABT534A	20	Octal D-Type Flip-Flop	★	✓	✓	✓	✓			SCBS187F
SN74ABT540	20	Octal Buffer/Driver		✓	✓	✓				SCBS188C
SN74ABT541B	20	Octal Buffer/Driver	★	✓	✓	✓	✓			SCBS093I
SN74ABT543A	24	Octal Registered Bus Transceiver	✓	✓	✓	✓	✓			SCBS157F
SN74ABT573A	20	Octal D-Type Transparent Latch	★	✓	✓	✓	✓			SCBS190C
SN74ABT574A	20	Octal D-Type Flip-Flop	★	✓	✓	✓	✓			SCBS191C
SN74ABT620	20	Octal Bus Transceiver		✓	✓	✓				SCBS113D
SN74ABT623	20	Octal Bus Transceiver	★	✓	✓	✓	✓			SCBS114D
SN74ABT640	20	Octal Bus Transceiver		✓	✓	✓	✓			SCBS104C
SN74ABT646A	24	Octal Registered Bus Transceiver	✓	✓	✓	✓	✓	✓		SCBS069G
SN74ABT651	24	Octal Registered Bus Transceiver		✓	✓	✓				SCBS083E
SN74ABT652A	24	Octal Registered Bus Transceiver	✓	✓	✓	✓				SCBS072F
SN74ABT657A	24	Octal Parity Bus Transceiver		✓	✓	✓				SCBS192E
SN74ABT821A	24	10-Bit Bus-Interface Flip-Flop	★	✓	✓	✓				SCBS193E
SN74ABT823	24	9-Bit Bus-Interface Flip-Flop	✓	✓	✓	✓				SCBS158E
SN74ABT827	24	10-Bit Buffer/Driver	✓	✓	✓	✓	✓			SCBS159D
SN74ABT833	24	8-Bit to 9-Bit Parity Bus Transceiver		✓	✓					SCBS195C
SN74ABT841A	24	10-Bit Bus-Interface D-Type Latch	★	✓	✓	✓	✓			SCBS196D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	
SN74ABT843	24	9-Bit Bus-Interface D-Type Latch	✓	✓	✓	✓				SCBS197D
SN74ABT853	24	8-Bit to-9 Bit Parity Bus Transceiver	✓	✓	✓	✓	✓			SCBS198F
SN74ABT861	24	10-Bit Bus Transceiver		✓	✓	✢				SCBS199C
SN74ABT863	24	9-Bit Bus Transceiver		✓	✓	✓				SCBS201D
SN74ABT2240A	20	Octal Buffer and Line/MOS Driver	✓	✓	✓	✓	✓			SCBS232D
SN74ABT2241	20	Octal Buffer and Line/MOS Driver		✓	✓	✓	✓			SCBS233B
SN74ABT2244A	20	Octal Buffer and Line/MOS Driver	★	✓	✓	✓	✓			SCBS106E
SN74ABTR2245	20	Octal Transceiver and Line/MOS Driver	✓	✓	✓	✓	✓	✓		SCBS680A
SN74ABT2827	24	10-Bit Buffer/Driver With Series Resistors		✓	✓					SCBS648A
SN74ABT2952A	24	Octal Registered Bus Transceiver		✓	✓	✓				SCBS203D
SN74ABT5400A	28	11-Bit Line/Memory Driver			✓					SCBS661B
SN74ABT5401	28	11-Bit Line/Memory Driver			✓					SCBS235B
SN74ABT5402A	28	12-Bit Line/Memory Driver			✓					SCBS660B
SN74ABT5403	28	12-Bit Line/Memory Driver			✓					SCBS236B
SN74ABT16240A	48	16-Bit Buffer/Driver	✓			✓	✓	✓		SCBS095F
SN74ABT16241A	48	16-Bit Buffer/Driver	✓			✓	✓	✓		SCBS096F
SN74ABT16244A	48	16-Bit Buffer/Driver	★			✓	✓	✓		SCBS073G
SN74ABTH16244	48	16-Bit Buffer/Driver				✓	✓	✢		SCBS677C
SN74ABT16245A	48	16-Bit Bus Transceiver	★			✓	✓	✓		SCBS300C
SN74ABTH16245	48	16-Bit Bus Transceiver				✓	✓	✓		SCBS662G
SN74ABTH16260	56	12-to-24 Multiplexed D-Type Latch With Power-Up 3-State and Bus Hold				✓	✓			SCBS204C
SN74ABT16373A	48	16-Bit D-Type Transparent Latch	✓			✓	✓			SCBS160C
SN74ABT16374A	48	16-Bit D-Type Flip-Flop	✓			✓	✓			SCBS205C
SN74ABTH16460	56	4-to-1 Multiplexed/Demultiplexed Transceiver				✓	✓			SCBS207F
SN74ABT16470	56	16-Bit Registered Bus Transceiver				✓	✓			SCBS085E
SN74ABT16500B	56	18-Bit Universal Bus Transceiver				✓	✓			SCBS057G
SN74ABT16501	56	18-Bit Universal Bus Transceiver				✓	✓			SCBS086C
SN74ABT16540A	48	16-Bit Buffer/Driver				✓	✓	✓		SCBS208C
SN74ABT16541A	48	16-Bit Buffer/Driver				✓	✓	✓		SCBS118C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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SOT (small-outline transistor)
DBV = 5 pins
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SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
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QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

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D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
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schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE SELECTION GUIDE

ABT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	
SN74ABT16543	56	16-Bit Registered Bus Transceiver	✓			✓	✓			SCBS087C
SN74ABT16600	56	18-Bit Universal Bus Transceiver				✓	✓			SCBS209B
SN74ABT16601	56	18-Bit Universal Bus Transceiver	✓			✓	✓			SCBS210C
SN74ABT16623	48	16-Bit Bus Transceiver				✓	✓			SCBS211B
SN74ABT16640	48	16-Bit Bus Transceiver	✓			✓	✓			SCBS107C
SN74ABT16646	56	16-Bit Registered Bus Transceiver	✓			✓				SCBS212B
SN74ABT16652	56	16-Bit Registered Bus Transceiver	✓			✓				SCBS215B
SN74ABT16657	56	16-Bit Parity Bus Transceiver				✓	✓			SCBS103B
SN74ABT16821	56	20-Bit Bus-Interface Flip-Flop				✓	✓			SCBS216B
SN74ABT16823	56	18-Bit Bus-Interface Flip-Flop	✓			✓	✓			SCBS217C
SN74ABTH16823	56	18-Bit Bus-Interface Flip-Flop				✓	✓	✢		SCBS664B
SN74ABT16825	56	18-Bit Buffer/Driver				✓	✓			SCBS218C
SN74ABT16827	56	20-Bit Buffer/Driver				✓	✓			SCBS220C
SN74ABT16833	56	Dual 8-Bit to 9-Bit Parity Bus Transceiver				✓	✓			SCBS097D
SN74ABT16841	56	20-Bit Bus-Interface D-Type Latch	✓			✓				SCBS222C
SN74ABT16843	56	18-Bit Bus-Interface D-Type Latch				✓	✓			SCBS223E
SN74ABT16853	56	Dual 8-Bit to 9-Bit Parity Bus Transceiver				✓				SCBS153B
SN74ABT16863	48	18-Bit Bus Transceiver				✓				SCBS225C
SN74ABT16952	56	16-Bit Registered Bus Transceiver				✓	✓			SCBS082C
SN74ABTH25245	24	25-Ω Octal Bus Transceiver		✓	✓					SCBS251F
SN74ABTH32245	100	36-Bit Bus Transceiver With Bus Hold							✓	SCBS228G
SN74ABTH32316	80	16-Bit Tri-Port Universal Bus Exchanger With Clock-Enable and Bus Hold							✓	SCBS179E
SN74ABTH32318	80	18-Bit Tri-Port Universal Bus Exchanger With Bus Hold							✓	SCBS180E
SN74ABTH32501	100	36-Bit Universal Bus Transceiver							✓	SCBS229F
SN74ABTH32543	100	36-Bit Registered Bus Transceiver							✓	SCBS230F
SN74ABT162244	48	16-Bit Buffer/Driver With Series Resistors	✓			✓	✓	✓		SCBS238D
SN74ABT162245	48	16-Bit Bus Transceiver With Series Resistors	✓			✓	✓			SCBS239D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	
SN74ABTH162245	48	16-Bit Bus Transceiver With Series Resistors and Bus Hold				✓	✓	✓		SCBS712
SN74ABTH162260	56	12-to-24 Multiplexed D-Type Latch With Series Resistors				✓	✓			SCBS240D
SN74ABTH162460	56	4-to-1 Multiplexed/Demultiplexed Registered Transceiver With Series Resistors				✓	✓			SCBS241E
SN74ABT162500	56	18-Bit Universal Bus Transceiver With Series Resistors				✓				SCBS242D
SN74ABT162501	56	18-Bit Universal Bus Transceiver With Series Resistors				✓	✓			SCBS243D
SN74ABT162601	56	18-Bit Universal Bus Transceiver With Series Resistors				✓	✓			SCBS247E
SN74ABT162823A	56	18-Bit Bus-Interface Flip-Flop With Series Resistors				✓				SCBS666A
SN74ABT162825	56	18-Bit Buffer/Driver With Series Resistors				✓				SCBS474C
SN74ABT162827A	56	20-Bit Buffer/Driver With Series Resistors				✓	✓			SCBS248E
SN74ABT162841	56	20-Bit Bus-Interface D-Type Latch With Series Resistors				✓	✓			SCBS665B

commercial package description and availability

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SOIC (small-outline integrated circuit)
D = 8/14/16 pins
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TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
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MIL – See page 4–3 for military package description and availability

ABTE/ETL
Advanced BiCMOS Technology/ Enhanced Transceiver Logic

ABTE has wider noise margins and is backward compatible with existing TTL logic. ABTE devices support the VME64-ETL specification with tight tolerances on skew and transition times. ABTE is manufactured using the latest 0.8-μ BiCMOS process by providing high drive up to 90 mA. Other features include a bias pin and internal pullup resistors on control pins for maximum live-insertion protection. Bus-hold circuitry eliminates external pullup resistors on the inputs and series-damping resistors on the outputs to damp reflections.

For ABTE/ETL data sheets, see the 1997 *GTL, BTL, and ETL Logic Data Book*, literature number SCED004.

DEVICE SELECTION GUIDE

ABTE/ETL

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	SSOP	TSSOP	
SN74ABTE16245	48	16-Bit Incident-Wave Switching ETL Bus Transceiver	✓	✓	✓	SCBS226F
SN74ABTE16246	48	11-Bit Incident-Wave Switching ETL Bus-Control Transceiver With 3-State and Open-Collector Outputs		✓	✓	SCBS227E

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
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NT = 24/28 pins

PLCC (plastic leaded chip carrier)
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QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

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MIL – See page 4–3 for military package description and availability

AC/ACT
Advanced CMOS Logic

The ACL family of devices is manufactured in 1-μ CMOS and has more than 70 functions, including gates, flip-flops, drivers, counters, and transceivers. The ACL family is a reliable, low-power logic family with 24-mA output drive.

Included in the family are standard end-pin products and center-pin V_{CC} and ground-configuration products with output-edge control (OEC™) circuitry. The OEC™ circuitry, available only with the center-pin products, helps reduce simultaneous switching noise associated with high-speed logic. Included in the center-pin products are 16-, 18-, and 20-bit bus-interface functions packaged in 48- and 56-pin shrink small-outline packages (SSOP) and thin shrink small-outline packages (TSSOP). These packages allow the designer to double functionality in the same circuit board area or reduce the circuit board area by one-half.

AC devices offer CMOS-compatible inputs and ACT devices offer TTL-compatible inputs.

For AC/ACT data sheets, see the 1997 *AC/ACT CMOS Logic Data Book*, literature number SCAD001D.

DEVICE SELECTION GUIDE

AC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74AC00	14	Quad 2-Input NAND Gate	✓	✓	✓	✓	✓	SCAS524C
SN74AC04	14	Hex Inverter	✓	✓	✓	✓	✓	SCAS519C
SN74AC08	14	Quad 2-Input AND Gate	✓	✓	✓	✓	✓	SCAS536B
SN74AC10	14	Triple 3-Input NAND Gate	✓	✓	✓	✓	✓	SCAS529B
SN74AC11	14	Triple 3-Input AND Gate	✓	✓	✓	✓	✓	SCAS532B
SN74AC14	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	✓	SCAS522D
SN74AC32	14	Quad 2-Input OR Gate	✓	✓	✓	✓	✓	SCAS528B
SN74AC74	14	Dual D-Type Flip-Flop	✓	✓	✓	✓	✓	SCAS521C
SN74AC86	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓	✓	✓	SCAS533A
SN74AC240	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCAS512C
SN74AC241	20	Octal Buffer/Driver		✓	✓	✓	✓	SCAS513C
SN74AC244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCAS514C
SN74AC245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	SCAS461D
SN74AC373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCAS540B
SN74AC374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	SCAS543B
SN74AC533	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCAS555A
SN74AC534	20	Octal D-Type Flip-Flop		✓	✓	✓	✓	SCAS554A
SN74AC563	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCAS552A
SN74AC564	20	Octal D-Type Flip-Flop		✓	✓	✓	✓	SCAS551A
SN74AC573	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCAS542B
SN74AC574	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	SCAS541B
74AC11000	16	Quad 2-Input Positive-NAND Gate		✓	✓			SCLS054A
74AC11004	20	Hex Inverter		✓	✓	✓		SCAS033B
74AC11008	16	Quad 2-Input Positive-AND Gate		✓	✓		✓	SCAS014C
74AC11032	14, 16	Quad 2-Input Positive-OR Gate		✓	✓	✓		SCAS007C
74AC11074	14	Dual D-Type Flip-Flop		✓	✓		✓	SCAS499A
74AC11086	16	Quad 2-Input Exclusive-OR Gate		✓	✓			SCAS081A
74AC11138	16	3-to-8 Decoder/Demultiplexer		✓	✓		✓	SCAS042B
74AC11139	16	Dual 2-to-4 Decoder/Demultiplexer		✓	✓		✓	SCAS070B
74AC11240	24	Octal Buffer/Driver		✓	✓	✓		SCAS448A

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
74AC11244	24	Octal Buffer/Driver		✓	✓	✓	✓	SCAS171A
74AC11245	24	Octal Bus Transceiver		✓	✓	✓	✓	SCAS010B
74AC11257	20	Quad 2-to-1 Data Selector/Multiplexer				✓	✓	SCAS049B
74AC11373	24	Octal D-Type Transparent Latch		✓	✓	✓		SCAS213A
74AC11374	24	Octal D-Type Flip-Flop		✓	✓	✓		SCAS214A
74AC11520	20	8-Bit Identity Comparator		✓				SCAS025C
74AC11652	28	Octal Registered Bus Transceiver		✓	✓			SCAS088A
74AC16240	48	16-Bit Buffer/LineDriver				✓		SCAS234B
74AC16244	48	16-Bit Buffer/Driver				✓	✓	SCAS120A
74AC16245	48	16-Bit Bus Transceiver				✓	✓	SCAS235A
74AC16373	48	16-Bit D-Type Transparent Latch				✓		SCAS121B
74AC16374	48	16-Bit D-Type Flip-Flop				✓		SCAS123B
74AC16472	56	16-Bit Latched Bus Transceiver				✓		SCAS165A
74AC16543	56	16-Bit Registered Bus Transceiver				✓		SCAS125B
74AC16620	48	16-Bit Bus Transceiver				✓		SCAS239A
74AC16640	48	16-Bit Bus Transceiver				✓		SCAS240A
74AC16646	56	16-Bit Registered Bus Transceiver				✓		SCAS241A
74AC16652	56	16-Bit Registered Bus Transceiver				✓		SCAS242A
74AC16823	56	18-Bit Bus-Interface Flip-Flop				✓		SCAS243A

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE SELECTION GUIDE

ACT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74ACT00	14	Quad 2-Input NAND Gate	✓	✓	✓	✓	✓	SCAS523A
SN74ACT04	14	Hex Inverter	✓	✓	✓	✓	✓	SCAS518A
SN74ACT08	14	Quad 2-Input AND Gate	✓	✓	✓	✓	✓	SCAS535A
SN74ACT10	14	Triple 3-Input NAND Gate	✓	✓	✓	✓	✓	SCAS526D
SN74ACT11	14	Triple 3-Input AND Gate	✓	✓	✓	✓	✓	SCAS531A
SN74ACT14	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	✓	SCAS557D
SN74ACT32	14	Quad 2-Input OR Gate	✓	✓	✓	✓	✓	SCAS530A
SN74ACT74	14	Dual D-Type Flip-Flop	✓	✓	✓	✓	✓	SCAS520D
SN74ACT86	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓	✓	✓	SCAS534A
SN74ACT240	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCAS515B
SN74ACT241	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCAS516B
SN74ACT244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCAS517B
SN74ACT245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	SCAS452C
SN74ACT373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCAS544C
SN74ACT374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	SCAS539D
SN74ACT533	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCAS553A
SN74ACT534	20	Octal D-Type Flip-Flop		✓	✓	✓	✓	SCAS556A
SN74ACT563	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCAS550A
SN74ACT564	20	Octal D-Type Flip-Flop		✓	✓	✓	✓	SCAS549A
SN74ACT573	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCAS538B
SN74ACT574	20	Octal D-Type Flip-Flop		✓	✓	✓	✓	SCAS537B
SN74ACT1284	20	7-Bit IEEE P1284 Driver/Receiver			✓	✓		SCAS459B
74ACT11004	20	Hex Inverter		✓	✓	✓	✢	SCAS215B
74ACT11008	16	Quad 2-Input Positive-AND Gate		✓	✓		✓	SCAS013C
74ACT11032	14, 16	Quad 2-Input Positive-OR Gate		✓	✓	✓	✓	SCAS008C
74ACT11074	14	Dual D-Type Flip-Flop		✓	✓	✓		SCAS498A
74ACT11139	16	Dual 2-to-4 Decoder/Demultiplexer		✓	✓		✓	SCAS175A
74ACT11240	24	Octal Buffer/Driver		✓	✓	✓		SCAS210A
74ACT11244	24	Octal Buffer/Driver		✓	✓	✓	✓	SCAS006C
74ACT11245	24	Octal Bus Transceiver		✓	✓	✓	✓	SCAS031C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

ACT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
74ACT11257	20	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	✓		SCAS053B
74ACT11286	14	9-Bit Parity Generator/Checker		✓	✓			SCAS069B
74ACT11373	24	Octal D-Type Transparent Latch		✓	✓	✓		SCAS015B
74ACT11374	24	Octal D-Type Flip-Flop		✓	✓	✓		SCAS217A
74ACT11543	28	Octal Registered Bus Transceiver			✓			SCAS136
74ACT11652	28	Octal Registered Bus Transceiver			✓			SCAS087A
74ACT11656	28	Octal Parity Bus Transceiver			✓			SCAS460A
74ACT16240	48	16-Bit Buffer/Driver	✓			✓		SCAS137C
74ACT16241	48	16-Bit Buffer/Driver				✓		SCAS189A
74ACT16244	48	16-Bit Buffer/Driver	✓			✓	✓	SCAS116B
74ACT16245	48	16-Bit Bus Transceiver	✓			✓	✓	SCAS097B
74ACT16254	64	32-to-16 VL Bus Multiplexer/Demultiplexer					✓	SCAS527A
74ACT16373	48	16-Bit D-Type Transparent Latch	✓			✓		SCAS122C
74ACT16374	48	16-Bit D-Type Flip-Flop	✓			✓		SCAS124B
74ACT16470	56	16-Bit Registered Bus Transceiver				✓		SCAS237A
74ACT16474	56	18-Bit Registered Bus Transceiver				✓		SCAS238A
74ACT16475	56	16-Bit Registered Transceiver				✓		SCAS198A
74ACT16540	48	16-Bit Buffer/Driver				✓		SCAS186A
74ACT16541	48	16-Bit Buffer/Driver				✓		SCAS208A
74ACT16543	56	16-Bit Registered Bus Transceiver	✓			✓	✓	SCAS126B
74ACT16544	56	16-Bit Registered Bus Transceiver				✓		SCAS161A
74ACT16620	48	16-Bit Bus Transceiver				✓		SCAS184A
74ACT16623	48	16-Bit Bus Transceiver				✓		SCAS152A
74ACT16640	48	16-Bit Bus Transceiver				✓		SCAS173A
74ACT16646	56	16-Bit Registered Bus Transceiver				✓		SCAS127B
74ACT16648	56	16-Bit Registered Bus Transceiver				✓		SCAS188A
74ACT16651	56	16-Bit Registered Bus Transceiver				✓		SCAS449A
74ACT16652	56	16-Bit Registered Bus Transceiver	✓			✓		SCAS128C
74ACT16657	56	Dual 8-to-9 Bit Parity Bus Transceiver				✓		SCAS164A
74ACT16821	56	20-Bit Bus-Interface Flip-Flop				✓		SCAS176A

commercial package description and availability

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SOIC (small-outline integrated circuit)
D = 8/14/16 pins
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TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
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TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
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PCB = 120 pins (FIFO only)

MIL – See page 4–3 for military package description and availability

schedule

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DEVICE SELECTION GUIDE

ACT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
74ACT16823	56	18-Bit Bus-Interface Flip-Flop				✓		SCAS160A
74ACT16825	56	18-Bit Buffer/Driver				✓		SCAS155B
74ACT16827	56	20-Bit Buffer/Driver				✓		SCAS163A
74ACT16833	56	Dual 8-to-9 Bit Parity Bus Transceiver				✓		SCAS166A
74ACT16841	56	20-Bit Bus-Interface D-Type Latch				✓	✓	SCAS174A
74ACT16861	56	20-Bit Bus Transceiver				✓		SCAS197B
74ACT16863	56	18-Bit Bus Transceiver				✓		SCAS162B
74ACT16864	56	18-Bit Bus Transceiver				✓		SCAS244A
74ACT16952	56	16-Bit Registered Bus Transceiver				✓		SCAS159C
74ACT162841	56	20-Bit Bus-Interface D-Type Latch With Series Resistors				✛		Call

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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MIL – See page 4–3 for military package description and availability

AHC/AHCT
Advanced High-Speed CMOS Logic

The AHC/AHCT logic family provides a natural migration for HCMOS users who need more speed for low-power, low-noise, and low-drive applications. The AHC logic family consists of basic gates, medium-scale integrated circuits, octal and 16-bit Widebus functions fabricated using the EPIC1-S process that produces high performance at low cost. In addition, TI offers a new single-gate solution, designated with 1G in the device name.

Performance characteristics of the AHC family are:

- Speed – With typical propagation delays of 5.2 ns (octals), which is about three times faster than HC devices, AHC devices are the quick and quiet solution for higher-speed operation.
- Low noise – The AHC family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices usually required to get AHC speeds.
- Low power – The AHC family, by using CMOS technology, exhibits low power consumption (40-μA maximum static current, half that of HCMOS).
- Drive – Output-drive current is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- Packaging – AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), PW (TSSOP), DGV (TVSOP), and DCK and DBV (5-pin SOT) packages. Selected AHC devices are available in military versions (SN54AHCXX).

Using TI products offers several business advantages:

- Competitive advantage – AHC and VHC devices have equivalent specifications; therefore, AHC devices are drop-in replaceable. With TI's production capacity, delivery performance, and competitive prices, AHC devices are among the most economical, easy-to-use, and easy-to-get logic products.
- Alternate source – TI has arrangements for one or more alternate sources for AHC/AHCT devices.

For AHC/AHCT data sheets, see the 1997 *AHC/AHCT Logic Advanced High-Speed CMOS Data Book*, literature number SCLD003A.

DEVICE SELECTION GUIDE

AHC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74AHC1G00	5	Single 2-Input Positive-NAND Gate							✓	SCLS313E
SN74AHC1G02	5	Single 2-Input Positive-NOR Gate							✓	SCLS342D
SN74AHC1G04	5	Single Inverter Gate							✓	SCLS318G
SN74AHC1GU04	5	Unbuffered Single Inverter Gate							✓	SCLS343H
SN74AHC1G08	5	Single 2-Input Positive-AND Gate							✓	SCLS314E
SN74AHC1G14	5	Single Schmitt-Trigger Inverter Gate							✓	SCLS321F
SN74AHC1G32	5	Single 2-Input Positive-OR Gate							✓	SCLS317F
SN74AHC1G86	5	Single 2-Input Exclusive-OR Gate							✓	SCLS323E
SN74AHC1G125	5	Single Bus Buffer Gate With 3-State Outputs							✢	SCLS377B
SN74AHC1G126	5	Single Bus Buffer Gate With 3-State Outputs							✢	SCLS379B
SN74AHC00	14	Quad 2-Input NAND Gate	✓	✓	✓	✓	✓	✓		SCLS227D
SN74AHC02	14	Quad 2-Input NOR Gate	✓	✓	✓	✓	✓	✢		SCLS254E
SN74AHC04	14	Hex Inverter	✓	✓	✓	✓	✓	✓		SCLS231H
SN74AHCU04	14	Unbuffered Hex Inverter	✓	✓	✓	✓	✓	✓		SCLS234F
SN74AHC05	14	Hex Inverter	✢	✢	✢	✢	✢	✢		SCLS357B
SN74AHC08	14	Quad 2-Input AND Gate	✓	✓	✓	✓	✓	✢		SCLS236C
SN74AHC14	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	✓	✢		SCLS238D
SN74AHC32	14	Quad 2-Input OR Gate	✓	✓	✓	✓	✓	✢		SCLS247C
SN74AHC74	14	Dual D-Type Flip-Flop With Preset and Clear	✓	✓	✓	✓	✓	✢		SCLS255D
SN74AHC86	14	Quad Exclusive-OR Gate	✓	✓	✓	✓	✓	✢		SCLS249C
SN74AHC123A	16	Dual Monostable Vibrator	✢	✢	✢	✢	✢	✢		SCLS352A
SN74AHC125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓	✓	✓	✢		SCLS256E
SN74AHC126	14	Quad Bus Buffer Gate (OE)	✓	✓	✓	✓	✓	✢		SCLS257F
SN74AHC132	14	Quad NAND Gate With Schmitt-Trigger Inputs	✢	✢	✢	✢	✢	✢		SCLS365B
SN74AHC138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	✓	✓	✓		SCLS258F
SN74AHC139	16	Dual 2-to-4 Line Decoder/Demultiplexer		✓	✓	✓	✓	✓		SCLS259F
SN74AHC157	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓	✓	✓	✓		SCLS345D

commercial package description and availability

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QFP (quad flat package)
RC = 52 pins (FB only)
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SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
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schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74AHC158	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	✓	✓	✓		SCLS346C
SN74AHC174	16	Hex D-Type Flip-Flop With Clear	✢	✢	✢	✢	✢	✢		SCLS425
SN74AHC240	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✢		SCLS251D
SN74AHC244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✓		SCLS226F
SN74AHC245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	✓		SCLS230E
SN74AHC257	20	Quad 2-to-1 Data Selector/Multiplexer		✢	✢	✢	✢	✢		SCLS349C
SN74AHC258	20	Quad 2-to-1 Data Selector/Multiplexer		✢	✢	✢	✢	✢		SCLS350C
SN74AHC273	20	Octal D-Type Flip-Flop With Clear	✓	✓	✓	✓	✓	✓		SCLS376C
SN74AHC367	16	Hex Buffer and Line Driver With 3-State Outputs	✢	✢	✢	✢	✢	✢		SCLS424
SN74AHC373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	✢		SCLS235E
SN74AHC374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	✢		SCLS240E
SN74AHC540	20	Inverting Octal Buffer/Driver	✓	✓	✓	✓	✓	✢		SCLS260E
SN74AHC541	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✢		SCLS261I
SN74AHC573	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	✢		SCLS242F
SN74AHC574	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	✢		SCLS244D
SN74AHC594	16	8-Bit Shift Register With Output Registers	✢	✢	✢	✢	✢	✢		SCLS423
SN74AHC595	16	8-Bit Shift Register With 3-State Output Registers	✢	✢	✢	✢	✢	✢		SCLS373B
SN74AHC4040	16	12-Bit Asynchronous Binary Counter	✢	✢	✢	✢	✢	✢		SCLS422
SN74AHC4051	16	Analog Multiplexer/Demultiplexer	✢	✢	✢	✢	✢	✢		SCLS415
SN74AHC4053	16	Analog Multiplexer/Demultiplexer	✢	✢	✢	✢	✢	✢		SCLS416
SN74AHC4066	14	Quad Bilateral Analog Switch		✢	✢	✢	✢	✢		SCLS421
SN74AHC16240	48	16-Bit Buffer/Driver	✢			✓	✓	✓		SCLS326D
SN74AHC16244	48	16-Bit Buffer/Driver	✢			✓	✓	✓		SCLS327D
SN74AHC16245	48	16-Bit Bus Transceiver	✢			✢	✢	✢		SCLS328B
SN74AHC16373	48	16-Bit D-Type Transparent Latch	✢			✓	✓	✓		SCLS329C
SN74AHC16374	48	16-Bit D-Type Flip-Flop	✢			✓	✓	✓		SCLS330D
SN74AHC16540	48	16-Bit Inverting Buffer/Driver	✢			✓	✓	✓		SCLS331C
SN74AHC16541	48	16-Bit Buffer/Driver	✢			✓	✓	✓		SCLS332C

commercial package description and availability

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SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
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QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
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PN = 80 pins
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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE SELECTION GUIDE

AHCT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74AHCT1G00	5	Single 2-Input Positive-NAND Gate							✓	SCLS316F
SN74AHCT1G02	5	Single 2-Input Positive-NOR Gate							✓	SCLS341E
SN74AHCT1G04	5	Single Inverter Gate							✓	SCLS319G
SN74AHCT1G08	5	Single 2-Input Positive-AND Gate							✓	SCLS315F
SN74AHCT1G14	5	Single Schmitt-Trigger Inverter Gate							✓	SCLS322H
SN74AHCT1G32	5	Single 2-Input Positive-OR Gate							✓	SCLS320F
SN74AHCT1G86	5	Single 2-Input Exclusive-OR Gate							✓	SCLS324F
SN74AHCT1G125	5	Single Bus Buffer Gate With 3-State Outputs							+	SCLS378B
SN74AHCT1G126	5	Single Bus Buffer Gate With 3-State Outputs							+	SCLS380B
SN74AHCT00	14	Quad 2-Input NAND Gate	✓	✓	✓	✓	✓	✓		SCLS229E
SN74AHCT02	14	Quad 2-Input NOR Gate	✓	✓	✓	✓	✓	✓		SCLS262E
SN74AHCT04	14	Hex Inverter	✓	✓	✓	✓	✓	✓		SCLS232H
SN74AHCT08	14	Quad 2-Input AND Gate	✓	✓	✓	✓	✓	✓		SCLS237F
SN74AHCT14	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	✓	✓		SCLS246I
SN74AHCT32	14	Quad 2-Input OR Gate	✓	✓	✓	✓	✓	✓		SCLS248F
SN74AHCT74	14	Dual D-Type Flip-Flop With Preset and Clear	✓	✓	✓	✓	✓	✓		SCLS263H
SN74AHCT86	14	Quad Exclusive-OR Gate	✓	✓	✓	✓	✓	✓		SCLS250G
SN74AHCT123A	16	Dual Retriggerable Monostable Vibrator	+	+	+	+	+	+		SCLS420
SN74AHCT125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓	✓	✓	✓		SCLS264I
SN74AHCT126	14	Quad Bus Buffer Gate (OE)	✓	✓	✓	✓	✓	✓		SCLS265J
SN74AHCT132	14	Quad NAND Gate With Schmitt-Trigger Inputs	+	+	+	+	+	+		SCLS366B
SN74AHCT138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	✓	✓	✓		SCLS266G
SN74AHCT139	16	Dual 2-to-4 Line Decoder/Demultiplexer		✓	✓	✓	✓	✓		SCLS267G
SN74AHCT157	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	✓	✓	✓		SCLS347F
SN74AHCT158	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	✓	✓	✓		SCLS348E
SN74AHCT174	16	Hex D-Type Flip-Flop With Clear	+	+	+	+	+	+		SCLS419
SN74AHCT240	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✓		SCLS252F

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
+ = Planned

MIL – See page 4–3 for military package description and availability

AHCT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74AHCT244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✓		SCLS228G
SN74AHCT245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	✓		SCLS233F
SN74AHCT257	20	Quad 2-to-1 Data Selector/Multiplexer		✛	✛	✛	✛	✛		SCLS351D
SN74AHCT258	20	Quad 2-to-1 Data Selector/Multiplexer		✛	✛	✛	✛	✛		SCLS344D
SN74AHCT273	20	Octal D-Type Flip-Flop With Clear	✛	✛	✛	✛	✛	✛		SCLS375A
SN74AHCT367	16	Hex Buffer and Line Driver With 3-State Outputs	✛	✛	✛	✛	✛	✛		SCLS418
SN74AHCT373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	✓		SCLS239H
SN74AHCT374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	✓		SCLS241G
SN74AHCT540	20	Inverting Octal Buffer/Driver	✓	✓	✓	✓	✓	✓		SCLS268G
SN74AHCT541	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	✓		SCLS269J
SN74AHCT573	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	✓		SCLS243H
SN74AHCT574	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	✓		SCLS245F
SN74AHCT594	16	8-Bit Shift Register With Output Registers	✛	✛	✛	✛	✛	✛		SCLS417
SN74AHCT595	16	8-Bit Shift Register With 3-State Output Registers	✛	✛	✛	✛	✛	✛		SCLS374B
SN74AHCT16240	48	16-Bit Buffer/Driver	✛			✓	✓	✓		SCLS333E
SN74AHCT16244	48	16-Bit Buffer/Driver	✛			✓	✓	✓		SCLS334E
SN74AHCT16245	48	16-Bit Bus Transceiver	✛			✓	✓	✓		SCLS335E
SN74AHCT16373	48	16-Bit D-Type Transparent Latch	✛			✓	✓	✓		SCLS336D
SN74AHCT16374	48	16-Bit D-Type Flip-Flop	✛			✓	✓	✓		SCLS337D
SN74AHCT16540	48	16-Bit Inverting Buffer/Driver	✛			✓	✓	✓		SCLS338D
SN74AHCT16541	48	16-Bit Buffer/Driver	✛			✓	✓	✓		SCLS339D

commercial package description and availability

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SOT (small-outline transistor)
DBV = 5 pins
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SSOP (shrink small-outline package)
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QSOP (quarter-size outline package)
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SOIC (small-outline integrated circuit)
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DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

ALB
Advanced Low-Voltage BiCMOS

The specially designed 3.3-V ALB family uses the latest 0.6-μ BiCMOS technology for bus-interface functions. In addition, ALB provides 25-mA drive at 3.3 V with maximum propagation delays of 2.2 ns, making it TI's fastest logic family to date. The inputs have clamping diodes to eliminate overshoot and undershoot.

The ALB family is currently available in a limited number of functions with Widebus™ and Shrink Widebus™ footprints with advanced packaging options such as shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and planned for thin very small-outline package (TVSOP).

DEVICE SELECTION GUIDE

ALB

DEVICE	NO. PINS	FUNCTION	AVAILABILITY SSOP	AVAILABILITY TSSOP	AVAILABILITY TVSOP	LITERATURE REFERENCE
SN74ALB16244	48	16-Bit Buffer/Driver	✓	✓	✓	SCBS647C
SN74ALB16245	48	16-Bit Bus Transceiver	✓	✓	✓	SCBS678B

commercial package description and availability

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QSOP (quarter-size outline package)
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SOIC (small-outline integrated circuit)
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DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
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PCB = 120 pins (FIFO only)

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MIL – See page 4–3 for military package description and availability

ALS
Advanced Low-Power Schottky Logic

The ALS family provides a full spectrum of over 130 bipolar logic functions.

This family, combined with the AS family, can be used to optimize systems through performance budgeting. By using AS in speed-critical paths and ALS where speed is less critical, designers can optimize speed and power performance.

The ALS family includes gates, flip-flops, counters, drivers, transceivers, registered transceivers, readback latches, clock drivers, register files, and multiplexers.

For ALS data sheets, see the 1995 *ALS/AS Logic Data Book*, literature number SDAD001C.

DEVICE SELECTION GUIDE

ALS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74ALS00A	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓		SDAS187A
SN74ALS02A	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓		SDAS111B
SN74ALS03B	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓		SDAS013B
SN74ALS04B	14	Hex Inverter	✓	✓	✓	✓	SDAS063B
SN74ALS05A	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	✓	SDAS190A
SN74ALS08	14	Quad 2-Input Positive-AND Gate	✓	✓	✓		SDAS191A
SN74ALS09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	✓	✓	✓		SDAS084B
SN74ALS10A	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓		SDAS002B
SN74ALS11A	14	Triple 3-Input Positive-AND Gate	✓	✓	✓		SDAS009C
SN74ALS20A	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓		SDAS192B
SN74ALS21A	14	Dual 4-Input Positive-AND Gate	✓	✓	✓		SDAS085B
SN74ALS27A	14	Triple 3-Input Positive-NOR Gate	✓	✓	✓		SDAS112B
SN74ALS30A	14	8-Input Positive-NAND Gate	✓	✓	✓		SDAS010B
SN74ALS32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓		SDAS113B
SN74ALS35A	14	Hex Noninverter With Open-Collector Outputs		✓	✓		SDAS011C
SN74ALS37A	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓		SDAS195A
SN74ALS38B	14	Quad 2-Input Postive-NAND Gate With Open-Collector Outputs	✓	✓	✓		SDAS196B
SN74ALS74A	14	Dual D-Type Flip-Flop With Clear and Preset	✓	✓	✓		SDAS143C
SN74ALS86	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓		SDAS006B
SN74ALS109A	16	Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flop	✓	✓	✓		SDAS198B
SN74ALS112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	✓	✓	✓		SDAS199A
SN74ALS133	16	13-Input Positive-NAND Gate	✓	✓	✓		SDAS202B
SN74ALS137A	16	3-to-8 Decoder/Demultiplexer With Address Registers	✓	✓	✓		SDAS203C
SN74ALS138A	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓		SDAS055E
SN74ALS139	16	Dual 2-to-4 Decoder/Demultiplexer	✓	✓	✓		SDAS204A
SN74ALS151	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS205A
SN74ALS153	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS206A
SN74ALS156	16	Dual 2-to-4 Decoder/Demultiplexer With Open-Collector Outputs		✓	✓		SDAS099C
SN74ALS157A	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS081C
SN74ALS158	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS081C

commercial package description and availability

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RC = 52 pins (FB only)
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SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74ALS161B	16	4-Bit Synchronous Binary Counter	✓	✓	✓		SDAS024A
SN74ALS163B	16	4-Bit Synchronous Binary Counter	✓	✓	✓		SDAS024A
SN74ALS164A	14	8-Bit Parallel-Out Serial Shift Register		✓	✓		SDAS159D
SN74ALS165	16	8-Bit Parallel-In Shift Register	✓	✓	✓		SDAS157B
SN74ALS166	16	8-Bit Parallel-In Shift Register		✓	✓		SDAS156C
SN74ALS169B	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDAS125B
SN74ALS174	16	Hex D-Type Flip-Flop With Clear	✓	✓	✓		SDAS207D
SN74ALS175	16	Quad D-Type Flip-Flop With Clear	✓	✓	✓		SDAS207D
SN74ALS191A	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDAS210C
SN74ALS193A	16	4-Bit Synchronous Up/Down Binary Counter With Dual Clock and Clear	✓	✓	✓		SDAS211C
SN74ALS240A	20	Octal Buffer/Driver	✓	✓	✓		SDAS214C
SN74ALS240A-1	20	Octal Buffer/Driver		✓	✓		SDAS214C
SN74ALS241C	20	Octal Buffer/Driver	✓	✓	✓		SDAS153E
SN74ALS241C-1	20	Octal Buffer/Driver		✓	✓		SDAS153E
SN74ALS243A	14	Quad Bus Transceiver	✓	✓	✓		SDAS069B
SN74ALS244C	20	Octal Buffer/Driver	✓	✓	✓	✓	SDAS142C
SN74ALS244C-1	20	Octal Buffer/Driver		✓	✓		SDAS142C
SN74ALS245A	20	Octal Bus Transceiver	✓	✓	✓	✓	SDAS272
SN74ALS245A-1	20	Octal Bus Transceiver		✓	✓		SDAS272
SN74ALS251	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS215A
SN74ALS253	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS216A
SN74ALS257A	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS124C
SN74ALS258A	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDAS124C
SN74ALS259	16	8-Bit Addressable Latch	✓	✓	✓		SDAS217A
SN74ALS273	20	Octal D-Type Flip-Flop With Clear	✓	✓	✓		SDAS218A
SN74ALS280	14	9-Bit Parity Generator/Checker		✓	✓		SDAS038C
SN74ALS299	20	8-Bit Universal Shift/Storage Register	✓	✓	✓		SDAS220B
SN74ALS323	20	8-Bit Universal Shift/Storage Register	✓	✓	✓		SDAS267A
SN74ALS373A	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	SDAS083B
SN74ALS374A	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	SDAS167B

commercial package description and availability

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DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
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MIL – See page 4–3 for military package description and availability

DEVICE SELECTION GUIDE

ALS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74ALS520	20	8-Bit Identity Comparator	✓	✓	✓		SDAS224B
SN74ALS521	20	8-Bit Identity Comparator		✓	✓		SDAS224B
SN74ALS533A	20	Octal D-Type Transparent Latch		✓	✓		SDAS270
SN74ALS534A	20	Octal D-Type Flip-Flop	✓	✓	✓		SDAS168B
SN74ALS540	20	Octal Buffer/Driver		✓	✓		SDAS025C
SN74ALS540-1	20	Octal Buffer/Driver		✓	✓		SDAS025C
SN74ALS541	20	Octal Buffer/Driver	✓	✓	✓		SDAS025C
SN74ALS541-1	20	Octal Buffer/Driver		✓	✓		SDAS025C
SN74ALS561A	20	4-Bit Synchronous Binary Counter	✓	✓	✓		SDAS225A
SN74ALS563B	20	Octal D-Type Transparent Latch	✓	✓	✓		SDAS163A
SN74ALS564B	20	Octal D-Type Flip-Flop	✓	✓	✓		SDAS164B
SN74ALS568A	20	4-Bit Synchronous Up/Down Decade Counter		✓			SDAS229A
SN74ALS569A	20	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDAS229A
SN74ALS573C	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	SDAS048D
SN74ALS574B	20	Octal D-Type Flip-Flop	✓	✓	✓		SDAS165B
SN74ALS575A	24	Octal D-Type Flip-Flop		✓	✓		SDAS165B
SN74ALS576B	20	Octal D-Type Flip-Flop	✓	✓	✓		SDAS065B
SN74ALS577A	24	Octal D-Type Flip-Flop		✓	✓		SDAS065B
SN74ALS580B	20	Octal D-Type Transparent Latch	✓	✓	✓		SDAS277
SN74ALS620A	20	Octal Bus Transceiver		✓	✓		SDAS226A
SN74ALS621A	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDAS226A
SN74ALS621A-1	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDAS226A
SN74ALS623A	20	Octal Bus Transceiver		✓	✓		SDAS226A
SN74ALS638A-1	20	Octal Bus Transceiver		✓	✓		SDAS123A
SN74ALS639A	20	Octal Bus Transceiver		✓	✓		SDAS123A
SN74ALS640B	20	Octal Bus Transceiver	✓	✓	✓		SDAS122A
SN74ALS640B-1	20	Octal Bus Transceiver		✓	✓		SDAS122A
SN74ALS641A	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDAS300
SN74ALS641A-1	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDAS300
SN74ALS642A-1	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDAS300

commercial package description and availability

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DGG = 48/56/64 pins

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DBB = 80 pins

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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74ALS645A	20	Octal Bus Transceiver	✓	✓	✓		SDAS278
SN74ALS645A-1	20	Octal Bus Transceiver		✓	✓		SDAS278
SN74ALS646A	24	Octal Registered Bus Transceiver	✓	✓	✓		SDAS039F
SN74ALS646A-1	24	Octal Registered Bus Transceiver		✓	✓		SDAS039F
SN74ALS648A	24	Octal Registered Bus Transceiver	✓	✓	✓		SDAS039F
SN74ALS651A	24	Octal Registered Bus Transceiver		✓	✓		SDAS066F
SN74ALS651A-1	24	Octal Registered Bus Transceiver		✓	✓		SDAS066F
SN74ALS652A	24	Octal Registered Bus Transceiver	✓	✓	✓		SDAS066F
SN74ALS652A-1	24	Octal Registered Bus Transceiver		✓	✓		SDAS066F
SN74ALS653	24	Octal Registered Bus Transceiver	✓	✓	✓		SDAS066F
SN74ALS654	24	Octal Registered Bus Transceiver		✓	✓		SDAS066F
SN74ALS666	24	8-Bit D-Type Transparent Readback Latch		✓	✓		SDAS227A
SN74ALS667	24	8-Bit D-Type Transparent Readback Latch		✓	✓		SDAS227A
SN74ALS688	20	8-Bit Identity Comparator	✓	✓	✓		SDAS228A
SN74ALS760	20	Octal Buffer/Driver With Open-Collector Outputs		✓	✓		SDAS141A
SN74ALS804A	20	Hex 2-Input NAND Gate	✓	✓	✓		SDAS022C
SN74ALS805A	20	Hex 2-Input NOR Gate	✓	✓	✓		SDAS023C
SN74ALS832A	20	Hex 2-Input Positive-OR Gate	✓	✓	✓		SDAS017C
SN74ALS841	24	10-Bit Bus-Interface D-Type Latch		✓	✓		SDAS059C
SN74ALS842	24	10-Bit Bus-Interface D-Type Latch		✓	✓		SDAS059C
SN74ALS843	24	9-Bit Bus-Interface D-Type Latch		✓	✓		SDAS232A
SN74ALS845	24	8-Bit Bus-Interface D-Type Latch		✓	✓		SDAS233A
SN74ALS857	24	Hex 2-to-1 Universal Multiplexer	✓	✓	✓		SDAS170A
SN74ALS867A	24	8-Bit Synchronous Up/Down Binary Counter		✓	✓		SDAS115C
SN74ALS869	24	8-Bit Synchronous Up/Down Binary Counter		✓	✓		SDAS115C
SN74ALS870	24	Dual 16 × 4 Register File	✓	✓	✓		SDAS139A
SN74ALS873B	24	Dual 4-Bit D-Type Latch	✓	✓	✓		SDAS036D
SN74ALS874B	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	✓	✓	✓		SDAS061C
SN74ALS876A	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop		✓	✓		SDAS061C
SN74ALS990	20	8-Bit D-Type Transparent Readback Latch		✓	✓		SDAS027B

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE SELECTION GUIDE

ALS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74ALS992	24	9-Bit D-Type Transparent Readback Latch		✓	✓		SDAS028B
SN74ALS994	24	10-Bit D-Type Transparent Readback Latch		✓	✓		SDAS237A
SN74ALS996	24	8-Bit D-Type Edge-Triggered Readback Latch	✓	✓	✓		SDAS098B
SN74ALS996-1	24	8-Bit D-Type Edge-Triggered Readback Latch		✓	✓		SDAS098B
SN74ALS1004	14	Hex Inverting Buffer		✓	✓		SDAS074B
SN74ALS1005	14	Hex Inverting Buffer With Open-Collector Outputs	✓	✓	✓		SDAS240A
SN74ALS1034	14	Hex Noninverting Buffer	✓	✓	✓		SDAS053B
SN74ALS1035	14	Hex Noninverting Buffer With Open-Collector Outputs	✓	✓	✓		SDAS243A
SN74ALS1244A	20	Octal Buffer/Driver	✓	✓	✓		SDAS186B
SN74ALS1245A	20	Octal Bus Transceiver	✓	✓	✓		SDAS245A
SN74ALS1640A	20	Octal Bus Transceiver		✓			SDAS246B
SN74ALS1645A	20	Octal Bus Transceiver		✓	✓		SDAS246B
SN74ALS2240	20	Octal Buffer/Driver With Series Resistors		✓	✓		SDAS268A
SN74ALS2541	20	Octal Buffer/Driver With Series Resistors		✓	✓		SDAS273
SN74ALS29821	24	10-Bit Bus-Interface Flip-Flop	✓	✓	✓		SDAS145B
SN74ALS29827	24	10-Bit Buffer/Driver		✓	✓		SDAS095B
SN74ALS29828	24	10-Bit Buffer/Driver		✓	✓		SDAS095B
SN74ALS29833	24	8-Bit to 9-Bit Parity Bus Transceiver		✓	✓		SDAS119D
SN74ALS29841	24	10-Bit D-Type Bus-Interface Latch		✓	✓		SDAS149A
SN74ALS29863	24	9-Bit Bus Transceiver		✓	✓		SDAS096C

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ALVC
Advanced Low-Voltage CMOS Technology

One of the highest-performance 3.3-V bus-interface families is the ALVC family. These specially designed 3-V products are processed in 0.6-μ CMOS technology, giving typical propagation delays of less than 3 ns, along with current drive of 24 mA and static power consumption of 40 μA for bus-interface functions. The ALVC devices have bus-hold cells on inputs to eliminate the need for external pullup resistors for floating inputs. With over 50 Widebus™ and Widebus™ with series-damping resistors already released and with gates/octals on the roadmap, ALVC is quickly becoming the industry standard for all 3.3-V logic applications. The family also features innovative functions that make it ideal for memory interleaving, multiplexing, and interfacing to SDRAMs.

The ALVC family is offered in the Widebus™ footprints with all of the advanced packaging such as shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP).

For ALVC data sheets, see the 1998 *ALVC Advanced Low-Voltage CMOS Data Book*, literature number SCED006.

DEVICE SELECTION GUIDE

ALVC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			SOIC	SSOP	TSSOP	TVSOP	SOT	
Gates and Octals								
SN74ALVC1G00	5	Single 2-Input Positive-NAND Gate					✛	SCES099B
SN74ALVC1G04	5	Single Inverter Gate					✛	SCES100B
SN74ALVC1G08	5	Single 2-Input Positive-AND Gate					✛	SCES102B
SN74ALVC1G14	5	Single Schmitt-Trigger Inverter					✛	SCES103C
SN74ALVC1G32	5	Single 2-Input Positive-OR Gate					✛	SCES104B
SN74ALVC1G79	5	Single Positive-Edge-Triggered D-Type Flip-Flop					✛	SCES105B
SN74ALVC1G125	5	Single Bus Buffer Gate					✛	SCES113C
SN74ALVC1G126	5	Single Bus Buffer Gate					✛	SCES114C
SN74ALVC00	14	Quad 2-Input Positive-NAND Gate	✛		✛	✛		SCES115B
SN74ALVC04	14	Hex Inverter	✓		✓	✓		SCES117E
SN74ALVC08	14	Quad 2-Input Positive-AND Gate	✛		✛	✛		SCES101C
SN74ALVC10	14	Triple 3-Input Positive-NAND Gate	✛		✛	✛		SCES106C
SN74ALVC14	14	Hex Inverter With Schmitt Trigger	✛		✛	✛		SCES107C
SN74ALVC32	14	Quad 2-Input Positive-OR Gate	✛		✛	✛		SCES108C
SN74ALVC74	14	Dual D-Type Flip-Flop With Preset and Clear	✛		✛	✛		SCES109D
SN74ALVC125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✛		✛	✛		SCES110C
SN74ALVC126	14	Quad Bus Buffer Gate (OE)	✛		✛	✛		SCES111C
SN74ALVCH244	20	Octal Buffer/Driver	✓		✓	✓		SCES112B
SN74ALVCH245	20	Octal Bus Transceiver	✛		✛	✛		SCES119B
SN74ALVCH373	20	Octal Transparent D-Type Latch	✛		✛	✛		SCES116C
SN74ALVCH374	20	Octal D-Type Flip-Flop	✛		✛	✛		SCES118C
Widebus™ Devices								
SN74ALVCH16240	48	16-Bit Buffer/Driver		✓	✓	✛		SCES045B
SN74ALVC16244A	48	16-Bit Buffer/Driver		✓	✓			SCAS250E
SN74ALVCH16244	48	16-Bit Buffer/Driver		✓	✓	✓		SCES014D
SN74ALVCH16245	48	16-Bit Bus Transceiver		✓	✓	✓		SCES015E
SN74ALVCH16260	56	12-to-24 Multiplexed D-Type Latch		✓	✓			SCES046C
SN74ALVCH16269	56	12-to-24 Registered Bus Exchanger		✓	✓			SCES019G
SN74ALVCH16270	56	12-to-24 Registered Bus Exchanger		✓	✓			SCES028D

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74ALVCH16271	56	12-to-24 Multiplexed Bus Exchanger		✓	✓			SCES017D
SN74ALVCH16282	80	18-to-36 Registered Bus Exchanger				✓		SCES036B
SN74ALVC16334	48	16-Bit Universal Bus Driver		✓	✓	✓		SCES128B
SN74ALVCH16334	48	16-Bit Universal Bus Driver		✓	✓	✓		SCES090G
SN74ALVCH16344	56	1-to-4 Address Driver		✓	✓	✓		SCES054E
SN74ALVCH16373	48	16-Bit D-Type Transparent Latch		✓	✓			SCES020B
SN74ALVCH16374	48	16-Bit D-Type Flip-Flop		✓	✓			SCES021C
SN74ALVCH16409	56	9-Bit, 4-Port Universal Bus Exchanger		✓	✓			SCES022D
SN74ALVCH16500	56	18-Bit Universal Bus Transceiver		✓	✓			SCES023E
SN74ALVCH16501	56	18-Bit Universal Bus Transceiver		✓	✓			SCES024B
SN74ALVCH16524	56	18-Bit Registered Bus Transceiver		✓	✓			SCES080B
SN74ALVCH16525	56	18-Bit Registered Bus Transceiver		✓	✓			SCES059B
SN74ALVCH16543	56	16-Bit Registered Bus Transceiver		✓	✓			SCES025C
SN74ALVCH16600	56	18-Bit Universal Bus Transceiver		✓	✓			SCES030C
SN74ALVCH16601	56	18-Bit Universal Bus Transceiver		✓	✓			SCES027C
SN74ALVCH16646	56	16-Bit Registered Bus Transceiver		✓	✓	✓		SCES032D
SN74ALVCH16721	56	20-Bit Bus-Interface Flip-Flop		✓	✓	✓		SCES052C
SN74ALVCH16820	56	10-Bit Bus-Interface Flip-Flop		✓	✓			SCES035D
SN74ALVCH16821	56	20-Bit Bus-Interface Flip-Flop		✓	✓			SCES037B
SN74ALVCH16823	56	18-Bit Bus-Interface Flip-Flop		✓	✓			SCES038C
SN74ALVCH16825	56	18-Bit Buffer/Driver		✓	✓			SCES039B
SN74ALVCH16827	56	20-Bit Buffer/Driver		✓	✓			SCES041B
SN74ALVCH16831	80	1-to-4 Address Driver				✓		SCES083C
SN74ALVCH16832	64	1-to-4 Address Driver			✓			SCES098C
SN74ALVC16834	56	18-Bit Universal Bus Driver		✛	✛	✛		Call
SN74ALVCH16834	56	18-Bit Universal Bus Driver		✛	✛	✛		Call
SN74ALVC16835	56	18-Bit Universal Bus Driver		✓	✓	✓		SCES125B
SN74ALVCH16835	56	18-Bit Universal Bus Driver		✓	✓	✓		SCES053D
SN74ALVCH16841	56	20-Bit Bus-Interface D-Type Latch		✓	✓			SCES043C
SN74ALVCH16863	48	18-Bit Bus Transceiver		✓	✓			SCES060A

commercial package description and availability

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DEVICE SELECTION GUIDE

ALVC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74ALVCH16901	64	18-Bit Universal Bus Transceiver With Clock Enable, Parity Generator			✓			SCES010D
SN74ALVCH16952	56	16-Bit Registered Bus Transceiver		✓	✓	✓		SCES011C
SN74ALVC162334	48	16-Bit Universal Bus Driver		✓	✓	✓		SCE127B
SN74ALVC162831	80	1-to-4 Address Driver				✓		SCAS605
SN74ALVC162835	56	18-Bit Universal Bus Driver		✓	✓	✓		SCES126C
SN74ALVC162836	56	20-Bit Universal Bus Driver		✓	✓	✓		SCES129A
SN74ALVC164245	48	16-Bit Transceiver and 3.3-V to 5-V Shifter		✓	✓			SCAS416D
Widebus™ Devices With Series-Damping Resistors								
SN74ALVCH162244	48	16-Bit Buffer/Driver		✓	✓			SCES065B
SN74ALVCHR162245	48	16-Bit Bus Transceiver With Input and Output Series-Damping Resistors		✓	✓			SCES064A
SN74ALVCH162260	56	12-to-24 Multiplexed D-Type Latch With Series-Damping Resistors		✓	✓			SCAS570D
SN74ALVCH162268	56	12-to-24 Registered Bus Exchanger		✓	✓			SCES018D
SN74ALVCHR162269A	56	12-to-24 Registered Bus Exchanger With Input and Output Series-Damping Resistors		✓	✓			SCES050G
SN74ALVCH162334	48	16-Bit Universal Bus Driver With Series-Damping Resistors on B Port		✓	✓	✓	✓	SCES120D
SN74ALVCH162344	56	1-to-4 Address Driver		✓	✓	✓	✓	SCES085D
SN74ALVCH162374	48	16-Bit D-Type Flip-Flop		✓	✓			SCES092A
SN74ALVCHR162409	56	9-Bit, 4-Port Universal Bus Exchanger With Input and Output Series-Damping Resistors		✓	✓			SCES056D
SN74ALVCH162525	56	18-Bit Registered Bus Transceiver		✓	✓			SCES058C
SN74ALVCH162601	56	18-Bit Universal Bus Transceiver		✓	✓			SCES026E
SN74ALVCHR162601	56	18-Bit Universal Bus Transceiver With Input and Output Series-Damping Resistors		✓	✓	✓		SCES123C
SN74ALVCH162721	56	20-Bit Bus-Interface Flip-Flop		✓	✓			SCES055C
SN74ALVCH162820	56	20-Bit Bus-Interface Flip-Flop With Dual Outputs		✓	✓			SCES012D
SN74ALVCH162827	56	20-Bit Buffer/Driver		✓	✓	✓		SCES013D
SN74ALVCH162830	80	1-to-2 Address Driver				✓		SCES082E
SN74ALVCHS162830	80	1-to-2 Address Driver				✓		SCES097D

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DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74ALVCH162831	80	1-to-4 Address Driver				✓		SCES084D
SN74ALVCH162832	64	1-to-4 Address Driver			✓			SCAS588D
SN74ALVCH162835	56	18-Bit Universal Bus Driver		✓	✓	✓		SCES121B
SN74ALVCH162836	56	20-Bit Universal Bus Driver		✓	✓	✓		SCES122C
SN74ALVCH162841	56	20-Bit Bus-Interface D-Type Latch With Input and Output Series-Damping Resistors		✓	✓			SCES088B

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ALVT
Advanced Low-Voltage BiCMOS Technology

ALVT is the highest performance 3.3-V TI bus-interface to date. These specially designed 5-V tolerant, 3.3-V products use the latest 0.6-μ BiCMOS technology for bus-interface functions. ALVT provides superior performance, delivering 2.4-ns propagation delays, current drive of 64 mA, and static power consumption of 90 μA. The ALVT devices have bus-hold cells on inputs to eliminate the need for external pullup resistors for floating inputs. The ALVT family also provides innovative features, such as series-damping resistors to reduce transmission-line effects, and power-up 3-state to eliminate bus-current loading. ALVT products also are well suited for live-insertion applications with an I_{off} of 0.1 mA. Looking to the future, the ALVT family is already specified for 2.5-V operation.

The ALVT family is planned in a limited number of functions with Widebus™ and Shrink Widebus™ footprints with advanced packaging options such as shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP).

DEVICE SELECTION GUIDE

ALVT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	SSOP	TSSOP	TVSOP	
SN74ALVTH16240	48	16-Bit Buffer/Driver		✢	✢		Call
SN74ALVTH16244	48	16-Bit Buffer/Driver		✢	✢	✢	SCES070D
SN74ALVTH16245	48	16-Bit Bus Transceiver		✢	✢	✢	SCES066D
SN74ALVTH16260	56	12-to-24 Multiplexed D-Type Latch		✢	✢		Call
SN74ALVTH16373	48	16-Bit Transparent D-Type Latch		✢	✢	✢	SCES067D
SN74ALVTH16374	48	16-Bit Edge-Triggered D-Type Flip-Flop		✢	✢	✢	SCES068D
SN74ALVTH16501	56	18-Bit Universal Bus Transceiver		✢	✢	✢	SCES071C
SN74ALVTH16543	56	16-Bit Registered Bus Transceiver		✢	✢		SCES073B
SN74ALVTH16601	56	18-Bit Universal Bus Transceiver		✢	✢		Call
SN74ALVTH16652		16-Bit Registered Bus Transceiver		✢	✢		Call
SN74ALVTH16821	56	20-Bit Bus-Interface Flip-Flop		✢	✢		SCES078B
SN74ALVTH16827	56	20-Bit Buffer/Driver		✢	✢		SCES076B
SN74ALVTH162244	48	16-Bit Buffer/Driver With Series-Damping Resistors		✢	✢		SCES074C
SN74ALVTH162245	48	16-Bit Bus Transceiver With Series-Damping Resistors		✢	✢		Call

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

AS
Advanced Schottky Logic

The AS family of high-performance bipolar logic includes over 90 functions that offer high drive capabilities.

This family, combined with the ALS family, can be used to optimize system speed and power through performance budgeting. By using AS in speed-critical paths and ALS where speed is less critical, designers can optimize speed and power performance.

The AS family includes gates, flip-flops, counters, drivers, transceivers, registered transceivers, readback latches, clock drivers, register files, and multiplexers.

For AS data sheets, see the 1995 *ALS/AS Logic Data Book*, literature number SDAD001C.

DEVICE SELECTION GUIDE

AS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN74AS00	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	SDAS187A
SN74AS02	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓	SDAS111B
SN74AS04	14	Hex Inverter	✓	✓	✓	SDAS063B
SN74AS08	14	Quad 2-Input Positive-AND Gate	✓	✓	✓	SDAS191A
SN74AS10	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓	SDAS002B
SN74AS11	16	Triple 3-Input Positive-AND Gate	✓	✓	✓	SDAS009C
SN74AS20	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓	SDAS192B
SN74AS21	14	Dual 4-Input Positive-AND Gate		✓	✓	SDAS085B
SN74AS27	14	Triple 3-Input Positive-NOR Gate	✓	✓	✓	SDAS112B
SN74AS30	14	8-Input Positive-NAND Gate	✓	✓	✓	SDAS010B
SN74AS32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	SDAS113B
SN74AS74A	14	Dual D-Type Flip-Flop	✓	✓	✓	SDAS143C
SN74AS109A	16	Dual J-$\overline{K}$ Edge-Triggered Flip-Flop	✓	✓	✓	SDAS198B
SN74AS137	16	3-to-8 Decoder/Demultiplexer		✓	✓	SDAS203C
SN74AS138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	SDAS055E
SN74AS151	16	8-to-1 Data Selector/Multiplexer		✓	✓	SDAS205A
SN74AS153	16	Dual 4-to-1 Data Selector/Multiplexer		✓	✓	SDAS206A
SN74AS157	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	SDAS081C
SN74AS158	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	SDAS081C
SN74AS161	16	4-Bit Synchronous Binary Counter	✓	✓	✓	SDAS024A
SN74AS163	16	4-Bit Synchronous Binary Counter	✓	✓	✓	SDAS024A
SN74AS169A	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓	SDAS125B
SN74AS174	16	Hex D-Type Flip-Flop With Clear	✓	✓	✓	SDAS207D
SN74AS175B	16	Quad D-Type Flip-Flop With Clear	✓	✓	✓	SDAS207D
SN74AS181A	24	4-Bit Arithmetic Logic Unit	✓	✓	✓	SDAS209B
SN74AS194	16	4-Bit Bidirectional Universal Shift Register	✓	✓	✓	SDAS212A
SN74AS230A	14	Octal Buffer/Driver		✓	✓	SDAS213B
SN74AS240A	20	Octal Buffer/Driver	✓	✓	✓	SDAS214C
SN74AS241A	20	Octal Buffer/Driver	✓	✓	✓	SDAS153E
SN74AS244A	20	Octal Buffer/Driver	✓	✓	✓	SDAS142C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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QFP (quad flat package)
RC = 52 pins (FB only)
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PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN74AS245	20	Octal Bus Transceiver	✓	✓	✓	SDAS272
SN74AS250A	20	16-to-1 Data Generator/Multiplexer	✓	✓	✓	SDAS137A
SN74AS253A	16	Dual 4-to-1 Data Selector/Multiplexer		✓	✓	SDAS216A
SN74AS257	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	SDAS124C
SN74AS258	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	SDAS124C
SN74AS280	14	9-Bit Parity Generator/Checker		✓	✓	SDAS038C
SN74AS286	14	9-Bit Parity Generator/Checker	✓	✓	✓	SDAS050B
SN74AS298A	16	Quad 2-to-1 Multiplexer		✓	✓	SDAS219B
SN74AS353B	16	Dual 4-to-1 Data Selector/Multiplexer		✓	✓	SDAS222A
SN74AS373	20	Octal D-Type Transparent Latch	✓	✓	✓	SDAS083B
SN74AS374	20	Octal D-Type Flip-Flop	✓	✓	✓	SDAS167B
SN74AS533A	20	Octal D-Type Transparent Latch		✓	✓	SDAS270
SN74AS573A	20	Octal D-Type Transparent Latch	✓	✓	✓	SDAS048D
SN74AS574	20	Octal D-Type Flip-Flop	✓	✓	✓	SDAS165B
SN74AS575	24	Octal D-Type Flip-Flop	✓	✓	✓	SDAS165B
SN74AS576	20	Octal D-Type Flip-Flop	✓	✓	✓	SDAS065B
SN74AS639	20	Octal Bus Transceiver		✓	✓	SDAS123A
SN74AS640	20	Octal Bus Transceiver	✓	✓	✓	SDAS122A
SN74AS641	20	Octal Bus Transceiver		✓	✓	SDAS300
SN74AS645	20	Octal Bus Transceiver	✓	✓	✓	SDAS278
SN74AS646	24	Octal Registered Bus Transceiver	✓	✓	✓	SDAS039F
SN74AS648	24	Octal Registered Bus Transceiver		✓	✓	SDAS039F
SN74AS651	24	Octal Registered Bus Transceiver	✓	✓	✓	SDAS066F
SN74AS652	24	Octal Registered Bus Transceiver	✓	✓	✓	SDAS066F
SN74AS756	20	Octal Buffer/Driver	✓	✓	✓	SDAS040B
SN74AS757	20	Octal Buffer/Driver		✓	✓	SDAS040B
SN74AS760	20	Octal Buffer/Driver	✓	✓	✓	SDAS141A
SN74AS804B	20	Hex 2-Input NAND Gate	✓	✓	✓	SDAS022C
SN74AS805B	20	Hex 2-Input NOR Gate	✓	✓	✓	SDAS023C
SN74AS808B	20	Hex 2-Input Positive-AND Gate	✓	✓	✓	SDAS018C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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DBV = 5 pins
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SSOP (shrink small-outline package)
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DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
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PCA, PZ = 100 pins (FB only)
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schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

DEVICE SELECTION GUIDE

AS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN74AS821A	24	10-Bit Bus-Interface Flip-Flop	✓	✓	✓	SDAS230A
SN74AS823A	24	9-Bit Bus-Interface Flip-Flop	✓	✓	✓	SDAS231A
SN74AS825A	24	8-Bit Bus-Interface Flip-Flop	✓	✓	✓	SDAS020B
SN74AS832B	20	Hex 2-Input OR Gate	✓	✓	✓	SDAS017C
SN74AS867	24	8-Bit Synchronous Up/Down Binary Counter	✓	✓	✓	SDAS115C
SN74AS869	24	8-Bit Synchronous Up/Down Binary Counter	✓	✓	✓	SDAS115C
SN74AS873A	24	Dual 4-Bit D-Type Flip-Flop	✓	✓	✓	SDAS036D
SN74AS874	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	✓	✓	✓	SDAS061C
SN74AS876	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop		✓	✓	SDAS061C
SN74AS885	24	8-Bit Magnitude Comparator	✓	✓	✓	SDAS236A
SN74AS1000A	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	SDAS056B
SN74AS1004A	14	Hex Inverting Buffer	✓	✓	✓	SDAS074B
SN74AS1008A	14	Quad 2-Input Positive-AND Gate		✓	✓	SDAS071B
SN74AS1032A	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	SDAS072B
SN74AS1034A	14	Hex Noninverting Buffer	✓	✓	✓	SDAS053B
SN74AS1804	20	Hex 2-Input NAND Gate		✓		SDAS042C
SN74AS1805	20	Hex 2-Input NOR Gate		✓		SDAS043C
SN74AS1808	20	Hex 2-Input Positive-AND Gate		✓		SDAS044C
SN74AS1832	20	Hex 2-Input Positive-OR Gate		✓		SDAS045C
SN74AS4374B	20	8-Bit Dual-Rank Synchronizer		✓	✓	SDAS109D

commercial package description and availability

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SOIC (small-outline integrated circuit)
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TSSOP (thin shrink small-outline package)
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DGV = 14/16/20/24/48/56 pins
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TQFP (plastic thin quad flat package)
PAH = 52 pins
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MIL – See page 4–3 for military package description and availability

BCT
BiCMOS Technology

BCT is a family of 8-, 9-, and 10-bit drivers, latches, transceivers, and registered transceivers. Designed specifically for bus-interface applications, BCT offers TTL I/O with high speeds, 64-mA output drive, and very low power in the disabled mode. Over 50 BCT functions are in production now.

A family of fast, high-drive bus-interface functions that provides the incident-wave switching required by large backplane applications has been incorporated into the BCT offering. Designed specifically to ensure incident-wave switching down to 25 Ω, the devices in the BiCMOS low-impedance driver family can maximize the speed and reliability of heavily loaded systems. Each device in this series delivers 188 mA of I_{OL} drive current.

Also included in our BCT family is a series of memory drivers. These devices incorporate a series-damping resistor to reduce overshoot and undershoot that can occur in memory-driving applications.

For BCT data sheets, see the 1994 *BCT BiCMOS Bus-Interface Logic Data Book*, literature number SCBD001B.

DEVICE SELECTION GUIDE

BCT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74BCT125A	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓		SCBS032E
SN74BCT126A	14	Quad Bus Buffer Gate (OE)	✓	✓	✓		SCBS252A
SN74BCT240	20	Octal Buffer/Driver	✓	✓	✓	✓	SCBS004E
SN74BCT241	20	Octal Buffer/Driver	✓	✓	✓	✓	SCBS005D
SN74BCT244	20	Octal Buffer/Driver	✓	✓	✓	✓	SCBS006E
SN74BCT245	20	Octal Bus Transceiver	✓	✓	✓	✓	SCBS013F
SN74BCT373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	SCBS016C
SN74BCT374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	SCBS019B
SN74BCT540A	20	Octal Buffer/Driver	✓	✓	✓		SCBS012D
SN74BCT541A	20	Octal Buffer/Driver	✓	✓	✓		SCBS011D
SN74BCT543	24	Octal Registered Bus Transceiver	✓	✓	✓		SCBS026C
SN74BCT574	20	Octal D-Type Flip-Flop	✓			✓	SCBS074B
SN74BCT623	20	Octal Bus Transceiver	✓	✓	✓		SCBS020A
SN74BCT640	20	Octal Bus Transceiver	✓	✓	✓		SCBS025C
SN74BCT646	24	Octal Registered Bus Transceiver	✓	✓	✓		SCBS037C
SN74BCT652	24	Octal Registered Bus Transceiver	✓	✓	✓		SCBS038A
SN74BCT756	20	Octal Buffer/Driver		✓	✓		SCBS056A
SN74BCT760	20	Octal Buffer/Driver	✓	✓	✓		SCBS034B
SN74BCT2240	20	Octal Buffer/Driver With Series Resistors	✓	✓	✓	✓	SCBS030D
SN74BCT2244	20	Octal Buffer/Driver With Series Resistors	✓	✓	✓		SCBS017C
SN74BCT2245	20	Octal Bus Transceiver With Series Resistors		✓	✓	✓	SCBS102B
SN74BCT2827C	24	10-Bit Buffer/Driver With Series Resistors	✓	✓	✓		SCBS007E
SN74BCT2828B	24	10-Bit Buffer/Driver With Series Resistors		✓	✓		SCBS058A
SN74BCT2953	24	Octal Bus Registered Transceiver		✓	✓		SCBS105B
SN74BCT25245	24	25-Ω Octal Bus Transceiver		✓	✓		SCBS053B
SN74BCT29821	24	10-Bit Bus-Interface Flip-Flop		✓	✓		SCBS021D
SN74BCT29823	24	9-Bit Bus-Interface Flip-Flop		✓	✓		SCBS018D
SN74BCT29827B	24	10-Bit Buffer/Driver		✓	✓		SCBS008C
SN74BCT29834	24	8-to-9-Bit Parity Bus Transceiver		✓	✓		SCBS256
SN74BCT29841	24	10-Bit Bus-Interface D-Type Latch		✓	✓		SCBS024C

commercial package description and availability

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QSOP (quarter-size outline package)
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SOIC (small-outline integrated circuit)
D = 8/14/16 pins
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TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
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TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74BCT29843	24	9-Bit Bus-Interface D-Type Latch		✓	✓		SCBS022C
SN74BCT29854	24	8-to-9-Bit Parity Bus Transceiver		✓	✓		SCBS257
SN74BCT29863B	24	9-Bit Bus Transceiver		✓	✓		SCBS015D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

64BCT
64-Series BiCMOS Technology

The 64BCT family offers all the features found in TI's standard BCT family. In addition, the family is characterized for operation from –40°C to 85°C and incorporates circuitry to protect the device in live-insertion applications.

For 64BCT data sheets, see the 1994 *BCT BiCMOS Bus-Interface Logic Data Book*, literature number SCBD001B.

DEVICE SELECTION GUIDE

64BCT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY PDIP	AVAILABILITY SOIC	LITERATURE REFERENCE
SN64BCT125A	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	SCBS052B
SN64BCT126A	14	Quad Bus Buffer Gate (OE)	✓	✓	SCBS051B
SN64BCT240	20	Octal Buffer/Driver	✓	✓	SCBS049A
SN64BCT241	20	Octal Buffer/Driver	✓	✓	SCBS046B
SN64BCT244	20	Octal Buffer/Driver	✓	✓	SCBS027A
SN64BCT245	20	Octal Bus Transceiver	✓	✓	SCBS040A
SN64BCT306	8	2-Bit Buffer/Driver	✓	✓	SCBS048B
SN64BCT541A	20	Octal Buffer/Line Driver	✓	✓	SCBS031B
SN64BCT757	20	Octal Buffer/Driver	✓	✓	SCBS479
SN64BCT25244	24	25-Ω Octal Buffer/Driver		✓	SCBS477
SN64BCT25245	24	25-Ω Octal Bus Transceiver	✓	✓	SCBS060A
SN64BCT29828B	24	10-Bit Buffer/Driver	✓	✓	SCBS478

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

BTA
Bus-Termination Arrays

The BTA family from TI offers a space-saving, efficient, and effective solution to bus-termination requirements. In high-speed digital systems with long transmission lines, reflecting waves on the line can cause voltage undershoots and overshoots that lead to malfunctions at the driven input. A BTA is a series of diodes that clamps a signal on a bus or any other signal trace using high-frequency logic to eliminate overshoot and undershoot problems.

For BTA data sheets, see the 1994 *F Logic Data Book*, literature number SDFD001B, or contact the Product Information Center at (972) 644-5580.

DEVICE SELECTION GUIDE

BTA

DEVICE	NO. PINS	FUNCTION	AVAILABILITY PDIP	AVAILABILITY SOIC	LITERATURE REFERENCE
SN74ACT1071	16	10-Bit Bus-Termination Array		✓	SCAS192
SN74ACT1073	20	16-Bit Bus-Termination Array		✓	SCAS193
SN74F1016	20	16-Bit Schottky Barrier Diode R-C Bus-Termination Array		✓	SDFS093
SN74F1056	16	8-Bit Schottky Barrier Diode Bus-Termination Array		✓	SDFS085
SN74S1050	16	12-Bit Schottky Barrier Diode Bus-Termination Array	✓	✓	SDLS015A
SN74S1051	16	12-Bit Schottky Barrier Diode Bus-Termination Array	✓	✓	Call
SN74S1052	20	16-Bit Schottky Barrier Diode Bus-Termination Array	✓	✓	SDLS016A
SN74S1053	20	16-Bit Schottky Barrier Diode Bus-Termination Array	✓	✓	SDLS017
SN74S1056	16	8-Bit Schottky Barrier Diode Bus-Termination Array		✓	SDLS019B

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

BTL/FB+
Backplane Transceiver Logic

The FB series devices are used for high-speed bus applications and are fully compatible with the IEEE 1194.1-1991 (BTL) and IEEE 896-1991 (Futurebus+) standards. These transceivers are available in 7-, 8-, 9-, and 18-bit versions with TTL and BTL translation in performance below 5 ns. Other features include drive up to 100 mA and bias pins for live-insertion applications.

For BTL/FB+ data sheets, see the 1997 *GTL, BTL, and ETL Logic Data Book*, literature number SCED004.

DEVICE SELECTION GUIDE

BTL/FB+

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	QFP	TQFP	
SN74FB1650	100	18-Bit TTL/BTL Universal Storage Transceiver			✓	SCBS178I
SN74FB1651	100	17-Bit TTL/BTL Universal Storage Transceiver With Buffered Clock Lines			✓	SCBS177I
SN74FB1653	100	17-Bit LVTTL-to-BTL Universal Storage Transceiver With Buffered Clock Lines			✓	SCBS702A
SN74FB2031	52	9-Bit TTL/BTL Address/Data Transceiver	✓	✓		SCBS176H
SN74FB2032	52	9-Bit TTL/BTL Competition Transceiver		✓		SCBS175F
SN74FB2033A	52	8-Bit TTL/BTL Registered Transceiver	✓	✓		SCBS174H
SN74FB2040	52	8-Bit TTL/BTL Transceiver	✓	✓		SCBS173G
SN74FB2041A	52	7-Bit TTL/BTL Transceiver		✓		SCBS172G

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

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MIL – See page 4–3 for military package description and availability

CBT
Crossbar Technology

In today's computing market, power and speed are two of the main concerns. CBT can address both of these issues in bus-interface applications. CBT enables a bus-interface device to function as a very fast bus switch, effectively isolating buses when the switch is open and offering very little propagation delay when the switch is closed. These devices can function as high-speed bus interfaces between computer-system components such as the central processing unit (CPU) and memory. CBT devices also can be used as 5-V to 3.3-V translators, allowing designers to mix 5-V or 3.3-V components in the same system.

The CBT devices are available in advanced packaging such as shrink small-outline packages (SSOP), thin shrink small-outline packages (TSSOP), and thin very small-outline packages (TVSOP) for reduced board area.

For CBT data sheets, see the 1998 *CBT (5-V) and CBTLV (3.3-V) Bus Switches Data Book*, literature number SCDD001B.

DEVICE SELECTION GUIDE

CBT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	SOIC	QSOP	SSOP	TSSOP	TVSOP	SOT	
SN74CBT1G125	5	Single FET Bus Switch							✓	SCDS046B
SN74CBT1G384	5	Single FET Bus Switch							+	Call
SN74CBTD1G384	5	Single FET Bus Switch With Level Shifting							+	Call
SN74CBTS1G384	5	Single FET Bus Switch With Clamping Diodes							+	Call
SN74CBT3125	14, 16	Quad FET Bus Switch		✓	✓	✓	✓			SCDS021E
SN74CBT3126	14	Quad FET Bus Switch		✓	✓	✓	✓			SCDS020E
SN74CBT3244	20	Dual 4-Bit FET Bus Switch With '244 Pinout		✓	✓	✓	✓	✓		SCDS001H
SN74CBT3245A	20	8-Bit FET Bus Switch With '245 Pinout		✓	✓	✓	✓	✓		SCDS002J
SN74CBT3251	16	8-to-1 FET Multiplexer/Data Selector		✓		✓	✓			SCDS019E
SN74CBT3253	16	Dual 4-Bit to 1-Bit FET Multiplexer/Demultiplexer		✓	✓	✓	✓	+		SCDS018I
SN74CBT3257	16	Quad 2-Bit to 1-Bit FET Multiplexer/Demultiplexer		✓	✓	✓	✓	+		SCDS017I
SN74CBT3306	8	Dual FET Bus Switch		✓			✓			SCDS016E
SN74CBTD3306	8	Dual FET Bus Switch With Level Shifting		✓			✓			SCDS030F
SN74CBTS3306	8	Dual FET Bus Switch With Clamping Diodes		✓			✓			SCDS029C
SN74CBT3345	20	8-Bit FET Bus Switch		✓		✓	✓			SCDS027D
SN74CBT3383	24	10-Bit FET Bus-Exchange Switch	✓	✓	✓	✓	✓			SCDS003I
SN74CBTH3383	24	10-Bit FET Bus-Exchange Switch With Bus Hold		+		+	+			SCDS023F
SN74CBT3384A	24	10-Bit FET Bus Switch		✓	✓	✓	✓	+		SCDS004I
SN74CBTD3384	24	10-Bit FET Bus Switch With Level Shifting	✓	✓	✓	✓	✓	✓		SCDS025J
SN74CBTS3384	24	10-Bit FET Bus Switch With Clamping Diodes		✓	✓	✓	✓			SCDS024G
SN74CBT3386	24	10-Bit FET Bus-Exchange Switch With Extended Voltage Range		+		+	+			SCDS022F
SN74CBT3861	24	10-Bit FET Bus Switch		+	+		+	+		SCDS061
SN74CBTD3861	24	10-Bit FET Bus Switch With Level Shifting		+	+		+	+		Call
SN74CBT6800	24	10-Bit FET Bus Switch With Precharged Outputs for Live Insertion		✓		✓	✓			SCDS005I

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
+ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	SOIC	QSOP	SSOP	TSSOP	TVSOP	SOT	
SN74CBT16209A	48	18-Bit FET Bus-Exchange Switch	★			✓	✓	✓		SCDS006K
SN74CBT16210	48	20-Bit FET Bus Switch With Flow-Through Pinout				✓	✓	✓		SCDS033C
SN74CBTD16210	48	20-Bit FET Bus Switch With Level Shifting				✓	✓	✓		SCDS049C
SN74CBT16211A	56	24-Bit FET Bus-Exchange Switch				✓	✓	✓		SCDS028H
SN74CBTD16211	56	24-Bit FET Bus-Exchange Switch With Level Shifting				✓	✓	✓		SCDS048C
SN74CBTH16211	56	24-Bit FET Bus-Exchange Switch With Bus Hold				✢	✢	✢		Call
SN74CBTS16211	56	24-Bit FET Bus-Exchange Switch With Clamping Diodes				✢	✢	✢		SCDS050B
SN74CBT16212A	56	24-Bit FET Bus-Exchange Switch	✓			✓	✓	✓		SCDS007L
SN74CBTH16212	56	24-Bit FET Bus-Exchange Switch With Bus Hold				✢	✢	✢		Call
SN74CBTS16212	56	24-Bit FET Bus-Exchange Switch With Clamping Diodes				✓	✓	✓		SCDS036B
SN74CBT16213	56	24-Bit FET Bus-Exchange Switch				✓	✓			SCDS026F
SN74CBTS16213	56	24-Bit FET Bus-Exchange Switch With Clamping Diodes				✢	✢	✢		SCDS051A
SN74CBT16214	56	12-Bit 3-to-1 FET Bus-Select Switch				✓	✓			SCDS008I
SN74CBT16232	56	16-Bit to 32-Bit Synchronous FET Multiplexer				✓	✓			SCDS009H
SN74CBT16233	56	16-Bit to 32-Bit FET Multiplexer/Demultiplexer				✓	✓			SCDS010F
SN74CBT16244	48	16-Bit FET Bus Switch	✢			✓	✓	✓		SCDS031F
SN74CBT16292	56	12-Bit 1-to-2 FET Multiplexer/Demultiplexer				✓	✓	✓		SCBS053B
SN74CBT16390	56	16-Bit to 32-Bit FET Multiplexer/Demultiplexer				✓	✓	✓		SCDS035B
SN74CBT162292	56	12-Bit 1-to-2 FET Multiplexer/Demultiplexer With Series-Damping Resistor				✓	✓	✓		SCDS052C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

CBTLV
Low-Voltage Crossbar Technology

TI has developed the SN74CBTLV family of 3.3-V bus switches to complement its existing SN74CBT family of 5-V bus switches. TI is the first to offer these devices designed for 3.3-V in its continuing drive to provide low-voltage solutions.

CBTLV devices can be used in multiprocessor systems as fast bus connections, bus-exchange switches for crossbar systems, ping-pong memory connections, or bus-byte swapping. They also can be used to replace relays, improving connect/disconnect speed and eliminating relay-reliability problems. The CBTLV family, designed to operate at 3.3 V, furthers the goal of an integrated system operating with LVTTL voltages.

The CBTLV devices are available in industry-leading packaging options such as the shrink small-outline package (SSOP), thin small-outline package (TSSOP), and thin very small-outline package (TVSOP) for reduced board area.

For CBTLV data sheets, see the 1998 *CBT (5-V) and CBTLV (3.3-V) Bus Switches Data Book*, literature number SCDD001B.

DEVICE SELECTION GUIDE

CBTLV

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			SOIC	SOT	SSOP	TSSOP	TVSOP	
SN74CBTLV1G125	5	Low-Voltage Single FET Bus Switch		✢				SCDS057A
SN74CBTLV3125	14	Low-Voltage Quad FET Bus Switch	✢			✢	✢	SCDS037B
SN74CBTLV3126	14	Low-Voltage Quad FET Bus Switch	✢			✢	✢	SCDS038B
SN74CBTLV3245	20	Low-Voltage 8-Bit FET Bus Switch With '245 Pinout	✓			✓	✓	SCDS034F
SN74CBTLV3251	16	Low-Voltage 8-to-1 FET Multiplexer/Data Selector	✢			✢	✢	SCDS054A
SN74CBTLV3253	16	Low-Voltage Dual 4-Bit to 1-Bit FET Multiplexer/Demultiplexer	✢			✢	✢	SCDS039B
SN74CBTLV3257	16	Low-Voltage Quad 2-Bit to 1-Bit FET Multiplexer/Demultiplexer	✢			✢	✢	SCDS040B
SN74CBTLV3383	24	Low-Voltage 10-Bit FET Bus-Exchange Switch	✢			✢	✢	SCDS047A
SN74CBTLV3384	24	Low-Voltage 10-Bit FET Bus Switch	✢			✢	✢	SCDS059A
SN74CBTLV3861	24	Low-Voltage 10-Bit FET Bus Switch	✢			✢		SCDS041B
SN74CBTLV16210	48	Low-Voltage 20-Bit FET Bus Switch With Flow-Through Pinout			✢	✢	✢	SCDS042B
SN74CBTLV16211	56	Low-Voltage 24-Bit FET Bus-Exchange Switch			✢	✢	✢	SCDS043B
SN74CBTLV16212	56	Low-Voltage 24-Bit FET Bus-Exchange Switch			✢	✢	✢	SCDS044B
SN74CBTLV16235	56	Low-Voltage 16-Bit to 36-Bit Synchronous FET Multiplexer			✢	✢	✢	SCDS060A
SN74CBTLV16292	56	Low-Voltage 12-Bit 1-to-2 FET Multiplexer/Demultiplexer			✢	✢	✢	SCDS055A
SN74CBTLV16390	56	Low-Voltage 16-Bit 1-to-2 FET Bus Switch			✢	✢	✢	Call
SN74CBTLV16800	48	Low-Voltage 20-Bit FET Bus Switch With Precharged Outputs			✢	✢	✢	SCDS045B
SN74CBTLV162292	56	Low-Voltage 12-Bit 1-to-2 FET Multiplexer/Demultiplexer With Damping Resistors			✢	✢	✢	SCDS056A

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
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PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

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MIL – See page 4–3 for military package description and availability

74F
Fast Logic

74F logic is a general-purpose family of high-speed advanced bipolar logic. TI provides over 60 functions, including gates, buffers/drivers, bus transceivers, flip-flops, latches, counters, multiplexers, and demultiplexers in the 74F logic family.

For 74F data sheets, see the 1994 *F Logic Data Book*, literature number SDFD001B.

DEVICE SELECTION GUIDE

74F

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74F00	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓		SDFS035A
SN74F02	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓		SDFS036A
SN74F04	14	Hex Inverter	✓	✓	✓		SDFS037A
SN74F08	14	Quad 2-Input Positive-AND Gate		✓	✓		SDFS038A
SN74F10	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓		SDFS039A
SN74F11	14	Triple 3-Input Positive-AND Gate	✓	✓	✓		SDFS040A
SN74F20	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓		SDFS041A
SN74F21	14	Dual 4-Input Positive-AND Gate	✓	✓	✓		SDFS006A
SN74F27	14	Triple 3-Input Positive-NOR Gate	✓	✓	✓		SDFS042A
SN74F30	14	8-Input Positive-NAND Gate	✓	✓	✓		SDFS043A
SN74F32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓		SDFS044A
SN74F38	14	Quad 2-Input Positive-NAND Gate		✓	✓		SDFS013A
SN74F74	14	Dual D-Type Flip-Flop	✓	✓	✓		SDFS046A
SN74F86	14	Quad 2-Input Exclusive-OR Gate		✓	✓		SDFS019B
SN74F109	16	Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flop With Clear and Preset	✓	✓	✓		SDFS047A
SN74F112	14	Dual J-K Negative-Edge-Triggered Flip-Flop With Clear and Preset		✓	✓		SDFS048A
SN74F125	14	Quad Bus Buffer Gate ($\overline{OE}$)		✓	✓		SDFS016A
SN74F126	14	Quad Bus Buffer Gate (OE)		✓	✓		SDFS017A
SN74F138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓		SDFS051B
SN74F151B	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS023A
SN74F153	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS052A
SN74F157A	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS053A
SN74F158A	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS054A
SN74F161A	16	4-Bit Synchronous Binary Counter		✓	✓		SDFS056A
SN74F163A	16	4-Bit Synchronous Binary Counter		✓	✓		SDFS088
SN74F169	16	4-Bit Synchronous Up/Down Binary Counter		✓	✓		SDFS089
SN74F174A	16	Hex D-Type Flip-Flop With Clear		✓	✓		SDFS029B
SN74F175	16	Quad D-Type Flip-Flop With Clear	✓	✓	✓		SDFS058A
SN74F240	20	Octal Buffer/Driver	✓	✓	✓	✓	SDFS061A
SN74F241	20	Octal Buffer/Driver	✓	✓	✓		SDFS090

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74F243	14	Quad Bus Transceiver		✓	✓		SDFS086
SN74F244	20	Octal Buffer/Driver	✓	✓	✓	✓	SDFS063A
SN74F245	20	Octal Bus Transceiver	✓	✓	✓	✓	SDFS010A
SN74F251B	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS066A
SN74F253	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS064A
SN74F257	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS065A
SN74F258	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDFS067A
SN74F260	14	Dual 5-Input Positive-NOR Gate		✓	✓		SDFS012A
SN74F280B	14	9-Bit Parity Generator/Checker	✓	✓	✓		SDFS008A
SN74F283	16	4-Bit Binary Full Adder With Fast Carry	✓	✓	✓		SDFS069A
SN74F299	20	8-Bit Universal Shift/Storage Register	✓	✓	✓		SDFS071A
SN74F373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	SDFS076A
SN74F374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	SDFS077A
SN74F377A	20	Octal D-Type Flip-Flop With Clock Enable		✓	✓		SDFS018D
SN74F521	20	8-Bit Identity Comparator	✓	✓	✓		SDFS091
SN74F541	20	Octal Buffer/Driver	✓	✓	✓		SDFS021A
SN74F543	24	Octal Registered Bus Transceiver		✓	✓	✓	SDFS025B
SN74F573	20	Octal D-Type Transparent Latch	✓	✓	✓		SDFS011A
SN74F574	20	Octal D-Type Flip-Flop		✓	✓		SDFS005A
SN74F623	20	Octal Bus Transceiver	✓	✓	✓		SDFS087
SN74F2244	20	Octal Buffer/Driver With Series Resistors		✓	✓	✓	SDFS095B
SN74F2245	20	Octal Bus Transceiver With Series-Damping Resistors		✓	✓		SDFS099
SN74F2373	20	Octal D-Type Transparent Latch With Series Resistors		✓	✓	✓	SDFS100

commercial package description and availability

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DBV = 5 pins
DCK = 5 pins

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DB = 14/16/20/24/28/30/38 pins
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DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

FIFO
First-In, First-Out Memories

TI has an extended product offering of Advanced CMOS (ACT), Advanced BiCMOS (ABT), and Advanced Low-Voltage CMOS (ALVC) FIFOs. The FIFO product family includes clocked unidirectional and bidirectional FIFOs offered in 64-bit to 2K memory depths and 1-bit to 36-bit widths.

TI's application-specific FIFOs are specially designed for use in telecommunications, DSP, internetworking systems, and high-bandwidth computing. These devices include features such as parity generate and check, retransmit, bus matching, byte swapping, bypass mode, and microprocessor-like control interface.

Application-specific FIFOs, in addition to TI's Widebus™ FIFO products, offer space-saving surface-mount packaging and multiple-speed sorts for ease of design.

DEVICE SELECTION GUIDE

FIFO

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	PLCC	QFP	TQFP	
36-Bit Clocked FIFOs										
SN74ABT3611	132, 120	64 × 36 Clocked FIFO						✓	✓	SCBS127E
SN74ABT3612	132, 120	64 × 36 × 2 Clocked Bidirectional FIFO						✓	✓	SCBS129G
SN74ABT3613	132, 120	64 × 36 Clocked FIFO						✓	✓	SCBS128F
SN74ABT3614	132, 120	64 × 36 × 2 Clocked Bidirectional FIFO	✓					✓	✓	SCBS126G
SN74ACT3622	132, 120	256 × 36 × 2 Clocked Bidirectional FIFO						✓	✓	SCAS247D
SN74ACT3631	132, 120	512 × 36 Clocked FIFO						✓	✓	SCAS246G
SN74ACT3632	132, 120	512 × 36 × 2 Clocked Bidirectional FIFO	✓					✓	✓	SCAS224D
SN74ACT3641	132, 120	1K × 36 Clocked FIFO	✓					✓	✓	SCAS338C
SN74ACT3651	132, 120	2K × 36 Clocked FIFO						✓	✓	SCAS439C
18-Bit Strobed FIFOs										
SN74ACT7814	56	64 × 18 Strobed FIFO				✓				SCAS209C
SN74ACT7806	56	256 × 18 Strobed FIFO				✓				SCAS438C
SN74ACT7804	56	512 × 18 Strobed FIFO				✓				SCAS204C
SN74ABT7820	80, 80	512 × 18 × 2 Strobed Bidirectional FIFO						✓	✓	SCAS206D
SN74ACT7802	68, 80	1K × 18 Strobed FIFO					✓		✓	SCAS187D
SN74ALVC7814	56	3.3-V 64 × 18 Strobed FIFO				✓				SCAS592A
SN74ALVC7806	56	3.3-V 256 × 18 Strobed FIFO				✓				SCAS591A
SN74ALVC7804	56	3.3-V 512 × 18 Strobed FIFO				✓				SCAS437E
18-Bit Clocked FIFOs										
SN74ACT7813	56	64 × 18 Clocked FIFO				✓				SCAS199B
SN74ACT7805	56	256 × 18 Clocked FIFO				✓				SCAS201B
SN74ACT7803	56	512 × 18 Clocked FIFO				✓				SCAS191C
SN74ABT7819	80, 80	512 × 18 × 2 Clocked Bidirectional FIFO						✓	✓	SCBS125F
SN74ACT7811	68, 80	1K × 18 Clocked FIFO					✓		✓	SCAS151C
SN74ACT7881	68, 80	1K × 18 Clocked FIFO	✓				✓		✓	SCAS227E
SN74ACT7882	68, 80	2K × 18 Clocked FIFO					✓		✓	SCAS445C
SN74ALVC7813	56	3.3-V 64 × 18 Clocked FIFO				✓				SCAS594A
SN74ALVC7805	56	3.3-V 256 × 18 Clocked FIFO				✓				SCAS593A
SN74ALVC7803	56	3.3-V 512 × 18 Clocked FIFO				✓				SDAS436D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
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N = 14/16/20 pins
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PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

FIFO

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	PLCC	QFP	TQFP	
9-Bit FIFOs										
SN74ACT2235	44, 64	1K × 9 × 2 Asynchronous Bidirectional FIFO					✓		✓	SCAS148E
SN74ACT7807	44, 64	2K × 9 Clocked FIFO					✓		✓	SCAS200D
SN74ACT7808	44, 64	2K × 9 Strobed FIFO					✓		✓	SCAS205D
1-Bit Telecom FIFOs										
SN74ACT2226	24	64 × 1 Clocked FIFO			✓					SCAS219C
SN74ACT2227	28	64 × 1 Clocked FIFO			✓					SCAS220C
SN74ACT2228	24	256 × 1 Clocked FIFO			✓					SCAS219C
SN74ACT2229	28	256 × 1 Clocked FIFO			✓					SCAS220C
Various-Width FIFOs										
SN74ACT3638	132, 120	512 × 32 × 2 Clocked Bidirectional FIFO						✓	✓	SCAS228D
SN74ALS232B	16, 16, 20	16 × 4 Asynchronous FIFO, 40 MHz		✓	✓		✓			SCAS251B
SN74LS224A	16	16 × 4 Synchronous Strobed FIFO, 10 MHz	✓	✓						SDLS023B
SN74ALS236	16, 20	64 × 4 Asynchronous FIFO, 30 MHz		✓	✓		✓			SDAS107C
SN74S225	20	16 × 5 Asynchronous FIFO, 10 MHz		✓						SDLS207B
SN74ALS233B	20	16 × 5 Asynchronous FIFO, 40 MHz		✓	✓		✓			SCAS253B

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
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PLCC (plastic leaded chip carrier)
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QFP (quad flat package)
RC = 52 pins (FB only)
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PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

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MIL – See page 4–3 for military package description and availability

GTL
Gunning-Transceiver-Logic Technology

GTL technology is a new reduced-voltage switching standard that provides high-speed, point-to-point communications with low power dissipation. TI offers GTL/TTL translators to interface with the TTL-based subsystems. This enables designers to use the GTL switching standards for speed-sensitive subsystems and to use the translators to interface with the rest of the system.

GTL devices have innovative circuitry, such as bus hold on the inputs to eliminate the need for external pullup resistors for floating inputs, which reduces power, cost, and board-layout time. Output edge-rate control (OEC™) is offered on the outputs to reduce electromagnetic interference (EMI) caused by the high frequencies of GTL.

Industry-leading packaging such as the shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP) is available for higher performance and reduced board space.

For GTL data sheets, see the 1997 *GTL, BTL, and ETL Logic Data Book*, literature number SCED004.

DEVICE SELECTION GUIDE

GTL

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	SSOP	TSSOP	
SN74GTL1655	64	16-Bit LVTTL-to-GTL Universal Bus Transceiver With Live Insertion			✓	SCBS696C
SN74GTL16612	56	18-Bit Universal Bus Transceiver With OEC™	✓	✓	✓	SCBS480G
SN74GTL16616	56	17-Bit Universal Bus Transceiver With Buffered Clock Outputs and OEC™	✢	✓	✓	SCBS481D
SN74GTL16622A	64	18-Bit LVTTL-to-GTL/GTL+ Registered Transceiver With 5-V Tolerance and OEC™			✓	SCBS673B
SN74GTL16923	64	18-Bit LVTTL-to-GTL/GTL+ Registered Transceiver With 5-V Tolerance and OEC™			✓	SCBS674D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

HC/HCT
High-Speed CMOS Logic

For low-power logic requirements, TI offers a full family of HC/HCT logic. Over 100 device types are available, including gates, latches, flip-flops, buffers/drivers, counters, multiplexers, transceivers, and registered transceivers.

The HC family offers CMOS-compatible inputs and the HCT family offers TTL-compatible inputs.

For HC/HCT data sheets, see the 1997 *HC/HCT Logic High-Speed CMOS Data Book*, literature number SCLD001D.

DEVICE SELECTION GUIDE

HC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74HC00	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	✓	✓	SCLS181B
SN74HC02	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓	✓	✓	SCLS076B
SN74HC03	14	Quad 2-Input Positive-NAND Gate With Open-Drain Outputs	✓	✓	✓			SCLS077B
SN74HC04	14	Hex Inverter	✓	✓	✓	✓	✓	SCLS078B
SN74HCU04	14	Unbuffered Hex Inverter	✓	✓	✓			SCLS079B
SN74HC05	14	Hex Inverter With Open-Drain Outputs	✓	✓	✓	✓	✓	SCLS080B
SN74HC08	14	Quad 2-Input Positive-AND Gate	✓	✓	✓	✓	✓	SCLS081B
SN74HC10	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓			SCLS083B
SN74HC11	14	Triple 3-Input Positive-AND Gate	✓	✓	✓			SCLS084B
SN74HC14	14	Hex Inverter With Schmitt-Trigger	✓	✓	✓	✓	✓	SCLS085B
SN74HC20	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓			SCLS086C
SN74HC21	14	Dual 4-Input Positive-AND Gate	✓	✓	✓			SCLS087C
SN74HC27	14	Triple 3-Input Positive-NOR Gate	✓	✓	✓			SCLS088B
SN74HC32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	✓	✓	SCLS200B
SN74HC42	16	4-to-10 BCD to Decimal Decoder	✓	✓	✓			SCLS091B
SN74HC74	14	Dual D-Type Flip-Flop	✓	✓	✓	✓	✓	SCLS094B
SN74HC86	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓	✓		SCLS100B
SN74HC109	16	Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flop	✓	✓	✓			SCLS098
SN74HC112	16	Dual J-K Negative-Edge-Triggered Flip-Flop	✓	✓	✓			SCLS099B
SN74HC125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓	✓	✓	SCLS104B
SN74HC126	14	Quad Bus Buffer Gate (OE)	✓	✓	✓	✓	✓	SCLS103B
SN74HC132	14	Quad 2-Input Positive-NAND Gate With Schmitt-Trigger Inputs	✓	✓	✓	✓	✓	SCLS034C
SN74HC138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	✓	✓	SCLS107C
SN74HC139	16	Dual 2–to-4 Line Decoder/Demultiplexer	✓	✓	✓	✓	✓	SCLS108B
SN74HC148	16	8-to-3 Line Priority Encoder	✓	✓	✓			SCLS109D
SN74HC151	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓	✓		SCLS110C
SN74HC153	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		✓	SCLS112B
SN74HC157	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓			SCLS113B
SN74HC161	16	4-Bit Synchronous Binary Counter	✓	✓	✓			SCLS297A
SN74HC163	16	4-Bit Synchronous Binary Counter	✓	✓	✓			SCLS298A

commercial package description and availability

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PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
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SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74HC164	14, 16	8-Bit Parallel-Out Serial Shift Register	✓	✓	✓			SCLS115B
SN74HC166	16	8-Bit Parallel-Load Shift Register	✓	✓	✓			SCLS117B
SN74HC174	16	Hex D-Type Flip-Flop	✓	✓	✓			SCLS119B
SN74HC175	16	Quad D-Type Flip-Flop With Clear	✓	✓	✓		✓	SCLS299A
SN74HC191	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓			SCLS121B
SN74HC193	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓			SCLS122B
SN74HC240	20	Octal Buffer/Driver	✓	✓	✓	✓		SCLS128B
SN74HC241	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCLS300A
SN74HC244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCLS130B
SN74HC245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	SCLS131B
SN74HC251	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓			SCLS132B
SN74HC253	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓			SCLS133B
SN74HC259	16	8-Bit Addressable Latch	✓	✓	✓	✓	✓	SCLS134B
SN74HC266	14	Quad 2-Input Exclusive-NOR Gate With Open-Drain Outputs		✓	✓			SCLS135C
SN74HC273	20	Octal D-Type Flip-Flop With Clear	✓	✓	✓	✓	✓	SCLS136B
SN74HC365	16	Hex Buffer/Driver	✓	✓	✓			SCLS308B
SN74HC367	16	Hex Buffer/Driver	✓	✓	✓			SCLS309B
SN74HC368	16	Hex Buffer/Driver	✓	✓	✓			SCLS310A
SN74HC373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCLS140B
SN74HC374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓	SCLS141B
SN74HC377	20	Octal D-Type Flip-Flop With Clock Enable	✓	✓	✓			SCLS307A
SN74HC393	14	Dual 4-Bit Binary Counter	✓	✓	✓	✓		SCLS143B
SN74HC534	20	Octal D-Type Flip-Flop	✓	✓	✓			SCLS311A
SN74HC540	20	Octal Buffer/Driver	✓	✓	✓			SCLS007B
SN74HC541	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCLS305A
SN74HC563	20	Octal D-Type Transparent Latch	✓	✓	✓			SCLS145B
SN74HC573A	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCLS147B
SN74HC574	20	Octal D-Type Flip-Flop	✓	✓	✓		✓	SCLS148C
SN74HC590A	16	8-Bit Binary Counter	✓	✓	✓			SCLS039C
SN74HC594	16	8-Bit Shift Register		✓	✓	✓		SCLS040C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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DBB = 80 pins

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PAH = 52 pins
PAG = 64 pins (FB only)
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schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

DEVICE SELECTION GUIDE

HC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74HC595	16	8-Bit Shift Register	✓	✓	✓	✓		SCLS041B
SN74HC623	20	Octal Bus Transceiver		✓	✓			SCLS149B
SN74HC640	20	Octal Bus Transceiver	✓	✓	✓			SCLS303A
SN74HC645	20	Octal Bus Transceiver	✓	✓	✓			SCLS304A
SN74HC646	24	Octal Registered Bus Transceiver		✓	✓			SCLS150B
SN74HC652	24	Octal Registered Bus Transceiver		✓	✓			SCLS151B
SN74HC682	20	8-Bit Magnitude Comparator		✓	✓			SCLS018C
SN74HC684	20	8-Bit Magnitude Comparator		✓	✓			SCLS340A
SN74HC688	20	8-Bit Magnitude Comparator	✓	✓	✓	✓	✓	SCLS010B
SN74HC4020	16	14-Bit Asynchronous Binary Counter	✓	✓	✓			SCLS158B
SN74HC4040	16	12-Bit Asynchronous Binary Counter	✓	✓	✓	✓	✓	SCLS160B
SN74HC4060	16	14-Bit Asynchronous Binary Counter/Oscillator		✓	✓			SCLS161B
SN74HC4066	14	Quad Bilateral Analog Switch		✓	✓	✓	✓	SCLS325B
SN74HC7001	14	Quad 2-Input Positive-AND Gate		✓	✓			SCLS035B
SN74HC7002	14	Quad 2-Input Positive-NOR Gate		✓	✓			SCLS033C
SN74HC7032	14	Quad 2-Input Positive-OR Gate		✓	✓			SCLS036B

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MIL – See page 4–3 for military package description and availability

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			MIL	PDIP	SOIC	SSOP	TSSOP	
SN74HCT00	14	Quad 2-Input Positive-NAND Gate		✓	✓	✓	✓	SCLS062B
SN74HCT02	14	Quad 2-Input Positive-NOR Gate		✓	✓	✓		SCLS065B
SN74HCT04	14	Hex Inverter	✓	✓	✓	✓	✓	SCLS042B
SN74HCT08	14	Quad 2-Input Positive-AND Gate		✓	✓	✓	✓	SCLS063B
SN74HCT14	14	Hex Inverter With Schmitt-Trigger	✓	✓	✓	✓	✓	SCLS225B
SN74HCT32	14	Quad 2-Input Positive-OR Gate		✓	✓	✓	✓	SCLS064B
SN74HCT74	14	Dual D-Type Flip-Flop		✓	✓	✓	✓	SCLS169B
SN74HCT125	14	Quad Bus Buffer Gate ($\overline{OE}$)		✓	✓			SCLS069C
SN74HCT138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	✓	✓	SCLS171C
SN74HCT139	16	Dual 2-to-4 Decoder/Demultiplexer		✓	✓	✓	✓	SCLS066B
SN74HCT157	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓			SCLS071B
SN74HCT240	20	Octal Buffer/Driver	✓	✓	✓			SCLS174B
SN74HCT244	20	Octal Buffer/Driver	✓	✓	✓	✓	✓	SCLS175B
SN74HCT245	20	Octal Bus Transceiver	✓	✓	✓	✓	✓	SCLS020C
SN74HCT257	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓			SCLS072B
SN74HCT273	20	Octal D-Type Flip-Flop With Clear		✓	✓	✓	✓	SCLS068C
SN74HCT373	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓	SCLS009B
SN74HCT374	20	Octal D-Type Flip-Flop	✓	✓	✓	✓		SCLS005B
SN74HCT377	20	Octal D-Type Flip-Flop With Clock Enable		✓	✓			SCLS067C
SN74HCT540	20	Octal Buffer/Driver	✓	✓	✓			SCLS008B
SN74HCT541	20	Octal Buffer/Driver	✓	✓	✓	✓		SCLS306A
SN74HCT573A	20	Octal D-Type Transparent Latch		✓	✓	✓	✓	SCLS176C
SN74HCT574	20	Octal D-Type Flip-Flop		✓	✓		✓	SCLS177C
SN74HCT623	20	Octal Bus Transceiver		✓	✓			SCLS016B
SN74HCT645	20	Octal Bus Transceiver		✓	✓			SCLS019B
SN74HCT646	24	Octal Registered Bus Transceiver		✓	✓			SCLS178B
SN74HCT652	24	Octal Registered Bus Transceiver		✓	✓			SCLS179B

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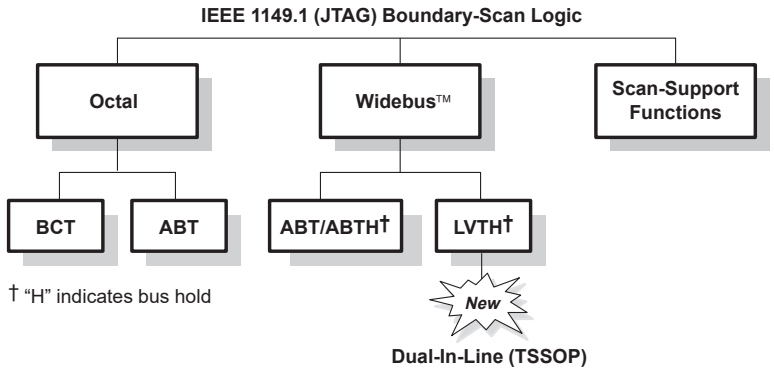
IEEE 1149.1 (JTAG) Boundary-Scan Logic

The IEEE 1149.1 (JTAG) boundary-scan logic family of octal, Widebus™, and scan-support functions incorporates circuitry that allows these devices and the electronic systems in which they are used to be tested without reliance on traditional probing techniques.

Bus-interface logic devices are available in BCT, ABT, and LVT technologies in 8-, 18-, and 20-bit options of the standard buffers, latches, and transceivers. The universal bus transceiver (UBT™), which can functionally replace 50+ standard bus-interface devices, is featured at Widebus widths (18 and 20 bits). Package options for these devices include plastic dual in-line (PDIP), small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin quad flatpack (TQFP). The scan-support functions include devices for controlling the test bus, performing at-speed functional testing, and partitioning the scan path into smaller, more manageable segments.

Over 40 devices, composed of a wide selection of BCT and ABT octals, ABT and LVT Widebus, and scan-support functions, are available. Bus-hold and series-damping resistor features also are available.

For JTAG data sheets, see the 1997 *Boundary-Scan Logic IEEE Std 1149.1 (JTAG)*, literature number SCTD002A.



DEVICE SELECTION GUIDE

IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	PLCC	TQFP	
Widebus™ Devices With Dual-Sided Terminals										
SN74ABT18245A	56	18-Bit Bus Transceiver	✓			✓	✓			SCBS110G
SN74ABT18640	56	18-Bit Inverting Bus Transceiver				✓	✓			SCBS267C
SN74LVT18512	64	18-Bit Universal Bus Transceiver					✓			SCBS711
SN74LVTH18512	64	18-Bit Universal Bus Transceiver					✓			SCBS671B
SN74LVTH182512	64	18-Bit Universal Bus Transceiver					✓			SCBS671B
SN74LVTH18514	64	20-Bit Universal Bus Transceiver					✓			SCBS670C
SN74LVTH182514	64	20-Bit Universal Bus Transceiver					✛			SCBS670C
SN74LVTH18516	64	18-Bit Universal Bus Transceiver					✛			SCBS672B
SN74LVTH182516	64	18-Bit Universal Bus Transceiver					✛			SCBS672B
Widebus™ Devices With Quad-Sided Terminals										
SN74ABTH18502A	64	18-Bit Universal Bus Transceiver	✓						✓	SCBS164E
SN74ABTH182502A	64	18-Bit Universal Bus Transceiver							✓	SCBS164E
SN74ABTH18504A	64	20-Bit Universal Bus Transceiver							✓	SCBS165C
SN74ABTH182504A	64	20-Bit Universal Bus Transceiver							✓	SCBS165C
SN74ABTH18646A	64	18-Bit Registered Bus Transceiver	✓						✓	SCBS166D
SN74ABTH182646A	64	18-Bit Registered Bus Transceiver							✓	SCBS166D
SN74ABTH18652A	64	18-Bit Registered Bus Transceiver							✓	SCBS167D
SN74ABTH182652A	64	18-Bit Registered Bus Transceiver							✓	SCBS167D
SN74LVTH18502A	64	18-Bit Universal Bus Transceiver	✓						✓	SCBS668A
SN74LVTH182502A	64	18-Bit Universal Bus Transceiver							✓	SCBS668A
SN74LVTH18504A	64	20-Bit Universal Bus Transceiver							✓	SCBS667B
SN74LVTH182504A	64	20-Bit Universal Bus Transceiver							✓	SCBS667B
SN74LVTH18646A	64	18-Bit Registered Bus Transceiver	✓						✓	SCBS311D
SN74LVTH182646A	64	18-Bit Registered Bus Transceiver							✓	SCBS311D
SN74LVTH18652A	64	18-Bit Registered Bus Transceiver							✓	SCBS312C
SN74LVTH182652A	64	18-Bit Registered Bus Transceiver							✓	SCBS312C

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	PLCC	TQFP	
Octal Bus-Interface Devices										
SN74ABT8245	24	Octal Bus Transceiver	✓		✓					SCBS124D
SN74ABT8543	28	Octal Registered Bus Transceiver	✓		✓	✓				SCBS120E
SN74ABT8646	28	Octal Registered Bus Transceiver	✓		✓	✓				SCBS123E
SN74ABT8652	28	Octal Registered Bus Transceiver	✓		✓	✓				SCBS122F
SN74ABT8952	28	Octal Registered Bus Transceiver			✓	✓				SCBS121D
SN74BCT8240A	24	Octal Buffer/Driver	✓	✓	✓					SCBS067E
SN74BCT8244A	24	Octal Buffer/Driver	✓	✓	✓					SCBS042E
SN74BCT8245A	24	Octal Bus Transceiver	✓	✓	✓					SCBS043E
SN74BCT8373A	24	Octal D-Type Latch	✓	✓	✓					SCBS044F
SN74BCT8374A	24	Octal D-Type Flip-Flop	✓	✓	✓					SCBS045E
Scan-Support Devices										
SN74LVT8980	24	Embedded Test Bus Controller	✢		✓					SCBS676C
SN74ACT8990	44	Test Bus Controller	✓					✓		SCAS190E
SN74ACT8994	28	Digital Bus Monitor						✓		SCAS196E
SN74ABT8996	24	Addressable Scan Port	✓		✓		✓			SCBS489B
SN74LVT8996	24	Addressable Scan Port	✢		✢		✢			SCBS686
SN74ACT8997	28	Scan-Path Linker	✓	✓	✓					SCAS157D
SN74ACT8999	28	Scan-Path Selector	✓	✓	✓					SCAS158D

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MIL – See page 4–3 for military package description and availability

LS
Low-Power Schottky Logic

With a wide array of functions, TI's LS family continues to offer replacement alternatives for mature systems. This classic line of devices was at the cutting edge of performance when introduced, and continues to deliver excellent value for many of today's designs. As the world leader in logic products, TI is committed to being the last major supplier at every price-performance node.

For LS data sheets, contact the Product Information Center at (972) 644-5580.

DEVICE SELECTION GUIDE

LS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74LS00	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	✓	SDLS025
SN74LS01	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	✓	✓	✓		SDLS026
SN74LS02	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓		SDLS027
SN74LS03	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	✓	✓	✓		SDLS028
SN74LS04	14	Hex Inverter	✓	✓	✓		SDLS029
SN74LS05	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓		SDLS030
SN74LS06	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	✓	SDLS020A
SN74LS07	14	Hex Buffer With Open-Collector Outputs	✓	✓	✓	✓	SDLS021A
SN74LS08	14	Quad 2-Input Positive-AND Gate	✓	✓	✓		SDLS033
SN74LS09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	✓	✓	✓		SDLS034
SN74LS10	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓		SDLS035
SN74LS11	14	Triple 3-Input Positive-AND Gate	✓	✓	✓		SDLS131
SN74LS14	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	SDLS049
SN74LS19A	14	Hex Inverter With Schmitt Trigger		✓	✓		SDLS138
SN74LS20	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓		SDLS079
SN74LS21	14	Dual 4-Input Positive-AND Gate	✓	✓	✓		SDLS022
SN74LS26	14	Quad 2-Input NAND Gate	✓	✓	✓		SDLS087
SN74LS27	14	Triple 3-Input Positive-NOR Gate	✓	✓	✓		SDLS089
SN74LS30	14	8-Input Positive-NAND Gate	✓	✓	✓		SDLS099
SN74LS31	14	Delay Element		✓	✓		SDLS157
SN74LS32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓		SDLS100
SN74LS33	14	Quad 2-Input NOR Gate With Open-Collector Outputs	✓	✓	✓		SDLS101
SN74LS37	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓		SDLS103
SN74LS38	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	✓	✓	✓		SDLS105
SN74LS42	16	4-to-10 BCD-to-Decimal Decoder	✓	✓	✓		SDLS109
SN74LS47	16	BCD 7-Segment Decoder/Driver	✓	✓	✓		SDLS111
SN74LS51	14	Dual 2-Input and Dual 3-Input AND/OR Gate	✓	✓	✓		SDLS113
SN74LS73A	14	Dual J-K Flip-Flop	✓	✓	✓		SDLS118
SN74LS74A	14	Dual D-Type Flip-Flop	✓	✓	✓		SDLS119
SN74LS75	16	4-Bit D-Type Latch	✓	✓	✓		SDLS120

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MIL – See page 4–3 for military package description and availability

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			MIL	PDIP	SOIC	SSOP	
SN74LS85	16	4-Bit Magnitude Comparator	✓	✓	✓		SDLS123
SN74LS86A	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓		SDLS124
SN74LS90	14	Decade Counter	✓	✓	✓		Call
SN74LS92	14	Divide-By-12 Counter	✓	✓	✓		Call
SN74LS93	14	4-Bit Binary Counter	✓	✓	✓		Call
SN74LS107A	14	Dual J-K Flip-Flop	✓	✓	✓		SDLS036
SN74LS109A	16	Dual J-$\overline{K}$ Flip-Flop	✓	✓	✓		SDLS037
SN74LS112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	✓	✓	✓		SDLS011
SN74LS122	14	One-Shot Multivibrator	✓	✓	✓		SDLS043
SN74LS123	16	Dual Monostable Multivibrator	✓	✓	✓		SDLS043
SN74LS125A	14	Quad Bus Buffer Gate ($\overline{OE}$)	✓	✓	✓		SDLS044
SN74LS126A	14	Quad Bus Buffer Gate (OE)	✓	✓	✓		SDLS044
SN74LS132	14	Quad 2-Input Positive-NAND With Schmitt Trigger	✓	✓	✓		SDLS047
SN74LS136	14	Quad Exclusive-OR Gate With Open-Collector Outputs	✓	✓	✓		SDLS048
SN74LS137	16	3-to-8 Decoder/Demultiplexer With Address Latch	✓	✓	✓		SDLS132
SN74LS138	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓		SDLS014
SN74LS139A	16	Dual 2-to-4 Decoder/Demultiplexer	✓	✓	✓		SDLS013
SN74LS145	16	BCD-to-Decimal Decoder/Driver	✓	✓	✓		SDLS051
SN74LS148	16	8-to-3-Line Priority Encoder	✓	✓	✓		Call
SN74LS151	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓		SDLS054
SN74LS153	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDLS055
SN74LS155A	16	Dual 1-to-4 Decoder	✓	✓	✓		SDLS057
SN74LS156	16	Dual 2-to-4-Line Decoder/Demultiplexer With Open-Collector Outputs	✓	✓	✓		SDLS057
SN74LS157	16	Quad 1-of-2 Data Selector/Multiplexer	✓	✓	✓		SDLS058
SN74LS158	16	Quad 1-of-2 Data Selector/Multiplexer	✓	✓	✓		SDLS058
SN74LS161A	16	4-Bit Synchronous Binary Counter	✓	✓	✓		SDLS060
SN74LS163A	16	4-Bit Synchronous Binary Counter	✓	✓	✓		SDLS060
SN74LS164	14	8-Bit Parallel-Out Serial Shift Register	✓	✓	✓		SDLS061
SN74LS165A	16	8-Bit Parallel-Load Shift Register	✓	✓	✓		Call
SN74LS166A	16	8-Bit Parallel-Load Shift Register	✓	✓	✓		SDLS063

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

LS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74LS169B	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDLS134
SN74LS173A	16	4-Bit D-Type Latch	✓	✓	✓		SDLS067
SN74LS174	16	Hex D-Type Flip-Flop	✓	✓	✓		SDLS068
SN74LS175	16	Quad D-Type Flip-Flop	✓	✓	✓		SDLS068
SN74LS191	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDLS072
SN74LS193	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓	✓		SDLS074
SN74LS194A	16	4-Bit Bidirectional Universal Shift Register	✓	✓	✓		SDLS075
SN74LS195A	16	4-Bit Bidirectional Universal Shift Register	✓	✓	✓		SDLS076
SN74LS221	16	Dual Monostable Multivibrator	✓	✓	✓		SDLS213A
SN74LS240	20	Octal Buffer/Driver	✓	✓	✓		SDLS144
SN74LS241	20	Octal Buffer/Driver	✓	✓	✓		SDLS144
SN74LS243	14	Quad Bus Transceiver	✓	✓	✓		SDLS145
SN74LS244	20	Octal Buffer/Driver	✓	✓	✓		SDLS144
SN74LS245	20	Octal Bus Transceiver	✓	✓	✓	✓	SDLS146A
SN74LS247	16	BCD-to-7-Segment Decoder	✓	✓	✓		SDLS083
SN74LS251	16	1-of-8 Data Selector/Multiplexer	✓	✓	✓		SDLS085
SN74LS253	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓		SDLS147
SN74LS257B	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDLS148
SN74LS258B	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓		SDLS148
SN74LS259B	16	8-Bit Addressable Latch	✓	✓	✓		SDLS086
SN74LS266	14	Quad 2-Input Exclusive-NOR Gate	✓	✓	✓		SDLS151
SN74LS273	20	Octal D-Type Flip-Flop	✓	✓	✓		SDLS090
SN74LS279A	16	Quad Set/Reset Latch	✓	✓	✓		SDLS093
SN74LS280	14	9-Bit Parity Generator/Checker	✓	✓	✓		SDLS152
SN74LS283	16	4-Bit Binary Full Adder	✓	✓	✓		SDLS095
SN74LS292	16	31-Bit Programmable Counter		✓			SDLS153
SN74LS294	16	16-Bit Programmable Counter		✓			SDLS153
SN74LS297	16	Digital Phase-Lock Loop		✓			SDLS155
SN74LS298	16	Quad 2-Input Multiplexer With Storage	✓	✓	✓		SDLS098
SN74LS299	20	8-Bit Universal Shift/Storage Register	✓	✓	✓		SDLS156

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74LS321	16	Crystal-Controlled Oscillator		✓			Call
SN74LS323	20	8-Bit Universal Shift/Storage Register	✓	✓	✓		SDLS160
SN74LS348	16	8-to-3-Line Encoder	✓	✓	✓		SDLS161
SN74LS365A	16	Hex Buffer/Driver	✓	✓	✓		SDLS102
SN74LS367A	16	Hex Buffer/Driver	✓	✓	✓		SDLS102
SN74LS368A	16	Hex Buffer/Driver	✓	✓	✓		SDLS102
SN74LS373	20	Octal D-Type Transparent Latch	✓	✓	✓		SDLS165
SN74LS374	20	Octal D-Type Flip-Flop	✓	✓	✓		SDLS165
SN74LS375	16	4-Bit Bistable Latch	✓	✓	✓		SDLS166
SN74LS377	20	Octal D-Type Flip-Flop With Clock Enable	✓	✓	✓		SDLS167
SN74LS378	16	Hex D-Type Flip-Flop With Clock Enable	✓	✓	✓		SDLS167
SN74LS379	16	Quad D-Type Flip-Flop With Clock Enable	✓	✓	✓		SDLS167
SN74LS382	20	4-Bit Arithmetic Logic Unit		✓			Call
SN74LS390	16	Dual 4-Bit Decade Counter	✓	✓	✓		SDLS107
SN74LS393	14	Dual 4-Bit Binary Counter	✓	✓	✓		SDLS107
SN74LS396	16	Octal Storage Register	✓	✓			SDLS173
SN74LS399	16	Quad 2-Input Multiplexer	✓	✓	✓		SDLS174
SN74LS423	16	Retriggerable Multivibrator	✓	✓	✓		SDLS175
SN74LS442	20	Bus Transceiver		✓	✓		SDLS176
SN74LS465	20	Octal Buffer/Driver		✓	✓		SDLS179
SN74LS466	20	Bus Transceiver		✓	✓		SDLS179
SN74LS540	20	Octal Buffer/Driver	✓	✓	✓		SDLS180
SN74LS541	20	Octal Buffer/Driver	✓	✓	✓		SDLS180
SN74LS590	16	8-Bit Binary Counter With 3-State Output Register	✓	✓	✓		SDLS003
SN74LS592	16	Binary Counter With Input Register	✓	✓	✓		SDLS004
SN74LS593	20	8-Bit Binary Counter With 3-State I/O Register	✓	✓	✓		SDLS004
SN74LS594	16	8-Bit Shift Register With Output Register		✓	✓		SDLS005
SN74LS595	16	8-Bit Shift Register With 3-State Output Register	✓	✓	✓		SDLS006
SN74LS596	16	Octal Shift Register		✓			SDLS006
SN74LS597	16	Shift Register With Input Latch	✓	✓	✓		SDLS007

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
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PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

LS

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	
SN74LS598	20	Shift Register With Input Latch	✓	✓	✓		SDLS007
SN74LS599	16	Shift Register With Output Latch		✓	✓		SDLS005
SN74LS623	20	Octal Bus Transceiver		✓	✓		SDLS185
SN74LS624	14	Voltage-Controlled Oscillator	✓	✓	✓		SDLS186
SN74LS628	14	Voltage-Controlled Oscillator	✓	✓	✓		SDLS186
SN74LS629	16	Voltage-Controlled Oscillator	✓	✓	✓		SDLS186
SN74LS640	20	Octal Bus Transceiver	✓	✓	✓		SDLS189
SN74LS640-1	20	Octal Bus Transceiver		✓	✓		SDLS189
SN74LS641	20	Octal Bus Transceiver With Open-Collector Outputs	✓	✓	✓		SDLS189
SN74LS641-1	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDLS189
SN74LS642	20	Octal Bus Transceiver With Open-Collector Outputs	✓	✓	✓		SDLS189
SN74LS642-1	20	Octal Bus Transceiver With Open-Collector Outputs		✓	✓		SDLS189
SN74LS645	20	Octal Bus Transceiver	✓	✓	✓		SDLS189
SN74LS646	24	Octal Registered Bus Transceiver		✓	✓		SDLS190
SN74LS647	24	Octal Registered Bus Transceiver		✓	✓		SDLS190
SN74LS648	24	Octal Registered Bus Transceiver		✓	✓		SDLS190
SN74LS652	24	Octal Registered Bus Transceiver		✓	✓		SDLS191
SN74LS669	16	4-Bit Up/Down Counter	✓	✓	✓		SDLS192
SN74LS670	16	4-By-4 Register File	✓	✓	✓		SDLS193
SN74LS673	24	16-Bit Shift Register	✓	✓	✓		SDLS195
SN74LS674	24	16-Bit Shift Register	✓	✓	✓		SDLS195
SN74LS682	20	8-Bit Magnitude Comparator	✓	✓	✓		SDLS008
SN74LS684	20	8-Bit Magnitude Comparator	✓	✓	✓		SDLS008
SN74LS686	24	Octal Magnitude/Identity Comparator		✓	✓		SDLS008
SN74LS688	20	8-Bit Identity Comparator	✓	✓	✓		SDLS008
SN74LS697	20	Synchronous Up/Down Binary Counter	✓	✓	✓		SDLS199

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

LV
Low-Voltage CMOS Technology

TI's LV CMOS technology products are specially designed parts for 3-V power supply use. The entire LV family also has been recharacterized to operate at 5 V.

The LV family is a 2-μ CMOS process that provides up to 8 mA of drive and propagation delays of 18 ns maximum, while having a static power consumption of only 20 μA for both bus-interface and gate functions.

The LV family is offered in the octal footprints with advanced packaging such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP).

For LV data sheets, see the 1998 *LVC and LV Low-Voltage CMOS Logic Data Book*, literature number SCBD152A, or the 1996 *AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book*, literature number SCLD004.

DEVICE SELECTION GUIDE

LV

DEVICE	NO. PINS	FUNCTION	AVAILABILITY				LITERATURE REFERENCE
			SOIC	SSOP	TSSOP	TVSOP	
SN74LV00A	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	✓	SCLS389B
SN74LV02A	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓	✓	SCLS390B
SN74LV04A	14	Hex Inverter	✓	✓	✓	✓	SCLS388A
SN74LVU04A	14	Hex Inverter	✓	✓	✓	✓	SCES130B
SN74LV08A	14	Quad 2-Input Positive-AND Gate	✓	✓	✓	✓	SCLS387B
SN74LV14A	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓	SCLS386A
SN74LV32A	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	✓	SCLS385A
SN74LV74A	14	Dual D-Type Flip-Flop	✓	✓	✓	✓	SCLS381C
SN74LV125A	14	Quad Bus Buffer Gate With 3-State Outputs	✓	✓	✓	✓	SCES124D
SN74LV126A	14	Quad Bus Buffer Gate With 3-State Outputs	✓	✓	✓	✓	SCES131C
SN74LV138A	16	3-to-8 Decoder/ Demultiplexer	✓	✓	✓	✓	SCLS395B
SN74LV164A	14	8-Bit Parallel-Out Serial Shift Register	✓		✓		SCLS403
SN74LV165A	16	8-Bit Parallel-Load Shift Register	✓	✓	✓		SCLS402B
SN74LV174A	16	Hex D-Type Flip-Flop With Clear	✓	✓	✓		SCLS401B
SN74LV240A	20	Octal Buffer/ Driver With 3-State Outputs	✓	✓	✓	✓	SCLS384B
SN74LV244A	20	Octal Buffer/ Driver With 3-State Outputs	✓	✓	✓	✓	SCLS383A
SN74LV245A	20	Octal Bus Transceiver With 3-State Outputs	✓	✓	✓	✓	SCLS382B
SN74LV273A	20	Octal D-Type Flip-Flop With Clear	✓	✓	✓		SCLS399
SN74LV373A	20	Octal Transparent D-Type Latch With 3-State Outputs	✓	✓	✓	✓	SCLS407
SN74LV374A	20	Octal D-Type Flip-Flop With 3-State Outputs	✓	✓	✓	✓	SCLS408
SN74LV573A	20	Octal Edge-Triggered D-Type Transparent Latch With 3-State Outputs	✓	✓	✓		SCLS411A
SN74LV574A	20	Octal D-Type Flip-Flop	✓	✓	✓		SCLS412A

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

LVC
Low-Voltage CMOS Technology

TI's LVC logic products are specially designed for 3-V power supplies.

The LVC family is a high-performance version with 0.8-μ CMOS process technology, 24-mA current drive, and 6.5-ns maximum propagation delays for driver operations. The LVC family includes both bus-interface and gate functions with 70 different functions planned.

The LVC family is offered in the octal and Widebus™ footprints with all of the advanced packaging such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP) with planned thin very small-outline (TVSOP) additions.

All LVC devices are available with 5-V tolerant inputs and outputs.

For LVC data sheets, see the 1998 *LVC and LV Low-Voltage CMOS Logic Data Book*, literature number SCBD152A.

DEVICE SELECTION GUIDE

LVC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74LVC1G00A	5	Single 2-Input Positive-NAND Gate						✢	SCAS609
SN74LVC1G02A	5	Single 2-Input Positive-NOR Gate						✢	SCAS610
SN74LVC1G04A	5	Single Inverter Gate						✢	SCES132
SN74LVC1G05A	5	Single Hex Inverter Gate						✢	Call
SN74LVC1G08A	5	Single 2-Input Positive-AND Gate						✢	SCES133
SN74LVC1G14A	5	Single Schmitt-Trigger Inverter Gate						✢	SCES134
SN74LVC1G32A	5	Single 2-Input Positive-OR Gate						✢	SCES135
SN74LVC1G79A	5	Single D-Type Flip-Flop Without Preset and Clear						✢	Call
SN74LVC1G86A	5	Single 2-Input Exclusive-OR Gate						✢	SCES136
SN74LVC1G125A	5	Single Bus Buffer Gate ($\overline{OE}$)						✢	Call
SN74LVC1G126A	5	Single Bus Buffer Gate (OE)						✢	Call
SN74LVC00A	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	✓			SCAS279G
SN74LVC02A	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓	✓			SCAS280H
SN74LVC04A	14	Hex Inverter	✓	✓	✓	✓			SCAS281H
SN74LVCU04A	14	Hex Inverter		✓	✓	✓			SCAS282F
SN74LVC06A	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	✓	✓		SCAS596B
SN74LVC07A	14	Hex Buffer With Open-Collector Outputs	✓	✓	✓	✓	✓		SCAS595E
SN74LVC08A	14	Quad 2-Input Positive-AND Gate	✓	✓	✓	✓			SCAS283G
SN74LVC10A	14	Triple 3-Input Positive-NAND Gate		✓	✓	✓			SCAS284F
SN74LVC14A	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	✓			SCAS285H
SN74LVC32A	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	✓			SCAS286H
SN74LVC74A	14	Dual Positive-Edge-Triggered D-Type Flip-Flop	✓	✓	✓	✓			SCAS287H
SN74LVC86A	14	Quad 2-Input Exclusive-OR Gate	✓	✓	✓	✓			SCAS288H
SN74LVC112A	16	Dual Negative-Edge-Triggered JK Flip-Flop		✓	✓	✓	✓		SCAS289F
SN74LVC125A	14	Quad Bus Buffer Gate ($\overline{OE}$)		✓	✓	✓			SCAS290F
SN74LVC126A	14	Quad Bus Buffer Gate (OE)		✓	✓	✓	✓		SCAS339F
SN74LVC137A	16	3-to-8 Decoder/Demultiplexer With Address Latches		✢	✢	✢			SCAS340E
SN74LVC138A	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	✓			SCAS291H
SN74LVC139A	16	Dual 2-to-4 Decoder/Demultiplexer		✓	✓	✓			SCAS341F

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✓ = Now ★ = See page 4–3
✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74LVC157A	16	Quad 2-to-1 Data Selector/Multiplexer		✓	✓	✓			SCAS292F
SN74LVC158A	16	Quad 2-to-1 Data Selector/Multliplexer		✢	✢	✢			SCAS342F
SN74LVC240A	20	Octal Buffer/Driver		✓	✓	✓	✓		SCAS293F
SN74LVC241A	20	Octal Buffer/Driver		✢	✢	✢			SCAS343E
SN74LVC244A	20	Octal Buffer/Driver		✓	✓	✓	✓		SCAS414I
SN74LVCH244A	20	Octal Buffer/Driver With Bus Hold	✓	✓	✓	✓	✓		SCES009G
SN74LVC245A	20	Octal Bus Transceiver		✓	✓	✓	✓		SCAS218I
SN74LVCH245A	20	Octal Bus Transceiver With Bus Hold	✓	✓	✓	✓	✓		SCES008F
SN74LVC257A	16	Quad 2-to-1 Data Selector/Multliplexer		✓	✓	✓			SCAS294F
SN74LVC258A	16	Quad 2-to-1 Data Selector/Multliplexer		✢	✢	✢			SCAS345F
SN74LVC373A	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓		SCAS295J
SN74LVC374A	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓		SCAS296I
SN74LVC540A	20	Octal Buffer/Driver	✓	✓	✓	✓	✓		SCAS297H
SN74LVC541A	20	Octal Buffer/Driver	✓	✓	✓	✓	✓		SCAS298H
SN74LVC543A	24	Octal Registered Bus Transceiver		✓	✓	✓			SCAS299F
SN74LVC544A	24	Octal Registered Transceiver		✢	✢	✢			SCAS346E
SN74LVC573A	20	Octal D-Type Transparent Latch	✓	✓	✓	✓	✓		SCAS300I
SN74LVC574A	20	Octal D-Type Flip-Flop	✓	✓	✓	✓	✓		SCAS301I
SN74LVC646A	24	Octal Registered Bus Transceiver	✓	✓	✓	✓			SCAS302G
SN74LVC652A	24	Octal Registered Bus Transceiver	✓	✓	✓	✓	✓		SCAS303G
SN74LVC821A	24	10-Bit Bus-Interface Flip-Flop		✓	✓	✓	✓		SCAS304F
SN74LVC823A	24	9-Bit Bus-Interface Flip-Flop		✓	✓	✓	✓		SCAS305F
SN74LVC827A	24	10-Bit Buffer/Driver		✓	✓	✓	✓		SCAS306G
SN74LVC828A	24	10-Bit Buffer/Driver		✓	✓	✓	✓		SCAS347E
SN74LVC841A	24	10-Bit Bus-Interface D-Type Latch		✓	✓	✓	✓		SCAS307G
SN74LVC843A	24	9-Bit Bus-Interface D-Type Latch		✢	✢	✢			SCAS308E
SN74LVC861A	24	10-Bit Bus Transceiver		✓	✓	✓	✓		SCAS309F
SN74LVC863A	24	9-Bit Bus Transceiver		✓	✓	✓	✓		SCAS310G
SN74LVC2244A	20	Octal Buffer/Driver With Series-Damping Resistors		✓	✓	✓	✓		SCAS572F

commercial package description and availability

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PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE SELECTION GUIDE

LVC

DEVICE	NO. PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	SOIC	SSOP	TSSOP	TVSOP	SOT	
SN74LVCR2245A	20	Octal Bus Transceiver With Series-Damping Resistors		✓	✓	✓	✓		SCAS581D
SN74LVC2952A	24	Octal Registered Bus Transceiver		✓	✓	✓	✓		SCAS311F
SN74LVCC3245A	24	Octal Bus Transceiver With Adjustable Output Voltage		✓	✓	✓			SCAS585E
SN74LVC4245	24	Octal Bus Transceiver and 3.3-V to 5-V Shifter		✓	✓	✓			SCAS375D
SN74LVCC4245A	24	Octal Level-Shifting Transceiver		✓	✓	✓			SCAS584E
SN74LVCH16240A	48	16-Bit Buffer/Driver With Bus Hold			✓	✓	✓		SCAS566G
SN74LVCH16241A	48	16-Bit Buffer/Driver With Bus Hold			✢	✢			SCAS348E
SN74LVC16244A	48	16-Bit Buffer/Driver			✓	✓	✓		SCES061G
SN74LVCH16244A	48	16-Bit Buffer/Driver With Bus Hold			✓	✓			SCAS313G
SN74LVC16245A	48	16-Bit Bus Transceiver			✓	✓	✓		SCES062G
SN74LVCH16245A	48	16-Bit Bus Transceiver With Bus Hold			✓	✓	✓		SCES063G
SN74LVCH16373A	48	16-Bit Transparent D-Type Latch With Bus Hold			✓	✓	✓		SCAS568G
SN74LVCH16374A	48	16-Bit Edge-Triggered D-Type Flip-Flop With Bus Hold			✓	✓	✓		SCAS565F
SN74LVCH16540A	48	16-Bit Buffer/ Driver With Bus Hold			✓	✓	✓		SCAS569G
SN74LVCH16541A	48	16-Bit Buffer/ Driver With Bus Hold			✓	✓	✓		SCAS567G
SN74LVCH16543A	56	16-Bit Registered Bus Transceiver With Bus Hold			✓	✓	✓		SCAS317F
SN74LVCH16646A	56	16-Bit Registered Bus Transceiver With Bus Hold			✓	✓	✓		SCAS318H
SN74LVCH16652A	56	16-Bit Registered Bus Transceiver With Bus Hold			✓	✓	✓		SCAS319G
SN74LVCH16952A	56	16-Bit Registered Bus Transceiver			✓	✓	✓		SCAS320F
SN74LVC161284	48	17-Bit IEEE P1284 Driver/Receiver			✓	✓			SCAS583G
SN74LVCH162244A	48	16-Bit Buffer/Driver With Series-Damping Resistors and Bus Hold			✓	✓	✓		SCAS545F
SN74LVCHR162245A	48	16-Bit Bus Transceiver With Series-Damping Resistors and Bus Hold				✓			SCAS582E

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
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PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

LVT
Low-Voltage BiCMOS Technology

The specially designed 3.3-V LVT family uses the latest 0.8-μ BiCMOS-process technology with performance specifications ideal for workstation, networking, and telecommunication applications. In addition to popular octal and Widebus™ bus-interface devices, TI also offers the universal bus transceiver (UBT™) in this low-voltage family.

Performance characteristics of the LVT family are:

- Speed – Provides high performance with typical propagation delays of 4 ns for buffers.
- 3.3-V operation with 5-V tolerant I/O – Capability to interface with a mixed-voltage environment. The I/Os can handle up to 7 V, which allows them to act as 5-V/3-V translators.
- Drive – The LVT family provides up to 64 mA of drive, yet consumes less than 100 μA of standby power at 3.3-V V_{CC}.

Additional features include:

- Live insertion – LVT devices also incorporate circuitry to protect the devices in live-insertion applications. The devices go into the high-impedance state during power up and power down, which is called powered-up 3-state (PU3S).
- Bus hold – Solves the floating input problem by holding the input at the last valid logic state. This eliminates the need for external pullup and pulldown resistors.
- Damping-resistor option – TI implements series-damping resistors on certain devices, which not only reduces overshoot and undershoot, but also matches the line impedance, minimizing ringing.
- Packaging – LVT devices are available in the octal and Widebus™ footprints in packaging options such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP).

For LVT data sheets, see the 1998 *LVT Low-Voltage Technology Data Book*, literature number SCBD154.

DEVICE SELECTION GUIDE

LVT

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	SOIC	SSOP	TSSOP	TVSOP	
LVT Octals (SN74LVTHxxx)								
SN74LVTH125	14	Quad Bus Buffer Gate		✢	✢	✢		SCBS703C
SN74LVTH240	20	Octal Buffer/Driver	★	✓	✓	✓		SCBS679C
SN74LVTH241	20	Octal Buffer/Driver	★	✓	✓	✓		SCAS352H
SN74LVTH244A	20	Octal Buffer/Driver	★	✓	✓	✓		SCAS586C
SN74LVTH245A	20	Octal Bus Transceiver	✓	✓	✓	✓		SCBS130O
SN74LVTH273	20	Octal D-Type Flip-Flop With Clear	★	✓	✓	✓		SCBS136J
SN74LVTH373	20	Octal D-Type Latch	★	✓	✓	✓		SCBS689D
SN74LVTH374	20	Octal Edge-Triggered D-Type Flip-Flop	★	✓	✓	✓		SCBS683D
SN74LVTH540	20	Octal Buffer/Driver		✓	✓	✓		SCBS681D
SN74LVTH541	20	Octal Buffer/Driver		✓	✓	✓		SCBS682D
SN74LVTH543	24	Octal Registered Bus Transceiver		✓	✓	✓	✓	SCBS704C
SN74LVTH573	20	Octal D-Type Transparent Latch	✓	✓	✓	✓		SCBS687D
SN74LVTH574	20	Octal D-Type Flip-Flop	✓	✓	✓	✓		SCBS688C
SN74LVTH646	24	Octal Registered Bus Transceiver	✓	✓	✓	✓	✓	SCBS705C
SN74LVTH652	24	Octal Registered Bus Transceiver		✓	✓	✓	✓	SCBS706C
SN74LVTH2952	24	Octal Registered Bus Transceiver		✓	✓	✓	✓	SCBS710C
LVT Widebus™ (SN74LVTH16xxx)								
SN74LVTH16240	48	16-Bit Buffer/Driver	★		✓	✓		SCBS684B
SN74LVTH16241	48	16-Bit Buffer/Driver			✓	✓		SCBS693B
SN74LVTH16244A	48	16-Bit Buffer/Driver	★		✓	✓	✓	SCBS142K
SN74LVTH16245A	48	16-Bit Bus Transceiver	★		✓	✓		SCBS143K
SN74LVTH16373	48	16-Bit D-Type Transparent Latch	★		✓	✓		SCBS144J
SN74LVTH16374	48	16-Bit D-Type Flip-Flop	★		✓	✓		SCBS145K
SN74LVT16500	56	18-Bit Universal Bus Transceiver			✓	✓		SCBS146D
SN74LVTH16500	56	18-Bit Universal Bus Transceiver			✢	✢		SCBS701B
SN74LVT16501	56	18-Bit Universal Bus Transceiver			✓	✓		SCBS147G
SN74LVTH16501	56	18-Bit Universal Bus Transceiver			✢	✢		SCBS700B
SN74LVTH16541	48	16-Bit Buffer/Driver	✓		✓	✓		SCBS691C
SN74LVTH16543	56	16-Bit Registered Bus Transceiver			✓	✓		SCBS699C

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
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schedule

✓ = Now ★ = See page 4–3
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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY					LITERATURE REFERENCE
			MIL	SOIC	SSOP	TSSOP	TVSOP	
SN74LVTH16646	56	16-Bit Registered Bus Transceiver			✓	✓		SCBS698D
SN74LVTH16652	56	16-Bit Registered Bus Transceiver With 3-State Outputs			✓	✓		SCBS150J
SN74LVT16835	56	18-Bit Buffer/Driver			✓	✓		SCBS309D
SN74LVTH16835	56	18-Bit DFF Memory Buffer/Driver			✢	✢		SCBS713A
SN74LVTH16952	56	16-Bit Registered Bus Transceiver	✓		✓	✓		SCBS697D
LVT Octals/Widebus™ With Series-Damping Resistors (SN74LVTH2xxx, SN74LVTH162xxx)								
SN74LVTH2245A	48	16-Bit Transceiver		✓	✓	✓	✓	SCBS707B
SN74LVTH162240	48	16-Bit Buffer/Driver	✓		✓	✓		SCBS685D
SN74LVTH162241	48	16-Bit Buffer/Driver With 3-State Outputs			✓	✓		SCBS692C
SN74LVTH162244	48	16-Bit Buffer/Driver	★		✓	✓		SCBS258I
SN74LVTH162245	48	16-Bit Bus Transceiver	★		✓	✓		SCBS260J
SN74LVTH162373	48	16-Bit D-Type Transparent Latch	★		✓	✓		SCBS261I
SN74LVTH162374	48	16-Bit D-Type Flip-Flop	★		✓	✓		SCBS262H
SN74LVTH162541	48	16-Bit Buffer/Driver With 3-State Outputs			✓	✓		SCBS690D

commercial package description and availability

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DBV = 5 pins
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DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
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TSSOP (thin shrink small-outline package)
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TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

S
Schottky Logic

With a wide array of functions, TI's S family continues to offer replacement alternatives for mature systems. This classic line of devices was at the cutting edge of performance when introduced, and continues to deliver excellent value for many of today's designs. As the world leader in logic products, TI is committed to being the last major supplier at every price-performance node.

For S data sheets, contact the Product Information Center at (972) 644-5580.

S

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN74S00	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	SDLS025
SN74S02	14	Quad 2-Input Positive-NOR Gate	✓	✓	✓	SDLS027
SN74S04	14	Hex Inverter	✓	✓	✓	SDLS029
SN74S05	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	SDLS030
SN74S08	14	Quad 2-Input Positive-AND Gate	✓	✓	✓	SDLS033
SN74S09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	✓	✓	✓	SDLS034
SN74S10	14	Triple 3-Input Positive-NAND Gate	✓	✓	✓	SDLS035
SN74S11	14	Triple 3-Input Positive-AND Gate	✓	✓	✓	SDLS131
SN74S20	14	Dual 4-Input Positive-NAND Gate	✓	✓	✓	SDLS079
SN74S30	14	8-Input Positive-NAND Gate	✓	✓	✓	SDLS099
SN74S32	14	Quad 2-Input Positive-OR Gate	✓	✓	✓	SDLS100
SN74S37	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	SDLS103
SN74S38	14	Quad 2-Input NAND Gate With Open-Collector Outputs	✓	✓	✓	SDLS105
SN74S51	14	Dual 2-Input and Dual 3-Input AND/OR Gate	✓	✓	✓	SDLS113
SN74S74	14	Dual D-Type Flip-Flop	✓	✓	✓	SDLS119
SN74S85	14	4-Bit Magnitude Comparator	✓	✓	✓	SDLS123
SN74S112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	✓	✓	✓	SDLS011
SN74S124	16	Dual Voltage-Controlled Oscillator	✓	✓	✓	SDLS201
SN74S132	14	Quad 2-Input Positive-NAND Schmitt Trigger	✓	✓	✓	SDLS047
SN74S133	16	13-Input NAND Gate	✓	✓	✓	SDLS202
SN74S138A	16	3-to-8 Decoder/Demultiplexer	✓	✓	✓	SDLS014
SN74S139A	16	Dual 2-to-4 Decoder/Demultiplexer	✓	✓	✓	SDLS013
SN74S140	14	Dual 50-Ω Line Driver	✓	✓	✓	SDLS210
SN74S151	16	8-to-1 Data Selector/Multiplexer	✓	✓	✓	SDLS054
SN74S153	16	Dual 4-to-1 Data Selector/Multiplexer	✓	✓	✓	SDLS055
SN74S157	16	Quad 1-of-2 Data Selector/Multiplexer	✓	✓	✓	SDLS058
SN74S158	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓	SDLS058
SN74S163	16	4-Bit Synchronous Binary Counter	✓	✓	✓	SDLS060
SN74S169	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓		SDLS134
SN74S174	16	Hex D-Type Flip-Flop	✓	✓		SDLS068

commercial package description and availability

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MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN74S175	16	Quad D-Type Flip-Flop	✓	✓	✓	SDLS068
SN74S194	16	4-Bit Bidirectional Universal Shift Register	✓	✓		SDLS075
SN74S195	16	4-Bit Bidirectional Universal Shift Register	✓	✓	✓	SDLS076
SN74S240	20	Octal Buffer/Driver	✓	✓	✓	SDLS144
SN74S241	20	Octal Buffer/Driver	✓	✓	✓	SDLS144
SN74S244	20	Octal Buffer/Driver	✓	✓	✓	SDLS144
SN74S251	16	1-of-8 Data Selector/Multiplexer	✓	✓	✓	SDLS085
SN74S257	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓	✓	SDLS148
SN74S260	14	Dual 5-Input Positive-NOR Gate	✓	✓	✓	SDLS208
SN74S280	14	9-Bit Parity Generator/Checker	✓	✓	✓	SDLS152
SN74S283	16	4-Bit Binary Full Adder	✓	✓		SDLS095
SN74S299	20	8-Bit Universal Shift Register	✓	✓	✓	SDLS156
SN74S373	20	Octal D-Type Transparent Latch	✓	✓	✓	SDLS165
SN74S374	20	Octal D-Type Flip-Flop	✓	✓	✓	SDLS165
SN74S381	20	Arithmetic Logic Unit	✓	✓		SDLS168

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
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DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
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TVSOP (thin very small-outline package)
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DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
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PCB = 120 pins (FIFO only)

schedule

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✢ = Planned

MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

SSTL
Stub Series-Terminated Logic

SSTL is the computer industry's leading choice for next-generation technology in high-speed memory subsystems, adopted by a Joint Electronic Device Engineering Committee (JEDEC) standard and endorsed by major memory module, workstation, and PC manufacturers.

The SSTL16837 is the industry's first device for driving 3.3-V address signals from a low-voltage memory controller to SDRAMs using SSTL technology. In designs operating at >75 MHz, the SSTL16837 provides fast address signaling with minimal propagation delay. The SSTL16837 converts LVTTL signals from the memory controller to SSTL signals that are used by the SDRAM input pins. Targeted users of the device initially include workstations and servers, with eventual migration to PCs, as high-speed memory subsystem technology evolves in desktop systems.

HSTL
High-Speed Transceiver Logic

DEVICE SELECTION GUIDE

SSTL/HSTL

DEVICE	NO. PINS	FUNCTION	AVAILABILITY MIL	AVAILABILITY SSOP	AVAILABILITY TSSOP	LITERATURE REFERENCE
SN74SSTL16837	64	20-Bit SSTL_3 Universal Bus Driver			✓	SCBS675F
SN74SSTL16847	64	20-Bit SSTL_3 Bus Driver (Like '244)			✛	SCBS709A
SN74SSTL16857	48	14-Bit SSTL_2/3 Universal Bus Driver			✛	Call
SN74HSTL162822	64	14-Bit HSTL-to-LVTTL Memory Address Latch			✓	SCES091A

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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✛ = Planned

MIL – See page 4–3 for military package description and availability

TTL
Transistor-Transistor Logic

With a wide array of functions, TI's TTL family continues to offer replacement alternatives for mature systems. This classic line of devices was at the cutting edge of performance when introduced, and continues to deliver excellent value for many of today's designs. As the world leader in logic products, TI is committed to being the last major supplier at every price-performance node.

For TTL data sheets, contact the Product Information Center at (972) 644-5580.

DEVICE SELECTION GUIDE

TTL

DEVICE	NO. PINS	FUNCTION	AVAILABILITY			LITERATURE REFERENCE
			MIL	PDIP	SOIC	
SN7400	14	Quad 2-Input Positive-NAND Gate	✓	✓	✓	SDLS025
SN7404	14	Hex Inverter	✓	✓		SDLS029
SN7405	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	SDLS030
SN7406	14	Hex Inverter With Open-Collector Outputs	✓	✓	✓	SDLS031
SN7407	14	Hex Buffer With Open-Collector Outputs	✓	✓	✓	SDLS032A
SN7414	14	Hex Inverter With Schmitt Trigger	✓	✓	✓	SDLS049
SN7416	14	Hex Inverter/Driver	✓	✓	✓	SDLS031
SN7417	14	Hex Buffer/Driver With Open-Collector Outputs	✓	✓	✓	SDLS032A
SN7430	14	8-Input Positive-NAND Gate	✓	✓		SDLS099
SN7432	14	Quad 2-Input OR Gate	✓	✓		SDLS100
SN7437	14	Quad 2-Input Positive-NAND Gate	✓	✓		SDLS103
SN7438	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	✓	✓	✓	SDLS105
SN7445	16	BCD-to-Decimal Decoder/Driver	✓	✓		SDLS110
SN7447A	16	BCD 7-Segment Decoder/Driver	✓	✓		SDLS111
SN7474	14	Dual D-Type Flip-Flop	✓	✓	✓	SDLS119
SN7497	16	Binary Rate Multiplier	✓	✓		SDLS130
SN74121	14	One-Shot Multivibrator	✓	✓	✓	SDLS042
SN74123	16	Dual Monostable Multivibrator	✓	✓		SDLS043
SN74128	14	50-Ω Line Driver	✓	✓	✓	SDLS045
SN74132	14	Quad 2-Input Positive-NAND With Schmitt Trigger	✓	✓		SDLS047
SN74145	16	BCD-to-Decimal Decoder/Driver	✓	✓		SDLS051
SN74148	16	8-to-3-Line Priority Encoder	✓	✓		SDLS053
SN74150	24	Data Selector/Multiplexer	✓	✓		SDLS054
SN74154	24	4-to-16-Line Decoder/Demultiplexer	✓	✓	✓	SDLS056
SN74156	16	Dual 2-to-4-Line Decoder/Demultiplexer With Open-Collector Outputs	✓	✓		SDLS057
SN74157	16	Quad 2-to-1 Data Selector/Multiplexer	✓	✓		SDLS058
SN74159	24	4-to-16-Line Decoder/Demultiplexer	✓	✓		SDLS059
SN74175	16	Quad D-Type Flip-Flop	✓	✓		SDLS068
SN74193	16	4-Bit Synchronous Up/Down Binary Counter	✓	✓		SDLS074
SN74276	20	Quad J-K Flip-Flop		✓	✓	SDLS091

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

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PCB = 120 pins (FIFO only)

schedule

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✢ = Planned

MIL – See page 4–3 for military package description and availability

DEVICE	NO. PINS	FUNCTION	AVAILABILITY MIL	AVAILABILITY PDIP	AVAILABILITY SOIC	LITERATURE REFERENCE
SN74367A	16	Hex Buffer/Driver	✓	✓		SDLS102
SN74368A	16	Hex Buffer/Driver	✓	✓		SDLS102
SN74376	16	Quad J-K Flip-Flop	✓	✓		SDLS104

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
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MIL – See page 4–3 for military package description and availability

TEXAS INSTRUMENTS

Appendix TI02

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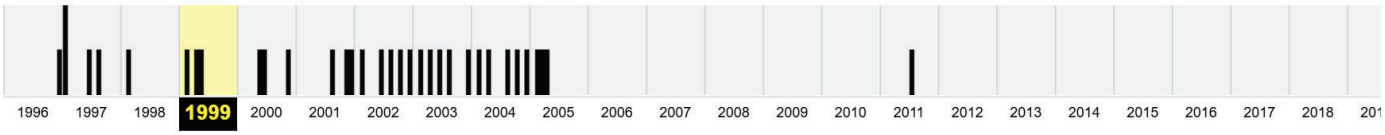
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Logic Products

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Packaging Options

August 1998 Logic Selection Guide

Texas Instruments (TI) offers a full spectrum of logic functions in a variety of technologies. TI's process technologies include CMOS, BiCMOS, and bipolar. These state-of-the-art process technologies offer the logic performance and features required in today's system designs. TI's product offerings include the following:

- AC, ACT, AHC, AHCT, ALVC, HC, HCT, LV, LVC
- ABT, ABTE, ALB, BCT, HSTL, LVT, SSTL
- BTA, CBT, CBTLV, FB, FIFO, GTL, JTAG
- ALS, AS, F, LS, S, TTL

TI has addressed many important design issues, including testability, memory, driving, bus termination, low skew requirements, and low-impedance line driving with specialized, advanced logic devices that improve overall system performance.

TI offers a wide variety of packaging options, including advanced packaging, such as the plastic thin quad flat package (TQFP), shrink small-outline package (SSOP), thin shrink small-outline package TSSOP), and thin very small-outline package (TVSOP). All of these deliver high performance and allow the designer to double input/output in the same board area or to reduce the board-area requirement by one-half.

The following pdf file provides an electronic simulation of the paper 'Logic Selection Guide' for August 1998 (literature number SDYU001K). The selection guide lists the functions that TI offers in each logic family, with package availability and data sheet literature numbers which can be ordered through your local sales office or TI authorized distributors. TI data sheets are available on the World-Wide Web at:

http://www.ti.com/sc/docs/psheets/pids.htm

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Download the following electronic simulation of the complete Logic Selection Guide.

Logic Selection Guide (August 1998, sdyu001k.pdf, 3306KB)

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Appendix ABIDI01

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245     10$a1994 IEEE Symposium on Low Power Electronics : $bdigest of technical papers / $c[Lewis Terman, symposium chair].
246     30$aDigest of technical papers
250     ##$a1st ed.
260     ##$a[New York] : $bInstitue of Electrical and Electronics Engineers ; $aPiscataway, N.J. : $bIEEE Service Center, $c1994.
300     ##$a104 p. : $bill. ; $c28 cm.
500     ##$a"October 10-12, San Diego"--Cover.
500     ##$a"IEEE catalog number 94TH0669-2."
500     ##$aSponsored by IEEE Solid-State Circuits Council.
500     ##$a"Publisher: John H. Wuorinen, Castine, ME 04421."
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710     2#$aIEEE Solid-State Circuits Council
948     ##$aLTI 09/01/2008
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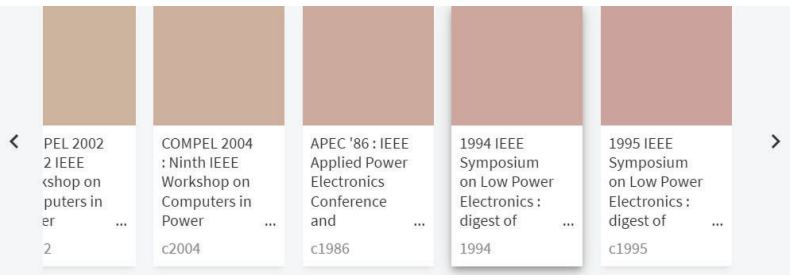
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Appendix ABIDI02

3.1

Low-Power RF-ICs in Wireless Transceivers

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Electrical Engineering Department
University of California
Los Angeles, CA 90024-1594

Introduction

It is anticipated that about 300 million portable consumer wireless devices will be in use by the year 2000 [1]. What IC technologies will enable the RF front-end of these devices? Do miniaturization and long battery-life call for architectural innovations in transceivers? What new circuit design styles will evolve in response?

There is much curiosity and speculation on these matters, yet little is known in general terms about RF-IC design, and the impact of large-scale integration and power-reduction strategies in front-ends of wireless transceivers. This paper presents a brief survey of the highlights in the application of IC technology to radios since the 1970s, and follows this with trends of what the author considers is the shape of things to come in wireless transceivers over the next few years. RF-ICs are roughly defined as integrated circuits operating in the band of frequencies from 100 MHz to 2000 MHz which covers most consumer wireless devices. MMICs, by contrast, are small-scale ICs operating at tens of GHz which are almost exclusively fabricated on III-V compound semiconductor substrates. Driven by defence applications over the past decade, they have become an established discipline. RF-ICs are principally driven by consumer needs. They are, and will continue to be, fabricated mostly in mature silicon technologies, combining analog and digital functions at relatively large levels of integration. It is the authors belief that in response to pressing demands for ubiquitous wireless access, the day of the "VLSI radio" is not that far off.

ICs in Broadcast Radio Receivers

Integrated circuits are used in one form or another in the front-end of most of today's broadcast receivers. However, it is fair to say that aside from contributing building blocks as the double-balanced mixr and the phase-locked loop, IC technology has *not* caused a profound re-thinking of radio receivers, whose architecture still resembles post-World War II radios. Some recent advances in this respect are now described.

The two most important specifications of a receiver are its *selectivity* and its *sensitivity*. Selectivity is the receiver's ability to reject adjacent channels and image frequencies, while sensitivity is its ability to detect weak input signals. The noise properties of the transistors in the front-end mainly set the sensitivity, whereas the receiver's frequency-allocation plan and quality of filters determine its selectivity. The frequency-allocation plan consists of the choice of the intermediate frequencies (IF) and of filtering to obtain a desired image suppression. In an FM receiver, for instance, as it is difficult to make high selectivity filters at RF, a first IF of 10.7 MHz is used to ensure that the unwanted image that will superpose itself on the desired channel lies outside the FM band of 88-108 MHz, and is inherently rejected by the detector. Passive crystal filters with a 150 kHz passband centered at 10.7 MHz then reject adjacent channels. In designing a low-power, miniature FM receiver, Kasperkovitz [2] at Philips realized there are many advantages in eliminating the RF and IF filters, and implementing the required selectivity on-chip. As it was impossible to integrate the RF filters on-chip with spiral monolithic inductors, or to replace the 10.7 MHz IF crystal filters with active gyrator filters, the key step in solving this problem was to *lower the IF* from 10.7 MHz to 70 kHz. Aside from a small off-chip inductor which provides a minimum of RF filtering, the channel bandwidth is mainly defined on-chip by high-order active *RC* filters. The power dissipation in these filters for a given dynamic range scales down with the IF [3], as does the required operating current in the IF amplifier. The image frequency, instead of lying outside the FM band, now lies *between* FM channels (Fig.1), so it only superposes noise on to the desired signal. However, a consequence of this choice is that the ±75 kHz frequency deviation of the desired FM channel may alias around DC to create distortion, so it is compressed to ±15 kHz by a negative frequency feedback. This single-chip FM mono receiver [4] requires only 15 small capacitors and two inductors, making it possible to fit the entire system within a wristwatch. The IC drains 8 mA from a 4.5V battery supply.

The same idea of low-IF has been pursued at Sony for their personal entertainment broadcast receivers. The bipolar RF-ICs operate at single-battery supplies as low as 0.95 V. A recent FM radio IC implements an unusual double-superheterodyne architecture [5]. At 30 MHz, the first IF is high enough for image-suppression by a fixed, low-selectivity bandpass filter after the antenna spanning the entire broadcast range from 88 to 108 MHz; no on-chip filter is used. Then, after amplification at the 30 MHz IF which comes readily in a state-of-the-art bipolar technology, a second *image-rejection mixer* (Fig.2) converts to a low IF of 150 kHz, and thereafter on-chip filtering is implemented by a 9th order active *RC* lowpass section. The RF amplifier transistors are integrated on-chip, although they require off-chip inductors for the load, and the local oscillator needs an off-chip *LC* tuned circuit. This receiver drains about 15 mA in either FM or AM mode.

ICs in Wireless Paging Receivers

Paging receivers have been in continuous development since the early 1960's, and have evolved into today's wide-area pagers which use digital signalling. The modern pager signals anywhere from 500 to 1200 b/s by encoding data with a simple positive or negative offset of the carrier frequency — the binary frequency-shift keyed (FSK) modulation. Paging receivers up to the early 1980's did not

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exploit the powerful simplifications this signaling scheme implied. Vance at Standard Telecommunication Laboratories realized how to simplify an FM receiver on to one chip with a quadrature downconversion mixer combined with *zero-IF*. Although this might not be suitable for a broadcast FM receiver, it was exactly the right solution for the binary-FSK digital paging receiver [6]. The remarkably simple receiver (Fig.3) consists only of a quadrature demodulator, lowpass filters in each arm, limiters, and a D-type flip-flop detector, and when integrated on one bipolar chip, it drains 2.5 mA from 1.8 V when active; in standby the drain falls to a mere 50 μA. More sophisticated detectors may be used to gain better noise rejection. Zero-IF means that the the image is entirely eliminated. DC offsets in the receiver or flicker noise now fall in-band, however, but as the data is encoded in frequencies ±4.5 kHz away from the carrier, the receiver may be AC coupled. The 10 kHz lowpass filters serve to eliminate out-of-band noise and blocking signals which would degrade the signal-to-noise ratio at the detector.

Single-chip bipolar zero-IF paging receivers are now quite common. A prominent feature they all share is that much of the die area is taken up by the capacitors for the on-chip lowpass filters and AC coupling [7, 8]. When active, these receivers consume only 1 to 2 mA from a single-battery, which is the typical specification for pagers. This example shows how the zero-IF, direct conversion architecture proved to be a good match to pager signalling.

ICs in Cellular Telephone Transceivers

Mobile and handheld cellular telephones are the first widespread two-way radios for consumer use, for which cordless telephones were a prelude. To be acceptable to the consumer, radio telephones must meet stringent demands for low weight and volume, long battery life, and low-cost. Further, to support a large numbers of users in a crowded radio spectrum, radio telephones require more signal processing than do other common transceivers. They must therefore use high levels of integration in the electronics.

The first generation of ICs for use in cellular telephones contained the frequently occurring building blocks used in conventional receivers, such as the mixer and local oscillator, or the IF amplifier chain and signal-strength indicator. Analog cellular telephones typically use the double-conversion architecture (Fig.6), assembled with these building blocks, often using GaAs ICs at the receiver and transmitter modules, silicon building blocks in the IF, surrounded by an impressive collection of discrete resonator filters and antenna duplexers [9].

Circuits to implement the complex modulation formats in the new generation of digital mobile telephones, with their greater requirements to withstand nearby blocking signals, require yet greater integration of the RF and IF electronics. In a 900 MHz transmitter silicon bipolar IC from Siemens [10], a precision quadrature-upconversion mixer implements the phase-shift keyed modulation specified in the European GSM system to produce a single-sideband, suppressed-carrier output. The IC, which includes an output stage to drive a separate power amplifier, drains 40 mA. The companion receiver IC includes a first mixer, with buffers to drive an IF off-chip bandpass SAW filter, and a quadrature downconversion mixer to detect the single-sideband input at baseband. Including an AGC with 70 dB range operating at the 40 to 90 MHz IF and a signal-strength indicator, the receiver drains 24 mA. Although the on-chip gain may become as large as 80 dB, it is distributed in different frequency bands and as a result there is little on-chip crosstalk.

Yet greater miniaturization is attained at Alcatel by integrating the transmitter and receiver sections together on one silicon bipolar chip. The zero-IF architecture makes this possible [11]. An off-chip low-noise amplifier drives directly into quadrature (I-Q) mixers, whose dynamic range is wide enough to withstand large blocking signals 3 MHz away from the carrier without producing significant intermodulation. Large (650 pF) off-chip capacitors constitute an anti-alias filter. The downconverted signals are sent to a baseband CMOS IC, containing a high-order switched capacitor lowpass filter to remove the blocking signals, and a demodulator. An *RC* and *CR* network with off-chip trimming shifts the local oscillator phase by ±45° to produce the quadrature drive to the mixers. Separate upconversion mixers in the transmitter drive a power amplifier module. The chip drains 25 mA from 5V in the receive mode, and 45 mA in the transmit mode, rather comparable to the Siemens chip set. It also suppresses the image and carrier by about 40 dB.

ICs for Spread-Spectrum Wireless Transceivers

As cellular telephones saturate the available radio frequency allocations, spread-spectrum techniques are being deployed in cordless telephones and wireless modems. These usually operate in the two lower bands allocated by the FCC for the industrial, scientific, and medical (ISM) communities for unlicensed spread-spectrum communications: 902 to 928 MHz, and 2.4 to 2.83 GHz. A ubiquitous wireless environment is envisioned, in which mobile users, wherever they are, may access data and communications services through an intricate network of base stations. The greatest hardware challenge is in developing the low-power, miniature handset.

A notable recent example of a miniature spread-spectrum transceiver is the 700 kb/s frequency-hopped device from Plessey, which operates in the 2.4 GHz band, and is assembled on 2"×3" PCMCIA card for insertion into notebook computers [12]. It communicates by binary frequency-shift keying of the carrier, and to spread the spectrum, the carrier frequency, in turn, is slowly hopped across the entire band by a variable-modulus PLL synthesizer. All the active devices in the transceiver are on *three ICs*, consisting of a GaAs RF front-end, a silicon bipolar IF receiver, and a CMOS IC for the hopping frequency-synthesis. Nevertheless, the transceiver requires 50 passive components, including six rather bulky passive components such as filters, and it dissipates more than 1 W while transmitting 100 mW.

The single-chip GaAs IC front-end in this transceiver [13] is one of the most highly integrated, as it includes the power amplifier and drivers for 2-GHz passive filters in the transmit and receive paths. Otherwise, it is a conventional double-superheterodyne architecture. In its first version, the IC has more than 20 on-chip spiral inductors, probably the largest number found on any MMIC! In receive mode, the IC drains 30 mA from a 5 V supply, and it selects one of two antennas with an on-chip RF switch for *spatial diversity*.

ICs to Enable Future Transceivers

What might the portable wireless communicator of the future look like? We may draw some conclusions from the foregoing summary of RF-IC developments. The crowded spectrum means that wireless communicators will predominantly use spread-spectrum techniques, and that the need for low power dissipation will force yet higher levels of integration. Much of the filtering will be done on-chip at low frequencies, with perhaps only one RF passive filter off-chip. The author with his colleagues and their graduate students at UCLA is investigating the architecture and circuit design of a frequency-hopped, binary frequency-shift keyed, zero IF, all-CMOS two-chip transceiver capable of delivering up to 160 kb/s (the base ISDN rate) in the 900 MHz ISM band (Fig.5) [14]. This approach is to a large degree inspired by the modern paging receiver, which is perhaps the lowest-energy wireless device in wide use. The transceiver ICs freely mix analog and digital circuits, making CMOS the IC technology of choice for the entire transceiver, *including* the RF front-end. These blocks will be implemented in an unmodified standard production 1-μm CMOS process.

Low-power operation requires that the entire system should operate on a 3V supply, which cannot be any lower because of the analog sections, and the unmodified FET threshold voltages. The power otherwise wasted in driving pad and trace parasitic capacitances is avoided with the use of on-chip inductors, whose self-resonance after the process of selective removal of the silicon substrate (Fig.6) [15] is as high as it is on semi-insulating GaAs substrates. Thus, a 1-μm CMOS 900 MHz RF amplifier (Fig.6) has 30 dB gain and drains only 3 mA. The input FETs are biased at low V_{GS}–V_t to attain a large g_m/I_D. The mixer in a direct-conversion receiver must be very linear to suppress intermodulation by interferers, and must not let the local oscillator signal leak out of the antenna. Both these problems are circumvented by an unusual, uniquely CMOS solution: a sub-sampling downconversion mixer (Fig.7) [16]. The circuit draws 4 mA to acquire samples of a 900 MHz modulated waveform at a 50 MHz rate which it directly translates to baseband. The linearity, as measured by a third-order intercept of +22 dBm, exceeds that of most continuous-time 900 MHz monolithic mixers.

Key to a frequency-hopped transceiver is a low-power, agile frequency synthesizer with high spectral purity. The requirements of purity and wideband agility are at odds in a VCO-based PLL synthesizer. In this work, a direct-digital frequency synthesizer (DDFS) produces digital words representing accurate samples of a sinewave, whose frequency is set anywhere from DC to half the clock rate by an 11b input control word. A low-power 50 MHz 10b D/A Converter follows to produce a baseband spread-spectrum. A CMOS implementation of the DDFS-DAC synthesizes sinewaves up to 13 MHz with spurious levels lower than –57 dBc while dissipating only 40 mW from 3 V (Fig.8) [17]. A fixed frequency 915 MHz local oscillator, consisting of a four-stage MOS ring oscillator (Fig.9) locked in a PLL to a lower frequency crystal reference, then upconverts this spectrum to the 902-928 MHz band. The PLL bandwidth is principally optimized to suppress oscillator noise. Quadrature outputs at 915 MHz for the image-reject mixers are tapped off at diametrically opposite points to within a phase accuracy of a couple of degrees. The power amplifier consists of a binary-weighted array of FETs biased near threshold, followed by a matching network. FETs in the array are digitally selected to deliver power levels as high as 20 mW to the antenna with a 45% conversion efficiency [18].

Such a "VLSI radio" would represent a major step forward in the gradual evolution of the low-power integrated radio as described in this paper.

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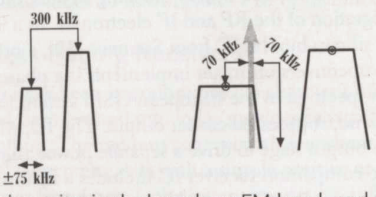


Fig.1. Channel spacing in the broadcast FM band, and the image frequency when the IF is reduced to 70 kHz.

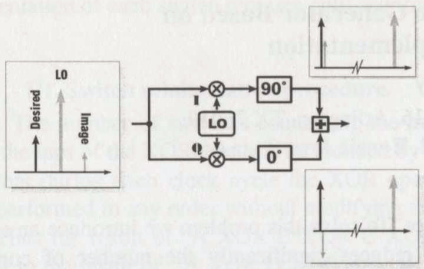


Fig.2. The image-cancelling mixer. This electronic alternative to a highly selective bandpass filter has only become practical on ICs, as the extent of image suppression depends on the matching of the two arms.

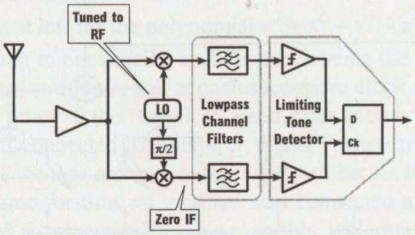


Fig.3. A simple zero IF receiver for binary-FSK signals. Including the lowpass channel filters,this may be readily integrated on a single IC.

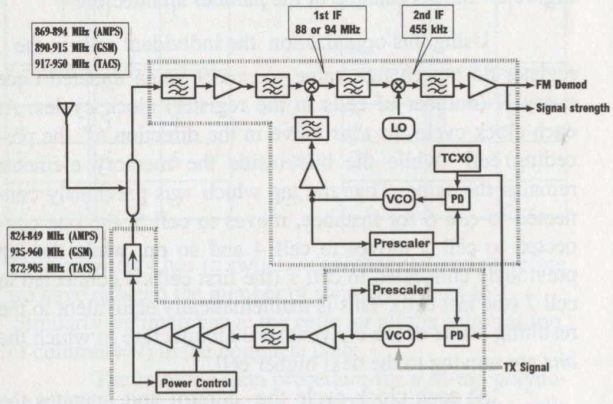


Fig.4. Architecture of a cellular telephone receiver and transmitter. Double conversion affords high selectivity, but at the expense of a large number of discrete filters.

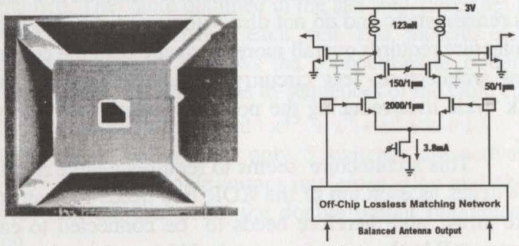


Fig.6. A 100 nH spiral inductor suspended over the silicon substrate. Self-resonance frequency is 3 GHz. A balanced CMOS RF amplifier affords 30 dB gain, 4 dB noise figure at 915 MHz.

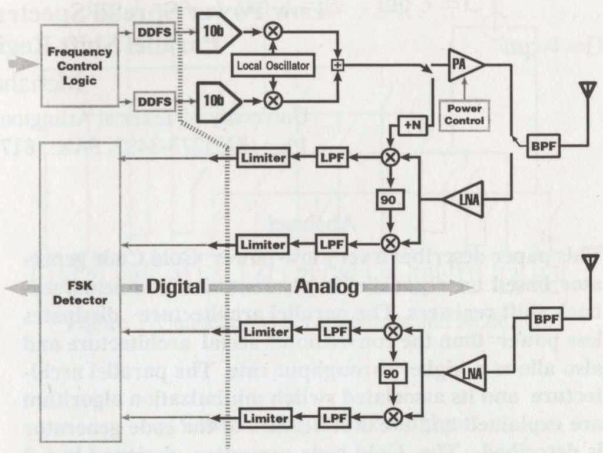


Fig.5. Architecture of the UCLA Frequency-Hopped FSK Transceiver. Two entire receive channels connected to the antennas help to combat multipath fading with spatial diversity.

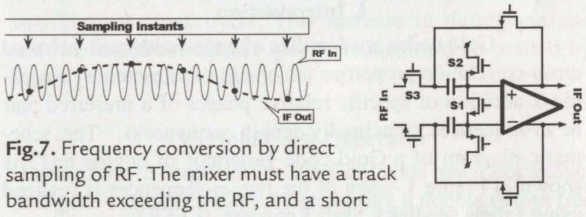


Fig.7. Frequency conversion by direct sampling of RF. The mixer must have a track bandwidth exceeding the RF, and a short sampling aperture.

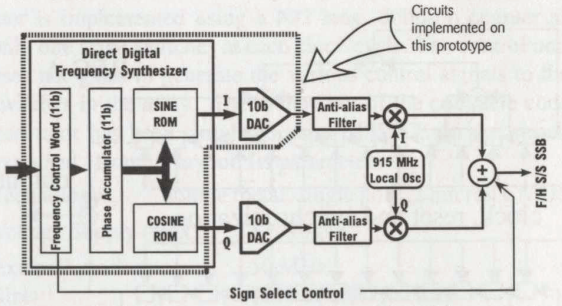


Fig.8. An agile frequency source using direct-digital frequency synthesis. Image reject mixer produces single-sideband, suppressed carrier output. Sign of summation at mixer outputs selects upper or lower sideband, so DDFS need only span 0 to 13 MHz to cover 902-928 MHz.

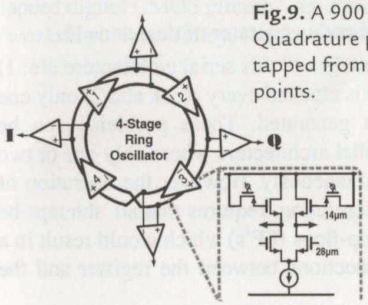


Fig.9. A 900 MHz CMOS VCO. Quadrature phases at any frequency tapped from diametrically opposite points.

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