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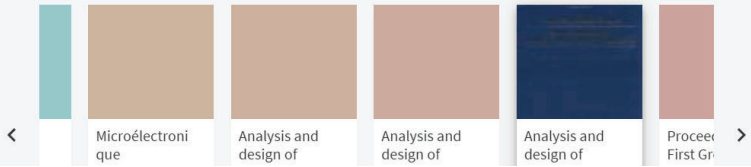
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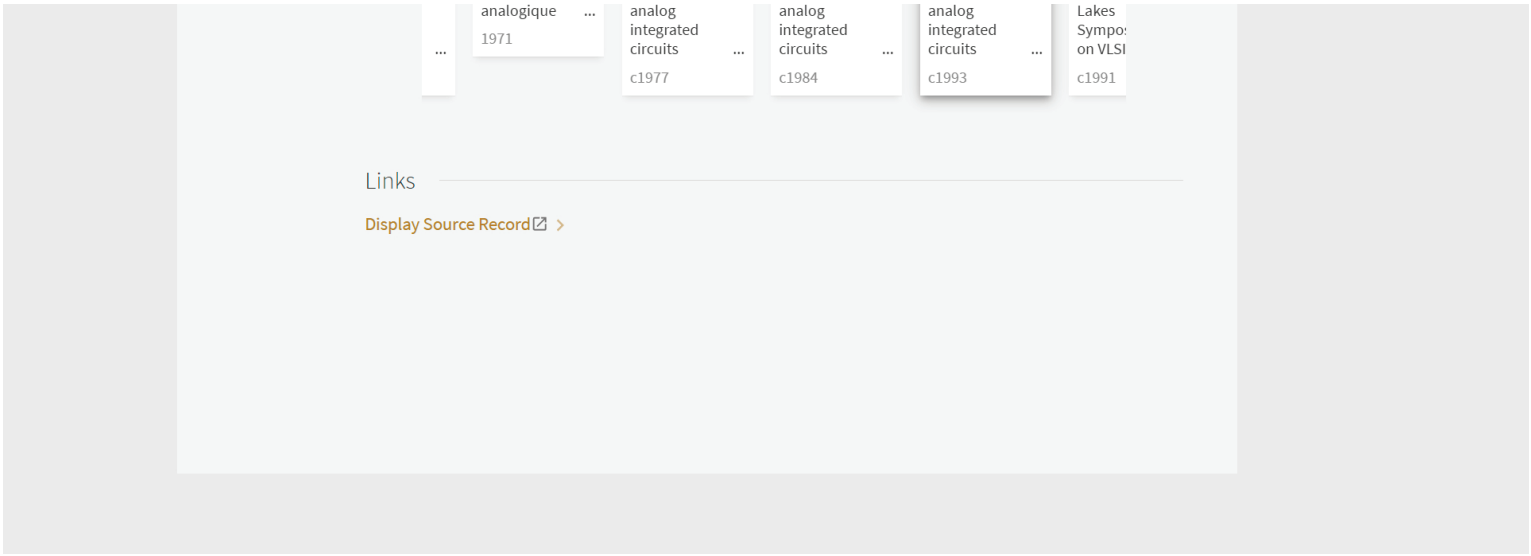
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to a short-circuit state by passing a large current through them in the reverse direction. In either case, the offset can be nulled when the devices are tested in wafer form, and the nulling does not introduce additional drift components since the collector resistances are all monolithic components of the same type. Since the resistors are binary weighted, the number of discrete steps into which the adjustment range is divided is proportional to 2^n where n is the number of fusible links in one collector. This is a powerful and low-cost technique for improving the input characteristics of monolithic precision operational amplifiers that can realize input offset voltages less than $50\,\mu$V.

Layout and Device Matching Considerations. A basic objective in the design of precision circuits like the 725 is the minimization of the input offset voltage, which requires the minimization of the mismatch between the collector resistors and the input devices.

The accuracy with which two identical transistors or resistors can be matched has a first-order effect on the attainable performance in monolithic operational amplifiers as well as many other types of analog integrated circuits such as voltage regulators (Chapter 8), analog multipliers (Chapter 10), analog-digital and digital-analog converters, voltage comparators, and others. The observed random distribution of the mismatches between two supposedly identical resistors or transistors is primarily the result of two factors:

1. Variations in the location of the edges of the resistor or transistor resulting from the limited resolution of the photolithographic process itself. This causes emitter area mismatches in bipolar transistors and length/width ratio mismatches in resistors and FETs.
2. Variations in sheet resistance and junction depth of the implanted and diffused regions across the wafer resulting from nonuniform conditions during the predeposition and/or diffusion of the impurities. This causes the resistor sheet resistance and the transistor parameters to vary with distance across the die. Ion-implanted processes have significantly better control and uniformity than diffused processes.

In addition to these random phenomena, systematic mismatches can occur from a number of causes, including errors in drawing the original mask and thermal gradients on the die. These systematic errors, however, are easily detected since they reoccur on each die, and can thus be corrected. The random fluctuations represent the basic factor limiting the attainable matching accuracy.

Since the photolithographic resolution limits the attainable matching, it is clear that the important parameter is the size of the resistor or transistor being defined in relation to the resolution. If the resistor is made wider, then the same amount of edge location uncertainty should have proportionately less effect and the matching should improve. This is indeed observed; a graph of observed resistor matching as a function of resistor width is shown in Fig. 6.29. Similarly, the matching of I_S observed in bipolar transistors improves markedly as the emitter size is made larger, as illustrated by the graph of observed matching data shown in Fig. 6.30. The increase in die size and resulting cost generally limits the size of the

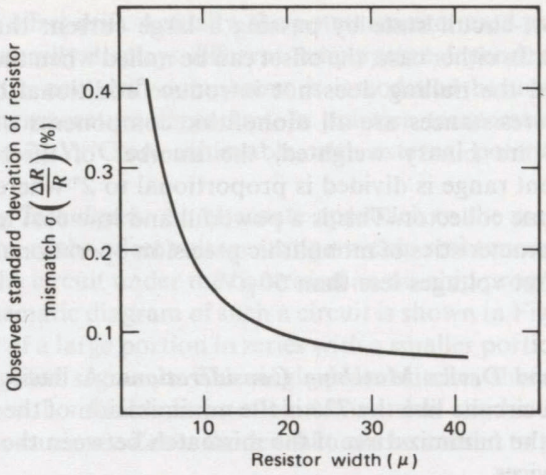


Figure 6.29 Experimentally observed standard deviation in the mismatch distribution of ion-implanted resistors with sheet resistance 250 Ω/□ and $W/L = 0.1$.

devices that can be used, but in the case of the precision operational amplifier, the input transistors and resistors are generally made as large as practicable.

The second factor limiting the matching, process-related gradients across the die, can be partially alleviated by use of appropriate geometries that cause the device mismatch to be insensitive to certain types of process gradients. Such geometries are termed common centroid, and the simplest case is illustrated in Fig. 6.31. Here the transistors making up the pair are formed from cross-connected segments of a quad of transistors. In a geometric sense, the centroid of both

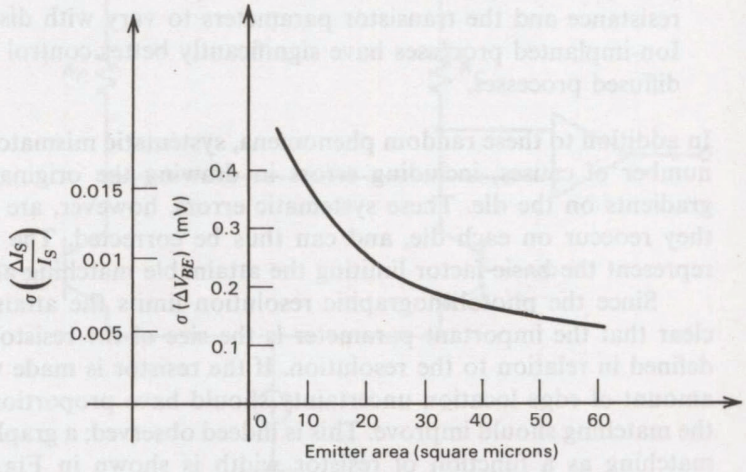


Figure 6.30 Observed standard deviation in the mismatch distribution of V_{BE} and I_S as a function of emitter area for ion-implanted bipolar transistors.

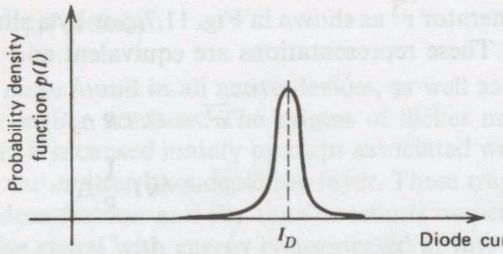


Figure 11.5 Probability density function for the diode current I. (Not to scale.)

noise signal is within these limits for 99.7 percent of the time. A brief description of the Gaussian distribution is given in Appendix A.3.1 in Chapter 3.

It is important to note that the distribution of noise in frequency as shown in Fig. 11.3 is due to the random nature of the hole and electron transitions across the *pn* junction. Consider the situation if all the carriers made transitions with uniform time separation. Since each carrier has a charge of 1.6×10^{-19} C, a 1-mA current would then consist of current pulses every 1.6×10^{-16} s. The Fourier analysis of such a waveform would give the spectrum of Fig. 11.6, which shows an average or dc value I_D and harmonics at multiples of $1/\Delta t$, where Δt is the period of the waveform and equals 1.6×10^{-16} s. Thus the first harmonic is at 6×10^6 GHz, which is far beyond the useful frequency of the device. There would be *no noise produced* in the normal frequency range of operation.

11.2.2 Thermal Noise [1,3,5]

Thermal noise is generated by a completely different mechanism from shot noise. In conventional resistors it is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. Since this source of noise is due to the thermal motion of electrons, we expect that it is related to absolute temperature T. In fact thermal noise is *directly proportional* to T (unlike shot noise, which is *independent of* T) and, as T approaches zero, thermal noise also approaches zero.

In a resistor R, thermal noise can be shown to be represented by a series

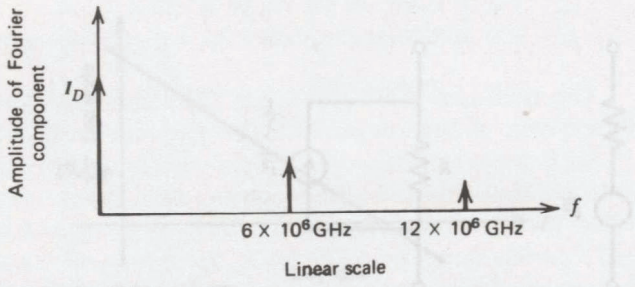


Figure 11.6 Shot-noise spectrum assuming uniform emission of carriers.

voltage generator $\overline{v^2}$ as shown in Fig. 11.7*a*, or by a shunt current generator $\overline{i^2}$ as in Fig. 11.7*b*. These representations are equivalent and

$$\overline{v^2} = 4kTR\,\Delta f \tag{11.4}$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \tag{11.5}$$

where k is Boltzmann's constant. At room temperature $4kT = 1.66 \times 10^{-20}$ V-C. Equations 11.4 and 11.5 show that the noise spectral density is again *independent* of frequency and, for thermal noise, this is true up to 10^{13} Hz. Thus thermal noise is another source of white noise. Note that the Norton equivalent of (11.5) can be derived from (11.4) as

$$\overline{i^2} = \frac{\overline{v^2}}{R^2} \tag{11.6}$$

A useful number to remember for thermal noise is that at room temperature (300°K), the thermal noise spectral density in a 1-kΩ resistor is $\overline{v^2}/\Delta f \simeq 16 \times 10^{-18}\ \text{V}^2/\text{Hz}$. This can be written in rms form as $v \simeq 4\,\text{nV}/\sqrt{\text{Hz}}$ where the form $\text{nV}/\sqrt{\text{Hz}}$ is used to emphasize that the *rms noise voltage* varies as the *square root* of the bandwidth. Another useful equivalence is that the thermal noise-current generator of a 1-kΩ resistor at room temperature is the same as that of 50 μA of direct current exhibiting shot noise.

Thermal noise as described above is a fundamental physical phenomenon and is present in *any* linear passive resistor. This includes conventional resistors and the radiation resistance of antennas, loudspeakers, and microphones. In the case of loudspeakers and microphones, the source of noise is the thermal motion of the air molecules. In the case of antennas, the source of noise is the black-body radiation of the object at which the antenna is directed. In all cases, (11.4) and (11.5) give the mean-square value of the noise.

The amplitude distribution of thermal noise is again Gaussian. Since both shot and thermal noise each have a flat frequency spectrum and a Gaussian amplitude distribution, they are indistinguishable once they are introduced into a circuit. The waveform of shot and thermal noise combined with a sinewave of equal power is shown in Fig. 11.21.

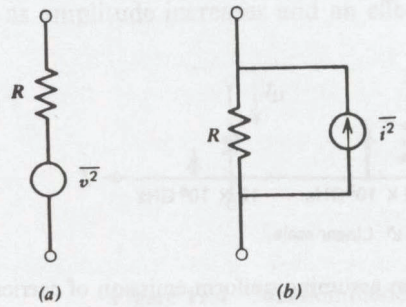


Figure 11.7 Alternative representations of thermal noise.

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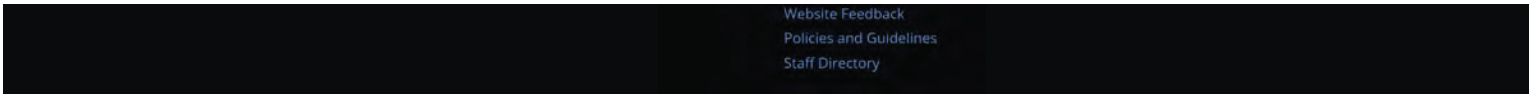
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Appendix KNOLLMAN02

Designing with op amps: Single-formula technique keeps it simple

DIETER KNOLLMAN, PHD, LUCENT TECHNOLOGIES

A simple single-op-amp design technique uses one formula—R_F/|gain|—for both positive and negative gains. The procedure works for all gain settings and produces designs with minimal bias-current error.

Numerous texts and application notes describe the design of op-amp circuits. Most designers use the R_F/R_I formula for inverting amplifiers and the $1+R_F/R_I$ formula for noninverting amplifiers, where R_F and R_I are the feedback and input resistors, respectively. These two formulas have been the basis of op-amp design for many years. Why learn a new procedure? One reason is that the new procedure is simple in that it uses the same formula—R_F divided by the magnitude of the gain—for both positive and negative gains.

Second, the procedure is universal and works for all sets of gains. Although you can use classic methods to design op-amp circuits with multiple negative-gain inputs and a single positive-gain input, circuits with multiple positive-gain inputs are difficult to design using classic methods. Another reason to learn this new procedure is that it creates designs that always exhibit minimal bias-current error.

The design procedure relies on two new circuit concepts: a gain formula and a circuit theorem (see **box** "Theoretical background") and is based on the following definitions and assumptions:

- The procedure applies to single op-amp circuits with any number of positive- and negative-gain inputs, and the op amp is ideal.
- All inputs are ideal voltage sources.
- Ground acts as an input and is a voltage source of value zero.
- If the input has a source impedance, the source impedance is part of the circuit.
- Gain is defined as the gain from the ideal voltage source to the op-amp output.
- The feedback resistor, R_F, connects from the op-amp output to the inverting input.
- The input resistor, R_I, connects from the ideal voltage source input to the op-amp input. Positive-gain inputs connect to the noninverting op-amp input terminal, and negative-gain inputs connect to the inverting op-amp input terminal. This definition differs from standard usage. In classic circuit analysis, the input resistor always connects to the inverting op-amp input. The R_I notation emphasizes the difference.
- The circuit's input im-pedance is equal to R_I only for negative inputs. For positive inputs, R_I is the impedance that connects the input to the noninverting op-amp terminal.

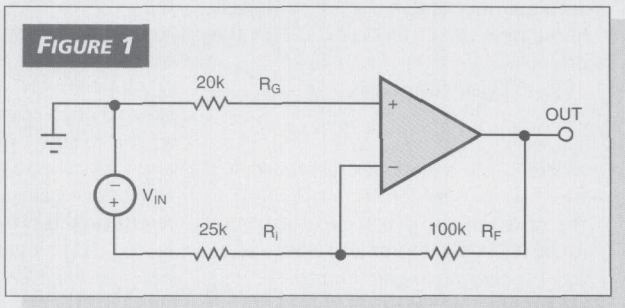
To implement the design, you must first specify the desired circuit gains. You then must calculate the ground gain, as follows:

Ground gain=1–the sum of the positive and negative gains from the desired circuit gains.

In other words, ground gain+Σcircuit gains=1. You must now choose a feedback-resistor value. For example, let R_F=100 kΩ. Next, calculate the resistor values for each input, including the ground-gain resistor, using $R_{I,G}=R_F/|gain|$.

You can have any number of positive-gain and negative-gain inputs, and each input must have a defined gain. Ground gain=1–sum of gains. Some op-amp circuits need a resistor to ground from the op amp's inverting input, and

FIGURE 1



To design an inverting amplifier with a gain of –4 and an R_F of 100 kΩ, you connect an R_I of 25 kΩ to the inverting input and an R_G of 20 kΩ to the noninverting input.

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OP-AMP DESIGN PROCEDURE

others need a resistor to ground on the noninverting input. The sign of the ground gain determines where to place the ground resistor. For positive ground gains, you connect the resistor to the op amp's noninverting terminal; for negative ground gains, you connect the resistor to the inverting terminal. If the desired gains add up to one, a ground resistor is unnecessary.

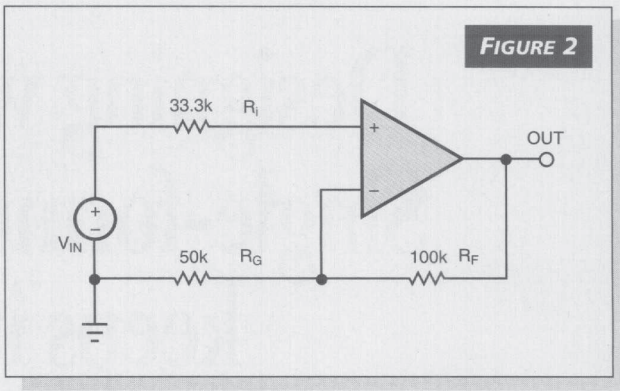
The feedback resistor you choose can theoretically be any value, but op-amp and circuit considerations usually limit the range of acceptable values. Selecting a feedback-resistor value that is a multiple of the gains avoids fractional values for the input resistors. Calculate the input resistor values as R_F divided by the magnitude of the gain for both positive and negative gains.

For those op-amp experts who have their doubts, consider an example: Design an inverting amplifier with a gain of –4. Thus, the circuit needs a ground gain equal to +5. Selecting R_F=100 kΩ yields an input-resistor value, R_I, of 25 kΩ and a ground-gain input-resistor value, R_G, of 20 kΩ (**Figure 1**). The –4-gain input resistor connects to the op amp's inverting input. The +5 ground-gain resistor connects to the noninverting input. The design of this inverting amplifier is similar to that of a classic inverting amplifier. The new procedure adds a ground resistor at the noninverting op-amp input. This ground resistor is necessary only to minimize bias-current error.

The noninverting op-amp input terminal sees a resistance of 20 kΩ looking into the circuit. The resistance at the inverting op-amp input is the parallel combination of the 100-kΩ feedback resistance and the 25-kΩ input resistance. Because the parallel resistance of 25-kΩ and 100-kΩ is 20-kΩ, both op-amp terminals see the same resistance looking into the circuit. The voltages that the op-amp bias current produces at the op-amp inputs are equal. The bias current creates only a common-mode input, which the op-amp rejects. Thus, the 20-kΩ grounded input resistor minimizes the bias-current error for this example.

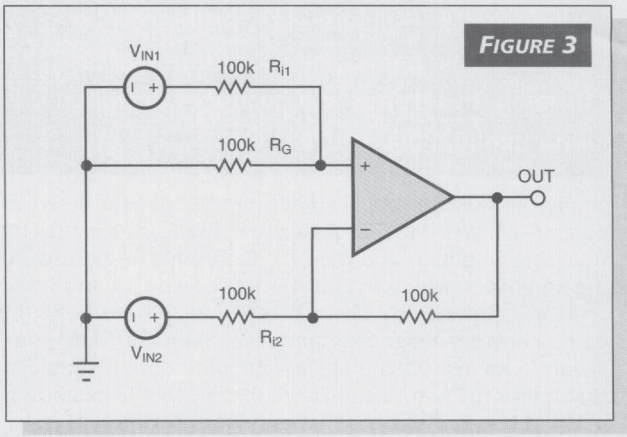
In another example, consider the design of a noninvert-

FIGURE 2



A noninverting amplifier with a gain of +3 and an R_F of 100 kΩ requires an R_I of 33.3 kΩ connected between the input and the noninverting terminal and an R_G of 50 kΩ connected between the inverting terminal and ground.

FIGURE 3



A differential amplifier with gains of +1 and –1 requires a ground gain of +1. With R_F=100 kΩ, all input resistors, including the ground resistor, are 100 kΩ.

THEORETICAL BACKGROUND

The design technique uses a new op-amp gain formula, Plato's gain formula, and a new circuit theorem, Daisy's theorem.

Plato's gain formula is

$$\text{gain}=p\times R_F/R_I,$$

where R_F is the feedback resistance, R_I is the resistor that connects the input to the op amp, and p is a circuit constant for positive-gain inputs and always equal to –1 for negative-gain inputs. For negative gains, Plato's gain formula is simply the classic R_F/R_I gain formula.

For positive gains, this formula differs from classic analysis. In classic analysis, the positive gain is the gain from the source to the noninverting op-amp terminal times $1+R_F/R_I$.

Alternatively, Plato's gain formula states that you can express positive gains as the product of a circuit-constant p and R_F/R_I. The value of p is the same for all positive gains in a given circuit. Different circuits may have different values for p. Don't assume p=1 for existing designs. For new designs, setting p=1 simplifies the formula and creates a better design. The only value that minimizes bias-current error is p=1.

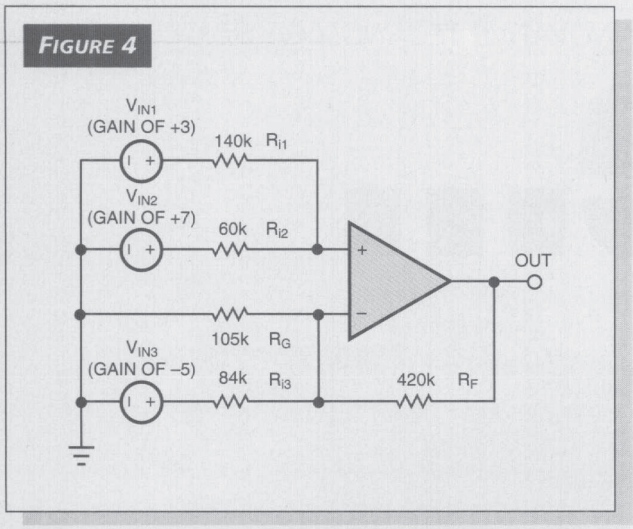
Daisy's theorem, which you use to determine the ground gain, is as follows:

The sum of the gains=1.

The design procedure assumes that the circuit inputs are ideal voltage sources and that ground is a voltage input of value 0. The overall gain is the gain from the ideal voltage source to the op-amp output. For new op-amp circuits, Daisy's theorem specifies whether a ground resistor is necessary at the op amp's noninverting or inverting input and specifies the magnitude of the ground gain.

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OP-AMP DESIGN PROCEDURE



The procedure makes it easy to design an op-amp circuit with multiple positive-gain inputs.

ing op-amp circuit with a gain of +3. Thus, the circuit needs a ground gain of –2. With R_F=100 kΩ, the input resistor, R_I, is 100 kΩ/3=33.3 kΩ, and the grounded input resistor, R_G, is 100 kΩ/2=50 kΩ (**Figure 2**). The 33.3-kΩ resistor is necessary only to minimize the bias-current error. Note that 33.3 kΩ is equal to the parallel resistance of 50 and 100 kΩ.

Classic design states that the gain of a noninverting amplifier is $1+R_F/R_I$. In this case, R_I of the classic case is equivalent to the ground-gain resistor, R_G. Thus, the ground gain of **Figure 2** is equal to $-R_F/R_G$. Adding the input gain (+3) and ground gain (–2) yields the gain sum of 1. For noninverting amplifiers, the positive-gain input resistor, R_i, is necessary only to minimize the bias-current error.

In another design example, consider a differential amplifier with gains of +1 and –1, corresponding to inputs V_{IN1} and V_{IN2}, respectively. Thus, the circuit needs a ground gain of +1. With R_F=100 kΩ, all resistor values—R_{i1}, R_{i2}, and R_G—are 100 kΩ (**Figure 3**). In this circuit, R_G acts as an attenuator for the positive-gain input, V_{IN1}. Note that the equivalent resistance at each op-amp input terminal is the same.

You can check this design using the classic formulas. The gain from the op amp's inverting input is 100 kΩ/100 kΩ=1. The gain from V_{IN1} to the op amp's noninverting input is 0.5. The gain from the op amp's noninverting input to the output is $1+R_F/R_{i2}$=2. Thus, the gain from V_{IN1} to the output is 0.5×2=1.

In another example, design a summing amplifier with gains of +3, –5, and +7. The presence of two positive gains makes this example difficult to design using classic methods. The input gains are +3, +7, and –5, which add up to +5. Thus, a ground gain of –4 is necessary. With R_F=420 kΩ, positive-gain input-resistor R_{i1} is 420 kΩ/3=140 kΩ, and positive-gain input-resistor R_{i2} is 420 kΩ/7=60 kΩ. The negative-gain input resistor, R_{i3}, is 420 kΩ/5=84 kΩ. The ground-gain input resistor is 420 kΩ/4=105 kΩ (**Figure 4**).

Note that the op amp's input terminals see the same equivalent resistance: 140 kΩ||60 kΩ=105 kΩ||84 kΩ||420 kΩ. The gain from V_{IN1} to the op amp's noninverting input is 60 kΩ/(60 kΩ+140 kΩ)=0.3. The gain from the noninverting input to the output is equal to $1+R_F/(R_{i3}||R_G)$=1+420 kΩ/(84 kΩ||105 kΩ)=10. Thus, the gain from V_{IN1} to the output is 0.3×10=3. You can verify the gains from V_{IN2} and V_{IN3} to the output in a similar manner. EDN

Author's biography



Dieter Knollman, PhD, is a distinguished member of the technical staff of Lucent Technologies (Denver), where he has worked for 33 years. In his current position, he designs PBX port circuits. Knollman earned a BSEE from the Virginia Polytechnic Institute and State University (Blacksburg, VA) an MSEE from the University of Illinois—Urbana/Champaign, and a PhD from New York University (New York).

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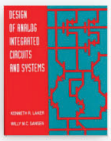
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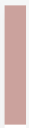

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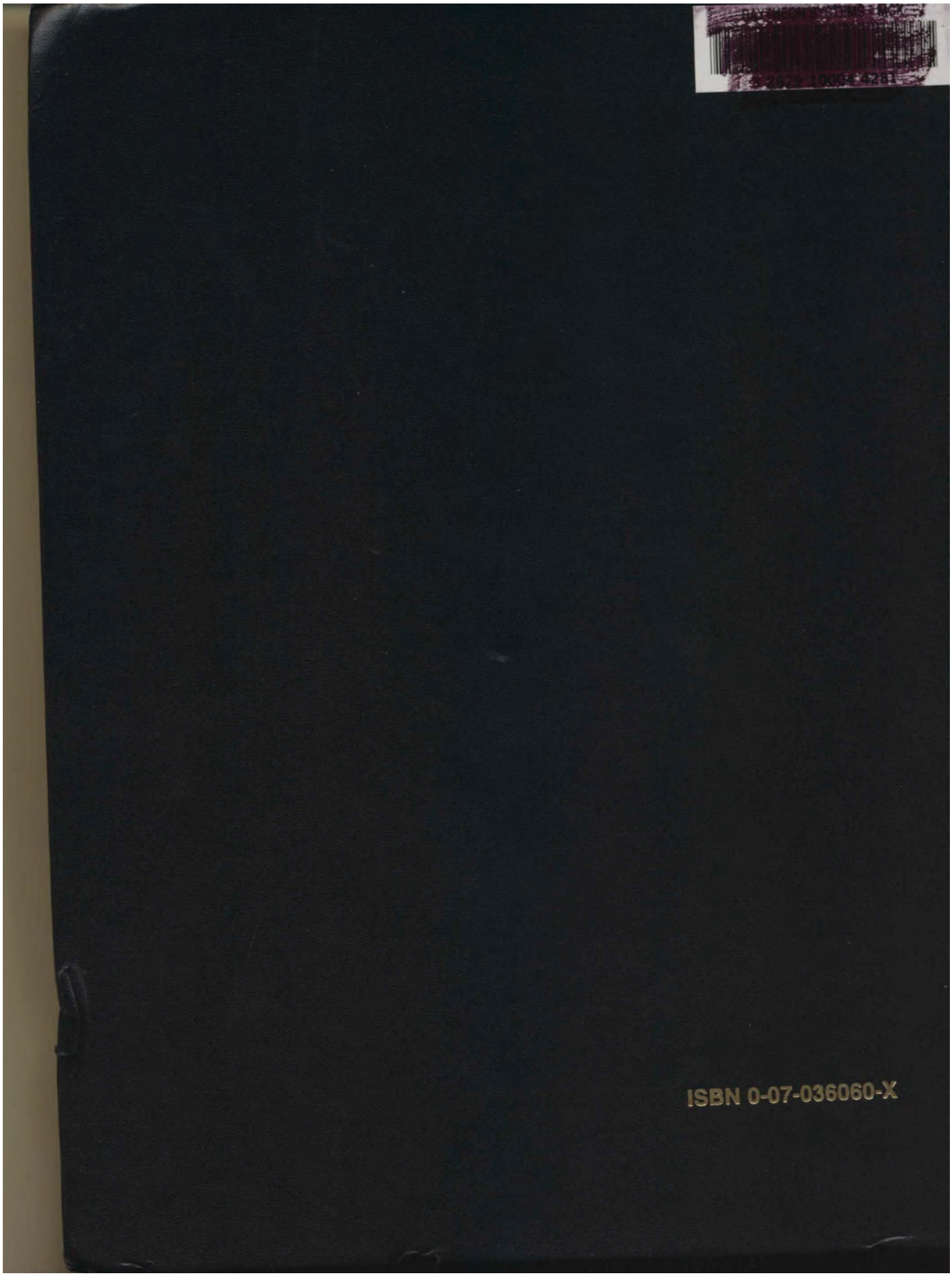
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Example 2-13

What is the cutoff frequency for a 1 kΩ resistor, realized in p-base diffusion with $R_R = 130\ \Omega/\square$ and $C_R = 0.2$ pF/□. Calculate the frequency at which the parasitic capacitance causes a phase shift of 10° with respect to low frequencies.

Solution. For 1 kΩ, 8 squares are needed. As a result, $f_{RC} = 15\ \text{GHz}/(L/W)^2$ or 15 GHz/64 = 230 MHz. A phase shift of 10° is reached at the frequency f_{10} where $tg(10°) = f_{10}/f_{RC}$ or at about 40 MHz.

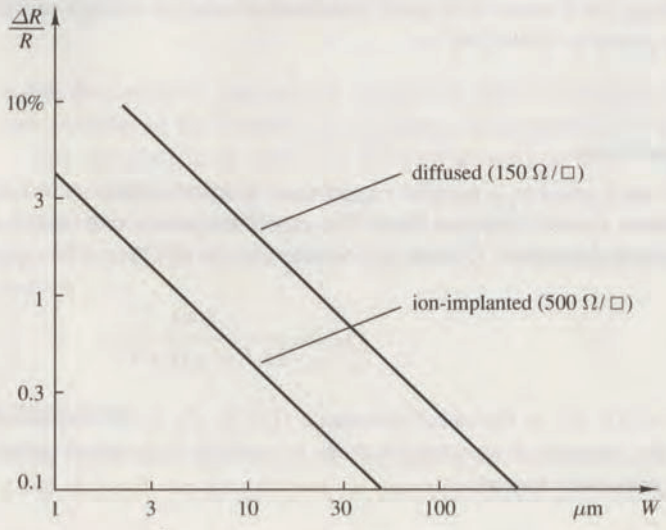
2-9-6 Absolute and Relative Accuracy

To realize a resistor with absolute accuracy is difficult, but layout tricks can be applied to reduce the uncertainties. For example, the contact and corner areas can be covered with $p+$ islands. Nevertheless, good design must never be based on absolute values. Relative values such as resistor ratios must be used. The relative errors obtained are about one-tenth of the absolute accuracies given in Table 2-6. Obviously, the larger the dimensions, the better the relative accuracy that can be achieved.

This is illustrated in Fig. 2-31 for both diffused (base diffusion: 150 Ω/□) resistors. The relative accuracy improves more or less proportionally to the resistor width. Moreover, the relative error is approximately a factor of three smaller for ion-implanted devices than for diffused ones. In order to reach a relative error of 0.1 percent, ion-implanted resistances must be taken with about 40 μm width.

Many other layout tricks (see Sec. 6-7) can be applied to improve matching.

FIGURE 2-31 Matching of resistors with width W.



2-9-7 Resistors in a CMOS Process

In a conventional n-well CMOS process, several resistances are available. They are the source/drain resistance, the polysilicon gate and the n-well region. However, none of these are intended to be used as a resistor. The control on the accuracy of the resistivity is very poor (see Table 2-6). An analog CMOS process quite often includes an additional polysilicon resistor with excellent properties. Its temperature and voltage coefficient are then low as well.

2-9-8 Thin Film Resistors

On top of a chip, a thin-film resistor can be easily deposited. Actually, the aluminium metallization layer is such a resistor, albeit with very low resistivity. A higher resistivity is obtained with NiCr or Ta, which yield values from 100 to 4 k $\Omega/\square$. The control on its resistivity is excellent and so are its temperature and voltage coefficient. This is why they are used for very high precision circuits and for circuits at very high frequencies.

2-9-9 Capacitors

In a bipolar process, junction capacitance is available at each junction. The most useful is the collector-base junction capacitance (see Table 2-7), shown in Fig. 2-32. It is not very accurate, however, and it is very voltage dependent (see Table 1-5). This applies to all other junction capacitances as well.

Note that the capacitance on the bottom side is always connected by a parasitic capacitance C_p to the substrate. This capacitance is always a fixed fraction of the useful capacitance and cannot be avoided.

Much more accuracy can be obtained with a MOS capacitance in a CMOS process (see Fig. 2-33). Not only is its value larger, but its accuracy is much higher, especially for the poly-to-poly capacitance. Also, the temperature and voltage coefficients are quasi-nihil. Its parasitic capacitance from the bottom plate to ground is decreased to

TABLE 2-7 CAPACITORS

Process	Type	C nF/cm^2	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent V	breakdown voltage V
Bipolar	C_{CB}	16	10	0.02	2	50
	C_{EB}	50	10	0.02	1	7
	C_{CS}	8	20	0.01	0.5	60
CMOS	C_{ox}(50 nm)	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	2	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20