

Patent Owner Demonstrative

Texas Instruments Incorporated (Petitioner)

v.

ParkerVision Inc. (Patent Owner)

Cases: IPR2024-00935, -01066

U.S. Patent No. 7,865,177

Oral Hearing: September 10, 2025

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

1

Conception: at least as early as Jan. 20, 1998

Reduced To Practice: at least as early as April 29, 1998

Conception

Sorrells' Testimony:

5. In the summer of 1996, ParkerVision began to design its first integrated circuit (IC) chip called "Eddie." ParkerVision completed the design of the Eddie chip by early 1997. [REDACTED]
[REDACTED]
[REDACTED]
6. By early 1997, ParkerVision completed the layout for the Eddie chip.
7. The layout of the first Eddie chip can be found in a file [REDACTED] (Exhibit 2012).

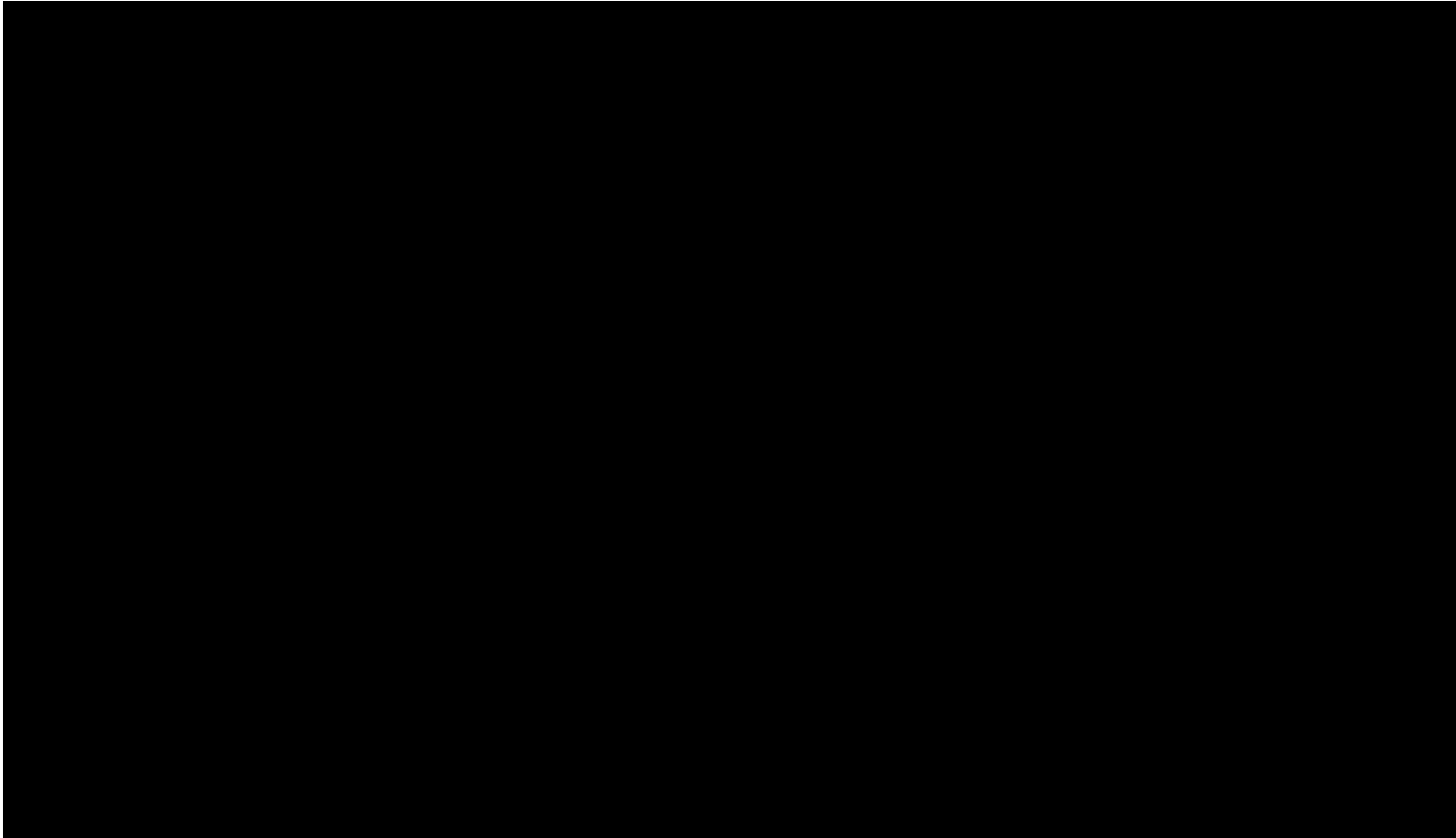
Conception

POR, 26-29; Ex. 2016, ¶¶5-10; Ex. 2012.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

4

Layout Label and Filename Are Near Identical



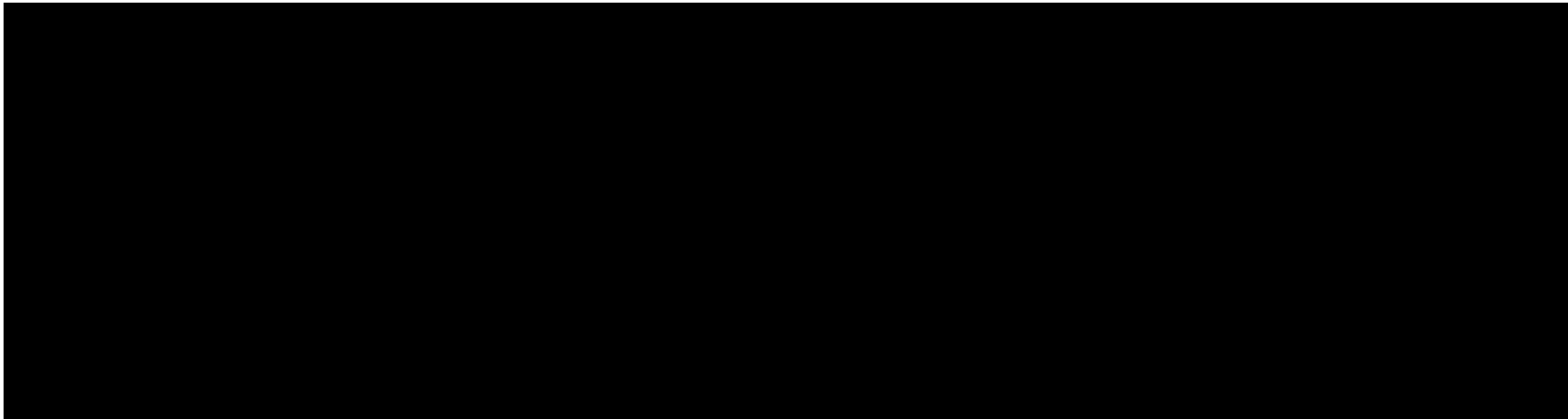
Reply, 2-4; Sur-Reply, 21; Ex. 2016,
¶¶5-10; Ex. 2012.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

5

Conception

Sorrells' Testimony:



Conception

Sorrells' Testimony:

14. As can be seen below in the bottom right corner of the schematic (expanded below), it has a file name of [REDACTED] and date of January 20, 1998 on its face. It was our practice at the time to date our schematics with the actual date the schematic was created. This date is consistent with the time that the ParkerVision team and I were working on the schematic of the circuit board for the Eddie chip.

15. As can be seen below in the metadata from a Relativity database, the file [REDACTED] was last modified on February 26, 1998. This date is consistent with the time that the ParkerVision team and I were working on the schematic of the circuit board for the Eddie chip.

Conception

POR, 26-29; Ex. 2016, ¶¶13-15; Ex. 2011.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

8

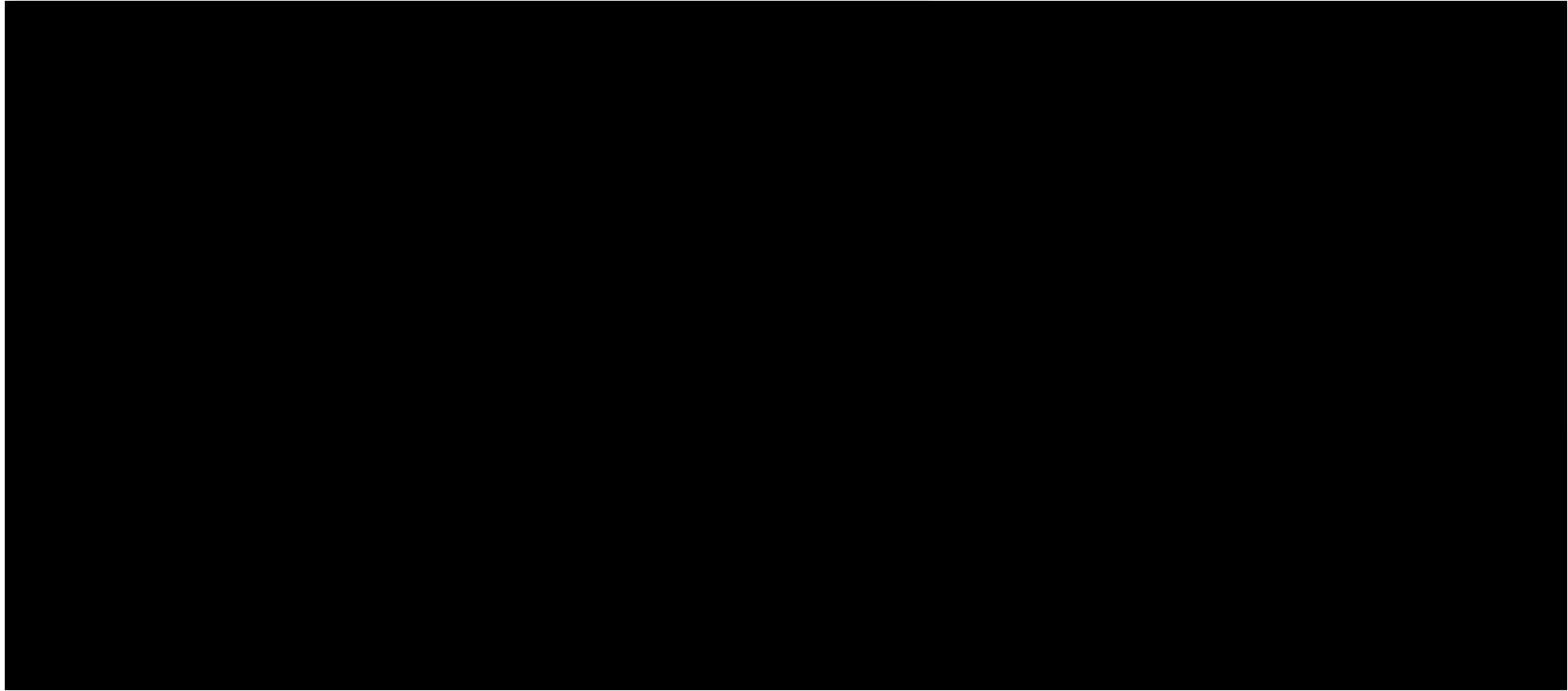
Conception

Sorrells' Testimony:

11. Below is a schematic of an early version of a circuit board (Exhibit 2014) that ParkerVision designed for mounting the Eddie chip.

12. As can be seen below in the bottom right corner of the schematic (expanded below), it has a date of August 21, 1997 on its face. It was our practice at the time to date our schematics with the actual date the schematic was created. This date is consistent with the time that the ParkerVision team and I were working on the schematic of an early circuit board for the Eddie chip.

Conception



POR, 26-29; Ex. 2016, ¶¶11-12; Ex. 2014.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

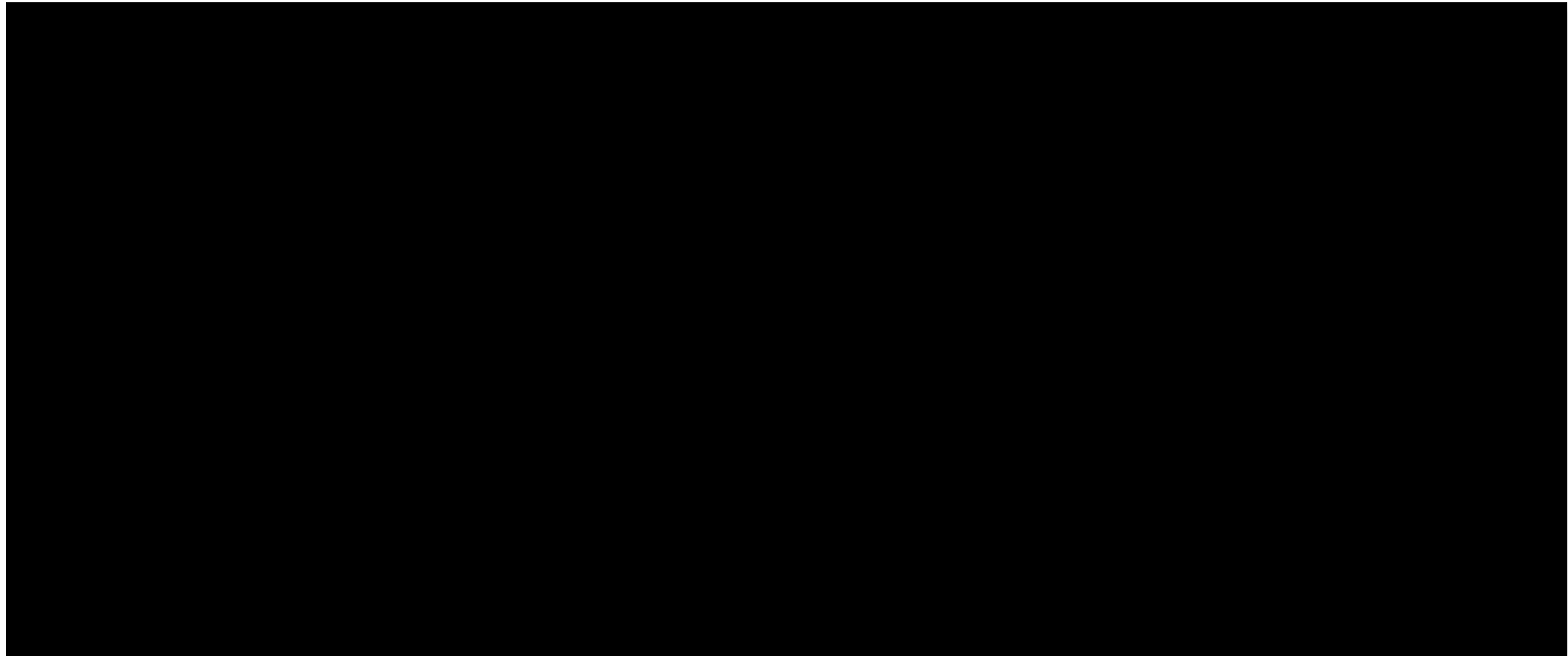
10

Conception

Sorrells' Testimony:

16. The layout of the circuit board (Exhibit 2013) can be seen below left and the schematic of the circuit board can be seen below right. Part 63 is shown both on the circuit board layout and schematic and represents the location of the Eddie chip on the circuit board. The layout of the circuit board was created in 1997.

Conception



POR, 26-29; Ex. 2016, ¶16; Exs. 2011, 2013. DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

12

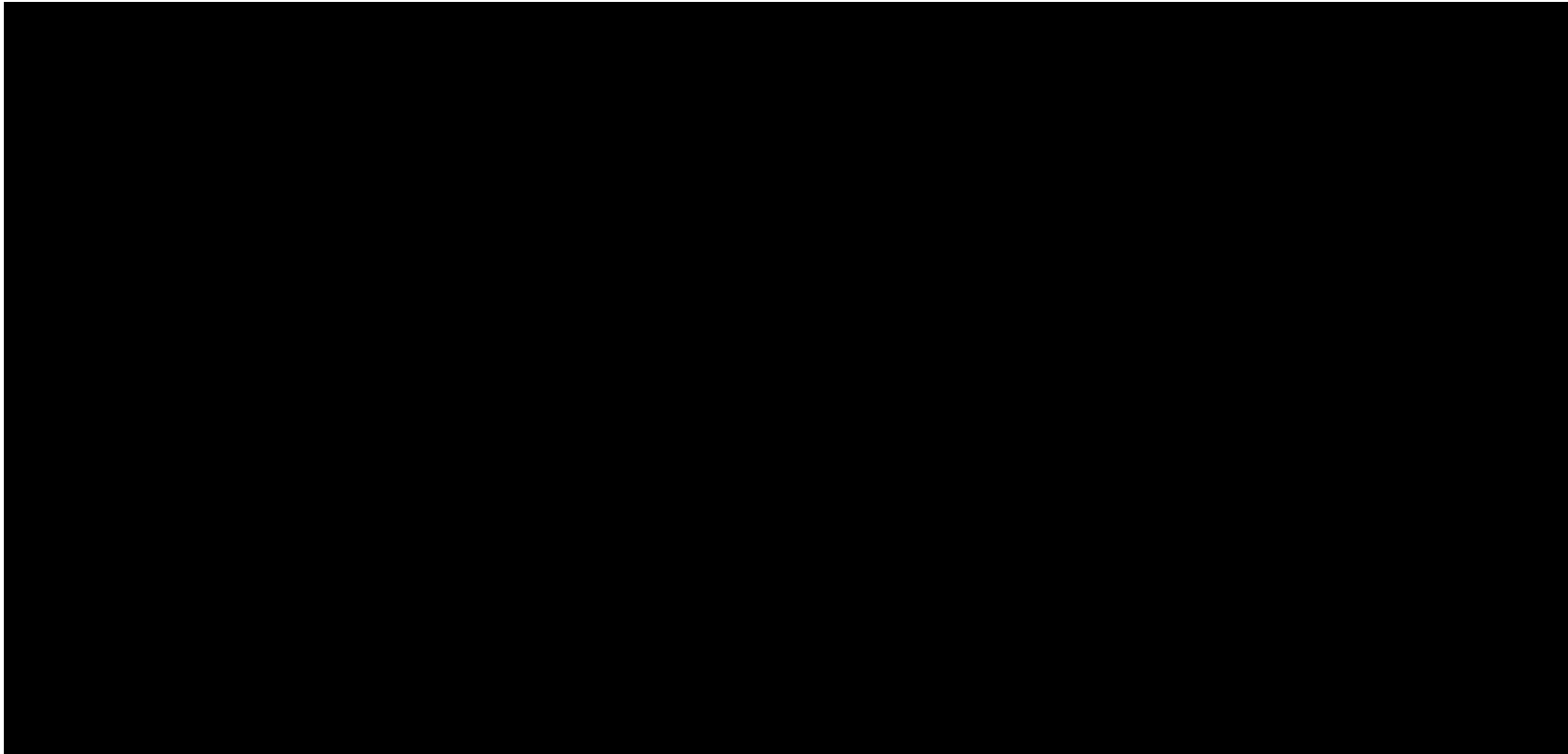
Conception

Sorrells' Testimony:

26. Below is an annotated version of the Eddie chip layout showing the the correspondence between the connections on the layout (below left) and the connections on the schematic of the circuit board (expanded below right). The



Conception



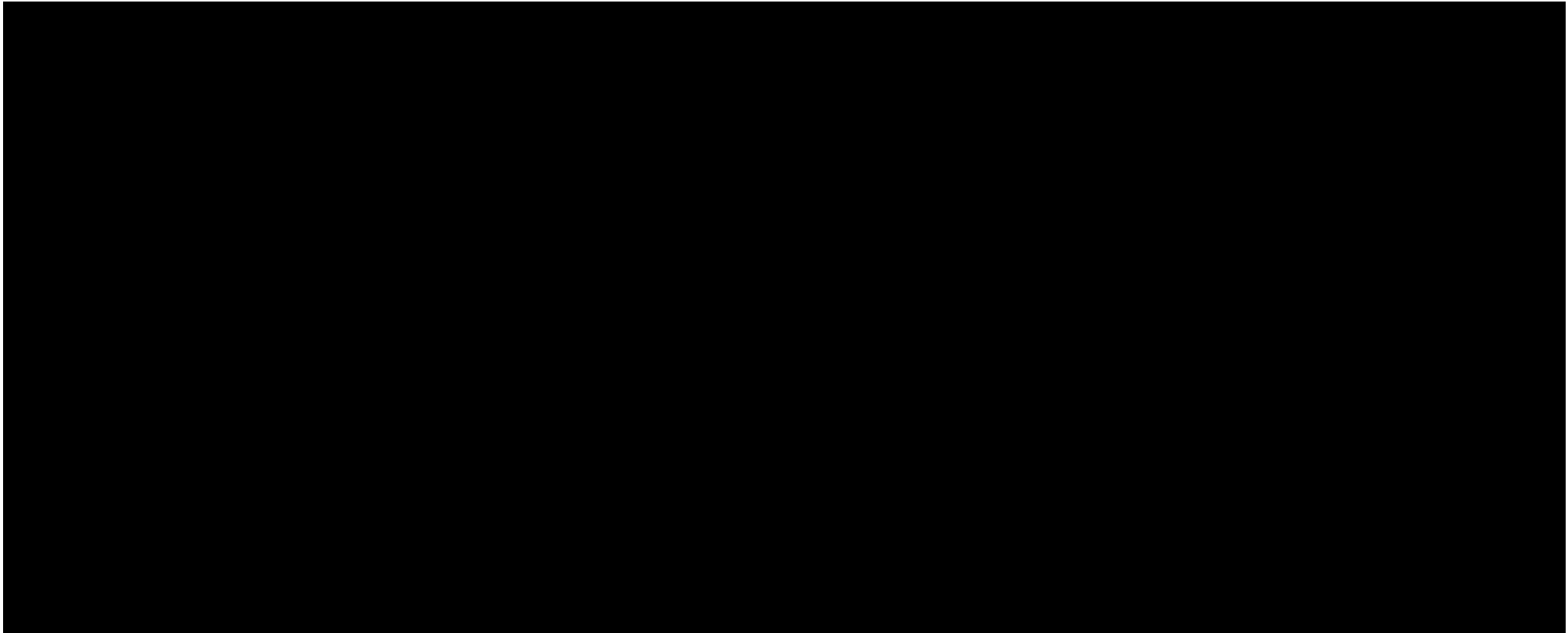
Conception

Sorrells' Testimony:

5. In the summer of 1996, ParkerVision began to design its first integrated circuit (IC) chip called "Eddie." ParkerVision completed the design of the Eddie chip by early 1997. [REDACTED]

[REDACTED]

Conception

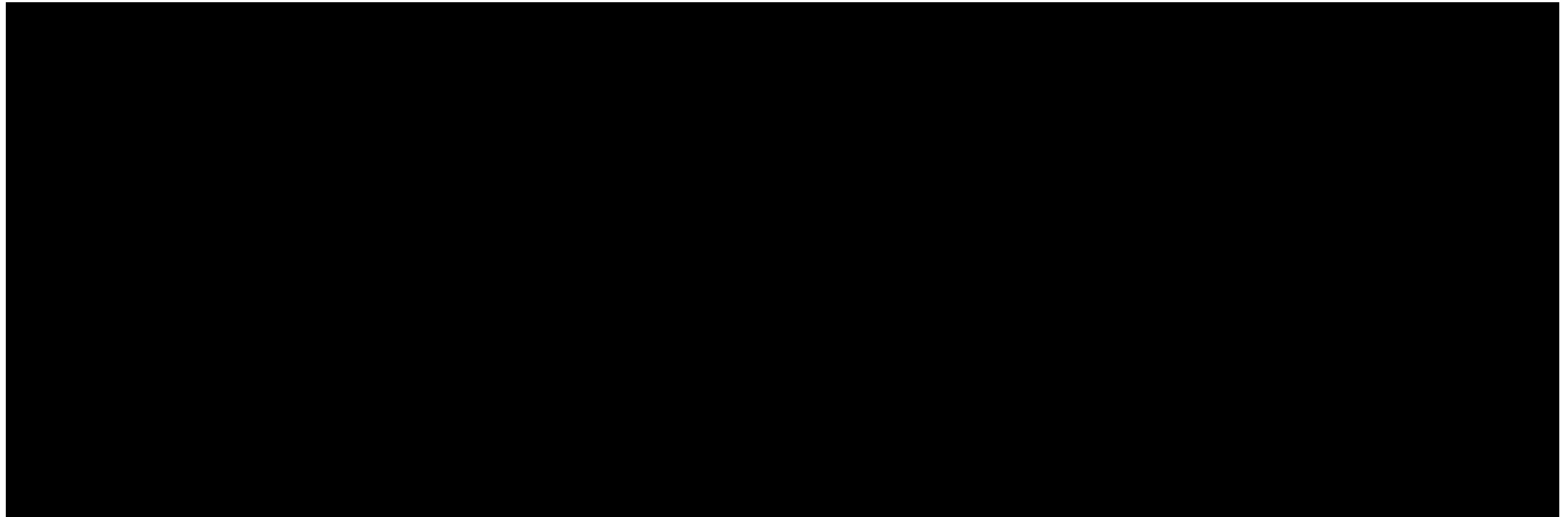


POR, 41-42 Reply, 5, 22-23; Sur-Reply, 21-22;
Exs. 2010, 2012, 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

16

Conception/Reduction to Practice



Reply, 5, 22-23; Sur-Reply, 21-22; Ex. 2016, ¶15; Exs. 2010, 2012, 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

17

Eddie Device Uses

'551 Patent:

Thus, the apertures 4701 can be approximately $\frac{1}{10}$, $\frac{1}{4}$, $\frac{1}{2}$, $\frac{3}{4}$, etc., or any other fraction of the period of the EM signal. Alternatively, the apertures 4701

Conception/Reduction to Practice

Sorrells' Testimony:

17. In 1997, ParkerVision chose [REDACTED] as its foundry to build the Eddie chip. The [REDACTED] agreement is shown in Exhibit 2027.

18. By no later than the first quarter of 1998, [REDACTED] provided ParkerVision with a fabricated Eddie chip using [REDACTED]

[REDACTED]

Conception/Reduction to Practice

POR, 26-29; Ex. 2016, ¶¶17-19; Ex. 2027.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

20

Reduction to Practice

Sorrells' Testimony:

20. By the first quarter of 1998, ParkerVision tested and evaluated the combined Eddie chip and circuit board. By the first quarter of 1998, ParkerVision issued press releases discussing testing/evaluation of the Eddie chip including the [REDACTED] Ex. 2019, Ex. 2020.

21. The dates of the press releases are consistent with my recollection of the date by when ParkerVision tested/evaluated the Eddie chip and circuit board. ParkerVision's internal testing/evaluation showed that the combined Eddie chip and circuit board worked for its intended purpose of down-converting an RF signal.

Reduction to Practice

FOR IMMEDIATE RELEASE

DECEMBER 10, 1997

Contact: Jeffrey Parker
President and CEO

ParkerVision Announces Breakthrough in Wireless Radio Frequency Technology

Company Invents the First Universal Direct Conversion Receiver IC's

Low Cost/High Performance RF Receiver Chips Now Available

The first generation of the technology has been incorporated into an integrated circuit (IC) which has been code named "Eddie".

Reduction to Practice

FOR IMMEDIATE RELEASE

Contact: Carolyn Wrenn
Director of Investor Relations

LABORATORY TESTS VERIFY PARKERVISION WIRELESS TECHNOLOGY

**- Testing Confirms The Ability to Create Single Chip High Performance/Low Cost RF
Receivers -**

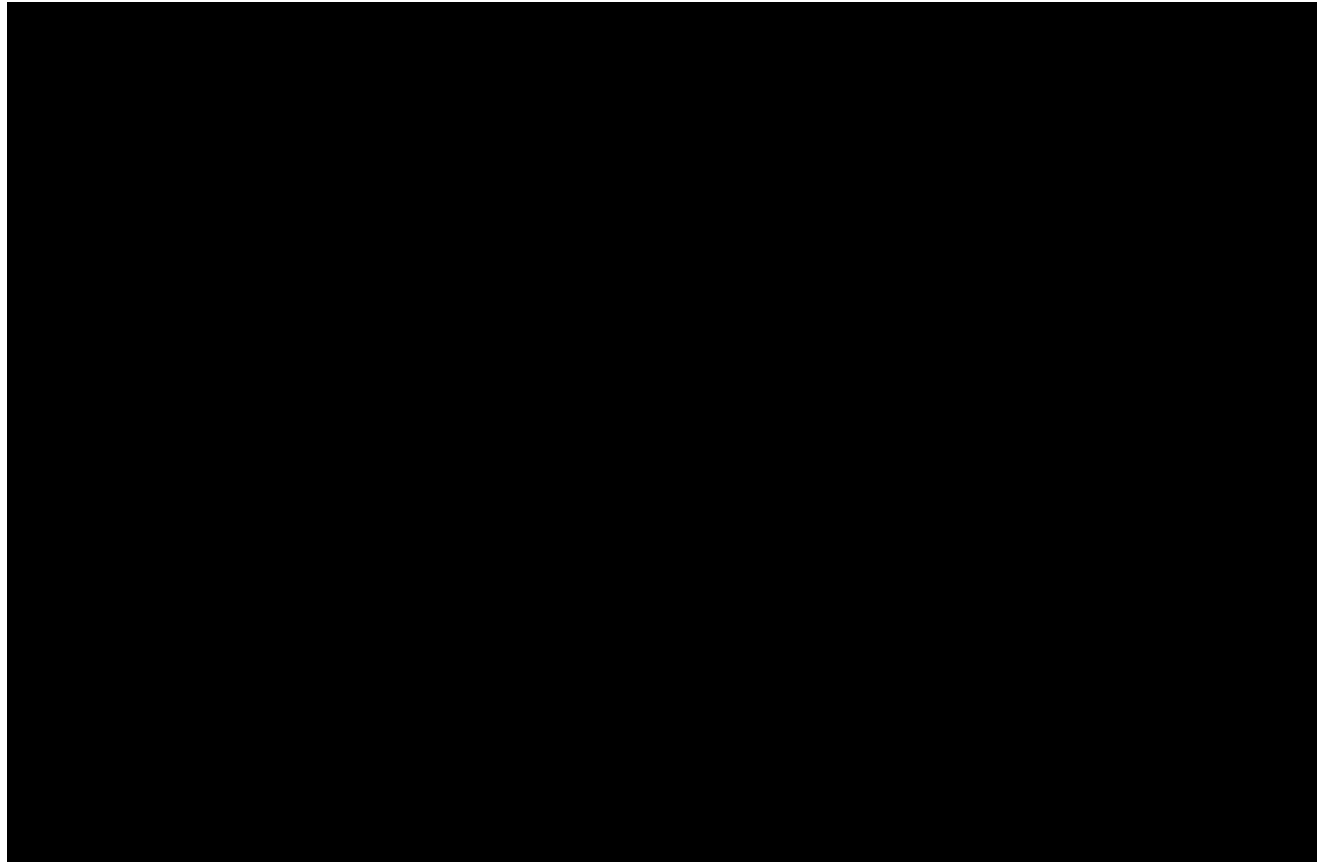
JACKSONVILLE, FLORIDA, **March 3, 1998**—PARKERVISION, INC. (NASDAQ NM SYMBOL PRKR), today announced that **The Boeing Company has completed a series of test measurements** for ParkerVision's recently announced Universal Direct Conversion Receiver and its first integrated circuit (IC) which has been code-named **'Eddie'**. ParkerVision said that the Boeing tests and those performed by ParkerVision internally are in accord.

Reduction to Practice

Sorrells' Testimony:

22. By the first quarter of 1998, ParkerVision sent the combined Eddie chip and circuit board to be tested by an independent testing company – [REDACTED] – to verify the performance of the combined Eddie chip and circuit board discussed above. ParkerVision and [REDACTED] entered into an agreement. Exhibit 2021. Boeing conducted tests in at least February and April 1998. Some testing notes and pictures from [REDACTED] test are shown in Exhibit 2022. I was present and observed some of the testing.

Reduction to Practice

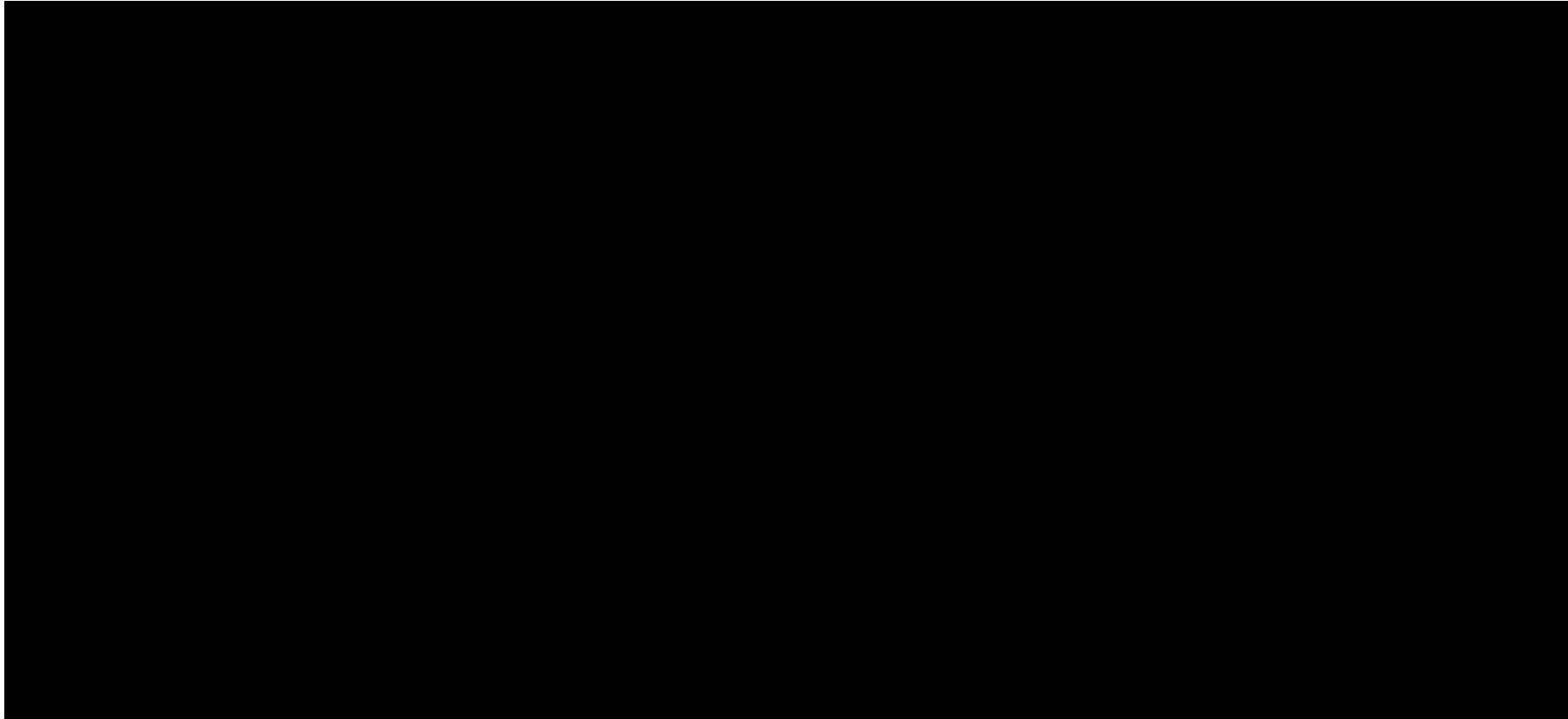


POR, 26-29; Ex. 2016, ¶22; Ex. 2021.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

25

Reduction to Practice



POR, 26-29; Ex. 2016, ¶¶23-24; Ex. 2010.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

26

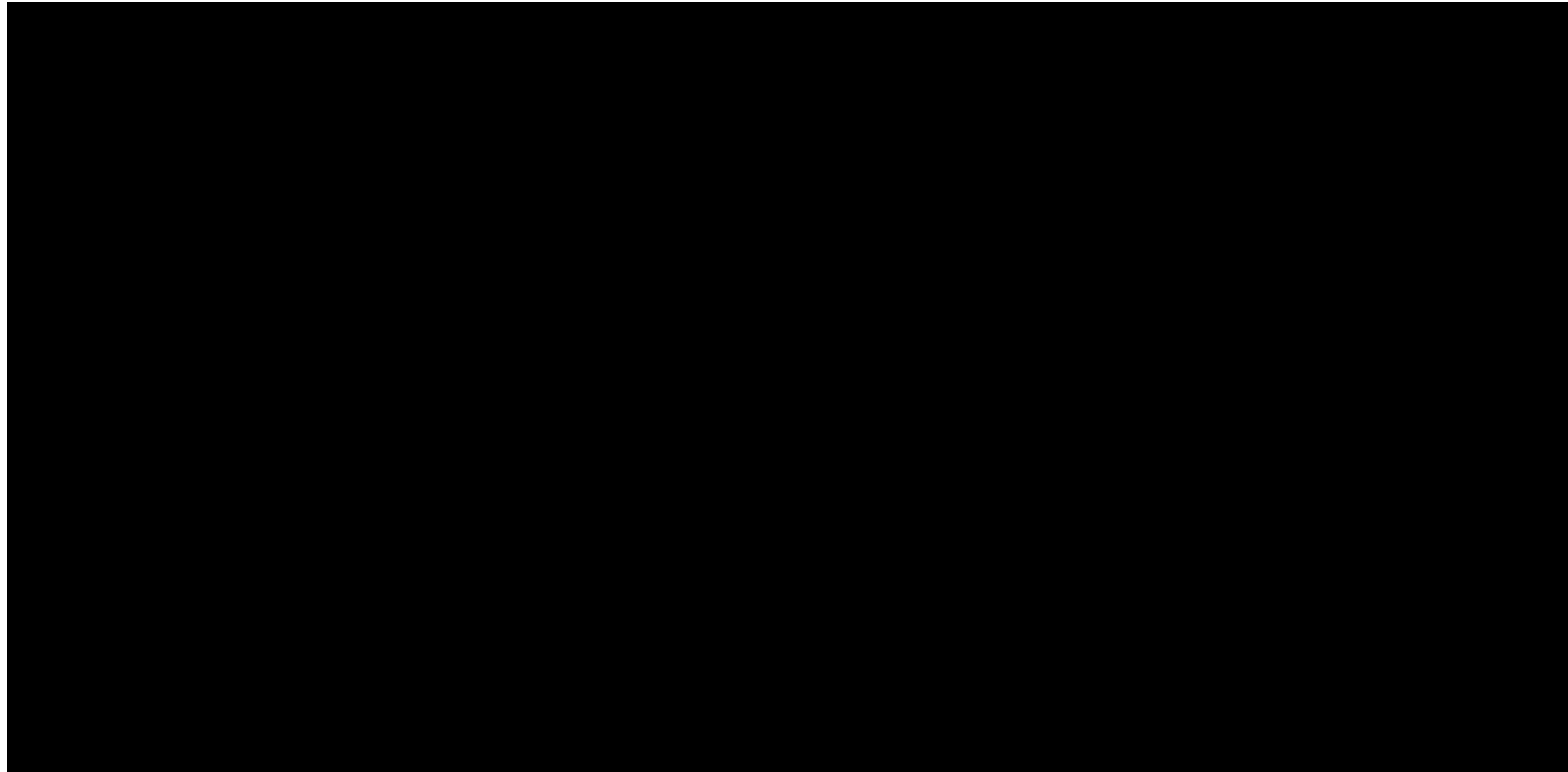
Reduction to Practice

Sorrells' Testimony:

23. The test report that [REDACTED] provided to ParkerVision is dated April 1998 (Exhibit 2010). The report shows the testing that was performed. This date is consistent with the time that I had the Eddie chip and circuit board sent to [REDACTED] for testing.

24. The test results confirmed the performance of the Eddie chip and circuit board. The [REDACTED] report confirmed ParkerVision's testing/evaluation and also showed that the combined Eddie chip and circuit board worked for its intended purpose of down-converting an RF signal.

Reduction to Practice



POR, 26-29; Sur-Reply, 19-20; Exs. 2010-2011. DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

28

Reduction to Practice

Sorrells' Testimony:

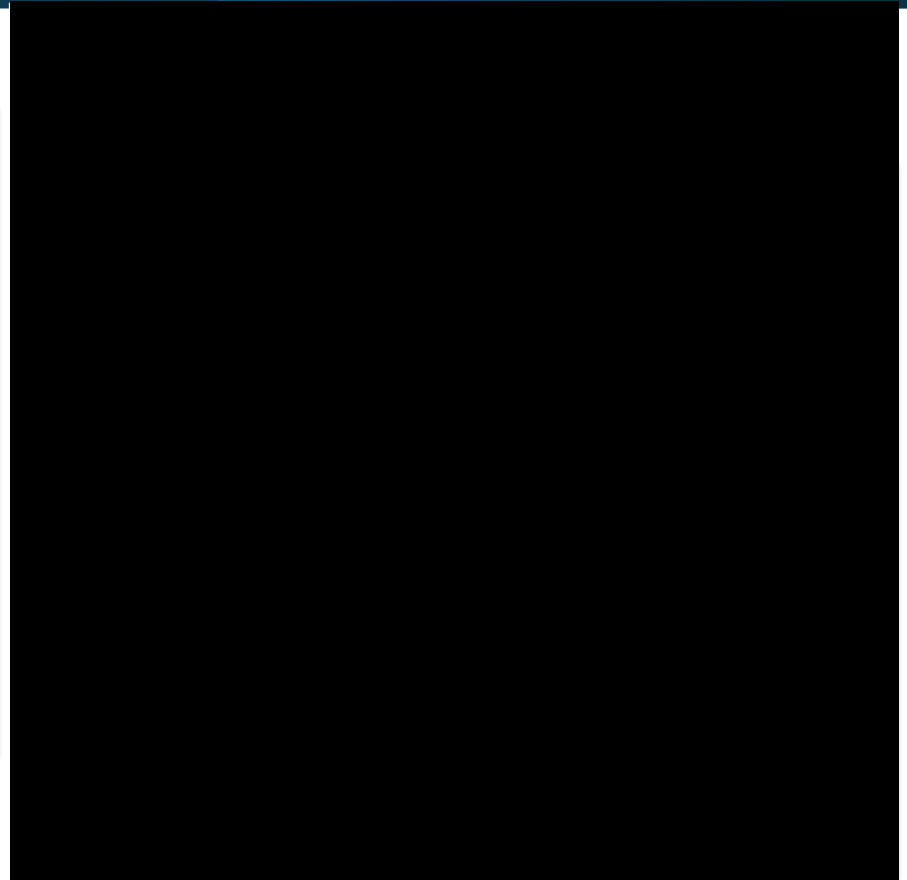
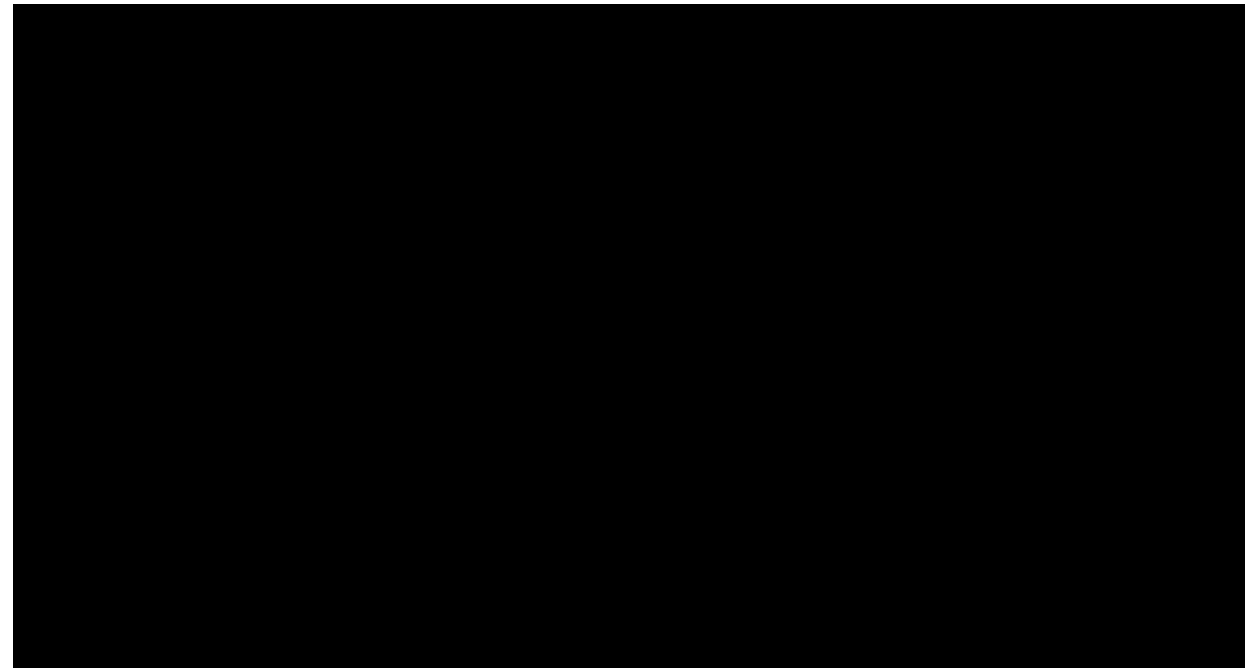
7. The layout of the first Eddie chip can be found in a file [REDACTED] (Exhibit 2012).

11. Below is a schematic of an early version of a circuit board (Exhibit 2014) that ParkerVision designed for mounting the Eddie chip.

13. As shown below, by January 20, 1998, ParkerVision designed the final schematic for a circuit board (Exhibit 2011) for mounting the Eddie chip. The schematic for the circuit board can be found in a file [REDACTED]

Reduction to Practice

Dickens' Admission:



POR,28; Reply, 7-8; Sur-Reply, 22; Ex.
2041, 54:2-8; Ex. 2010,7-8.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

30

Diligence

Sorrells' Testimony:

28. From at least March 6, 1997 through the filing of U.S Patent No. 6,061,551 (from which the '177 patent claims priority) on October 21, 1998, ParkerVision employees worked consistently on the design, development, testing, and/or evaluation of the Eddie Chip. From at least January 20, 1998 through October 21, 1998, ParkerVision employees worked consistently on the design, development, testing, and/or evaluation of the Eddie Chip and the circuit board into which the Eddie chip was incorporated.

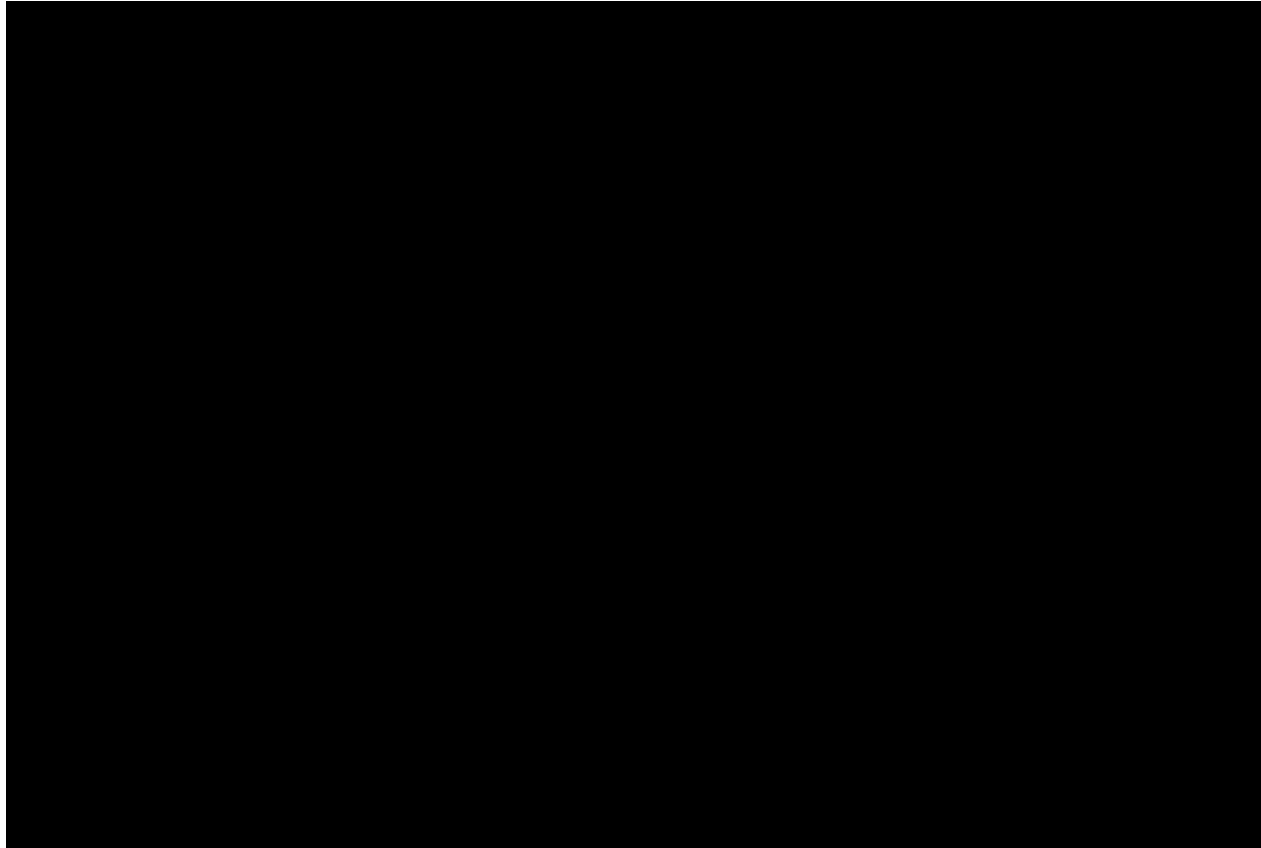
Diligence

Sorrells' Testimony:

29. ParkerVision files related to the design, development, testing, and/or evaluation of the Eddie chip and circuit board discussed above are maintained in a Relativity database. The Relativity database shows the metadata including file extension, file name, and last modified date of these files. A search of the database was run. Below is an excerpt from the search.

30. The results of the search were exported to a excel spreadsheet which is shown in Figure 2029. The files in the spreadsheet reflects ParkerVision's continuous work from at least January 1997 through October 1998 related to designing and developing the Eddie chip and circuit board.

Diligence



POR, 26-29; Ex. 2016, ¶¶29-30; Ex. 2029.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

33

Sorrells' Deposition

REMOTE ORAL DEPOSITION OF

DAVID SORRELLS

Middleburg, Florida

May 23, 2025 - 9:02 a.m.

I know we haven't been going for very long, but can you give me ten minutes for a break, please.

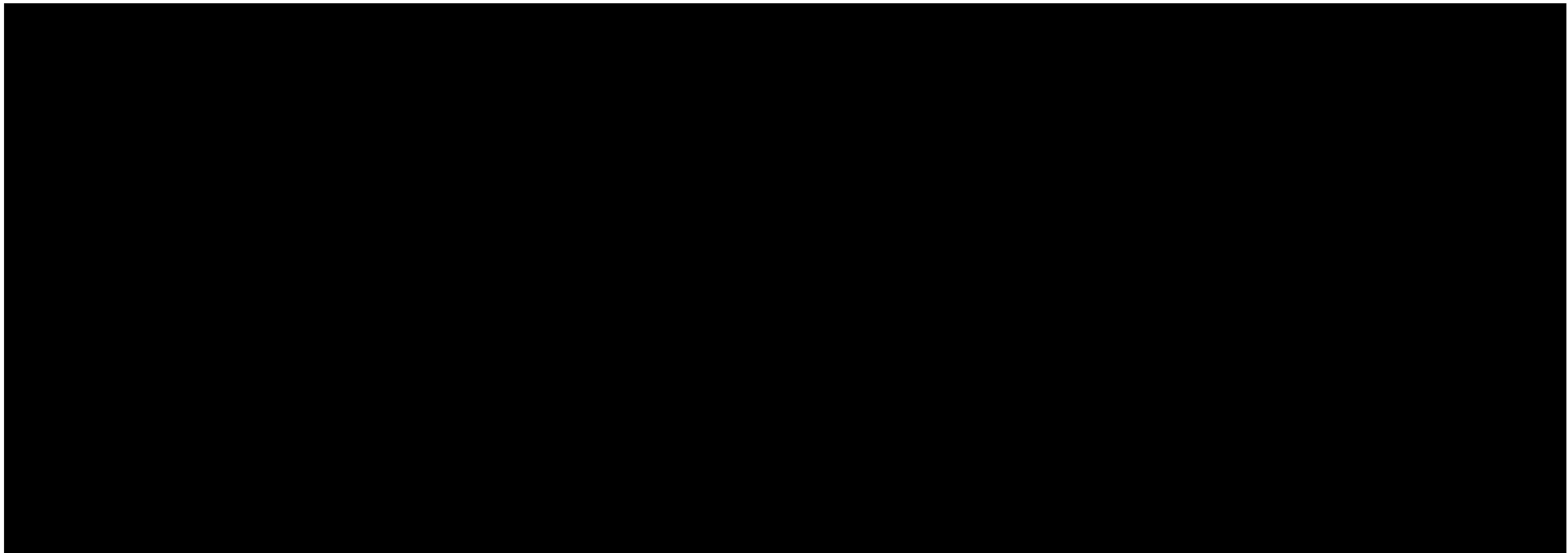
A. Sir, this is your deposition. And I'm, by the way, incredibly happy to be doing it remotely, so I'm on your schedule. record.

MS. LEPORE: That's fine with me as well.

(Recess taken from 9:34 a.m. to 9:47 a.m.)

MR. GRISWOLD: We have no further questions. We surrender the witness.

Different Versions of Files Have Different Names/Timestamps



Reply, 2-4; Sur-Reply, 21; Ex. 2016,
¶¶5-10; Ex. 2012.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

35

Claim 14 is Entitled to the Priority Date of the '551 Patent

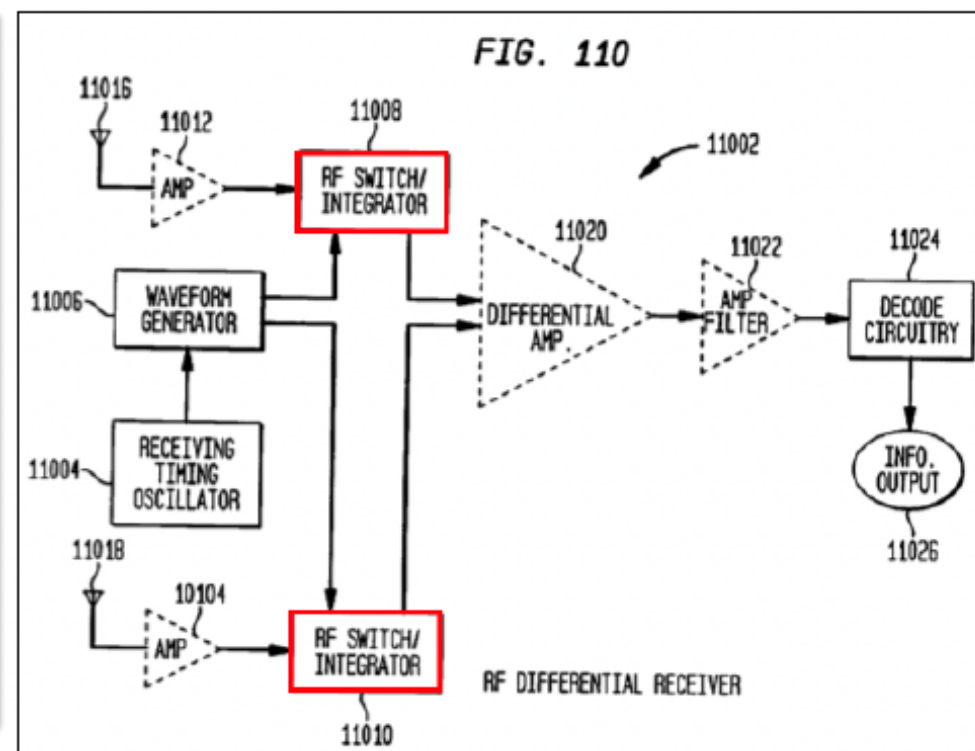
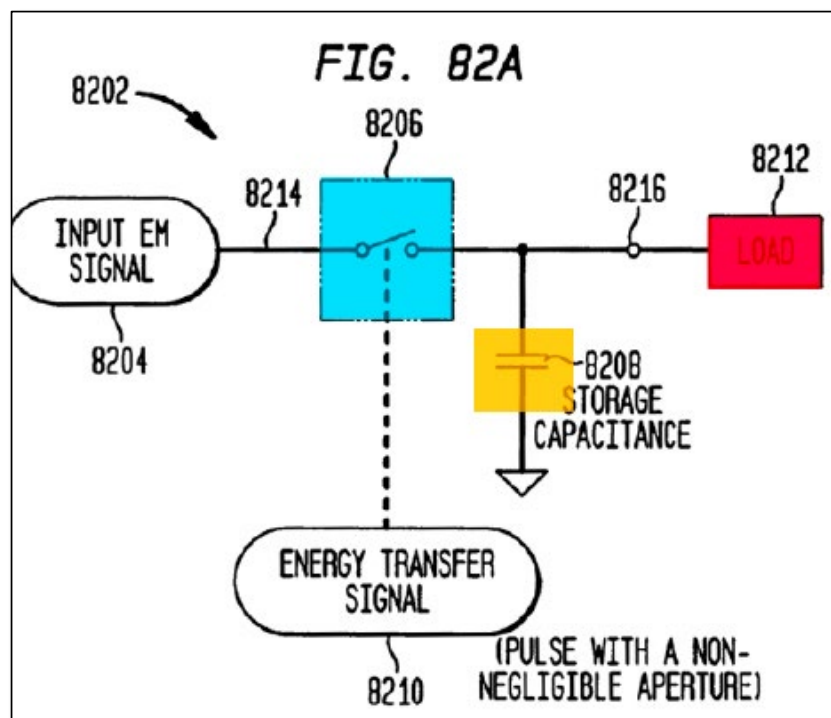
'551 Patent:

123. The method according to claim 33, wherein step (2) further comprises the step of gating the carrier signal according to a control signal comprising a stream of pulses, having non-negligible apertures that are substantially synchronized with the carrier signal.

In this example, where an FSK signal is being down-converted to a PSK signal, the aliasing rate is substantially equal to a harmonic or, more typically, a sub-harmonic, of the mid-point between the frequencies 6106 and 6108. In this example, where the first frequency 6106 is 899 MHZ and second frequency 6108 is 901 MHZ, the mid-point is approximately 900 MHZ. Suitable aliasing rates thus include 1.8 GHZ, 900 MHZ, 450 MHZ, etc.

Claim 14 is Entitled to the Priority Date of the '551 Patent

'551 Patent:



Reply, 21-22; Sur-Reply, 23-25; Ex. 2033,
Figs. 82A/82B, 110; Ex.-2024, ¶¶148-49

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

37

Petitioner Misrepresents PO's Position on Priority

as discovery progresses, ParkerVision contends that the claims identified below are entitled to a priority date of **no later than** the dates specified below:

Patent	Claim(s)	Priority Date (at least as early as)	Basis and Support
7,865,177	1, 2, 3, 5, 7, 8, 9, 10, 11, 12, 14	March 9, 2000	Filing date application No. 09/521,879 (now abandoned and file history produced at PV1100243263), of which the '177 Patent is a continuation-in-part.

Reply, 21; Sur-Reply, 25-26; Ex. 1044, 3.

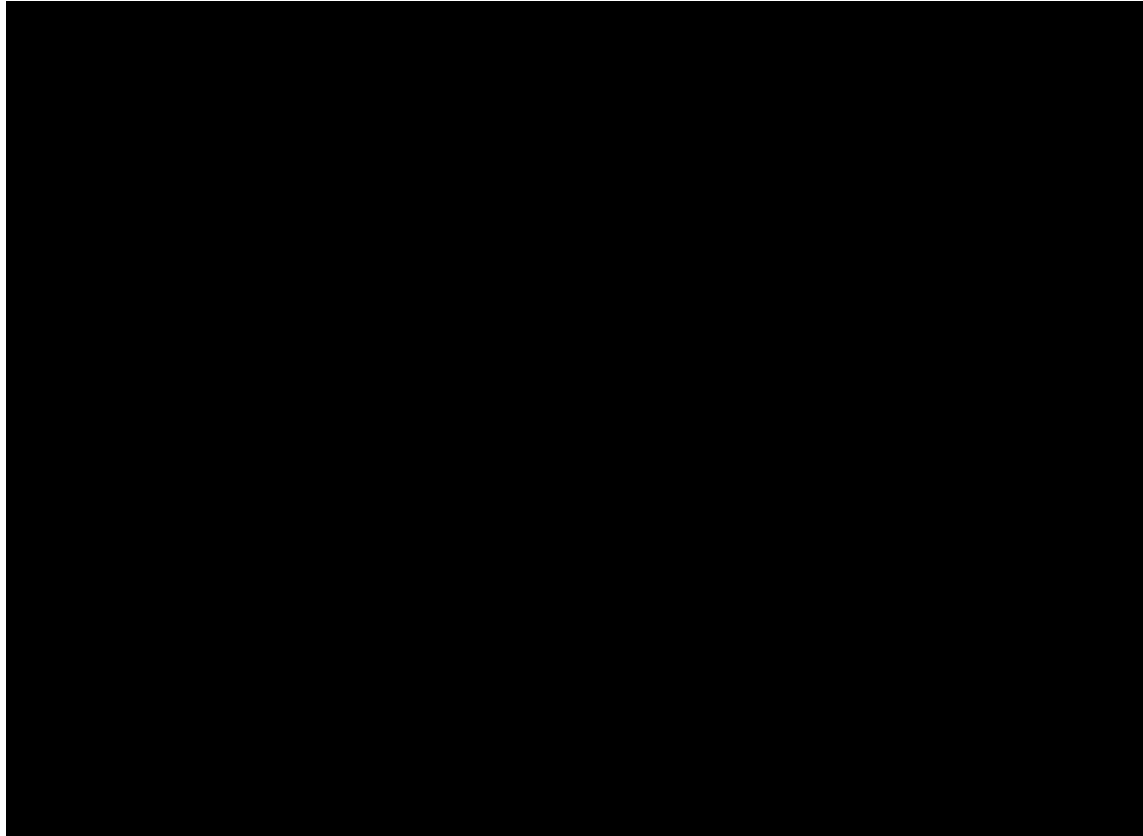
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

The Eddie Device Practices Claim 14

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

39

Eddie Device Practices Claim 14

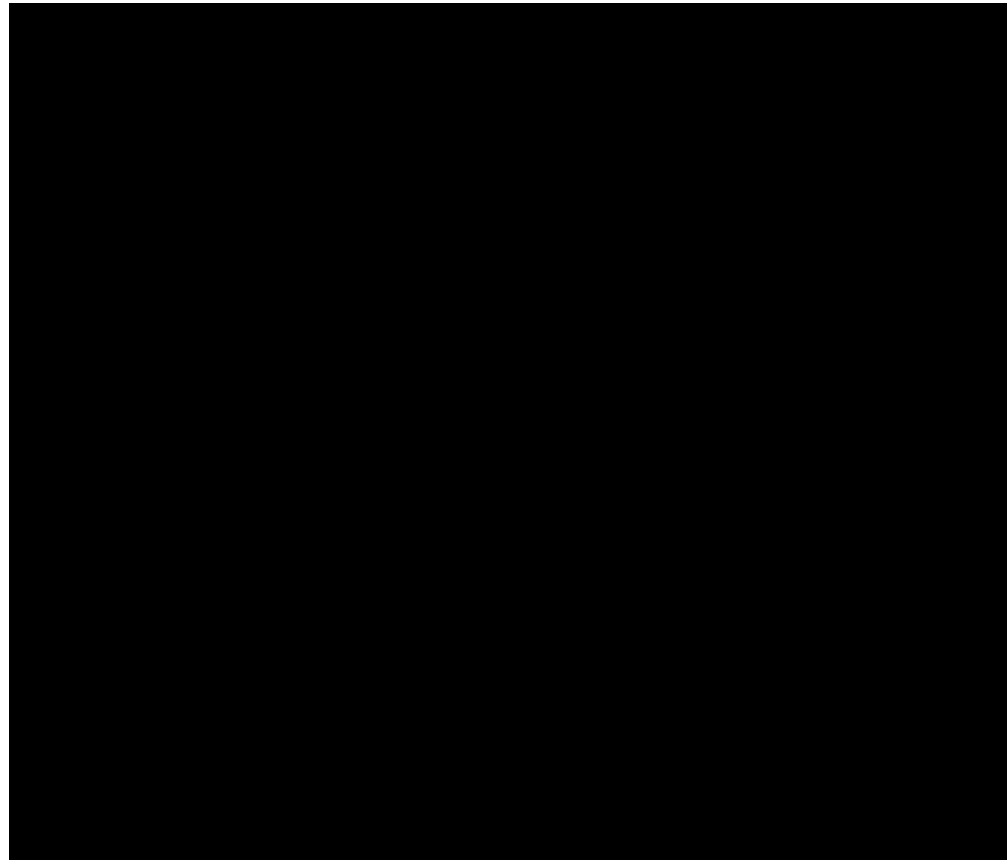


Sur-Reply, 2-6; Ex. 2024, ¶165; Ex. 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

40

Eddie Device Practices Claim 14

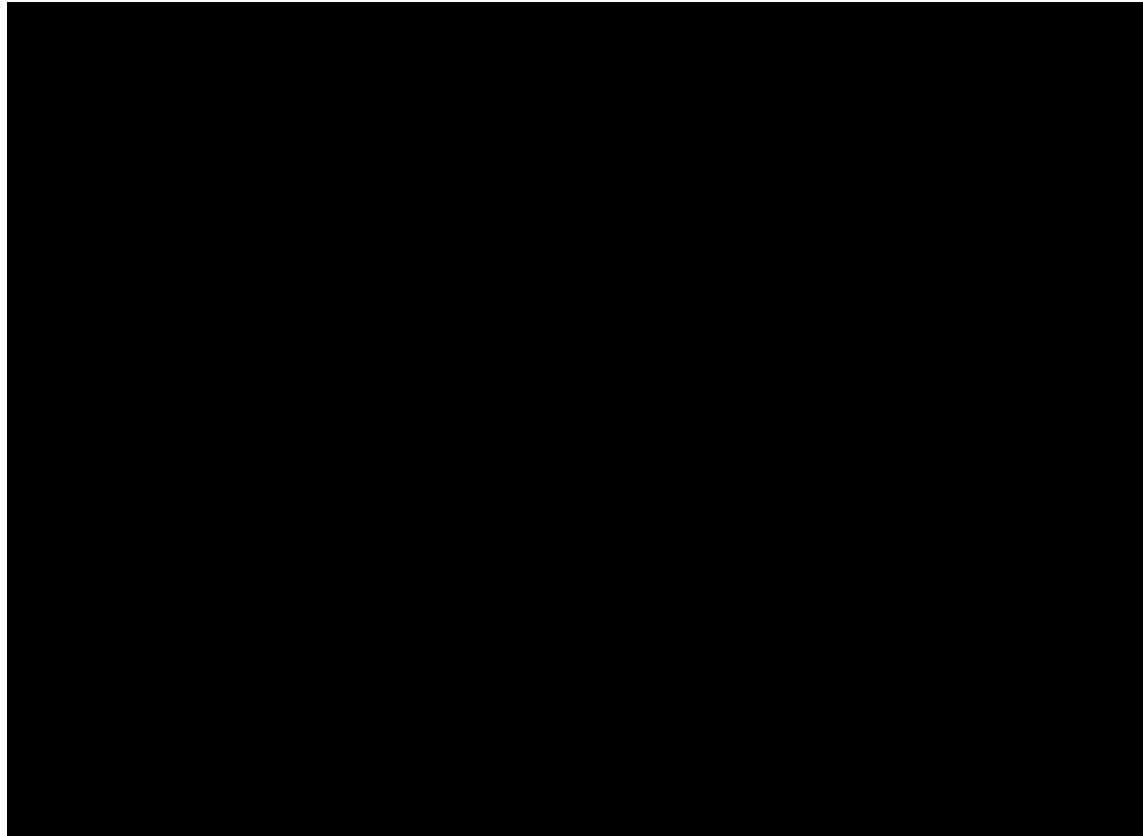


Sur-Reply, 2-6; Ex. 2024, ¶165; Ex. 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

41

Eddie Device Practices Claim 14

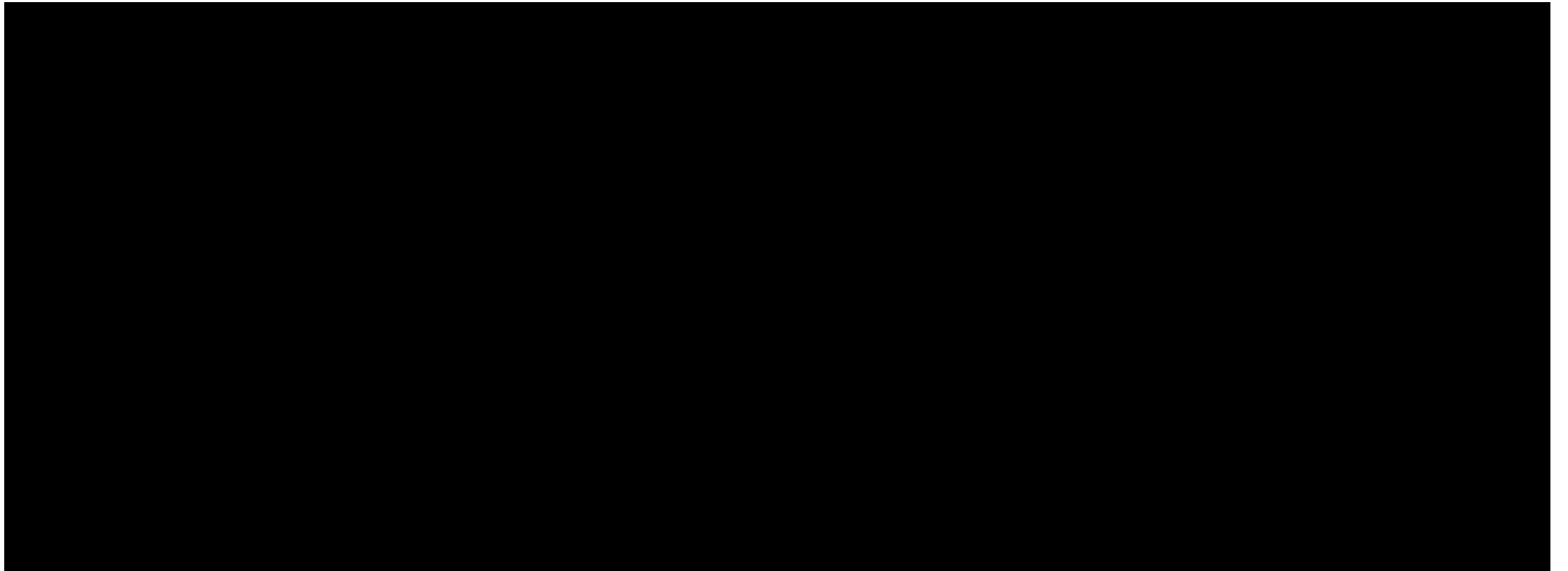


Sur-Reply, 2-6; Ex. 2024, ¶165; Ex. 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

42

Eddie Device Practices Claim 14

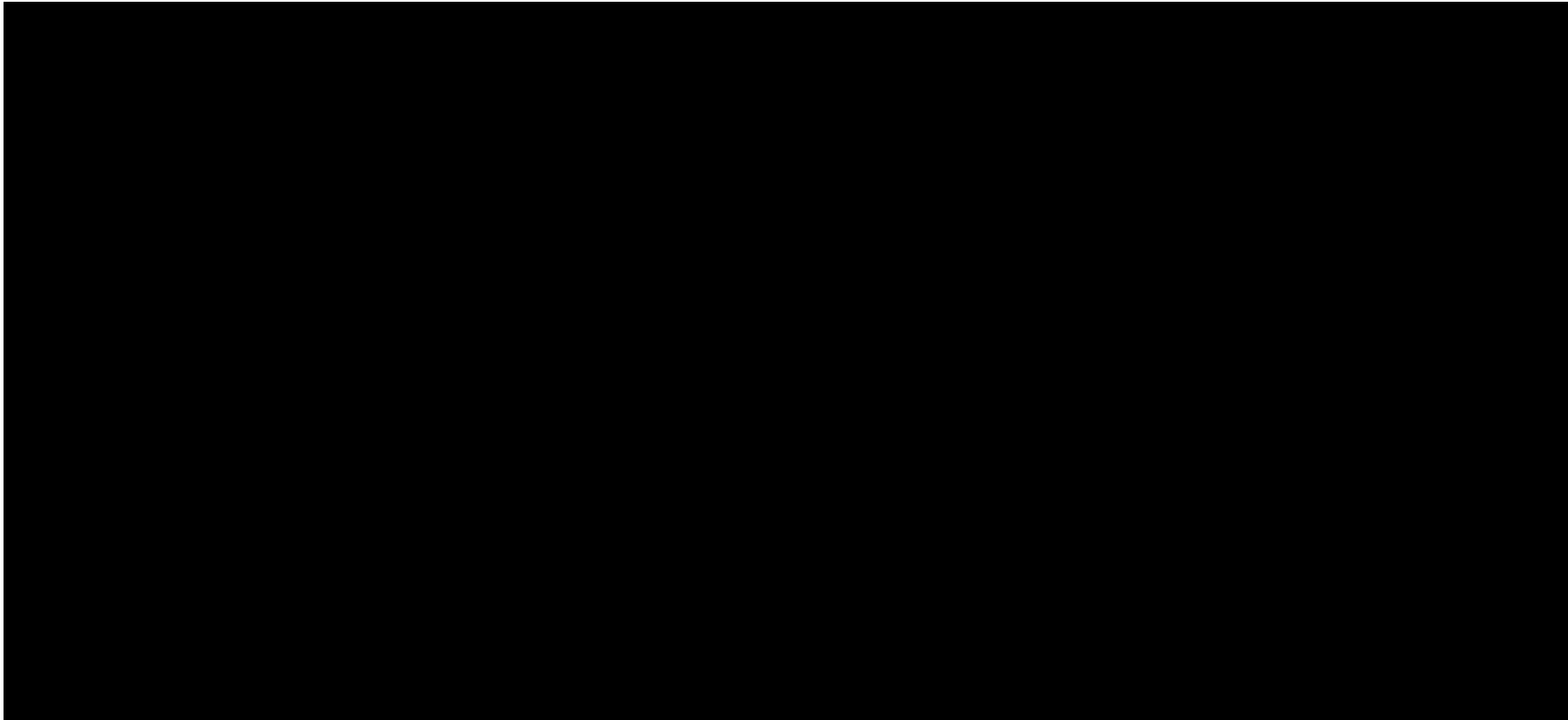


Sur-Reply, 2-6; Ex. 2024, ¶165; Ex. 2015.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

43

Eddie Device Practices Claim 14

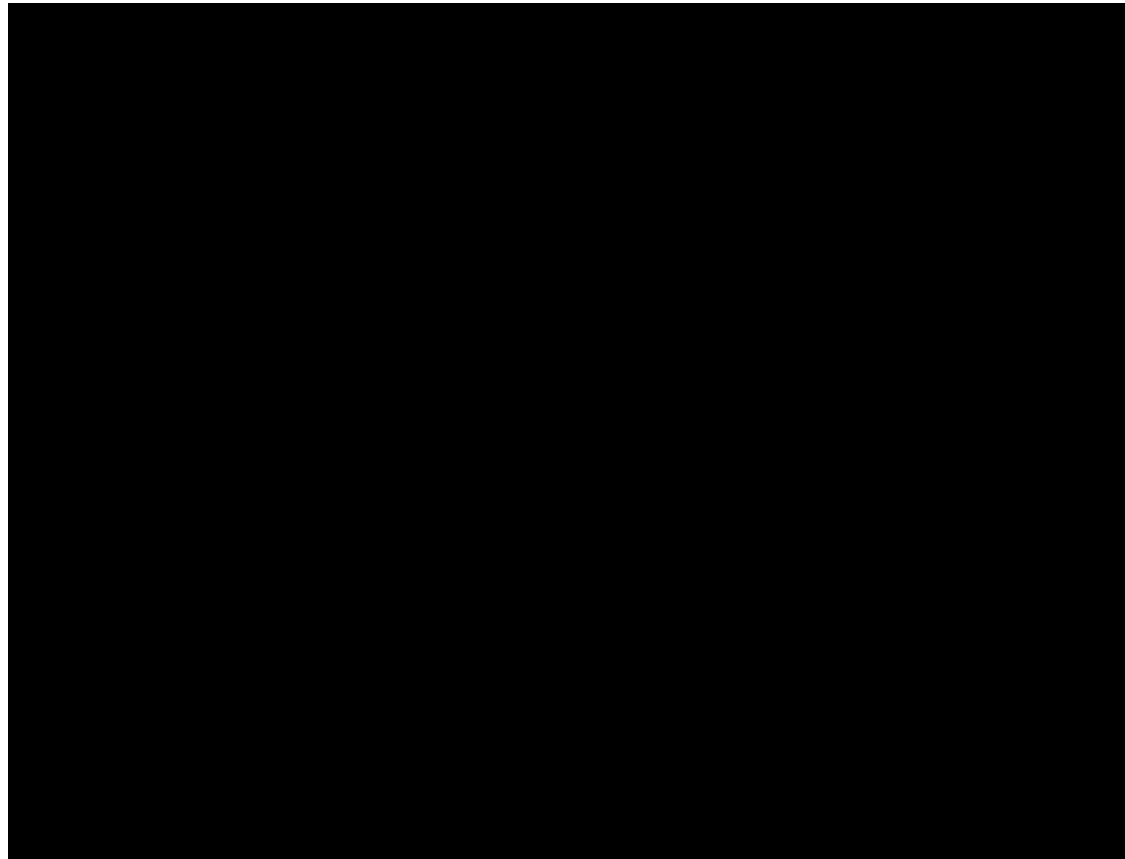


Sur-Reply, 6-10; Ex. 2015,14, 24.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

44

Eddie Device Practices Claim 14



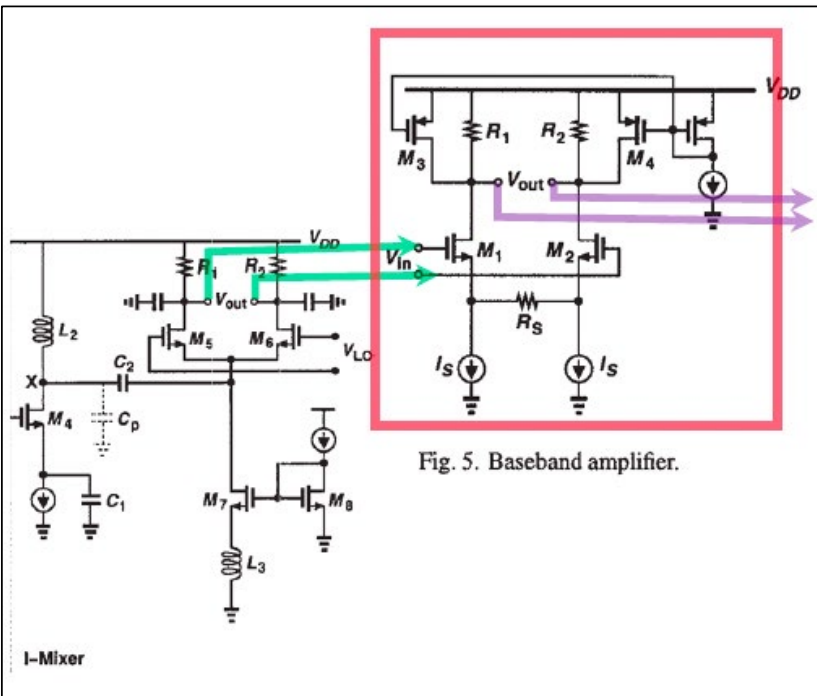
Petitioner's Experts Take Inconsistent Positions

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

46

Petitioner's Experts Take Inconsistent Positions

Galton:

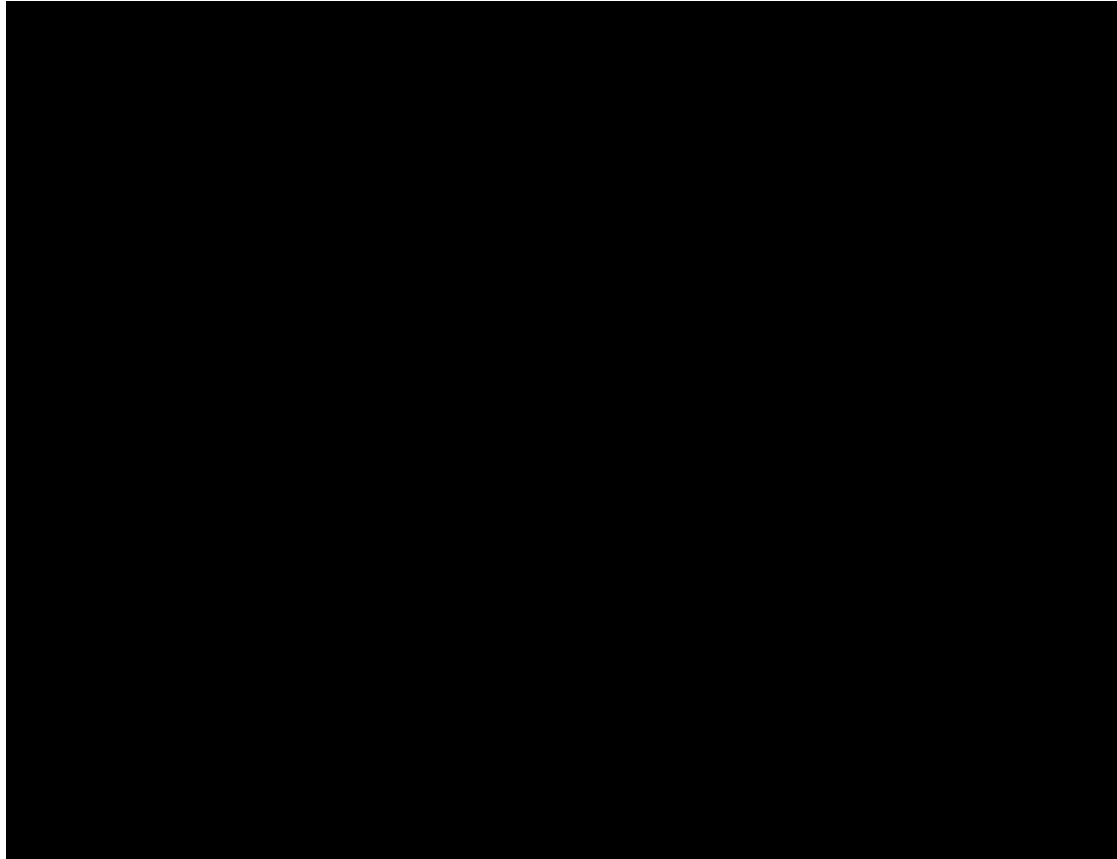


each of the baseband amplifier's V_{out} output signals contains an amplified version of the difference between the baseband amplifier's two V_{in} inputs, i.e., the difference between said down-converted signal and said inverted down-converted signal. *See, e.g.,* Razavi, 2:35-48, FIGS. 2, 5.

187. A POSITA would have recognized that each of the two V_{out} signals is a combined version of said first and second down-converted signals, and, furthermore, the two V_{out} signals taken together represent a differential version of the combination of said first and second down-converted signals.

Eddie Device Practices Claim 14

Ricketts:



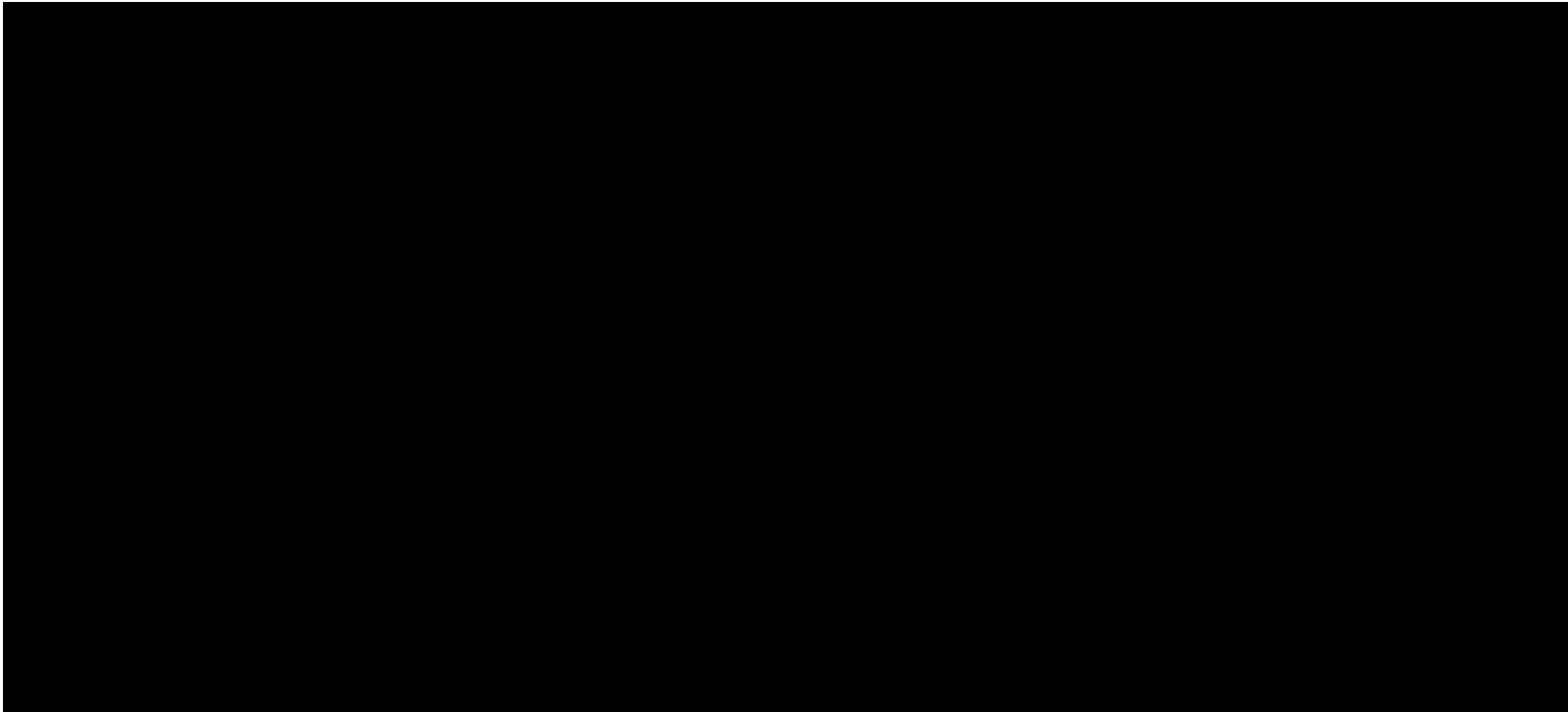
Eddie Device Practices Claim 14

Ricketts:



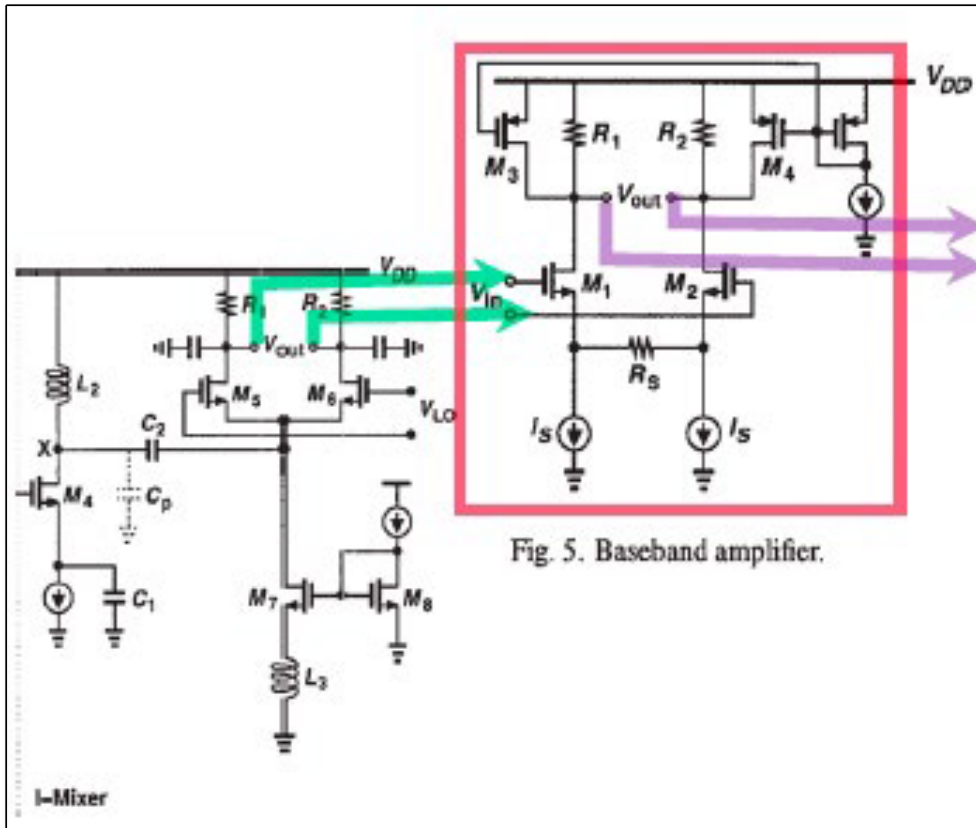
Petitioner's Experts Take Inconsistent Positions

Dickens:



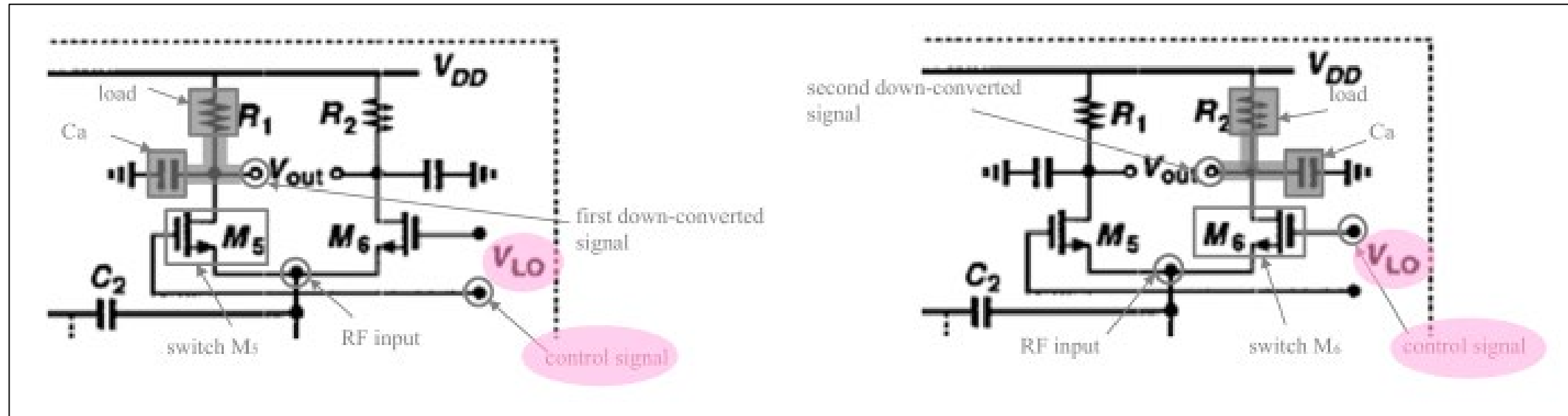
Petitioner's Experts Take Inconsistent Positions





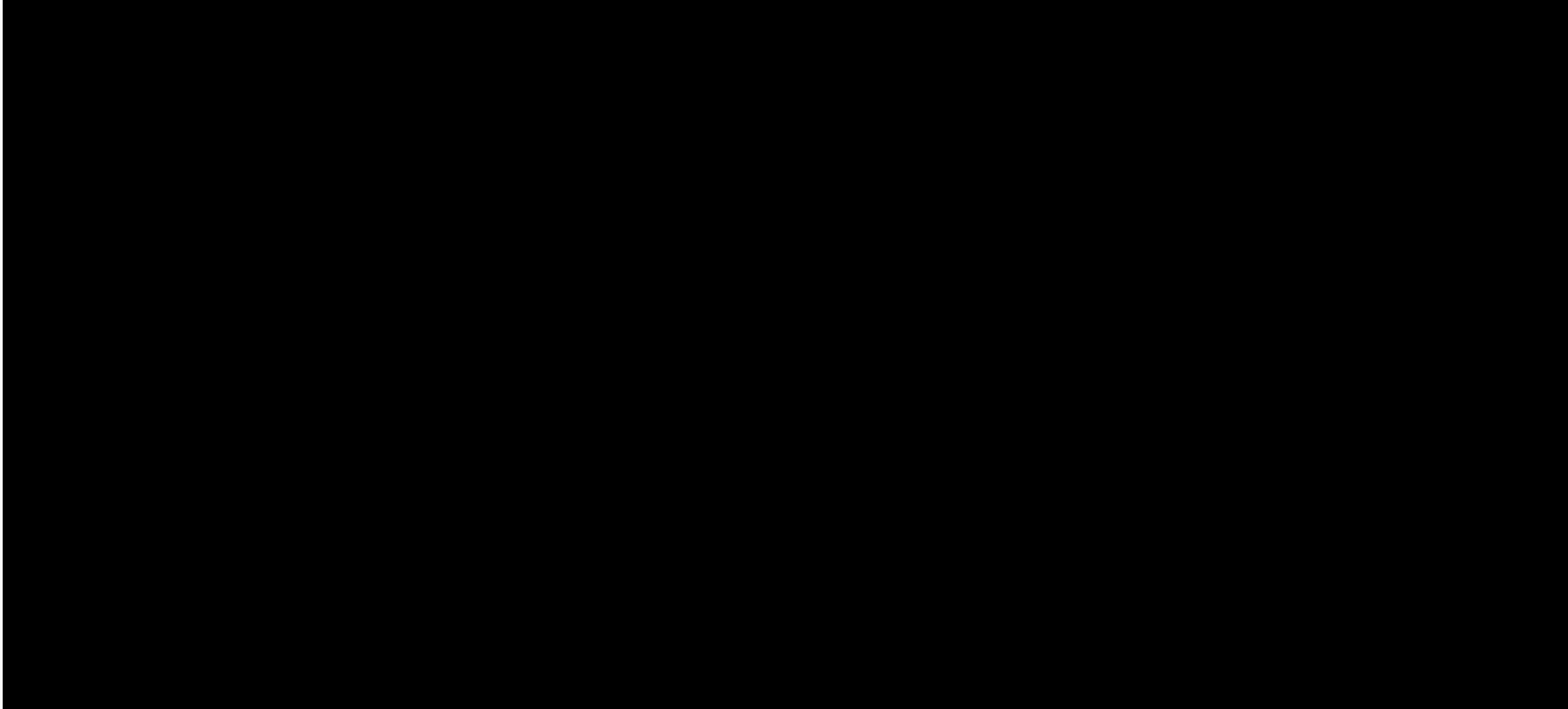
Petitioner's Experts Take Inconsistent Positions

Galton:

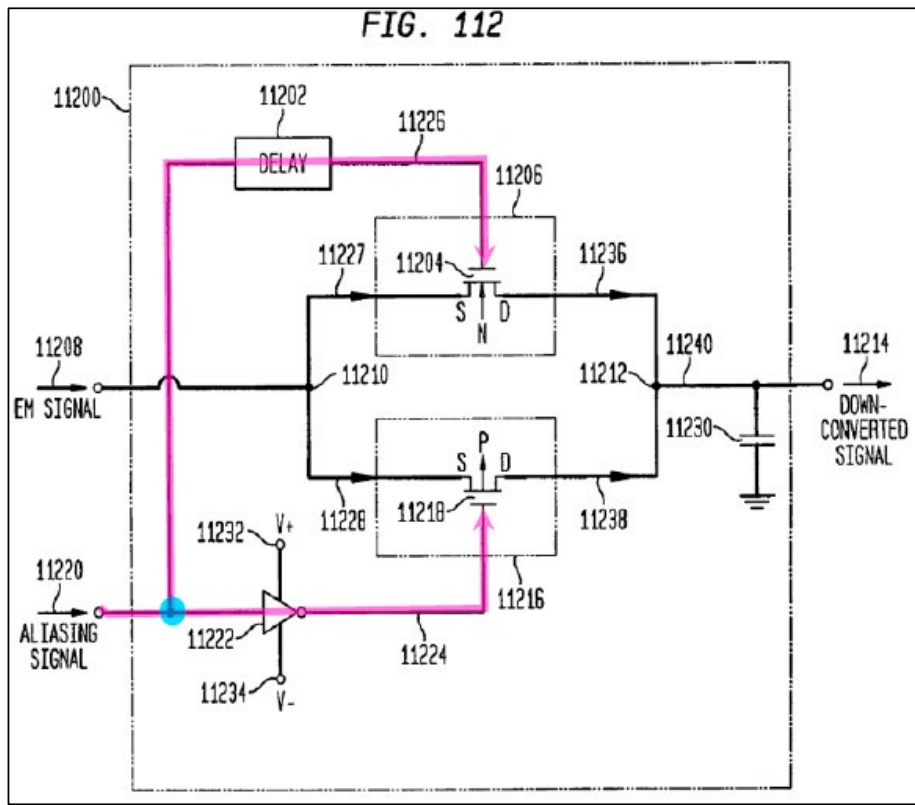


Eddie Device Practices Claim 14

Ricketts:



'177 Patent is Consistent with Ricketts' Position



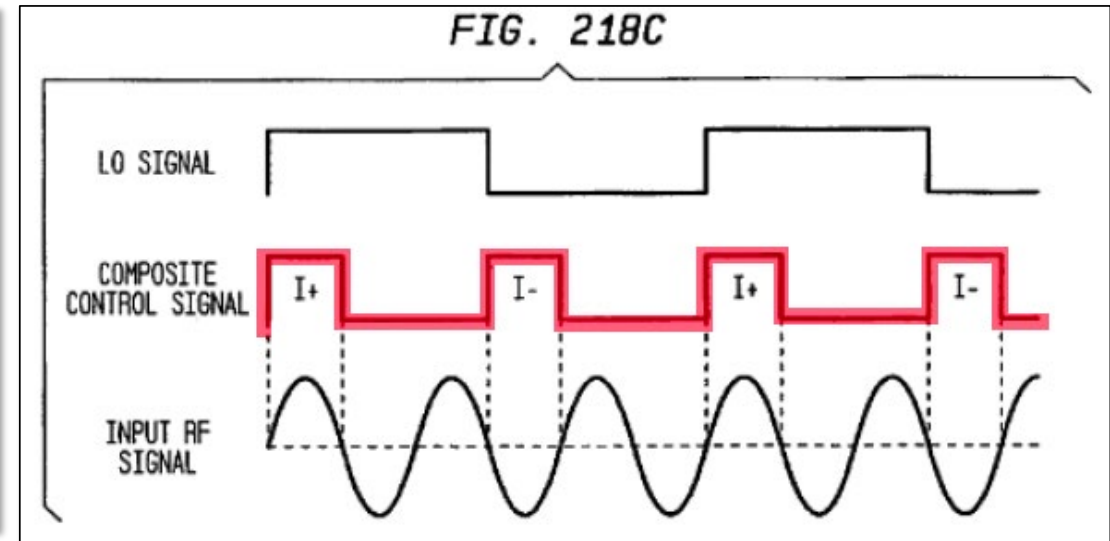
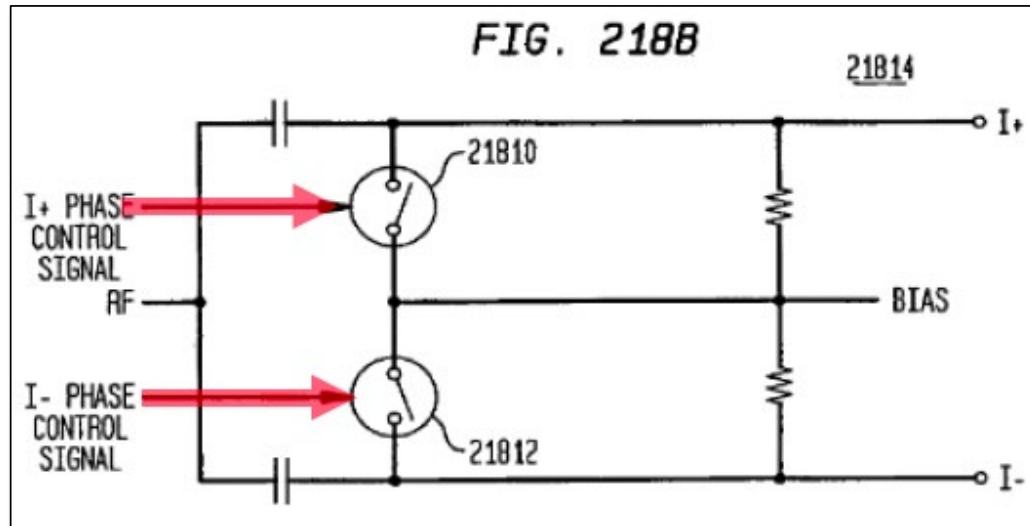
This requires that two complementary aliasing signals **11224**, **11226** be generated from aliasing signal **11220** to control the sampling by FETs **11218**, **11204**, respectively.

Sur-Reply, 6-10; Ex. 1001, 110:32-35; Figs. 112, 114-115.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

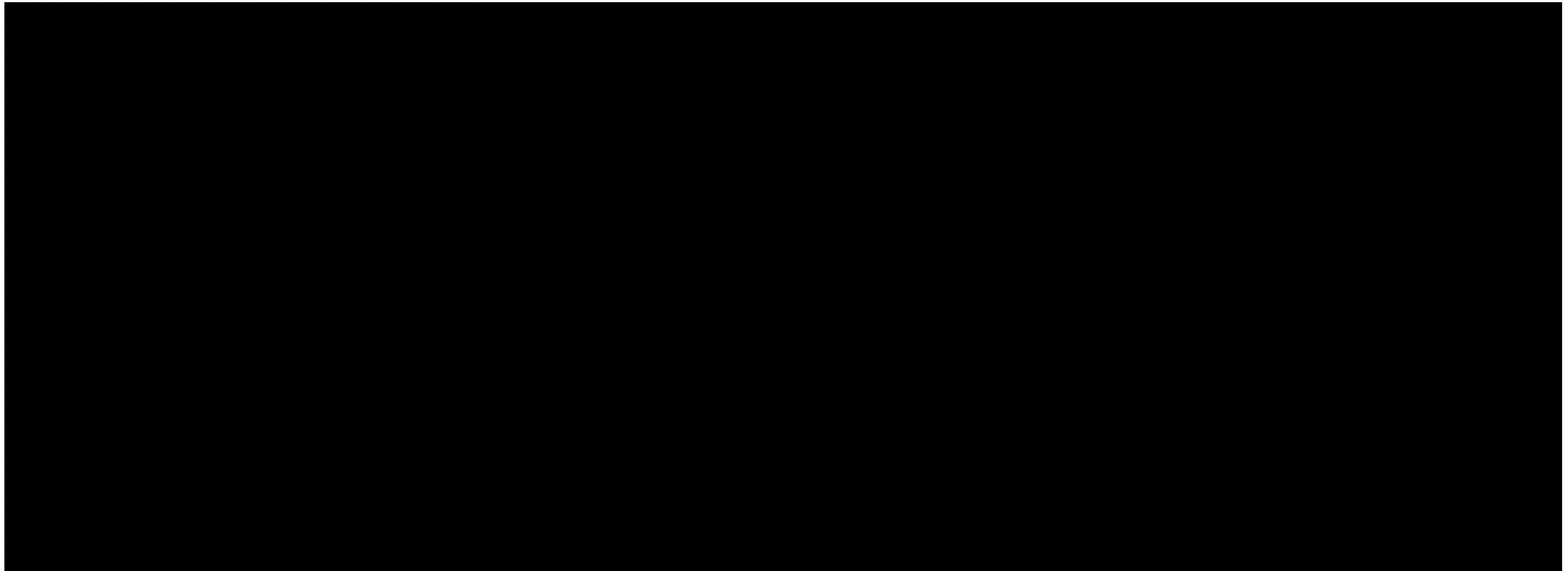
55

'177 Patent is Consistent with Ricketts' Position



Petitioner's Experts Take Inconsistent Positions

Dickens:



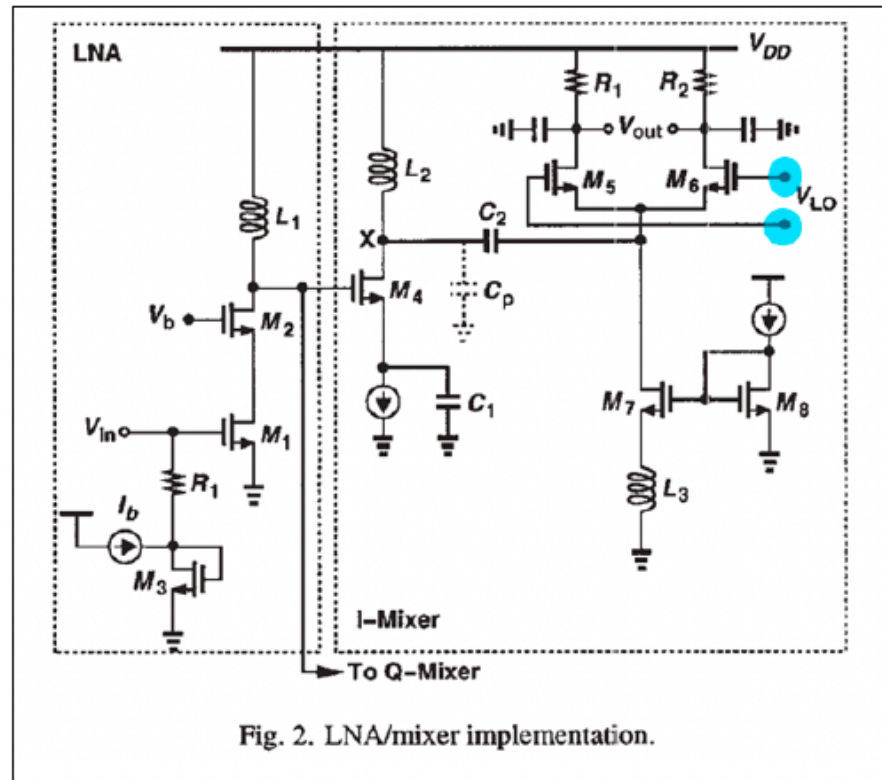
Sur-Reply, 6-10; Ex. 1067, ¶¶13-15.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

57

Petitioner's Experts Take Inconsistent Positions

Galton:



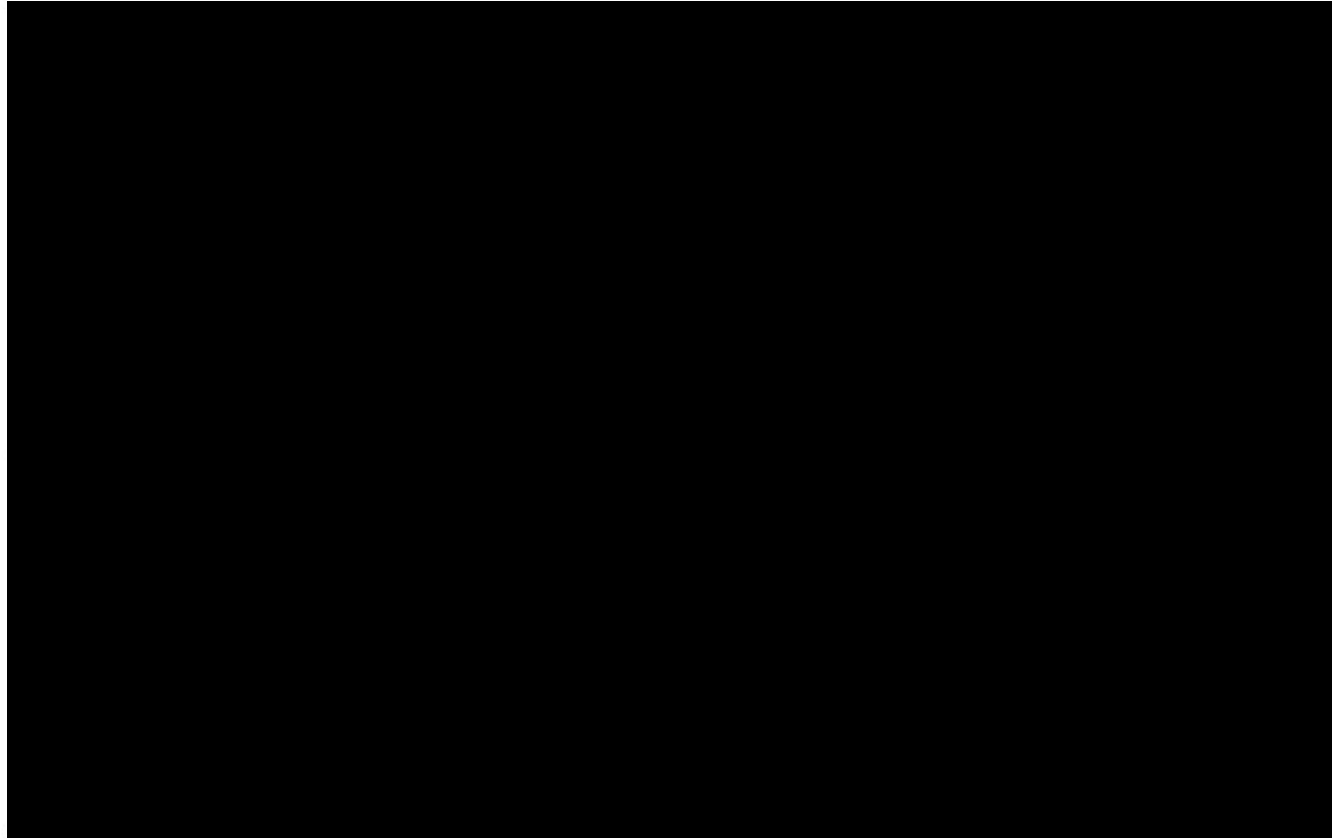
Sur-Reply, 10-14; Ex. 1003, ¶1176;
Ex. 1017, Fig. 2.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

58

Eddie Device Practices Claim 14

Ricketts:



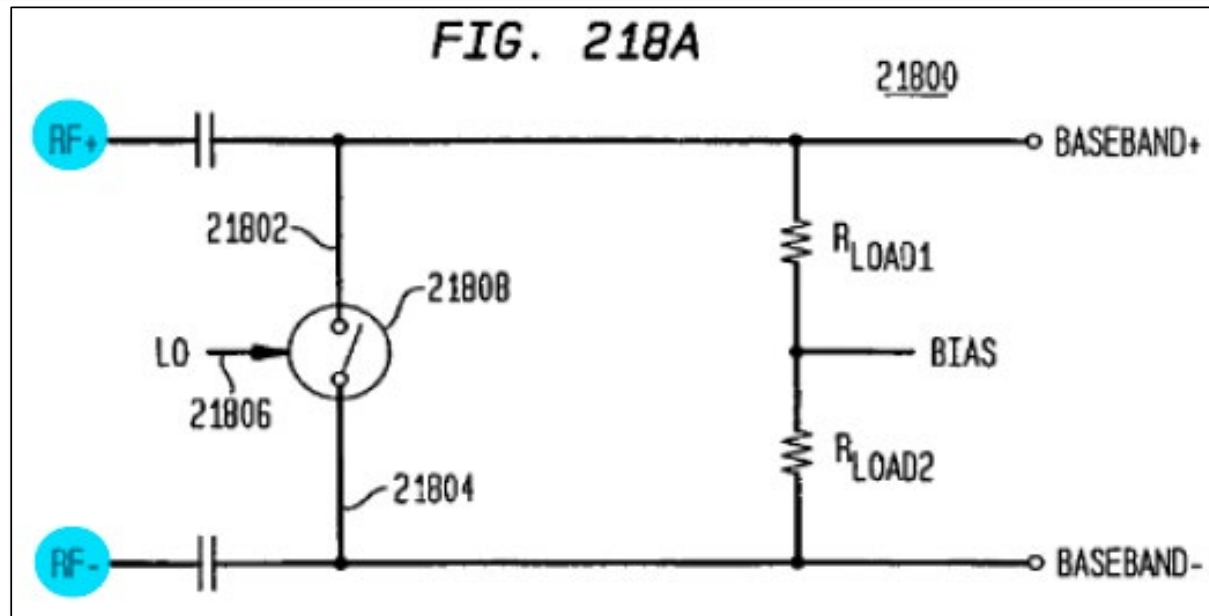
Sur-Reply, 10-14; Ex. 2015,10,12,21;
Ex. 1003,¶46.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

59

'177 Patent is Consistent with Ricketts' Position

FIG. 218A illustrates an example differential input, differential output receiver configuration, according to an embodiment of the present invention;



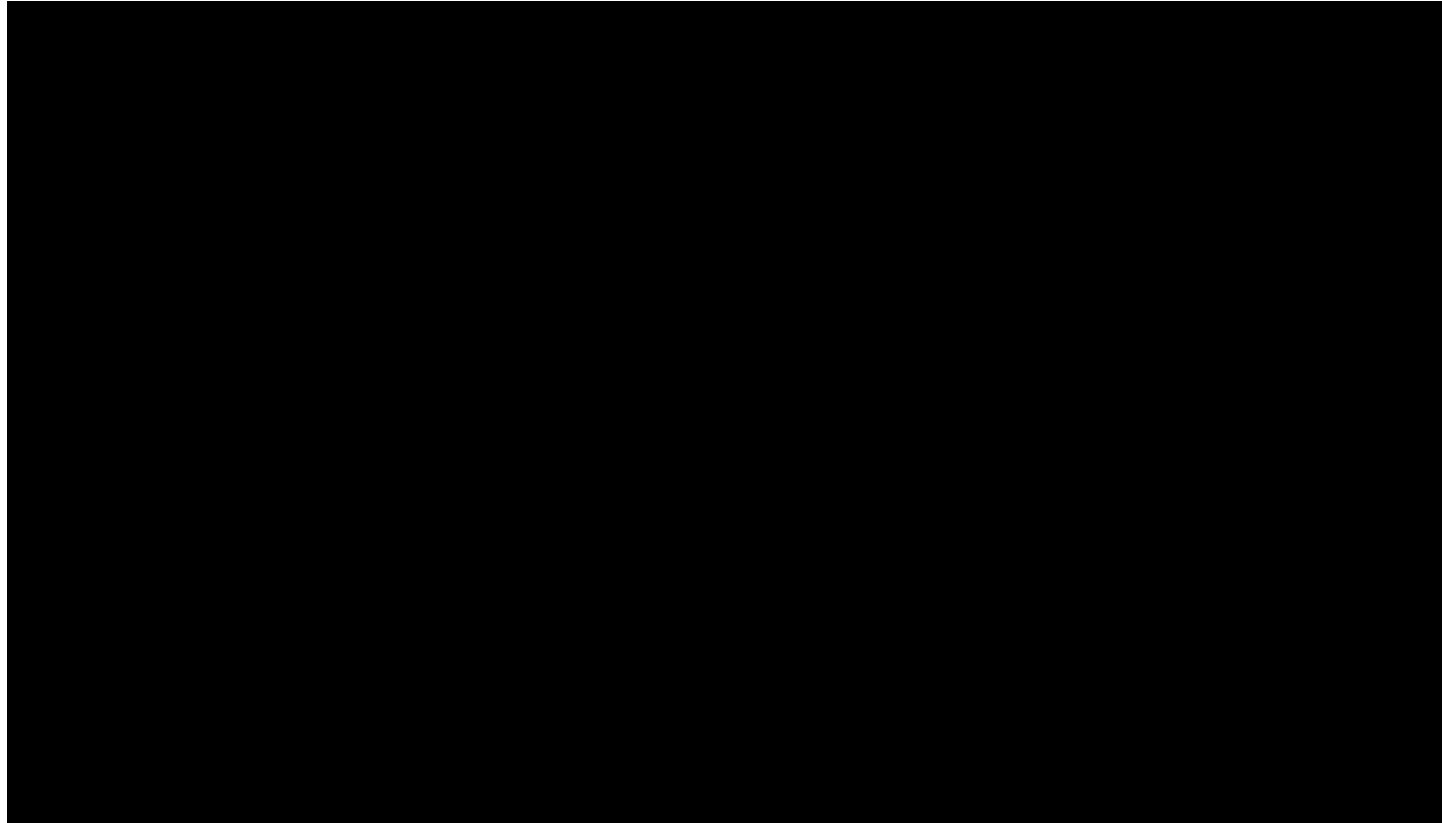
Sur-Reply, 10-14; Ex. 1001, 12:43-44,
6:5-6, Fig. 218A.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

60

Petitioner's Experts Take Inconsistent Positions

Dickens:

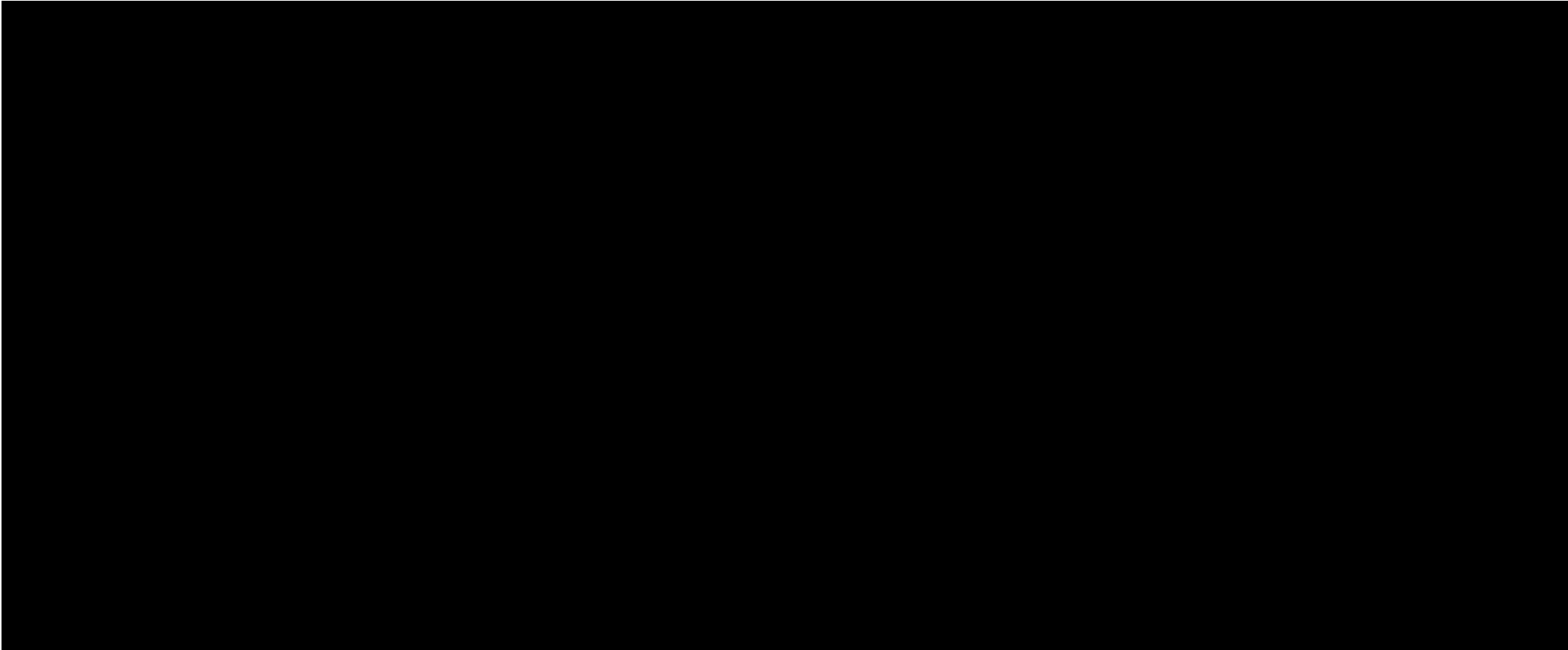


Sur-Reply, 10-14; Ex. 1067, ¶¶ 25-27.

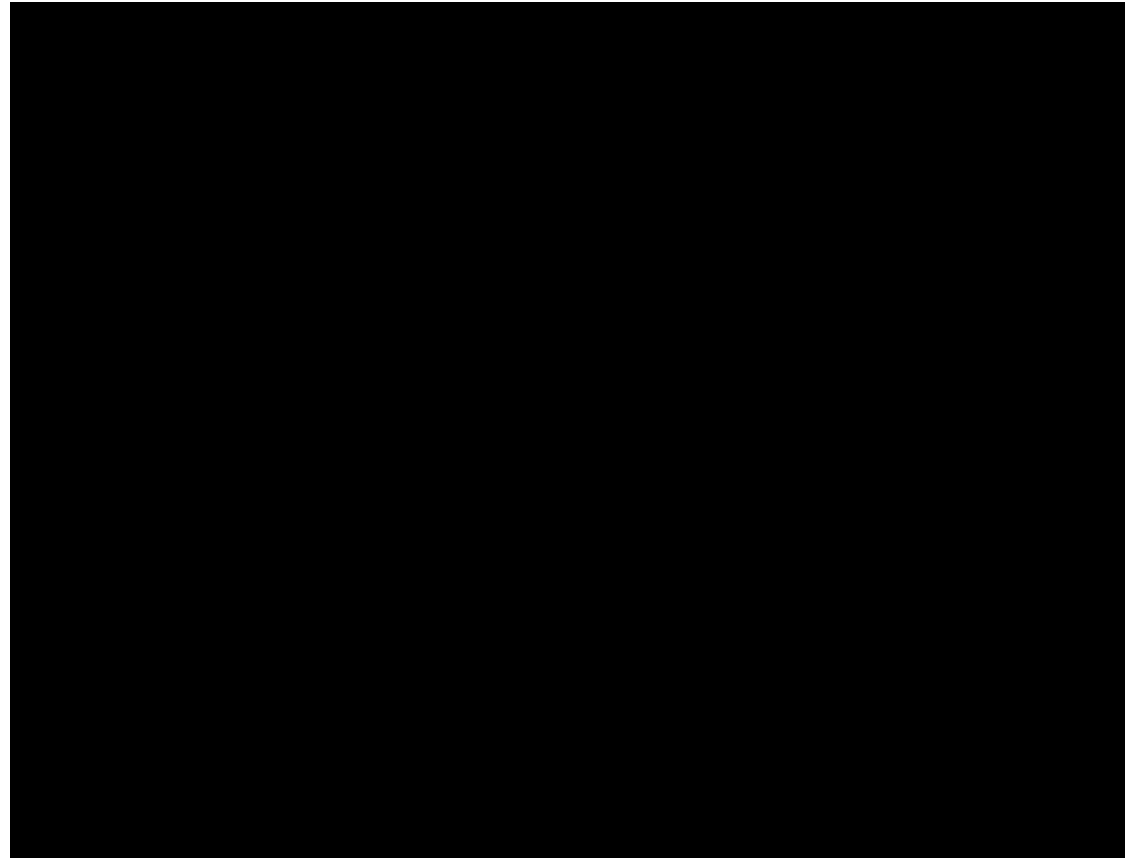
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

61

 Refers to Eddie's 



Dickens Fails to Address the Relevant Capacitors

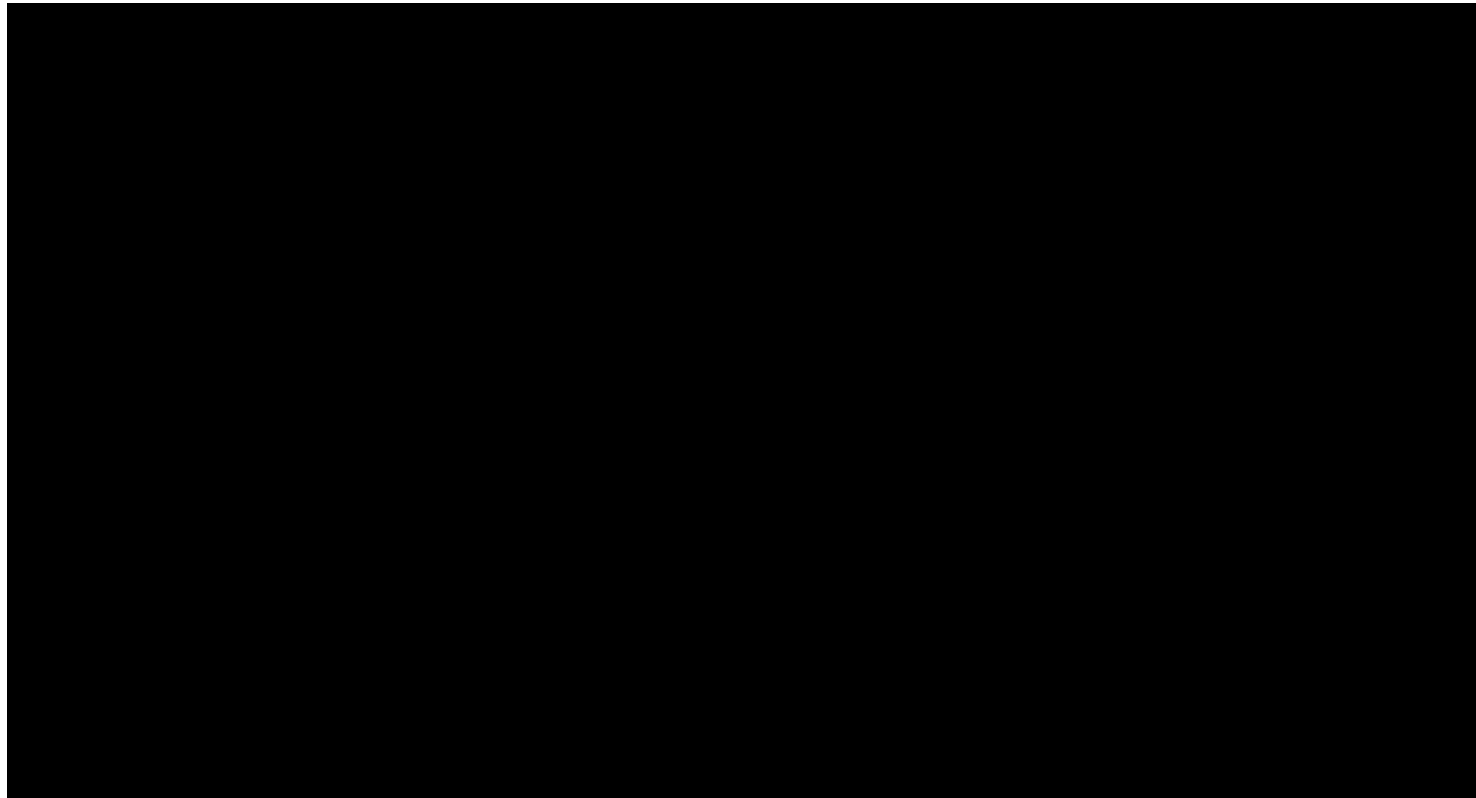


Reply,14-17; Sur-Reply, 17; Ex. 2015, 20.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

63

Dickens Admits That Eddie Performs Down-Conversion

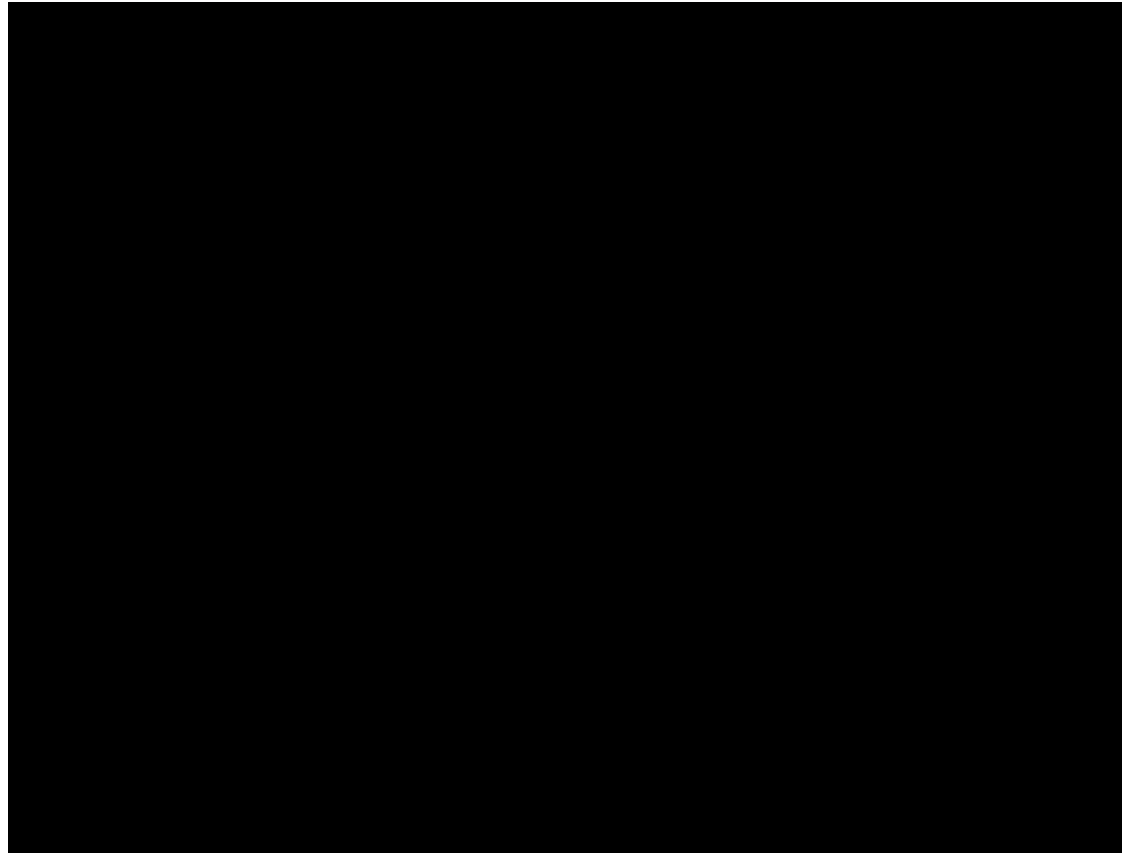


Sur-Reply, 14-15; Ex.2041,54:2-8,70:7-16, 55:1-59:18, 63:8-65:2.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

64

Dickens Ignores Eddie's Actual Testing Configuration



Sur-Reply, 15-16; Ex. 1067, ¶¶ 16-20.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

65

Dickens Ignores Eddie's Actual Testing Configuration

In preparing your opinions in this case, or in the IPRs, did you do anything to confirm that the Eddie device that [REDACTED] tested used any of the [REDACTED] shown in Exhibit 2011, which is the schematic.

ATTORNEY MAGEE: Objection to form.

A No. I didn't do any of that. I mean, I was told that that was the schematic, so I was asked to analyze that. I didn't -- I didn't try to analyze -- I didn't hypothesize what -- what circuit they might have been using.
No. I didn't do that.

And in fact, [REDACTED] If you go back to the -- to the schematic, they show that the -- [REDACTED]
[REDACTED]

Dickens Ignores Eddie's Actual Testing Configuration

Exhibit 3 shows that for a [REDACTED]
megahertz signal, the device under test would have
a [REDACTED] ohm input impedance real part, correct?
ATTORNEY MAGEE: Objection. Form.
A Yes. That's correct. The real part would
be -- is [REDACTED] That's correct. And the
imaginary is the [REDACTED]

Sur-Reply, 15-16; Ex. 1067, ¶¶16-20;
Ex. 2041, 30:16-22.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

67

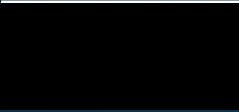
Dickens Has No Basis for the Impedance of [REDACTED]

Sur-Reply, 15-16; Ex. 1067, ¶¶ 16-17.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

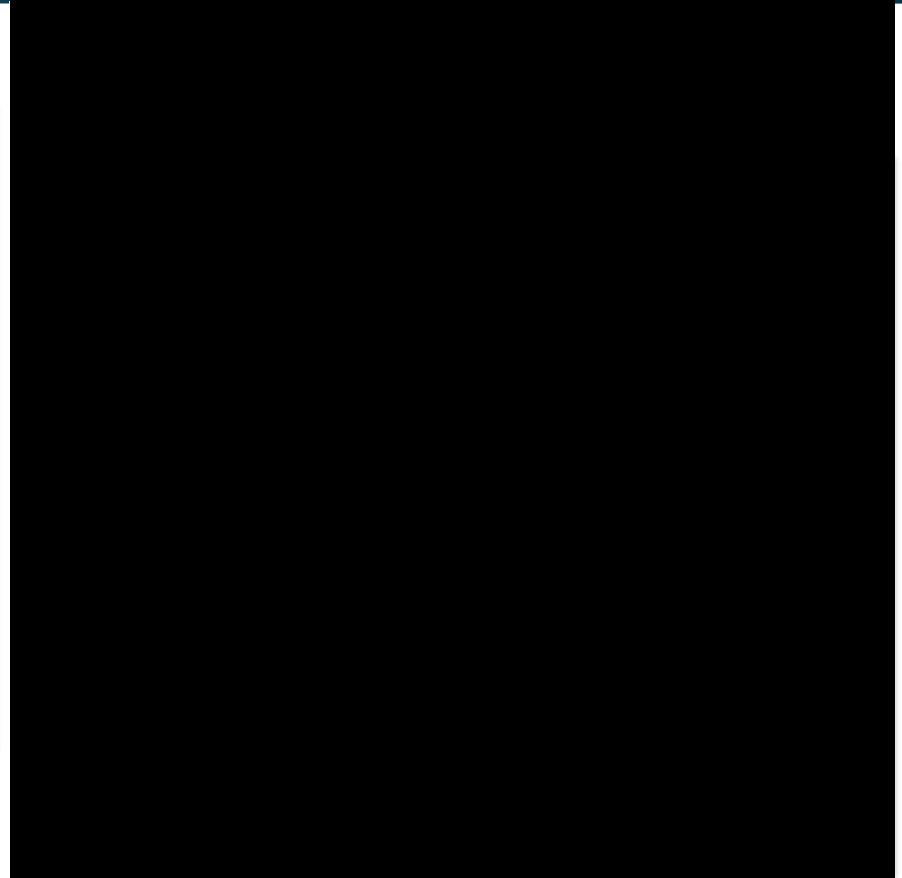
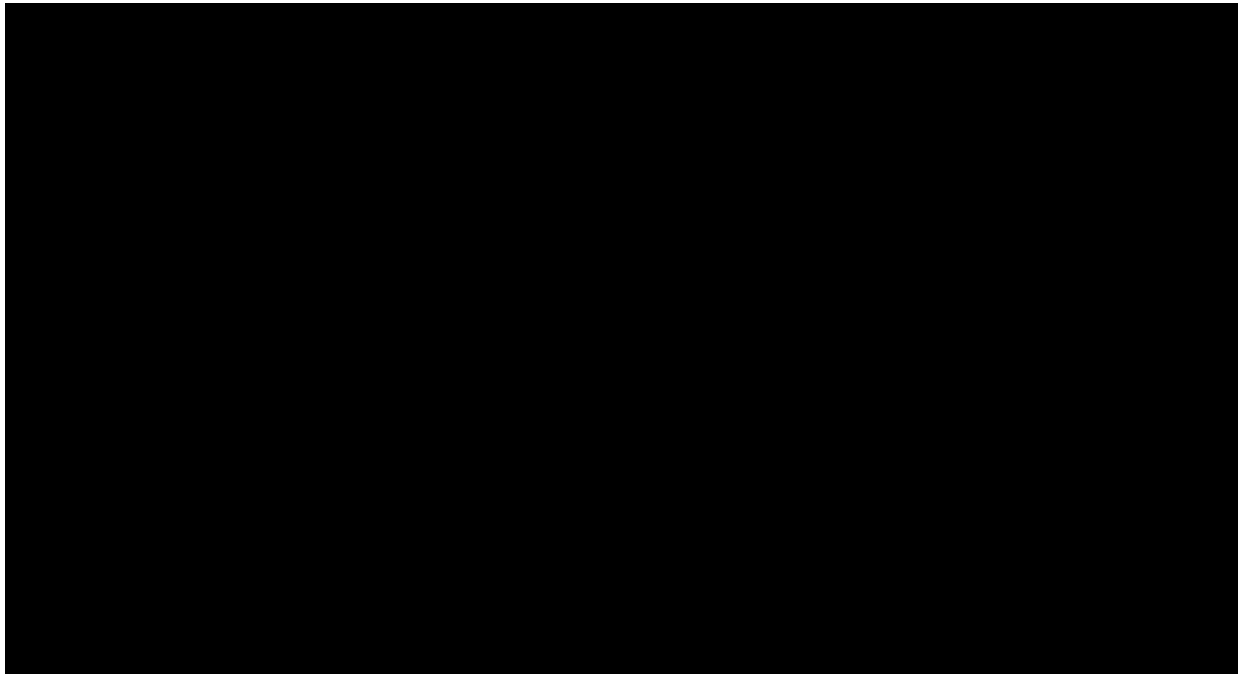
68

Dickens' Admits the



Report Demonstrates Down-Conversion

Dickens' Admission:



POR,19,43-45, 52-54; Reply,13; Sur-Reply,
16-17; Ex. 2010,7-8; Ex. 2041,54:2-8.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

69

Claim Construction

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

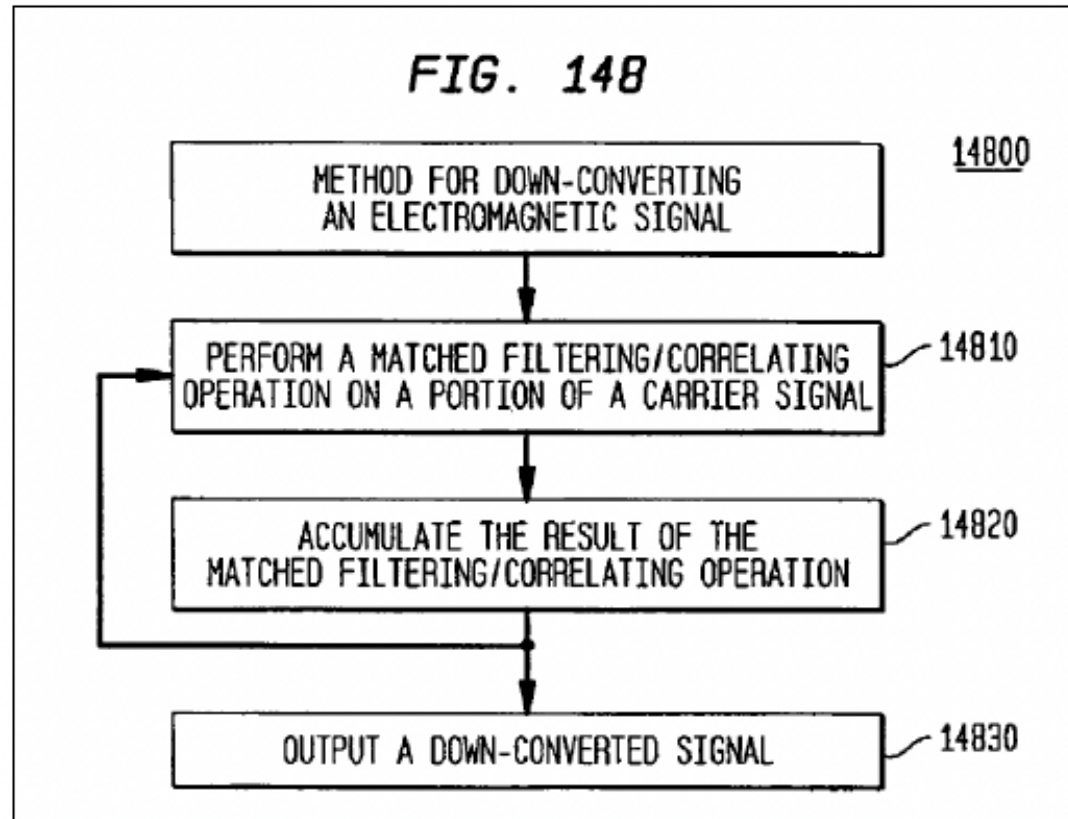
70

Claim Construction – “Matched Filtering/Correlation Module”

Proposed Construction:

- **PO** — “circuitry that samples an input signal at an aliasing rate using a switch such that energy of the input signal is integrated and *transferred to a load to form a down-converted signal*”
- **Petitioner** — Does not require that energy is transferred to a load

Claim Construction – “Matched Filtering/Correlation Module”

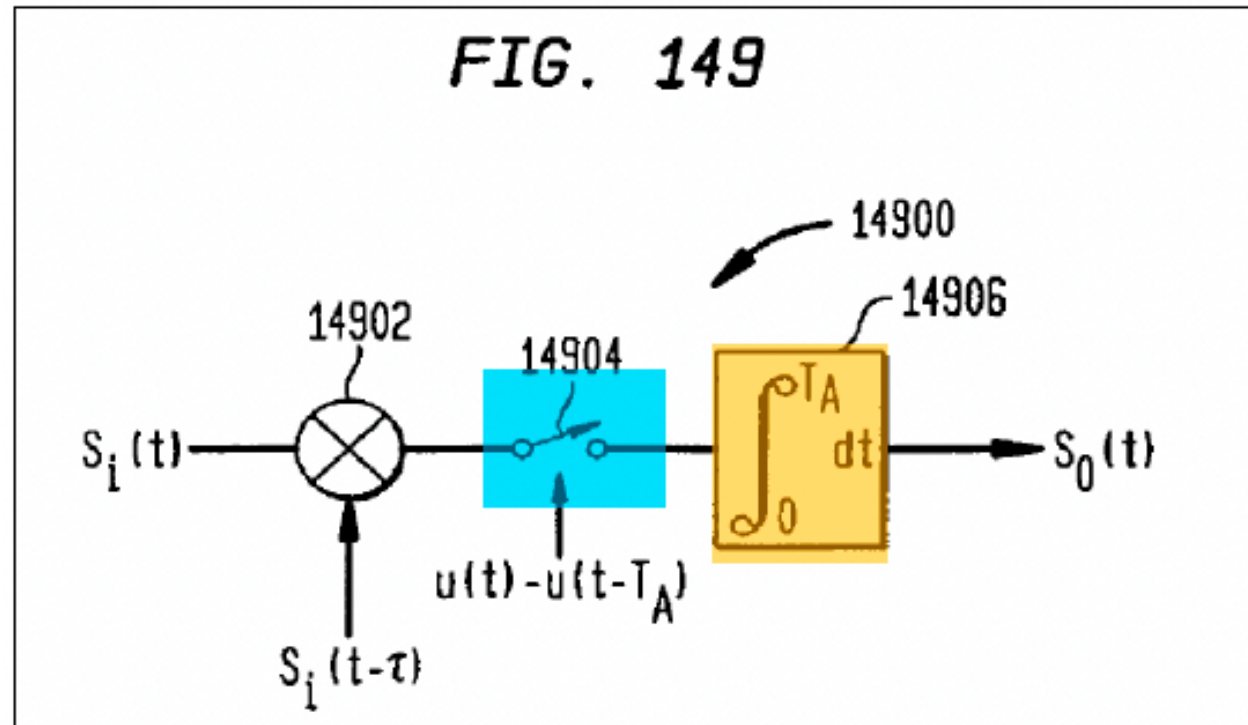


POR, 57-68; Sur-Reply, 26-35.

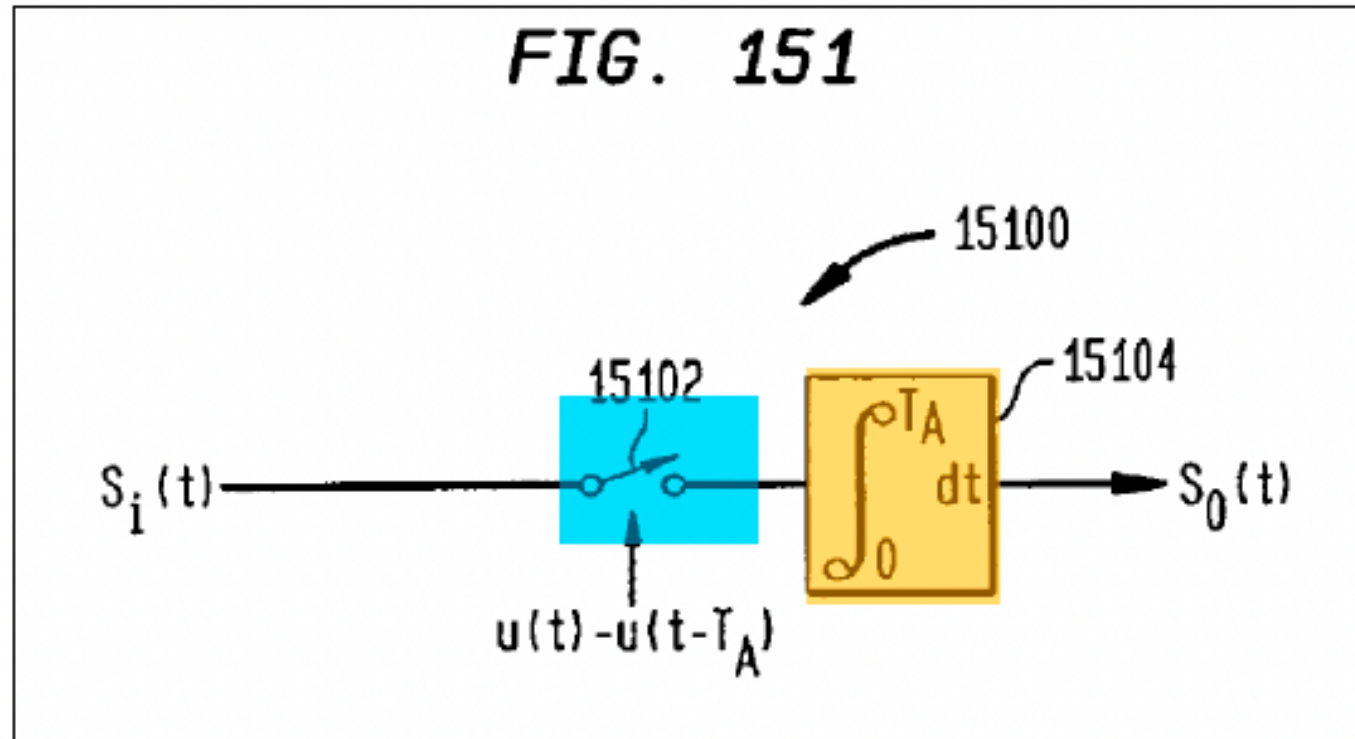
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

72

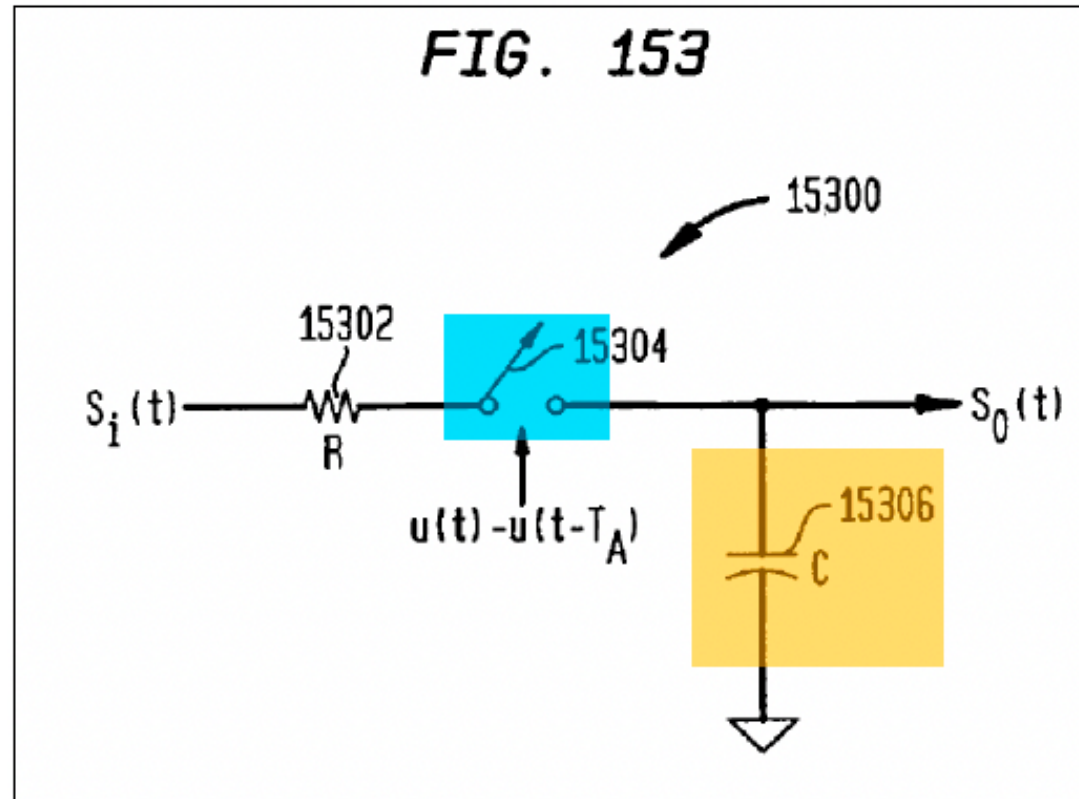
Claim Construction – “Matched Filtering/Correlation Module”



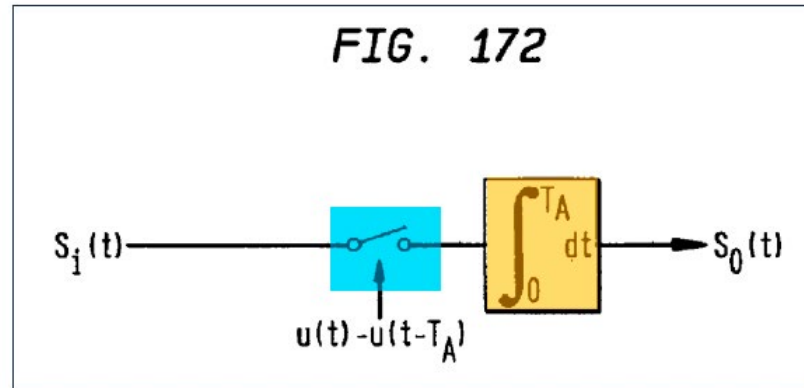
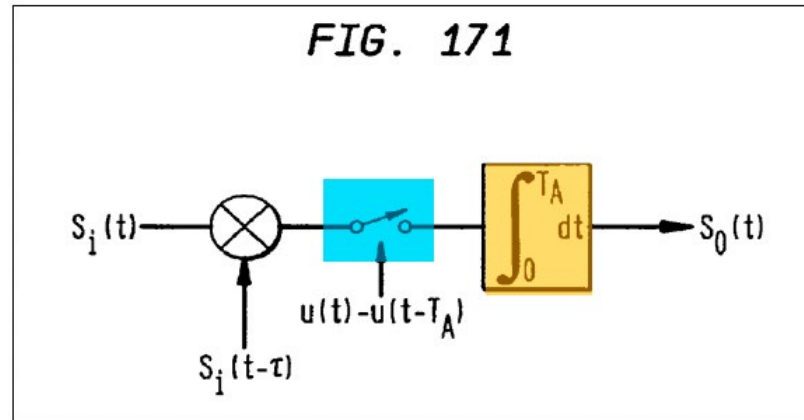
Claim Construction – “Matched Filtering/Correlation Module”



Claim Construction – “Matched Filtering/Correlation Module”



Claim Construction – “Matched Filtering/Correlation Module”

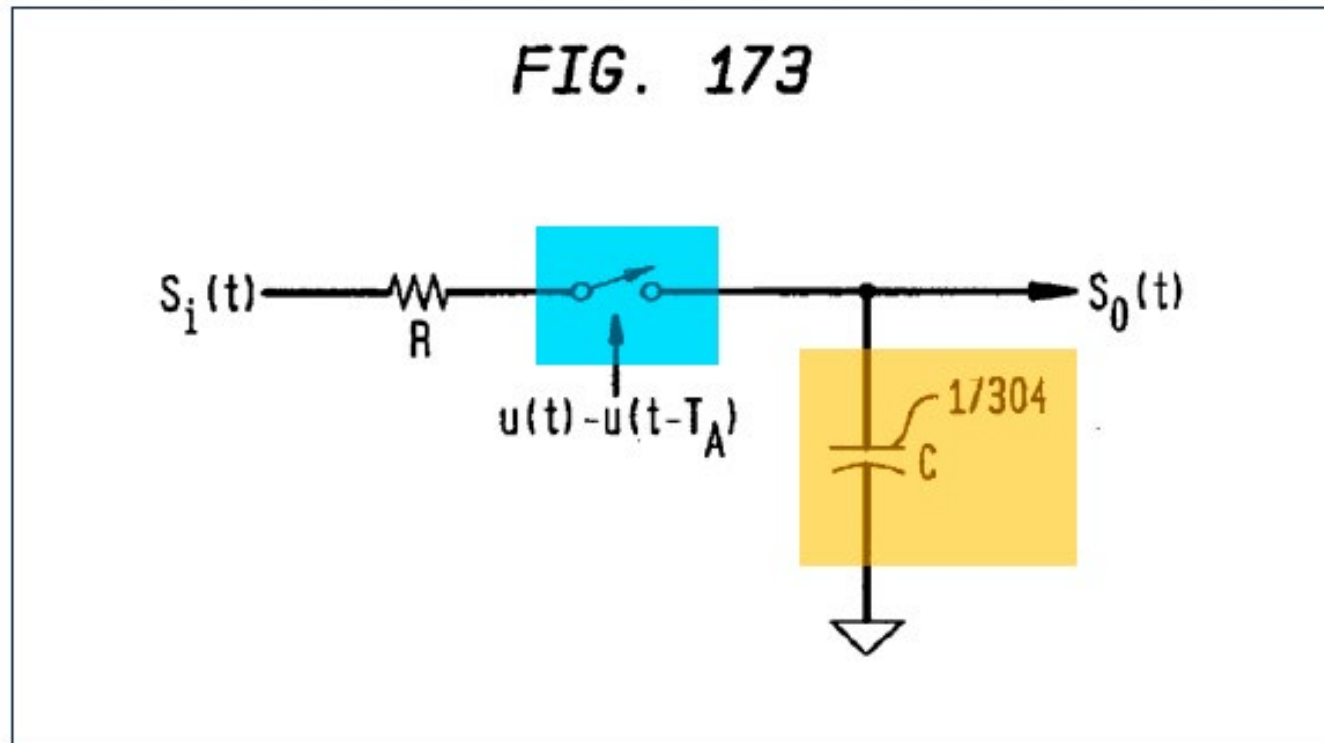


POR, 57-68; Sur-Reply, 26-35.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

76

Claim Construction – “Matched Filtering/Correlation Module”



Claim Construction – “Matched Filtering/Correlation Module”

The results of each matched filtering/correlating process are accumulated, for example using a capacitive storage device, and used to form a down-converted version of the electromagnetic signal.

Claim Construction – “Matched Filtering/Correlation Module”

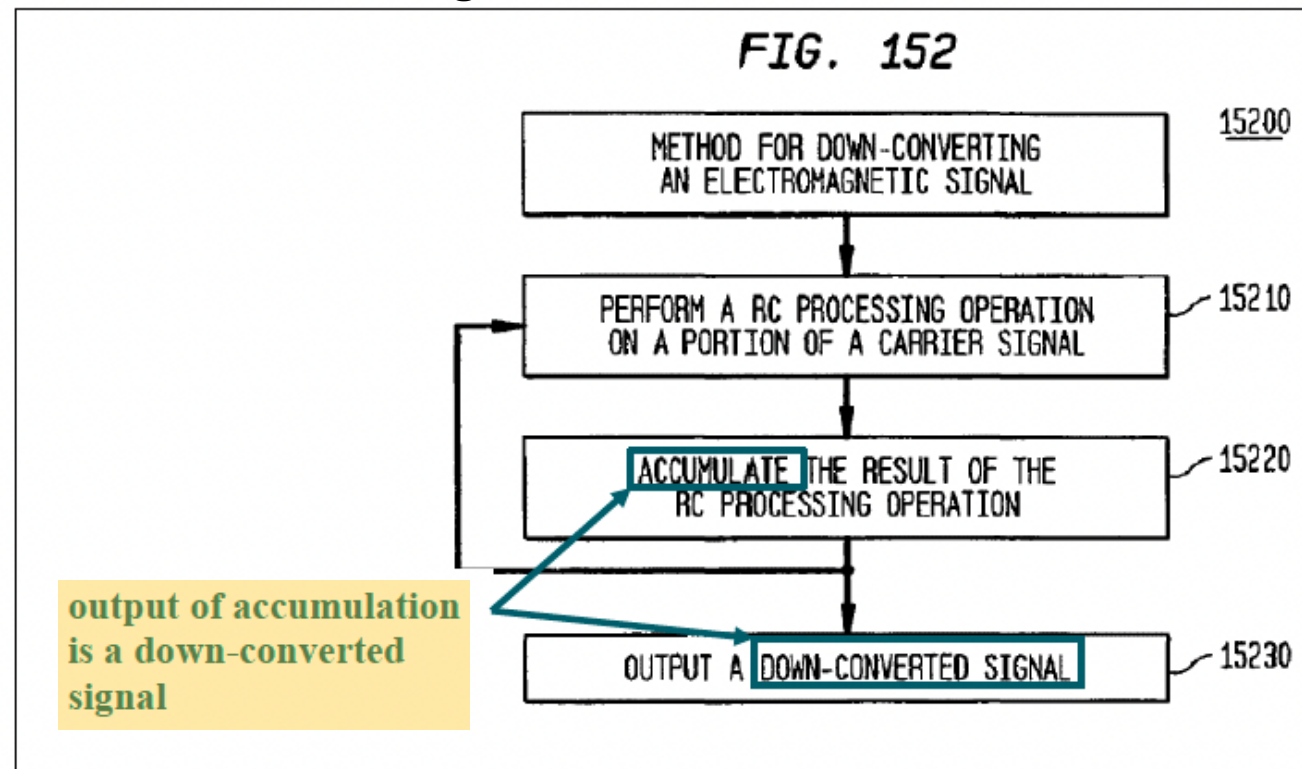
5.2 Load Resistor Consideration

The general forms of the differential equation and transfer function, described above, for embodiments of the present invention are the same as for a case involving a load resistor, R_L , applied across capacitor, C . FIG. 175A illustrates an example RC processor embodiment 17502 of the present invention having a load resistance 17504 across a capacitance 17506.

FIG. 175B illustrates an example implementation of the invention, modeled as a switch S , a capacitor C_S , and a load resistance R . FIG. 175D illustrates example energy transfer pulses, having apertures A , for controlling the switch S . FIG. 175C illustrates an example charge/discharge timing diagram for the capacitor C_S , where the capacitor C_S charges during the apertures A , and discharge between the apertures A .

Claim Construction – “Matched Filtering/Correlation Module”

Petitioner’s Annotated Figure 152:

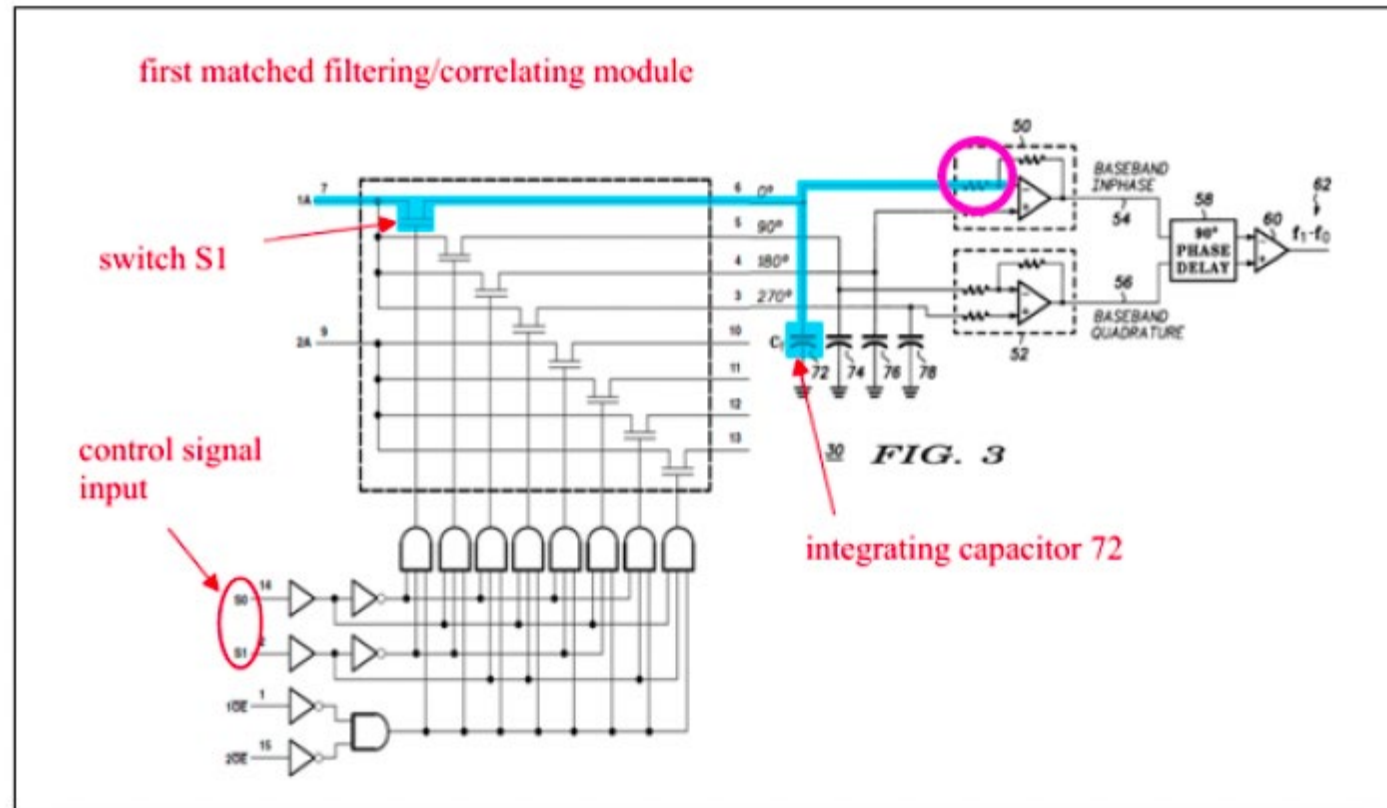


POR, 63-68; Reply, 25-29; Sur-Reply, 26-35;
Ex. 1001, 130:28-31, 147:35-42, 148:17-24.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

80

The Petition Identifies a Load for the Claimed “Matched Filtering/Correlation Module”

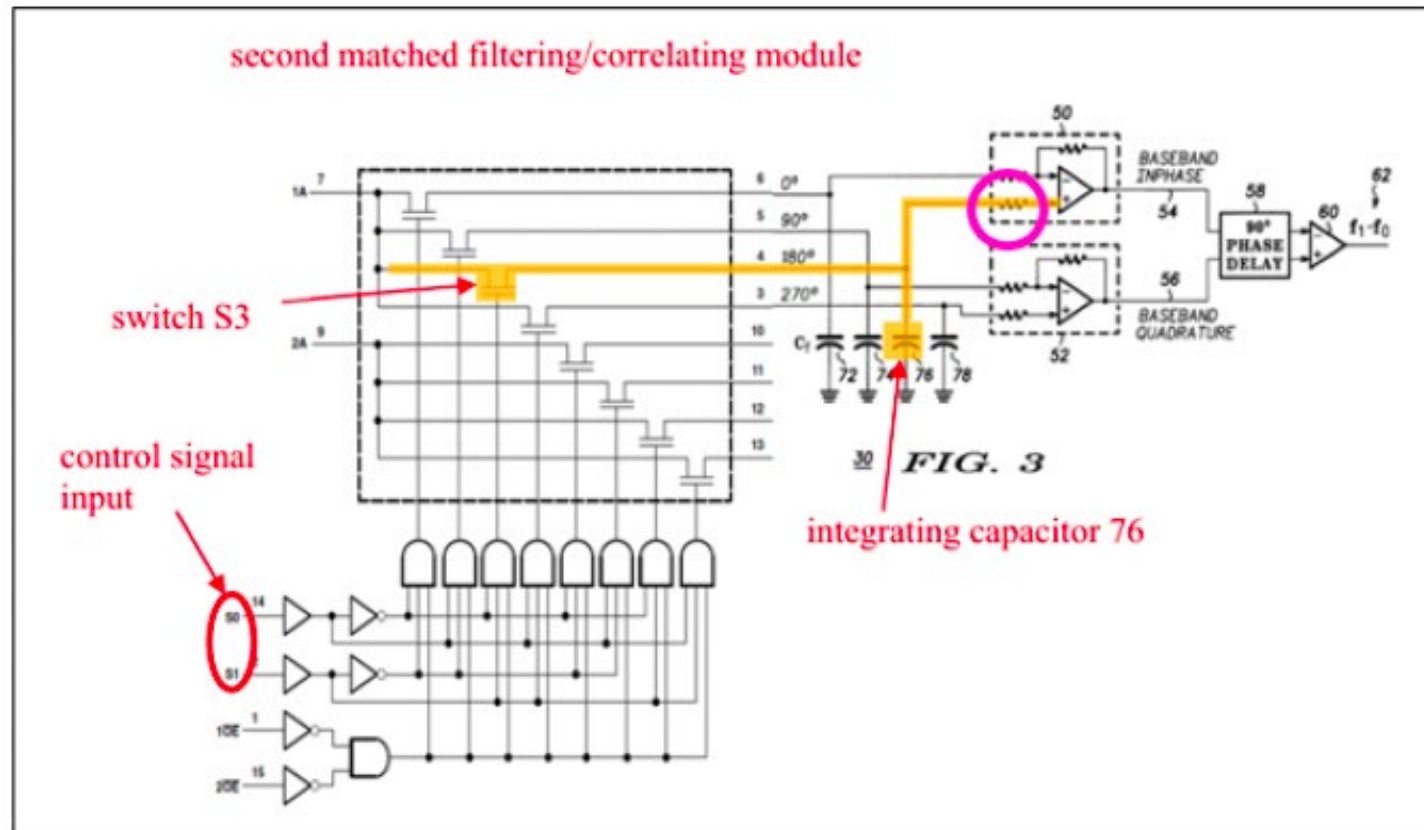


POR, 63-68; Reply, 25-29; Sur-Reply, 26-35;
Ex. 1003, ¶¶ 136, 149, 174, 185.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

81

The Petition Identifies a Load for the Claimed “Matched Filtering/Correlation Module”

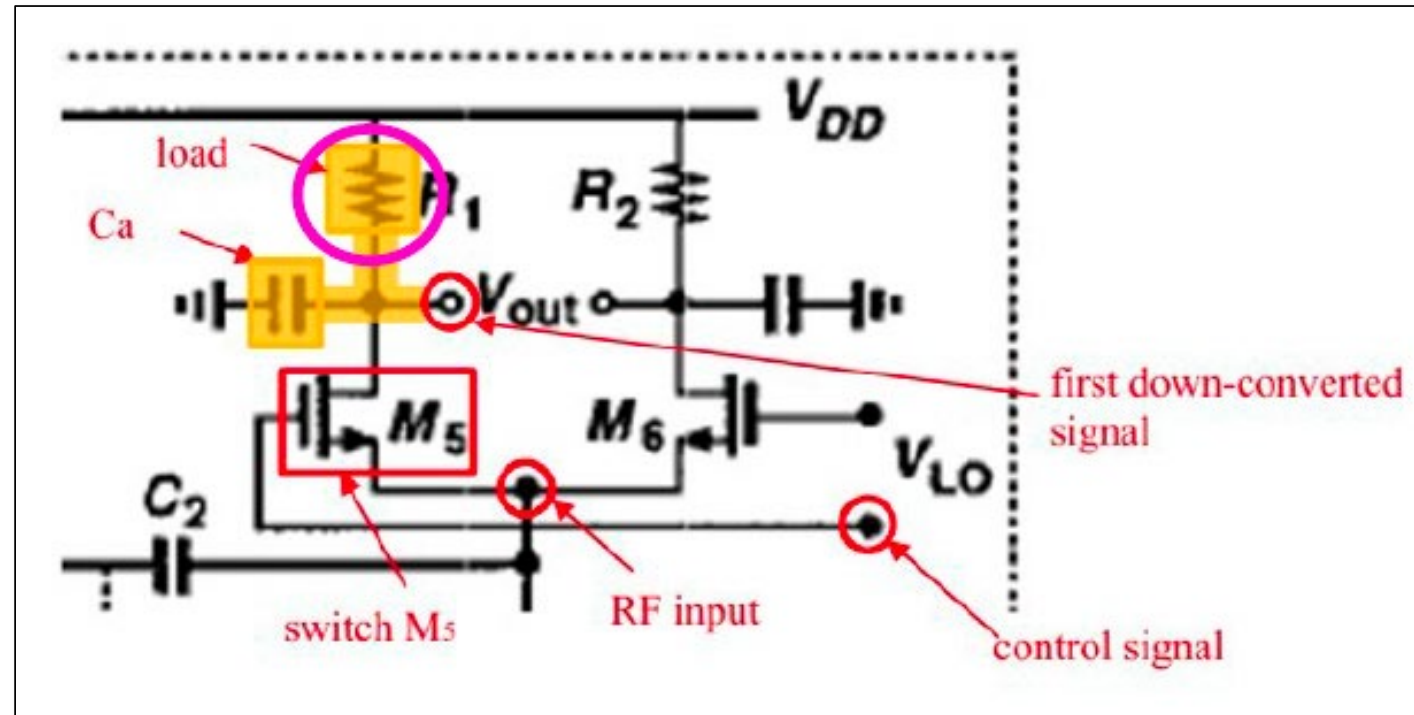


POR, 63-68; Reply, 25-29; Sur-Reply, 26-35;
Ex. 1003, ¶¶ 136, 149, 174, 185.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

82

The Petition Identifies a Load for the Claimed “Matched Filtering/Correlation Module”

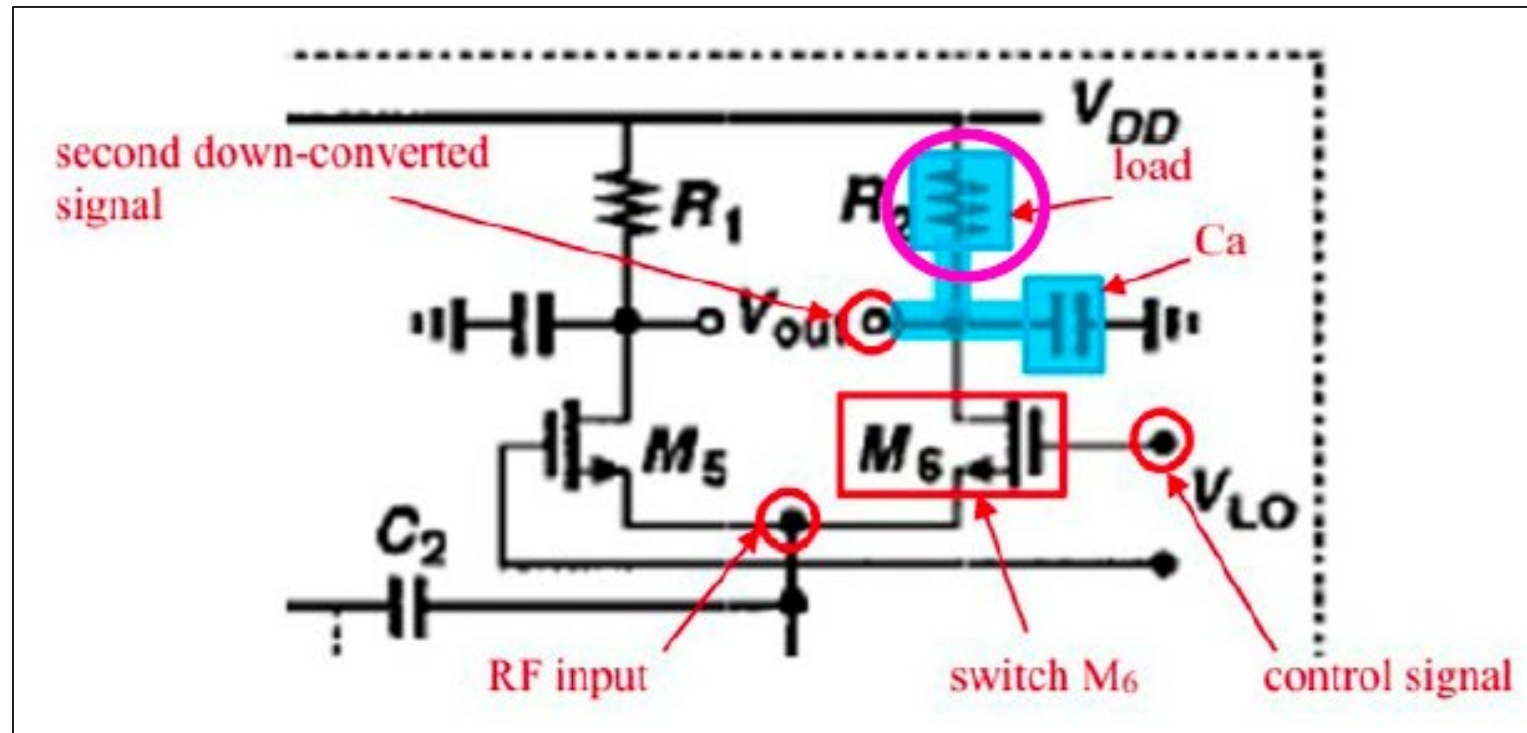


POR, 63-68; Reply, 25-29; Sur-Reply, 26-35; Ex. 1003, ¶¶136,149,174,185.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

83

The Petition Identifies a Load for the Claimed “Matched Filtering/Correlation Module”



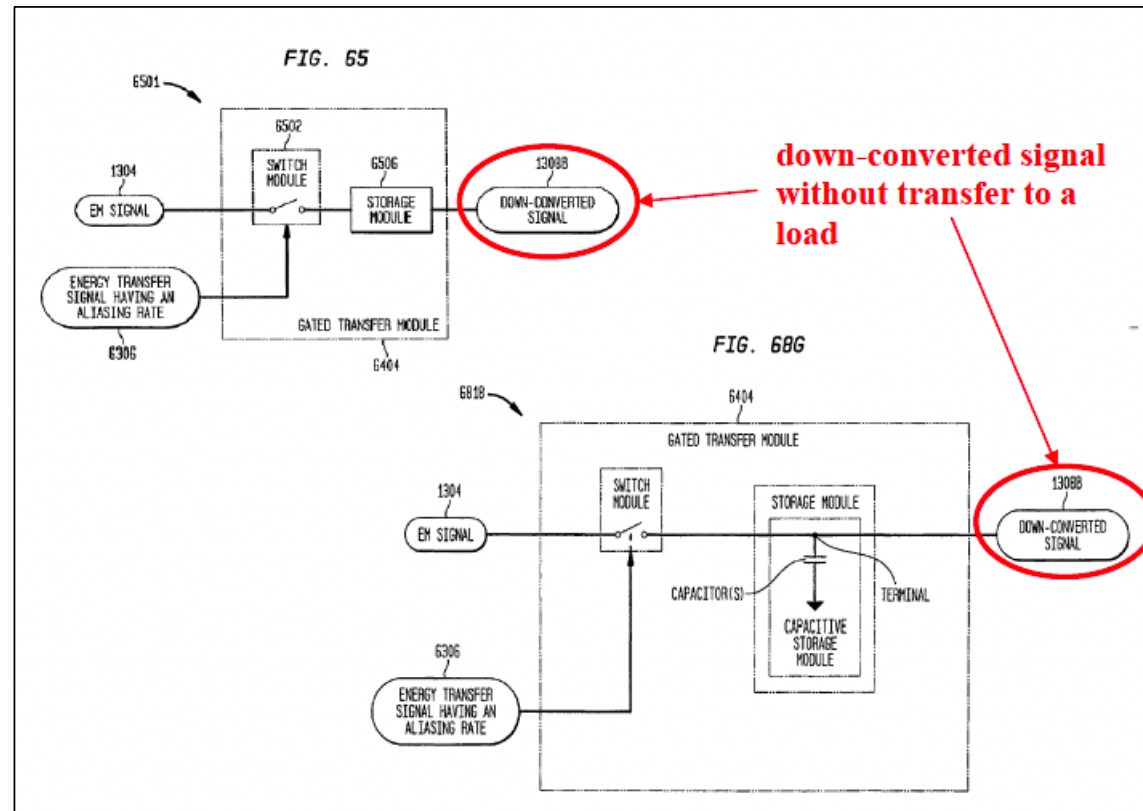
POR, 63-68; Reply, 25-29; Sur-Reply, 26-35; Ex. 1003, ¶¶136, 149, 174, 185.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

84

Figures 65/68G Require a Load

Reply:



POR, 63-68; Reply, 30-31; Sur-Reply, 31-32;
Ex. 1001, Figs. 65, 86G.

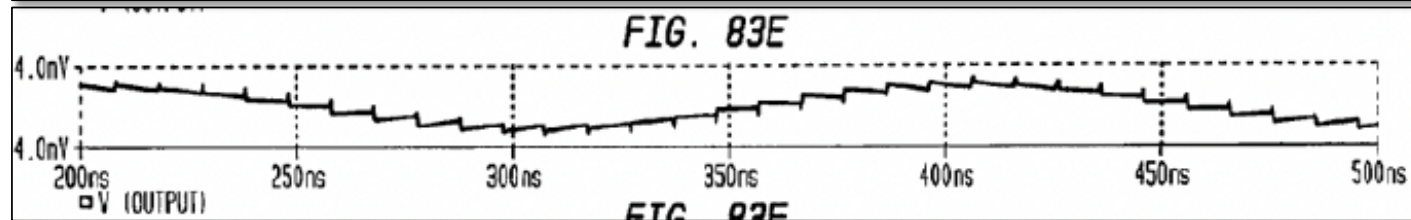
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

85

Figures 65/68G Require a Load

For example, operation of the switch module 6502 and the storage module 6506 is now described for down-converting the EM signal 1304 to an intermediate signal, with reference to the flowchart 4607 and the example timing diagrams in FIG. 83A-F.

FIG. 68G illustrates an integrated gated transfer system 6818 that can be implemented to down-convert the EM signal 1304 as illustrated in, and described with reference to, FIGS. 83A-F.



Figures 65/68G Require a Load

Galton:

Charging and discharging indicates the presence of a load, correct?

MR. MAGEE: Objection to form.

A. We'd have to look at a particular embodiment, but generally, yes.

A Okay. So this architecture where there is a switch which is closed and opened at an aliasing rate in perfect synchrony with the carrier, and then integrated over a -- over the aperture window, and then output, that is -- that has all the features of a matched filter/correlator. So it has a switch that opens and closes with an aperture rate. It's -- the aperture is synchronous with the -- with the carrier of the signal. And the integration is performed over that window.

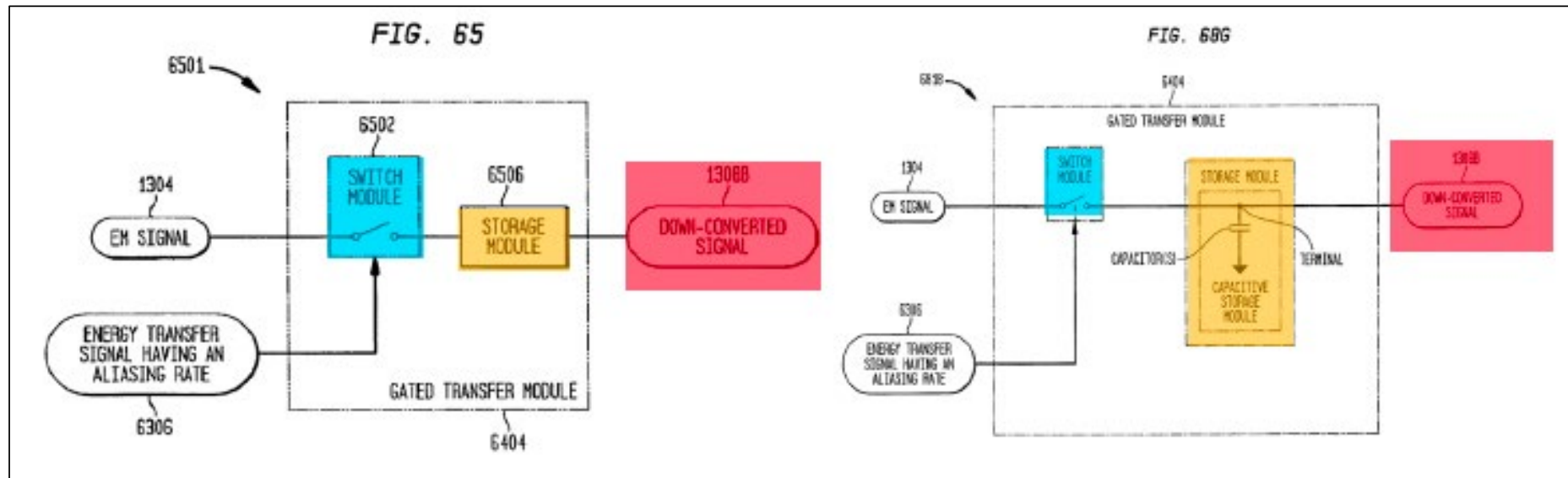
Reply, 31-32; Sur-Reply, 31-32; Ex.
2040, 12:10-22; Ex. 2034, 26:16-27:16.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

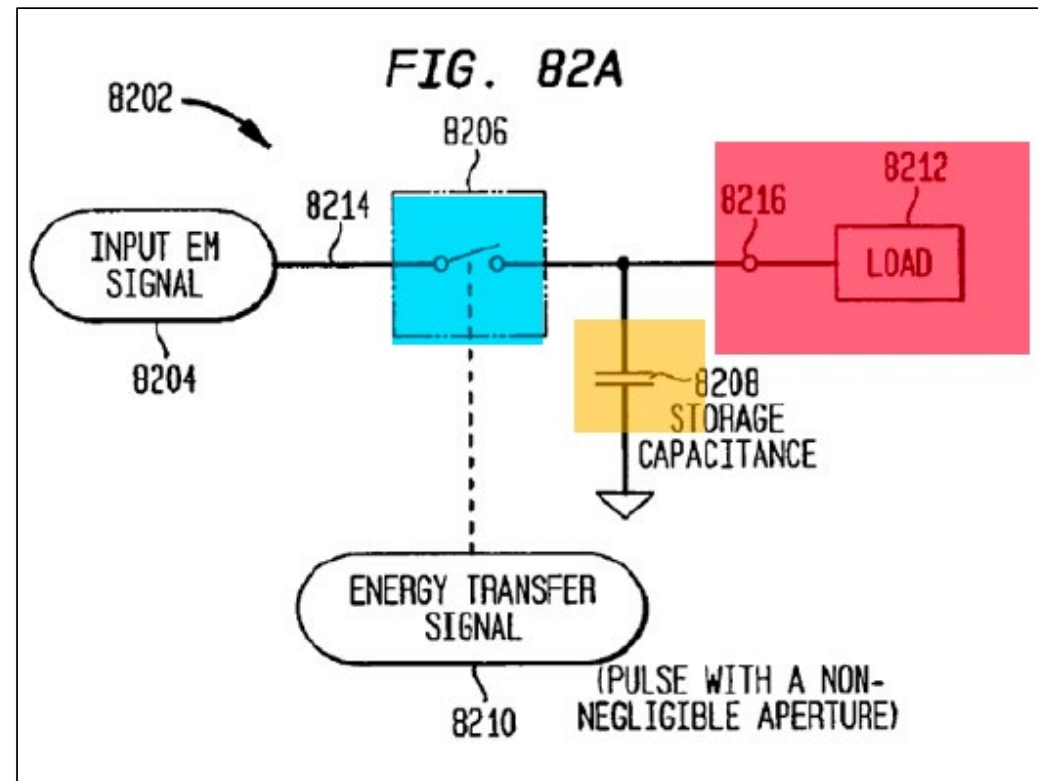
87

Figures 65/68G Require a Load

FIGS. 83A-F illustrate example timing diagrams for the energy transfer system 8202 in FIG. 82. FIG. 83A illustrates an example input EM signal 8302.



Figures 65/68G Require a Load



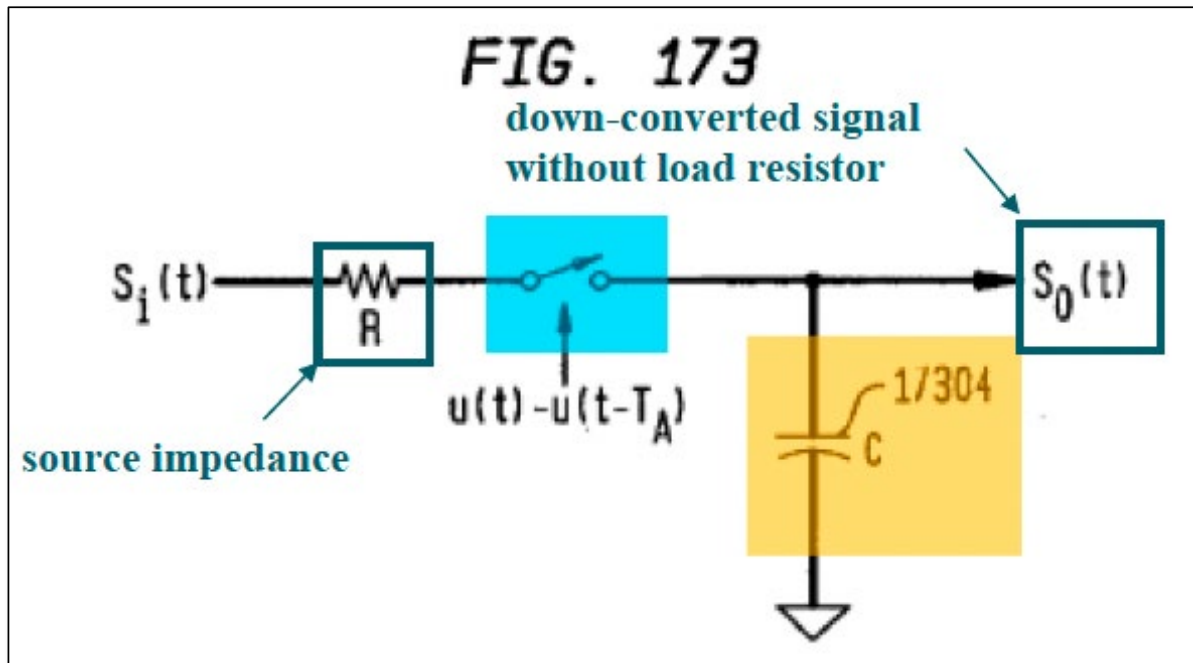
Reply,31-32; Sur-Reply, 32-33; Ex.-
1001,74:20-21, Figs. 65, 68G, 82A.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

89

Figure 173 Relates to Charge Accumulation

Reply:



Maximizing the charge, q , requires maximizing EQ. (37) with respect to t and β

40

$$\frac{\partial^2 V_0(t)}{\partial t \partial \beta} = 0$$

EQ. (55)

45

It is easier, however, to set $R=1$, $T_A=1$, $A=1$, $f_A=T_A^{-1}$ and then calculate $q=cV_0$ from the previous equations by recognizing that

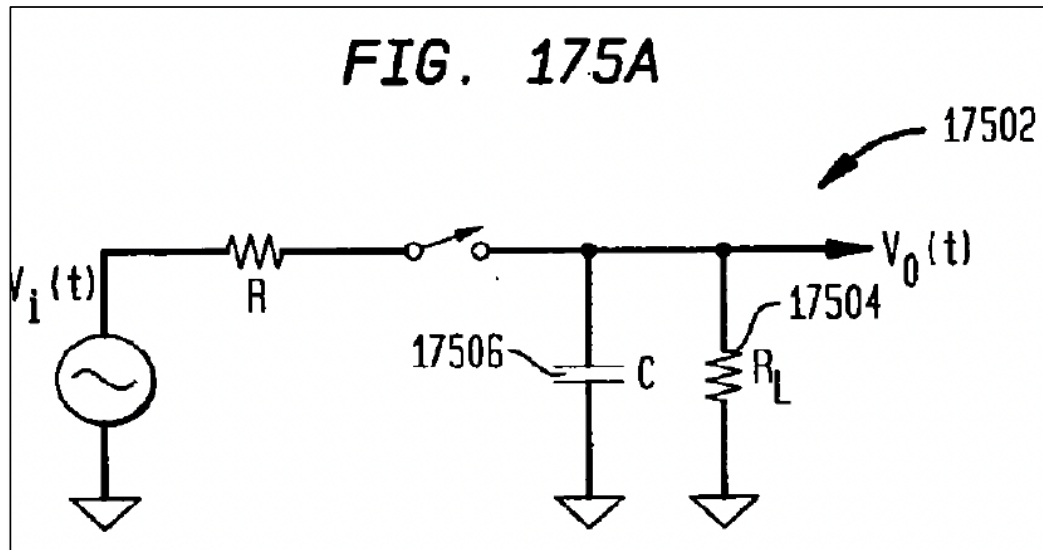
50

$$q = \frac{\beta^{-1}}{R} V_0 = cV_0,$$

charge independent of load impedance

55 which produces a normalized response.

Figure 175A Shows How Load Affects Discharge



5.2 Load Resistor Consideration

The general forms of the differential equation and transfer function, described above, for embodiments of the present invention are the same as for a case involving a load resistor, R_L , applied across capacitor, C . FIG. 175A illustrates an example RC processor embodiment 17502 of the present invention having a load resistance 17504 across a capacitance 17506.

Tayloe/TI-Datasheet

Does Not Render Claim 14 Obvious

Tayloe is Not Prior Art

Filed: Oct. 15, 1998

(12) **United States Patent**
Tayloe

(10) Patent No.: **US 6,230,000 B1**
(45) Date of Patent: **May 8, 2001**

(54) **PRODUCT DETECTOR AND METHOD THEREFOR**

(75) Inventor: **Daniel Richard Tayloe**, Phoenix, AZ (US)

(73) Assignee: **Motorola Inc.**, Schaumburg, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/173,030**
(22) Filed: **Oct. 15, 1998**

(51) Int. Cl.⁷ **H04B 1/26; H04B 1/00**
(52) U.S. Cl. **455/323; 455/303; 455/304; 455/313**

(58) Field of Search 455/302, 303, 455/304, 324, 338, 339, 313, 318, 323, 375/323, 329, 332, 327/113, 45; 329/304

(56) **References Cited**
U.S. PATENT DOCUMENTS
4,847,860 * 7/1989 Robert 375/136
4,878,029 10/1989 Saulnier et al. 329/341
5,150,124 9/1992 Moore et al. 342/68
5,339,459 8/1994 Schiltz et al. 455/333
5,355,103 * 10/1994 Kozak 455/289
5,557,642 9/1996 Williams 375/316
5,761,615 * 6/1998 Jaffee 455/314
5,805,093 9/1998 Heikkinen et al.
5,838,675 * 11/1998 Rauscher 370/343
5,999,574 * 12/1999 Sun et al. 375/326
6,073,001 * 6/2000 Sokoler 455/323
6,088,581 * 7/2000 Bickley et al. 455/131
FOREIGN PATENT DOCUMENTS
0691733 6/1995 (EP) H03B21/00

(57) **ABSTRACT**
A product detector for converting a signal to baseband includes a commutating switch which serves to sample an RF waveform four times per period at the RF frequency. The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees. The average voltage at 0 degrees is the baseband in-phase signal, and the average voltage at 90 degrees is the baseband quadrature signal. Alternatively, to increase gain, the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal, and the 90 degree average can be differentially summed with the 270 degree average to produce the baseband quadrature signal.

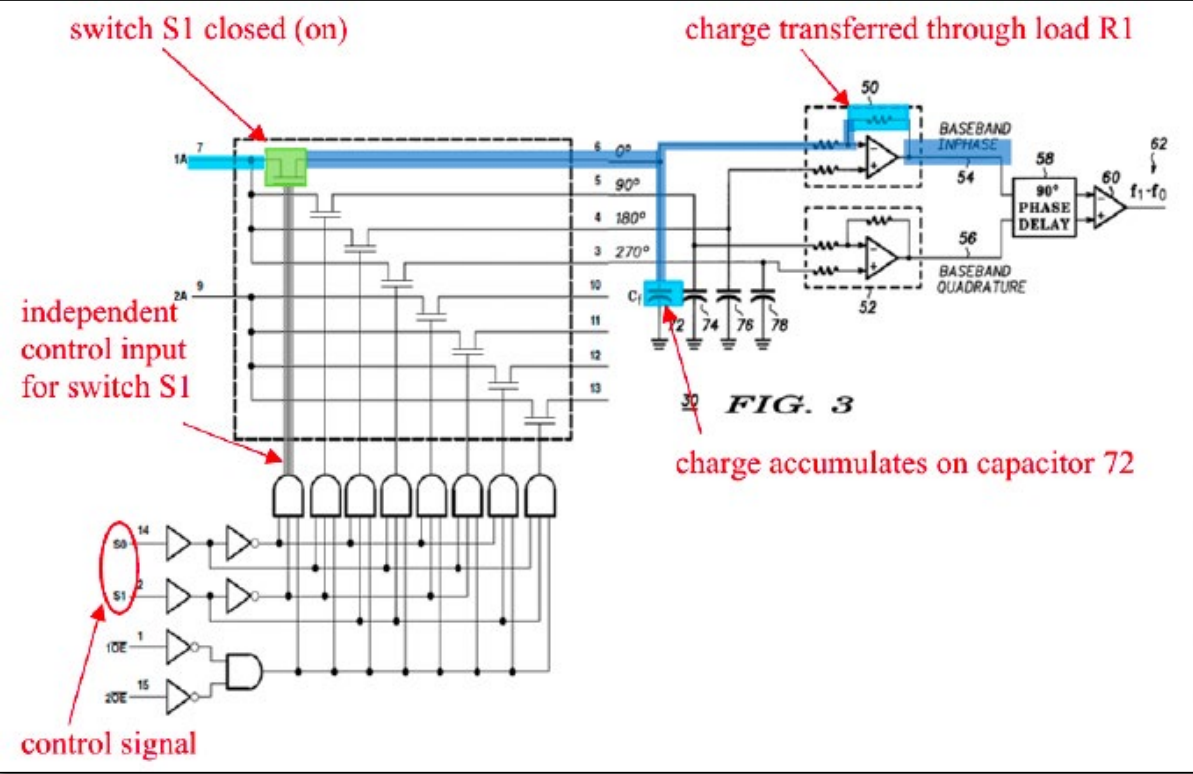
14 Claims, 3 Drawing Sheets

Ex. 1004; POR, 94.

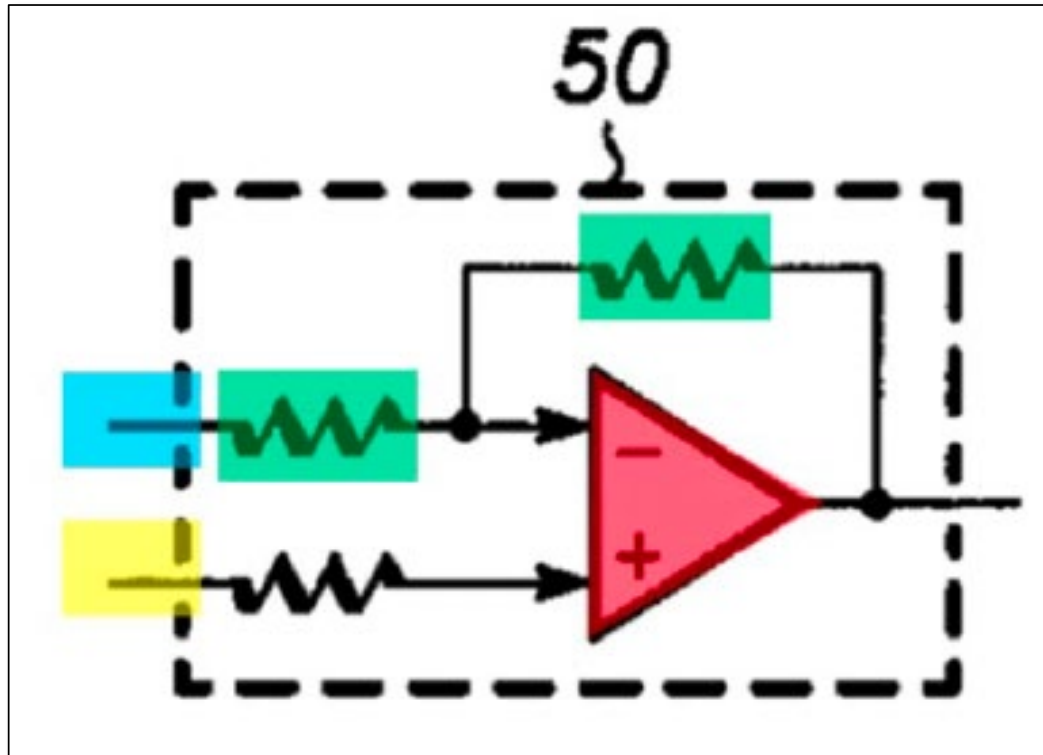
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

93

Tayloe



Tayloe Does Not Transfer Energy to a Load



POR, 94-100; Sur-Reply, 35-39; Ex.
2024, ¶¶ 127, 226-34; Ex. 2034, 72:14-73:6.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

Q And just looking at the op amp circuit itself, the gates of a MOSFET have a very, very high resistance. Correct?

MR. MAGEE: Objection to form.

A Yes.

THE WITNESS: Sorry, Bobby.

A Yes. But again, subject to the -- you know, the precondition that we're taking the op amp out of the circuit and looking at it in

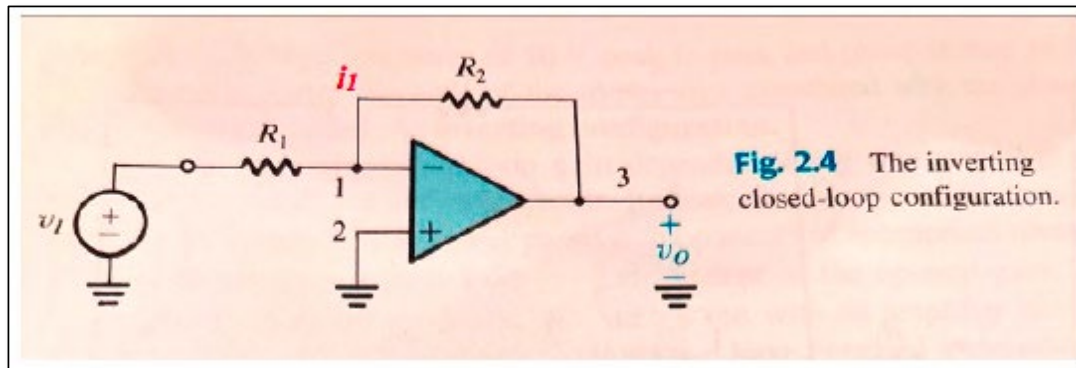
Q Correct.

So my answer -- the answer is I'm correct if we're taking the op amp and looking at it outside of the rest of the circuit. Correct?

A Yes.

95

Sedra is Not Relevant



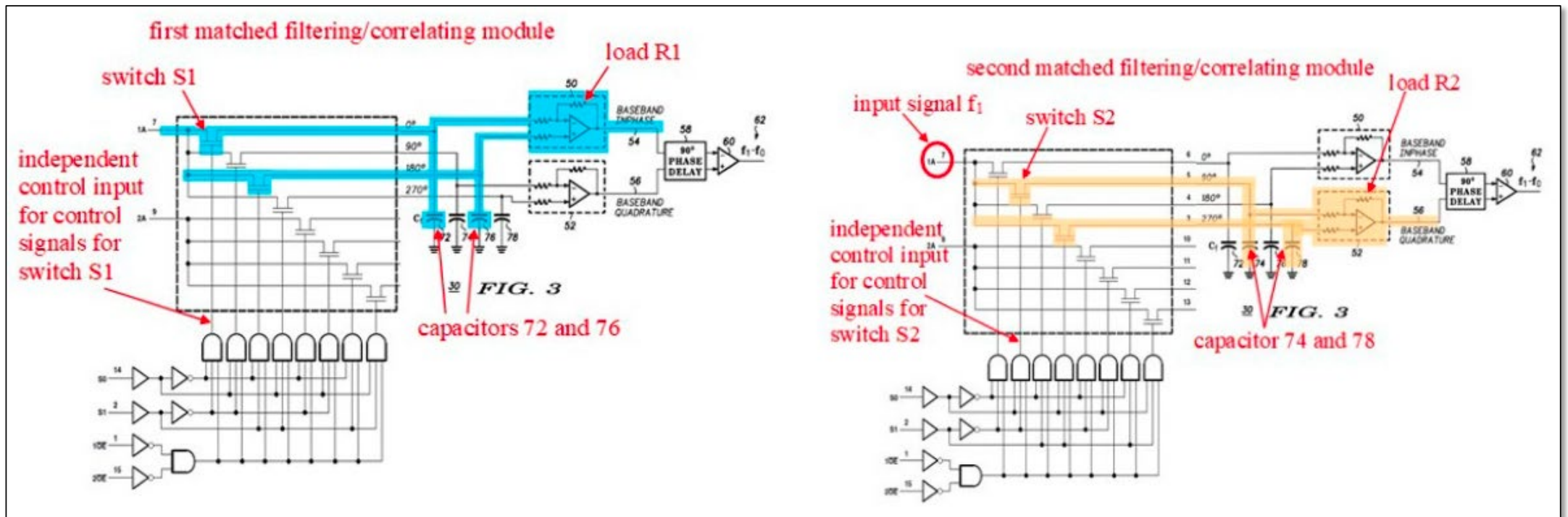
Q. All right. And that figure 2.4 is from the Sedra Smith textbook, correct?

A. Yes.

Q. All right. And in figure 2.4 of Sedra, the plus terminal of the Op-amp circuit is connected to ground, correct?

A. Yes.

Taylor Uses a Different Configuration Than Sedra



Pet., 26, 43; POR, 94-100; Reply, 37-38;
Sur-Reply, 35-39; Ex. 2040, 15:5-11

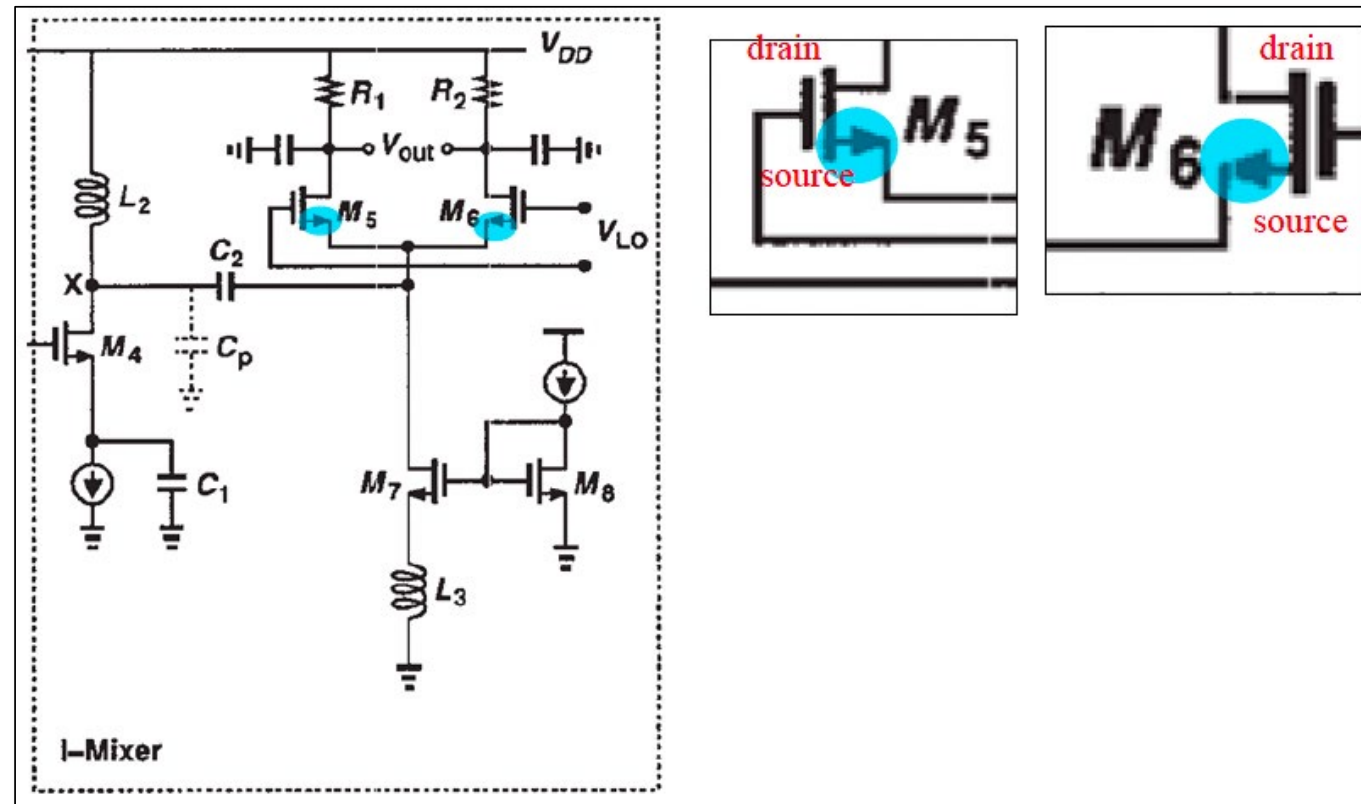
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

97

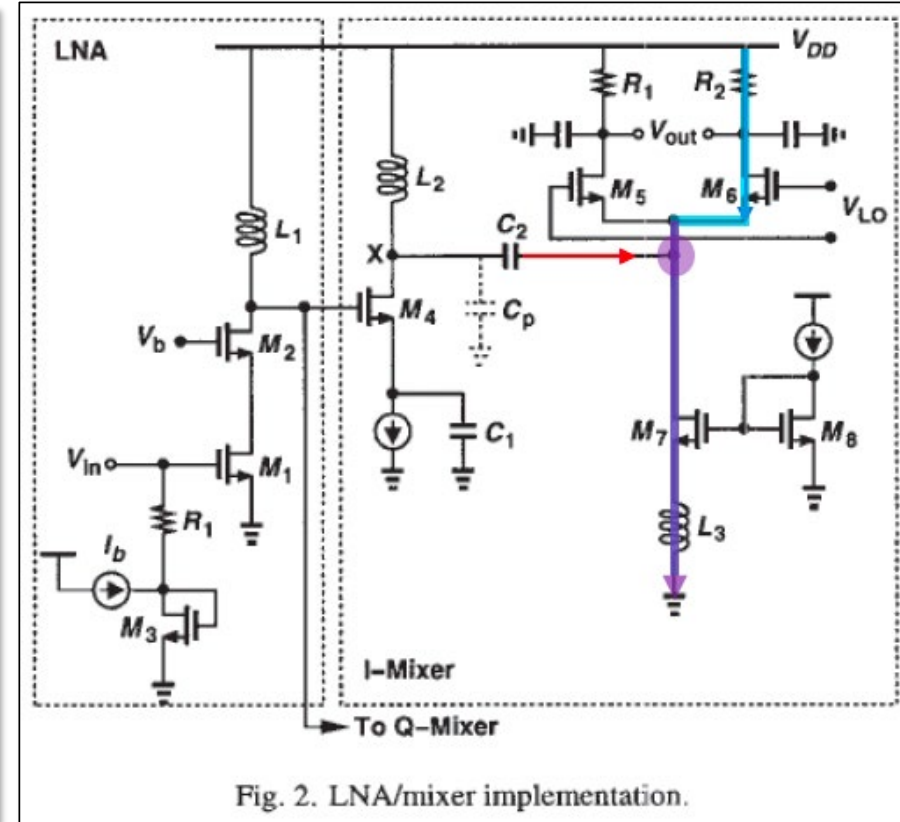
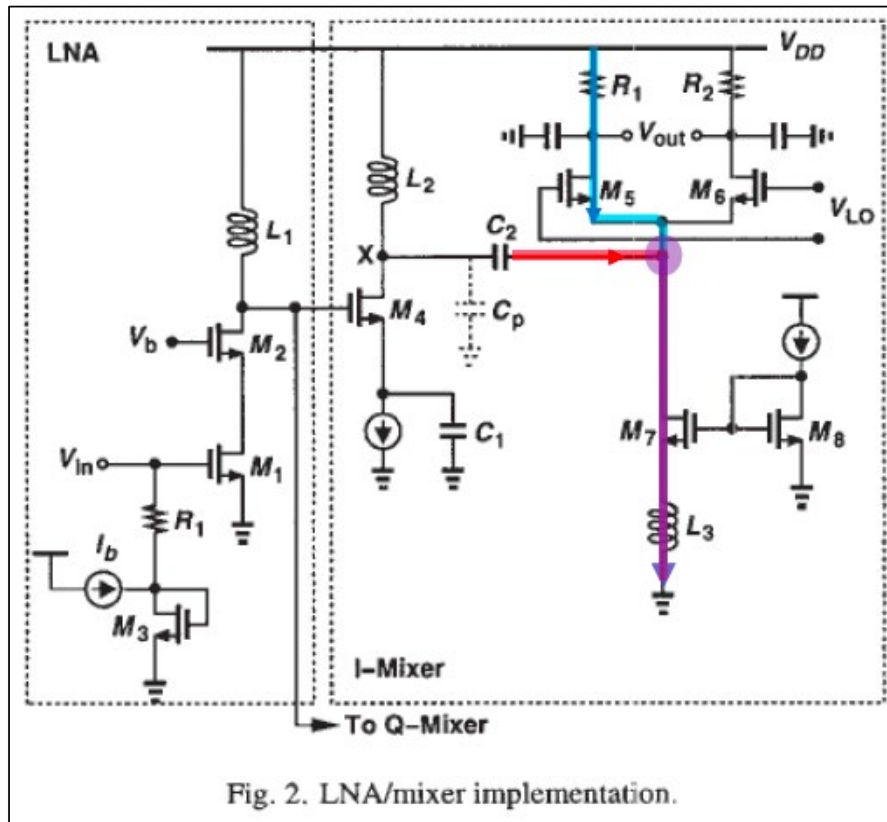
Razavi

Does Not Render Claim 14 Obvious

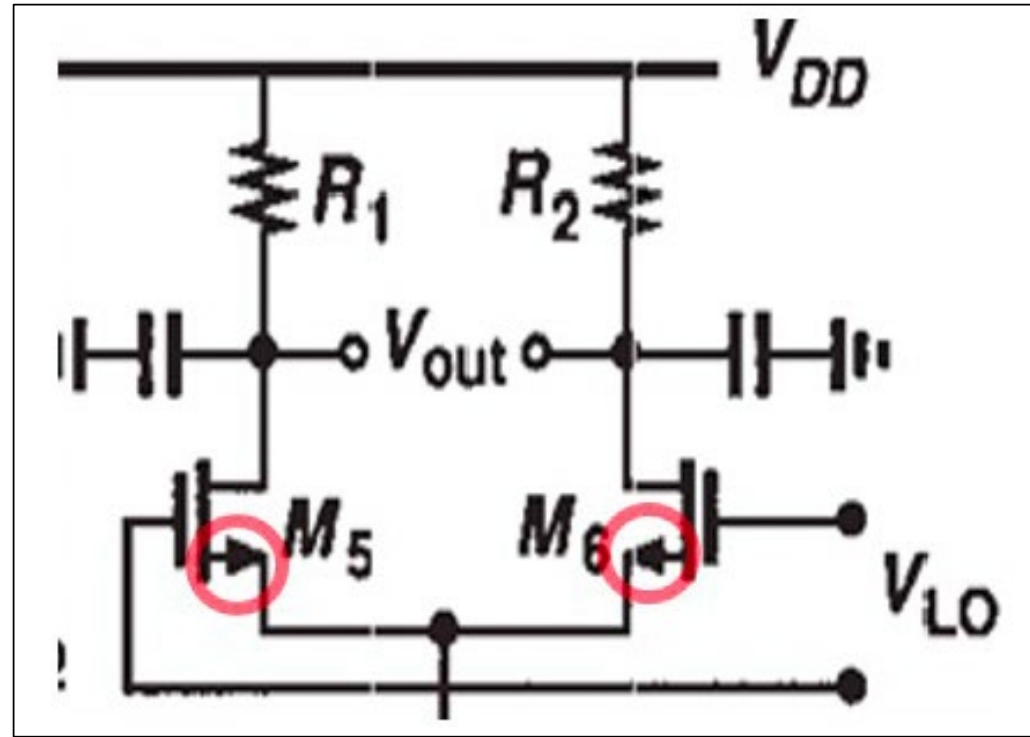
Razavi



Razavi



Razavi Does Not Disclose Sampling an Input (RF) Signal at an Aliasing Rate

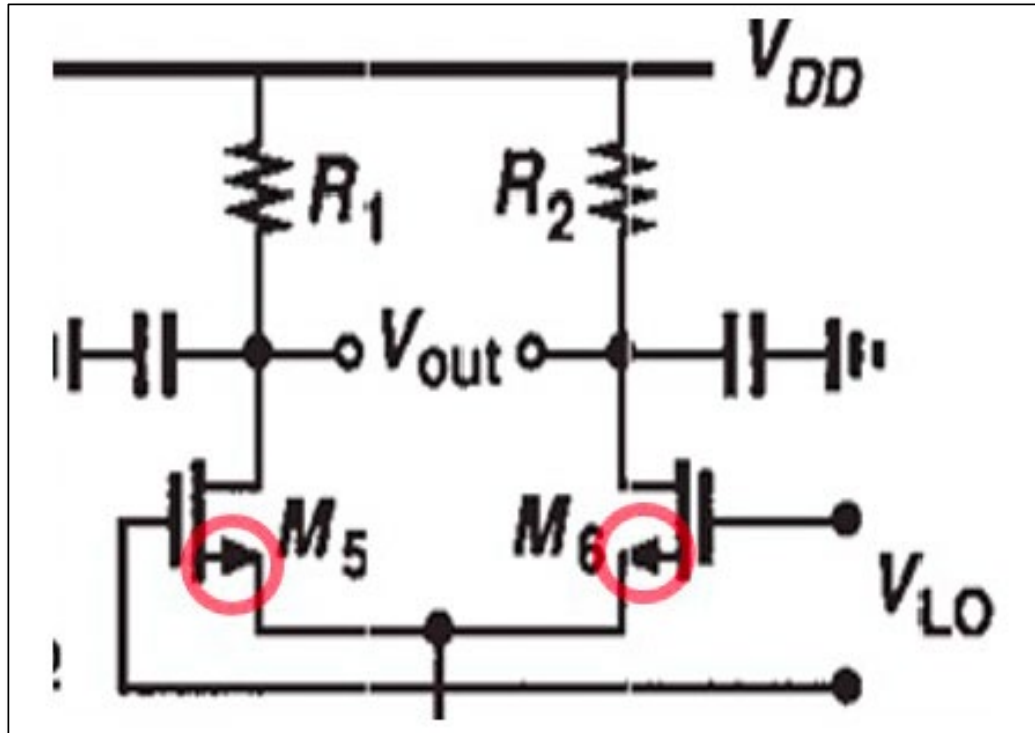


POR, 101-107; Sur-Reply, 39-44;
Ex. 2024, ¶¶306-22; Ex. 1017,1.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

101

Razavi Does Not Disclose Sampling an Input (RF) Signal at an Aliasing Rate



To achieve a high conversion gain, M_5 and M_6 must remain in saturation and, more importantly, the voltage drop across R_1 and R_2 must be maximized.

Galton:

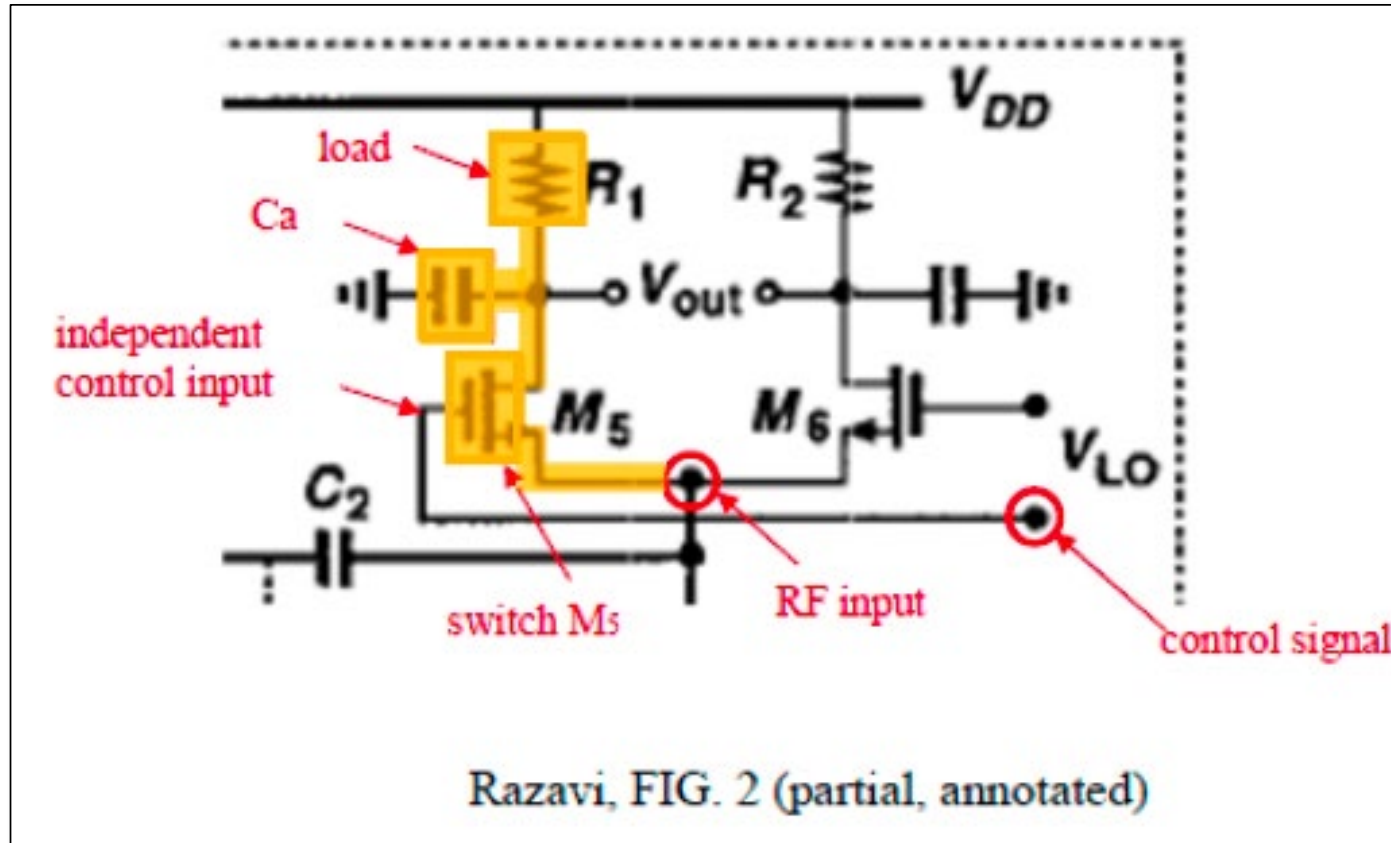
Q. (BY MR. CHARKOW) Okay. In saturation, an NMOS transistor conducts current from drain to source, correct?

A. In --

MR. MAGEE: Objection to form.

A. In saturation, a -- an NMOS transistor conducts current -- conventional current from drain to source, yes.

Razavi Does Not Disclose “Energy of the Input Signal is Integrated and Transferred to a Load to Form a Down-converted Signal.”



Claim 14 Should be Analyzed Based on Conventional Current

Galton:

So the ParkerVision patents refer to conventional current. You know, when you're talking about charging and discharging, it's talking about conventional current or it's discussing conventional current, correct?

A. We'd have to look at specific cases, but that's probably true.

Q. In circuits, "I" -- the letter I, capital I, stands for current, correct?

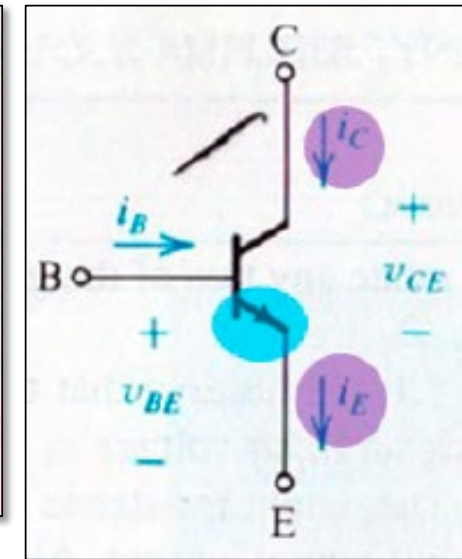
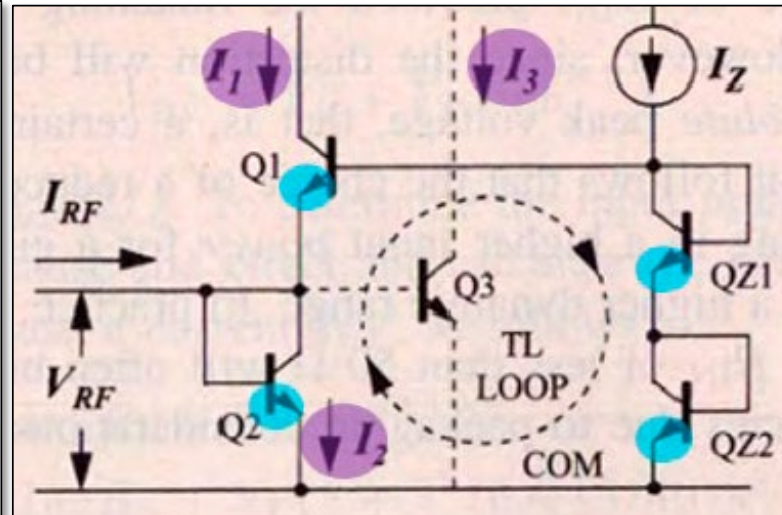
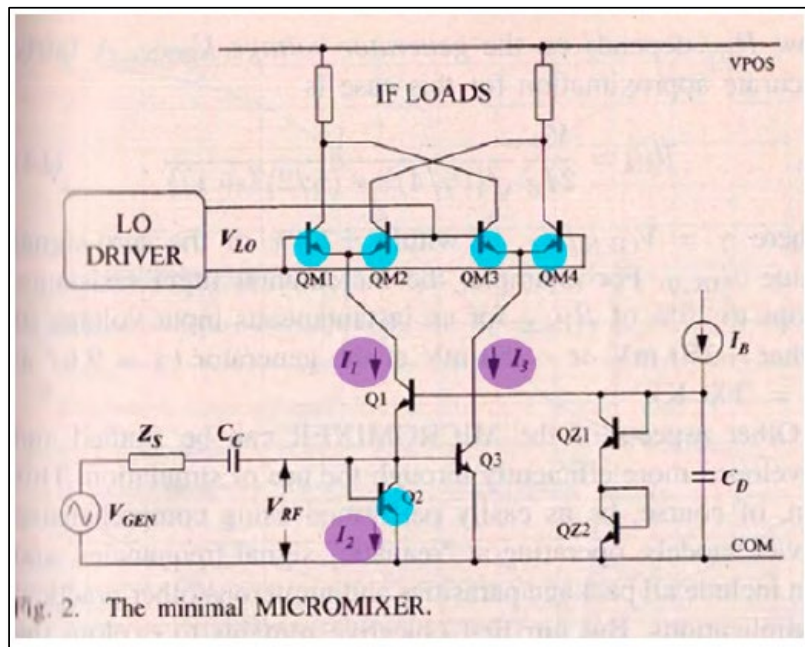
A. Often, yes.

Q. Okay. And "I" refers to conventional current, correct?

A. Sorry. It often does.

Claim 14 Should be Analyzed Based on Conventional Current

Petitioner's Technical References:



Sur-Reply, 40-44; Ex. 1053,13; Ex. 1046,40; Ex. 1045,25,34,76,77.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

105

Petitioner's Reply Violates 37 C.F.R. § 42.6(a)(3) and C.F.R § 42.22(a)(2).

Petitioner submitted two expert declarations collectively spanning *78 pages* (nearly *14,000 words/120 paragraphs*) of *substantive* analysis. But the Reply itself contains only short, conclusory arguments, followed by citations to numerous paragraphs in these declarations. *See, e.g.*, Reply, 11 (citing TI-1067, ¶¶16-20), 13 (citing TI-1067, ¶¶19-22), 29-30 (citing TI-1066, ¶¶8-11), 33, (citing TI-1066, ¶¶15-21, 92-97), 34 (citing TI-1066, ¶¶5-26), 37 (citing TI-1066, ¶¶ 32-45, 49-55), 38 (citing TI-1066, ¶¶49-53), 39 (citing TI-1066, ¶¶32-55), 40 (citing TI-1066, ¶¶65-71), 41 (citing TI-1066, ¶¶72-82, 89-99).