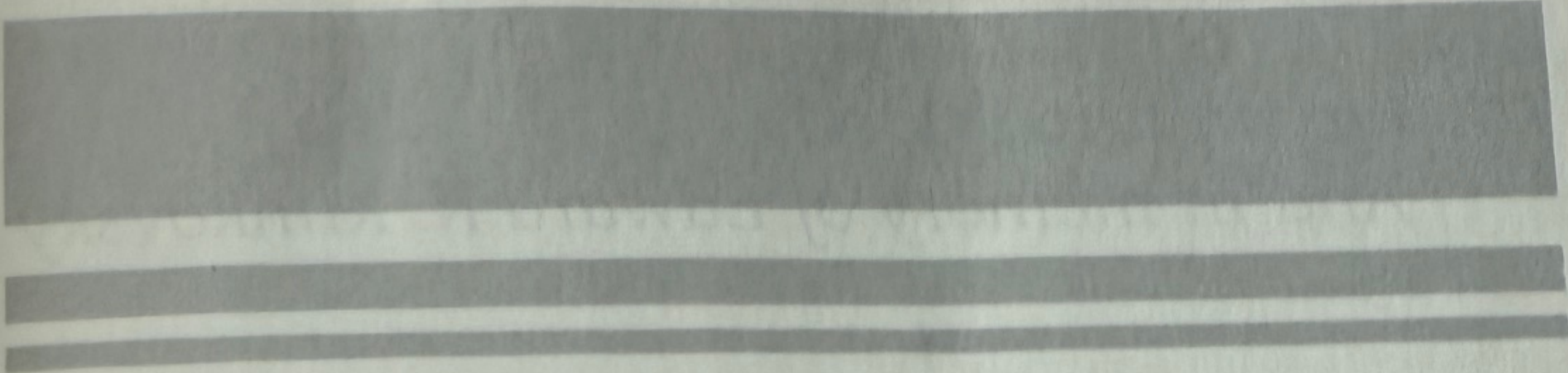




CMOS Analog Circuit Design

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*To Margaret and Candy
And in memory of Edward R. Klinkovsky*

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N is the total number of bits of the digital word and b_i is the i th bit coefficient and is either 0 or 1. Therefore, the output of a D/A converter can be expressed by combining Eqs. (1) and (2) to get

$$V_{\text{OUT}} = KV_{\text{REF}} \left[\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \dots + \frac{b_N}{2^N} \right] \quad (3)$$

or

$$V_{\text{OUT}} = KV_{\text{REF}} [b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_N 2^{-N}] \quad (4)$$

In many cases the digital word is synchronously clocked. In this case latches must be used to hold the word for conversion and a sample-and-hold circuit is needed at the output, as shown in Fig. 10.1-2(b). The sample-and-hold circuit consists of a circuit such as that shown in Fig. 10.1-3. The sample mode occurs when the switch is closed and the analog signal is sampled on a capacitor C_H . During the switch-open cycle or the hold mode,

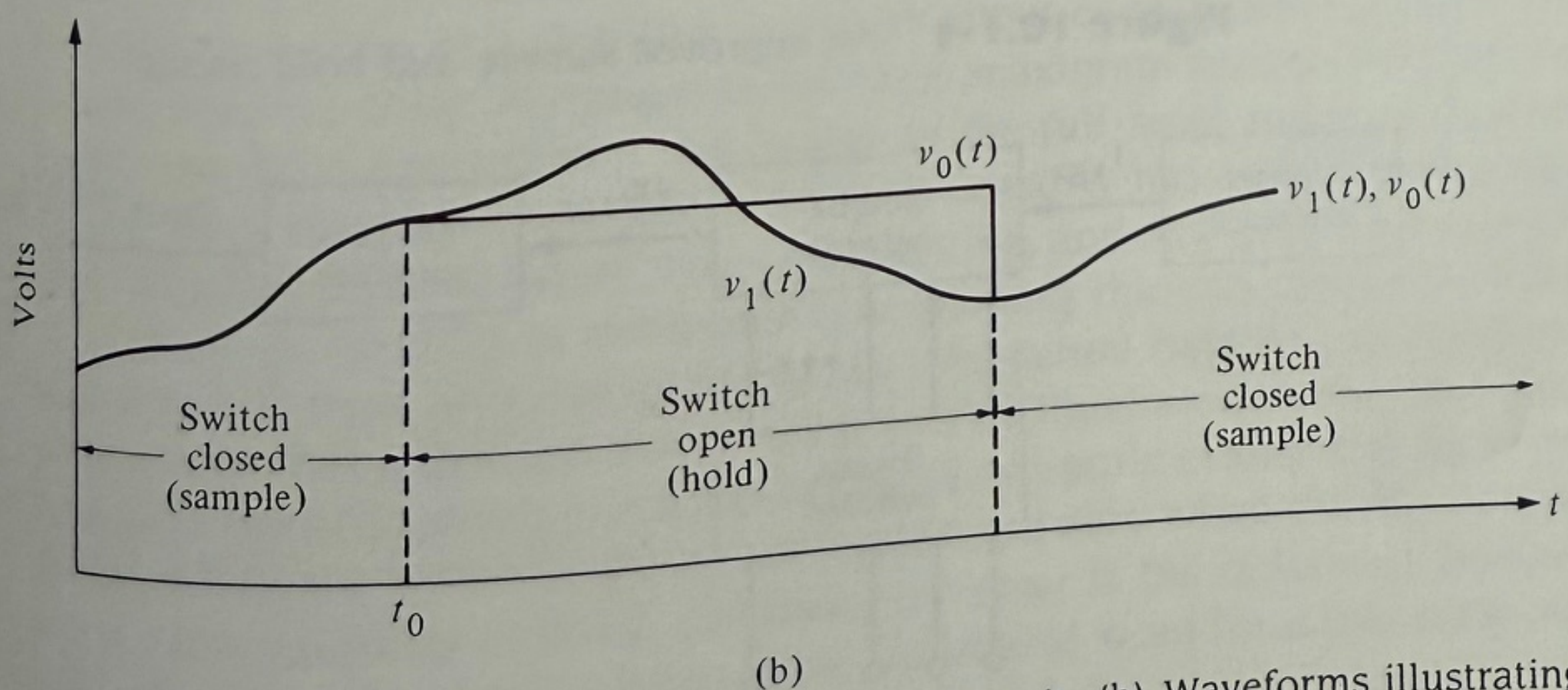
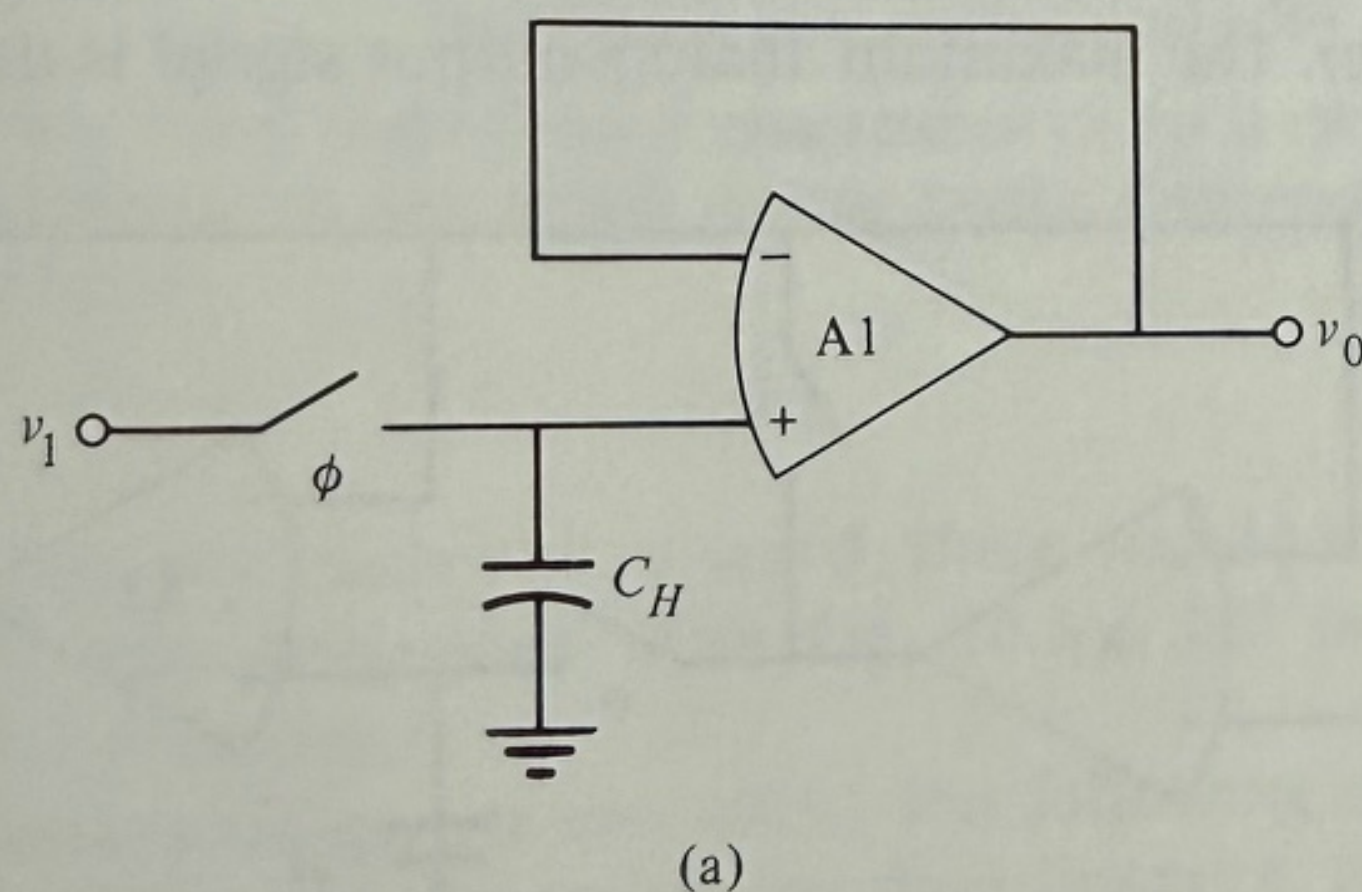


Figure 10.1-3 (a) Simple sample-and-hold circuit. (b) Waveforms illustrating the operation of the sample and hold.

the voltage at the time t_0 is available at the output. An alternate version of the sample-and-hold circuit with higher performance is shown in Fig. 10.1-4. The sample-and-hold circuit must be able to rapidly track changes in the input voltage in the sample mode and not discharge the capacitor when in the hold mode.

The basic form of the D/A converter is shown in Fig. 10.1-5. The various blocks include binary switches, a scaling network, and an output amplifier. The scaling network and binary switches operate on the externally-supplied reference voltage to create the digital word as either a voltage or charge signal and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of the conversion.

The characterization of the D/A converter is very important in understanding its design. The characteristics of the D/A converter can be divided into static and dynamic properties. The ideal static behavior of a D/A converter is shown in Fig. 10.1-6. The digital input word is on the horizontal axis, which consists of all possible combinations of that word. Fig. 10.1-6 is for a 3-bit digital word. The vertical scale is the analog output of the ideal D/A converter. The maximum analog-output signal is designated as the full

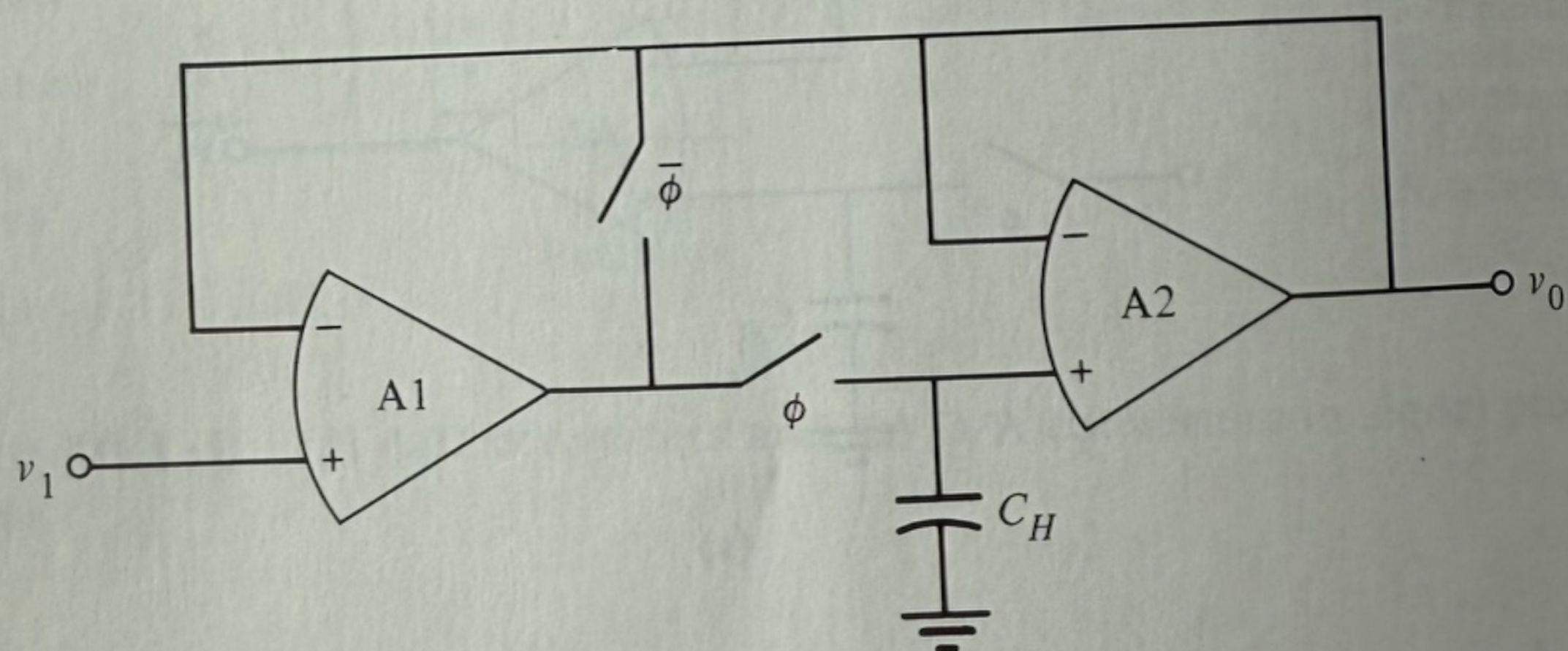


Figure 10.1-4 An improved sample-and-hold circuit.

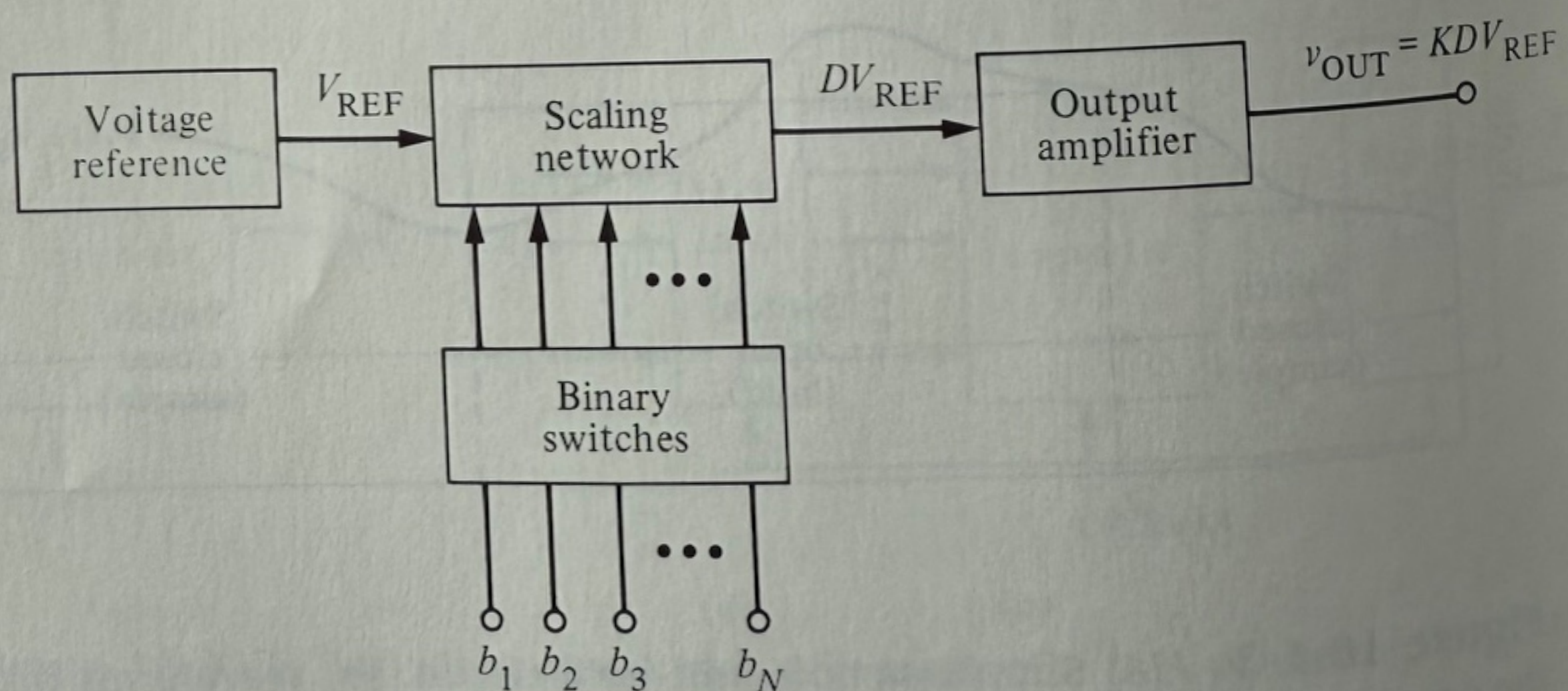


Figure 10.1-5 Block diagram of a D/A converter.