

GRAY
MEYER

Analysis and Design of
ANALOG INTEGRATED CIRCUITS

THIRD
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Paul R. Gray / Robert G. Meyer

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PAUL R. GRAY
ROBERT H. MEYER
University of California, Berkeley



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Illustration	Jaime Perea

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Preface

To Liz and Judy

In the 15 years since the publication of the first edition of this book, the field of analog integrated circuits has changed dramatically. The initial product was based in bipolar technology, but the advent of MOS analog integrated circuits in recent years has emerged as a serious contender to the original technologies. Although more expensive to fabricate, Bi-MOS allows the designer to use both bipolar and MOS devices to fully best advantage and also allows innovative combinations of the characteristics of both devices. In addition, BiCMOS can reduce the very important time to market, by allowing direct use of many existing cells in realizing a given analog circuit function. Analog circuits in BiCMOS can be combined on the same chip with dense, low-power CMOS logic and high-speed ECL digital circuits.

In this third edition, we have combined the consideration of MOS and bipolar circuits into a unified treatment that also includes MOS-bipolar combinations made possible by BiCMOS technology. It has become increasingly important for the analog circuit designer to have a thorough appreciation of the similarities and differences between MOS and bipolar devices, and to be able to design with either one where this is appropriate.

Since the SPICE computer analysis program is now readily available to most electrical engineering students and professionals, we have included extensive use of SPICE in this edition, particularly as an integral part of many examples in the problem sets. We have used computer analysis as it is most commonly employed in the engineering design process—both as a more accurate check on hand calculations, and also as a tool to examine complex circuit behavior beyond the scope of hand analysis. In the problem sets we have also included a number of open-ended design problems in order to expose the reader to real-world situations where a whole range of circuit solutions may be found to satisfy a given performance specification.

This book is intended to be useful both as a text for students and as a reference book for practicing engineers. For class use, there are numerous worked problems in each chapter, the problem sets at the end of each chapter illustrate the practical applications of the material in the text. Both authors have had extensive industrial experience in integrated-circuit (IC) design as well as in the teaching of courses on this subject, and this experience is reflected in the choice of text material and in the problem sets.

Although this book is concerned largely with the design of ICs, a considerable amount of material is also included on applications. In practice, these two subjects are very closely linked, and a knowledge of both is essential for designers and users. The latter comprise the larger group by far, and it has been our experience that a working knowledge of IC design is a great advantage to an IC user. This is particularly apparent when the user must choose from among a number of competing designs to satisfy a particular need. An understanding of the IC

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1.2 Depletion Region of a pn Junction

The properties of reverse-biased pn junctions have an important influence on the characteristics of many integrated-circuit components. For example, reverse-biased pn junctions exist between many integrated-circuit elements and the underlying substrate, and these junctions all contribute voltage-dependent parasitic capacitances. In addition, a number of important characteristics of active devices

to a short-circuit state by passing a large current through them in the reverse direction. In either case, the offset can be nulled when the devices are tested in wafer form, and the nulling does not introduce additional drift components since the collector resistances are all monolithic components of the same type. Since the resistors are binary weighted, the number of discrete steps into which the adjustment range is divided is proportional to 2^n where n is the number of fusible links in one collector. This is a powerful and low-cost technique for improving the input characteristics of monolithic precision operational amplifiers that can realize input offset voltages less than $50\text{ }\mu\text{V}$.

Layout and Device Matching Considerations. A basic objective in the design of precision circuits like the 725 is the minimization of the input offset voltage, which requires the minimization of the mismatch between the collector resistors and the input devices.

The accuracy with which two identical transistors or resistors can be matched has a first-order effect on the attainable performance in monolithic operational amplifiers as well as many other types of analog integrated circuits such as voltage regulators (Chapter 8), analog multipliers (Chapter 10), analog-digital and digital-analog converters, voltage comparators, and others. The observed random distribution of the mismatches between two supposedly identical resistors or transistors is primarily the result of two factors:

1. Variations in the location of the edges of the resistor or transistor resulting from the limited resolution of the photolithographic process itself. This causes emitter area mismatches in bipolar transistors and length/width ratio mismatches in resistors and FETs.
2. Variations in sheet resistance and junction depth of the implanted and diffused regions across the wafer resulting from nonuniform conditions during the predeposition and/or diffusion of the impurities. This causes the resistor sheet resistance and the transistor parameters to vary with distance across the die. Ion-implanted processes have significantly better control and uniformity than diffused processes.

In addition to these random phenomena, systematic mismatches can occur from a number of causes, including errors in drawing the original mask and thermal gradients on the die. These systematic errors, however, are easily detected since they reoccur on each die, and can thus be corrected. The random fluctuations represent the basic factor limiting the attainable matching accuracy.

Since the photolithographic resolution limits the attainable matching, it is clear that the important parameter is the size of the resistor or transistor being defined in relation to the resolution. If the resistor is made wider, then the same amount of edge location uncertainty should have proportionately less effect and the matching should improve. This is indeed observed; a graph of observed resistor matching as a function of resistor width is shown in Fig. 6.29. Similarly, the matching of I_S observed in bipolar transistors improves markedly as the emitter size is made larger, as illustrated by the graph of observed matching data shown in Fig. 6.30. The increase in die size and resulting cost generally limits the size of the

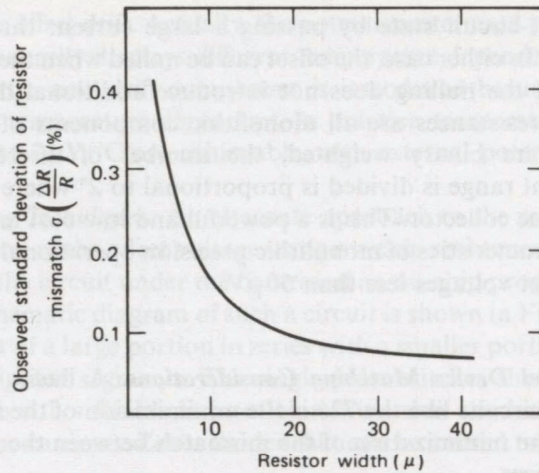


Figure 6.29 Experimentally observed standard deviation in the mismatch distribution of ion-implanted resistors with sheet resistance $250 \Omega/\square$ and $W/L = 0.1$.

devices that can be used, but in the case of the precision operational amplifier, the input transistors and resistors are generally made as large as practicable.

The second factor limiting the matching, process-related gradients across the die, can be partially alleviated by use of appropriate geometries that cause the device mismatch to be insensitive to certain types of process gradients. Such geometries are termed common centroid, and the simplest case is illustrated in Fig. 6.31. Here the transistors making up the pair are formed from cross-connected segments of a quad of transistors. In a geometric sense, the centroid of both

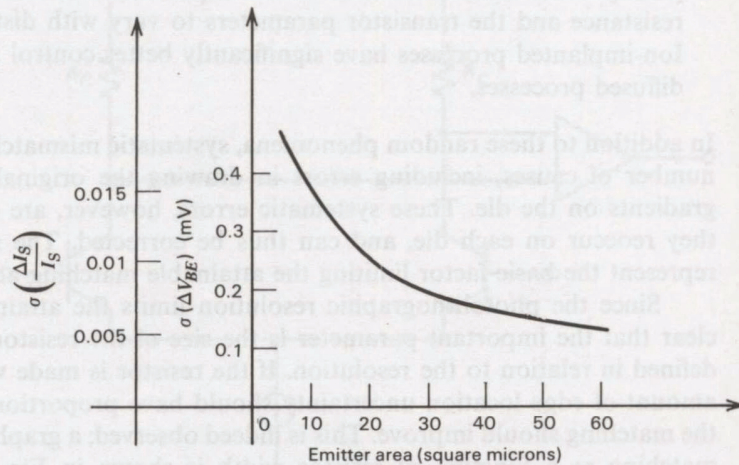


Figure 6.30 Observed standard deviation in the mismatch distribution of V_{BE} and I_S as a function of emitter area for ion-implanted bipolar transistors.

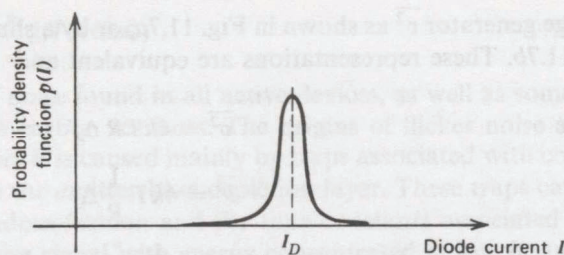


Figure 11.5 Probability density function for the diode current I . (Not to scale.)

noise signal is within these limits for 99.7 percent of the time. A brief description of the Gaussian distribution is given in Appendix A.3.1 in Chapter 3.

It is important to note that the distribution of noise in frequency as shown in Fig. 11.3 is due to the random nature of the hole and electron transitions across the pn junction. Consider the situation if all the carriers made transitions with uniform time separation. Since each carrier has a charge of 1.6×10^{-19} C, a 1-mA current would then consist of current pulses every 1.6×10^{-16} s. The Fourier analysis of such a waveform would give the spectrum of Fig. 11.6, which shows an average or dc value I_D and harmonics at multiples of $1/\Delta t$, where Δt is the period of the waveform and equals 1.6×10^{-16} s. Thus the first harmonic is at 6×10^6 GHz, which is far beyond the useful frequency of the device. There would be *no noise produced* in the normal frequency range of operation.

11.2.2 Thermal Noise^{1,3,5}

Thermal noise is generated by a completely different mechanism from shot noise. In conventional resistors it is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. Since this source of noise is due to the thermal motion of electrons, we expect that it is related to absolute temperature T . In fact thermal noise is *directly proportional* to T (unlike shot noise, which is *independent of* T) and, as T approaches zero, thermal noise also approaches zero.

In a resistor R , thermal noise can be shown to be represented by a series

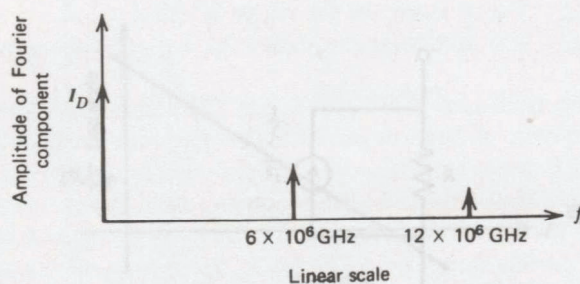


Figure 11.6 Shot-noise spectrum assuming uniform emission of carriers.

voltage generator $\overline{v^2}$ as shown in Fig. 11.7a, or by a shunt current generator $\overline{i^2}$ as in Fig. 11.7b. These representations are equivalent and

$$\overline{v^2} = 4kTR\Delta f \quad (11.4)$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \quad (11.5)$$

where k is Boltzmann's constant. At room temperature $4kT = 1.66 \times 10^{-20}$ V-C. Equations 11.4 and 11.5 show that the noise spectral density is again *independent* of frequency and, for thermal noise, this is true up to 10^{13} Hz. Thus thermal noise is another source of white noise. Note that the Norton equivalent of (11.5) can be derived from (11.4) as

$$\overline{i^2} = \frac{\overline{v^2}}{R^2} \quad (11.6)$$

A *useful number* to remember for thermal noise is that at room temperature (300°K), the thermal noise spectral density in a 1-k Ω resistor is $\overline{v^2}/\Delta f \simeq 16 \times 10^{-18}$ V²/Hz. This can be written in rms form as $v \simeq 4$ nV/ $\sqrt{\text{Hz}}$ where the form nV/ $\sqrt{\text{Hz}}$ is used to emphasize that the *rms noise voltage* varies as the *square root* of the bandwidth. Another useful equivalence is that the thermal noise-current generator of a 1-k Ω resistor at room temperature is the same as that of 50 μ A of direct current exhibiting shot noise.

Thermal noise as described above is a fundamental physical phenomenon and is present in *any* linear passive resistor. This includes conventional resistors and the radiation resistance of antennas, loudspeakers, and microphones. In the case of loudspeakers and microphones, the source of noise is the thermal motion of the air molecules. In the case of antennas, the source of noise is the black-body radiation of the object at which the antenna is directed. In all cases, (11.4) and (11.5) give the mean-square value of the noise.

The amplitude distribution of thermal noise is again Gaussian. Since both shot and thermal noise each have a flat frequency spectrum and a Gaussian amplitude distribution, they are indistinguishable once they are introduced into a circuit. The waveform of shot and thermal noise combined with a sinewave of equal power is shown in Fig. 11.21.

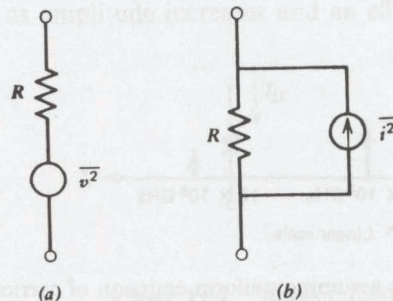


Figure 11.7 Alternative representations of thermal noise.