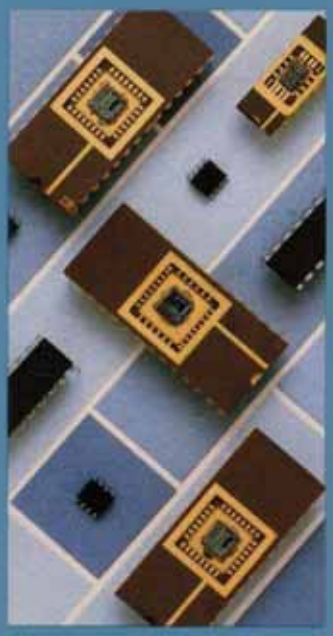
ANALOG DEVICES



LINEAR PRODUCTS DATABOOK

OPERATIONAL AMPLIFIERS
COMPARATORS
INSTRUMENTATION AMPLIFIERS
ISOLATION AMPLIFIERS
ANALOG MULTIPLIERS/DIVIDERS
LOG/ANTILOG AMPLIFIERS
RMS-TO-DC CONVERTERS
SPECIAL FUNCTION COMPONENTS
TEMPERATURE TRANSDUCERS
SIGNAL CONDITIONING COMPONENTS & SUBSYSTEMS
DIGITAL PANEL INSTRUMENTS
APPLICATION SPECIFIC ICS
POWER SUPPLIES
COMPONENT TEST SYSTEMS

TI 1057
TI v. ParkerVision
IPR2024-00936

1988 LINEAR PRODUCTS DATABOOK

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LINEAR PRODUCTS DATABOOK
April 1988

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Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.:
RE29,619, RE29,992, RE30,586, RE31,850, DES. 233,909, 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,793,563, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,268,759, 4,270,118, 4,268,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,427,973, 4,439,724, 4,460,891, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,511,413, 4,521,764, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,678,936, 4,684,922, 4,685,200, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883

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Sweden:
7603320-8

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General Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes – and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SO, LCC, PLCC) and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. More than twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high-performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the 1986 supplement to our 1984 *Data Acquisition Databook*, more than 120 significant new products have been introduced; they run the gamut from brand new product categories and technologies to new standard products (with improvements in price, performance, or design) to augmented second-source products. They are all classified and summarized in these Volumes, along with existing products that are desirable for use in new designs.

Among the landmark new linear products are high-accuracy op amps – such as the ultralow-offset-and-drift AD707, wideband transconductance op amps – both monolithic (AD5539) and hybrid (AD9611) and the 60-femtoampere AD549 electrometer – using ADI's patented Top-Gate FET process. Other new high-performance monolithic devices include the fast, accurate AD9686 comparator, the AD625 software-programmable-gain amplifier, the innovative AD693 4-to-20mA sensor transmitter, the AD834 ultimate analog multiplier, plus the AD9521 r-f log devices and the AD890/891 data-recovery chip set. Also of note are the 5B Series of compact modular isolated signal-conditioners, the AD210 high-performance isolator and the 1B series of DIP-packaged signal conditioners – all of which employ automated surface mount assembly for compactness, low cost and high reliability.

THE 1988 LINEAR PRODUCTS DATABOOK

This Volume provides complete technical data on Analog Devices "linear" products – designed to process, condition and otherwise operate on *analog signals* with *analog results*. One of a set of three volumes, it is accompanied by the *DSP Products Databook*, dedicated to products for high-performance digital signal-processing (i.e., *digital-to-digital*) and the *Conversion Products Databook*, which covers products involved in spanning the interface *between analog and digital*.

The product data in this book is intended primarily for the majority of users who are concerned with new designs. For this reason, those existing and available products that offer little if any unique advantage over newer products in future designs are included in the Index and their data sheets are available from us separately – but they aren't published in this book.

This book includes:

- Comprehensive data sheets on more than 160 significant product families;
- Orientation material and selection guides for rapid product finding;
- A representative list of available Analog Devices technical publications on real-world analog and digital signal-processing;
- Worldwide Service Directory; and
- Product Index to all three volumes.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for precision measurement and control. Besides tutorial material and comprehensive data sheets, including a large amount in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control and test. *DSPatch* is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs, we also publish several short-form catalogs on specific product families. You will find Technical Publications described on pages 17–6 and 17–7 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory, as of the publication date, appears on pages 17-8 and 17-9 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 for ICs in the U.S. and Ireland and MIL-STD-1772 for hybrids. More than 20 of our products – both proprietary and second-source – have qualified for JAN part numbers; others are in the process. A larger number of products – including many of the newer ones just starting the JAN qualification process – are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts (the 1987 issue contains data on nearly 150 available product families). A newsletter, *Analog Briefings*, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, they are often suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 17-4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 17-5 you will find a guide to substitutions (where possible) for products no longer available.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

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Selection Guide
Operational Amplifiers

HIGH SPEED AMPLIFIERS

Model	GBWP MHz	Slew Rate V/μs	Settling Time ns to %		Load Current mA	Supply Current mA	Offset Voltage mV	Minimum Stable Gain	Page	Notes
AD5539	1400	600	12	1	20	14	3	3	2 – 183	
AD849	750	300	65	0.1	35	5	0.5	25	2 – 181	
AD846	450	450	110	0.01	50	5	0.075	1	2 – 165	Transimpedance amplifier
AD840	400	400	110	0.01	50	14	0.5	10	2 – 157	
AD9611	280	2100	13	0.1	50	25	0.5	1	2 – 207	Transimpedance amplifier
AD848	175	300	65	0.1	35	5	0.5	5	2 – 179	
AD9610	100	3500	20	0.1	50	25	0.5	1	2 – 199	Transimpedance amplifier
HOS-050	100	300	80	0.1	100	20	15	1	2 – 245	
HOS-060	100	300	80	0.1	100	20	1	1	2 – 251	
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AD841	40	300	110	0.01	50	16	1	1	2 – 159	
AD847	50	300	65	0.1	35	5	0.5	1	2 – 177	
AD380	40	330	250	0.01	60	12	1	1	2 – 15	FET input, external compensation
AD507	35	35	900	0.1	20	4	3	10	2 – 27	
AD509	20	120	500	0.1	–	6	8	3	2 – 31	
AD845	16	100	300	0.01	50	10	0.25	1	2 – 163	FET input
AD744	13	75	500	0.01	10	3.5	0.25	1	2 – 137	FET input, dual available
AD381	5	30	750	0.1	10	5	1	1	2 – 21	FET input
AD382	5	30	750	0.1	50	6	1	1	2 – 21	FET input

UNITY GAIN BUFFERS

Model	−3dB Bandwidth MHz	Slew Rate V/μs	Load Current mA	Supply Current mA	Offset Voltage mV	Page
HOS-200	200	1600	100	15	10	2 – 257
HOS-100	125	1500	100	15	5	2 – 255
ADLH0033	100	1500	100	20	5	2 – 219

PRECISION AMPLIFIERS
(low V_{OS}, low drift, high dc gain)

Model	Offset Voltage μV	Offset Drift μV/°C	Bias Current nA	Open-Loop Gain kV/V	Slew Rate V/μs	GBWP MHz	Page	Notes
AD707	15	0.1	1	13000	0.3	0.9	2 – 103	Dual available
AD OP-07	25	0.6	2	3000	0.17	0.6	2 – 223	
AD OP-37	25	0.6	40	1000	17	63	2 – 237	Decompensated AD OP-27
AD OP-27	25	0.6	40	1000	2.8	8	2 – 229	Low noise
AD517	50	1.3	1	1000	0.1	–	2 – 41	
AD821	250	3	0.01	300	3	1.3	2 – 153	Single-supply, low power
AD548	250	2	0.01	300	1	1	2 – 55	Low power, dual available
AD547	250	1	0.025	250	3	1	2 – 47	Dual available

LOW INPUT CURRENT AMPLIFIERS

Model	Input Current pA	Offset Voltage mV	Offset Drift µV/°C	Open-Loop Gain kV/V	Slew Rate V/µs	GBWP MHz	Page	Notes
AD549	0.06	0.25	5	300	3	1	2 – 63	
AD515A	0.075	1	15	40	0.3	0.35	2 – 35	
AD548	10	0.25	2	300	1	1	2 – 55	Dual available

LOW COST, GENERAL PURPOSE OPERATIONAL AMPLIFIERS

Model	Offset Voltage mV	Offset Drift µV/°C	Bias Current nA	Open-Loop Gain kV/V	Slew Rate V/µs	GBWP MHz	Settling Time to 0.01%	Page	Notes
AD711	2.	20	0.05	200	20	4	1µs	2 – 107	Dual, quad available
AD548	2	20	0.025	200	1	1	8µs	2 – 55	Dual available
AD OP-07	0.15	2.5	12	1000	0.17	0.6	–	2 – 223	
AD544	2	20	0.05	30	13	2	3µs	2 – 47	Dual available
AD542	2	20	0.05	100	3	1	–	2 – 47	Dual available
AD741	6	–	500	20	0.5	1	–	2 – 133	

DUAL OPERATIONAL AMPLIFIERS

Model	Offset Voltage mV	Offset Drift µV/°C	Bias Current nA	Open Loop Gain kV/V	Slew Rate V/µs	GBWP MHz	Settling Time to 0.01%	Page	Type
AD642	0.5	5	0.035	250	3	1	–	2 – 75	Dual AD542
AD644	0.5	5	0.035	50	13	2	–	2 – 81	Dual AD544
AD647	0.25	1	0.025	250	3	1	–	2 – 87	Dual AD547
AD648	0.25	2	0.01	300	1	1	–	2 – 93	Dual AD548
AD708	0.03	0.3	1	13000	0.3	0.9	–	2 – 105	Dual AD707
AD712	0.25	3	0.035	200	20	4	1µs	2 – 119	Dual AD711
AD746	0.25	3	0.06	200	60	13	500ns	2 – 149	Dual AD744

QUAD OPERATIONAL AMPLIFIERS

Model	Offset Voltage mV	Offset Drift µV/°C	Bias Current nA	Open-Loop Gain kV/V	Slew Rate V/µs	GBWP MHz	Settling Time to 0.01%	Page	Notes
AD713	0.25	3	0.035	200	20	4	1µs	2 – 131	Quad AD711

Orientation
Operational Amplifiers

The amplifiers listed in this volume are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more general requirements in electronic circuits. The technical data included here* cover the properties of more than 40 op amp families, comprising about 100 distinct types. Some are general purpose; others provide near optimum performance for specific classes of application.

They differ in a variety of ways, for example, circuit technology, circuit architecture, package type and contents, input properties, output properties, operating temperature range and in terms of the many performance specifications. Most are monolithic ICs, including precision and high-speed dual devices; some are hybrid ICs.

The IC and hybrid amplifiers catalogued in this volume are available in a broad choice of packaging styles, temperature ranges, and performance grades. If your application calls for versions of these products that have been processed in accordance with MIL-STD-883, a wealth of relevant information can be found in the latest edition of the *Military Products Databook*, available free upon request from Analog Devices.

BACKGROUND

The operational amplifier is today the most widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control) and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 2-14 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. Analog Devices' op-amp data sheets are an excellent source of pertinent information.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To make a proper choice of an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.*
   Signal levels, closed-loop gain, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.
2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.*
   Two manufacturers may have comparable published specifications, but they may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks" and linear circuit books as well as in application notes and data sheets.
2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps and establish acceptable ranges of parameters and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high frequency performance and transient behavior of the op amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.
3. The designer must then relate acceptable performance of the op amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows this discussion.

***In addition to the products listed here, which are recommended for new designs, a number of older products are still available (see page 17–4); data sheets are available upon request.**

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. For example, an adjustable-gain wideband application may call for a *transimpedance* op amp to keep bandwidth independent of gain setting.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical and environmenal requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the dc discussion below. The reader is then returned to an expanded discussion of gain bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

1. If dc information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and/or output and all of the "drift" specifications may usually be ignored, and
2. Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where dc information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain bandwidth of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open-loop gain over closed-loop gain, and is responsible for the diminishing error due to fluctuations in the open-loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1,000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Most operational amplifiers are voltage-to-voltage amplifiers. However, for wide bandwidth applications, it is often useful to consider applying a class of current-to-voltage amplifiers called *transimpedance amplifiers*. They are characterized by *transresistance* ($\Delta V_o/\Delta I_i$) instead of gain ($\Delta V_o/\Delta V_i$). Unlike voltage amplifiers, with their high input impedance, transimpedance amplifiers have *low* (ideally zero) input impedance in order to minimize the gain-error voltage developed by their input current. Such amplifiers tend to be characterized by high slewing rates and high closed-loop bandwidth. In contrast to the *constant gain* × *bandwidth* of most voltage amplifiers, the closed-loop bandwidth of a transimpedance amplifier is essentially independent of closed-loop gain – as long as the feedback resistance is kept constant when the gain is adjusted.

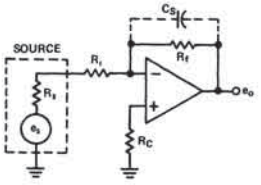
Offset and Drift Considerations

In the majority of op amp applications, final selection is determined by the dc offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around the inverting and noninverting circuits of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i, and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback), and in this case input impedance is approximately equal to the common-mode impedance of the amplifier R_{CM}.
2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a dc input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

   When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b) and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.



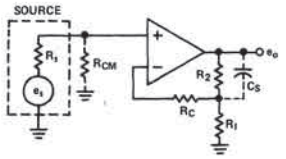
$$e_o = -\frac{R_f}{R_i}\left[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i}_{\text{Input Drift Error} = V_d}\right] \quad \text{For } R_C = 0 \text{ and } R_s \ll R_i$$

$$e_o = -\frac{R_f}{R_i}\left[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\frac{R_f + R_i}{R_f} + i_d R_i}_{\text{Input Drift Error} = V_d}\right] \quad \text{For } R_C = R_i R_f/(R_i + R_f) \text{ and } R_s \ll R_i$$

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1a. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_s}_{\text{Drift Error} = V_d}\right] \text{ for } R_C = 0$$

$$e_o = \frac{R_2 + R_i}{R_i}\left[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_d R_s}_{\text{Drift Error} = V_d}\right] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1b. Noninverting Configuration

For example, in the case of the inverting circuit, an offset error voltage, $i_b R_i$, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

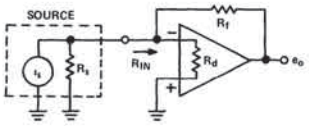
Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications where common-mode errors may rule out this circuit configuration. Transimpedance amplifiers in the noninverting configuration have high dynamic input impedance, but they must be driven from a source that can furnish the input current. This rules out the possibility of unloading some high impedance sources but still permits a single amplifier to be used for noninverting gains (as always, it is helpful to consult the data sheet).

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from $+25°C$ need be considered. For example, over the range of $-25°C$ to $+85°C$, the maximum temperature excursion (ΔT) from $+25°C$ would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2a. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2b.

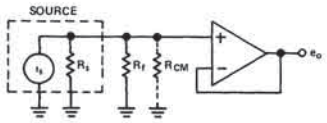


$$e_o = -R_f\left[\underbrace{i_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b}_{\text{Drift error} = I\epsilon}\right]$$

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d} \quad \% \text{ Drift Error} = \frac{100\, I\epsilon}{i_s}$$

Figure 2a. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

Input Impedance $R_{IN} \approx R_f$

$$\% \text{ Drift Error} = \frac{100V_d}{R_f i_s}$$

Figure 2b. Voltage Amplifier with Sampling Resistor

This approach has several disadvantages as compared to the circuit of Figure 2a. First, the noninverting amplifier introduces common-mode errors which do not occur for Figure 2a. Second, an ideal current meter would have zero impedance whereas R_f in Figure 2b may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2a circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open-loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for dc and audio-frequency-range applications. However, amplifiers having unity-gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μs, in general, require special design techniques. Amplifiers with wideband, fast response characteristics have been listed in the Wide Bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1a, if R_f were one megohm, and stray capacitance, C_S, were one picofarad, then the closed-loop bandwidth would be limited to 160kHz ($1/(2\pi R_f C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged, which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_S$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1b) is that input impedance, being determined by potentiometric feedback, is independent of the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_S will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common-mode rejection error (with frequency) introduced by the noninverter.

For greater emphasis, wideband applications can be separated into categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

2

STEADY STATE APPLICATIONS

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is dc coupling required?* If dc information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output dc offset. Your only concern here is that dc offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for ac signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at dc as shown in Figure 3. The gain of this kind of circuit can be small at dc but large at high frequencies.

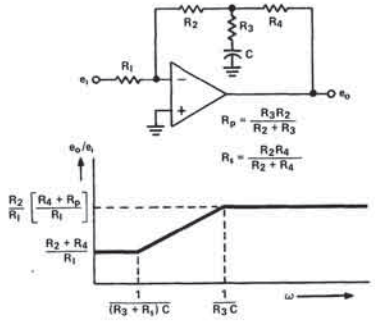


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed-loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. For V/V amplifiers, to a first approximation the intersection of the open- and closed-loop gain curves in Figure 4 gives the closed loop bandwidth, f_{c1} (– 3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain. For transimpedance amplifiers, f_{c1} changes little over a wide range of gain as set by the choice of R_1.
3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed-loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open- to closed-loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed-loop characteristic of a feedback (V/V) amplifier that the loop gain ($A\beta$) is the

determining factor in performance. Some of the more notable examples of this point are as follows:

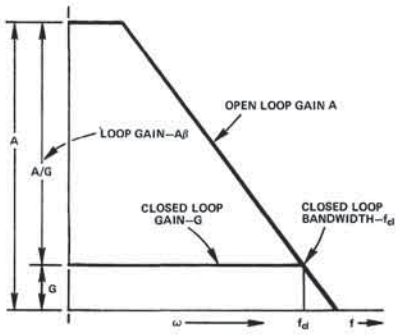


Figure 4. Closed Loop Bandwidth and Loop Gain

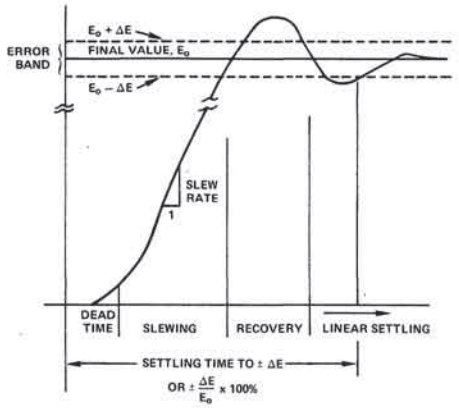


Figure 5. Typical Settling Time Characteristics

a. Closed-loop gain stability $= \Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1+A\beta)]$ where $\Delta A/A$ is the open-loop gain stability, usually about 1%/°C.

b. Closed-loop output impedance $= Z_{ocl} = Z_o/(1+A\beta)$, where Z_o is the open-loop output impedance, usually 200 to 5,000 ohms.

c. Closed-loop nonlinearity $= L_{cl} = L_{ol}/(1+A\beta)$, where L_{ol} is the open-loop linearity error, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications, and this is readily achievable at dc and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?*
You should examine your expected output waveform and select an amplifier whose slewing rate, with the expected capacitive output load, exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions, you will get distortion and unexpected dc offsets at the output of the amplifier.

For some monolithic amplifier designs intended for high-gain and wide-bandwidth applications, their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance at lower closed-loop gains. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated V/V op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

TRANSIENT APPLICATIONS

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

The time and frequency response of a linear, bilateral network or amplifier are related by well know mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed-loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed-loop parameter, it cannot be readily predicted from the open-loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels and no capacitive loading (unless otherwise indicated). A full-scale step input is used to determine settling time and the step is generally unipolar – i.e., from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full-scale step transition.

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

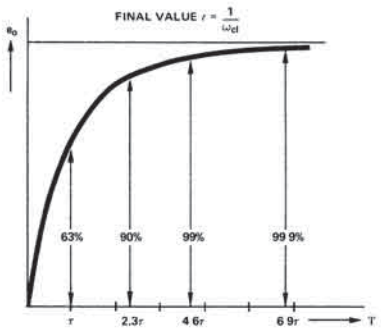


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF and digital noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will greatly reduce noise pickup.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise," is generated in the resistive component of any impedance and has a value:

$$e_n = \sqrt{4kTBR}$$

where e_n = the rms value of the noise voltage
k = Boltzman's Constant (1.38×10^{23} joules/K)
T = absolute temperature of the resistance, K
B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the thermal noise equation may appear unwieldy, for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

1. Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100k\Omega}\,(BW)}\right)$$

2. To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.
3. The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

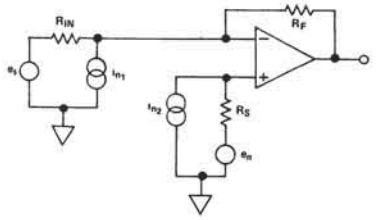
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be less than 5%.

4. Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7a illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a rms fashion.

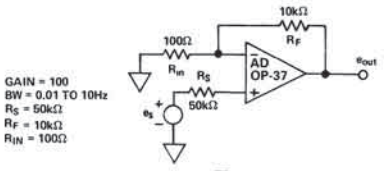


COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4kTBR_{IN}}\,(R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4kTBR_S}\,(R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4kTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1}R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2}R_S)\,(R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\,(R_F/R_{IN}+1)$

TOTAL NOISE = $\sqrt{(e_{R_{IN}}G)^2 + [e_{R_S}(G+1)]^2 + e^2_{R_F} + [(i_{n_1}R_F)^2] + [(i_{n_2}R_S)(G+1)]^2 + [e_n(G+1)]^2}$

Figure 7a. Noise Components

Figure 7b illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, a low noise type amplifier (AD OP-37) is being used with a 50kΩ source impedance. The two major noise sources, in addition to the AD OP-37's input voltage noise of 0.18μV p-p, are the Johnson noise (59μV p-p) and current noise (83pA p-p).



1) RESISTOR NOISE $R_F \rightarrow 13nV/\sqrt{Hz}$
$R_{IN} \rightarrow (1\ 3nV/\sqrt{Hz}$
$R_S \rightarrow (28nV/\sqrt{Hz})\ 101 = 2\ 8\mu V/\sqrt{Hz}$
TOTAL RESISTOR NOISE IN 10Hz BW =
$(2\ 8\mu V/\sqrt{Hz})\ (\sqrt{10Hz})\ 6.6\mu V$ p-p/μV rms = $59\mu V$ p-p

2) AMPLIFIER CURRENT NOISE (83pA p-p) (50k) (101) = $422\mu V$ (R_S)
(83pA p-p) (10k) = $0\ 8\mu V$ (R_F)

3) AMPLIFIER VOLTAGE NOISE (0 18V p-p) (101) = $18\ 2\mu V$ p-p

TOTAL OUTPUT NOISE = $\sqrt{(422)^2 + (59)^2 + (18\ 2)^2 + (0\ 18)^2}$ = $426\mu V$ p-p

Figure 7b. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature: Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD549L). Also popular is the "extended" range, −55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, −25°C to +85°C, designated by A, B. Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD741L).

SELECTION GUIDES

Seven Selection Guides classify operational amplifiers within these categories:

High-Speed Amplifiers
Unity-Gain Buffers
Precision Amplifiers (low V_{OS}, low drift, high dc gain)
Low-Input-Current Amplifiers
Low-Cost, General-Purpose Op Amps
Dual Op Amps
Quad Op Amps

The choice of category depends on which class of specifications is most critical. Within these categories, the selection guides provide comparisons of salient specifications.

These selection areas are pretty broad; they include various criteria, not all of which are central to the application. For example, if one is seeking a high-input-impedance amplifier for an ac application, voltage offset and drift may be far less critical than bias current, and both of these may be unimportant compared to bandwidth.

With the hope that it will be found useful, the following interpretive list identifies the best device choices in a variety of categories:

(At the extremes of performance are the *fastest* op amps and the *highest-precision* op amps.)

The *fastest* op amps include those having

- the highest *slewing rates*, – the hybrid AD9610 (3,500V/μs) and AD9611 (2,100V/μs), and the monolithic AD5539 (600V/μs)
- the lowest *settling time* – the monolithic CB (complementary bipolar) AD840/841/842/846 (110ns to ±0.01%), the hybrid AD9610 and AD9611 (20ns and 13ns to 0.1%) and (again) the AD5539 (12ns to 1.0%)
- the highest *gain-bandwidth* – the AD5539 (1,400MHz) and the CB AD849 (725MHz) and AD840 (400MHz)

High-speed op amps are characterized by high slewing rates, fast settling time and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data in buffers, D/A converters, and multiplexer circuits; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimum distortion since the large-signal bandwidth is closely related to the slewing rate.

ICs using the proprietary Analog Devices CB (complementary bipolar) process contain wideband PNP and NPN transistors that have similar characteristics – without the use of dielectric isolation. Since poor frequency response of lateral PNPs is the source of the bandwidth limitation in conventional linear bipolar processes, CB devices can have much faster response.

The *highest-precision* monolithic op amp families include those having

- the grades with the lowest *untrimmed offset voltage*– the AD707 (15μV) and AD OP-07/27/37 (25μV)
- the lowest *bias current* – the revolutionary *electrometer* op amp using top-gate-FET inputs, the AD549 (60 femtoamperes)
- the *lowest drift* – the AD707 (100nV/°C)
- the *highest open-loop gain* (hence highest accuracy as an integrator and high-gain amplifier) – again the AD707! (13×10^6V/V) and the CB FET-input AD821 (3×10^6V/V – also capable of single-supply operation)
- the highest *common-mode rejection* – once again the AD707 (130dB), followed by the AD OP-27/37 (114dB) and the AD OP-07 (110dB)

Precision op amps (in this list) include those emphasizing

- *Low bias current and high input impedance.* These types use the inherently high input impedance and low leakage current of junction field-effect transistors (FETs) to deal with configurations that measure low currents or involve high resistance values. Applications range from general

purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers such as photomultipliers, flame detectors, pH cells and radiation detectors.

- *High accuracy* through low offset and drift voltage, low voltage noise, high open-loop gain, and high common-mode rejection (CMR). Such types are used for high-accuracy instrumentation, low-level transducer circuitry, precision voltage comparison, and impedance buffering.

  All FET-input op amps from Analog Devices are conservatively manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to *either* input (some manufacturers call "bias current" the *average* of the two input currents).

For applications needing high, but not extreme, performance or *where high speed and high precision must be combined*, there are a number of device families to be considered. For example,

- the complementary-bipolar AD846 family *combines low offset voltage* (200μV) *with high slewing rate* (400V/μs)
- the AD744 BiFET family *combines low input bias current* (50pA) *with low settling time* (500ns to 0.01%)
- the AD OP-37 family *combines low drift* (600nV/°C) *with wide gain bandwidth* (63MHz)
- the hybrid AD381/382 combine 50pA bias current with 0.75μs settling time (to 0.1%) and 50mA output-current range

Fast amplifiers, which often boast output current ranges of 50mA or 100mA, include families with

- *high slewing rate* – the CB monolithic AD846 (400V/μs) and AD840/841/842 (400/300/375V/μs), and the hybrid ADLH0032 (500V/μs), AD380 (330V/μs), and HOS-060 (300V/μs)
- *low settling time* – the monolithic AD847/848/849 (65ns to 0.1%) and hybrid HOS-050 (80ns to 0.1%, 200ns to 0.01%), and the AD845 and AD744 families (300ns and 500ns to 0.01%)
- *wide gain-bandwidth* – the monolithic AD848 (250MHz) and the hybrid AD9611 (280MHz) and HOS-050/060 (100MHz)

High-precision monolithic amplifier families start with lower grades of the highest-precision families; beyond this, they include the

- *low-drift* AD OP-07/27/37 families (600nV/°C)
- *high-gain* AD OP-07 (3×10^6) and AD OP-27/37 (1×10^6)
- *high-CMR* AD821 (90dB); low-V_{os} AD846 (200μV) and a
- wide selection of low-bias-current FET-input op amps – the AD821 and AD548 (10pA), and the AD711 (25pA)

Many of these devices are duplicated in a single package; for example,

- the AD712 is a dual AD711
- the AD746 is a dual AD744
- the AD648 is a dual AD548
- the AD708 is a dual AD707
- the AD713 is a *quad* version of the AD711

Also included in this section are *buffers*, wideband amplifiers having slightly less than unity gain, low output impedance and high output-current availability (100mA). Although they can stand alone, a more frequent use is inside-the-loop as a "booster" amplifier to magnify the output power capability of any op amp or reduce the dynamic output impedance without losing precision. A typical example is the HOS-100, which can follow slewing rates of up to 1,500V/μs with a full-power frequency of 125MHz and deliver voltages up to ±12V and currents up to ±100mA.

2

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage

Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, under overload conditions or between applications, such as voltage comparators, the voltage between the inputs can be large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is usually expressed logarithmically: CMR (in dB) = $20 \log_{10}$ (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified but decrease and become less in the neighborhood of large CMV. Published CMR specifications for op amps pertain to low-frequency voltages, unless specified otherwise: CMR decreases with frequency.

Common-Mode Voltage, Maximum

For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connections.

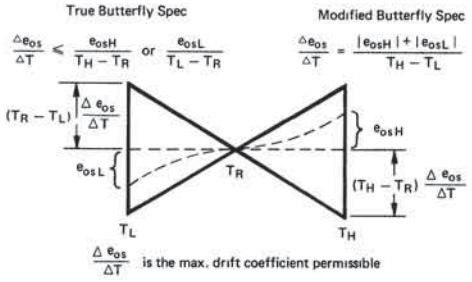
Drift vs. Supply

Offset voltage, bias current and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature

Offset voltage, bias current and difference current all change, or "drift," from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature range); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drift in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").



The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time

Offset voltage, bias current and difference current change with time as components age. It is important to realize that drift with time is random and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift might be quoted at 15μV/month, whereas cumulative drift might not exceed 50μV in a year. A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response

The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a predetermined distortion level. There is no industrywide accepted value for the distortion level which determines the full-linear-response limitation, but unless otherwise noted, we use 3% as a a maximum acceptable limit.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more serious effect (often overlooked) is an effect equivalent to dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average*.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature*. (Some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" specs used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. Uncompensated input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated internally at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal impedance loads at both inputs.

Input Impedance

Differential input impedance of voltage-input op amps is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry).

However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the noninverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. When evaluating noise performance, bandwidth or period must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise," resistor noise or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some amplifiers types, spectral-density plots or "spot noise," at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain
Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response*.

For *transimpedance amplifiers*, since the input is a current and the output is a voltage, the "gain" is expressed in ohms ($R = V/I$). Because small changes in current cause large voltage changes, the transimpedance can be quite large – e.g., 100MΩ for the AD846. As long as the amplifier's internal input impedance is very low, errors in closed-loop circuitry depend principally on the ratio, R_F/R_T, relative to unity – where R_F is the feedback resistance and R_T is the transimpedance. It will be recalled that, in V/V op amps, the increase in error depends mainly on $R_F/(AR_I)$, where A is the open-loop gain and R_I is the resistance of the external input resistor. The significant difference is that, as gain or transresistance decreases with increasing frequency, the error in transimpedance-amplifier circuits is independent of R_I; hence closed-loop gain can be increased by reducing R_I without substantially affecting bandwidth.

Overload Recovery
Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output
Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time
Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate limited overload (if it occurs) and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate
The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response
Unity-gain small-signal response is the frequency at which the open-loop gain (or its projection on a Bodé plot) falls to 1V/V, or 0dB under a specified compensation condition. For amplifiers having 6 dB-per-octave rolloff, this frequency is also called

unity-gain bandwidth; for such amplifiers, the *gain-bandwidth product* is essentially constant. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification.

For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and noninverting configurations. However, if feed-forward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

For amplifiers having 6 dB-per-octave rolloff, this frequency is also called *unity-gain bandwidth;* for such amplifiers, the *gain-bandwidth product* is essentially constant.

A BRIEF BIBLIOGRAPHY ON OP AMPS

BOOKS (Not available from Analog Devices except where noted)

A Designer's Guide to: Innovative Linear Circuits, by Jim Williams, Newton, MA, Cahners, 1985

Analog Signal Processing and Instrumentation, by Arie F. Arbel, Cambridge (UK), Cambridge University Press, 1980

Bipolar and MOS Analog Integrated Circuit Design, by Alan B. Greben, New York, Wiley-Interscience, 1984

Electronics with Digital and Analog Integrated Circuits, by Richard J. Higgins, Englewood Cliffs, NJ, Prentice Hall, Inc., 1983

IC Op-Amp Cookbook, by Walter Jung, Howard Sams & Co., Third Edition, 1986, down-to-earth and practical paperback

Nonlinear Circuits Handbook, edited by D.H. Sheingold, 1976. $5.95. Analog Devices, Box 796, Norwood, MA 02062

Operational Amplifier Circuits, Theory and Applications, by E.J. Kennedy, New York, Holt, Rinehart and Winston, Inc., 1988

Operational Amplifiers and Linear ICs, by R.F. Coughlin and F.F. Driscoll, Prentice-Hall, Third Edition, 1987. Practical textbook

Operational Amplifiers, Theory and Practice, by J.K. Roberge, J. Wiley & Sons, 1975. Authoritative book on op amp principles and circuitry: contains extensive material on compensation to optimize dynamic performance

Transducer Interfacing Handbook, edited by D.H. Sheingold, 1980. $14.50. Analog Devices, Box 796, Norwood, MA 02062

ARTICLES AND APPLICATION NOTES (Available upon request; ask for specific issue of Analog Dialogue)

"Amplifier Noise Basics Revisited," *Analog Dialogue* 18-1, 1984

"Analog Signal Handling for High Speed and Accuracy," by A.P. Brokaw, *Analog Dialogue* 11-2

"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A.P. Brokaw, Application Note

"Applications of High-Performance BiFET Op Amps," Application Note

"Avoiding Passive-Component Pitfalls," *Analog Dialogue* 17-2, 1983

"Current Inverter with Wide Dynamic Range," by Barrie Gilbert, *Analog Dialogue* 9-1, 1975

"How to Select Operational Amplifiers," Application Note

"How to Test Operational Amplifier Parameters," Application Note

"Laser-Trimming on the Wafer, A Powerful New Tool for ICs," by R. Wagner, *Analog Dialogue* 9-3, 1975

"Shielding and Guarding," by Alan Rich, *Analog Dialogue* 17-1, 1983

"Simple Rules for Choosing Resistor Values in Adder-Subtractor Circuits," by D. Sheingold, *Analog Dialogue* 10-1, 1976

"Understanding Interference-Type Noise," by Alan Rich, *Analog Dialogue* 16-3, 1982

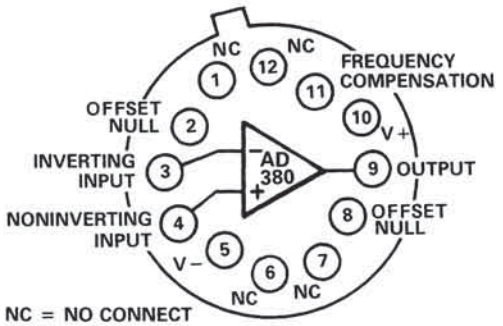
ANALOG DEVICES

Wideband, Fast-Settling FET-Input Op Amp

AD380

FEATURES
High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE OPTION[4]				
TO-8 Style	H-12A	*	*	*

NOTES
[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled
[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.
[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.
[4]See Section 16 for package outline information
*Specifications same as AD380JH
**Specifications same as AD380KH.
Specifications subject to change without notice.

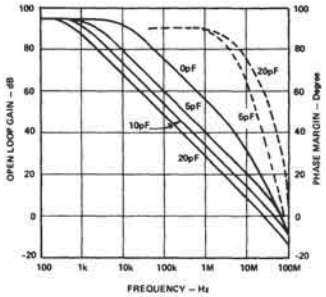


Figure 1. Open Loop Frequency Response

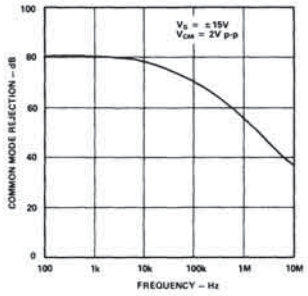


Figure 2. CMRR vs. Frequency

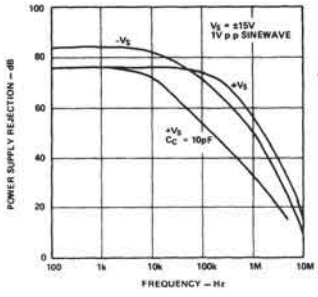


Figure 3. PSRR vs. Frequency

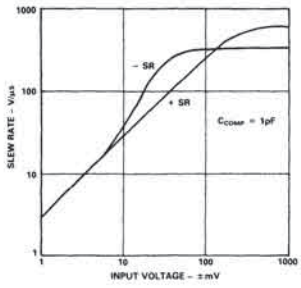


Figure 4. Slew Rate vs. Differential Input Voltage

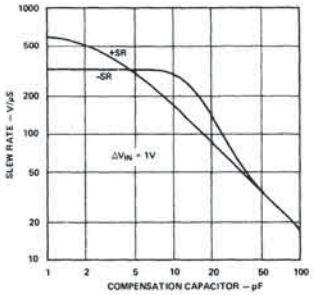


Figure 5. Slew Rate vs. Compensation Capacitor

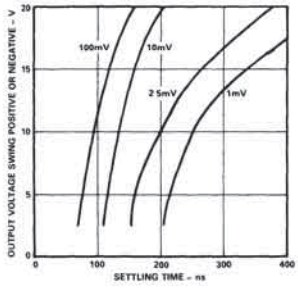


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

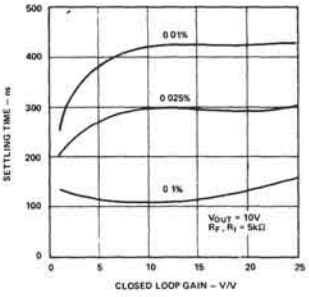


Figure 7. Settling Time vs. Closed Loop Gain

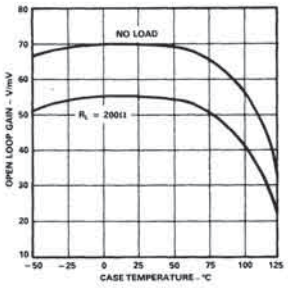


Figure 8. Gain vs. Temperature

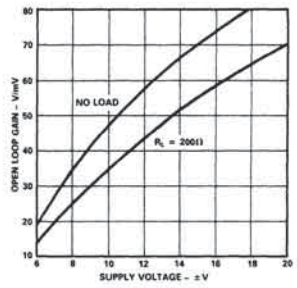


Figure 9. Gain vs. Supply Voltage

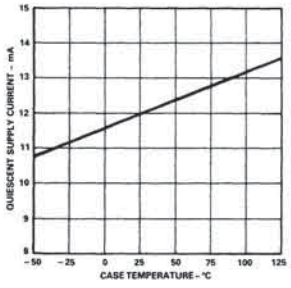


Figure 10. Supply Current vs. Temperature

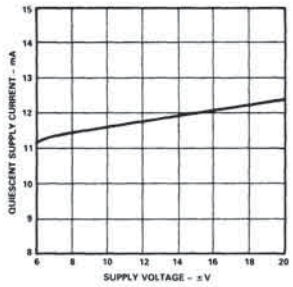


Figure 11. Supply Current vs. Supply Voltage

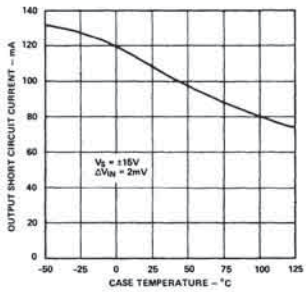


Figure 12. I_{SC} vs. Temperature

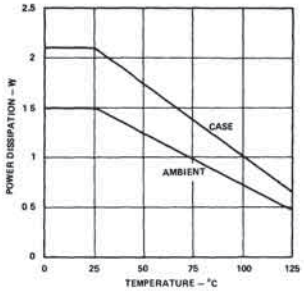


Figure 13. Power Dissipation vs. Temperature

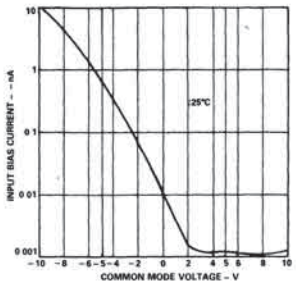


Figure 14. Input Bias Current vs. Common Mode Voltage

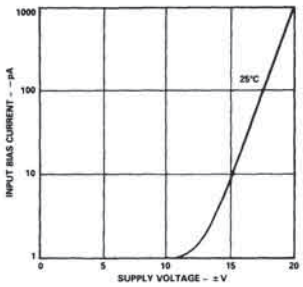


Figure 15. Input Bias Current vs. Supply Voltage

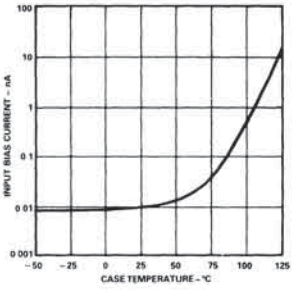


Figure 16. Input Bias Current vs. Temperature

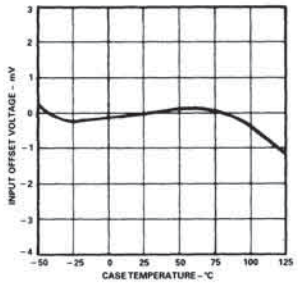


Figure 17. Offset Voltage vs. Temperature

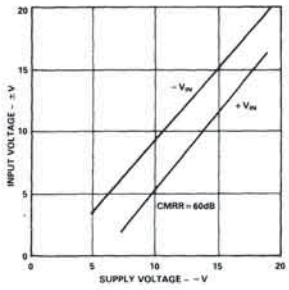


Figure 18. Input Voltage Range vs. Supply Voltage

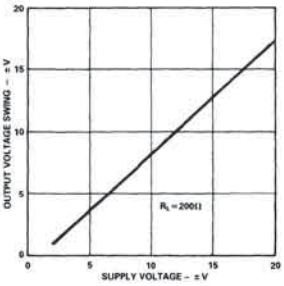


Figure 19. Output Voltage Swing vs. Supply Voltage

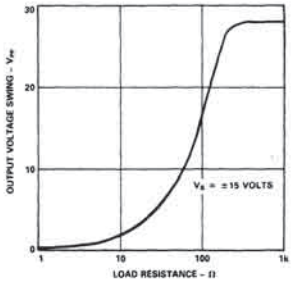


Figure 20. Output Voltage Swing vs. Load Resistance

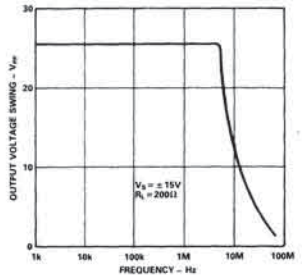


Figure 21. Large Signal Frequency Response

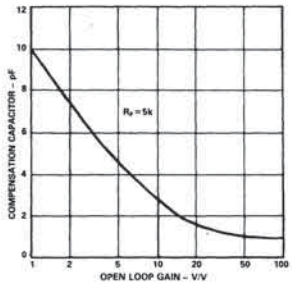


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

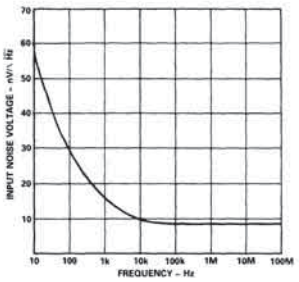


Figure 23. Input Noise Voltage Spectral Density

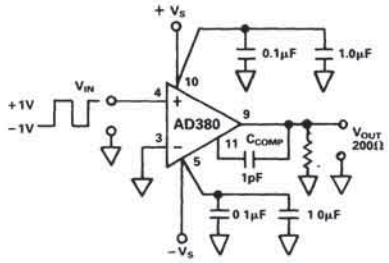


Figure 24a. Overdrive Recovery Test Circuit

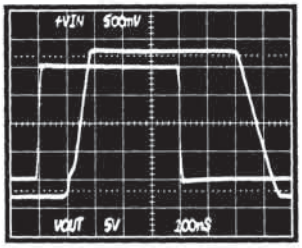


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

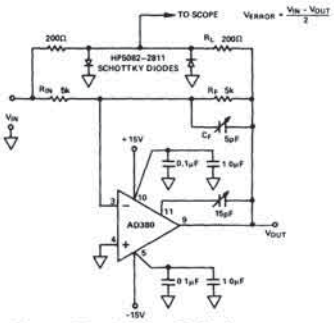


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

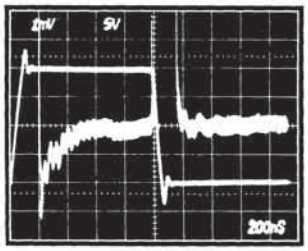


Figure 25b. Unity Gain Inverter Large Signal Response

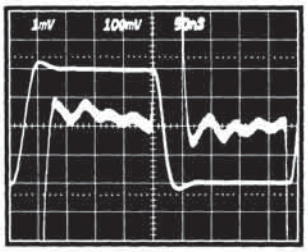


Figure 25c. Unity Gain Inverter Small Signal Response

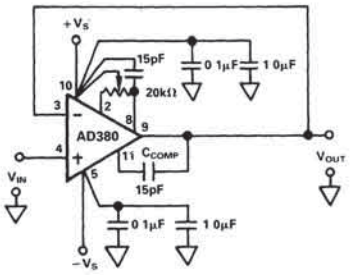


Figure 26a. Unity Gain Buffer Circuit

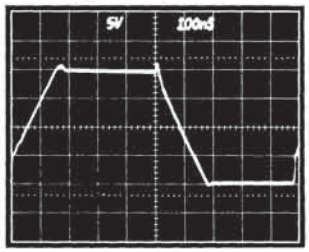


Figure 26b. Unity Gain Buffer Large Signal Response

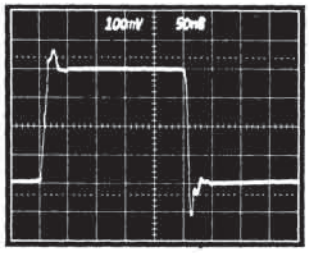


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits

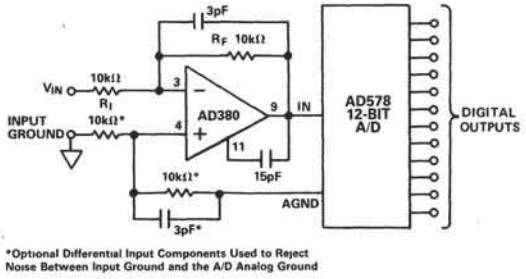


Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

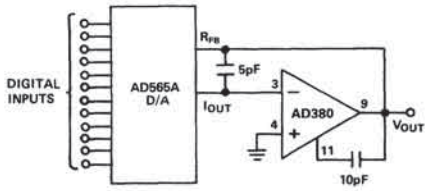


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

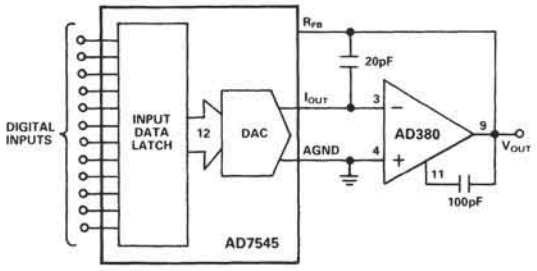


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

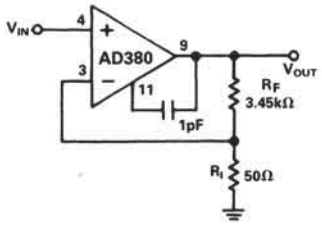


Figure 30. Video Amplifier

The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.

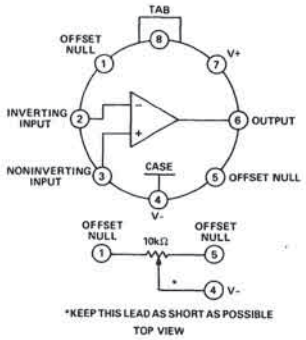
ANALOG DEVICES

High Speed, Low Drift FET Operational Amplifiers

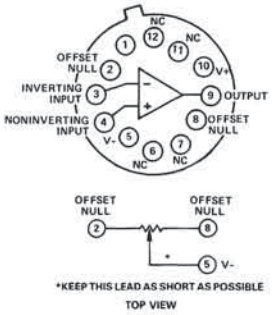
AD381/AD382

FEATURES
High Slew Rate 30V/μs
Fast Settling to 0.1%: 700ns
High Output Current: 50mA for AD382 (10mA for AD381)
Low Drift (5μV/°C–L Grades)
Low Offset Voltage (250μV–L Grades)
Low Input Bias Currents
Low Noise (2μV p-p)

AD381 PIN CONFIGURATION



AD382 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD381/AD382 are hybrid operational amplifiers combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for the L grades) and offset voltage drift (5μV/°C maximum for the L grades) are exceptionally low for high speed operational amplifiers.

In addition to superior low drift performance, the AD381 and AD382 offer the lowest guaranteed input bias currents of any wideband FET amplifier with 100pA max for the J grades of each and 50pA max for the AD382 K, L and S grades. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD381 and AD382 are especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD381 and AD382 are offered in three commercial versions, J, K and L specified from 0 to +70°C, and one extended temperature version, the S specified from −55°C to +125°C. All grades are packaged in hermetically sealed metal cans.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 250μV max on the L grade versions.
2. Analog Devices FET processing provides 100pA max (20pA typical) bias currents specified after 5 minutes of warm-up.
3. Internal frequency compensation, low offset voltage, and full device protection eliminate the need for external components and adjustments. This reduces circuit size and complexity and increases reliability.
4. The fast settling output (700ns to 0.1%) makes the AD381 and AD382 ideal for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts) makes it suitable for driving terminated (200Ω) twisted pair cables over the commercial temperature ranges.
6. The high slew rate (30V/μs) and high gain bandwidth product (5MHz) make the AD381 and AD382 an ideal choice for sample and holds and for high speed integrator circuits.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD381JH AD382JH	AD381KH AD382KH	AD381LH AD382LH	AD381SH AD382SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$ (AD381)	60,000 min	100,000 min	**	**
V_{OUT} = ±10V, R_L = 200Ω (AD382)	25,000 min	35,000 min	**	**
R_L = 10kΩ (AD382)	100,000 min	150,000 min	**	**
OUTPUT CHARACTERISTICS (AD382)				
Voltage @ R_L = 200Ω	±12V (±10V min)	*	*	Note 1
Voltage @ R_L = 10kΩ	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	80mA	*	*	*
OUTPUT CHARACTERISTICS (AD381)				
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	Note 2
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	20mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	5MHz	*	*	*
Full Power Response	500kHz	*	*	*
Slew Rate, Unity Gain	30V/μs (20V/μs min)	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*
10V Step to 0.01%	1.2μs	1.2μs (2.0μs max)	**	**
INPUT OFFSET VOLTAGE	1.0mV max	0.5mV max	0.25mV max	*
vs. Temperature, T_A = min to max[3]	15μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max
vs. Supply	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT[4]				
Either Input (AD381)	20pA (100pA max)	*	*	*
Either Input (AD382)	20pA (100pA max)	10pA (50pA max)	**	**
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 7pF$	*	*	*
Common Mode	$10^{12}\Omega \| 7pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	
Quiescent Current AD382	3.4mA (6mA max)	*	*	*
AD381	3.2mA (5mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz–10Hz	2μV p-p	*	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE[6]				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance – θJA (AD382)	100°C/W	*	*	*
Thermal Resistance – θJC (AD382)	70°C/W	*	*	*

NOTES

[1]The AD382SH has an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. To +125°C the output current is 35mA.

[2]The AD381SH has an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +70°C. From +70°C to +125°C the output current is 7mA.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C for every mV of offset nulled.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6]The S-grade is available in full compliance with MIL-STD-883 Rev C. Ask for the MIL-data sheet.

*Specifications same as J grade.

**Specifications same as K grade.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Offset	Offset T.C.	Output	Package Options*
AD381JH	1mV	15μV/°C	10mA	H-08B
AD381KH	0.5mV	10μV/°C	10mA	H-08B
AD381LH	0.25mV	5μV/°C	10mA	H-08B
AD381SH	1mV	10μV/°C	10mA	H-08B
AD382JH	1mV	15μV/°C	50mA	H-12A
AD382KH	0 5mV	10μV/°C	50mA	H-12A
AD382LH	0.25mV	5μV/°C	50mA	H-12A
AD382SH	1mV	10μV/°C	50mA	H-12A

*See Section 16 for package outline information

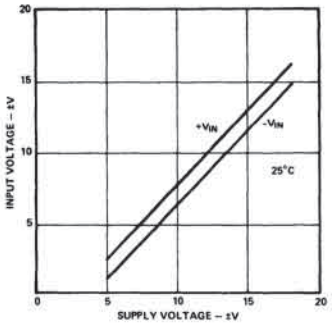


Figure 1. Input Voltage Range vs. Supply Voltage

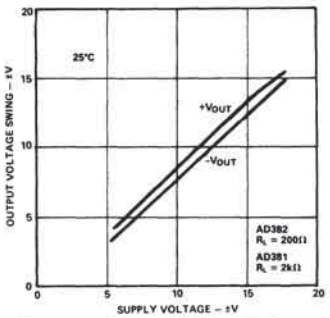


Figure 2. Output Voltage Swing vs. Supply Voltage

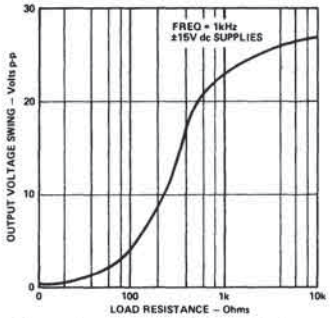


Figure 3a. Output Voltage Swing vs. Load Resistor for AD381

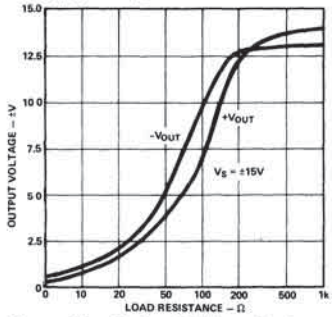


Figure 3b. Output Voltage Swing vs. Load Resistor for AD382

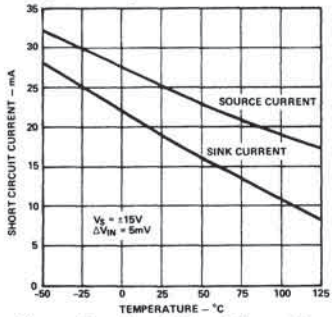


Figure 4a. Short Circuit Current vs. Temperature for AD381

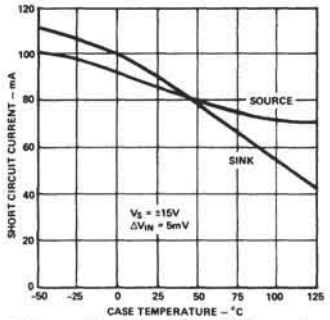


Figure 4b. Short Circuit Current vs. Temperature for AD382

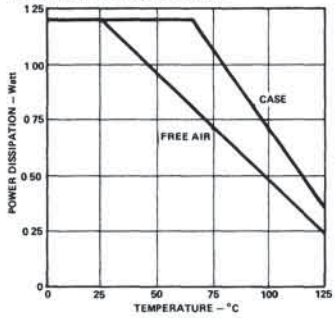


Figure 5. Permitted Dissipation vs. Temperature for AD382

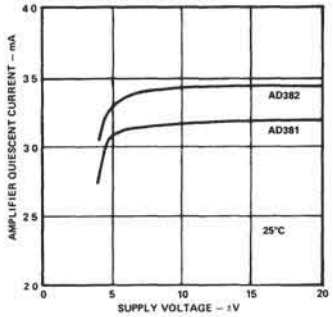


Figure 6. Quiescent Current vs. Supply Voltage

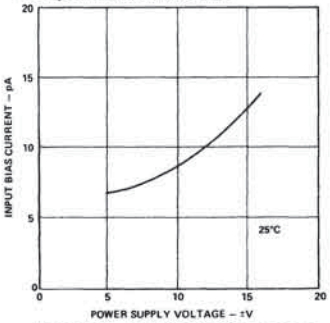


Figure 7. Input Bias Current vs. Supply Voltage

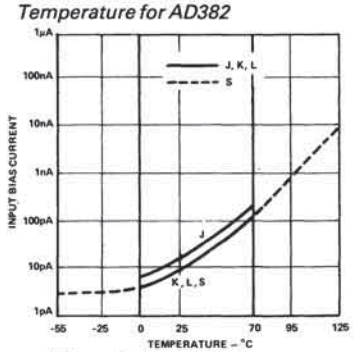


Figure 8. Input Bias Current vs. Temperature

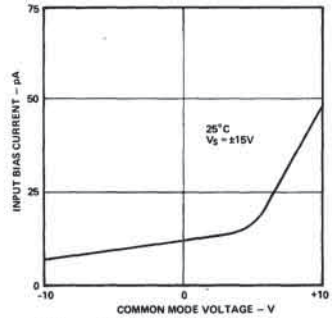


Figure 9. Input Bias Current vs. CMV

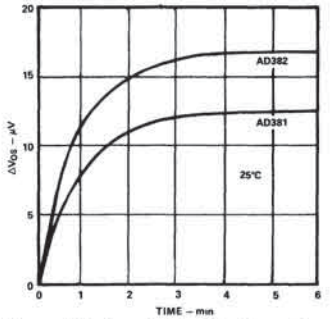


Figure 10. Input Offset Voltage Turn On Drift vs. Time

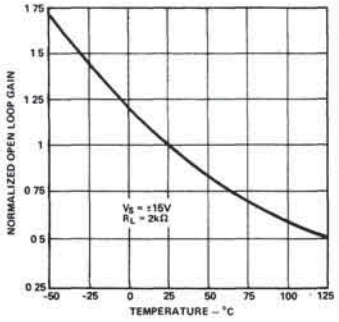


Figure 11a. Open Loop Gain vs. Temperature for AD381

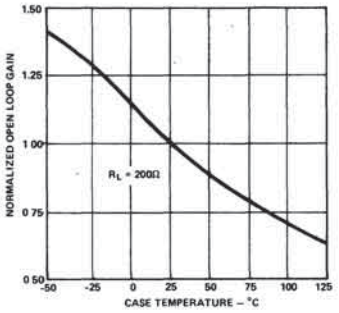


Figure 11b. Open Loop Gain vs. Temperature for AD382

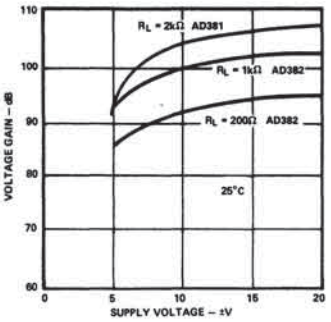


Figure 12. Open Loop Voltage Gain vs. Supply Voltage

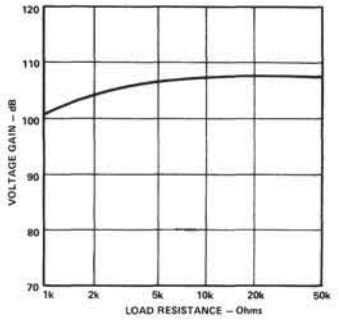


Figure 13a. Voltage Gain vs. Load Resistance for AD381

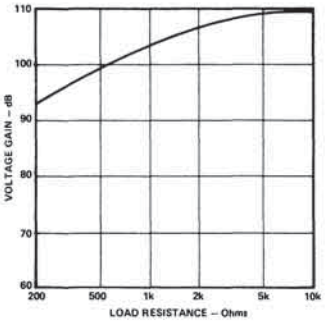


Figure 13b. Voltage Gain vs. Load Resistance for AD382

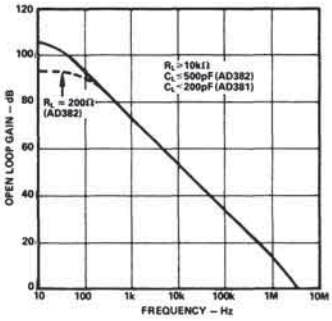


Figure 14. Open Loop Gain vs. Frequency

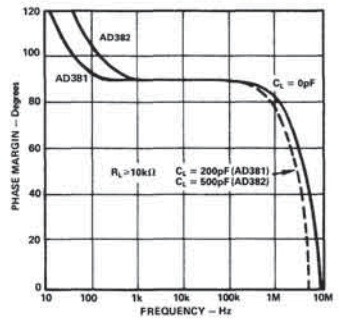


Figure 15. Phase Margin vs. Frequency

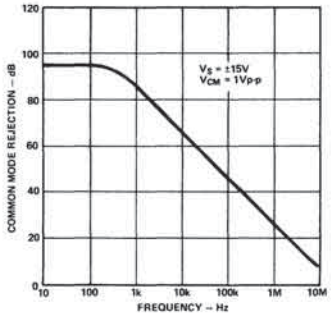


Figure 16. Common-Mode Rejection vs. Frequency

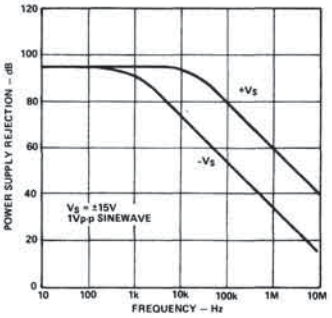


Figure 17. Power Supply Rejection vs. Frequency

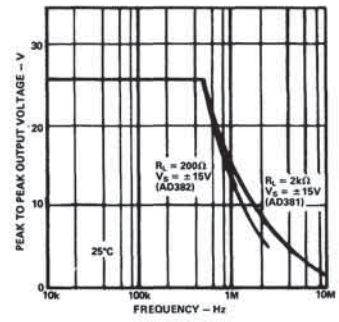


Figure 18. Large Signal Frequency Response

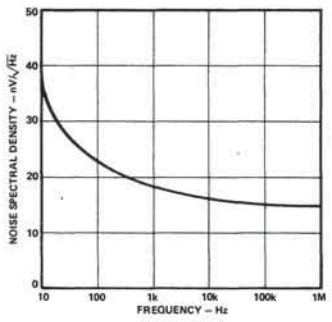


Figure 19. Noise vs. Frequency

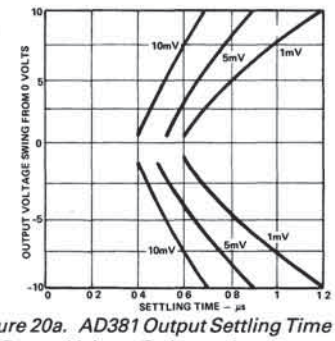


Figure 20a. AD381 Output Settling Time vs. Output Voltage Swing and Error (Circuit of Figure 22a)

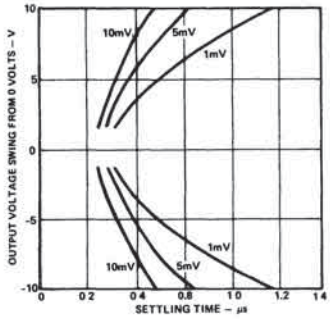


Figure 20b. AD382 Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

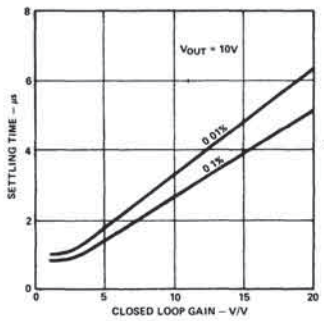


Figure 21. Settling Time vs. Closed Loop Gain (Circuits of Figures 22a & 23a)

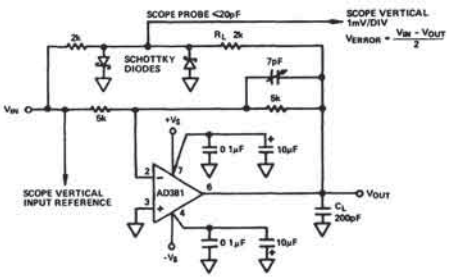


Figure 22. AD381 Unity Gain Inverter Settling Time Test Circuit

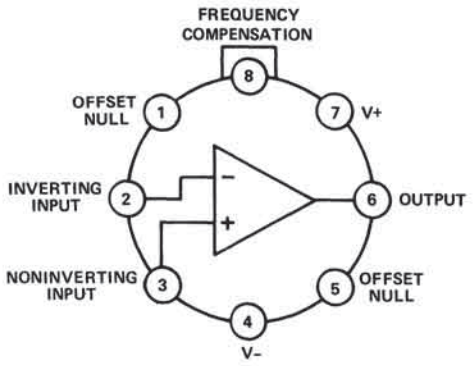
2

IC, Wideband, Fast Slewing General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

AD507 PIN CONFIGURATION



PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, -55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.
5. To take full advantage of the inherent high reliability of IC's, every AD507S receives a 24 hour stabilization bake at +150°C.

MIL-STANDARD-883

The AD507S/883 has the same electrical specifications as the AD507S, but is subjected to the 100% screening requirements specified in MIL-STD-883, Method 5004, Class B.

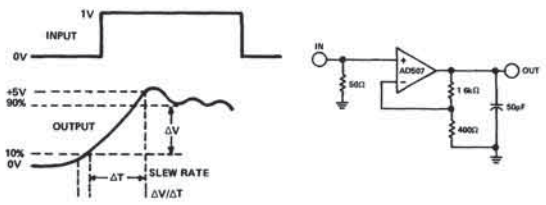
This procedure includes:

1. Pre-Cap Visual Inspection: Method 2010, Condition B.
2. Stabilization Bake: Method 1008, Condition C, 24 hours @ +150°C.
3. Temperature Cycle: Method 1010, Condition C, -65°C to +150°C, 10 cycles.
4. Centrifuge: Method 2001, Condition E, 30,000 g, Y_1 orientation.
5. Hermeticity, Gross Leak: Method 1014, Condition C, steps 1 and 2.
6. Hermeticity, Fine Leak: Method 1014, Condition A, 5×10^{-8} atm/cc/sec.
7. Burn-In: Method 1015, 160 hours @ +125°C.
8. Final Electrical Test.
9. External Visual: Method 2009.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S(AD507S/883)**
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T_{min} to T_{max}	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-65°C to +150°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION[1]			
H-08A	AD507JH	AD507KH	AD507SH

NOTES
[1] See Section 16 for package outline information.
*Specifications same as AD507J.
**AD507S/88 3 minimum order 10 pieces.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V- 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

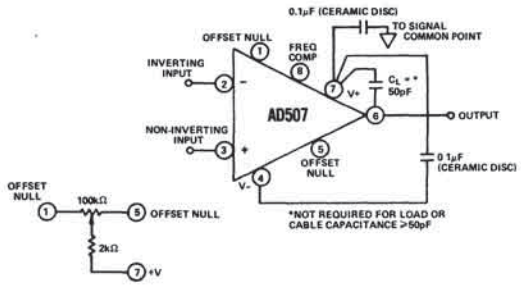


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

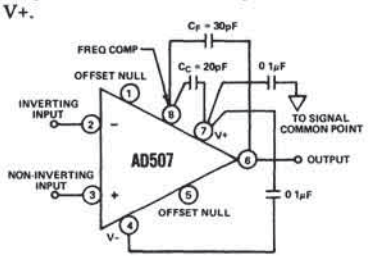


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

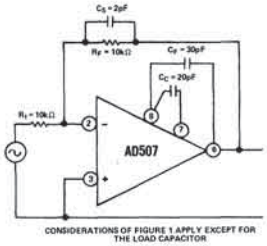
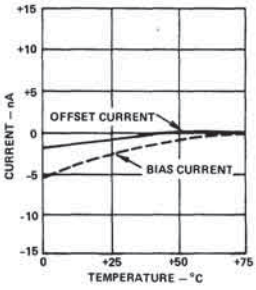
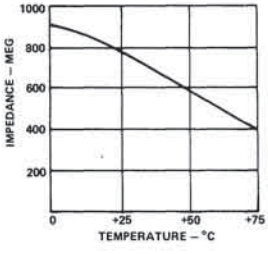


Figure 3. Fast Settling Time Configuration

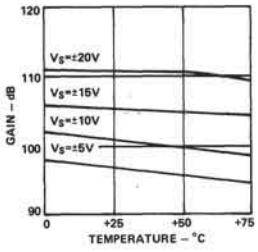
TYPICAL PERFORMANCE CURVES



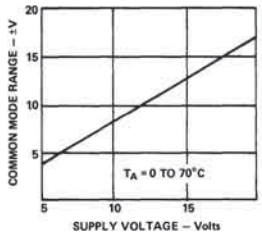
Input Bias Current and Offset Current vs Temperature



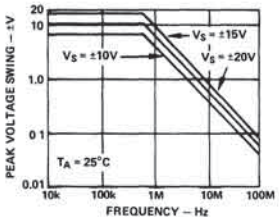
Input Impedance vs Temperature



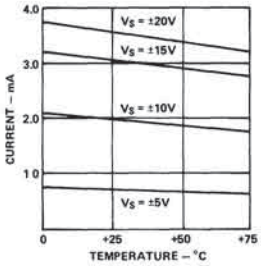
Open Loop Voltage Gain vs Temperature



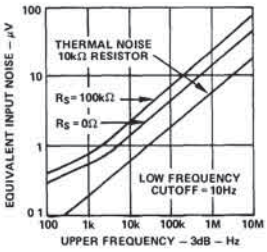
Common Mode Voltage Range vs Supply Voltage



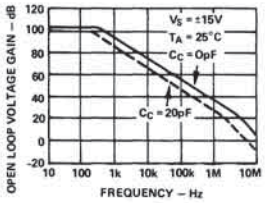
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

FEATURES

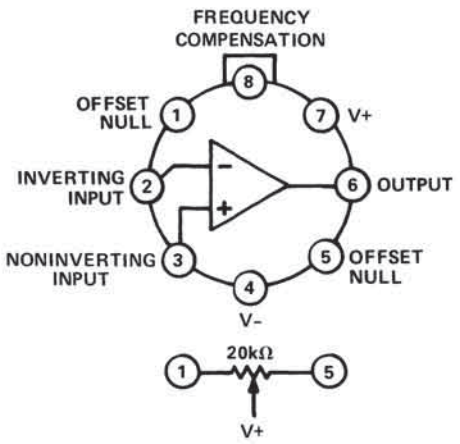
- Fast Settling Time
  - 0.1% in 500ns max
  - 0.01% in 2.5μs max
- High Slew Rate: 100V/μs min
- Low I_{OS}: 25nA max
- Guaranteed V_{OS} Drift: 30μV/°C max
- High CMRR: 80dB min
- Drives 500pF
- Low Price

APPLICATIONS

- D/A and A/D Conversion
- Wideband Amplifiers
- Multiplexers
- Pulse Amplifiers

AD509 PIN CONFIGURATIONS

TO-99



TOP VIEW

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
2. The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD509J Min	AD509J Typ	AD509J Max	AD509K Min	AD509K Typ	AD509K Max	AD509S Min	AD509S Typ	AD509S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**7,500**	15,000		**10,000**	15,000		**10,000**	15,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	5,000			7,500			**7,500**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80	120		80	120		100	120		V/μs
Settling Time										
to 0.1%		200			200			200	500	ns
to 0.01%		1.0			1.0			1.0	2.5	μs
INPUT OFFSET VOLTAGE										
Initial Offset		5	**10**		4	**8**		4	**8**	mV
Input Offset Voltage T_{min} to T_{max}			14			11			**11**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**	μV/V
INPUT BIAS CURRENT										
Initial		125	**250**		100	**200**		100	**200**	nA
T_{min} to T_{max}			500			400			**400**	nA
INPUT OFFSET CURRENT										
Initial		20	50		10	25		10	25	nA
T_A = min to max			100			50			50	nA
INPUT IMPEDANCE										
Differential	40	100		50	100		50	100		MΩ
INPUT VOLTAGE RANGE										
Differential		±15			±15			±15		V
Common Mode		±10			±10			±10		V
Common Mode Rejection	**74**	90		**80**	90		**80**	90		dB
INPUT NOISE VOLTAGE										
f = 10Hz		100			100			100		nV/√Hz
f = 100Hz		30			30			30		nV/√Hz
f = 100kHz		19			19			19		nV/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±20	±5		±20	±5		±20	V
Quiescent Current		4	**6**		4	**6**		4	**6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]										
TO-99 Style (H-08A)		AD509JH			AD509KH			AD509SH		

NOTES

[1]See Section 16 for package outline information

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

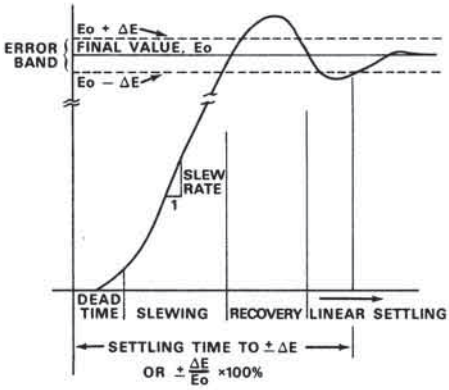


Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope display. The resultant waveform of ($E_O - E_{IN}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

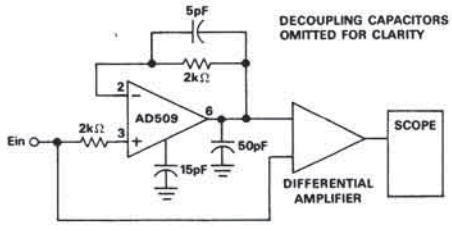


Figure 2. AD509 Settling Time Test Circuit

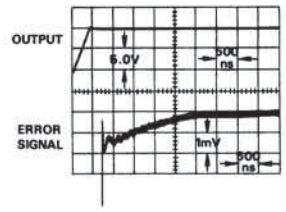


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

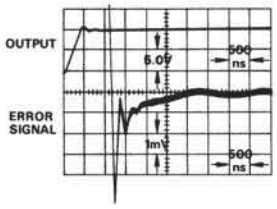


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

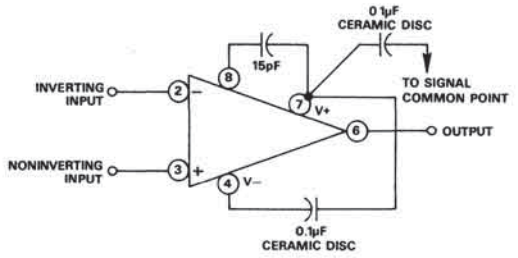


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

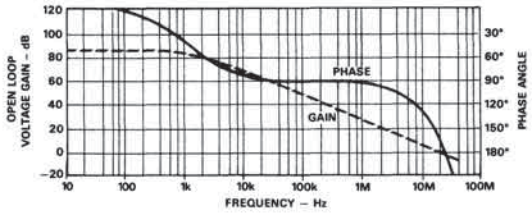


Figure 6. Open Loop Frequency and Phase Response

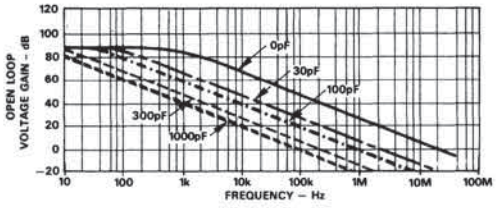


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s \text{ TOTAL} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

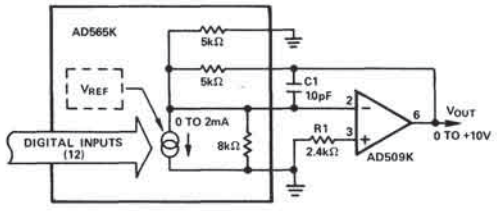


Figure 8. AD509 as an Output Amplifier for a Fast Current-Output D-to-A Converter

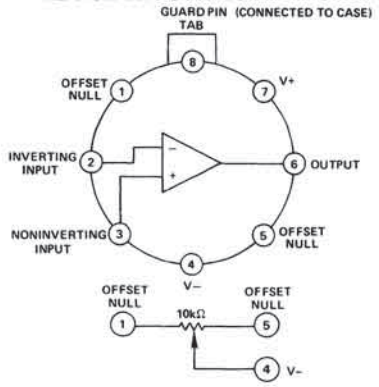
Monolithic Precision, Low-Power FET-Input Electrometer Op Amp

AD515A*

FEATURES

Ultralow Bias Current: 0.075pA max (AD515AL)
0.150pA max (AD515AK)
0.300pA max (AD515AJ)
Low Power: 1.5mA max Quiescent Current (0.6mA typ)
Low Offset Voltage: 1.0mV max (AD515AK & L)
Low Drift: 15μV/°C max (AD515AK)
Low Noise: 4μV p-p, 0.1Hz to 10Hz

AD515A PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD515A is a monolithic FET-input operational amplifier with a guaranteed maximum input bias current of 75fA (AD515AL). The AD515A is a monolithic successor to the industry standard AD515 electrometer, and will replace the AD515 in most aplications. The AD515A also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultralow bias current circuits. All devices are internally compensated, free of latch-up and short circuit protected.

The AD515A's combination of low input bias current, offset voltage and drift optimizes it for a wide variety of electrometer and very high impedance buffer applications including photo-current detection, vacuum ion-gage measurement, long-term precision integration and low drift sample/hold applications. This amplifier is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological micro-probes. In addition, the low cost and pin compatibility of the AD515A with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The $10^{15}\Omega$ common-mode input impedance ensures that the input bias current is essentially independent of common-mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (Pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients.

The AD515A is available in three versions of bias current and offset voltage, the "J", "K" and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package. The industry standard hybrid version, AD515, will also be available.

***Covered by Patent No. 4,639,683.**

PRODUCT HIGHLIGHTS

1. The AD515A provides subpicoampere bias currents in an integrated circuit amplifier.
   - The ultralow input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±V supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is 15μV/°C maximum on the K grade.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per mV).
3. The low quiescent current drain of 0.6mA typical and 1.5mA maximum, keeps self-heating effects to a minimum and renders the AD515A suitable for a wide range of remote probe applications.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over 1MΩ up to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristic.
5. Every AD515A receives a 24-hour stabilization bake at +150°C, to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

Model	AD515AJ	AD515AK	AD515AL
OPEN-LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**20,000V/V min**	**40,000V/V min**	**25,000V/V min**
$R_L \geq 10k\Omega$	**40,000V/V min**	**100,000V/V min**	**50,000V/V min**
T_A = min to max $R_L \geq 2k\Omega$	**15,000V/V min**	**40,000V/V min**	**25,000V/V min**
OUTPUT CHARACTERISTICS			
Voltage@ R_L = 2kΩ, T_A = min to max	**±10V min (±12V typ)**	*	*
@ R_L = 10kΩ, T_A = min to max	**±12V min (±13V typ)**	*	*
Load Capacitance[2]	1000pF		
Short-Circuit Current	**10mA min (20mA typ)**		
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1MHz	*	*
Full Power Response	5kHz min (30kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (2.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*
INPUT OFFSET VOLTAGE[3]	**3.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**
vs. Temperature, T_A = min to max	**50μV/°C max**	**15μV/°C max**	**25μV/°C max**
vs. Supply, T_A = min to max	**400μV/V max (50μV/V typ)**	**100μV/V max**	**200μV/V max**
INPUT BIAS CURRENT			
Either Input[4]	**300fA max**	**150fA max**	**75fA max**
INPUT IMPEDANCE			
Differential V_{DIFF} = ±1V	1.6pF‖$10^{13}\Omega$	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	75nV/$\sqrt{Hz}$	*	*
f = 100Hz	55nV/$\sqrt{Hz}$	*	*
f = 1kHz	50nV/$\sqrt{Hz}$	*	*
Current, 0.1Hz to 10Hz	0.003pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	**±20V min**	*	*
Common Mode, T_A = min to max	**±10V min (+12V, −11 typ)**	*	*
Common-Mode Rejection, V_{IN} = ±10V	**66dB min (94dB typ)**	**80dB min**	**70dB min**
Maximum Safe Input Voltage[5]	$\pm V_S$	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	**±5V min (±18V max)**	*	*
Quiescent Current	**1.5mA max (0.6mA typ)**	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*
PACKAGE OPTION[6]			
TO-99 (H-08A)	AD515AJH	AD515AKH	AD515ALH

NOTES
*Specifications same as AD515AJ.
[1]Open Loop Gain is specified with or without nulling of V_{OS}.
[2]A conservative design would not exceed 750pF of load capacitance.
[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage. See next page.
[6]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515A, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515A can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultralow input currents of the AD515A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation and, hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515A is brought out separately to Pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry and reduces common-mode input capacitance to about 0.8pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

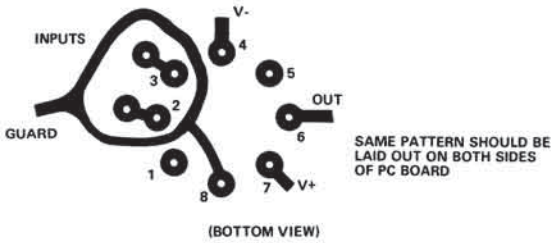


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515A can deliver. The best performance will be realized by using a teflon IC socket for the AD515A; but at least a teflon stand-off should be used for the high impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

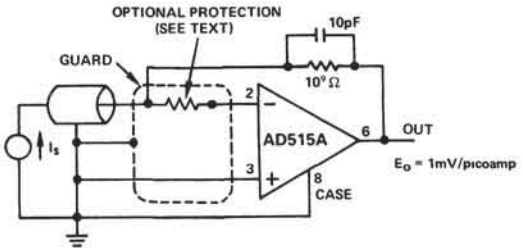


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

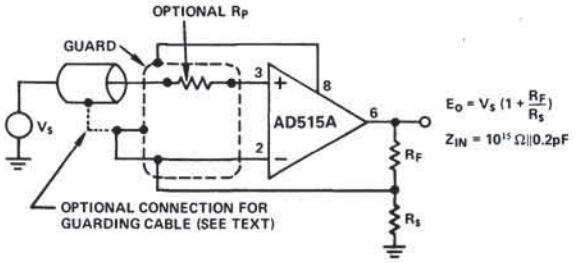


Figure 3. Very High Impedance Noninverting Amplifier

INPUT PROTECTION

The AD515A is guaranteed for a maximum safe input potential equal to the power supply potential.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate Zener protection schemes which often compromise overall performance. The AD515A requires input protection only if the source is not current limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.1mA (for example, 1MΩ for a 100V overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515A virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short, rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is usually about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515A. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will destabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Noninverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to a guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may be destabilized and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at Pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

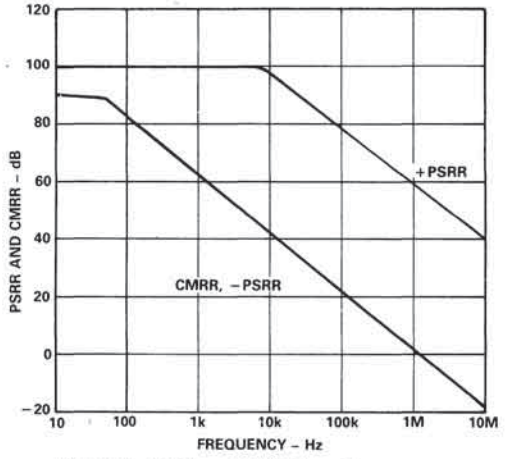


Figure 4. PSRR and CMRR vs. Frequency

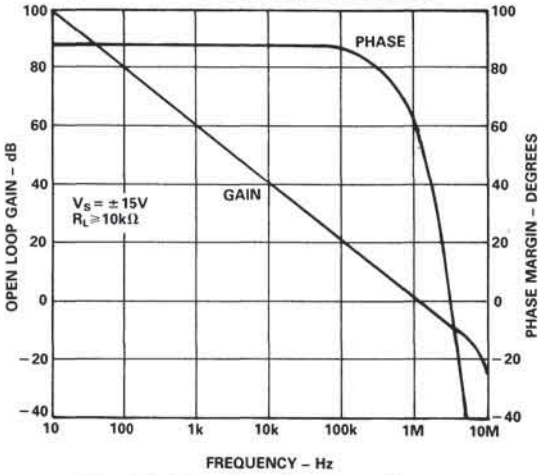


Figure 5. Open Loop Frequency Response

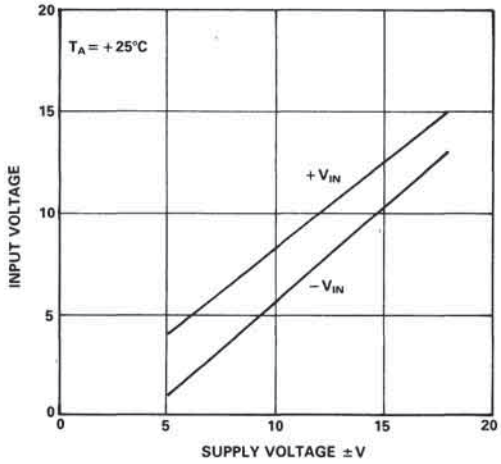


Figure 6. Input Common-Mode Range vs. Supply Voltage

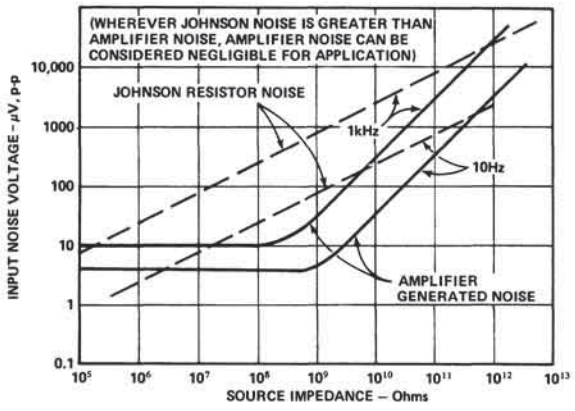


Figure 7. Peak-to-Peak Input Noise Voltage vs. Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515A offers subpicoampere input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515A and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515A has been reduced to less than 1mA. Figure 8 shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load resistance to be at least 10kΩ.
4. Figure 10 shows the AD515A's input current versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1 to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

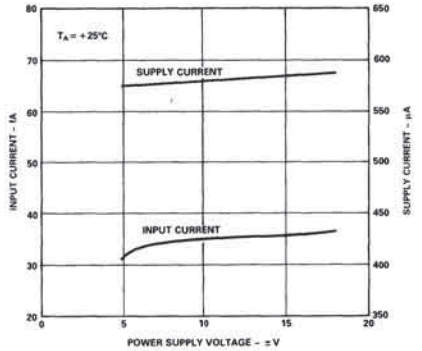


Figure 8. Input Bias Current and Supply Current vs. Supply Voltage

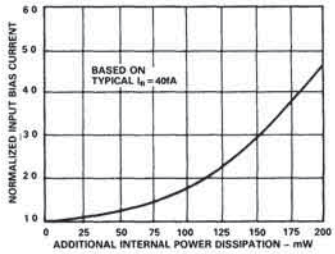


Figure 9. Input Bias Current vs. Additional Power Dissipation

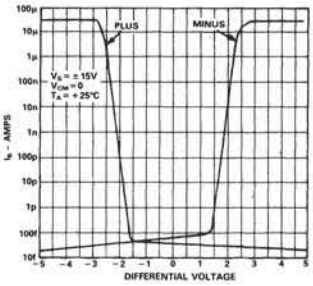


Figure 10. Input Bias Current vs. Differential Input Voltage

AD515A CIRCUIT APPLICATION NOTES

The AD515A is quite simple to apply to a wide variety of applications because of the pretrimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High MΩ resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high MΩ resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long-term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515A is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515A are significant only above $10^{11}\Omega$.

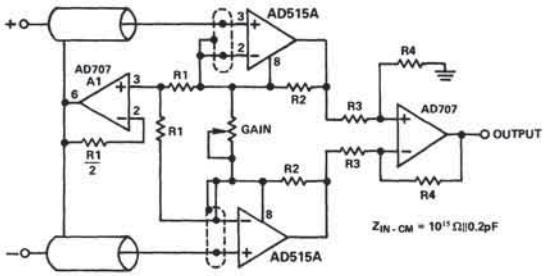


Figure 11. Very High Impedance Instrumentation Amplifier

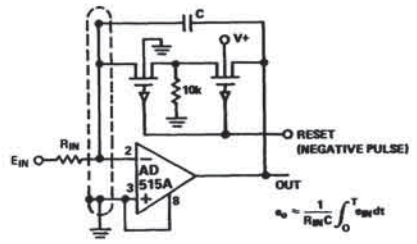


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT-TO-VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515A makes the tradeoff easier.

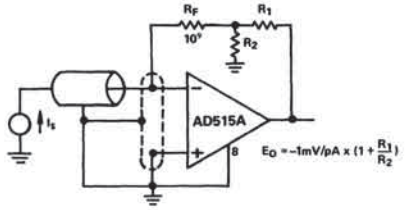


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the noninverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD524 instrumentation amplifier converts the floating differential signal to a single-ended output.

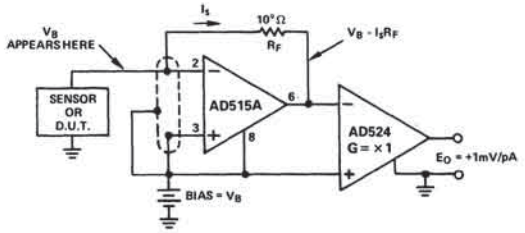


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG DEVICES

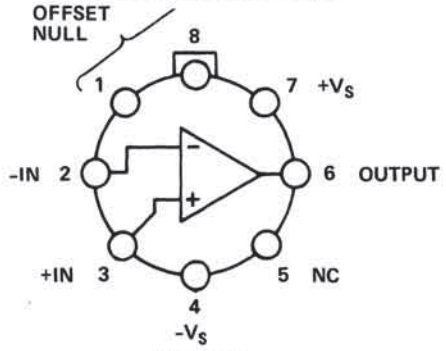
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 1.3μV/°C (AD517L)
Internal Compensation
MIL-Standard Parts Available
8-Pin TO-99 Hermetic Metal Can

AD517 PIN CONFIGURATION



TOP VIEW

PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Chips are available.

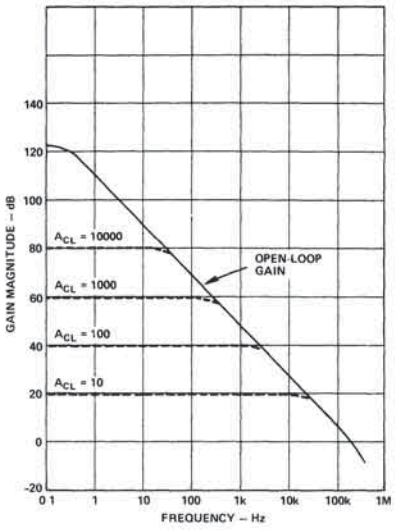
SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD517J Min	AD517J Typ	AD517J Max	AD517K Min	AD517K Typ	AD517K Max	AD517L Min	AD517L Typ	AD517L Max	AD517S Min	AD517S Typ	AD517S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, R_L ≥ 2kΩ	**10^6**			**10^6**			**10^6**			**10^6**			V/V
T_{min} to T_{max}, R_L = 2kΩ	500,000			500,000			500,000			**250,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**			**±10**			**±10**			**±10**			V
Load Capacitance		1000			1000			1000			1000		pF
Output Current	10			10			10			10			mA
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		250			250			250			250		kHz
Full Power Response		1 5			1 5			1 5			1 5		kHz
Slew Rate, Unity Gain		0 10			0.10			0 10			0 10		V/μs
INPUT OFFSET VOLTAGE													
Initial Offset			**150**			**75**			**50**			**75**	μV
Input Offset vs Temp.			3.0			**1.8**			**1.3**			**1.8**	μV/°C
Input Offset vs Supply			**25**			**10**			**10**			**10**	μV/V
T_{min} to T_{max}			40			15			15			**20**	μV/V
INPUT BIAS CURRENT													
Initial			5			**2**			**1.0**			**2.0**	nA
T_{min} to T_{max}			8			3 5			1 5			**10**	nA
vs. Temp, T_{min} to T_{max}			±20			±10			±4			±10	pA/°C
INPUT OFFSET CURRENT													
Initial			**1.0**			**0.75**			**0.25**			**2.0**	nA
T_{min} to T_{max}			1 5			1 25			0 4			**10**	nA
INPUT IMPEDANCE													
Differential		15‖1 5			20‖1 5			20‖1 5			20‖1 5		MΩ‖pF
Common Mode		2 0 × 10"			2 0 × 10"			2.0 × 10"			2 0 × 10"		Ω
INPUT VOLTAGE RANGE													
Differential		±V_S			±V_S			±V_S			±V_S		V
Common Mode Rejection	**94**			**110**			**110**			**110**			dB
Common Mode Rejection T_{min} to T_{max}	94			110			100			**100**			dB
INPUT NOISE													
Voltage, 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		25			25			25			25		nV/√Hz
f = 1kHz		20			20			20			20		nV/√Hz
Current, f = 10kHz		0 05			0 05			0.05			0 05		pA/√Hz
f = 100Hz		0 03			0 03			0 03			0 03		pA/√Hz
f = 1kHz		0 03			0.03			0 03			0 03		pA/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**4**			**3**			**3**			**3**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[1]													
TO-99 Style (H-08B)		AD517JH			AD517KH			AD517LH			AD517SH		

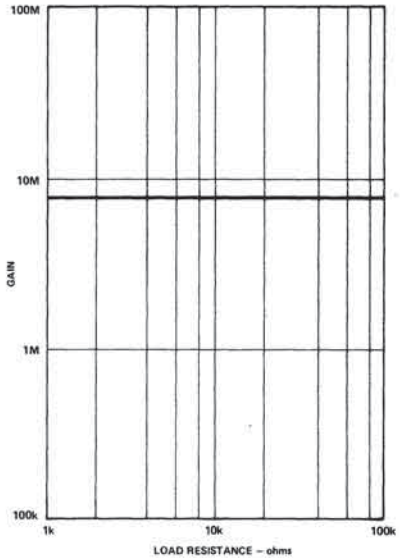
NOTES
[1]See Section 16 for package outline information
Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

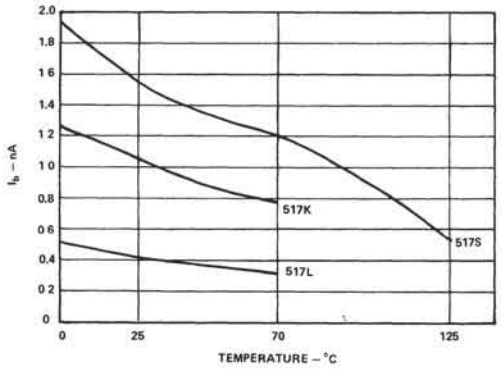
Typical Performance Curves



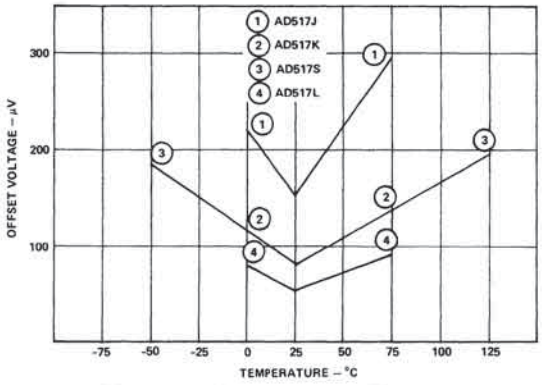
Small-Signal Gain vs. Frequency



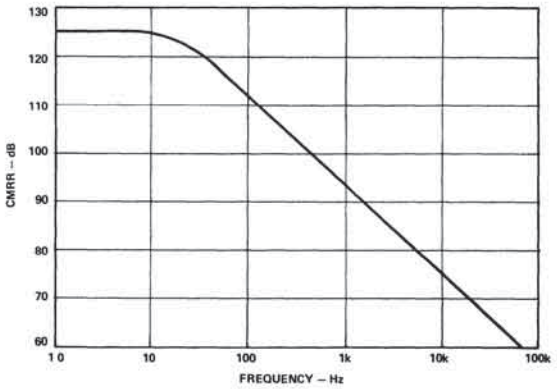
Open-Loop Gain vs. Load Resistance



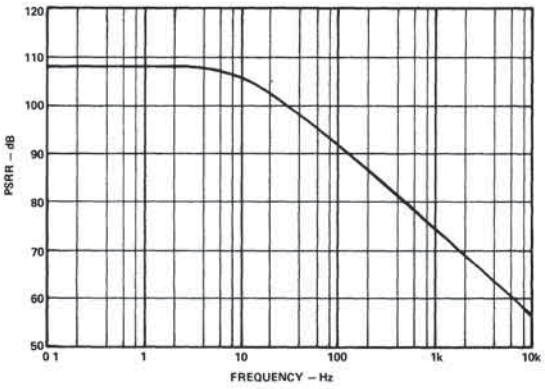
Input Bias Current vs. Temperature



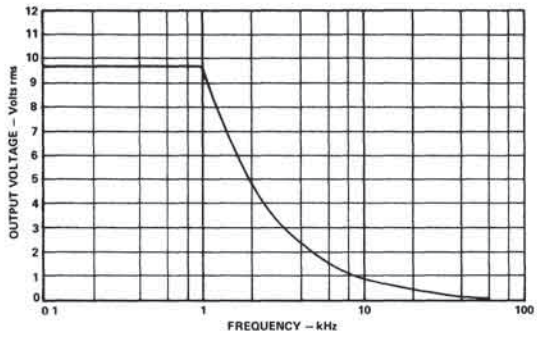
Untrimmed Offset Voltage vs. Temperature



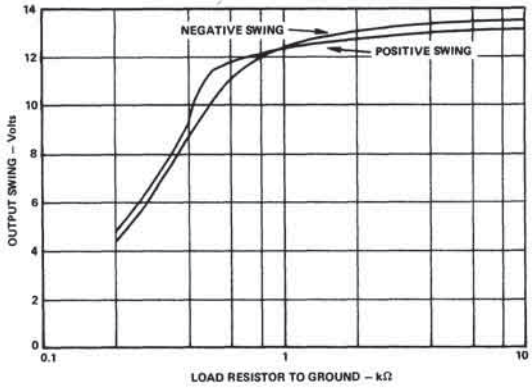
CMRR vs. Frequency



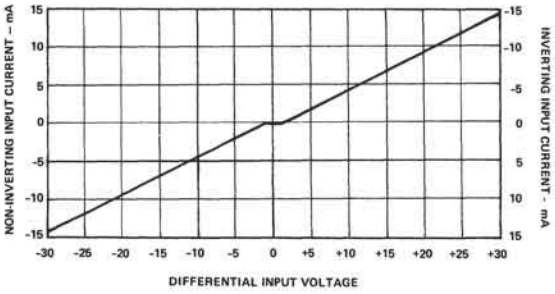
PSRR vs. Frequency



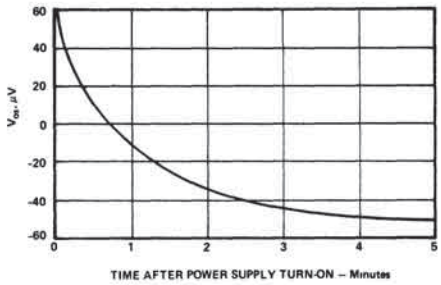
Maximum Undistorted Output vs. Frequency (Distortion ⩽ 1%)



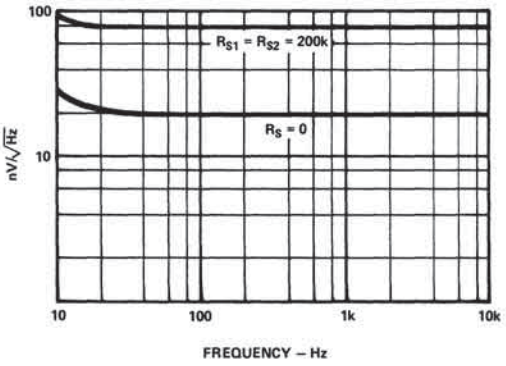
Output Voltage vs. Load Resistance



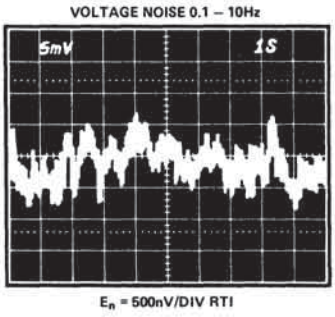
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

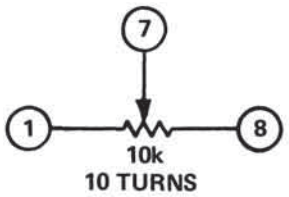
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

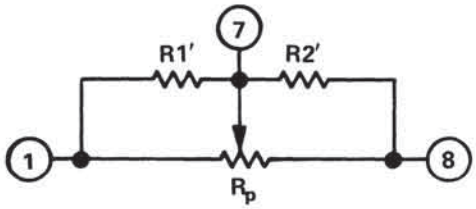
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

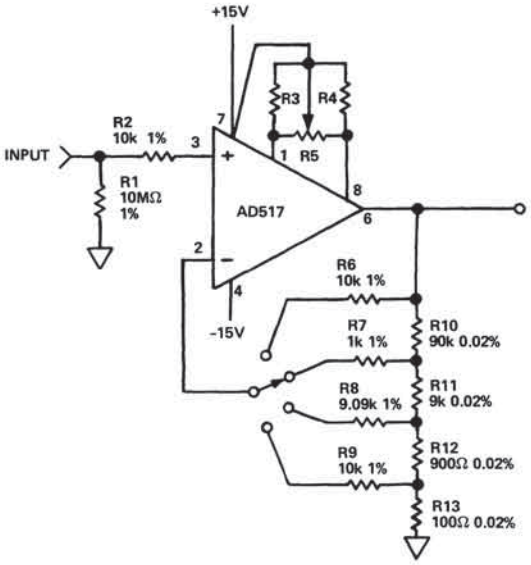


Figure 2. Stable Instrument Input Amplifier

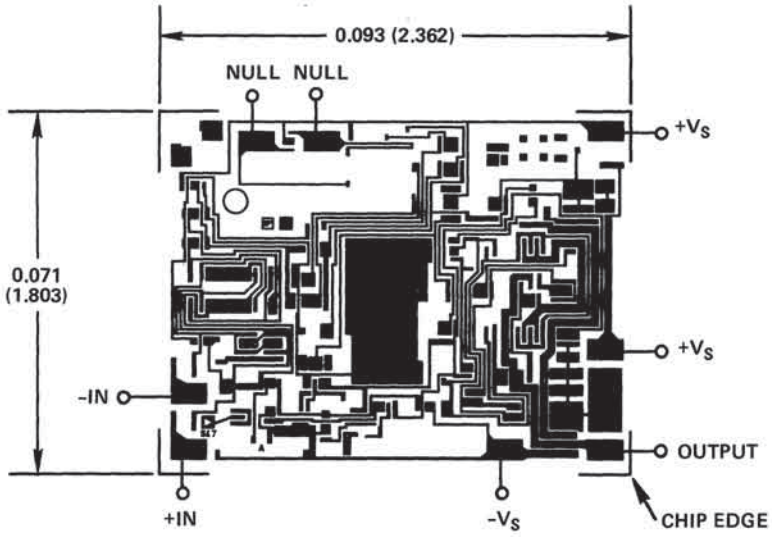
Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6. R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN LASER-TRIMMED CHIP FORM.

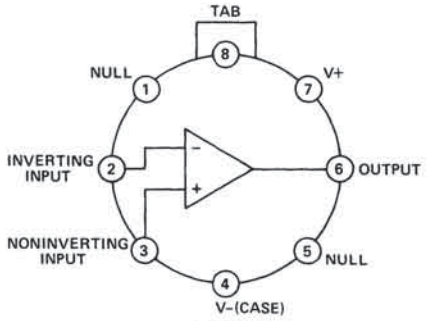
ANALOG DEVICES

High Performance BiFET Operational Amplifiers

AD542/AD544/AD547

FEATURES
Ultralow Drift: 1μV/°C – AD547L
Low Offset Voltage: 0.25mV – AD547L
Low Input Bias Currents: 25pA max, Warmed-Up
Low Quiescent Current: 1.5mA
Low Noise: 2μV p-p
High Open Loop Gain: 110dB
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0025%

AD542, AD544, AD547 FUNCTIONAL BLOCK DIAGRAM



TOP VIEW

PRODUCT DESCRIPTION

The BiFET series are precision monolithic FET-input operational amplifiers fabricated with the most advanced BiFET and laser trimming technologies. The series offers bias currents significantly lower than currently available BiFET devices, 25pA max, warmed-up.

In addition, the offset voltage is laser trimmed to less than 0.25mV on the AD547L which is achieved by utilizing Analog's exclusive laser-wafer trimming (LWT) process. When combined with the AD547's low offset voltage drift (1μV/°C), these features offer the user IC performance truly superior to existing BiFET op amps–and at low, BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain–even under heavy loading–ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it the first choice as an output amplifier for current output D/A converters such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the −55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and offset voltage to only 0.25mV max on the AD547L.
4. Low voltage noise (2μV, p-p), and low offset voltage drift enhance performance as a precision op amp.
5. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0025%) make the AD544 an ideal choice for audio applications.
7. Unmounted chips available for hybrid circuit applications.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD542 Min	AD542 Typ	AD542 Max	AD544 Min	AD544 Typ	AD544 Max	AD547 Min	AD547 Typ	AD547 Max	Units
OPEN LOOP GAIN[1]										
$V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$										
J	**100,000**			**30,000**			**100,000**			V/V
K, L, S	**250,000**			**50,000**			**250,000**			V/V
$T_A = T_{min}$ to T_{max}										
J	100,000			20,000			100,000			V/V
S	**100,000**			**20,000**			**100,000**			V/V
K, L	**250,000**			**40,000**			**250,000**			V/V
OUTPUT CHARACTERISTICS										
$V_{OUT} = R_L = 2k\Omega$										
$T_A = T_{min}$ to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		Volts
$V_{OUT} = R_L = 10k\Omega$										
$T_A = T_{min}$ to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		Volts
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2 0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	**2.0**	3 0		**8.0**	13 0		**2.0**	3.0		V/μs
Total Harmonic Distortion					0 0025					%
INPUT OFFSET VOLTAGE[2]										
J			**2.0**			**2.0**			**1.0**	mV
K			**1.0**			**1.0**			**0.5**	mV
L			**0.5**			**0.5**			**0.25**	mV
S			**1.0**			**1.0**			**0.5**	mV
vs Temperature[3]										
J			20			20			5	μV/°C
K			**10**			**10**			**2**	μV/°C
L			5			5			**1**	μV/°C
S			**15**			**15**			**5**	μV/°C
vs Supply, $T_A = T_{min}$ to T_{max}										
J			200			200			**200**	μV/V
K, L, S			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[4]										
Either Input										
J			**50**			**50**			**50**	pA
K, L, S		10	**25**		10	**25**		10	**25**	pA
Input Offset Current										
J		5	**15**		5	**15**		5	**15**	pA
K, L, S		2	**15**		2	**15**		2	**15**	pA
INPUT IMPEDANCE										
Differential		$10^{12}\Omega$‖6pF			$10^{12}\Omega$‖6pF			$10^{12}\Omega$‖6pF		
Common Mode		$10^{12}\Omega$‖3pF			$10^{12}\Omega$‖3pF			$10^{12}\Omega$‖3pF		
INPUT VOLTAGE[5]										
Differential		±20			±20			±20		Volts
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		Volts
Common-Mode Rejection										
$V_{IN} = \pm 10V$										
J	**76**			**76**			**76**			dB
K, L, S	**80**			**80**			**80**			dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		Volts
Operating	±5		**±18**	±5		**±18**	±5		**±18**	Volts
Quiescent Current		1 1	1.5		1 8	2.5		1 1	1.5	mA
VOLTAGE NOISE										
0 1–10Hz										
J		2 0			2 0			2 0		μV p-p
K, L, S		2 0			2 0				**4.0**	μV p-p
10Hz		70			35			70		nV/√Hz
100Hz		45			22			45		nV/√Hz
1kHz		30			18			30		nV/√Hz
10kHz		25			16			25		nV/√Hz
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L		0 to + 70			0 to + 70			0 to + 70		°C
S		55 to + 125			55 to + 125			55 to + 125		°C
Storage		65 to + 150			65 to + 165			65 to + 165		°C
PACKAGE OPTIONS[6]										
TO-99 (H-08A)	AD542JH, AD542KH AD542LH, AD542SH			AD544JH, AD544KH AD544LH, AD544SH			AD547JH, AD547KH AD547LH, AD547SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled Nulling will induce an additional 3μV/°C/mV of nulled offset.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$ For higher temperatures, the current doubles every 10°C

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6]See Section 16 for package outline information

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test Results from those tests are used to calculate outgoing quality levels All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

Typical Characteristics

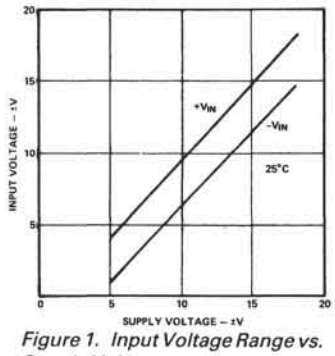


Figure 1. Input Voltage Range vs. Supply Voltage

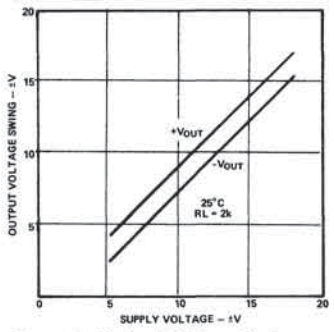


Figure 2. Output Voltage Swing vs. Supply Voltage

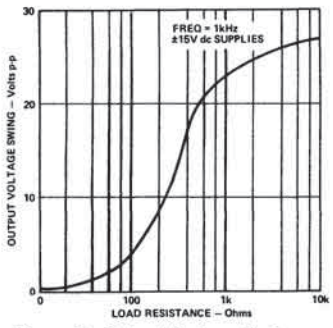


Figure 3. Output Voltage Swing vs. Resistive Load

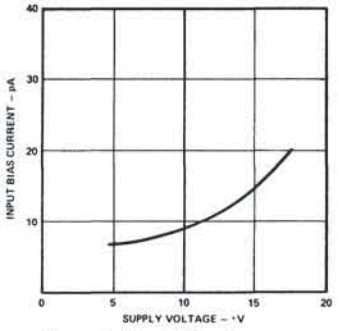


Figure 4. Input Bias Current vs. Supply Voltage

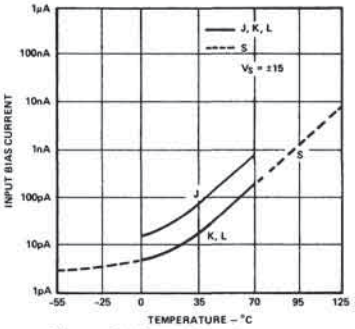


Figure 5. Input Bias Current vs. Temperature

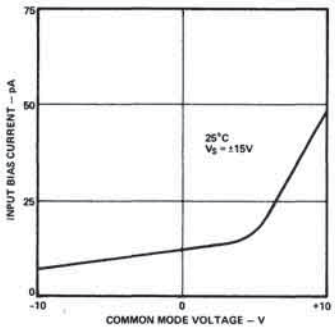


Figure 6. Input Bias Current vs. CMV

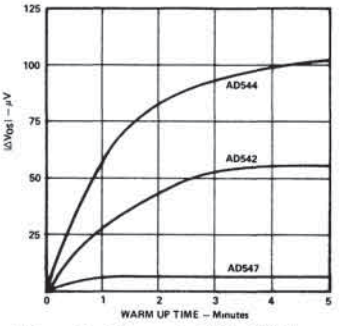


Figure 7. Change in Offset Voltage vs. Warm-Up Time

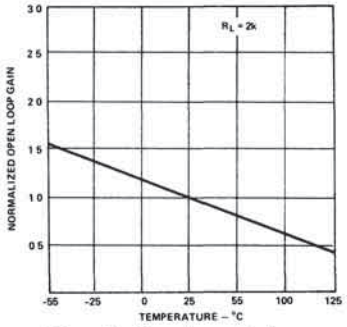


Figure 8. Open Loop Gain vs. Temperature

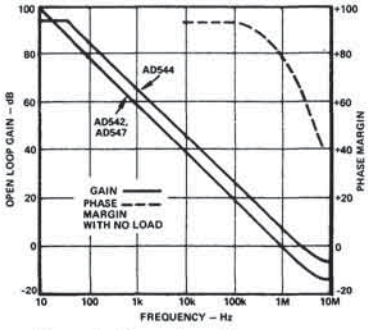


Figure 9. Open Loop Frequency Response

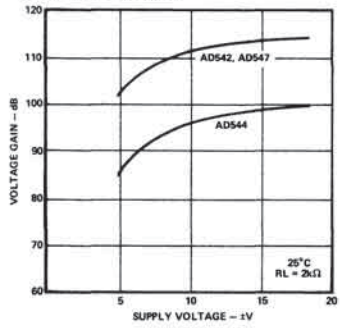


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

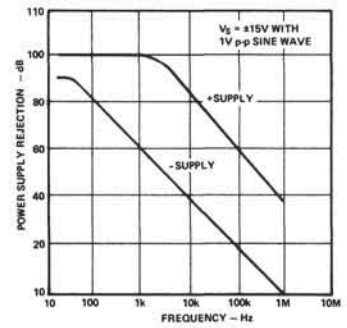


Figure 11. Power Supply Rejection vs. Frequency

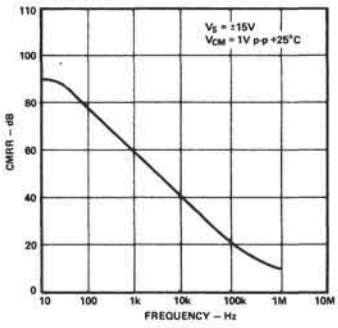


Figure 12. Common Mode Rejection Ratio vs. Frequency

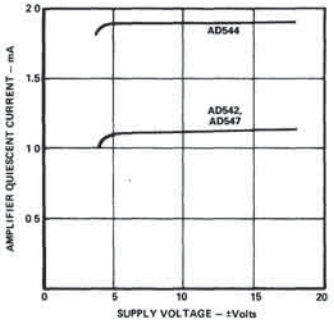


Figure 13. Quiescent Current vs. Supply Voltage

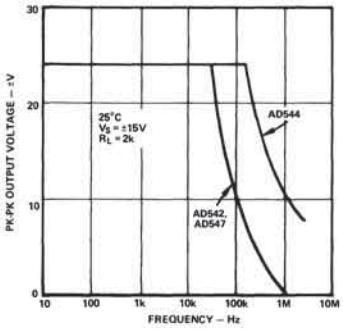


Figure 14. Large Signal Frequency Response

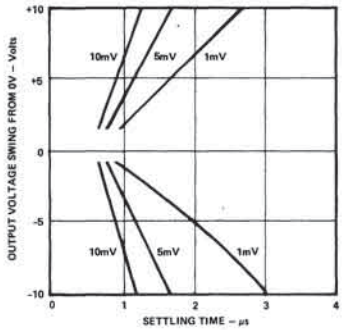


Figure 15. AD544 Output Settling Time vs. Output Swing and Error

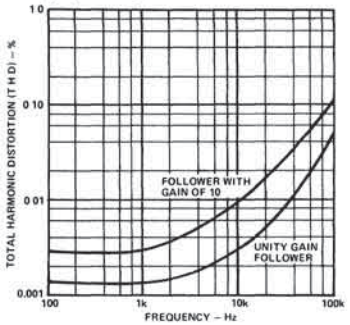


Figure 16. AD544 Total Harmonic Distortion vs. Frequency

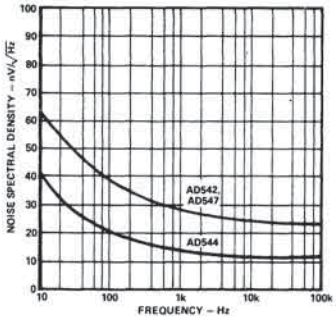


Figure 17. Input Noise Voltage Spectral Density

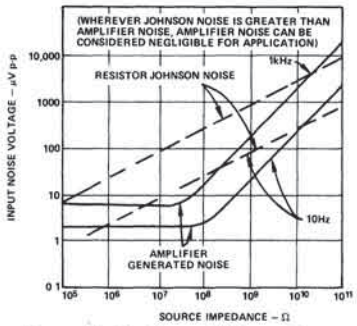
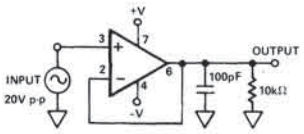
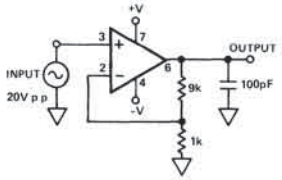


Figure 18. Total rms Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

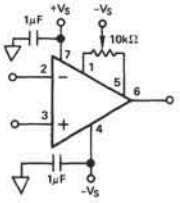


Figure 20. Standard Null Circuit

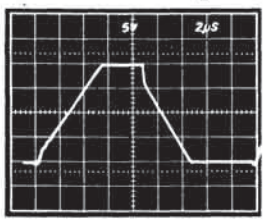


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

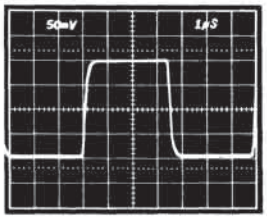


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

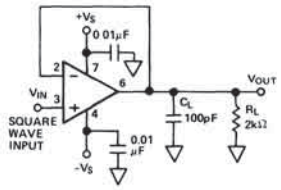


Figure 21c. Unity Gain Follower–AD542/AD547

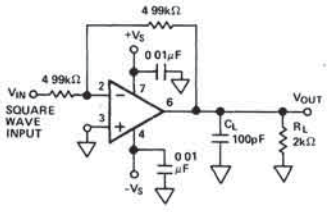


Figure 22a. Unity Gain Inverter–AD542/AD547

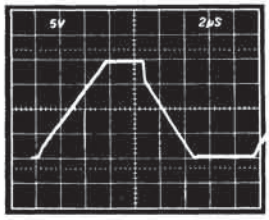


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

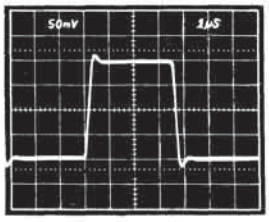


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

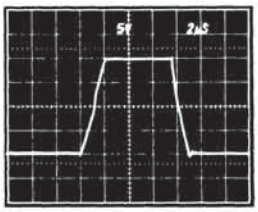


Figure 23a. Unity Gain Follower Pulse Response (Large Signal)

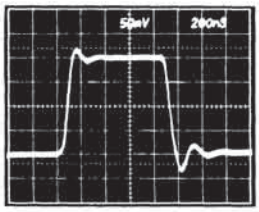


Figure 23b. Unity Gain Follower Pulse Response (Small Signal)

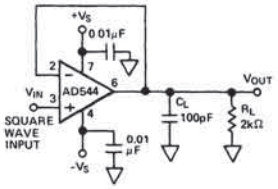


Figure 23c. Unity Gain Follower

2

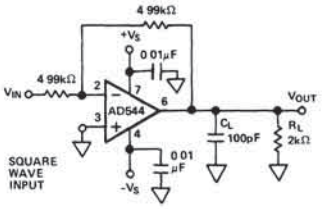


Figure 24a. Unity Gain Inverter

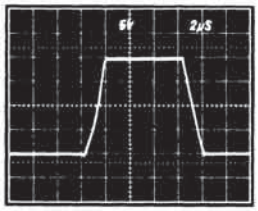


Figure 24b. Unity Gain Inverter Pulse Response (Large Signal)

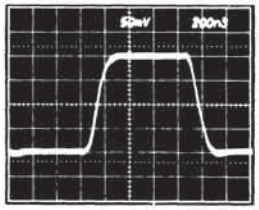


Figure 24c. Unity Gain Inverter Pulse Response (Small Signal)

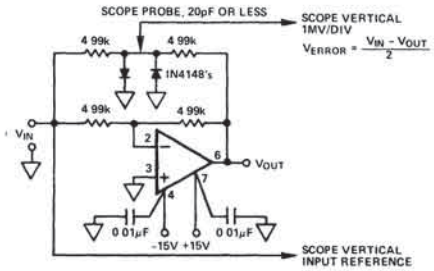


Figure 25. Settling Time Test Circuit

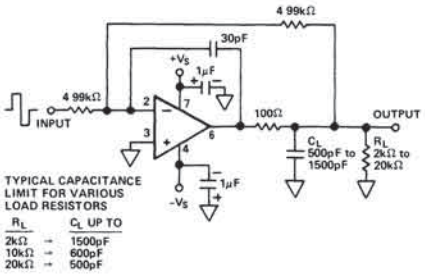


Figure 27. Circuit for Driving a Large Capacitance Load

The upper trace of the oscilloscope photograph of Figure 26 shows the settling characteristic of the AD544. The lower trace represents the input to Figure 27. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

The circuit in Figure 27 employs a 100Ω isolation resistor which enables the amplifier to drive capacitance loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

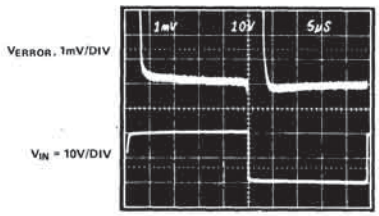


Figure 26. Settling Characteristic Detail – AD544

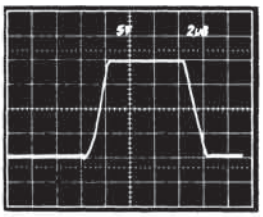


Figure 28. Transient Response $R_L = 2k\Omega$ $C_L = 500pF$–AD544

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for 10V Step
AD542JH	2.0mV	20μV/°C	5μs
AD542KH	1.0mV	10μV/°C	5μs
AD542LH	0.5mV	5μV/°C	5μs
AD542SH	1.0mV	15μV/°C	5μs
AD547JH	1.0mV	5μV/°C	5μs
AD547KH	0.5mV	2μV/°C	5μs
AD547LH	0.25mV	1μV/°C	5μs
AD547SH	0.5mV	5μV/°C	5μs
AD544JH	2.0mV	20μV/°C	3μs
AD544KH	1.0mV	10μV/°C	3μs
AD544LH	0.5mV	5μV/°C	3μs
AD544SH	1.0mV	15μV/°C	3μs

BiFET Application Hints

APPLICATION NOTES

The BiFET series was designed for high performance op-amp applications that require true dc precision. To capitalize on all of the performance available from the BiFETs there are some practical error sources that should be considered.

The bias currents of JFET input amplifiers double with every 10°C increase in chip temperature. Therefore, minimizing the junction temperature of the chip will result in extending the performance limits of the device.

1. Heat dissipation due to power consumption is the main contributor to self-heating and can be minimized by reducing the power supplies to the lowest level allowed by the application.
2. The effects of output loading should be carefully considered. Greater power dissipation increases bias currents and decreases open loop gain.

GUARDING

The low input bias current (25pA) and low noise characteristics of the high performance BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from these amplifiers. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit.

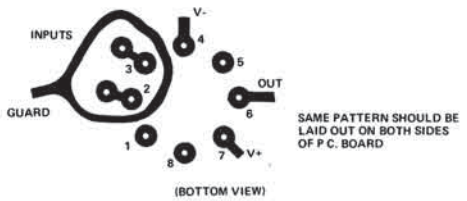


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The BiFET series is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the BiFET series suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The BiFET series requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

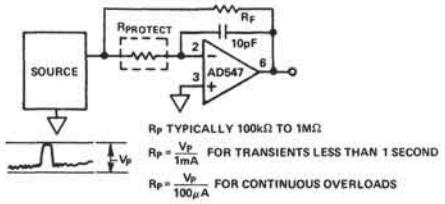


Figure 30. Input Protection

D/A CONVERTER APPLICATIONS

The BiFET series of operational amplifiers can be used with CMOS DACs to perform both 2-quadrant and 4-quadrant operation. The output impedance of a CMOS DAC varies with the digital word, thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The BiFET series with trimmed offset will minimize this effect. Additionally, the Schottky protection diodes recommended for use with many older CMOS DACs are not required when using one of the BiFET series amplifiers.

Figure 31a shows the AD547 and AD7541 configured for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit operates as a unipolar converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

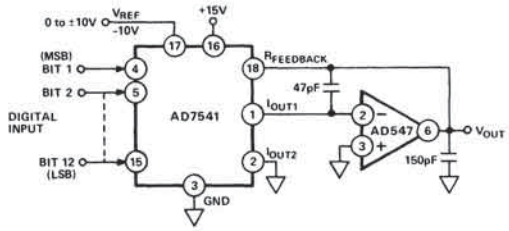


Figure 31a. AD547 Used as DAC Output Amplifier

The oscilloscope photo of Figure 31b shows the output of the circuit of Figure 31a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC (Gain $1-2^{-n}$). The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

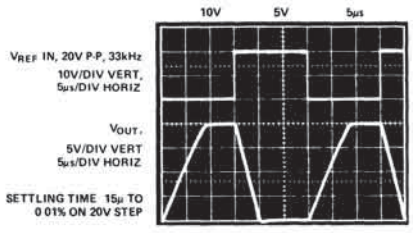


Figure 31b. Voltage Output DAC Settling Characteristic

Figure 32a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function.

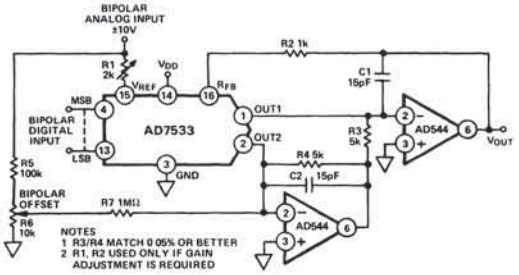


Figure 32a. AD544 Used as DAC Output Amplifiers

The photos exhibit the response to a step input at V_{REF}. Figure 32b is the large signal response and Figure 32c is the small signal response. C1 phase compensation (15pF) is required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and the output capacitance of the DAC.

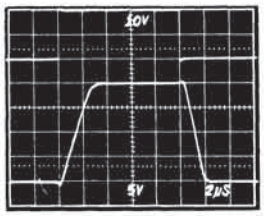


Figure 32b. Large Signal Response

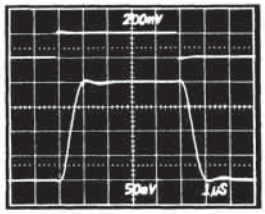


Figure 32c. Small Signal Response

USING THE AD547 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD547 make it suitable for wide dynamic range log amplifiers. Figure 33 is a schematic of a log ratio circuit employing the AD547 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

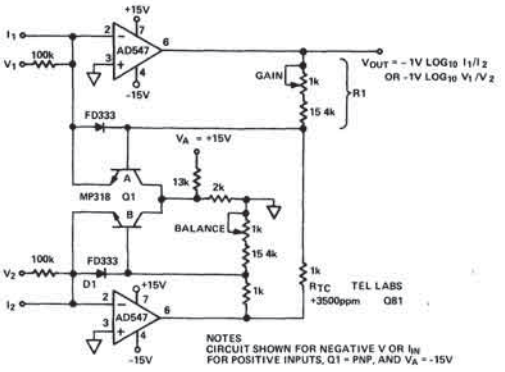


Figure 33. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{Kkt}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\ kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The −3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = −10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = −10.00V, V2 = −1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

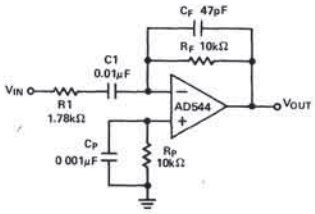


Figure 34. Differentiator

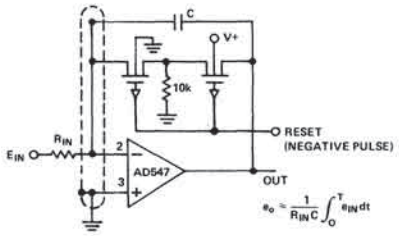


Figure 35. Low Drift Integrator and Low-Leakage Guarded Reset

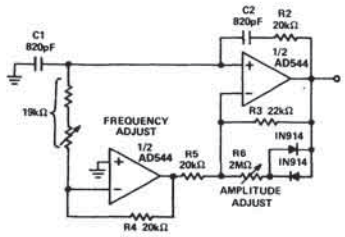


Figure 36. Wien-Bridge Oscillator – f_o = 10kHz

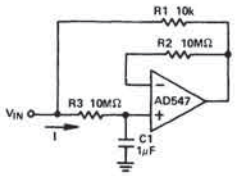


Figure 37. Capacitance Multiplier

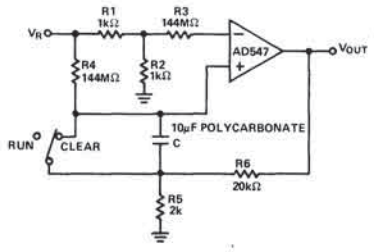


Figure 38. Long Interval Timer – 1,000 Seconds

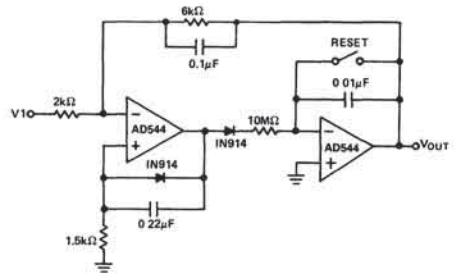


Figure 39. Positive Peak Detector

Precision, Low-Power BiFET Op Amp

AD548

FEATURES

DC Performance:
- **200μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD548C)**
- **250μV max Offset Voltage (AD548C)**
- **2μV/°C max Drift (AD548C)**
- **2μV p-p Noise, 0.1 to 10Hz**

AC Performance:
- **1.8 V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

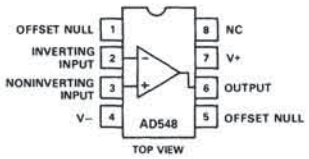
Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages

MIL-STD-883B Parts Available

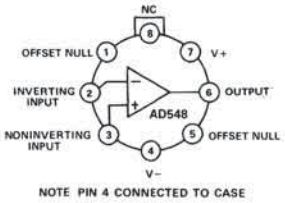
Dual Version Available: AD648

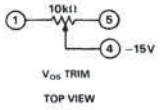
AD548 CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



TO-99
(H) Package





PRODUCT DESCRIPTION

The AD548 is a low-power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The AD548S and AD548T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, small outline or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. The AD548 is available in chip form.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD548J/A/S			AD548K/B/T			AD548C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	**2.0**		0.3	**0.5**		0 10	**0.25**	mV
T_{min} to T_{max}			3.0/3.0/**3.0**			**0.7/0.8/1.0**			**0.4**	mV
vs Temp.			20			5			**2.0**	µV/°C
vs. Supply			**80**			**86**			**86**	dB
vs. Supply, T_{min} to T_{max}			76/76/**76**			**80**			**80**	dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0 65/10			0 65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			**15**			**15**	pA
Offset Current, V_{CM} = 0		5	**10**		2	5		2	5	pA
Offset Current at T_{max}			0.25/0 65/10			0 15/0.35/5			0 35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10V	**76**	90		**82**	92		**86**	98		dB
T_{min} to T_{max}	76/76/**76**	90		**82**	92		**86**	98		dB
V_{CM} = ±11V	**70**	84		**76**	86		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	84		**76**	86		**76**	90		dB
INPUT VOLTAGE NOISE										
Voltage 0 1Hz to 10Hz		2			2			2	**4.0**	µV p-p
f = 10Hz		80			80			80		nV/√Hz
f = 100Hz		40			40			40		nV/√Hz
f = 1kHz		30			30			30		nV/√Hz
f = 10kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		1.8			1 8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0 8	1 0		0 8	1.0		0 8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1 8		**1.0**	1 8		**1.0**	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 10k\Omega$	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10k\Omega$	300/300/**300**	700		**300**	700		**300**	700		V/mV
V_O = ±10V, $R_L \geq 5k\Omega$	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq 5k\Omega$	150/150/**150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10k\Omega$,	**±12**	±13		**±12**	±13		**±12**	±13		V
T_{min} to T_{max}	±12/±12/**±12**			**±12**			**±12**			
Voltage @ $R_L \geq 5k\Omega$,	**±11**	±12 3		**±11**	±12 3		**±11**	±12 3		V
T_{min} to T_{max}	±11/±11/**±11**			**±11**			**±11**			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		170	**200**		170	**200**		170	**200**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD548J			AD548K					
Industrial (−40°C to +85°C)		AD548A			AD548B			AD548C		
Military (−55°C to +125°C)		AD548S			AD548T					
PACKAGE OPTIONS[4]										
Plastic (N-8)		AD548JN			AD548KN					
Cerdip (Q-8)		AD548AQ, AD548SQ			AD548BQ, AD548TQ			AD548CQ		
Metal Can (H-08A)		AD548AH, AD548SH			AD548BH, AD548TH			AD548CH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C For higher temperature, the current doubles every 10°C

[3]Defined as voltages between inputs, such that neither exceeds ±10V from ground.

[4]See Section 16 for package outline information

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test Results from those tests are used to calculate outgoing quality levels All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

ABSOLUTE MAXIMUM RATINGS[1]

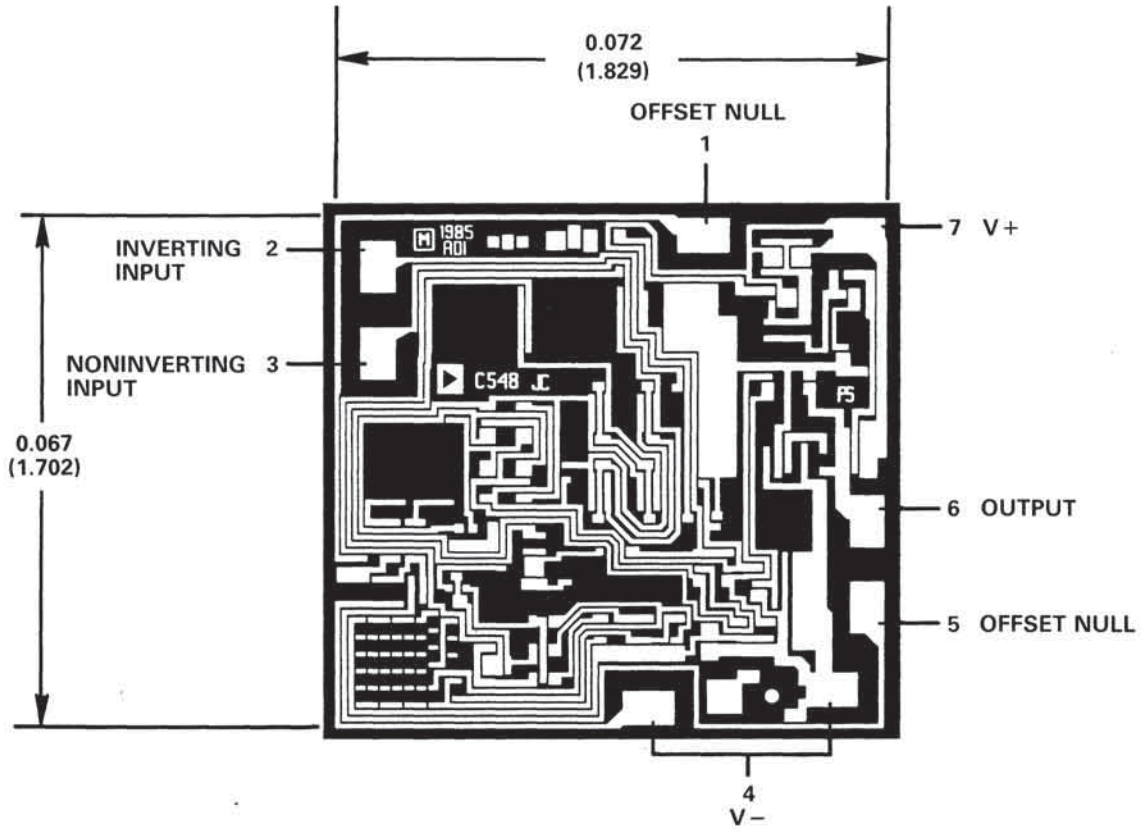
Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
N	−65°C to +125°C
Operating Temperature Range	
AD548J/K	0 to +70°C
AD548A/B/C	−40°C to +85°C
AD548S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

2

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



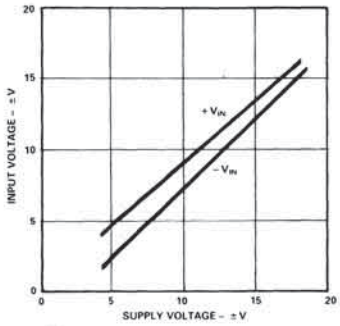


Figure 1. Input Voltage Range Vs. Supply Voltage

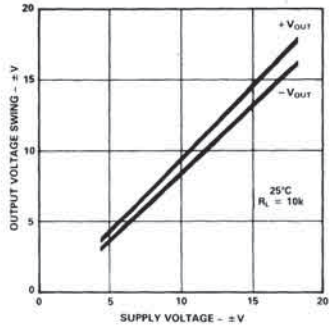


Figure 2. Output Voltage Swing Vs. Supply Voltage

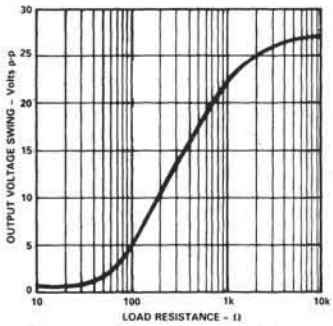


Figure 3. Output Voltage Swing vs. Resistive Load

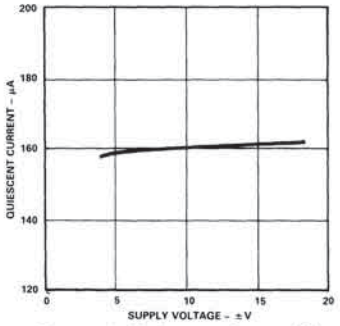


Figure 4. Quiescent Current Vs. Supply Voltage

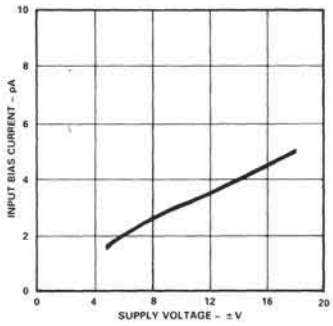


Figure 5. Input Bias Current Vs. Supply Voltage

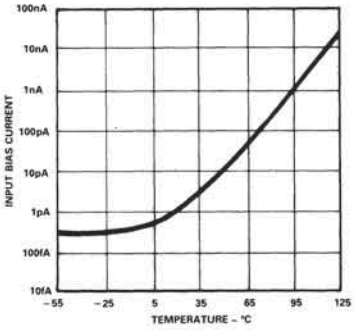


Figure 6. Input Bias Current Vs. Temperature

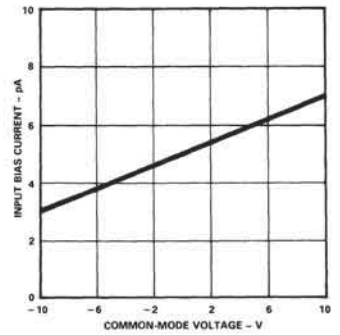


Figure 7. Input Bias Current Vs. Common-Mode Voltage

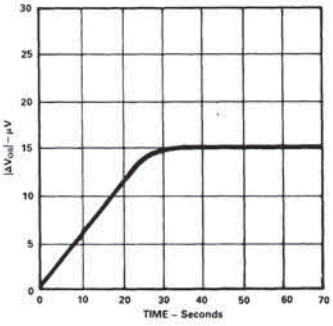


Figure 8. Change in Offset Voltage Vs. Warm-Up Time

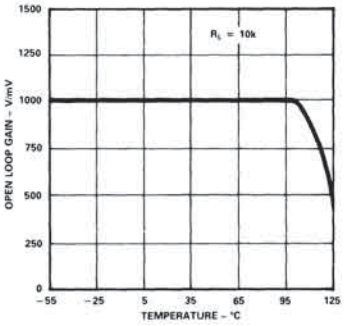


Figure 9. Open Loop Gain Vs. Temperature

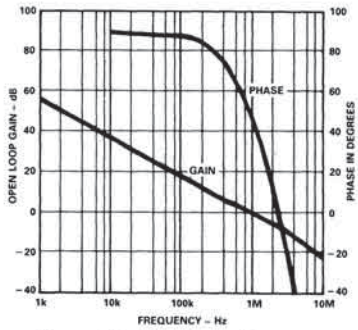


Figure 10. Open Loop Frequency Response

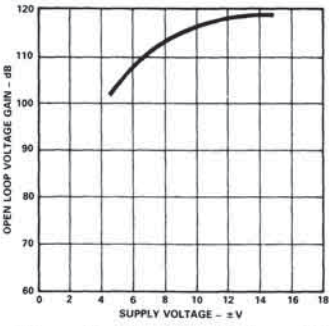


Figure 11. Open Loop Voltage Gain Vs. Supply

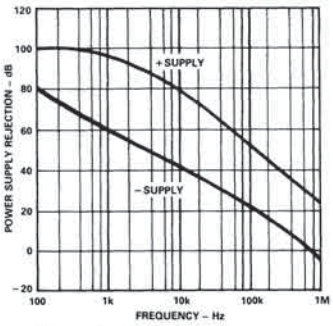


Figure 12. PSRR Vs. Frequency

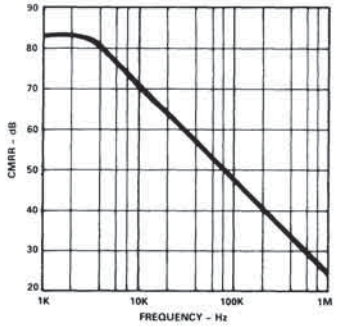


Figure 13. CMRR Vs. Frequency

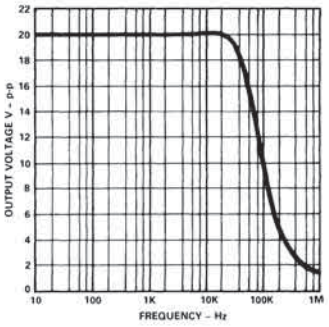


Figure 14. Large Signal Frequency Response

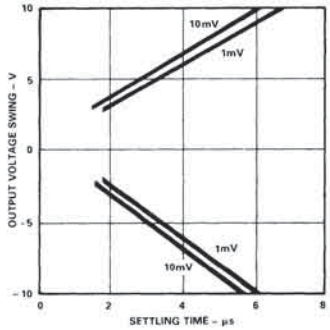


Figure 15. Output Settling Time Vs. Output Swing and Error Voltage

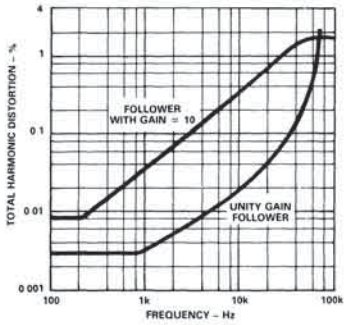


Figure 16. Total Harmonic Distortion vs. Frequency

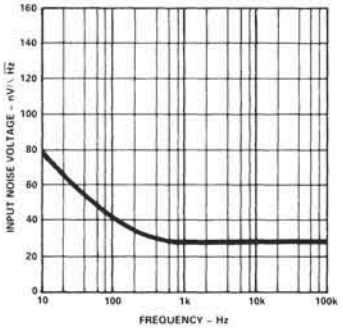


Figure 17. Input Noise Voltage Spectral Density

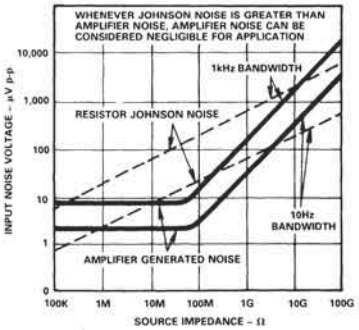


Figure 18. Total Noise Vs. Source Resistance

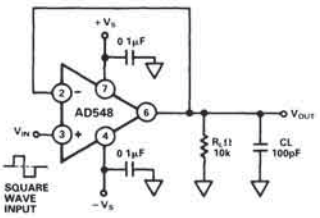


Figure 19a. Unity Gain Follower

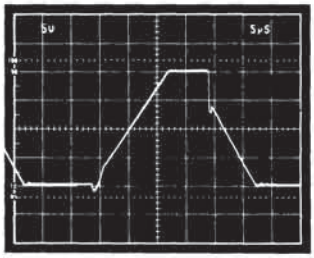


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

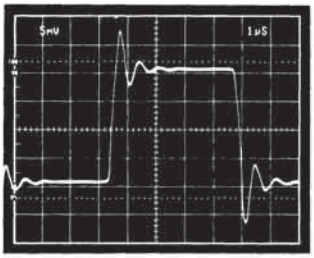


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

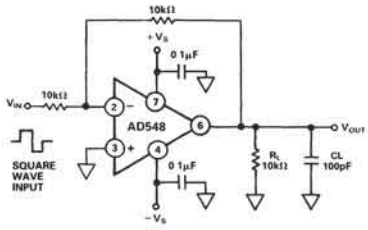


Figure 20a. Unity Gain Inverter

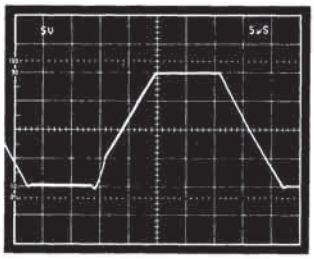


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

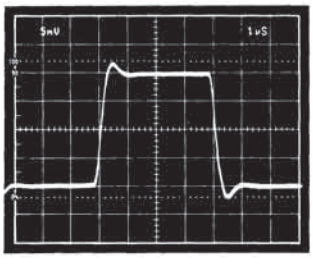


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

Applying the AD548

APPLICATION NOTES

The AD548 is a JFET-input op amp with a guaranteed maximum I_B of less than 10pA, and offset and drift laser-trimmed to 0.25mV and 2μV/°C respectively (AD548C). AC specs include 1MHz bandwidth, 1.8V/μs typical slew rate and 8μs settling time for a 20V step to ±0.01% – all at a supply current less than 200μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD548 reduce self-heating or "warm-up" effects on input offset voltage, making the AD548 ideal for on/off battery powered applications. The power dissipation due to the AD548's 200μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15V, due to power supply rejection effects. The common-mode range of the AD548 extends from 3V more positive than the negative supply to 1V more negative than the positive supply. Designed to cleanly drive up to 10kΩ and 100pF loads, the AD548 will drive a 2kΩ load with reduced open loop gain.

OFFSET NULLING

Unlike bipolar input amplifiers, zeroing the input offset voltage of a BiFET op amp will not minimize offset drift. Using balance Pins 1 and 5 to adjust the input offset voltage as shown in Figure 21 will induce an added drift of 0.24μV/°C per 100μV of nulled offset. The low initial offset (0.25mV) of the AD548C results in only 0.6μV/°C of additional drift.

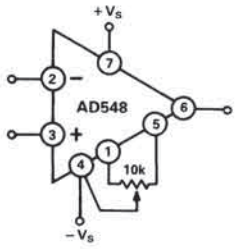


Figure 21. Offset Null Configuration

LAYOUT

To take full advantage of the AD548's 10pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between $1 \times 10^{12}\Omega$ and $3 \times 10^{12}\Omega$. This can result in an additional leakage of 5pA between an input of 0V and a −15V supply line. Teflon or a similar low leakage material (with a resistance exceeding $10^{17}\Omega$) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

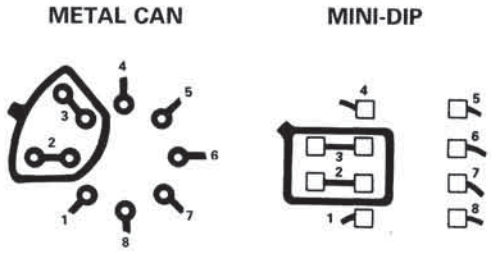


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD548 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figure 23 shows a simple current limiting scheme that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0mA (100kΩ for a 100V overload, for example).

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

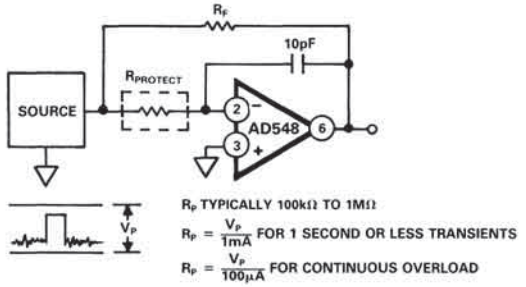


Figure 23. Input Protection of IV Converter

D/A CONVERTER OUTPUT BUFFER

The circuit in Figure 24 shows the AD548 and AD7545 12-bit CMOS D/A converter in a unipolar binary configuration. V_{OUT} will be equal to V_{REF} attenuated by a factor depending on the digital word. V_{REF} sets the full scale. Overall gain is trimmed by adjusting R_{IN}. The AD548's low input offset voltage, low drift and clean dynamics make it an attractive low power output buffer.

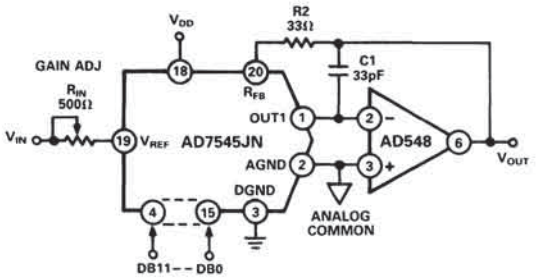


Figure 24. AD548 Used as DAC Output Amplifier

The input offset voltage of the AD548 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier. That is:

$$V_{OS}\ \text{Output} = V_{OS}\ \text{Input}\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD548 in this configuration provides a 700kHz small signal bandwidth and 1.8V/μs typical slew rate. The 33pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 25 and 26 show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The AD548 settles to ±0.01% for a 20V input step in 14μs.

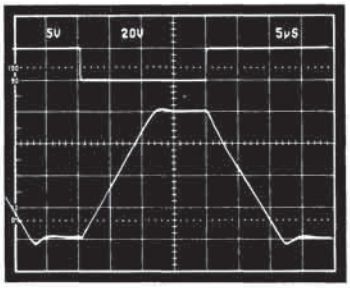


Figure 25. Response to ±20V p-p Reference Square Wave

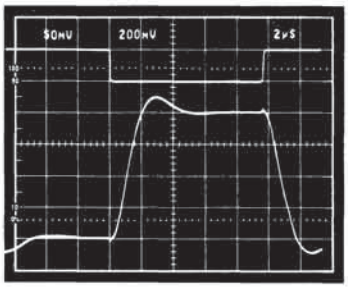


Figure 26. Response to ±100mV p-p Reference Square Wave

PHOTODIODE PREAMP

The performance of the photodiode preamp shown in Figure 27 is enhanced by the AD548's low input current, input voltage offset and offset voltage drift. The photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

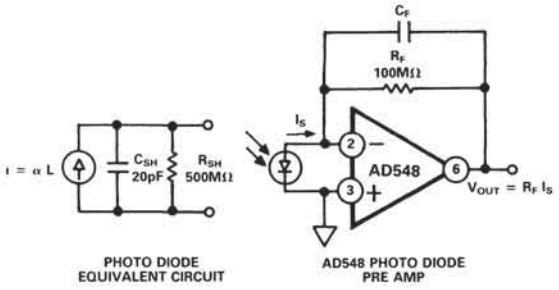


Figure 27.

An error budget illustrating the importance of low amplifier input current, voltage offset and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2mm² area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1+R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500MΩ, and the maximum input current and input offset voltage specs of an AD548C.

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1 + R_F/R_{SH})\,V_{OS}$	I_B (pA)	$I_B R_F$	TOTAL
−25	15,970	150	151μV	0.30	30μV	181μV
0	2,830	200	207μV	2.26	262μV	469μV
+25	500	250	300μV	10 00	1.0mV	1.30mV
+50	88.5	300	640μV	56.6	5.6mV	6.24mV
+75	15.6	350	2 6mV	320	32mV	34.6mV
+85	7.8	370	5.1mV	640	64mV	69.1mV

Figure 28. Photo Diode Pre-Amp Errors Over Temperature

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of bandwidth.

INSTRUMENTATION AMPLIFIER

The AD548C's maximum input current of 10pA makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

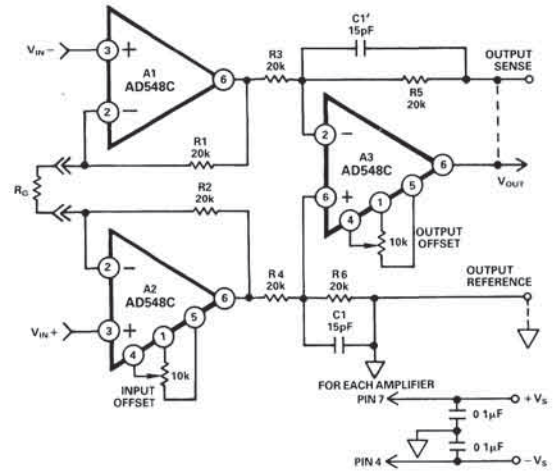


Figure 29. Low Power Instrumentation Amplifier

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_1 + R_2)}{R_G}$$

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. Referred to input errors, which contribute an output error proportional to in amp gain, include a maximum untrimmed input offset voltage of 0.5mV and an input offset voltage drift over temperature of 4μV/°C. Output errors, which are independent of gain, will contribute an additional 0.5mV offset and 4μV/°C drift. The maximum input current is 15pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. Resistor pairs R3/R5 and R4/R6 should be ratio matched to 0.01% to take full advantage of the AD548's high common mode rejection. Capacitors C1 and C1′ compensate for peaking in the gain over frequency caused by input capacitance when gains of 1 to 3 are used.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700kHz for a gain of 1 and 10kHz for a gain of 100. The typical output slew rate is 1.8V/μs.

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD548's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q) \ln (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10} (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300kHz at input currents above 100μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

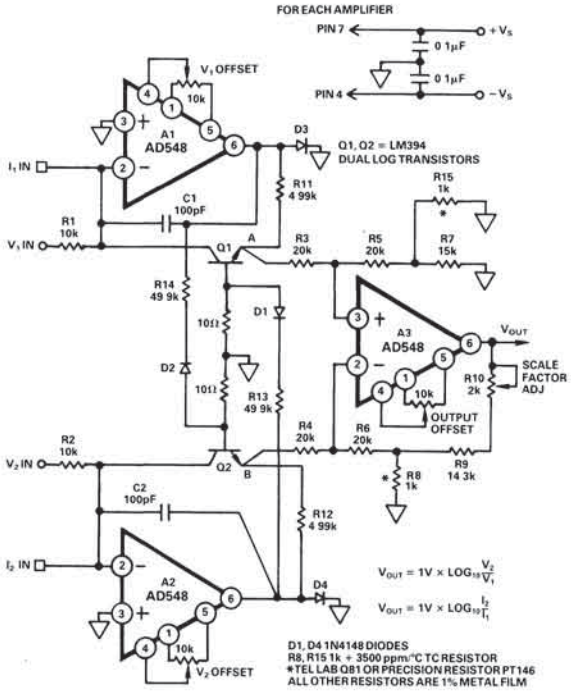


Figure 30. Log Ratio Amplifier

To trim this circuit, set the two input currents to 10μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300pA to 1mA, with low level accuracy limited by the AD548's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD548.

Monolithic Electrometer Operational Amplifier

AD549*

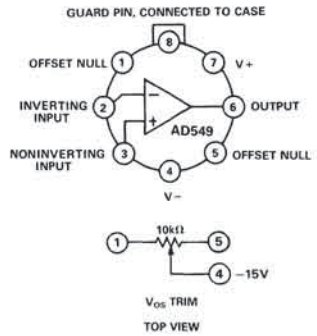
FEATURES

Ultralow Bias Current: 60fA max (AD549L)
250fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25mV max (AD549K)
1.00mV max (AD549J)
Low Offset Drift: 5μV/°C max (AD549K)
20μV/°C max (AD549J)
Low Power: 700μA max Supply Current
Low Input Voltage Noise: 4μV p-p 0.1 to 10Hz
MIL-STD-883B Parts Available

APPLICATIONS

Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

AD549 CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The $10^{15}\Omega$ common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range –0 to +70°C. The S grade is specified over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. PLUS screening includes 168-hour burn in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25mV and 5μV/°C (AD549K), 1mV and 20μV/°C (AD549J).
3. A maximum quiescent supply current of 700μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1MHz unity gain bandwidth and 3V/μs slew rate. Settling time for a 10V input step is 5μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

***Covered by Patent No. 4,639,683.**

SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10V		150	250		75	100		40	60		75	100	fA
Either Input at T_{max}, V_{CM} = 0V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{max}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	**1.0**		0.15	**0.25**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{max}			**1.9**			**0.4**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		2	**5**		5	**10**		10	**15**	μV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	μV/V
vs. Supply, T_{min} to T_{max}		32	**100**		10	**32**		10	**32**		32	**50**	μV/V
Long-Term Offset Stability		15			15			15			15		μV/month
INPUT VOLTAGE NOISE													
f = 0.1Hz to 10Hz		4			4	**6**		4			4		μV p-p
f = 10Hz		90			90			90			90		nV/√Hz
f = 100Hz		60			60			60			60		nV/√Hz
f = 1kHz		35			35			35			35		nV/√Hz
f = 10kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f = 0.1Hz to 10Hz		0.7			0.5			0.36			0.5		fA p-p
f = 1kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential V_{DIFF} = ±1		10^{13}‖1			10^{13}‖1			10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode V_{CM} = ±10		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN LOOP GAIN													
V_O @ ±10V, R_L = 10k	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_O @ ±10V, R_L = 10k, T_{min} to T_{max}	**300**	800		**300**	800		**300**	800		**300**	800		V/mV
V_O = ±10V, R_L = 2k	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
V_O = ±10V, R_L = 2k, T_{min} to T_{max}	**80**	200		**80**	200		**80**	200		**25**	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Common-Mode Rejection Ratio													
V = +10V, −10V	**80**	90		**90**	100		**90**	100		**90**	100		dB
T_{min} to T_{max}	**76**	80		**80**	90		**80**	90		**80**	90		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10k, T_{min} to T_{max}	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	V
Voltage @ R_L = 2k, T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Short Circuit Current	15	20	35	15	20	35	15	20	35	15	20	35	mA
T_{min} to T_{max}	**9**			**9**			**9**			**6**			mA
Load Capacitance Stability G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/μs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		μs
0.01%		5			5			5			5		μs
Overload Recovery, 50% Overdrive, G = −1		2			2			2			2		μs
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TEMPERATURE RANGE													
Operating, Rated Performance	0		70	0		70	0		70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		−150	°C
PACKAGE OPTION[4]													
TO-99 (H-08A)		AD549JH			AD549KH			AD549LH			AD549SH		

NOTES
[1]Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifictions are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between the inputs such that neither input exceeds ±10V from ground.
[4]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

2

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 500mW
Input Voltage . . . . . ±18V[2]
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range H . . . . . −65°C to +150°C
Operating Temperature Range
AD549J, K, L . . . . . 0 to +70°C
AD549S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

ESD PRECAUTIONS

Charges as high as 4000V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

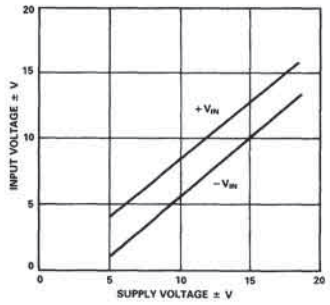


Figure 1. Input Voltage Range vs. Supply Voltage

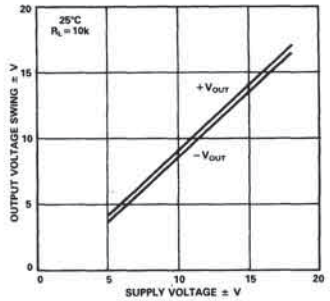


Figure 2. Output Voltage Swing vs. Supply Voltage

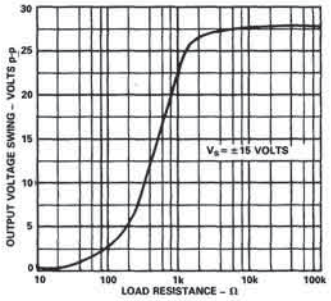


Figure 3. Output Voltage Swing vs. Resistive Load

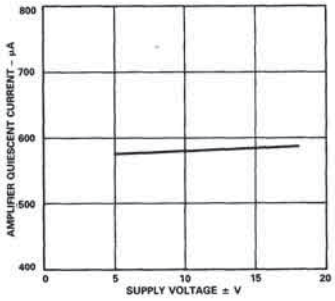


Figure 4. Quiescent Current vs. Supply Voltage

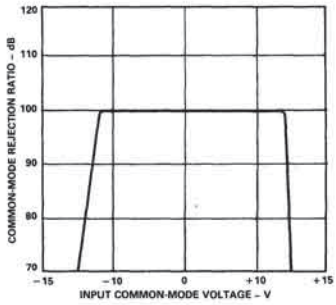


Figure 5. CMRR vs. Input Common-Mode Voltage

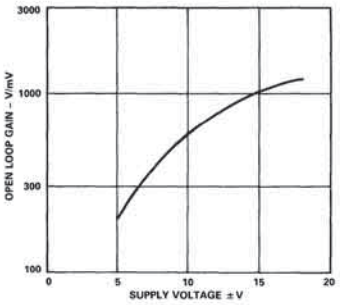


Figure 6. Open Loop Gain vs. Supply Voltage

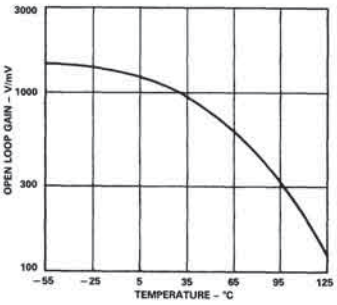


Figure 7. Open Loop Gain vs. Temperature

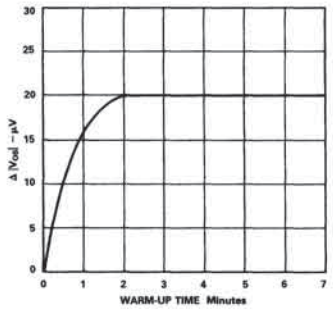


Figure 8. Change in Offset Voltage vs. Warm-Up Time

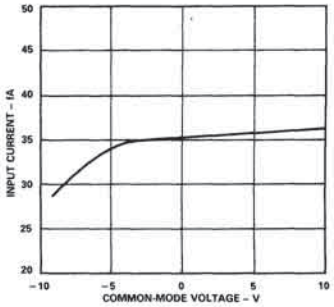


Figure 9. Input Bias Current vs. Common-Mode Voltage

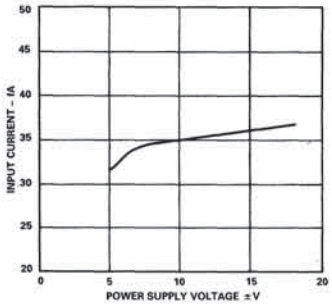


Figure 10. Input Bias Current vs. Supply Voltage

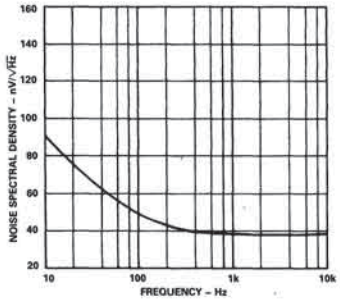


Figure 11. Input Voltage Noise Spectral Density

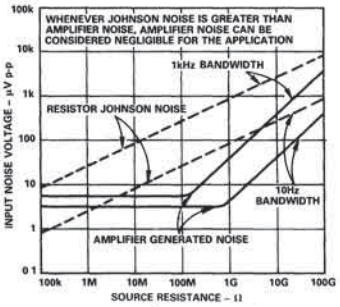


Figure 12. Noise vs. Source Resistance

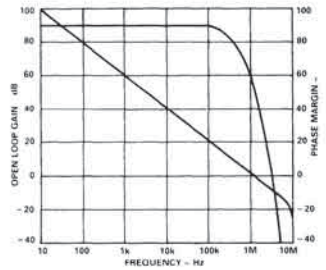


Figure 13. Open Loop Frequency Response

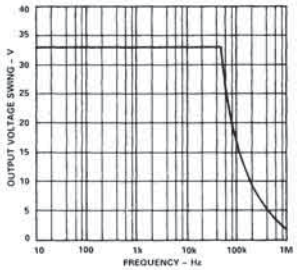


Figure 14. Large Signal Frequency Response

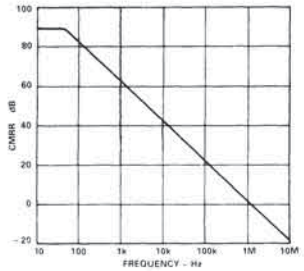


Figure 15. CMRR vs. Frequency

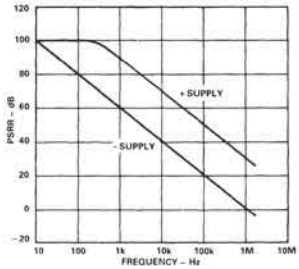


Figure 16. PSRR vs. Frequency

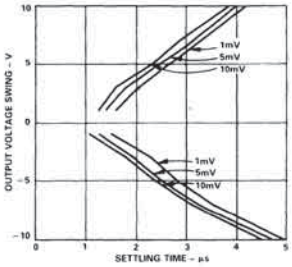


Figure 17. Output Settling Time vs. Output Swing and Error Voltage

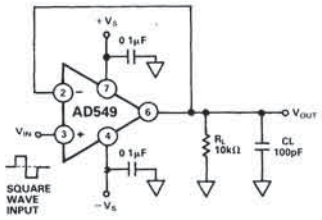


Figure 18. Unity Gain Follower

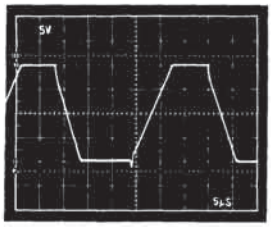


Figure 19. Unity Gain Follower Large Signal Pulse Response

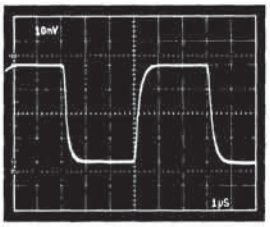


Figure 20. Unity Gain Follower Small Signal Pulse Response

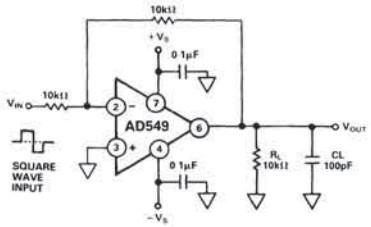


Figure 21. Unity Gain Inverter

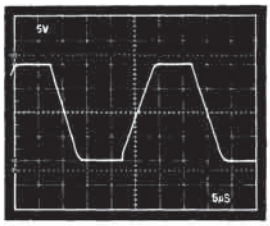


Figure 22. Unity Gain Inverter Large Signal Pulse Response

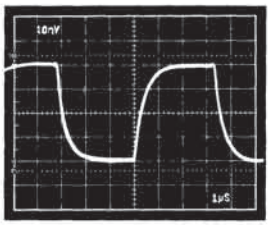


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD549 has been optimized for low input current and offset voltage. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD549's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD549 input current versus ambient temperature.

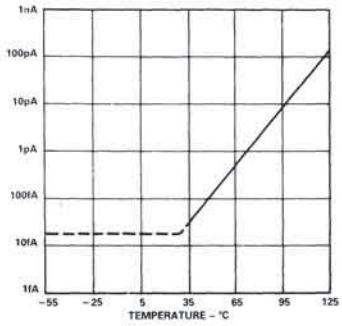


Figure 24. AD549 Input Bias Current vs. Ambient Temperature

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD549's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10kΩ is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

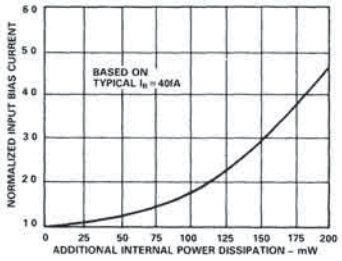


Figure 25. AD549 Input Bias Current vs. Additional Power Dissipation

CIRCUIT BOARD NOTES

There are a number of physical phenomena that generate spurious currents that degrade the accuracy of low current measurements. Figure 26 is a schematic of an I-to-V converter with these parasitic currents modeled.

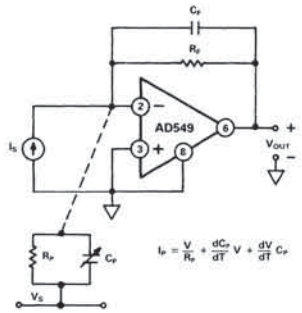


Figure 26. Sources of Parasitic Leakage Currents

Finite resistance from input lines to voltages on the board, modeled by resistor R_P, results in parasitic leakage. Insulation resistance of over $10^{15}\Omega$ must be maintained between the amplifier's signal and supply lines in order to capitalize on the AD549's low input currents. Standard PC board material does not have high enough insulation resistance. Therefore, the AD549's input leads should be connected to standoffs made of insulating material with adequate volume resistivity (e.g., Teflon*). The surface of the insulator's surface must be kept clean in order to preserve surface resistivity. For Teflon, an effective cleaning procedure consists of swabbing the surface with high-grade isopropyl alcohol, rinsing with deionized water, and baking the board at 80°C for 10 minutes.

In addition to high volume and surface resistivity, other properties are desirable in the insulating material chosen. Resistance to water absorption is important since surface water films drastically reduce surface resistivity. The insulator chosen should also exhibit minimal piezoelectric effects (charge emission due to mechanical stress) and triboelectric effects (charge generated by friction). Charge imbalances generated by these mechanisms can appear as parasitic leakage currents. These effects are modeled by variable capacitor C_P in Figure 26. The table in Figure 27 lists various insulators and their properties.[1]

Material	Volume Resistivity (Ω – CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon	$10^{17}-10^{18}$	W	W	G
Kel-F**	$10^{17}-10^{18}$	W	M	G
Sapphire	$10^{16}-10^{18}$	M	G	G
Polyethylene	$10^{14}-10^{18}$	M	G	M
Polystyrene	$10^{12}-10^{18}$	W	M	M
Ceramic	$10^{12}-10^{14}$	W	M	W
Glass Epoxy	$10^{10}-10^{17}$	W	M	W
PVC	$10^{10}-10^{15}$	G	M	G
Phenolic	$10^{9}-10^{12}$	W	G	W

G – Good with Regard to Property
M – Moderate with Regard to Property
W – Weak with Regard to Property

Figure 27. Insulating Materials and Characteristics

[1]Electrometer Measurements, pp. 15-17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.

*Teflon is a registered trademark of E.I. du Pont Co.

**Kel-F is a registered trademark of 3-M Company.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced since the voltage between the input line and the guard is very low. Second, stray capacitance at the input node is minimized. Input capacitance can substantially degrade signal bandwidth and the stability of the I-to-V converter. The case of the AD549 is connected to Pin 8 so that it can be bootstrapped near the input potential. This minimizes pin leakage and input common-mode capacitance due to the case. Guard schemes for inverting and noninverting amplifier topologies are illustrated in Figures 28 and 29.

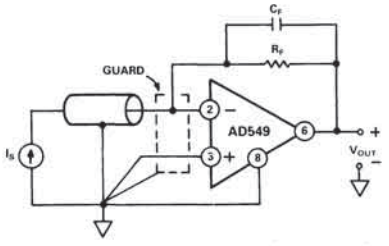


Figure 28. Inverting Amplifier with Guard

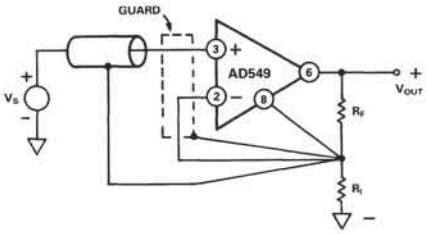


Figure 29. Noninverting Amplifier with Guard

Other guidelines include keeping the circuit layout as compact as possible and input lines short. Keeping the assembly rigid and minimizing sources of vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding against interference noise. Low noise coax or triax cables should be used for remote connections to the input signal lines.

OFFSET NULLING

The AD549's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 30. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4μV/°C per millivolt of nulled offset (a maximum additional drift of 0.6μV/°C for the AD549K, 1.2μV/°C for the AD549L, 2.4μV/°C for the AD549J).

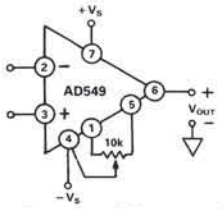


Figure 30. Standard Offset Null Circuit

The approach in Figure 31 can be used when the amplifier is used as an inverter. This method introduces a small voltage referenced to the power supplies in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

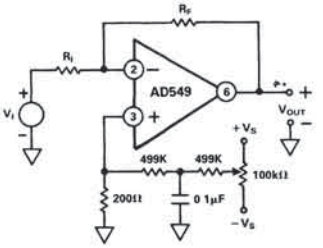


Figure 31. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100kΩ will magnify the effect of input capacitances (stray and inherent to the AD549) on the ac behavior of the circuit. The effects of common mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance and input common-mode capacitance form a pole that limits the bandwidth to $1/2\pi\ R_S C_S$. Bootstrapping the metal case by connecting Pin 8 to the output minimizes capacitance due to the package. Figures 32 and 33 show the follower pulse response from a 1MΩ source resistance with and without the package connected to the output. Typical common-mode input capacitance for the AD549 is 0.8pF.

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1MΩ appears in Figure 34. Figure 35 shows the response of the same circuit with a 1pF feedback capacitance. Typical differential input capacitance for the AD549 is 1pF.

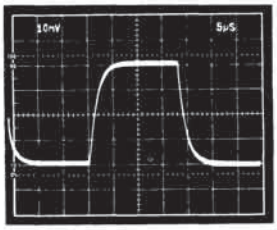


Figure 32. Follower Pulse Response from 1 MΩ Source Resistance, Case Not Bootstrapped

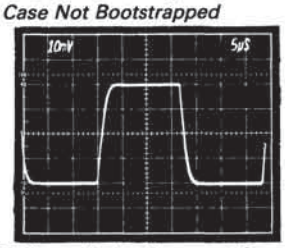


Figure 33. Follower Pulse Response from 1 MΩ Source Resistance, Case Bootstrapped

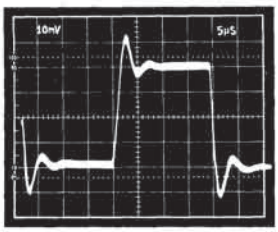


Figure 34. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

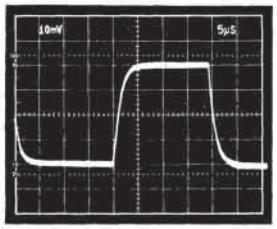


Figure 35. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1pF Feedback Capacitance

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD549 is from 3V less than the positive supply voltage to 5V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common-mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2µs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5µs of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD549's input currents versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 36. The input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 to 1.5V above the other terminal. Under these conditions, the input current limits at 30µA.

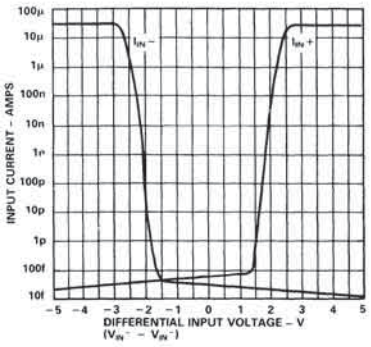


Figure 36. Input Current vs. Differential Input Voltage

INPUT PROTECTION

The AD549 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 37. R_P is chosen to limit the current through the inverting input to 1mA for expected transient (less than 1 second) overvoltage conditions, or to 100µA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's DC gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

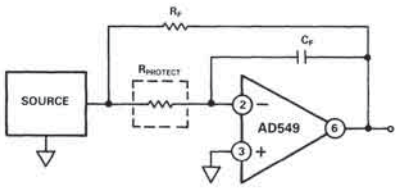


Figure 37. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 38, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a $f = 1/2\pi RC$. Again, the Johnson noise R_P will add to the amplifier's input voltage noise.

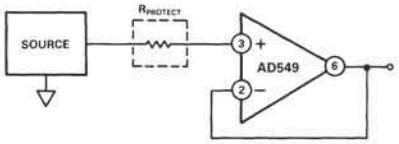


Figure 38. Follower with Input Current Limit

Figure 39 is a schematic of the AD549 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes, such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

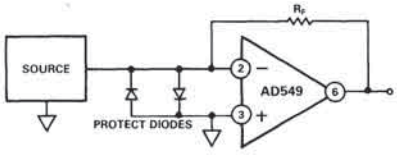


Figure 39. Input Voltage Clamp with Diodes

SAMPLE AND DIFFERENCE CIRCUIT TO MEASURE ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physical layout are essential to making accurate leakage measurements.

Figure 40 is a schematic of the sample and difference circuit. It uses two AD549 electrometer amplifiers (A and B) as current to voltage converters with high value ($10^{10}\Omega$) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10fA/mV (10pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low-leakage polystyrene capacitor. An ultralow-leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

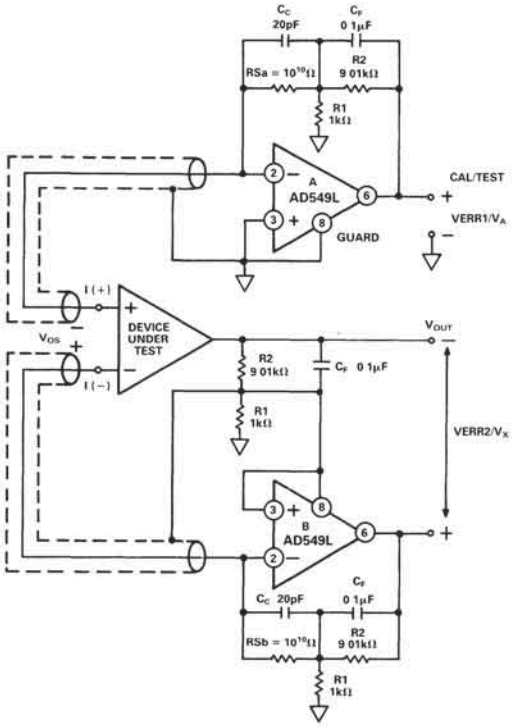


Figure 40. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\,(V_{OS}A - I_BA \times RSa)$$
$$V_{ERR2} = 10\,(V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$
$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current to voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD549's low input current and low input offset voltage make it an excellent choice for very sensitive photodiode preamps (Figure 41). The photodiode develops a signal current, I_S equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in Watts and R is the photodiode responsivity in Amps/Watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

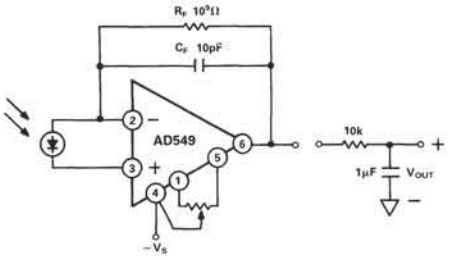


Figure 41. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2mm square) photodiode are indicated in Figure 42.

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

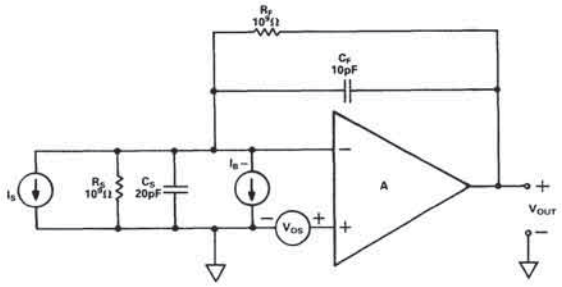


Figure 42. Photodiode Preamp DC Error Sources

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (1+R_F/R_S)\, V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of $10^9\Omega$), R_F/R_S can easily be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift must be used in order to maintain accuracy. The AD549K offers guaranteed maximum 0.25mV offset voltage, and 5μV/°C drift for very sensitive applications.

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 43; Figure 44 is the spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 42 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

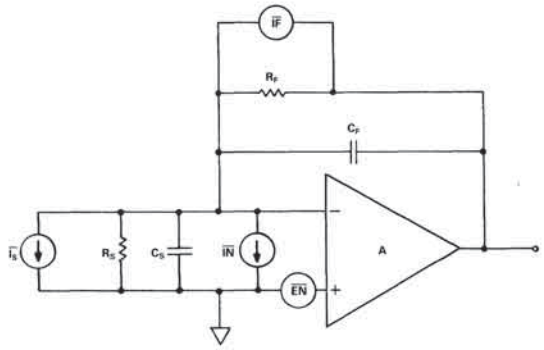


Figure 43. Photodiode Preamp Noise Sources

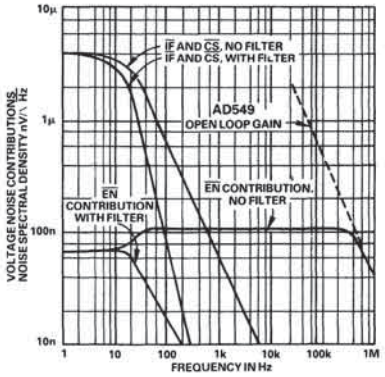


Figure 44. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

The photodiode preamp in Figure 41 can detect a signal current of 26fA rms at a bandwidth of 16Hz, which assuming a photodiode responsivity of 0.5A/W, translates to a 52fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

Log Ratio Amplifier

Logarithmic ratio circuits are useful for processing signals with wide dynamic range. The AD549L's 60fA maximum input current makes it possible to build a log ratio amplifier with 1% log conformance for input current ranging from 10pA to 1mA, a dynamic range of 160dB. The useful resolution of the log amplifier extends down to 100fA, for a total dynamic range of 10 decades or 200dB.

The log ratio amplifier in Figure 45 provides an output voltage proportional to the log base 10 of the ratio of the input currents I1 and I2. Resistors R1 and R2 are provided for voltage inputs. Since NPN devices are used in the feedback loop of the front-end amplifiers that provide the log transfer function, the output is valid only for positive input voltages and input currents. The input currents set the collector currents IC1 and IC2 of a matched pair of log transistors Q1 and Q2 to develop voltages VA and VB:

$$VA, B = -(kT/q) \ln IC/IES$$

where IES is the transistors' saturation current.

The difference of VA and VB is taken by the subtractor section to obtain:

$$VC = (kT/q) \ln (IC2/IC1)$$

VC is scaled up by the ratio of (R9 + R10)/R8, which is equal to approximately 16 at room temperature, resulting in the output voltage:

$$V_{OUT} = 1 \times \log(IC2/IC1)\ V.$$

R8 is a resistor with a positive 3500ppm/°C temperature coefficient to provide the necessary temperature compensation. The parallel combination of R15 and R7 is provided to keep the subtractor section's gain for positive and negative inputs matched over temperature.

Frequency compensation is provided by R11, R12, and C1 and C2. The bandwidth of the circuit is 300kHz at input signals greater than 50μA, and decreases smoothly with decreasing signal levels.

To trim the circuit, set the input currents to 10μA and trim A3's offset using the amplifier's trim potentiometer so the output equals 0. Then set I1 to 1μA and adjust the output to equal 1V by trimming R10. Additional offset trims on the amplifiers A1 and A2 can be used to increase the voltage input accuracy and dynamic range.

The very low input current of the AD549 makes this circuit useful over a very wide range of signal currents. The total input current (which determines the low-level accuracy of the circuit) is the sum of the amplifier input current, the leakage across the compensating capacitor (negligible if polystyrene or Teflon capacitor is used), and the collector to collector, and collector to base leakages of one side of the dual log transistors. The magnitude of these last two leakages depend on the amplifier's input offset voltage and are typically less than 10fA with 1mV offsets. The low-level accuracy is limited primarily by the amplifier's input current, only 60fA maximum when the AD549L is used.

The effects of the emitter resistance of Q1 and Q2 can degrade the circuit's accuracy at input currents above 100μA. The networks composed of R13, D1, R16, and R14, D2, R17 compensate for these errors, so that this circuit has less than 1% log conformance error at 1mA input currents. The correct value for R13 and R14 depends on the type of log transistors used. 49.9kΩ resistors were chosen for use with LM394 transistors. Smaller resistance values will be needed for smaller log transistors.

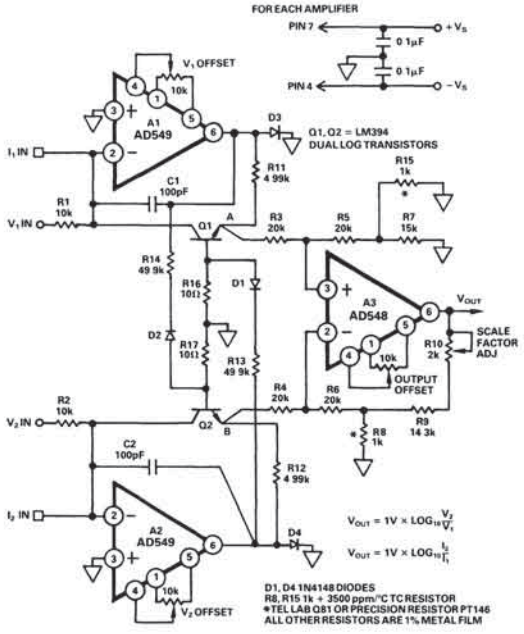


Figure 45. Log Ratio Amplifier

TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and $10^9\Omega$. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 46 illustrates the use of the AD549 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD549's low input current. If an AD549L (60fA max input current) is used, the error contributed by input current will be held below 60μV for pH electrode source impedances up to $10^9\Omega$. Input offset voltage (which can be trimmed) will be below 0.5mV.

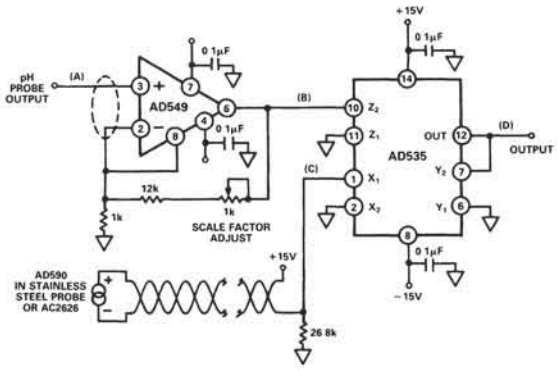


Figure 46. Temperature Compensated pH Probe Amplifier

The pH probe output is ideally zero volts at a pH of 7 independent of temperature. The slope of the probe's transfer function, though predictable, is temperature dependent (−54.2mV/pH at 0 and −74.04mV/pH at 100°C). By using an AD590 temperature sensor and an AD535 analog divider, an accurate temperature compensation network can be added to the basic pH probe amplifier. The table in Figure 47 shows voltages at various points and illustrates the compensation. The AD549 is set for a noninverting gain of 13.51. The output of the AD590 circuitry (point C) will be equal to 10V at 100°C and decrease by 26.8mV/°C. The output of the AD535 analog divider (point D) will be a temperature compensated output voltage centered at zero volts for a pH of 7, and having a transfer function of −1.00V/pH unit. The output range spans from −7.00V (pH = 14) to +7.00V (pH = 0).

PROBE TEMP	A (PROBE OUTPUT)	B (A × 13.51)	C (590 OUTPUT)	D (10B/C)
0	54.20mV	0.732V	7.32V	1.00V
25°C	59.16mV	0.799V	7.99V	1.00V
37°C	61.54mV	0.831V	8.31V	1.00V
60°C	66.10mV	0.893V	8.93V	1.00V
100°C	74.04mV	1.000V	10.00V	1.00V

Figure 47. Table Illustrating Temperature Compensation

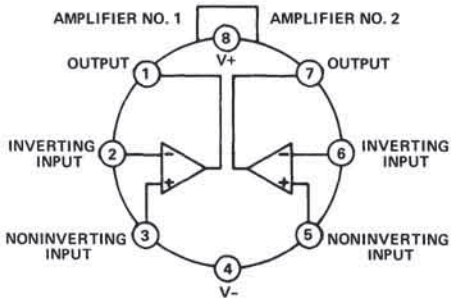
Precision Low-Cost Dual BiFET Op Amp

AD642

FEATURES

- **Matched Offset Voltage**
- **Matched Offset Voltage Over Temperature**
- **Matched Bias Current**
- **Crosstalk-124dB at 1kHz**
- **Low Bias Current: 35pA max Warmed Up**
- **Low Offset Voltage: 500μV max**
- **Low Input Voltage Noise: 2μV p-p**
- **High Open Loop Gain**
- **Low Quiescent Current: 2.8mA max**
- **Low Total Harmonic Distortion**
- **Standard Dual Amplifier Pin Out**

AD642 PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high-speed monolithic BiFET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to product matched bias currents which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low-cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C extented operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.
6. The AD642 is available in chip form.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD642J Min	AD642J Typ	AD642J Max	AD642K Min	AD642K Typ	AD642K Max	AD642L Min	AD642L Typ	AD642L Max	AD642S Min	AD642S Typ	AD642S Max	Units
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		±12	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		10			10			10			10		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	30		**2.0**	30		**2.0**	3.0		V/µs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			35			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	35		10	35		10	35	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			35			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			25			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD642JH			AD642KH			AD642LH			AD642SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

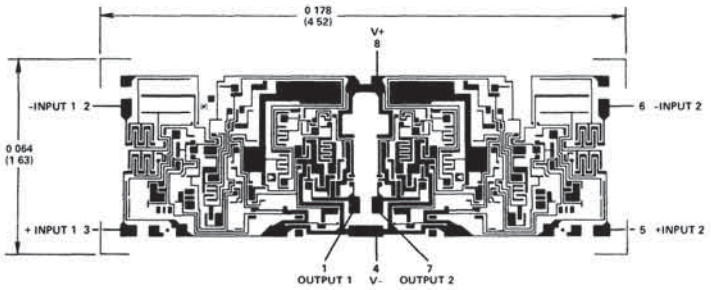
[5]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm)



Typical Characteristics

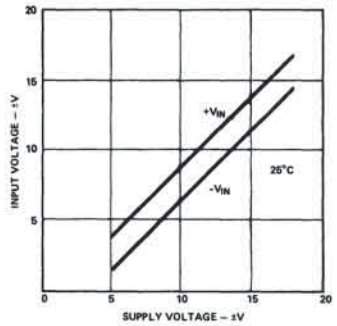


Figure 1. Input Voltage Range vs. Supply Voltage

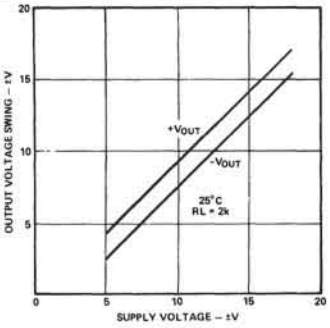


Figure 2. Output Voltage Swing vs. Supply Voltage

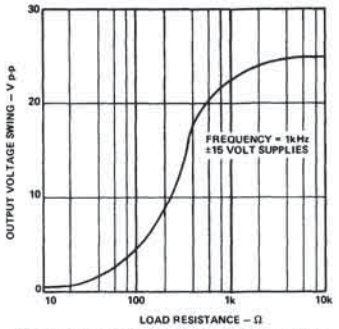


Figure 3. Output Voltage Swing vs. Resistive Load

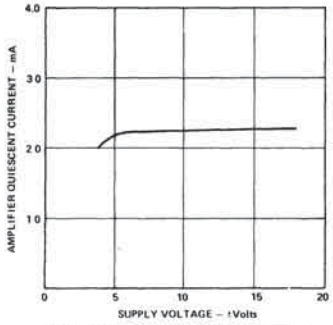


Figure 4. Quiescent Current vs. Supply Voltage

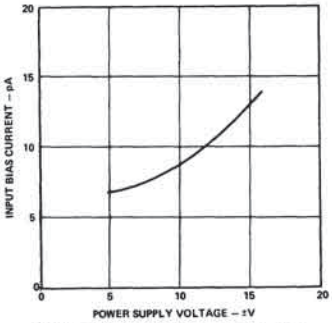


Figure 5. Input Bias Current vs. Supply Voltage

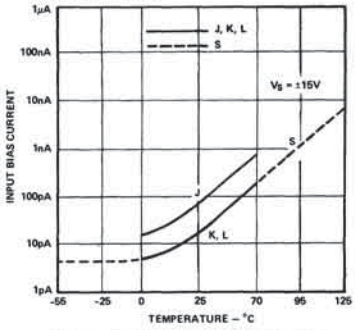


Figure 6. Input Bias Current vs. Temperature

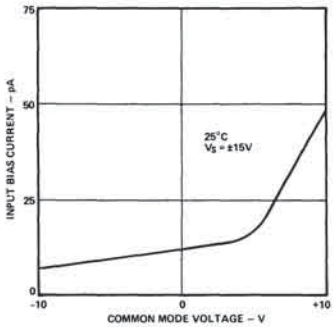


Figure 7. Input Bias Current vs. CMV

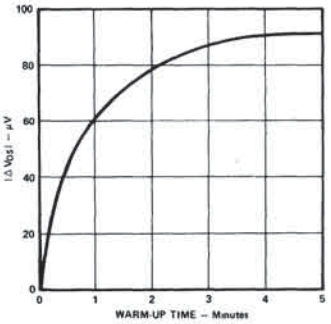


Figure 8. Input Offset Voltage Turn On Drift vs. Time

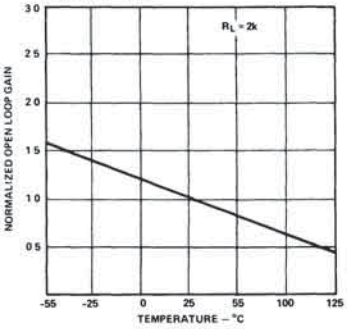


Figure 9. Open Loop Gain vs. Temperature

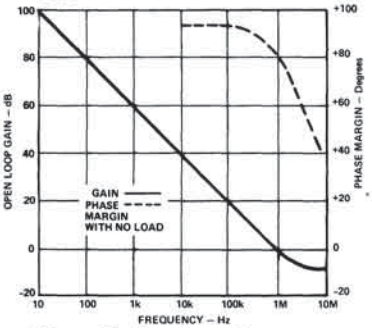


Figure 10. Open Loop Frequency Response

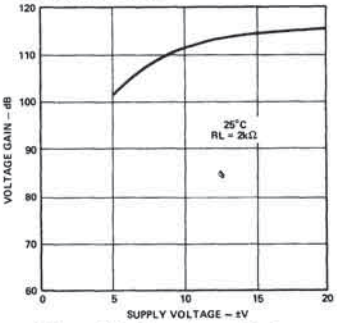


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

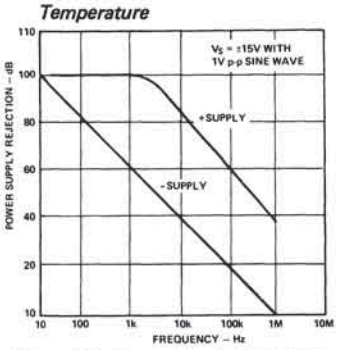


Figure 12. Power Supply Rejection vs. Frequency

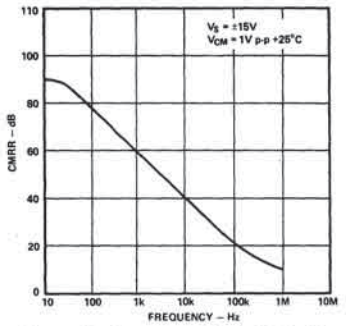


Figure 13. Common Mode Rejection vs. Frequency

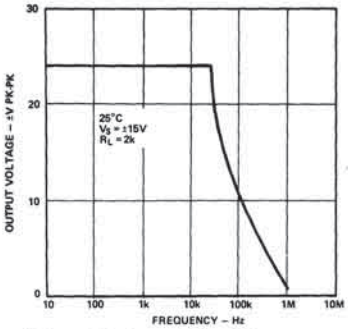


Figure 14. Large Signal Frequency Response

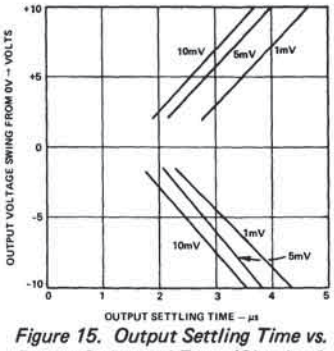


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

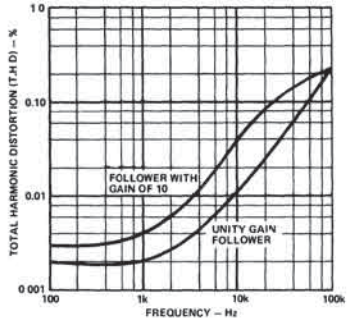


Figure 16. Total Harmonic Distortion vs. Frequency

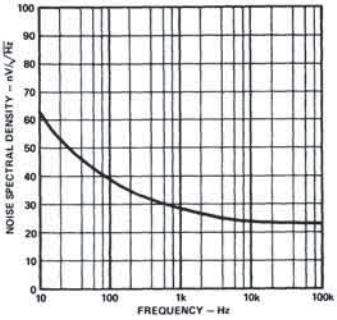


Figure 17. Input Noise Voltage Spectral Density

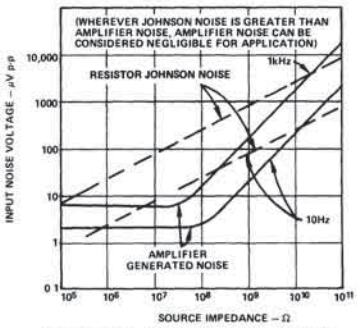
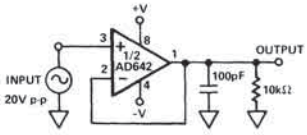
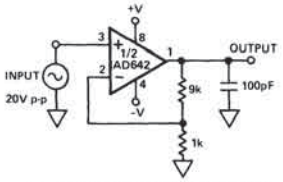


Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

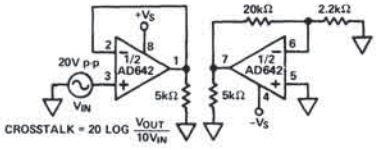


Figure 20. Crosstalk Test Circuit

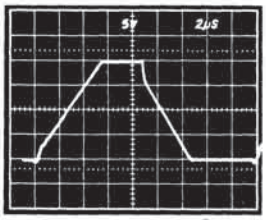


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

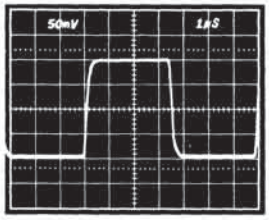


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

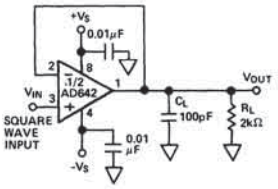


Figure 21c. Unity Gain Follower

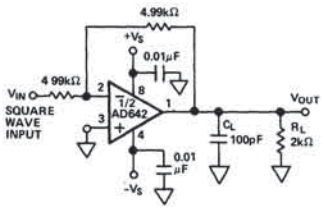


Figure 22a. Unity Gain Inverter

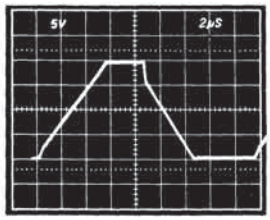


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

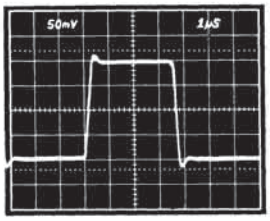


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

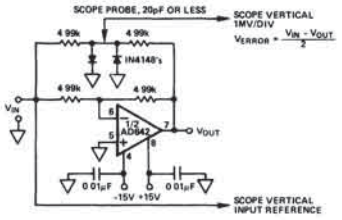


Figure 23. Settling Time Test Circuit

Fast settling time (8μs to 0.01% for 20V p-p step), low power and low offset voltage make the AD642 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

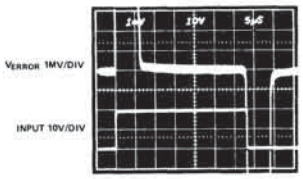


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 24 shows the settling characteristic of the AD642. The lower trace represents the input to Figure 23. The AD642 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.

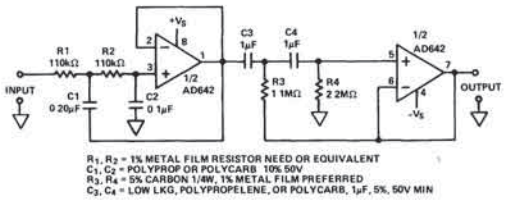


Figure 25. 0.1Hz to 10Hz 2nd Order Bandpass Filter, Maximally Flat

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10Hz, but it can be important for low frequency-high gain applications.

The low noise characteristics of the AD642 make it ideal for 1/f noise testing circuits. The circuit of Figure 25 is a 0.1Hz to 10Hz bandpass filter with second order filter characteristics.

The circuit illustrated in Figure 26 uses two AD642s to construct an instrumentation amplifier with low input current (35pA max), high linearity and low offset voltage and offset voltage drift. The AD644 may be substituted for increased speed, but the higher open-loop gain of the AD642 maintains better linearity over the gain range of 1 to 1000. Amplifier A1 is an AD642L for low input offset voltage (250μV max) and low input offset voltage drift at high gains because matching and tracking are very important for the balanced input stage. Amplifier A2 serves two nonrelated functions, output amplifier and active data-guard drive, and does not require close matching between sections; thus it may be an AD642J.

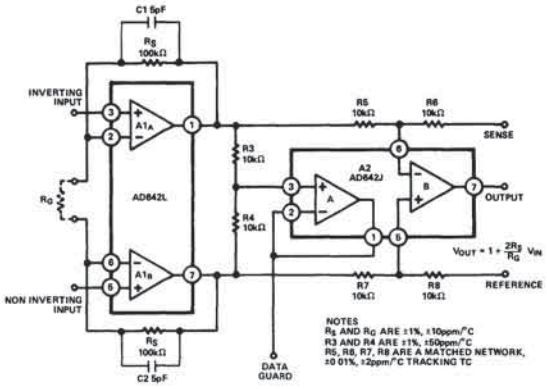


Figure 26. Precision FET Input Instrumentation Amplifier

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD642K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD642.

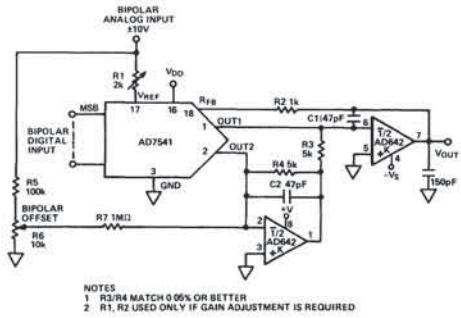


Figure 27a. AD642 Used as DAC Output Amplifier

Figure 27a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

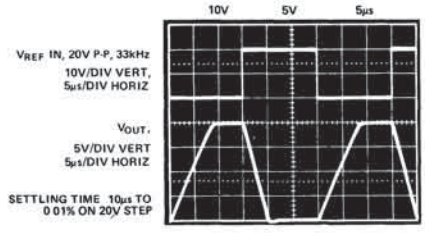


Figure 27b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 27a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback

resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD642 make it suitable for wide dynamic range log amplifiers. Figure 28 is a schematic of a log ratio circuit employing the AD642 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

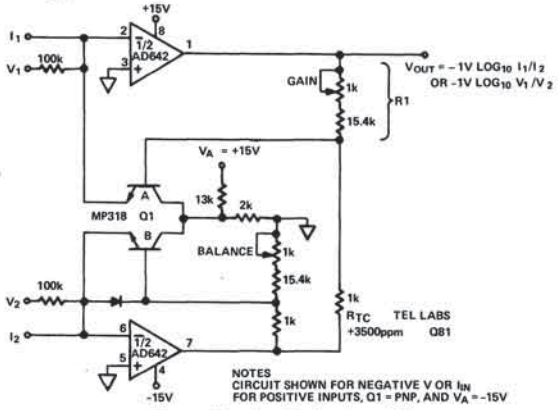


Figure 28. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

The low input bias current (35pA) and low noise characteristics of the AD642 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD642 can deliver. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

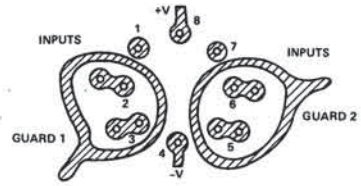


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD642 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD642 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD642 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

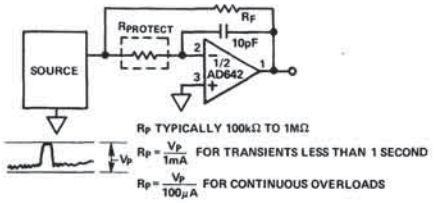


Figure 30. AD642 Input Protection

ANALOG DEVICES

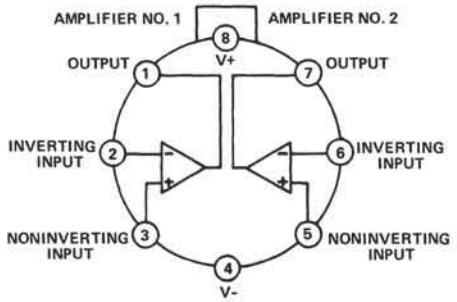
Dual High-Speed Implanted BiFET Op Amp

AD644

FEATURES

- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Currents
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 500μV max
- Low Input Voltage Noise: 2μV p-p
- High Slew Rate: 13V/μs
- Low Quiescent Current: 4.5mA max
- Fast Settling to ±0.01%: 3μs
- Low Total Harmonic Distortion: 0.0015% at 1kHz
- Standard Dual Amplifier Pin Out

AD644 PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high-speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser-trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual BiFET operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.
9. The AD644 is available in chip form.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD644J Min	AD644J Typ	AD644J Max	AD644K Min	AD644K Typ	AD644K Max	AD644L Min	AD644L Typ	AD644L Max	AD644S Min	AD644S Typ	AD644S Max	Units
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	20,000			**40,000**			**40,000**			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2 0			2.0			2 0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	**8.0**	13 0		**8.0**	13 0		**8.0**	13 0		**8.0**	13 0		V/μs
Total Harmonic Distortion		0 0015			0 0015			0.0015			0 0015		%
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			3 5			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		10			5			5			5		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0 1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		22			22			22			22		nV/√Hz
f = 1kHz		18			18			18			18		nV/√Hz
f = 10kHz		16			16			16			16		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		3 5	**4.5**		3 5	**4.5**		3 5	**4.5**		3 5	**4.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD644JH			AD644KH			AD644LH			AD644SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

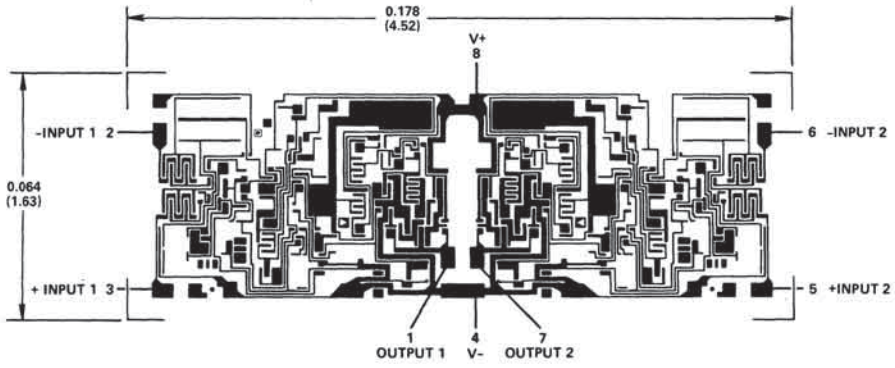
[5]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



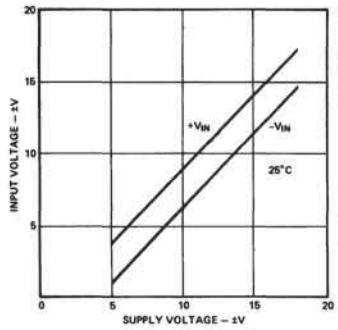


Figure 1. Input Voltage Range vs. Supply Voltage

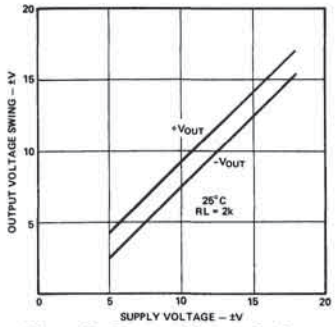


Figure 2. Output Voltage Swing vs. Supply Voltage

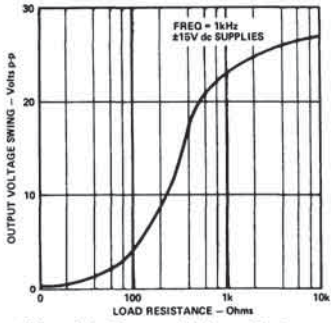


Figure 3. Output Voltage Swing vs. Resistive Load

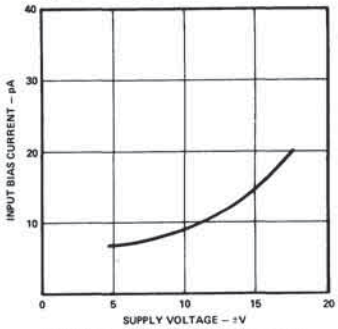


Figure 4. Input Bias Current vs. Supply Voltage

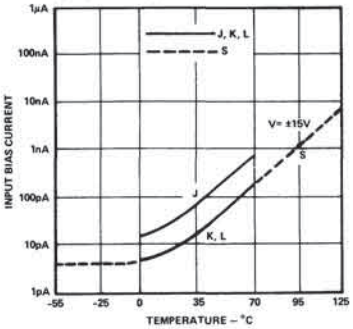


Figure 5. Input Bias Current vs. Temperature

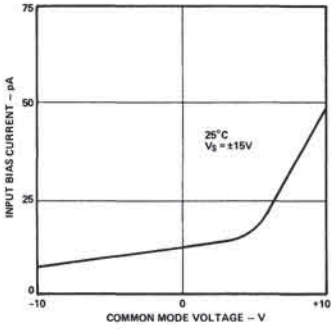


Figure 6. Input Bias Current vs. CMV

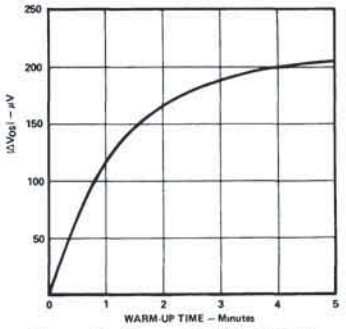


Figure 7. Change in Offset Voltage vs. Warm-Up Time

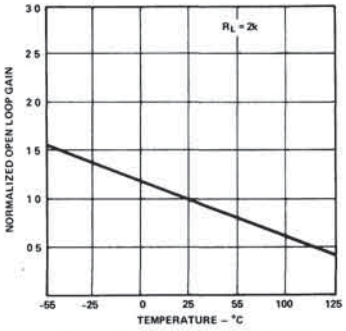


Figure 8. Open Loop Gain vs. Temperature

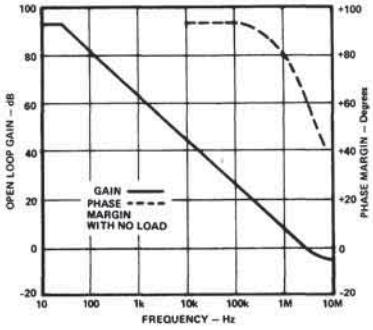


Figure 9. Open Loop Frequency Response

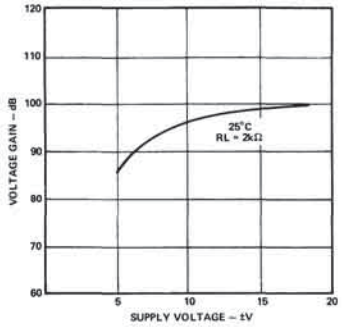


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

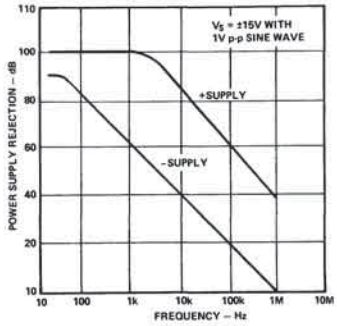


Figure 11. Power Supply Rejection vs. Frequency

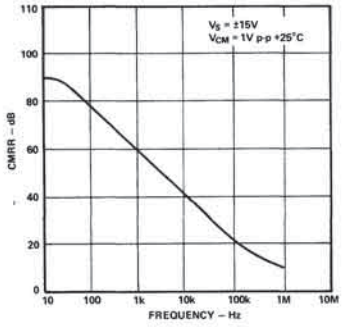


Figure 12. Common Mode Rejection Ratio vs. Frequency

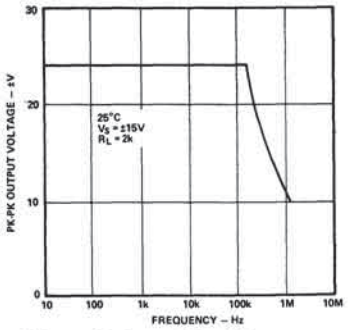


Figure 13. Large Signal Frequency Response

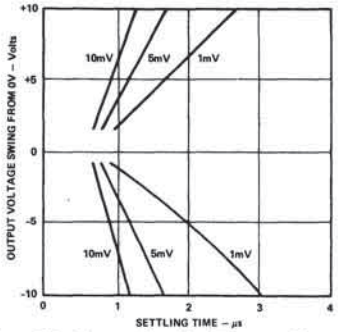


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

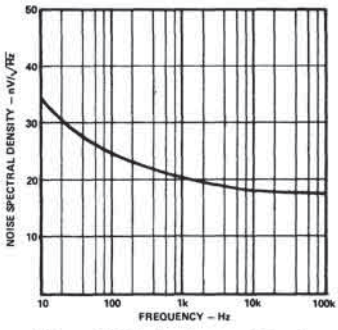


Figure 15. Noise Spectral Density

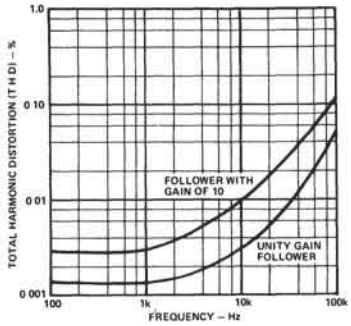


Figure 16. Total Harmonic Distortion vs. Frequency

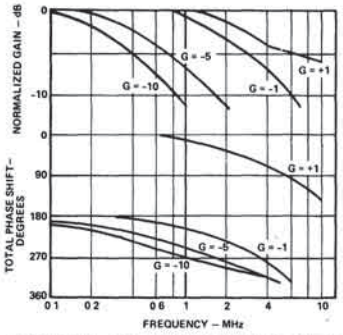


Figure 17. Closed Loop Gain & Phase vs. Frequency

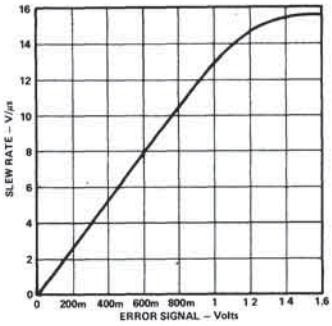
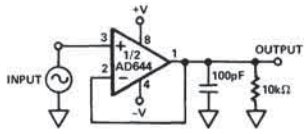
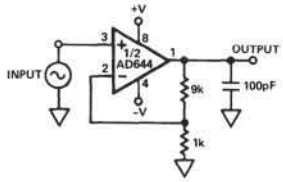


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

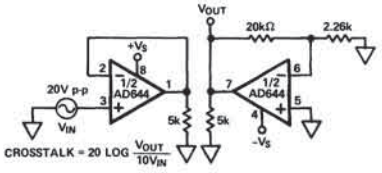


Figure 20. Crosstalk Test Circuit

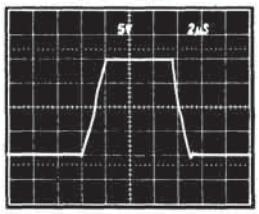


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

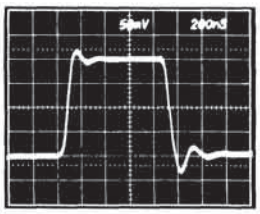


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

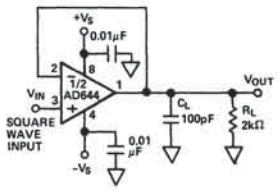


Figure 21c. Unity Gain Follower

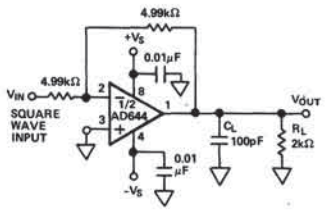


Figure 22a. Unity Gain Inverter

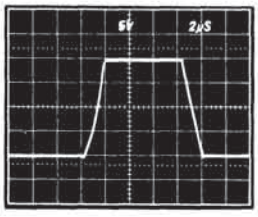


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

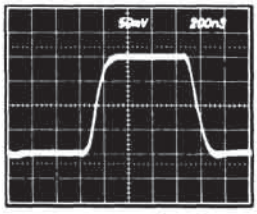


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

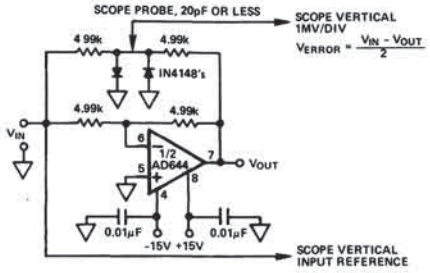


Figure 23a. Settling Time Test Circuit

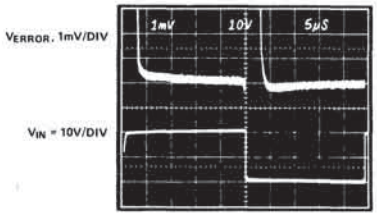


Figure 23b. Settling Characteristic Detail

The fast settling time (3.0μs to 0.01% for 20V p-p step) and low offset voltage make the AD644 an excellent choice as an output amplifier for current output D/A converters such as the AD7541. The upper trace of the oscilloscope photograph of Figure 23b shows the settling characteristics of the AD644. The lower trace represents the input to Figure 23a. The AD644 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

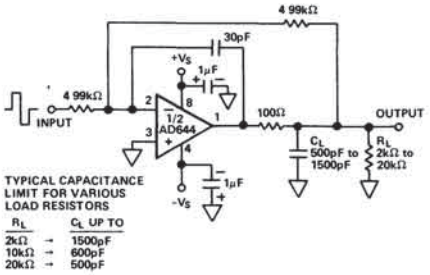
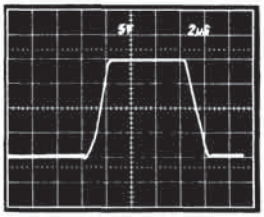


Figure 24. Circuit for Driving a Large Capacitive Load



Transient Response $R_L = 2k\Omega$ $C_L = 500pF$

The circuit in Figure 24 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

The low input bias current (35pA), low noise, high slew rate and high bandwidth characteristics of the AD644 make it suitable for electrometer applications such as photodiode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD644 can deliver. The input guarding scheme shown in Figure 25 will minimize leakage as much as possible. The same layout should be used on both sides of a double side board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, such conductors should be replaced by rigid shielded cables.

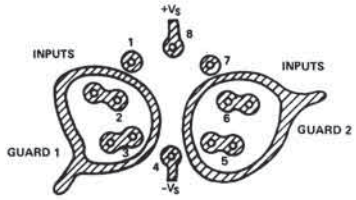


Figure 25. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD644 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD644 suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD644 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 26 shows proper connections.

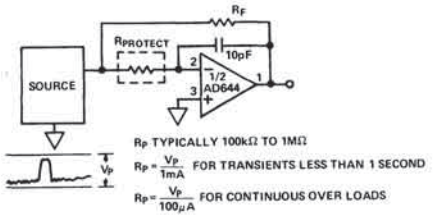


Figure 26. AD644 Input Protection

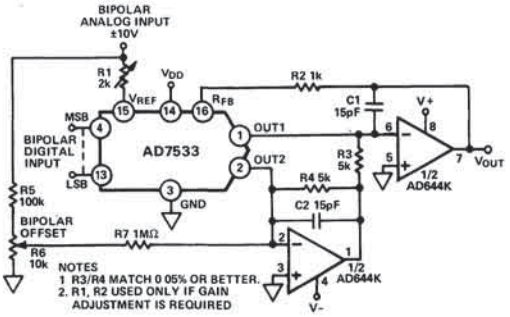


Figure 27a. AD644 Used as DAC Output Amplifiers

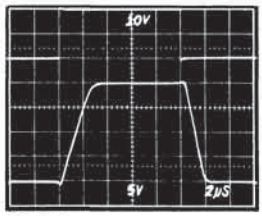


Figure 27b. Large Signal Response

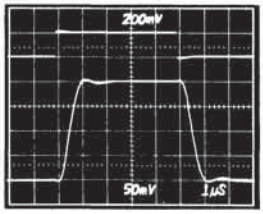


Figure 27c. Small Signal Response

Figure 27a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 27b is the large signal response and Figure 27c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD644K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD644.

ACTIVE FILTERS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter however, depends on the component selection to achieve the desired performance. The AD644 is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

The state variable filter (Figure 28) is stable, easily tuned and is independent of circuit Q and gain. The use of the AD644 with its low input bias current simplifies the resistor (R3, R4) selection for the passband center frequency, circuit Q and voltage gain.

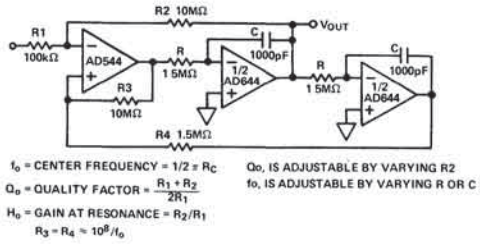


Figure 28. Band Pass State Variable Filter

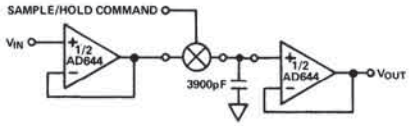


Figure 29. Sample and Hold Circuit

The sample and hold circuit, shown in Figure 29 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15μs.

The droop rate is very low 25×10^{-9} V/μs due to the low input bias currents of the AD644. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.

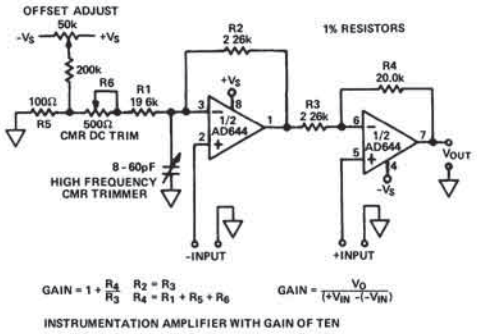


Figure 30. Wide Bandwidth Instrumentation Amplifier

The AD644 in the circuit of Figure 30 provides highly accurate signal conditioning with high frequency input signals. It provides an offset voltage drift of 10μV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (-3dB) at 1V p-p output. The circuit of Figure 30 can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

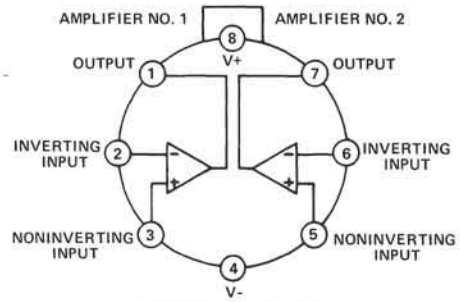
Ultralow-Drift Dual BiFET Op Amp

AD647

FEATURES

- Low Offset Voltage Drift
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Current
- Crosstalk –124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 250μV max
- Low Input Voltage Noise: 2μV p-p
- High Open Loop Gain: 108dB
- Low Quiescent Current: 2.8mA max
- Low Total Harmonic Distortion
- Standard Dual Amplifier Pin Out

AD647 PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

PRODUCT DESCRIPTION

The AD647 is an ultralow-drift dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

This high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 also offers high levels of performance for Digital to Analog Converter output amplifiers, and filtering applications.

The AD647 is offered in four performance grades, three commercial (the J, K, and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guaranteed at 4μV p-p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pin out permits the direct substitution of the AD647 for lower performance devices.
8. The AD647 is available in chip form.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD647J Min	AD647J Typ	AD647J Max	AD647K Min	AD647K Typ	AD647K Max	AD647L Min	AD647L Typ	AD647L Max	AD647S Min	AD647S Typ	AD647S Max	Units
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3 0		**2.0**	3.0		**2.0**	3 0		**2.0**	3 0		V/µs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs Temp			**10**			5			**2.5**			**5.0**	µV/°C
Input Offset Voltage vs Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**10**			5			**2.5**			**10.0**	µV/°C
Input Bias Current			**35**			**25**			**25**			**25**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common-Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0 1Hz to 10Hz		2				**4**			**4**			**4**	µV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD647JH			AD647KH			AD647LH			AD647SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C

[3]Matching is defined as the difference between parameters of the two amplifiers

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground

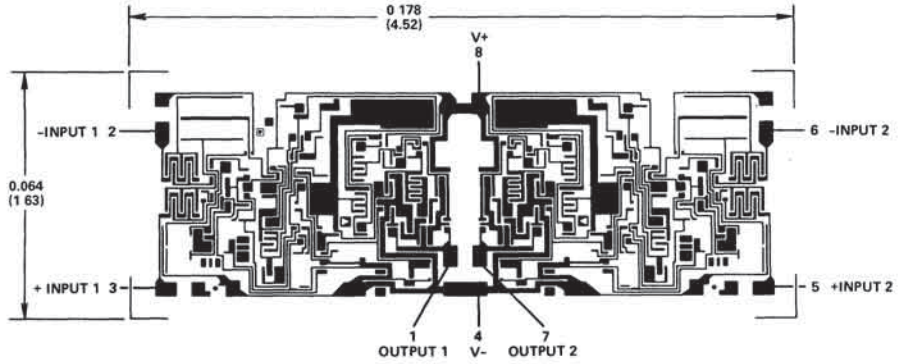
[5]See Section 16 for package outline information

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).



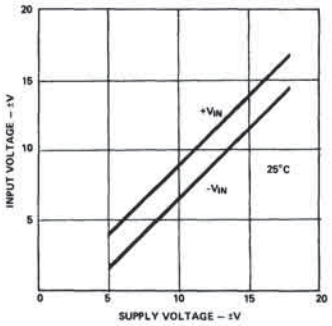


Figure 1. Input Voltage Range vs. Supply Voltage

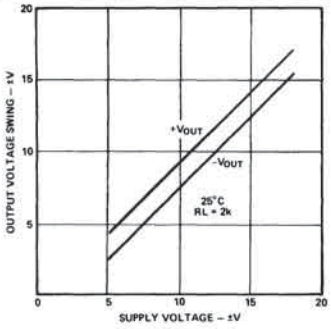


Figure 2. Output Voltage Swing vs. Supply Voltage

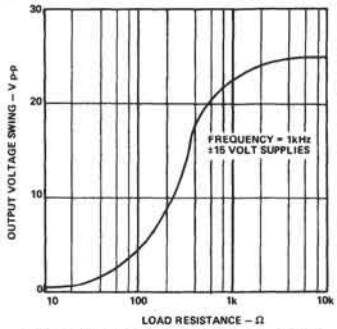


Figure 3. Output Voltage Swing vs. Resistive Load

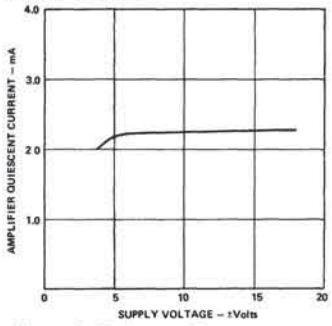


Figure 4. Quiescent Current vs. Supply Voltage

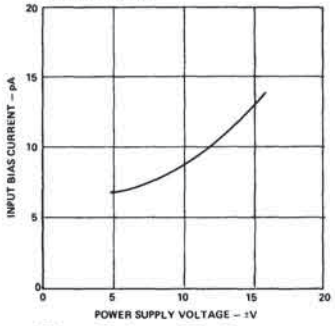


Figure 5. Input Bias Current vs. Supply Voltage

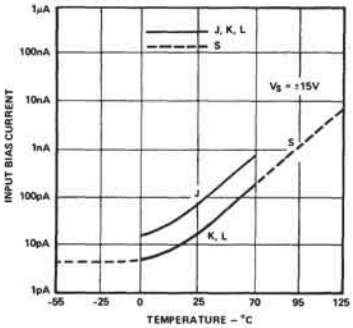


Figure 6. Input Bias Current vs. Temperature

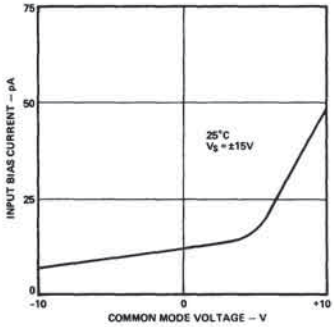


Figure 7. Input Bias Current vs. CMV

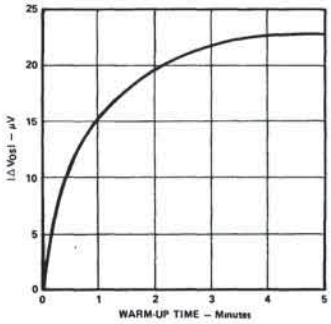


Figure 8. Input Offset Voltage Turn On Drift vs. Time

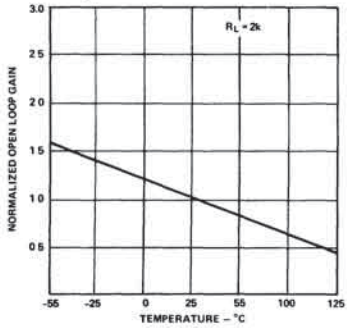


Figure 9. Open Loop Gain vs. Temperature

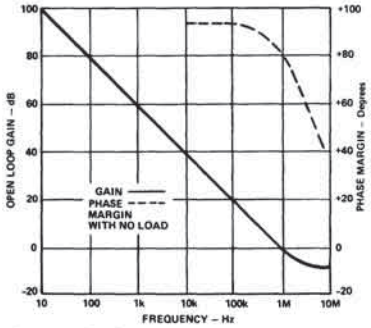


Figure 10. Open Loop Frequency Response

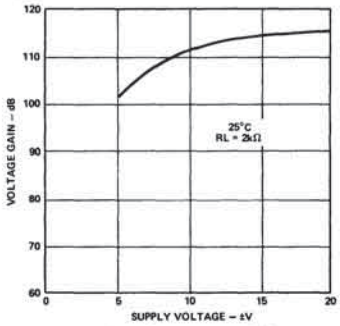


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

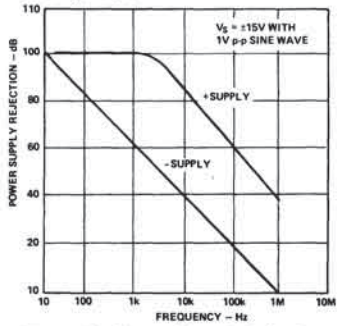


Figure 12. Power Supply Rejection vs. Frequency

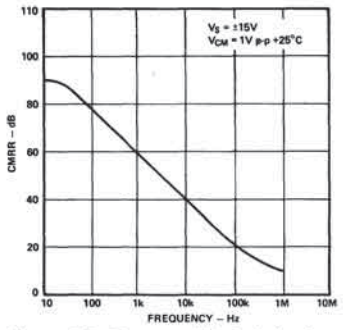


Figure 13. Common Mode Rejection vs. Frequency

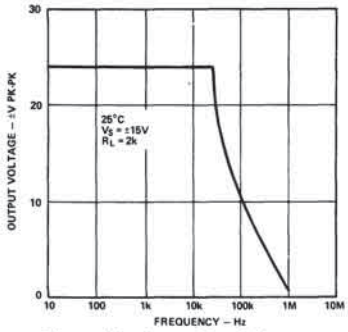


Figure 14. Large Signal Frequency Response

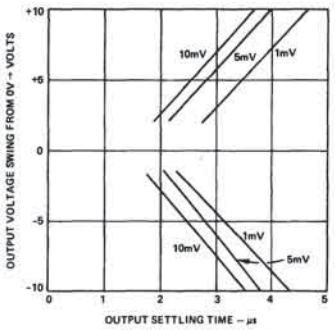


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

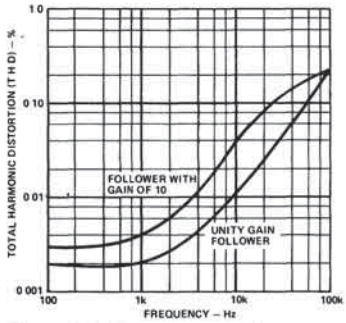


Figure 16. Total Harmonic Distortion vs. Frequency

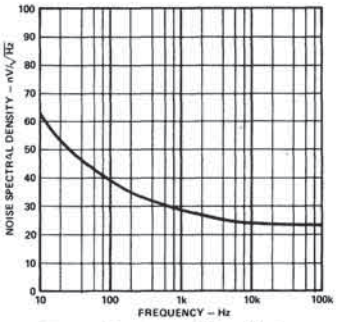


Figure 17. Input Noise Voltage Spectral Density

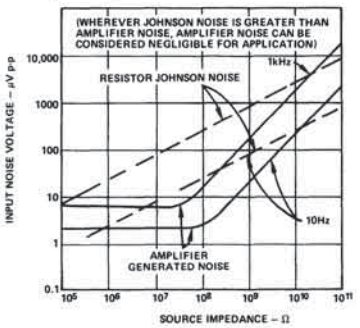
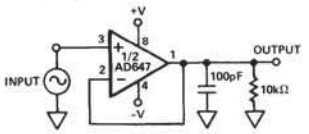
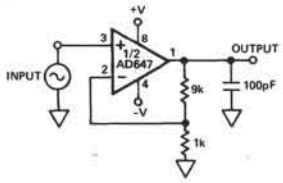


Figure 18. Total rms Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

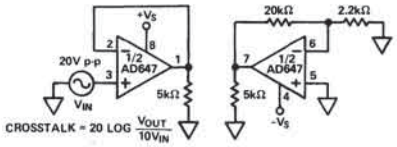


Figure 20. Crosstalk Test Circuit

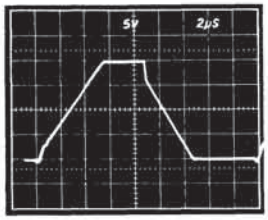


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

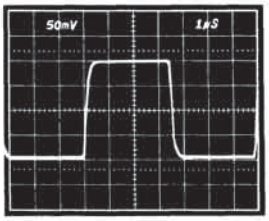


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

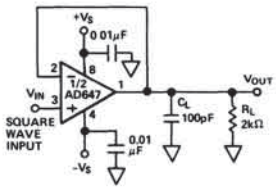


Figure 21c. Unity Gain Follower

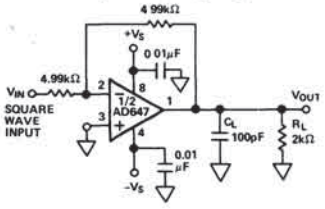


Figure 22a. Unity Gain Inverter

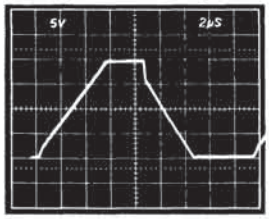


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

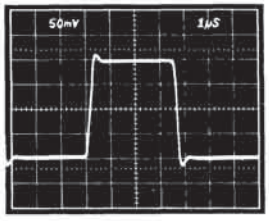


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD647 is fully specified under actual operating conditions to insure high performance in any application, but there are some steps that will improve on even this high level of performance.

The bias current of a JFET amplifier doubles with every 10°C increase in junction temperature. Any heat source that can be eliminated or minimized will significantly improve bias current performance. To account for normal power dissipation, the largest contributor to chip self-heating, the bias currents of the AD647 are guaranteed fully warmed up with ±15V supplies. A decrease in supply voltage will decrease power consumption, resulting in a corresponding drop in bias currents.

Open loop gain and bias currents, to some extent, are affected by output loading. In applications where high linearity is essential, load impedance should be kept as high as possible to minimize degradation of open loop gain.

The outstanding ac and dc performance of the AD647 make it an ideal choice for critical instrumentation applications. In such applications, leakage paths, line losses and external noise sources should be considered in the layout of printed circuit boards. A guard ring surrounding the inputs and connected to a low impedance potential (at the same level as the inputs) should be placed on both sides of the circuit board. This will eliminate leakage paths that could degrade bias current performance. All signal paths should be shielded to minimize noise pick-up.

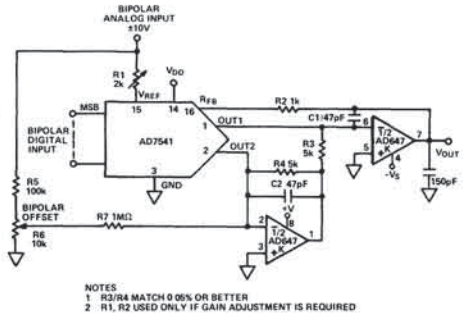


Figure 23. AD647 Used as DAC Output Amplifier

A CMOS DAC AMPLIFIER

The output impedance of a CMOS DAC, such as the AD7541, varies with digital input code. This causes a corresponding variation in the noise gain of the DAC-amplifier combination. This noise gain modulation introduces a nonlinearity whose magnitude is dependent on the amount of offset voltage present.

Laser wafer drift trimming lowers the initial offset voltage and the offset voltage drift of the AD647, therefore minimizing the effect of this nonlinearity and its drift with temperature. This, in conjunction with the low bias current and high open loop gain, makes the AD647 ideal for DAC output amplifier applications.

THE AD647 USED WITH THE AD7546

Figure 24 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function: amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

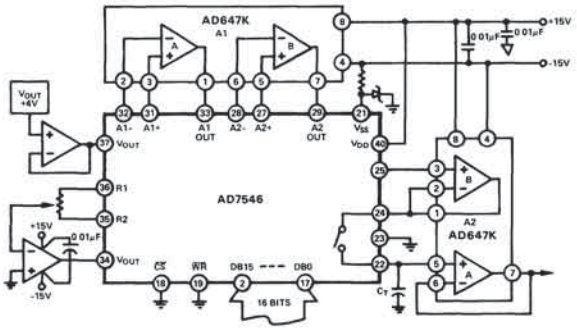


Figure 24. AD647 Used with AD7546 16-Bit DAC

USING THE AD647 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

The picoamp level input current and low offset voltage of the AD647 make it suitable for wide dynamic range log amplifiers. Figure 27 is a schematic of a log ratio circuit employing the AD647 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

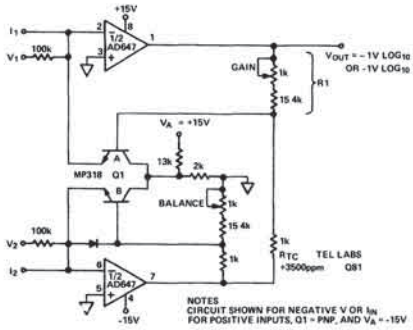


Figure 25. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation.

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce a 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, which may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ACTIVE FILTERS

In active low pass filtering applications the dc accuracy of the amplifiers used is critical to the performance of the filter circuits. DC error sources such as offset voltage and bias currents represent the largest individual contributors to output error. Offset voltages will be passed by the filtering network and may, depending on the design of the filter circuit, be amplified and generate unacceptable output offset voltages. In filter circuits for low frequency ranges large value resistors are used to generate the low pass filter function. Input bias currents passing through these resistors will generate an additional offset voltage that will also be passed to the output of the filter.

The use of the AD647 will minimize these error sources and, therefore, maximize filter accuracy. The wide variety of performance levels of the AD647 allows for just the amount of accuracy required for any given application.

AD647 AS AN INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 26 uses the AD647 to construct an ultra high precision instrumentation amplifier. In this type of application the matching characteristics of a monolithic dual amplifier are crucial to ensure high performance.

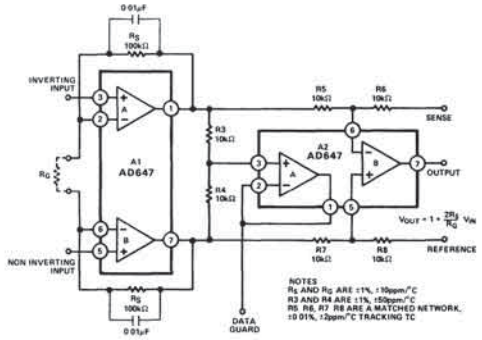


Figure 26. Precision FET Input Instrumentation Amplifier

The use of an AD647L as the input amplifier A1, guarantees maximum offset voltage of 250μV, drift of 2.5μV/°C and bias currents of 35pA. A2 serves two less critical functions in the amplifier and, therefore can be an AD647J. Amplifier A is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B is the output amplifier of the instrumentation amplifier. To attain the precision available from this configuration, a great deal of care should be taken when selecting the external components. CMRR will depend on the matching of resistors R1, R2, R3, and R4. The gain drift performance of this circuit will be affected by the matching TC of the resistors used.

Dual Precision Low-Power BiFET Op Amp

AD648

2

FEATURES

DC Performance:
- **400μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD648C)**
- **300μV max Offset Voltage (AD648C)**
- **3μV/°C max Drift (AD648C)**
- **2μV p-p Noise, 0.1 to 10Hz**

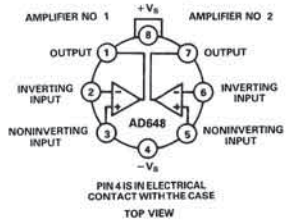
AC Performance:
- **1.8 V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages

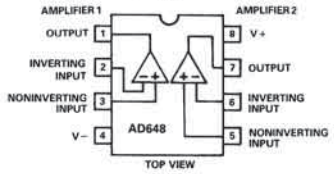
MIL-STD-883B Parts Available

AD648 CONNECTION DIAGRAM

TO-99
(H) Package



Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD648 is a matched pair of low-power, precision monolithic operational amplifiers. It offers both low bias current (10pA max, warmed up) and low quiescent current (400μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD648's entire common-mode voltage range.

The economical J grade has a maximum guaranteed offset voltage of less than 2mV and an offset voltage drift of less than 20μV/°C. The C grade reduces offset voltage to less than 0.30mV and offset voltage drift to less than 3μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD648 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD648's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD648 is pinned out in a standard dual op amp configuration and is available in seven performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0 to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of −40°C to +85°C. The AD648S and AD648T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD648 is available in an 8-pin plastic mini-DIP, cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high-performance, low-power applications.
2. The AD648 is pin compatible with industry standard dual op amps such as the LF442, TL062, and AD642, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD648J are achieved utilizing Analog Devices' laser drift trimming technology.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. Matching characteristics are excellent for all grades. The input offset voltage matching between amplifiers in the AD648J is within 2mV, for the C grade matching is within 0.4mV.
6. Crosstalk between amplifiers is less than −120dB at 1kHz.
7. The AD648 is available in chip form.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD648J/A/S Min	AD648J/A/S Typ	AD648J/A/S Max	AD648K/B/T Min	AD648K/B/T Typ	AD648K/B/T Max	AD648C Min	AD648C Typ	AD648C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0 75	**2.0**		0.3	**1.0**		0.10	**0.3**	mV
T_{min} to T_{max}			3.0/3.0/**3.0**			**1.5/1.5/2.0**			**0.5**	mV
vs Temp			20			**10**			**3.0**	µV/°C
vs Supply			**80**			**86**			**86**	dB
vs Supply, T_{min} to T_{max}			76/76/**76**			**80**			**80**	dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1 3/20			0.25/0 65/10			0 65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			**15**			**15**	pA
Offset Current, V_{CM} = 0		5	**10**		2	5		2	5	pA
Offset Current at T_{max}			0.25/0.7/10			0 15/0 35/5			0 35	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage		1 0	**2.0**		0.5	**1.0**		0 2	**0.4**	mV
Input Offset Voltage T_{min} to T_{max}			3 0/3 0/**3.0**			**1.5/1.5/2.0**			**0.5**	mV
Input Offset Voltage vs Temp		8			5			2.5		µV/°C
Input Bias Current			**10**			5			5	pA
Crosstalk		−120			−120			−120		dB
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10V	**76**			**82**			**86**			dB
T_{min} to T_{max}	76/76/**76**			**82**			**86**			dB
V_{CM} = ±11V	**70**			**76**			**76**			dB
T_{min} to T_{max}	70/70/**70**			**76**			**76**			dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	4	µV p-p
f = 10Hz		80			80			80		nV/√Hz
f = 100Hz		40			40			40		nV/√Hz
f = 1kHz		30			30			30		nV/√Hz
f = 10kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		1 8			1 8			1 8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0 8	1 0		0.8	1 0		0.8	1 0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1 8		**1.0**	1 8		**1.0**	1.8		V/µs
Settling Time to ±0 01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 10k\Omega$	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10k\Omega$	300/300/**300**	700		**300**	700		**300**	700		V/mV
V_O = ±10V, $R_L \geq 5k\Omega$	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq 5k\Omega$	150/150/**150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10k\Omega$, T_{min} to T_{max}	±12/±12/**±12**	±13		**±12**	±13		**±12**	±13		V
Voltage @ $R_L \geq 5k\Omega$, T_{min} to T_{max}	±11/±11/**±11**	±12		**±11**	±12		**±11**	±12		V
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current (Both Amplifiers)		340	**400**		340	**400**		340	**400**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD648J			AD648K					
Industrial (−40°C to +85°C)		AD648A			AD648B			AD648C		
Military (−55°C to +125°C)		AD648S			AD648T					
PACKAGE OPTIONS[5]										
Plastic (N-8)		AD648JN			AD648KN					
Cerdip (Q-8)		AD648AQ, AD648SQ			AD648BQ, AD648TQ			AD648CQ		
Metal Can (H-08A)		AD648AH, AD648SH			AD648BH, AD648TH			AD648CH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C
For higher temperature, the current doubles every 10°C

[3]Matching is defined as the difference between parameters of the two amplifiers

[4]Defined as voltages between inputs, such that neither exceeds ±10V from ground

[5]See Section 16 for package outline information

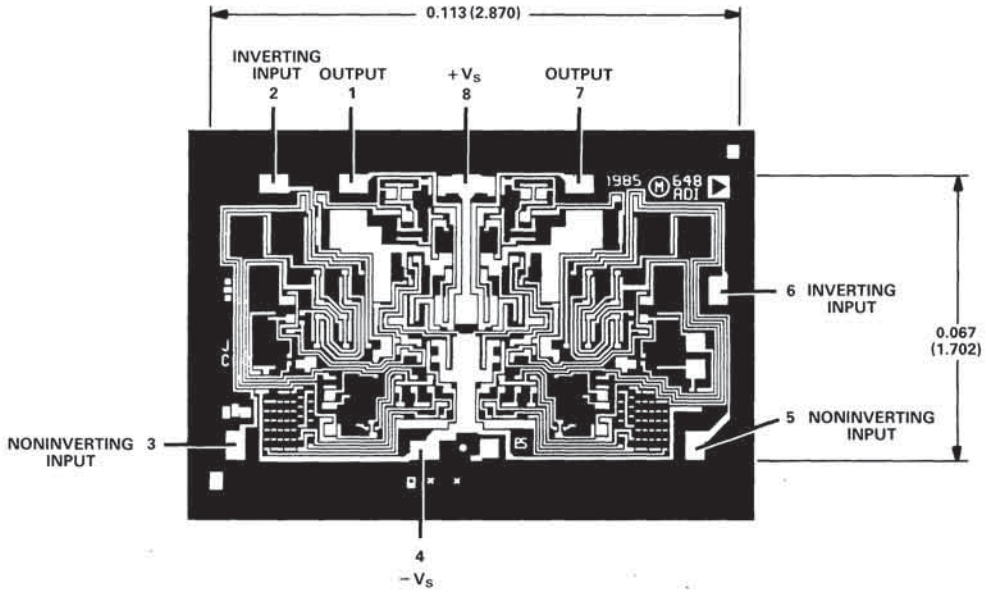
Specifications subject to change without notice

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
N	−65°C to +125°C
Operating Temperature Range	
AD648J/K	0 to +70°C
AD648A/B/C	−40°C to +85°C
AD648S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.



CHIP DIMENSIONS AND PAD LAYOUT
Dimensions shown in inches and (mm).

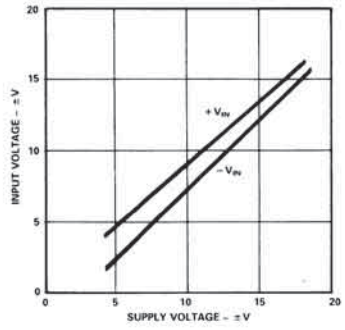


Figure 1. Input Voltage Range vs. Supply Voltage

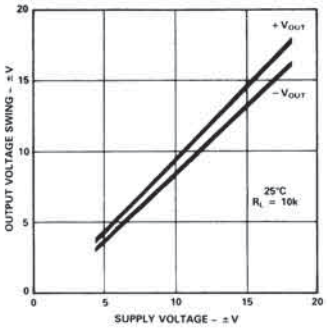


Figure 2. Output Voltage Swing vs. Supply Voltage

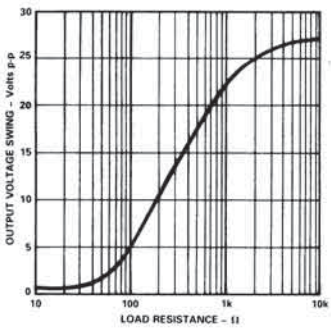


Figure 3. Output Voltage Swing vs. Resistive Load

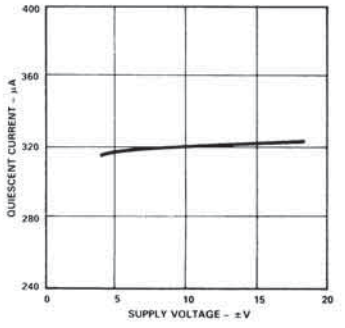


Figure 4. Quiescent Current vs. Supply Voltage

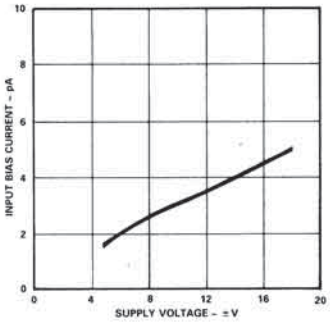


Figure 5. Input Bias Current vs. Supply Voltage

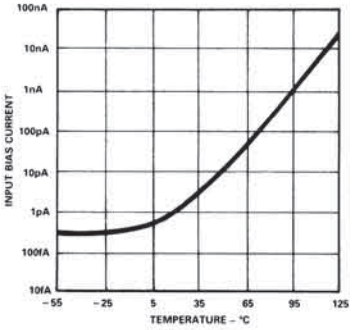


Figure 6. Input Bias Current vs. Temperature

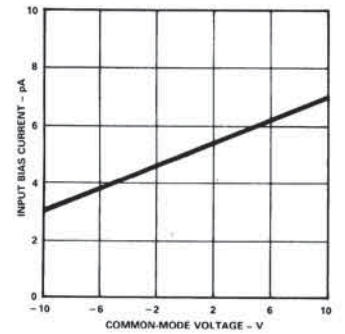


Figure 7. Input Bias Current vs. Common-Mode Voltage

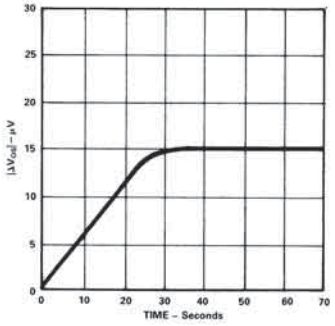


Figure 8. Change in Offset Voltage vs. Warm-Up Time

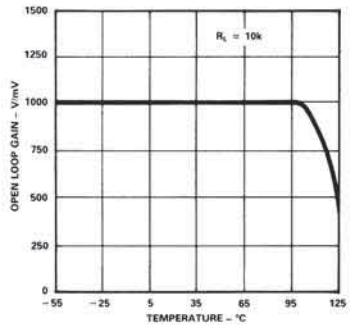


Figure 9. Open Loop Gain vs. Temperature

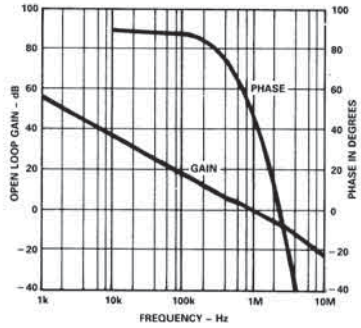


Figure 10. Open Loop Frequency Response

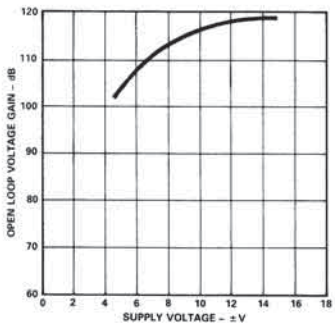


Figure 11. Open Loop Voltage Gain vs. Supply

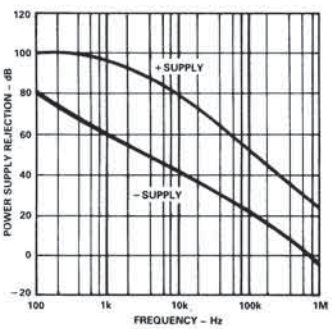


Figure 12. PSRR vs. Frequency

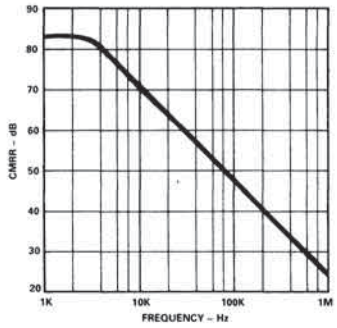


Figure 13. CMRR vs. Frequency

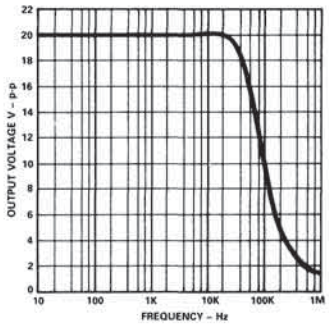


Figure 14. Large Signal Frequency Response

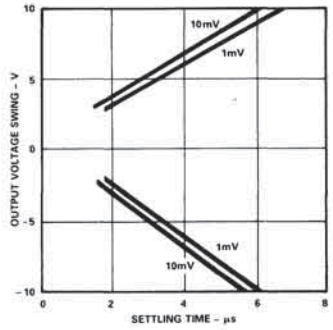


Figure 15. Output Settling Time vs. Output Swing and Error Voltage

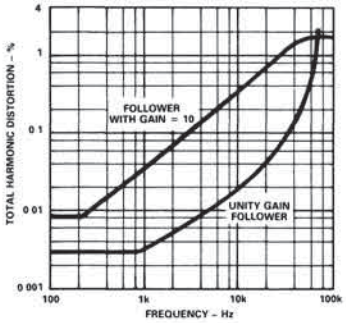


Figure 16. Total Harmonic Distortion vs. Frequency

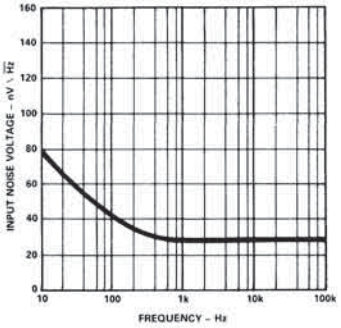


Figure 17. Input Noise Voltage Spectral Density

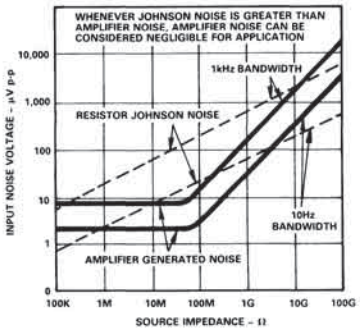


Figure 18. Total Noise vs. Source Resistance

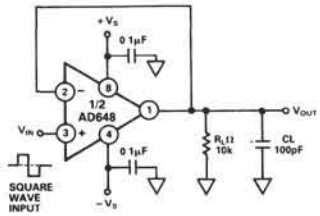


Figure 19a. Unity Gain Follower

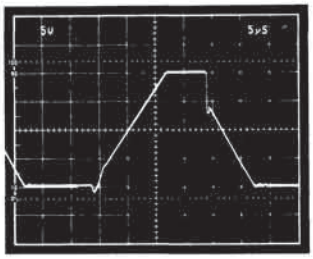


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

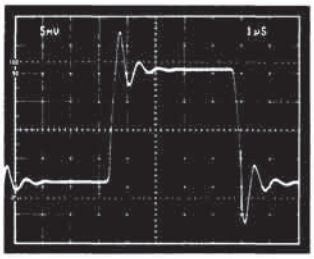


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

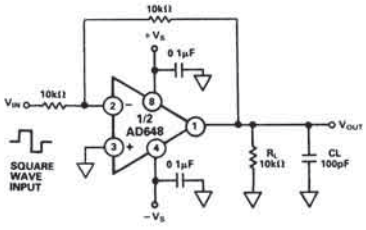


Figure 20a. Unity Gain Inverter

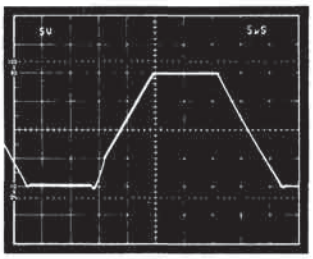


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

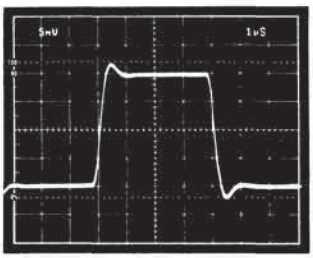


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

Applying the AD648

APPLICATION NOTES

The AD648 is a pair of JFET-input op amps with a guaranteed maximum I_B of less than 10pA, and offset and drift laser-trimmed to 0.3mV and 3μV/°C respectively (AD648C). AC specs include 1MHz bandwidth, 1.8V/μs typical slew rate and 8μs settling time for a 20V step to ±0.01% – all at a supply current less than 400μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD648 reduce self-heating or "warm-up" effects on input offset voltage, making the AD648 ideal for on/off battery powered applications. The power dissipation due to the AD648's 400μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15V, due to power supply rejection effects. Common mode range extends from 3V more positive than the negative supply to 1V more negative than the positive supply. Designed to cleanly drive up to 10kΩ and 100pF loads, the AD648 will drive a 2kΩ load with reduced open loop gain.

Figure 21 shows the recommended crosstalk test circuit. A typical value for crosstalk is −120dB at 1kHz.

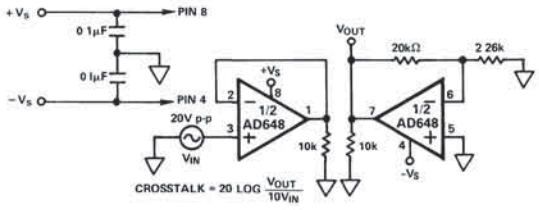


Figure 21. Crosstalk Test Circuit

LAYOUT

To take full advantage of the AD648's 10pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between $1 \times 10^{12}\Omega$ and $3 \times 10^{12}\Omega$. This can result in an additional leakage of 5pA between an input of 0V and a −15V supply line. Teflon or a similar low leakage material (with a resistance exceeding $10^{17}\Omega$) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

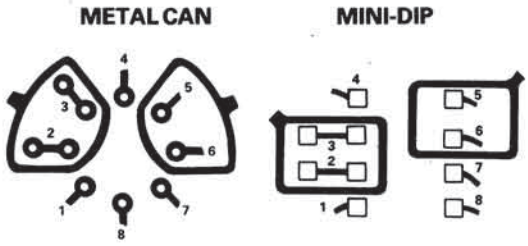


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD648 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figures 23a and 23b show simple current limiting schemes that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0mA (for example 100kΩ for a 100V overload).

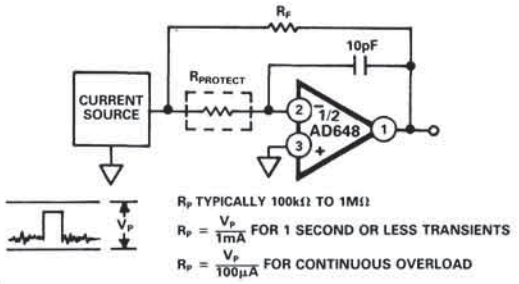


Figure 23a. Input Protection of I-to-V Converter

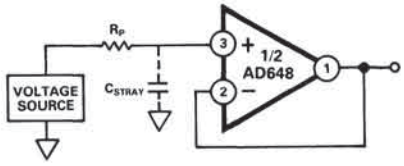


Figure 23b. Voltage Follower Input Protection Method

Figure 23b shows the recommended method for protecting a voltage follower from excessive currents due to high voltage breakdown. The protection resistor, R_p, limits the input current. A nominal value of 100kΩ will limit the input current to less than 1mA with a 100 volt input voltage applied.

The stray capacitance between the summing junction and ground will produce a high frequency roll-off with a corner frequency equal to:

$$f_{corner} = \frac{1}{2\pi R_p C_{stray}}$$

Accordingly, a 100kΩ value for R_p with a 3pF C_{stray} will cause a 3dB corner frequency to occur at 531kHz.

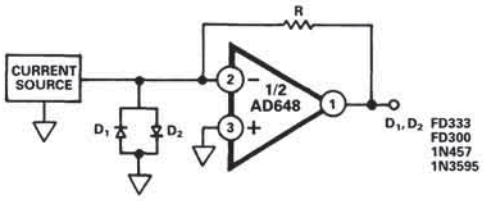


Figure 23c. I-to-V Converter with Diode Input Protection

Figure 23c shows a diode clamp protection scheme for an I-to-V converter using low leakage diodes. Because the diodes are connected to the op amp's summing junction, which is a virtual ground, their leakage contribution is minimal.

Exceeding the negative common mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common mode on both inputs simultaneously forces the output high. Exceeding the positive common mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common mode range.

2

D/A CONVERTER BIPOLAR OUTPUT BUFFER

The circuit in Figure 24 provides 4 quadrant multiplication with a resolution of 12 bits. The AD648 is used to convert the AD7545 CMOS DAC's output current to a voltage and provides the necessary level shifting to achieve a bipolar voltage output. The circuit operates with a 12-bit plus sign input code. The transfer function is shown in Figure 25.

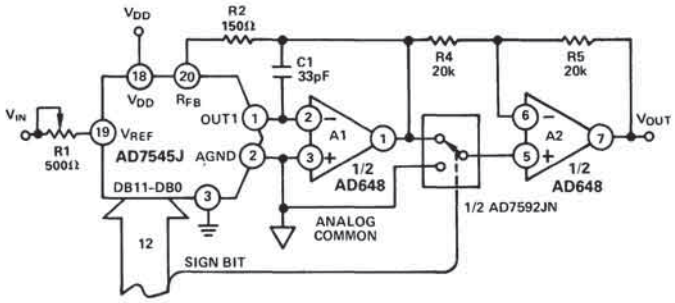


Figure 24. 12-Bit Plus Sign Magnitude D/A Converter

SIGN BIT	BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
0	1111 1111 1111	$+V_{IN} \times (4095/4096)$
0	0000 0000 0000	0 VOLTS
1	0000 0000 0000	0 VOLTS
1	1111 1111 1111	$-V_{IN} \times (4095/4096)$

NOTE: SIGN BIT AT "0" CONNECTS THE NONINVERTING INPUT OF A2 TO ANALOG COMMON

Figure 25. Sign Magnitude Code Table

The AD7592 is a fully protected dual CMOS SPDT switch with data latches. R4 and R5 should match to within 0.01% to maintain the accuracy of the converter. A mismatch between R4 and R5 introduces a gain error. Overall gain is trimmed by adjusting R_{IN}. The AD648's low input offset voltage, low drift over temperature, and excellent dynamics make it an attractive low power output buffer.

The input offset voltage of the AD648 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier. That is:

$$V_{OS}\ \text{Output} = V_{OS}\ \text{Input}\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD648 in this configuration provides a 700kHz small signal bandwidth and 1.8V/μs typical slew rate. The 33pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 26a and 26b show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1's. The circuit settles to ±0.01% for a 20V input step in 14μs.

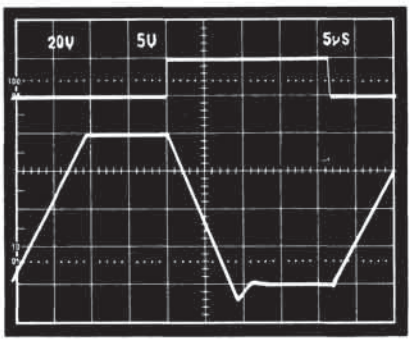


Figure 26a. Response to ±20V p-p Reference Square Wave

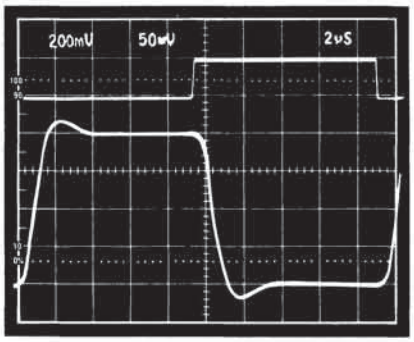


Figure 26b. Response to ±100mV p-p Reference Square Wave

DUAL PHOTODIODE PREAMP

The performance of the dual photodiode preamp shown in Figure 27 is enhanced by the AD648's low input current, input voltage offset, and offset voltage drift. Each photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

An error budget illustrating the importance of low amplifier input current, voltage offset, and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small ($0.2mm^2$ area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1+R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500MΩ, and the maximum input current and input offset voltage specs of an AD648C.

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of signal bandwidth.

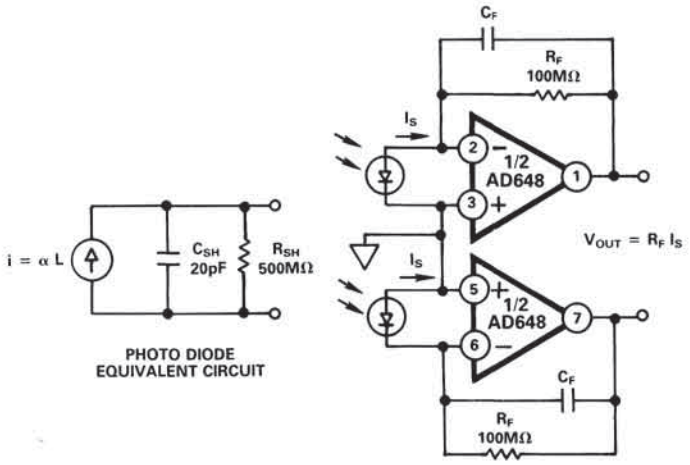


Figure 27. A Dual Photodiode Pre-Amp

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1 + R_F/R_{SH})\,V_{OS}$	I_B (pA)	I_BR_F	TOTAL
−25	15,970	150	151μV	0.30	30μV	181μV
0	2,830	225	233μV	2.26	262μV	495μV
+25	500	300	360μV	10.00	1.0mV	1.36mV
+50	88.5	375	800μV	56.6	5.6mV	6.40mV
+75	15.6	450	3.33mV	320	32mV	35.3mV
+85	7.8	480	6.63mV	640	64mV	70.6mV

Figure 28. Photodiode Pre-Amp Errors Over Temperature

INSTRUMENTATION AMPLIFIER

The AD648J's maximum input current of 20pA per amplifier makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_3 + R_4)}{R_G}$$

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. The maximum input current is 30pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. The capacitors C1, C2, C3 and C4 compensate for peaking in the gain over frequency which is caused by input capacitance.

To calibrate this circuit, first adjust trimmer R1 for common-mode rejection with +10 volts dc applied to the input pins. Next, adjust R2 for zero offset at V_{OUT} with both inputs grounded. Trim the circuit a second time for optimal performance.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700kHz for a gain of 1 and 10kHz for a gain of 100. The typical output slew rate is 1.8V/μs.

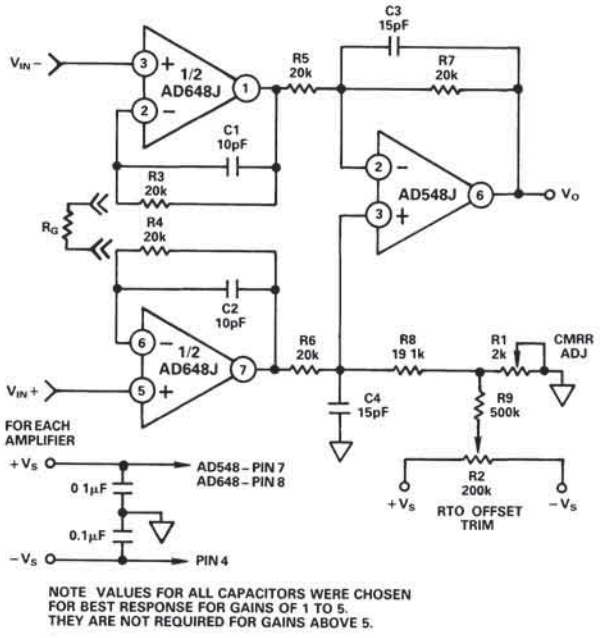


Figure 29. Low Power Instrumentation Amplifier

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD648's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q) \ln (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10} (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300kHz at input currents above 100μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

To trim this circuit, set the two input currents to 10μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300pA to 1mA, with low level accuracy limited by the AD648's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD648.

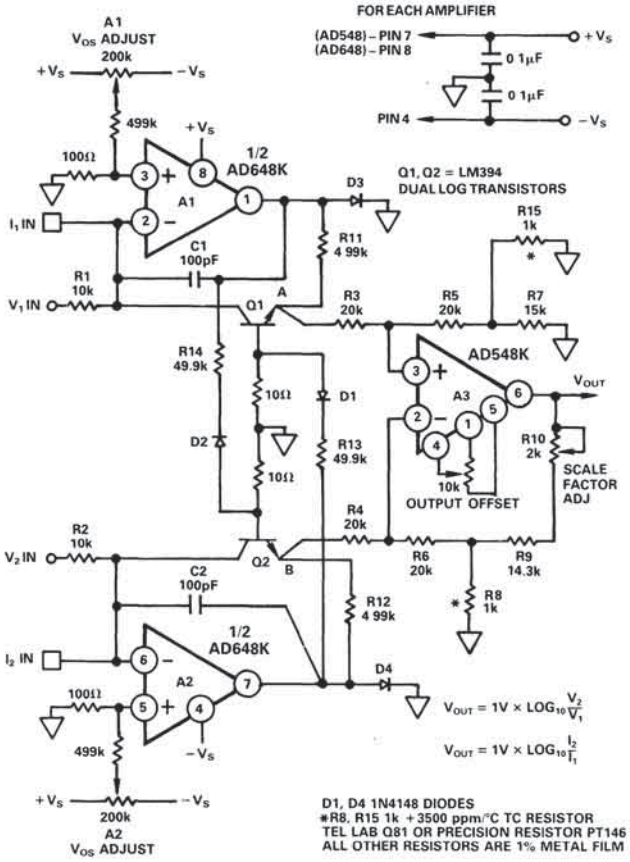


Figure 30. Precision Log Ratio Amplifier

ANALOG DEVICES

Ultralow-Drift Op Amp

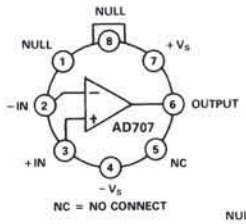
AD707

FEATURES

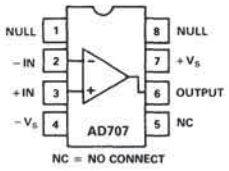
Very High dc Precision
15μV max Offset Voltage
0.1μV/°C max Offset Voltage Drift
0.35μV p-p max Voltage Noise (0.1Hz to 10Hz)
8 V/μV min Open-Loop Gain
130dB min CMRR
120dB min PSRR
1nA max Input Bias Current

AC Performance
0.3V/μs Slew Rate
0.9MHz Closed Loop-Bandwidth

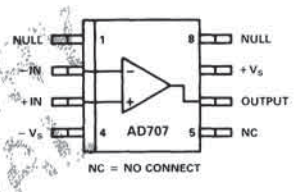
AD707 CONNECTION DIAGRAMS



TO-99 (H) Package



Plastic (N), and Cerdip (Q) Packages



Small Outline (R) Package

PRODUCT DESCRIPTION

The AD707 is a low-cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15μV is the best available in a bipolar op amp, and maximum input offset current is 1.0nA. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1μV/°C, and offset current drift and input bias current drift are both specified at 25pA/°C maximum.

The AD707's open-loop gain is 8V/μV minimum over the full ±10V output range when driving a 1kΩ load. Maximum input voltage noise is 350nVp-p (0.1Hz to 10Hz). CMRR and PSRR are 130dB and 120dB minimum respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline, hermetic cerdip and hermetic TO-99 metal can packages. Chips and Mil Standard/883 parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13V/μV typical open-loop gain and 140dB typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77 and the LT1001.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

	Conditions	AD707J/A Min	AD707J/A Typ	AD707J/A Max	AD707K/B/S Min	AD707K/B/S Typ	AD707K/B/S Max	AD707C/T Min	AD707C/T Typ	AD707C/T Max	Units
INPUT OFFSET VOLTAGE											
Initial			30	**90**		10	**25**		5	**15**	μV
vs Temperature			0.3	1 0		0.1	**0.3**		0.03	**0.1**	μV/°C
	$T_{min}-T_{max}$		50	100		15	**45**		7/8/8	**25**	μV
Long-Term Stability			0.3			0 3			0.2		μV/month
Adjustment Range	R_P 20kΩ		±4			±4			±4		mV
INPUT BIAS CURRENT			1 0	**2.5**		0 5	**1.5**		0 5	**1.0**	nA
	$T_{min}-T_{max}$		2.0	4 0		1 5	**3.0**		1.0	**2.0**	nA
Average Drift			15	40		15	25/25/35		10	25	pA/°C
OFFSET CURRENT	V_{CM} 0V		0.5	**2.0**		0 3	**1.5**		0.1	**1.0**	nA
	$T_{min}-T_{max}$		2.0	4.0		1 0	**2.0**		0.2	**1.5**	nA
Average Drift			2	40		1	25/25/35		1	25	pA/°C
INPUT VOLTAGE NOISE	0 1 to 10Hz		0.23	0.6		0.23	0.6		0 23	**0.35**	μV p-p
	f 10Hz		10 3	15		10 3	14		10 3	13	nV/√Hz
	f 100Hz		10.0	13 0		10.0	12		10.0	11 0	nV/√Hz
	f 1kHz		9 6	11 0		9 6	11 0		9 6	11 0	nV/√Hz
INPUT CURRENT NOISE	0 1Hz to 10Hz		14	35		14	30		14	**30**	pA p-p
	f 10Hz		0 32	0 9		0.32	0 8		0 32	0.8	pA/√Hz
	f 100Hz		0 14	0 27		0 14	0 23		0 14	0 23	pA/√Hz
	f 1kHz		0 12	0 18		0 12	0.17		0 12	0 17	pA/√Hz
COMMON-MODE REJECTION RATIO	V_{CM} ±13V	**120**	140		**130**	140		**130**	140		dB
	T_{min} to T_{max}	120	140		**130**	140		**130**	140		dB
OPEN-LOOP GAIN	V_O ±10V										
	$R_{LOAD}\geq 2k\Omega$	**3**	13		**5**	13		**8**	13		V/μV
	T_{min} to T_{max}	3	13		5	13		8	13		V/μV
	$R_{LOAD}\geq 1k\Omega$	**3**	13		5	13		8	13		V/μV
POWER SUPPLY REJECTION RATIO	V_S ±3V to ±18V	**110**	130		**115**	130		**120**	130		dB
	T_{min} to T_{max}	110	130		**115**	130		**120**	130		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth			0,5	0 9		0.5	0.9		0 5	0 9	MHz
Slew Rate			0 15	0 3		0.15	0.3		0 15	0.3	V/μs
INPUT RESISTANCE											
Differential			24	100		45	200		60	200	MΩ
Common Mode				200			300			400	GΩ
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq 10k\Omega$	**13.5**	14		**13.5**	14		**13.5**	14		±V
	$R_{LOAD}\geq 2k\Omega$	**12.5**	13.0		**12.5**	13 0		**12.5**	13.0		±V
	$R_{LOAD}\geq 1k\Omega$	**12.0**	12.5		**12.0**	12 5		**12.0**	12.5		±V
	$R_{LOAD}\geq 2k\Omega$ T_{min} to T_{max}	12 0	13.0		**12.0**	13.0		**12.0**	13.0		±V
OPEN-LOOP OUTPUT Resistance			60			60			60		Ω
POWER SUPPLY											
Current, Quiescent			2.5	**3**		2.5	**3**		2.5	**3**	mA
Power Consumption	V_S ±15V,										
	No Load		70	**90**		70	**90**		70	**90**	mW
	V_S ±3V		7.2	**9.0**		7 2	**9.0**		7 2	**9.0**	mW
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial	0 to +70°C	AD707JN, AD707JR			AD707KN, AD707KR[1]						
Industrial	−40°C to +85°C	AD707AQ, AD707AH			AD707BQ, AD707BH			AD707CQ, AD707CH			
Military	−55°C to +125°C				AD707SQ, AD707SH			AD707TQ, AD707TH			
PACKAGE OPTIONS[2]											
Plastic (N-8)		AD707JN			AD707KN						
Cerdip (Q-8)		AD707AQ			AD707BQ/SQ			AD707CQ/TQ			
TO-99 (H-08A)		AD707AH			AD707BH/SH			AD707CH/TH			
SOIC (R-8)		AD707JR			AD707KR						

NOTES

[1]AD707KR parts are production tested at +25°C only. All T_{min} to T_{max} specifications are guaranteed but not 100% tested.

[2]See Section 16 for package outline information

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels

Specifications are subject to change without notice

Dual Ultralow Drift Op Amp

AD708

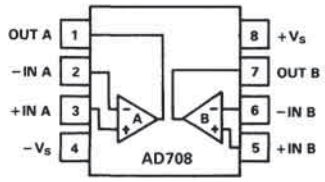
FEATURES

Very High dc Precision
30μV max Offset Voltage
0.3μV/°C max Offset Voltage Drift
0.35μV p-p max Voltage Noise (0.1 to 10Hz)
8 Million V/V min Open Loop Gain
130dB min CMRR
120dB min PSRR
Matching Characteristics
- **30μV max Offset Voltage Match**
- **0.3μV/°C max Offset Voltage Drift Match**
- **140dB min CMRR Match**

AC PERFORMANCE
0.3V/μs Slew Rate
0.9MHz Closed-Loop Bandwidth
Single: AD707
Available in 8-Pin Plastic Mini-DIPs and Hermetic Cerdip and TO-99 Metal Can Packages

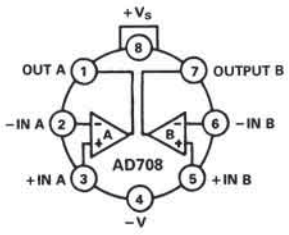
AD708 CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



TOP VIEW

TO-8 (H) Package



TOP VIEW

NOTE PIN 4 CONNECTED TO CASE

PRODUCT DESCRIPTION

The AD708 is a dual precision, low offset voltage and low offset voltage drift, monolithic operational amplifier. Each amplifier individually offers excellent dc precision and all important dc specifications show excellent stability over temperature. The offset voltage drift match of 0.3μV/°C and offset voltage match of 30μV are the best available matching specifications for any dual bipolar op amp.

The AD708 sets a new standard for dual precision op amps by providing 8V/μV min open loop gain and guaranteed max input voltage noise of 350nV p-p. Input bias current is 1.0nA max guaranteed. Offset current drift is typically 1pA/°C and input bias current drift is 25pA/°C max. Both CMRR (130dB min) and PSRR (120dB min) are an order of magnitude improved over any available single monolithic op amp except the AD707.

The AD708 is available in six performance grades. The AD708J and AD708K are rated over the commercial temperature range of 0 to +70°C and are available in plastic mini-DIP, cerdip, and TO-99 packages. The AD708A and AD708B are rated over the industrial temperature range of −40°C to +85°C and are available in cerdip and TO-99 packages. The AD708S and AD708T are rated over the military temperature range of −55°C to +125°C and are available in cerdip and TO-99 packages. Military versions are available processed to MIL-STD-883B, Rev. C..

APPLICATION HIGHLIGHTS

1. The AD708's 13V/μV typical open loop gain and 140dB common-mode rejection make it ideal for precision instrumentation applications.
2. The combination of outstanding matching and individual specfications makes the AD708 ideal for constructing high gain, precision instrumentation amplifiers.
3. The low offset voltage drift and noise of the AD708 allows the designer to amplify very small signals without sacrificing overall system preformance.
4. Unmounted dice are available for hybrid circuit applications.
5. The AD708 is an improved replacement for the OP-207 and the LT1002.

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD708J/A/S Min	AD708J/A/S Typ	AD708J/A/S Max	AD708K/B/T Min	AD708K/B/T Typ	AD708K/B/T Max	Units
INPUT OFFSET VOLTAGE			30	**100**		5	**30**	μV
	$T_{min}-T_{max}$		50	125/145/170		15	**60**	μV
Drift			0.3	0.7		0.1	**0.3**	μV/°C
Long-Term Stability			0.3			0.3		μV/month
INPUT BIAS CURRENT			1.0	**2.5**		0.5	**1.0**	nA
	$T_{min}-T_{max}$		2.0	4.0		1.0	**2.0**	nA
Average Drift			15	40		10	25	pA/°C
OFFSET CURRENT	$V_{CM}=0V$		0.5	**2.0**		0.1	**1.0**	nA
	$T_{min}-T_{max}$		2.0	4.0		0.2	**1.5**	nA
Average Drift			2	60		1	25	pA/°C
MATCHING CHARACTERISTICS								
Offset Voltage				**80**			**30**	μV
	$T_{min}-T_{max}$			180			**60**	μV
Offset Voltage Drift				1.0			**0.3**	μV/°C
Input Bias Current				4.0			**2.0**	nA
	$T_{min}-T_{max}$			5.0			**5.0**	nA
Common-Mode Rejection		**120**	150		**140**	150		dB
	$T_{min}-T_{max}$	115			**130**			dB
Power Supply Rejection		**110**			**120**			dB
	$T_{min}-T_{max}$	110			**120**			dB
Channel Separation		**130**			**130**			dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		0.23	0.6		0.23	0.35	μV p-p
	f = 10Hz		10.3	18		10.3	12	$nV/\sqrt{Hz}$
	f = 100Hz		10.0	13.0		10.0	11.0	$nV/\sqrt{Hz}$
	f = 1kHz		9.6	11.0		9.6	11.0	$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	0.1Hz to 10Hz		14	35		14	30	pA p-p
	f = 10Hz		0.32	0.9		0.32	0.8	$pA/\sqrt{Hz}$
	f = 100Hz		0.14	0.27		0.14	0.23	$pA/\sqrt{Hz}$
	f = 1kHz		0.12	0.18		0.12	0.17	$pA/\sqrt{Hz}$
COMMON-MODE								
Rejection Ratio	$V_{CM}=\pm 13V$	**120**	140		**130**	140		dB
	T_{min} to T_{max}	120	140		**130**	140		dB
OPEN LOOP GAIN	$V_O=\pm 10V$,							
	$R_{LOAD}\geq 2k\Omega$	**3**	13		**8**	13		V/μV
	T_{min} to T_{max}	3	13		**8**	13		V/μV
	$R_{LOAD}\geq 1k\Omega$	**3**	13		**8**	13		V/μV
POWER SUPPLY								
Rejection Ratio	$V_S=+3V$ to $+18V$	**110**	130		**120**	130		dB
	T_{min} to T_{max}	110	130		**120**	130		dB
FREQUENCY RESPONSE								
Closed Loop Bandwidth		0.5	0.9		0.5	0.9		MHz
Slew Rate		0.15	0.3		0.15	0.3		V/μs
INPUT RESISTANCE								
Differential		20	60		50	200		MΩ
Common Mode			200			400		GΩ
OUTPUT VOLTAGE	$R_{LOAD}\geq 10k\Omega$	**13.5**	14		**13.5**	14		±V
	$R_{LOAD}\geq 2k\Omega$	**12.5**	13.0		**12.5**	13.0		±V
	$R_{LOAD}\geq 1k\Omega$	**12.0**	12.5		**12.0**	12.5		±V
	$R_{LOAD}\geq 2k\Omega$							
	T_{min} to T_{max}	12.0	13.0		**12.0**	13.0		±V
OPEN LOOP OUTPUT								
Resistance			60			60		Ω
POWER SUPPLY								
Current, Quiescent			4.5	5.5		4.5	5.5	mA
Power Consumption	$V_S=\pm 15V$,							
	No Load		135	165		135	165	mW
	$V_S=\pm 3V$		12	**18**		12	**18**	mW
Operating Range		±3		±22	±3		±22	V
PACKAGE OPTIONS[1]								
Plastic (N-8)		AD708JN			AD708KN			
Cerdip (Q-8)		AD708JQ/AQ/SQ			AD708KQ/BQ/TQ			
TO-99 (H-08A)		AD708JH/AH/SH			AD708KH/BH/TH			

NOTE

[1]See Section 16 for package outline information

Specifications subject to change without notice

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

PRELIMINARY TECHNICAL DATA

Precision Low-Cost High-Speed BiFET Op Amp

AD711

FEATURES

AC PERFORMANCE:
- Settles to ±0.01% in 1μs
- 16V/μs min Slew Rate (AD711J)
- 3MHz min Unity Gain Bandwidth (AD711J)

DC PERFORMANCE:
- 0.25mV max Offset Voltage: (AD711C)
- 3μV/°C max Drift: (AD711C)
- 200V/mV min Open-Loop Gain (AD711K)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD711C)

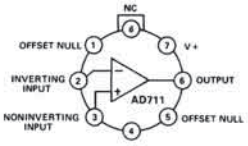
Available in Plastic Mini-DIP, Plastic SO, Hermetic Cerdip, and Hermetic Metal Can Packages

MIL-STD-883B Parts Available

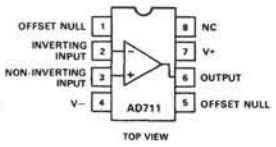
Dual Version Available: AD712

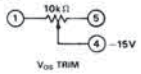
AD711 CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Small Outline (R) and Cerdip (Q) Packages





PRODUCT DESCRIPTION

The AD711 is a high-speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S and AD711T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD711 is available in an 8-pin plastic mini-DIP, 8-pin small outline, cerdip, or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3μV/°C max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and an input offset current of 10pA max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.
6. Available in chip form.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD711J/A/S			AD711K/B/T			AD711C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**2/1/1**		0.2	**0.5**		0.1	**0.25**	mV
T_{min} to T_{max}			3/2/2			**1.0**			**0.45**	mV
vs. Temp.		7	20/20/**20**		5	**10**		2	**3**	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**86**			dB
Long Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		15	**50**		15	**50**		15	**25**	pA
Either Input at T_{max}, V_{CM} = 0 (70°C/85°C/125°C)			1.1/3.2/51			1.1/3.2/51			1.6	nA
Either Input, V_{CM} = + 10V		20	**100**		20	**100**		20	**50**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max} (70°C/85°C/125°C)			0.57/1.6/26			0.57/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%[3]		1	1.2		1	1 2		1	1 2	µs
Total Harmonic Distortion f = 1kHz										
$R_L \geq 2k\Omega$, V_O = 3V RMS		0.0003			0 0003			0 0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5\ 5$		Ω‖pF
Common-Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5\ 5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		± 20			± 20			± 20		V
Common-Mode Voltage Over Max Operating Range[5]	$-V_S+4V$	+ 14.5, − 11.5	$+V_S-2V$	$-V_S+4V$	+ 14.5, − 11 5	$+V_S-2V$	$-V_S+4V$	+ 14.5, 11 5	$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ± 10V	**76**	88		**80**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ± 11V	**70**	84		**76**	84		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4.0**	µV p-p
f = 10Hz		45			45			45		$nV/\sqrt{Hz}$
f = 100Hz		22			22			22		$nV/\sqrt{Hz}$
f = 1kHz		18			18			18		$nV/\sqrt{Hz}$
f = 10kHz		16			16			16		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0 01		$pA/\sqrt{Hz}$
OPEN LOOP GAIN[6]										
V_O = ± 10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
V_O = ± 10V, $R_L \geq 2k\Omega$, T_{min} to T_{max}	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+ 13.9, − 13.3		**+13, −12.5**	+ 13.9, − 13 3		**+13, −12.5**	+ 13.9, − 13 3		V
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	± 12/± 12/**± 12**	+ 13.8, − 13 1		**± 12**	+ 13.8, − 13.1		**± 12**	+ 13 8, 13.1		V
Short-Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		± 15			± 15			± 15		V
Operating Range	**± 4.5**		**± 18**	**± 4.5**		**± 18**	**± 4.5**		**± 18**	V
Quiescent Current		2.5	**3.4**		2 5	**3.0**		2 5	**2.8**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to + 70°C)		AD711J			AD711K					
Industrial (− 40°C to + 85°C)		AD711A			AD711B			AD711C		
Military (− 55°C to + 125°C)		AD711S			AD711T					
PACKAGE OPTIONS[7]										
Plastic (N-8)		AD711JN			AD711KN					
SOIC (R-8)		AD711JR			AD711KR					
Cerdip (Q-8)		AD711AQ, AD711SQ			AD711BQ, AD711TQ			AD711CQ		
TO-99 (H-08A)		AD711AH, AD711SH			AD711BH, AD711TH			AD711CH		

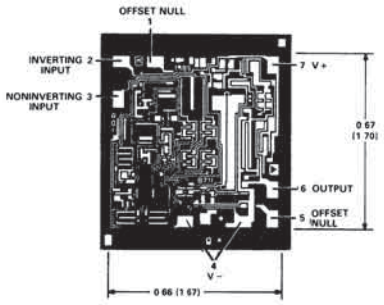
NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[3]Refer to Figure 29.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal
[6]Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[7]See Section 16 for package outline information

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Dimensions in inches and (mm).



2

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD711J/K	0 to +70°C
AD711A/B/C	−40°C to +85°C
AD711S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Typical Characteristics

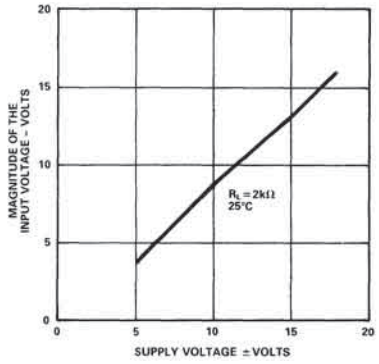


Figure 1. Input Voltage Swing vs. Supply Voltage

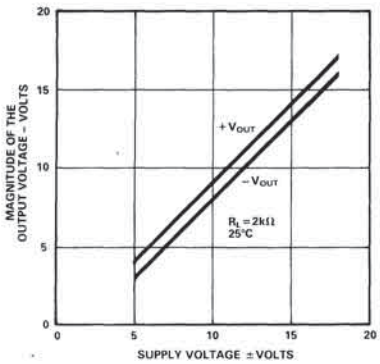


Figure 2. Output Voltage Swing vs. Supply Voltage

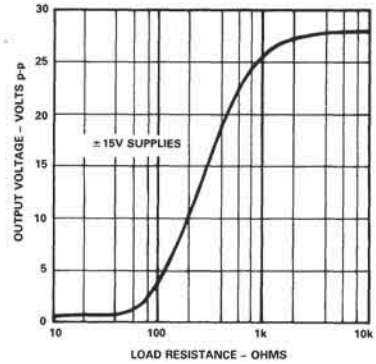


Figure 3. Output Voltage Swing vs. Resistive Load

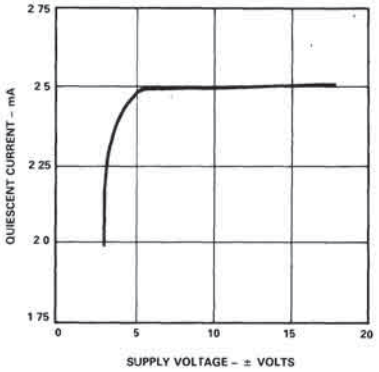


Figure 4. Quiescent Current vs. Supply Voltage

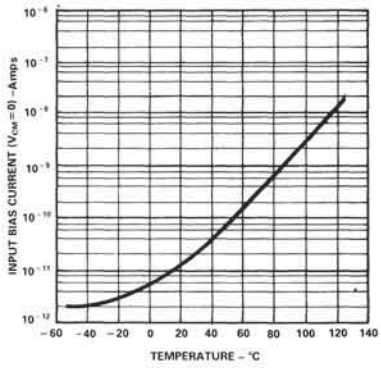


Figure 5. Input Bias Current vs. Temperature

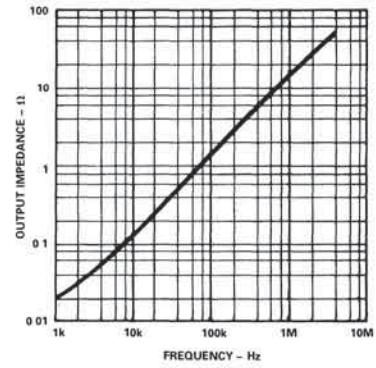


Figure 6. Magnitude of Output Impedance vs. Frequency

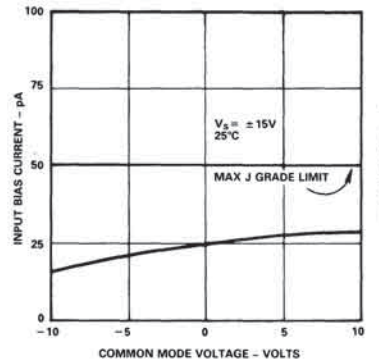


Figure 7. Input Bias Current vs. Common Mode Voltage

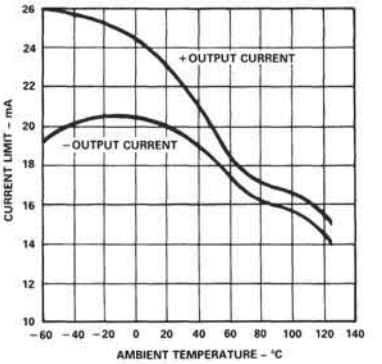


Figure 8. Short Circuit Current Limit vs. Temperature

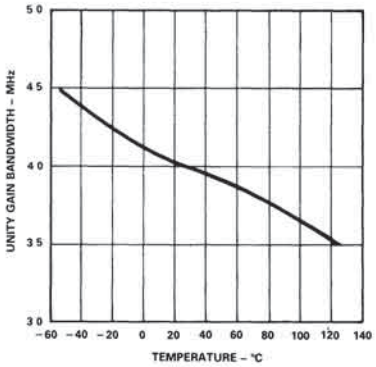


Figure 9. Unity Gain Bandwidth vs. Temperature

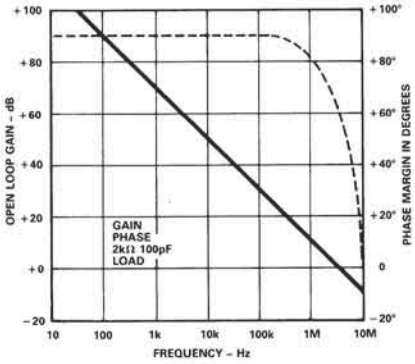


Figure 10. Open Loop Gain and Phase vs. Frequency

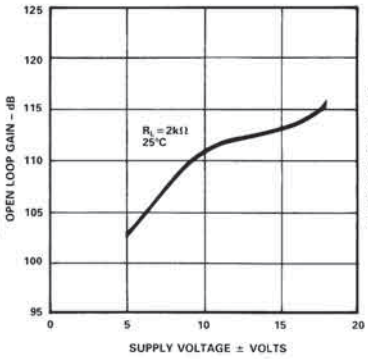


Figure 11. Open Loop Gain vs. Supply Voltage

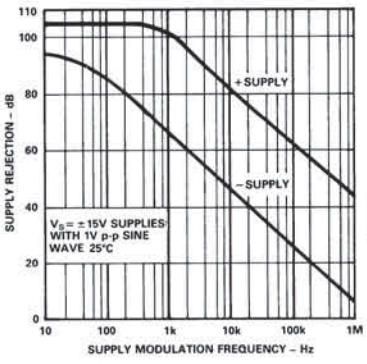


Figure 12. Power Supply Rejection vs. Frequency

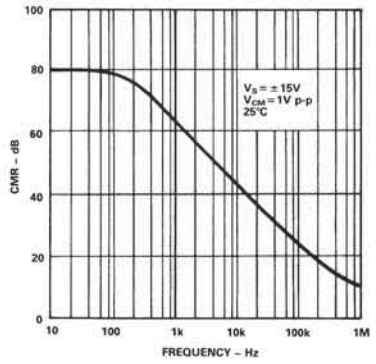


Figure 13. Common Mode Rejection vs. Frequency

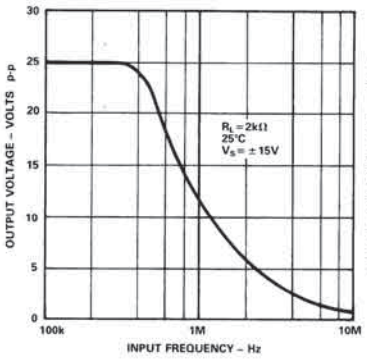


Figure 14. Large Signal Frequency Response

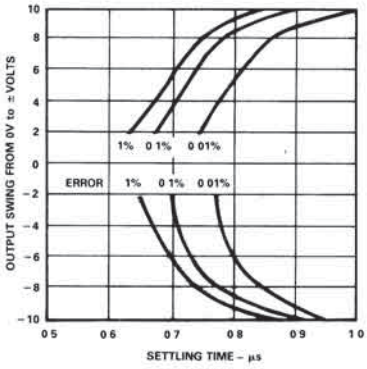


Figure 15. Output Swing and Error vs. Settling Time

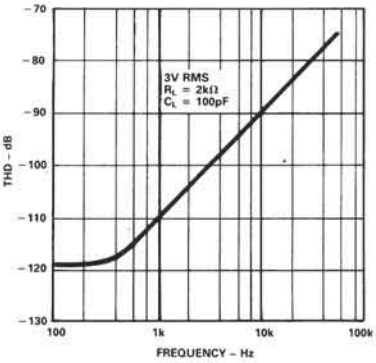


Figure 16. Total Harmonic Distortion vs. Frequency

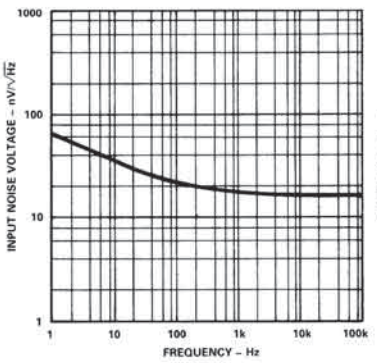


Figure 17. Input Noise Voltage Spectral Density

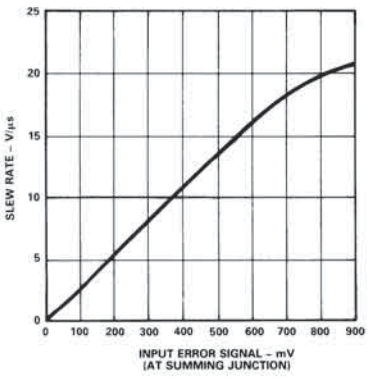


Figure 18. Slew Rate vs. Input Error Signal

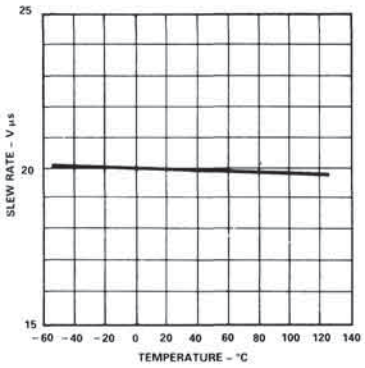


Figure 19. Slew Rate vs. Temperature

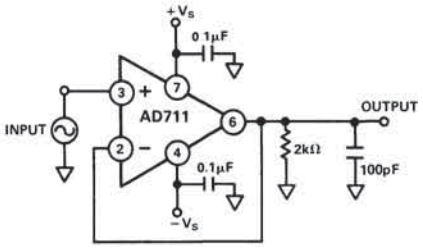


Figure 20. T.H.D. Test Circuit

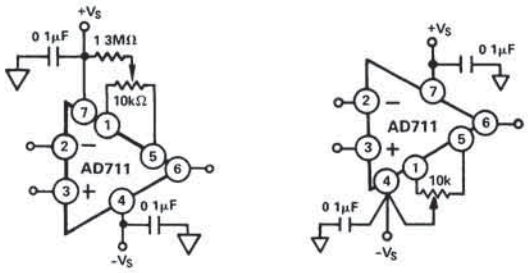


Figure 21. Offset Null Configurations

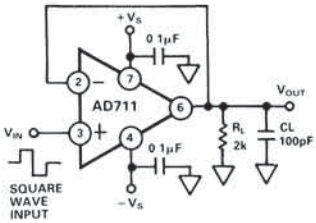


Figure 22a. Unity Gain Follower

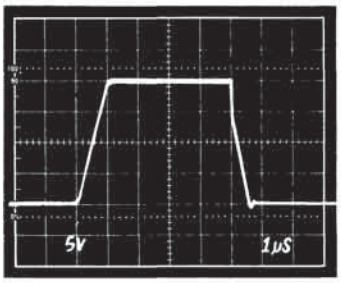


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

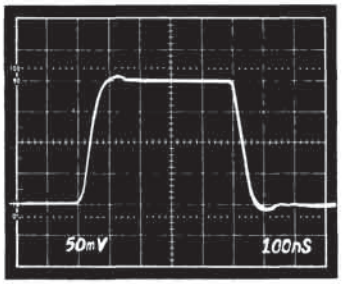


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

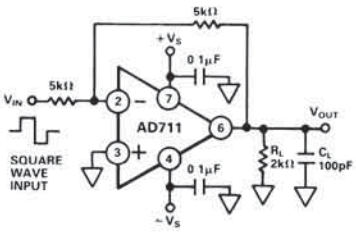


Figure 23a. Unity Gain Inverter

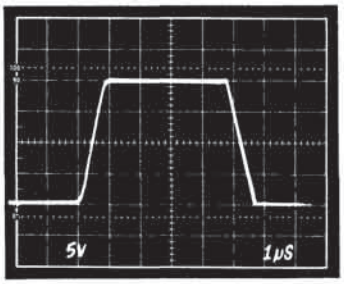


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

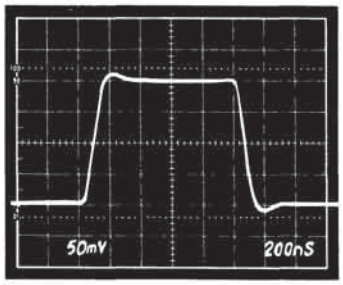


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD711 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD711 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedence together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD711 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD711/AD565 combination is 1.2 microseconds.

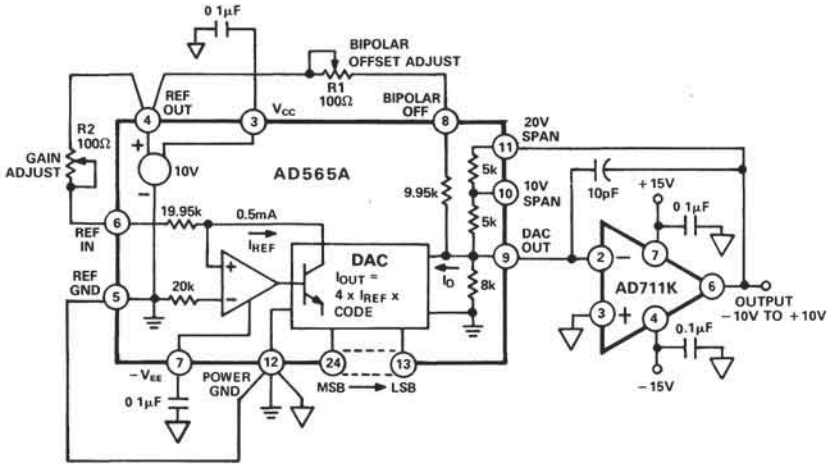
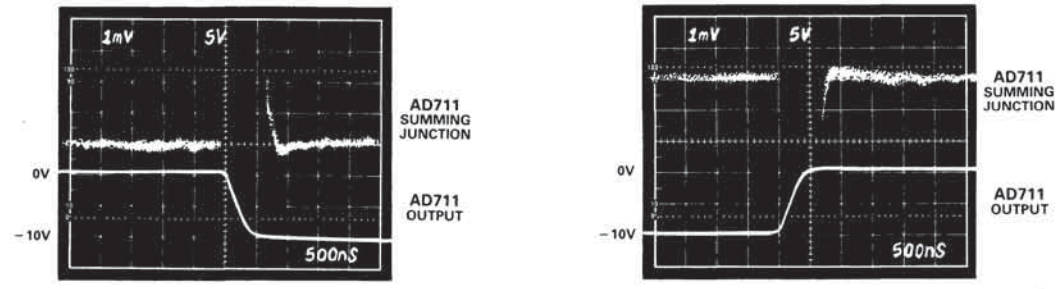


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)

b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD711 with AD565A

OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD711 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD711 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel)

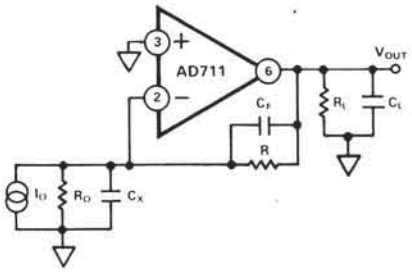


Figure 26a. Simplified Model of the AD711 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

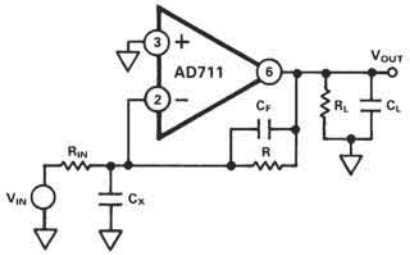


Figure 26b. Simplified Model of the AD711 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD711 with R = 4kΩ.

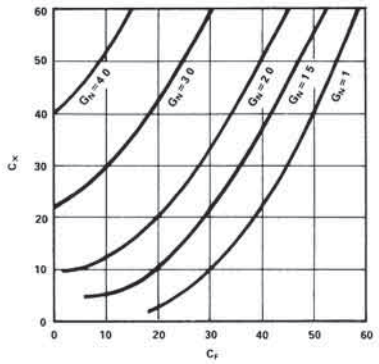


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD711 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

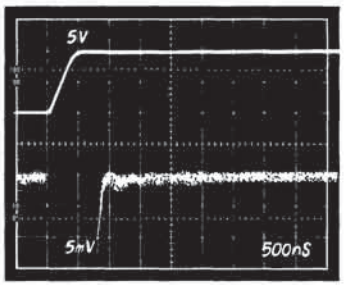


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

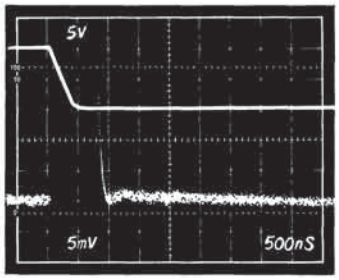


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

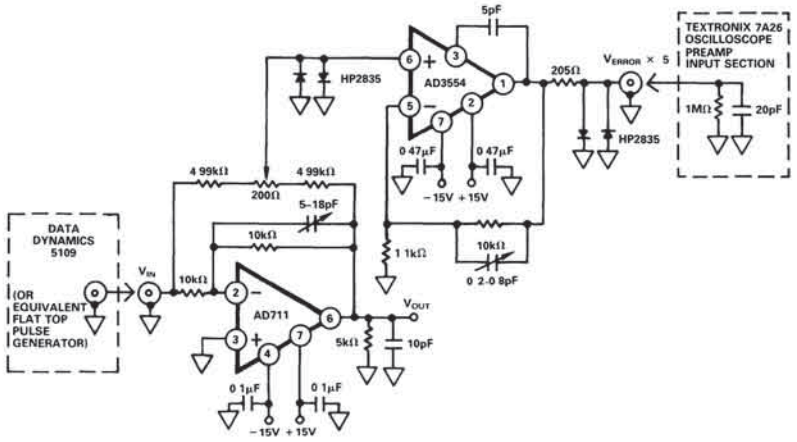


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD711 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

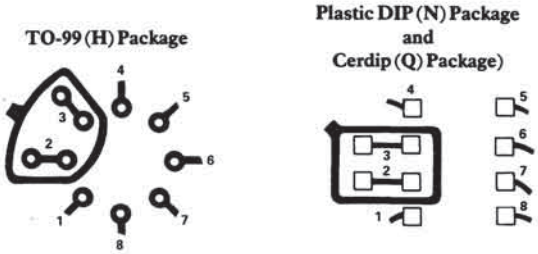


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD711 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD711K with guaranteed 500μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD711 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

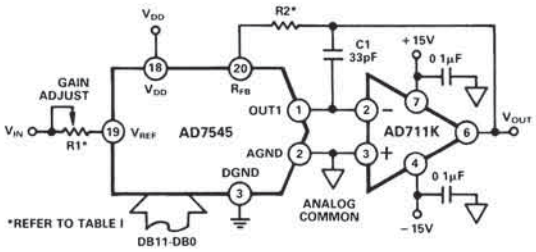


Figure 31. Unipolar Binary Operation

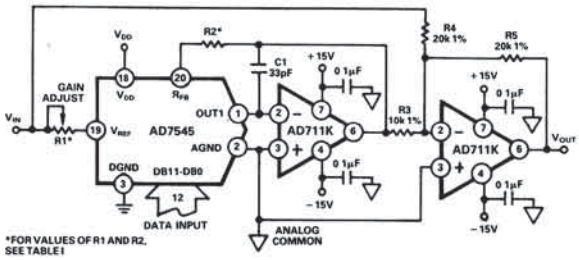


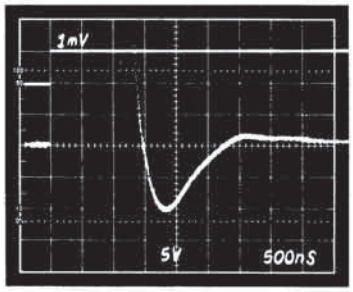
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

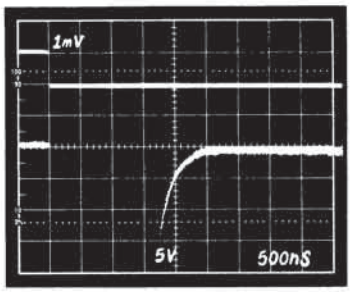
TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD711 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition



b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD711 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the I/F region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD711C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD711C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD711 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD711 is ideally suited to drive high speed A/D converters since it offers both wide bandwidth and high open-loop gain.

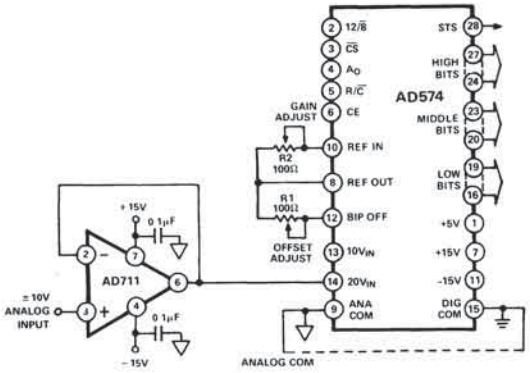
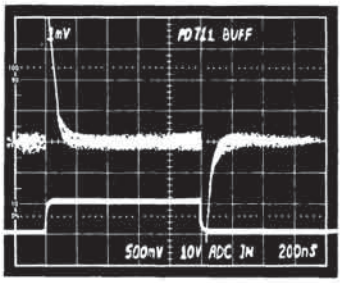
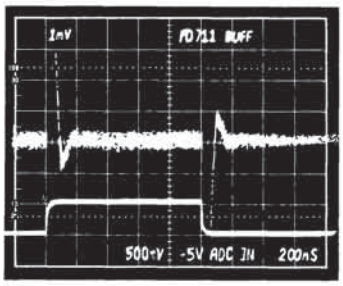


Figure 34. AD711 as ADC Unity Gain Buffer



a. Source Current = 2mA



b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

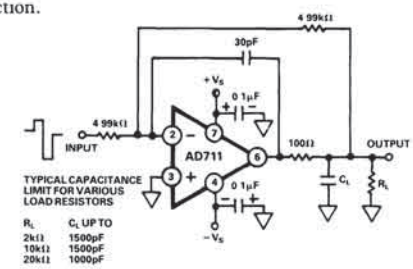


Figure 36. Circuit for Driving a Large Capacitive Load

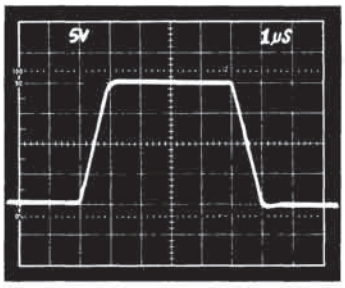


Figure 37. Transient Response R_L = 2kΩ, C_L =500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD711 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD711 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD711 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

R1 = R2 = user selected (typical values: 10kΩ – 100kΩ)

$$C1 = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)} \quad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

Where C1 and C2 are in farads.

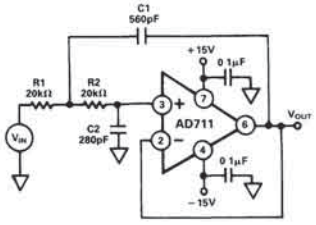


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD711 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low cost BiFET op amp showing 17dB more feedthrough at 5MHz.

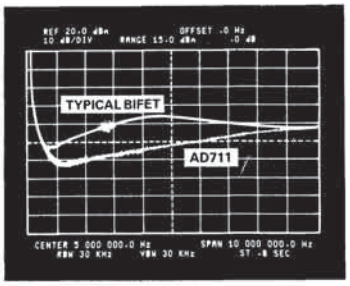


Figure 39.

9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD711 and its dual counterpart, the AD712, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

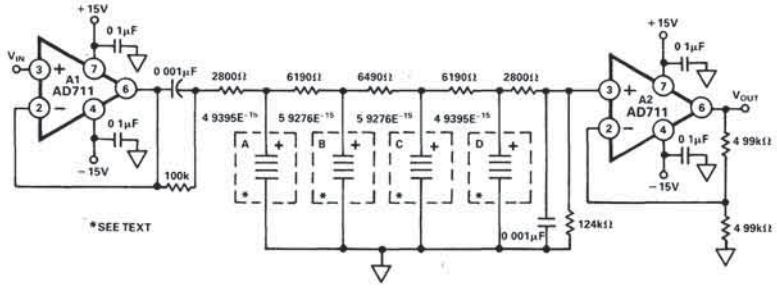


Figure 40. 9 Pole Chebychev Filter

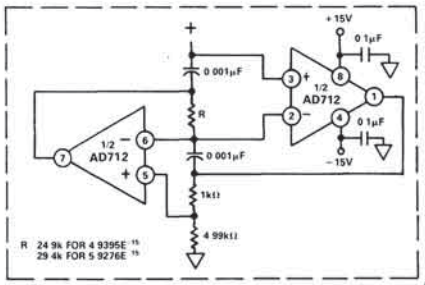


Figure 41. FDNR for 9 Pole Chebychev Filter

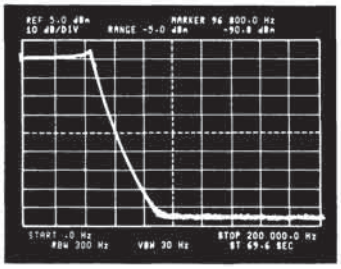


Figure 42. High Frequency Response for 9 Pole Chebychev Filter

Dual Precision High-Speed BiFET Op Amp

AD712

FEATURES

AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD712J)**
- **3MHz min Unity Gain Bandwidth (AD712J)**

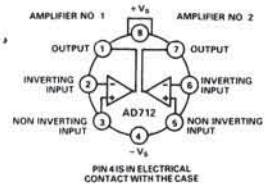
DC PERFORMANCE:
- **0.30mV max Offset Voltage: (AD712C)**
- **5μV/°C max Drift: (AD712C)**
- **200V/mV min Open Loop Gain (AD712K)**
- **4μV p-p max Noise, 0.1Hz to 10Hz (AD712C)**

Available in Plastic, Hermetic Cerdip, and Hermetic Metal Can Packages

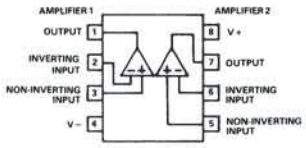
MIL-STD-883B Parts Available

AD712 FUNCTIONAL BLOCK DIAGRAM

TO-99
(H) Package



Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD712 is a high-speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD712 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0 to +70°C. The AD712A, AD712B and AD712C are rated over the industrial temperature range of −40°C to +85°C. The AD712S and AD712T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD712 is available in an 8-pin plastic mini-DIP, cerdip, or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.3mV max, C grade, 3mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 5μV/°C max on the AD712C.
3. Along with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD712 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD712C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 50pA max (AD712C) and an input offset current of 10pA max (AD712C). Both input bias current and input offset current are guaranteed in the warmed-up condition.
6. Available in chip form.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD712J/A/S			AD712K/B/T			AD712C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**3/1/1**		0.2	**1/0.7/0.7**		0.1	**0.30**	mV
T_{mun} to T_{max}			**4/2/2**			**2/1.5/1.5**			**0.60**	mV
vs. Temp.		7	**20/20/20**		7	**10**		3	**5**	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{mun} to T_{max}	**76/76/76**			**80**			**86**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		25	**75**		20	**75**		20	**50**	pA
Either Input at T_{max},										
V_{CM} = 0 (70°C/85°C/125°C)		0.6/1.6/26	1.7/4.8/77		0.5/1.3/20	1.7/4.8/77		1.3	3.2	nA
Either Input, V_{CM} = + 10V			**100**			**100**			**75**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)		0.3/0.7/11	0 6/1.6/26		0.1/0.3/5	0.6/1.6/26		0.3	0.7	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage			**3/1/1**			**1/0.7/0.7**			**0.3**	mV
Input Offset Voltage T_{mun} to T_{max}			**4/2/2**			**2/1.5/1.5**			**0.6**	mV
Input Offset Voltage vs. Temp			**20/20/20**			**10**			**5**	µV/°C
Input Bias Current			**25**			**25**			**10**	pA
Crosstalk[4] @ 1kHz		120			120			120		dB
@ 100kHz		90			90			90		dB
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%[5]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion										
f = 1kHz, $R_L \geq 2k\Omega$, V_O = 3V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[6]		± 20			± 20			± 20		V
Common-Mode Voltage										
Over Max Operating Range[7]	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ± 10V	**76**	88		**80**	88		**86**	94		dB
T_{mun} to T_{max}	**76/76/76**	84		**80**	84		**86**	90		dB
V_{CM} = ± 11V	**70**	84		**76**	84		**76**	90		dB
T_{mun} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4**	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN										
V_O = ± 10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
T_{mun} to T_{max}, $R_L \geq 2k\Omega$	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
T_{mun} to T_{max}	±12, ±12, **±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		± 15			± 15			± 15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current,										
Both Amplifiers		5	**6.8**		5	**6.0**		5	**5.6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to + 70°C)		AD712J			AD712K					
Industrial (− 40°C to + 85°C)		AD712A			AD712B			AD712C		
Military (− 55°C to + 125°C)		AD712S			AD712T					
PACKAGE OPTIONS[8]										
Plastic (N-8)		AD712JN			AD712KN					
Cerdip (Q-8)		AD712AQ, AD712SQ			AD712BQ, AD712TQ			AD712CQ		
TO-99 (H-08A)		AD712AH, AD712SH			AD712BH, AD712TH			AD712CH		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C
[3]Matching is defined as the difference between parameters of the two amplifers
[4]Refer to Figure 21
[5]Refer to Figure 29
[6]Defined as voltage between inputs, such that neither exceeds ± 10V from ground.
[7]Typically exceeding − 14.1V negative common-mode voltage on either input results in an output phase reversal
[8]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications in boldface are tested on all production units at final electrical test Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD712J/K	0 to +70°C
AD712A/B/C	−40°C to +85°C
AD712S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Typical Characteristics

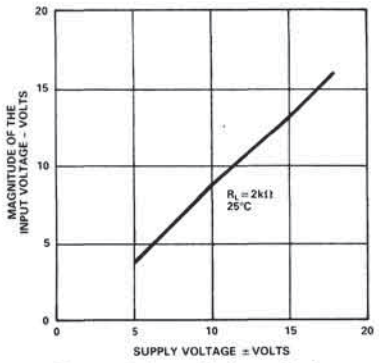


Figure 1. Input Voltage Swing vs. Supply Voltage

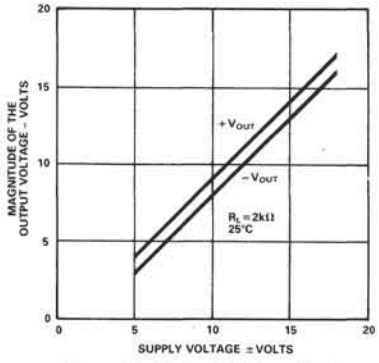


Figure 2. Output Voltage Swing vs. Supply Voltage

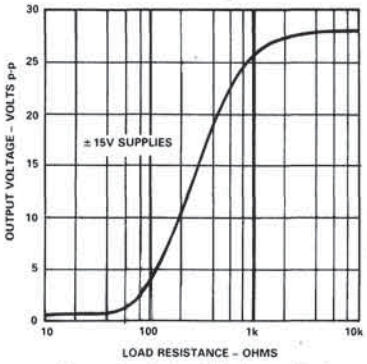


Figure 3. Output Voltage Swing vs. Resistive Load

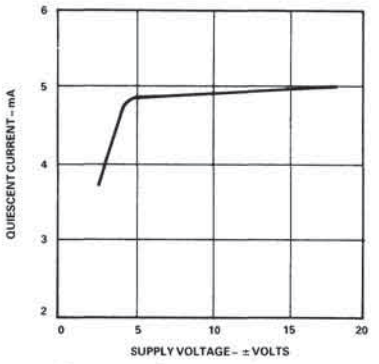


Figure 4. Quiescent Current vs. Supply Voltage

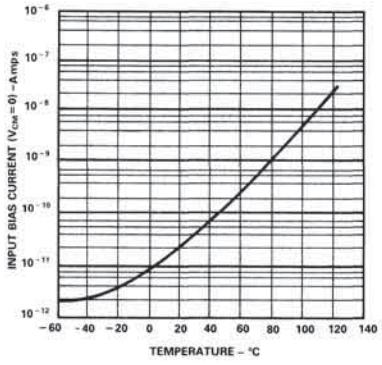


Figure 5. Input Bias Current vs. Temperature

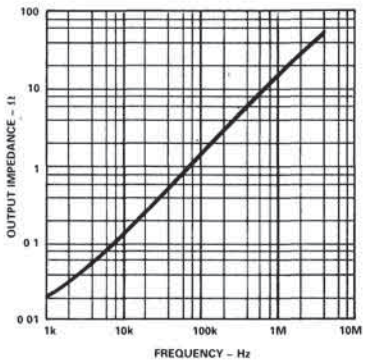


Figure 6. Magnitude of Output Impedance vs. Frequency

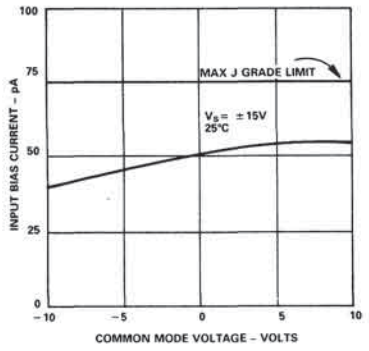


Figure 7. Input Bias Current vs. Common Mode Voltage

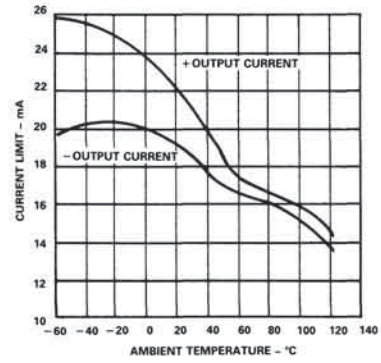


Figure 8. Short Circuit Current Limit vs. Temperature

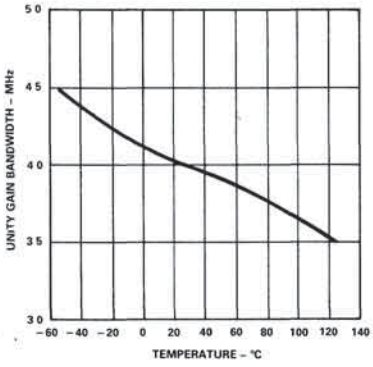


Figure 9. Unity Gain Bandwidth vs. Temperature

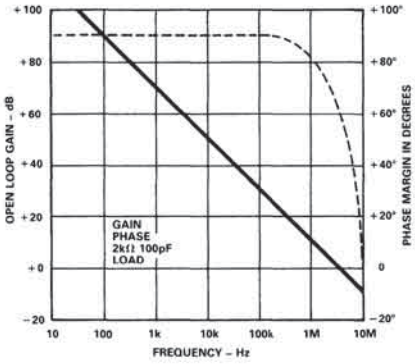


Figure 10. Open Loop Gain and Phase vs. Frequency

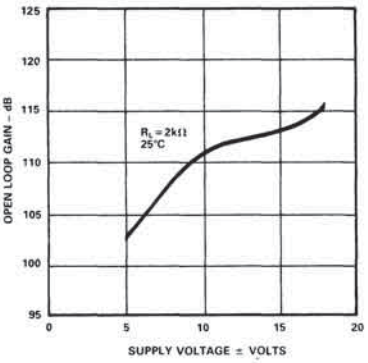


Figure 11. Open Loop Gain vs. Supply Voltage

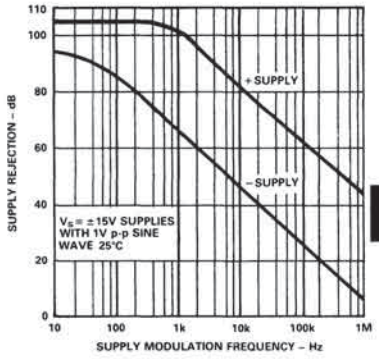


Figure 12. Power Supply Rejection vs. Frequency

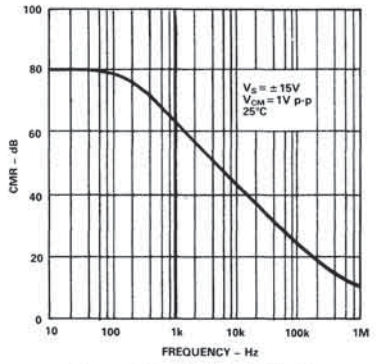


Figure 13. Common Mode Rejection vs. Frequency

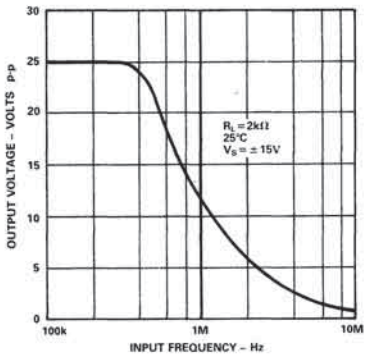


Figure 14. Large Signal Frequency Response

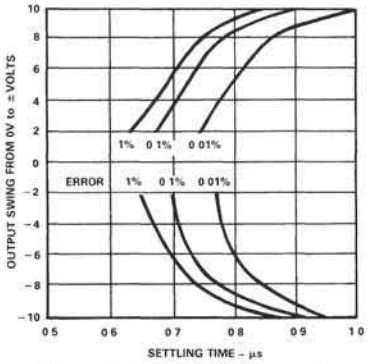


Figure 15. Output Swing and Error vs. Settling Time

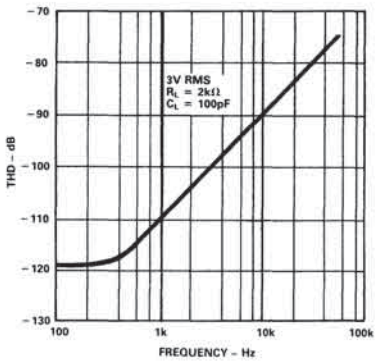


Figure 16. Total Harmonic Distortion vs. Frequency

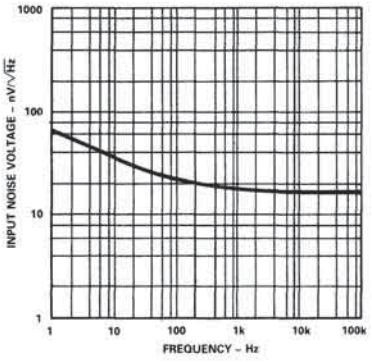


Figure 17. Input Noise Voltage Spectral Density

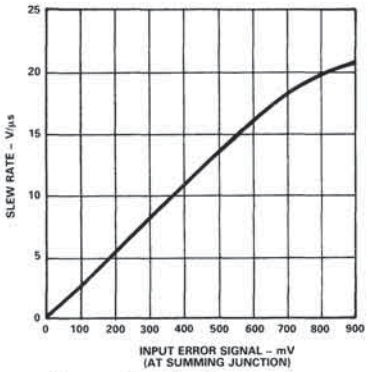


Figure 18. Slew Rate vs. Input Error Signal

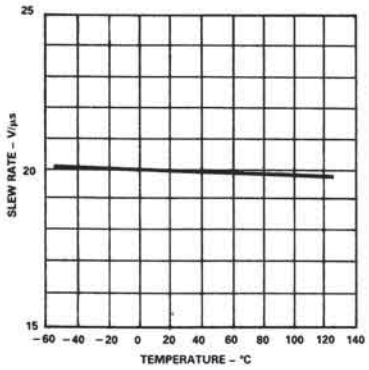


Figure 19. Slew Rate vs. Temperature

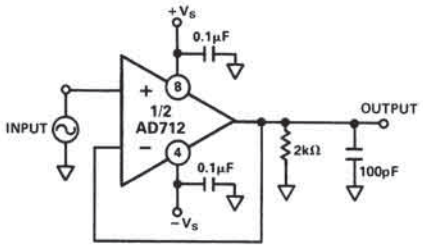


Figure 20. T.H.D. Test Circuit

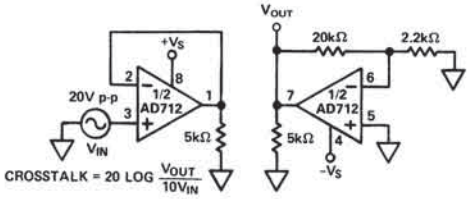


Figure 21. Crosstalk Test Circuit

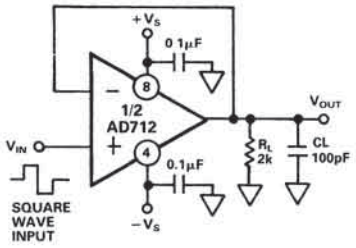


Figure 22a. Unity Gain Follower

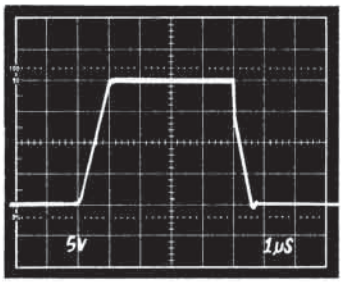


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

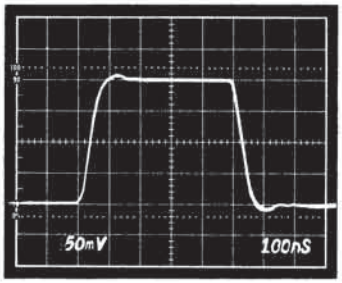


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

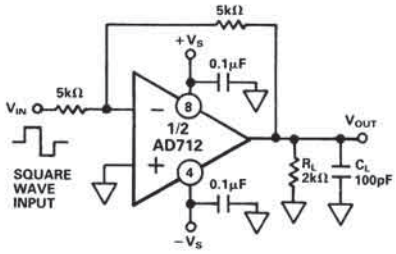


Figure 23a. Unity Gain Inverter

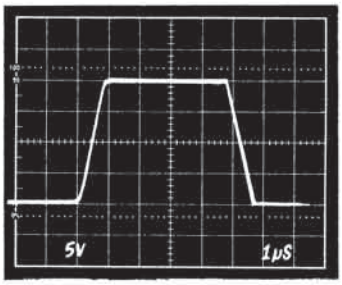


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

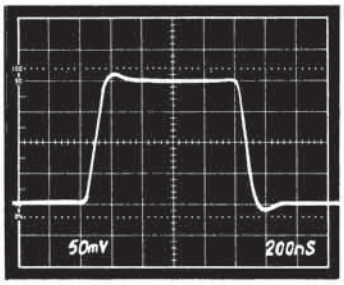


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op-amp is required for current-to-voltage conversion. The settling time of the converter/op-amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op-amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711/AD712 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD712 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD712 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op-amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op-amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op-amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD712 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD712/AD565 combination is 1.2 microseconds.

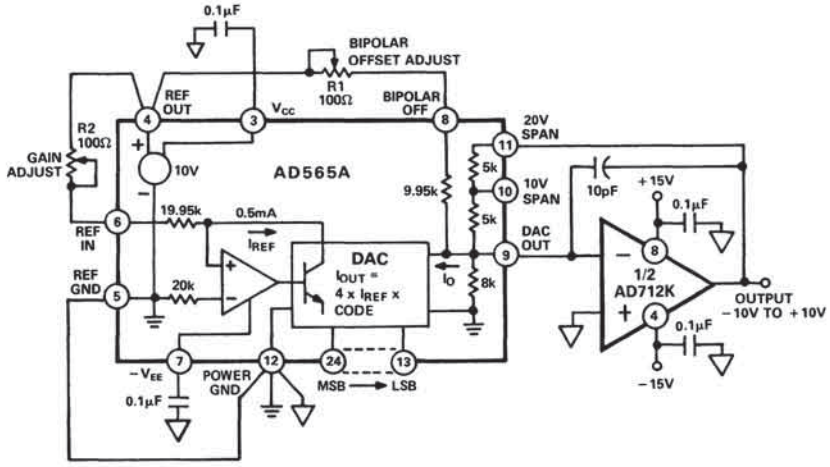
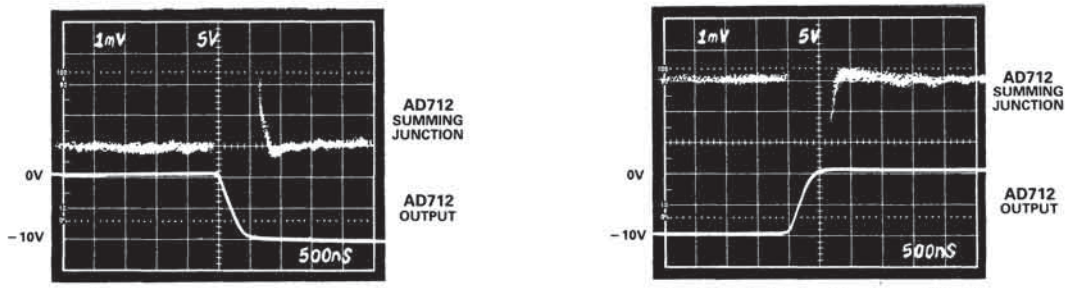


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)

b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD712 with AD565A

OP-AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD712 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD712 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op-amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op-amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op-amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1-G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op-amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op-amp (since the two are in parallel).

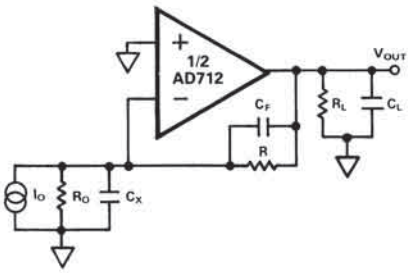


Figure 26a. Simplified Model of the AD712 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op-amp if a simple inverting op-amp is being simulated OR it is the combined capacitance of the DAC output and the op-amp input if the DAC buffer is being modeled.

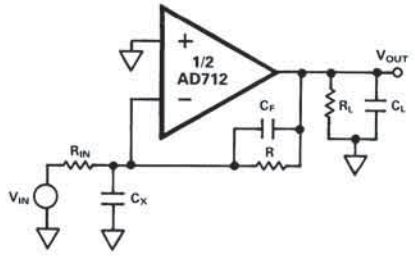


Figure 26b. Simplified Model of the AD712 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op-amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD712 with R = 4kΩ.

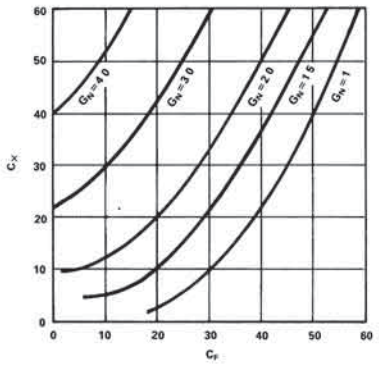


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD712 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high-speed, FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

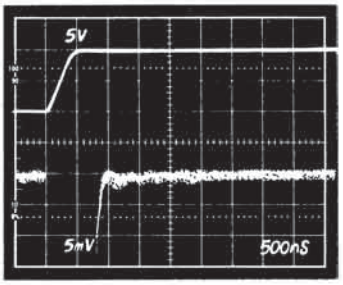


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

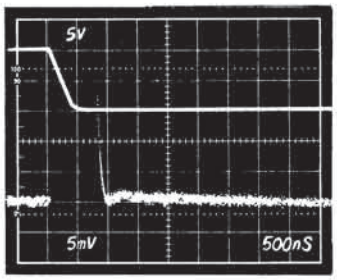


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

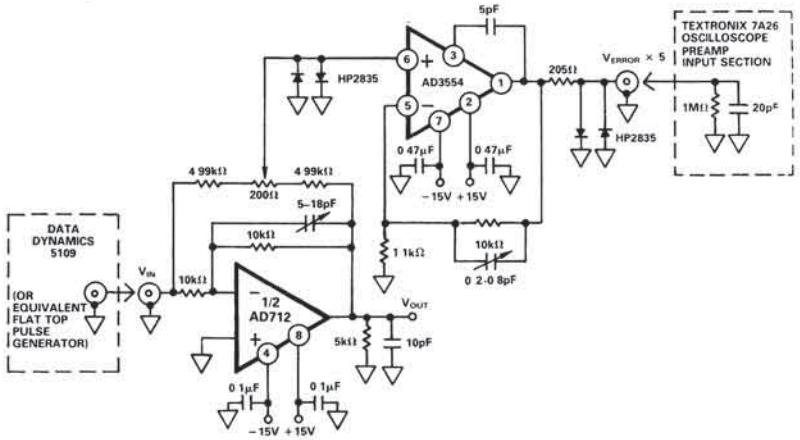


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD712 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

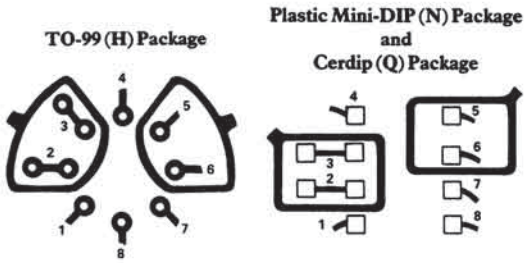


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD712 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD712K with guaranteed 700μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD712 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2 quadrant multiplication) or bipolar (4 quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

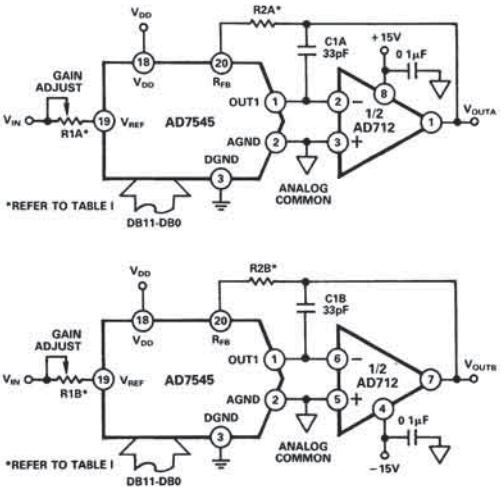


Figure 31. Unipolar Binary Operation

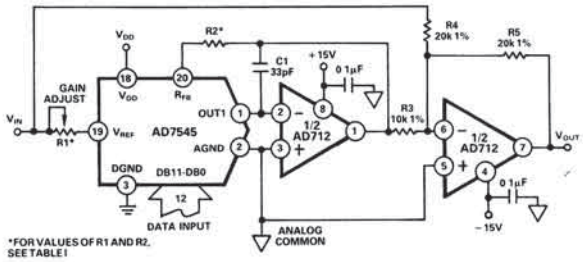


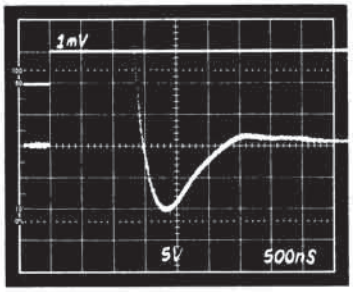
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

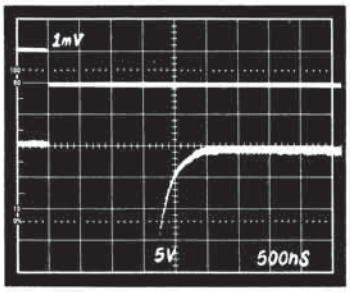
TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD712 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition



b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD712 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the I/F region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD712C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD712C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD712 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically-changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD712 is ideally suited to drive high-speed A/D converters since it offers both wide bandwidth and high open-loop gain.

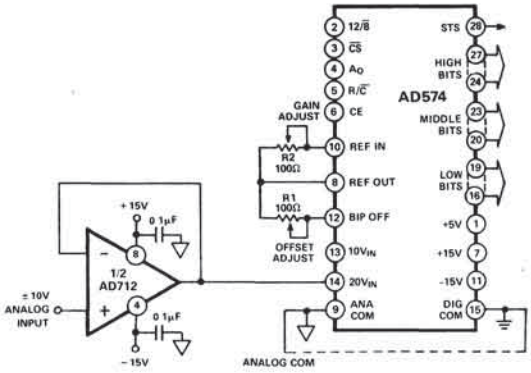
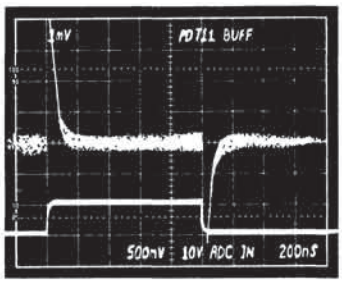
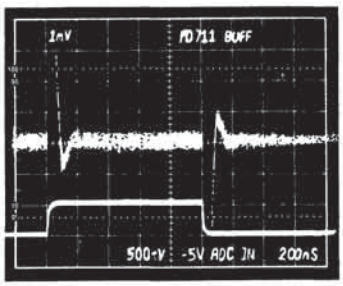


Figure 34. AD712 as ADC Unity Gain Buffer



a. Source Current = 2mA



b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

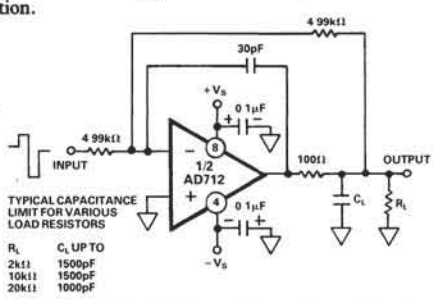


Figure 36. Circuit for Driving a Large Capacitive Load

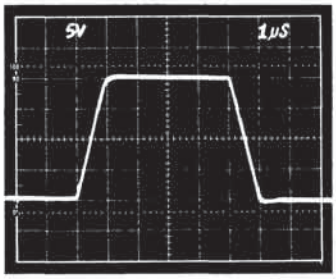


Figure 37. Transient Response R_L = 2kΩ, C_L = 500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the d.c. accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op-amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op-amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD712 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD712 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD712 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

R1 = R2 = user selected (typical values: 10kΩ – 100kΩ)

$$C1 \text{ (in farads)} = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)} \qquad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

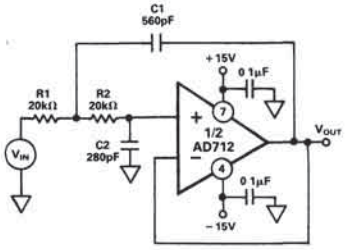


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD712 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low-cost BiFET op amp showing 17dB more feedthrough at 5MHz.

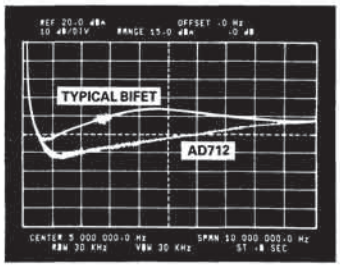


Figure 39.

9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD712 and its single counterpart, the AD711, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001µF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001µF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

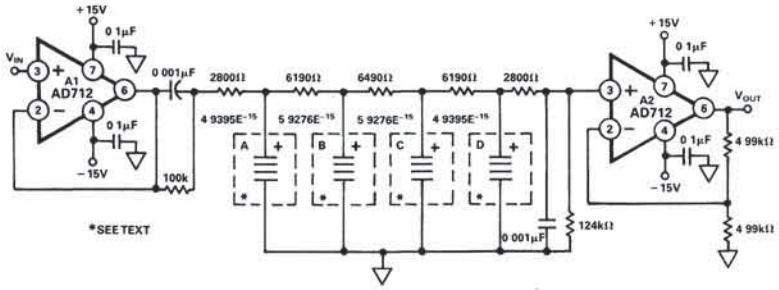


Figure 40. 9 Pole Chebychev Filter

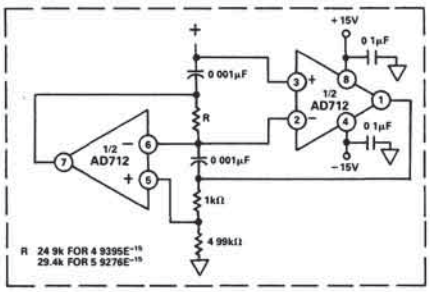


Figure 41. FDNR for 9 Pole Chebychev Filter

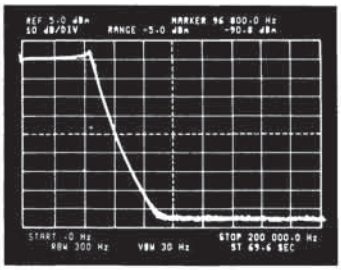


Figure 42. High Frequency Response for 9 Pole Chebychev Filter

Quad Precision High-Speed BiFET Op Amp

AD713

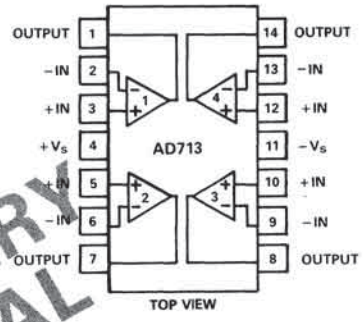
FEATURES

AC PERFORMANCE
- Settles to ±0.01% in 1μs
- 16V/μs min Slew Rate
- 3MHz min Unity Gain Bandwidth

DC PERFORMANCE
- 0.25mV max Offset Voltage
- 10μV/°C max Drift
- 200V/mV min Open Loop Gain
- 4μV p-p max Noise, 0.1Hz to 10Hz
- Single Version Available: AD711, Dual: AD712
- Available In Plastic and Hermetic Cerdip Packages
- MIL-STD-883B Parts Available

AD713 FUNCTIONAL BLOCK DIAGRAM

Plastic DIP (N) Package
and
Cerdip (Q) Package



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD713 is comprised of four high-speed precision, FET input operational amplifiers on one monolithic die. The AD713 offers superior ac and dc performance in a low cost quad op amp. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs, while still allowing the cost and board space savings of a quad op amp.

The combination of Analog Devices' advanced processing technology, laser-wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage (0.25mV, C Grade), input bias current 100pA, C Grade), and input offset current (15pA, C Grade) are specified in the warmed-up condition and are 100% tested. In addition, the AD713 has a guaranteed and tested max voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD713C).

Along with dc precision, the AD713 offers exceptional dynamic response. It settles to 0.01% in 1μs and has a 100% tested minimum slew rate of 18V/μs (AD713B).

The AD713 is pinned out in a standard quad op amp configuration and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0 to +70°C. The AD713A, AD713B and AD713C are rated over the industrial temperature range of −40°C to +85°C. The AD713S and AD713T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C. The AD713 is available in an 14-pin plastic DIP or 14-pin cerdip.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

PRODUCT HIGHLIGHTS

1. Active Filters: The superior ac and dc performance of this op amp make it well-suited for active filter applications.
2. Buffers: With a slew rate of 16V/μs and a settling time of 1μs to 0.01%, the AD713 is ideal as a buffer for A/D and quad D/A converters.
3. Precision Data Acquisition Systems: Common-mode rejection of 88dB and open-loop gain of 400V/mV ensure 12-bit accuracy even in high-speed data acquisition circuits.
4. Photodiode Preamps: The combination of excellent noise performance and low input current makes the AD713 useful as a photodiode preamp.
5. The AD713 is an enchanced replacement for the TL074, LF414 and other quad op amps in applications where precision and demanding ac performance are essential.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	AD713C Min	AD713C Typ	AD713C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**2.0**		0.25	**0.5**		0 1	**0.25**	mV
T_{min} to T_{max}			3.5/3.5/**3.5**			**1.5**			**0.75**	mV
vs. Temp		16	30/30/**30**		12	20		5	10	µV/°C
vs Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**86**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		40	**150**		40	**150**		40	**100**	pA
Either Input at T_{max},										
V_{CM} = 0 (70°C/85°C/125°C)			3 4/9 6/154			3.4/9.6/**154**			6.4	nA
Either Input, V_{CM} = +10V		50	200		50	**200**		50	**150**	pA
Offset Current, V_{CM} = 0		10	35		5	**35**		5	**15**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)			0.8/2 2/36			0 8/2 2/36			1 0	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage			1			1/0 7/0.7			0 3	mV
Input Offset Voltage T_{min} to T_{max}			2			2/1 5/1.5			0 6	mV
Input Offset Voltage vs Temp			40			25			15	µV/°C
Input Bias Current			25			25			10	pA
Crosstalk @ 1kHz		120			120			120		dB
@ 100kHz		90			90			90		dB
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.4	4		3.4	4		3 4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%		1	1.2		1	1 2		1	1.2	µs
Total Harmonic Distortion										
f = 1kHz, $R_L \geq 2k\Omega$, V_O = 3V rms		0 0003			0 0003			0 0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω ‖ pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω ‖ pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common-Mode Voltage		+14 5, −11 5			+14.5, −11.5			+14 5, −11 5		V
Over Max Operating Range[5]	**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	**78**	88		**82**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		80	84		**86**	90		dB
V_{CM} = ±11V	**72**	84		**78**	84		**80**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4**	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0 01			0 01			0.01		pA/√Hz
OPEN LOOP GAIN[6]										
V_O = ±10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
T_{min} to T_{max}, $R_L \geq 2k\Omega$	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13 3		**+13, −12.5**	+13.9, −13 3		**+13, −12.5**	+13.9, −13 3		V
T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13 1		**±12**	+13.8, −13 1		**±12**	+13 8, −13 1		V
Short-Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		10 0	**13.5**		10.0	**12.0**		10 0	**11.2**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD713J			AD713K					
Industrial (−40°C to +85°C)		AD713A			AD713B			AD713C		
Military (−55°C to +125°C)		AD713S			AD713T					
PACKAGE OPTIONS[7]										
Plastic (N-14)		AD713JN			AD713KN					
Cerdip (Q-14)		AD713AQ, AD713SQ			AD713BQ, AD713TQ			AD713CQ		

PRELIMINARY TECHNICAL DATA

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C
For higher temperature, the current doubles every 10°C
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground
[5]Typically exceeding −14 1V negative common-mode voltage on either input results in an output phase reversal
[6]Open loop gain is specified with V_{OS} nulled and unnulled.
[7]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ANALOG DEVICES

Low Cost High Accuracy IC Op Amps

AD741 SERIES

2

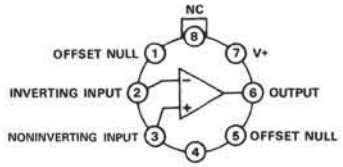
FEATURES

Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

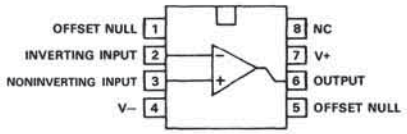
AD741 SERIES FUNCTIONAL DIAGRAMS

TO-99



NOTE PIN 4 CONNECTED TO CASE
TOP VIEW

8-Pin Mini-DIP



TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD741 series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection. For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of -55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from -55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

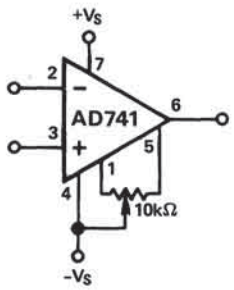
Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	20,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	15,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max							±10	±13		V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq$ 10V p-p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10kΩ, Adj. to Zero		1.0	6.0		1.0	5.0		1.0	3.0	mV
T_A = min to max		1.0	7.5		1.0	6.0			4.0	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	200		20	200		5	50	nA
T_A = min to max		40	300		85	500			100	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	500		80	500		40	200	nA
T_A = min to max		120	800		300	1,500			400	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common Mode, max Safe	±12	±13		±12	±13			±15		V
Common Mode Rejection,										
$R_S \leq$ 10kΩ, T_A = min to max,										
V_{IN} = ±12V	70	90		70	90		80	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	150		30	150				μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.2	3.3	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	−55		+125	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C

NOTES

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Nulling Offset Circuit

Model	AD741K Min	AD741K Typ	AD741K Max	AD741L Min	AD741L Typ	AD741L Max	AD741S Min	AD741S Typ	AD741S Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	50,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	25,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max										V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13		±10	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Respone (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq 10k\Omega$, Adj. to Zero		0.5	2.0		0.2	0.5		1.0	2	mV
T_A = min to max			3.0			1.0			4	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	10		2	5		2	10	nA
T_A = min to max			15			10			25	nA
Average vs. Temperature		0.02	0.2		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	75		30	50		30	75	nA
T_A = min to max			120			100			250	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common Mode max Safe		±15			±15			±15		V
Common Mode Rejection, $R_S \leq 10k\Omega$, T_A = min to max V_{IN} = ±12V	90	100		90	100		90	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio										μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.0	2.8	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								75	115	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTES
[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Temperature Range	Package Options*	Initial Off-Set Voltage
AD741CN	0 to +70°C	Mini-DIP (N-8)	6.0mV
AD741CH	0 to +70°C	TO-99 (H-08A)	6.0mV
AD741JN	0 to +70°C	Mini-DIP (N-8)	3.0mV
AD741JH	0 to +70°C	TO-99 (H-08A)	3.0mV
AD741KN	0 to +70°C	Mini-DIP (N-8)	2.0mV
AD741KH	0 to +70°C	TO-99 (H-08A)	2.0mV
AD741LN	0 to +70°C	Mini-DIP (N-8)	0.5mV
AD741LH	0 to +70°C	TO-99 (H-08A)	0.5mV
AD741H	-55°C to +125°C	TO-99 (H-08A)	5.0mV
AD741SH	-55°C to +125°C	TO-99 (H-08A)	2.0mV

*See Section 16 for package outline information.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22V	±18V
Internal Power Dissipation	500mW[1]	500mW
Differential Input Voltage	±30V	±30V
Input Voltage	±15V	±15V
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (soldering, 60 seconds)	300°C	300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES
[1] Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5mW/°C for ambient temperatures above +70°C.
[2] Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

Typical Performance Curves

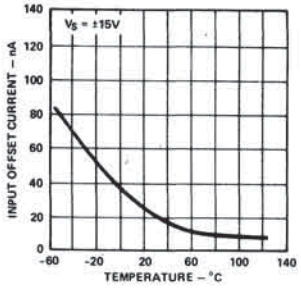


Figure 1. Offset Current vs. Temperature

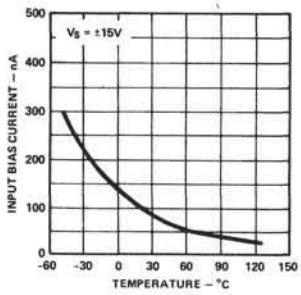


Figure 2. Bias Current vs. Temperature

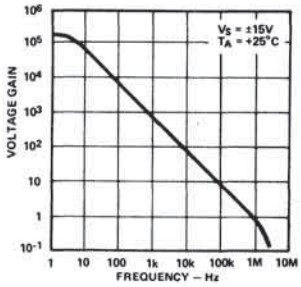


Figure 3. Open Loop Gain vs. Frequency

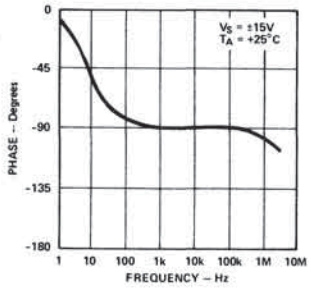


Figure 4. Open Loop Phase Response vs. Frequency

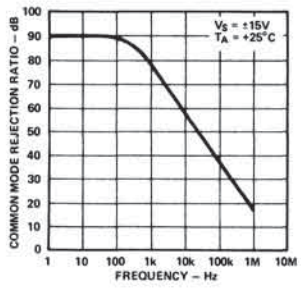


Figure 5. Common Mode Rejection vs. Frequency

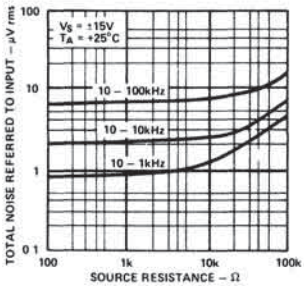


Figure 6. Broad Band Noise vs. Source Resistance

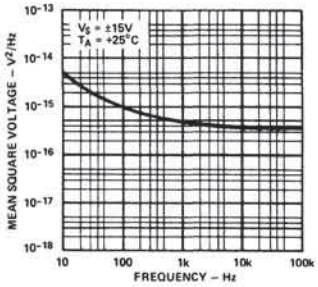


Figure 7. Input Noise Voltage vs. Frequency

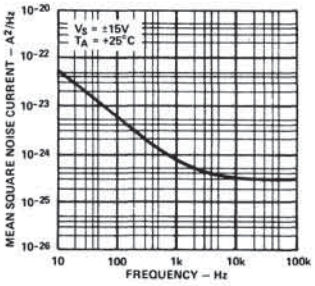


Figure 8. Input Noise Current vs. Frequency

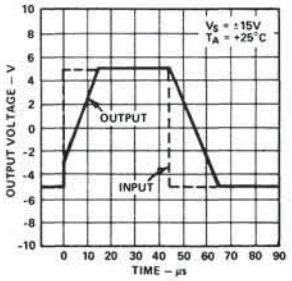


Figure 9. Voltage Follower Large Signal Pulse Response

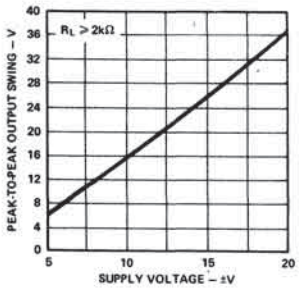


Figure 10. Output Voltage Swing vs. Supply Voltage

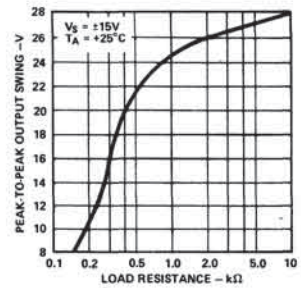


Figure 11. Output Voltage Swing vs. Load Resistance

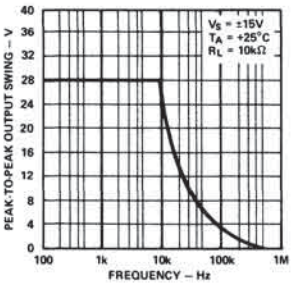


Figure 12. Output Voltage Swing vs. Frequency

Precision, 500ns Settling BiFET Op Amp

AD744

FEATURES

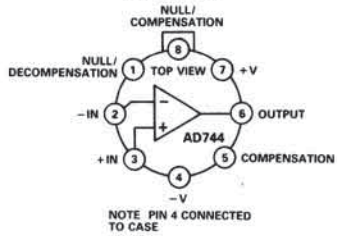
AC PERFORMANCE
- 500ns Settling to 0.01% for 10V Step
- 1.5μs Settling to 0.0025% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth – Internal Compensation
- >200MHz Gain Bandwidth (G = 1000) – External Decompensation
- >1000pF Capacitive Load Drive Capability with 10V/μs Slew Rate – External Compensation

DC PERFORMANCE
- 0.25mV max Offset Voltage (AD744C)
- 3μV/°C max Drift (AD744C)
- 250V/mV min Open-Loop Gain (AD744B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD744C)
- Available in Plastic Mini-DIP, Hermetic Cerdip and Hermetic Metal Can Packages
- MIL-STD-883B Processing Available

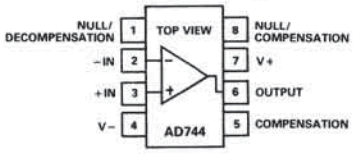
APPLICATIONS
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

AD744 CONNECTION DIAGRAMS

TO-99
(H) Package



Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500ns to 0.01%. This feature combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000pF capacitive loads, slewing at 10V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0 to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of −40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin cerdip, or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OP42, OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD744C).

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	AD744C Min	AD744C Typ	AD744C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0 3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	$T_{min}-T_{max}$			2/2/2			**1.0**			**0.45**	mV
vs. Temp			5	20/20/**20**		5	**10**		2	**3**	µV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs. Supply	$T_{min}-T_{max}$	82/82/**82**			**88**			**92**			dB
Long-Term Stability			15			15			15		µV/month
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM}=0V$		30	**100**		30	**100**		30	**50**	pA
Either Input @ T_{max}	$V_{CM}=0V$										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1 9	6.4		1 9	6.4		1.9	3 2	nA
S, T	125°C		31	102		31	102				nA
Either Input	$V_{CM}=+10V$		40	150		40	**150**		40	**100**	pA
Offset Current	$V_{CM}=0V$		20	**50**		10	**50**		10	**20**	pA
Offset Current @ T_{max}	$V_{CM}=0V$										
J, K	70°C		0 4	1.1		0 2	1.1				nA
A, B, C	85°C		1.3	3 2		0 6	3.2		0.6	1 3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G=-1$	**8**	13		**9**	13		**9**	13		MHz
Full Power Response	$V_O=20V$ p-p		600			600			600		kHz
Slew Rate, Unity Gain	$G=-1$	**45**	75		**50**	75		**50**	75		V/µs
Settling Time to 0 01%[4]	$G=-1$		0 5	0 9		0 5	0.9		0.5	0 9	µs
Total Harmonic	f = 1kHz										
Distortion	R1 ≥ 2kΩ										
	$V_O=3V$ rms		0 0003			0.0003			0 0003		%
INPUT IMPEDANCE											
Differential			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5\ 5$		Ω|pF
Common Mode			$3\times10^{12}\|5\ 5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω|pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14 5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio	$V_{CM}=\pm10V$	**78**	88		**82**	88		**86**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
	$V_{CM}=\pm11V$	**72**	84		**78**	84		**80**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		2			2			2	**4**	µV p-p
	f = 10Hz		45			45			45		nV/√Hz
	f = 100Hz		22			22			22		nV/√Hz
	f = 1kHz		18			18			18		nV/√Hz
	f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1kHz		0 01			0 01			0 01		pA/√Hz
OPEN LOOP GAIN[7]	$V_O=\pm10V$										
	$R_{LOAD}\geq2k\Omega$	**200**	400		**250**	400		**250**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq2k\Omega$	**+13, −12.5**	+13.9, −13 3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13 9, −13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13 8, −13.1		**±12**	+13.8, −13 1		**±12**	+13 8, −13.1		V
Current	Short-Circuit		25			25			25		mA
Capacitive Load[8]	Gain = −1			**1000**			**1000**			**1000**	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			3.5	5.0		3 5	4.0		3 5	4.0	mA
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD744J			AD744K					
Industrial (−40°C to +85°C)			AD744A			AD744B			AD744C		
Military (−55°C to +125°C)			AD744S			AD744T					
PACKAGE OPTIONS[9]											
8-Pin Plastic Mini-DIP (N-8)			AD744JN			AD744KN					
8-Pin Cerdip (Q-8)			AD744AQ, AD744SQ			AD744BQ, AD744TQ			AD744CQ		
TO-99 Metal Can (H-08A)			AD744AH, AD744SH			AD744BH, AD744TH			AD744CH		

NOTES

[1] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A=+25°C$

[2] PSRR test conditions: $+V_S=15V$, $-V_S=12V$ to 18V and $+V_S=12V$ to 18V, $-V_S=-15V$

[3] Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A=+25°C$. For higher temperature, the current doubles every 10°C.

[4] Gain = −1, $R_L=2k$, $C_L=10pF$, refer to Figure 25.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground

[6] Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

[7] Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8] Capacitive load drive specified for $C_{COMP}=20pF$ with the device connected as shown in Figure 32. Under these conditions, slew rate = 14V/µs and 0 01% settling time = 1.5µs typical. Refer to Table II for optimum compensation while driving a capacitive load

[9] See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD744J/K	0 to +70°C
AD744A/B/C	−40°C to +85°C
AD744S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Typical Characteristics

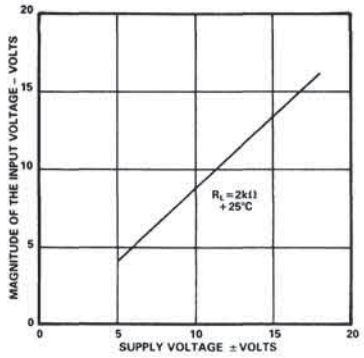


Figure 1. Input Voltage Swing vs. Supply Voltage

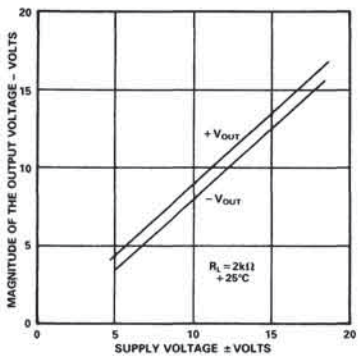


Figure 2. Output Voltage Swing vs. Supply Voltage

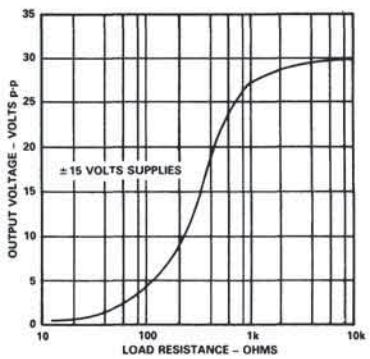


Figure 3. Output Voltage Swing vs. Resistive Load

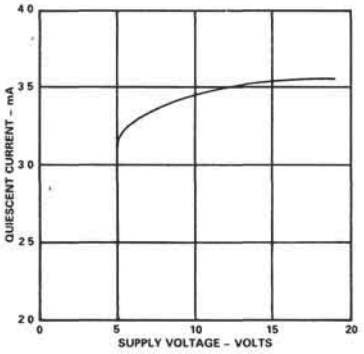


Figure 4. Quiescent Current vs. Supply Voltage

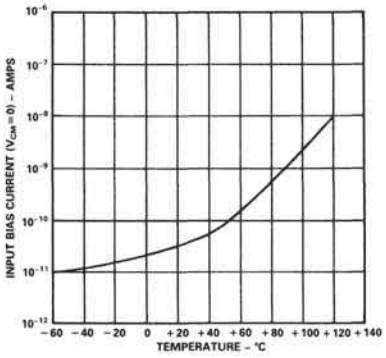


Figure 5. Input Bias Current vs. Temperature

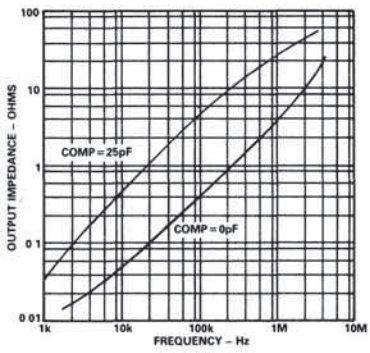


Figure 6. Magnitude of Output Impedance vs. Frequency

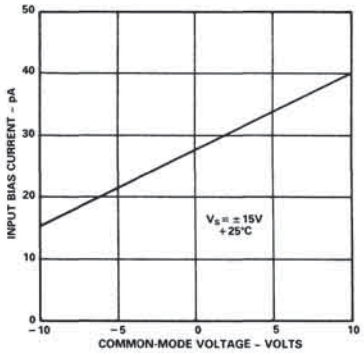


Figure 7. Input Bias Current vs. Common-Mode Voltage

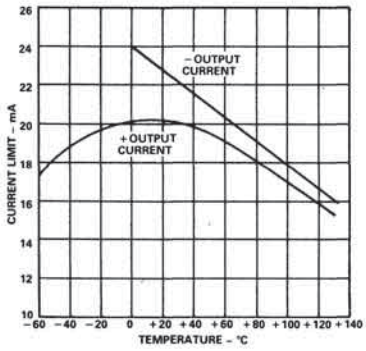


Figure 8. Short Circuit Current Limit vs. Temperature

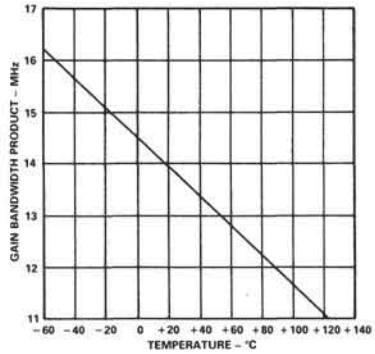


Figure 9. Gain Bandwidth Product vs. Temperature

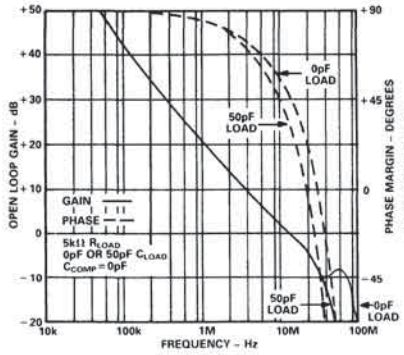


Figure 10. Open Loop Gain and Phase vs. Frequency C_{COMP} = 0pF

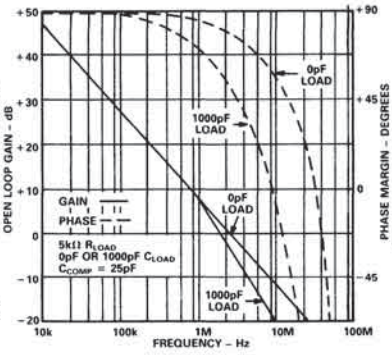


Figure 11. Open Loop Gain and Phase vs. Frequency C_{COMP} = 25pF

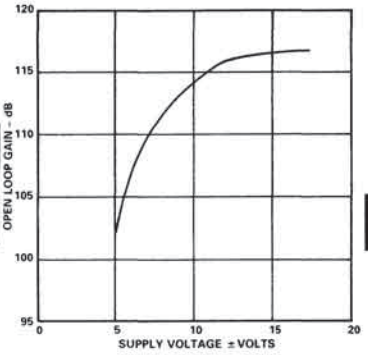


Figure 12. Open Loop Gain vs. Supply Voltage

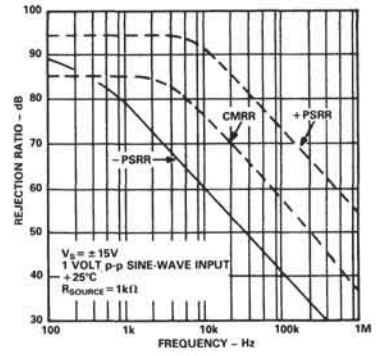


Figure 13. Common-Mode and Power Supply Rejection vs. Frequency

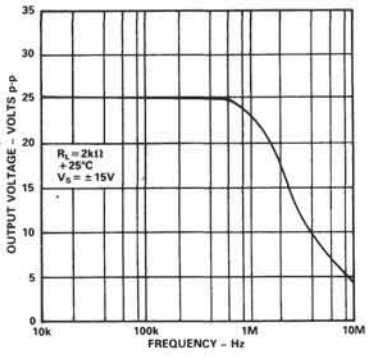


Figure 14. Large Signal Frequency Response

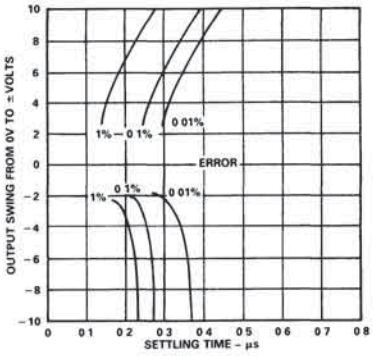


Figure 15. Output Swing and Error vs. Settling Time

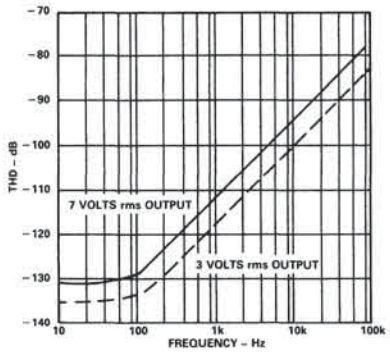


Figure 16. Total Harmonic Distortion vs. Frequency, Circuit of Figure 20 (G = 10)

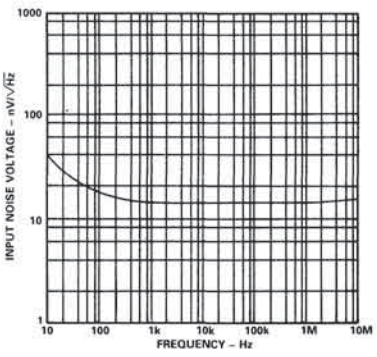


Figure 17. Input Noise Voltage Spectral Density

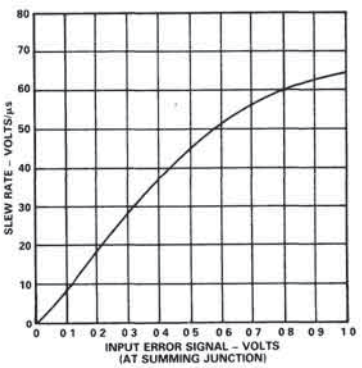


Figure 18. Slew Rate vs. Input Error Signal

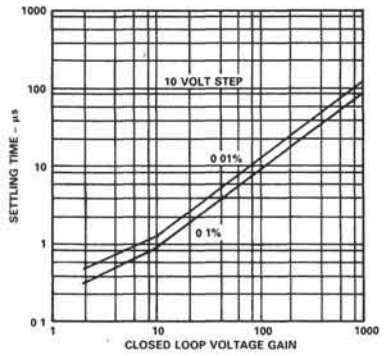


Figure 19. Settling Time vs. Closed Loop Voltage Gain

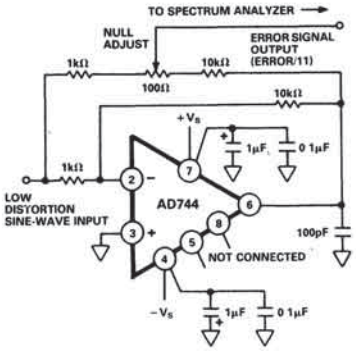


Figure 20. THD Test Circuit

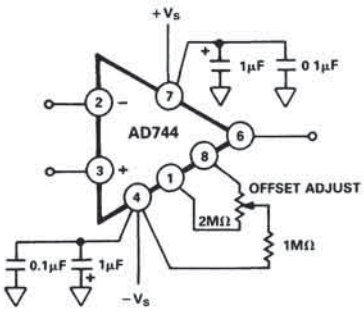


Figure 21. Offset Null Configuration

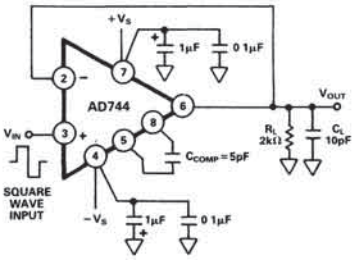


Figure 22a. Unity Gain Follower

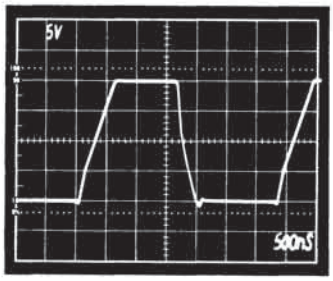


Figure 22b. Unity Gain Follower Large Signal Pulse Response, C_{COMP} = 5pF

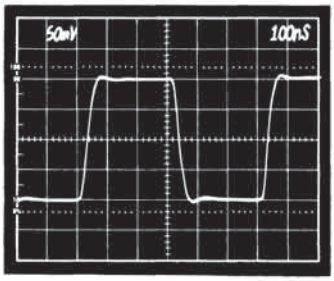


Figure 22c. Unity Gain Follower Small Signal Pulse Response, C_{COMP} = 5pF

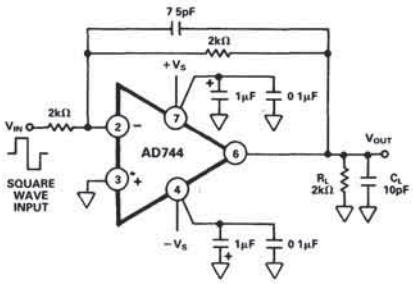


Figure 23a. Unity Gain Inverter

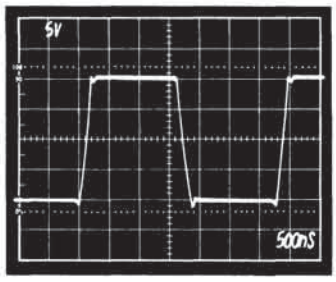


Figure 23b. Unity Gain Inverter Large Signal Pulse Response, C_{COMP} = 0pF

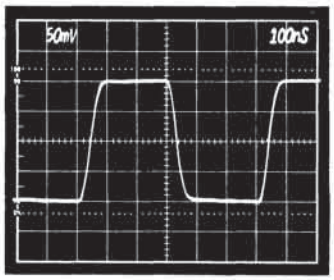


Figure 23c. Unity Gain Inverter Small Signal Pulse Response, C_{COMP} = 0pF

POWER SUPPLY BYPASSING

The power supply connections to the AD744 must maintain a low impedance to ground over a bandwidth of 10MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 24 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

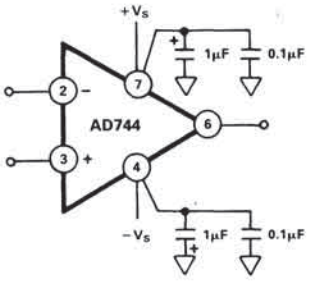


Figure 24. Recommended Power Supply Bypassing

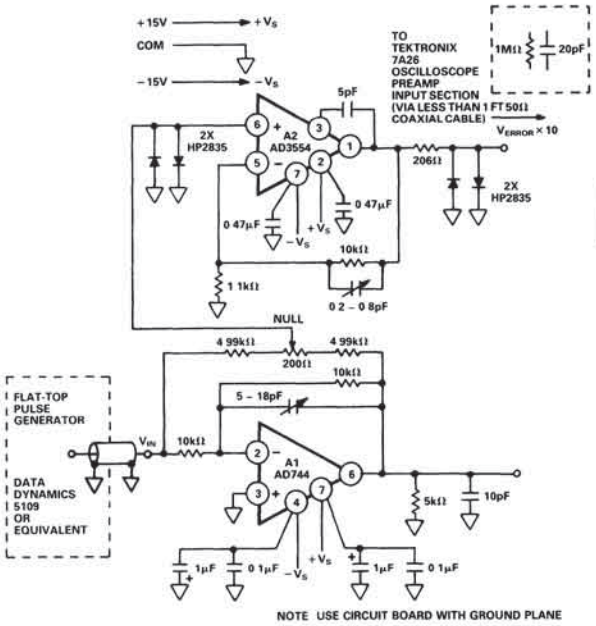


Figure 25. Settling Time Test Circuit

MEASURING AD744 SETTLING TIME

The photos of Figures 26 and 27 show the dynamic response of the AD744 while operating in the settling time test circuit of Figure 25. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD744 under test, is clamped, amplified by op amp A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4V overload quickly enough to allow accurate measurement of the AD744's 500ns settling time. Amplifier A2 is a very high-speed FET-input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD744 under test.

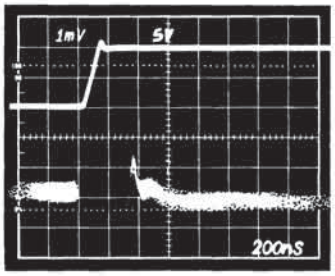


Figure 26. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD744 Under Test (5V/div)
Lower Trace: Amplified Error Voltage (0.01%/div)

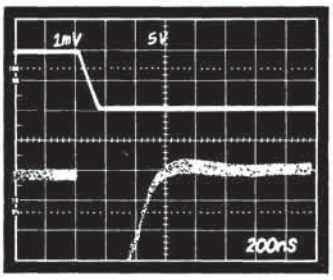


Figure 27. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD744 Under Test (5V/div)
Lower Trace: Amplified Error Voltage (0.01%/div)

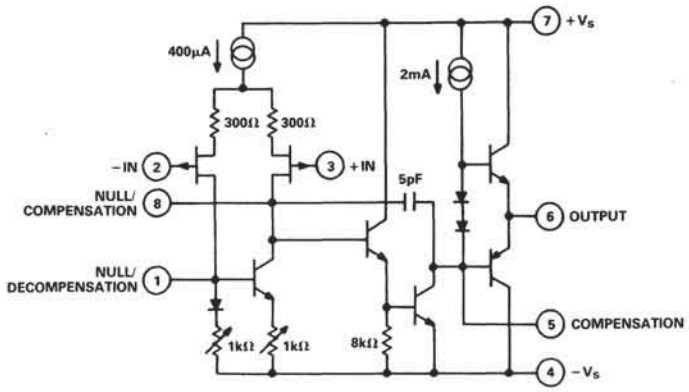


Figure 28. AD744 Simplified Schematic

EXTERNAL FREQUENCY COMPENSATION

Even though the AD744 is useable without compensation in most applications, it may be externally compensated for even more flexibility. This is accomplished by connecting a capacitor between Pins 5 and 8. Figure 28, a simplified schematic of the AD744, shows where this capacitor is connected. This feature is useful because it allows the AD744 to be used as a unity gain voltage follower. It also enables the amplifier to drive capacitive loads up to 2000pF and greater.

The slew rate and gain bandwidth product of the AD744 are inversely proportional to the value of the compensation capacitor, C_{COMP}. Therefore, when trying to maximize the speed of the amplifier, the value of C_{COMP} should be minimized. C_{COMP} can also be used to slow the amplifier to a point where the slew rate is perfectly symmetrical and well controlled. Figure 29 summarizes the effect of external compensation on slew rate and bandwidth.

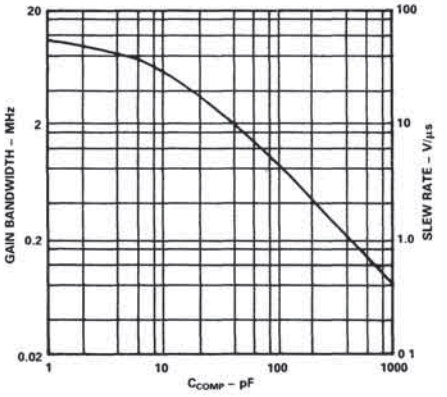


Figure 29. Gain Bandwidth and Slew Rate vs. C_{COMP}

The following section provides tables to show what C_{COMP} values will provide the necessary compensation for given circuit configurations and capacitive loads. In each case, the recommended C_{COMP} is a minimum value. A larger C_{COMP} can always be used, but slew rate and bandwidth performance will be degraded.

Figure 30 shows the AD744 configured as a unity gain voltage follower. In this case, a minimum compensation capacitor of 5pF is necessary for stable operation. Larger compensation capacitors can be used for driving larger capacitive loads. Table I outlines recommended minimum values for C_{COMP} based on the desired capacitive load. It also gives the slew rate and bandwidth that will be achieved for each case.

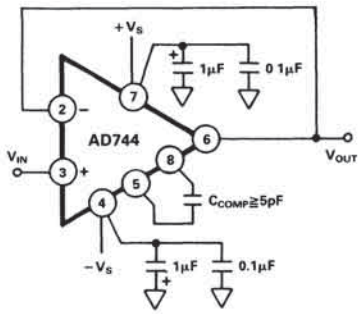


Figure 30. AD744 Connected as a Unity Gain Voltage Follower

Gain	Max C_{LOAD} (pF)	C_{COMP} (pF)	Slew Rate (V/µs)	–3dB Bandwidth (MHz)
1	50	5	37	6.5
1	150	10	25	4.3
1	2000	25	12.5	2.0

Table I. Recommended Values of C_{COMP} vs. Various Capacitive Loads

Figures 31 and 32 show the AD744 as a voltage follower with gain and as an inverting amplifier. In these cases, external compensation is not necessary for stable operation. However, compensation may be applied to drive capacitive loads above 50pF. Table II gives recommended C_{COMP} values, along with expected slew rates and bandwidths for a variety of load conditions and gains for the circuits in Figures 31 and 32.

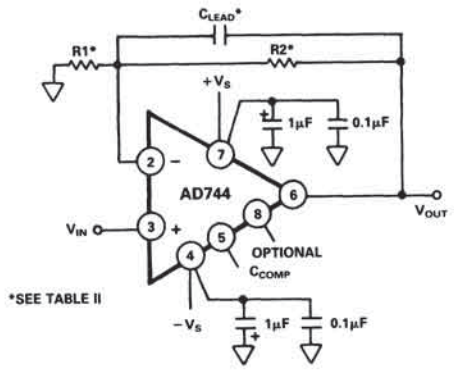


Figure 31. AD744 Connected as a Voltage Follower Operating at Gains of 2 or Greater

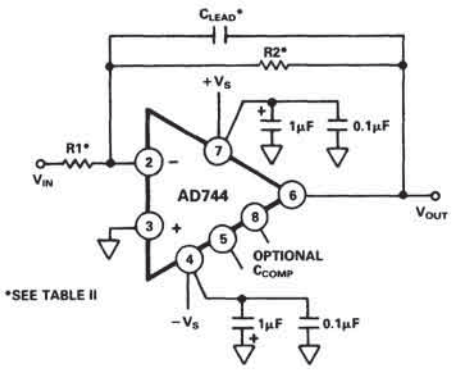


Figure 32. AD744 Connected as an Inverting Amplifier Operating at Gains of 1 or Greater

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	Max C_{LOAD} (pF)	C_{COMP} (pF)	C_{LEAD} (pF)	Slew Rate (V/μs)	−3dB Bandwidth (MHz)
4.99k	4.99k	2	1	50	0	7	75	2.5**
4.99k	4.99k	2	1	150	5	7	37	2.3**
4.99k	4.99k	2	1	1000	20	–	14	1.2
4.99k	4.99k	2	1	>2000	25	–	12.5*	1.0
499Ω	4.99k	11	10	270	0	–	75	1.2
499Ω	4.99k	11	10	390	2	–	50	0.85
499Ω	4.99k	11	10	1000	5	–	37*	0.60

*Into large capacitive loads the AD744's 25mA output current limit sets the slew rate of the amplifier, in V/μs, equal to 0.025 amps divided by the value of C_{LOAD} in μF. Slew rate is specified into rated max C_{LOAD} except for cases marked *, which are specified with a 50pF load.
**Bandwidth with C_{LEAD} adjusted for minimum settling time.

Table II. Recommended Values of C_{COMP} vs. Various Load Conditions for the Circuits of Figures 31 and 32.

Using Decompensation to Extend the Gain Bandwidth Product

When the AD744 is used in applications where the closed-loop gain is greater than 10, gain bandwidth product may be enhanced by connecting a small capacitor between Pins 1 and 5 (Figure 33). At low frequencies, this capacitor cancels the effects of the chip's internal compensation capacitor, C_{COMP}, effectively decompensating the amplifier.

Due to manufacturing variations in the value of the internal C_{COMP}, it is recommended that the amplifier's response be optimized for the desired gain by using a 2 to 10pF trimmer capacitor rather than using a fixed value.

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	−3dB Bandwidth	Gain/BW Product
1k	10k	11	10	2.5MHz	25MHz
100	10k	101	100	760kHz	76MHz
100	100k	1001	1000	225kHz	225MHz

Table III. Performance Summary for the Circuit of Figure 33

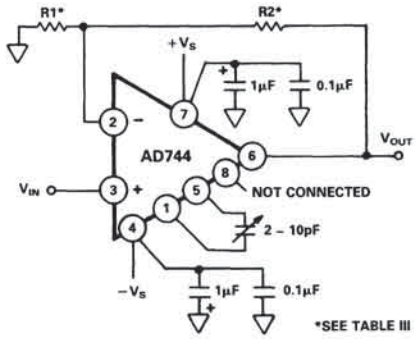


Figure 33. Using the Decompensation Connection to Extend Gain Bandwidth

HIGH-SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

Digital-to-analog converters which use bipolar transistors to switch currents into (or out of) their outputs can achieve very fast settling times. The AD565A, for example, is specified to settle to 12 bits in less than 250ns, with a current output. However, in many applications, a voltage output is desirable, and it would be useful – perhaps essential – that this I-to-V conversion be accomplished without increasing the settling time or without degrading the accuracy of the DAC.

Figure 34 is a schematic of an AD565A DAC using an AD744 output buffer. The 10pF C_{LEAD} capacitor compensates for the DAC's output capacitance, plus the 5.5pF amplifier input capacitance.

Figure 35 is an oscilloscope photo of the AD744's output voltage with a +10V to 0V step applied; this corresponds to an all "1s" to all "0s" code change on the DAC. Since the DAC is connected in the 20V span mode, 1LSB is equal to 4.88mV. Output settling time for the AD565/AD744 combination is less than 500ns to within a 2.44mV, 1/2LSB error band.

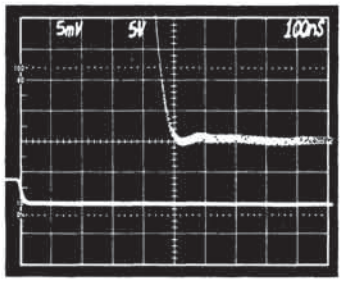


Figure 35. Upper Trace: AD744 Output Voltage for a +10V to 0V Step, Scale: 5mV/division. Lower Trace: Logic Input Signal, Scale: 5V/division.

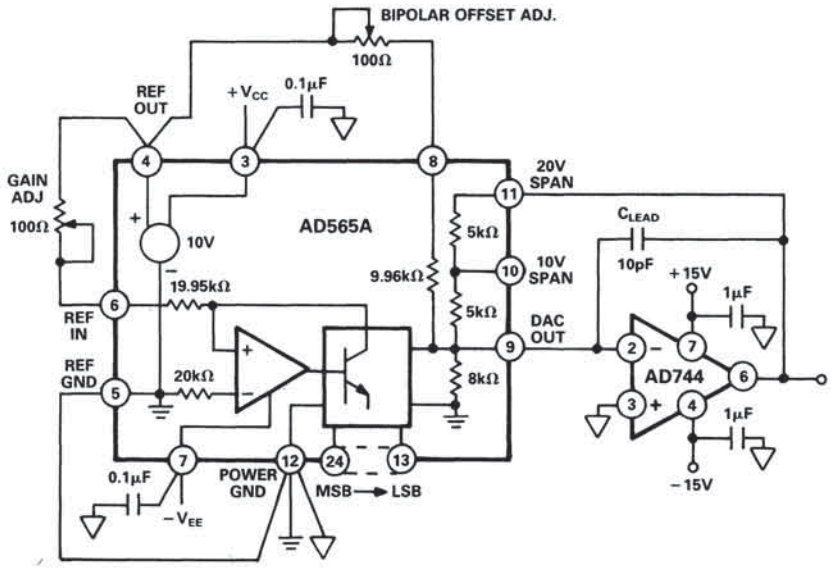


Figure 34. ±10V Voltage Output Bipolar DAC Using the AD744 as an Output Buffer

A HIGH-SPEED, 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 36 can provide a range of gains from unity up to 1000 and higher. The circuit bandwidth is 4MHz at a gain of 1 and 750kHz at a gain of 10; settling time for the entire circuit is less than 2μs to within 0.01% for a 10V step, (G = 10).

While the AD744 is not stable with 100% negative feedback (as when connected as a standard voltage follower), phase margin and therefore stability at unity gain may be increased to an acceptable level by placing the parallel combination of a resistor and a small lead capacitor between each amplifier's output and its inverting input terminal.

The only penalty associated with this method is a small bandwidth reduction at low gains. The optimum value for C_{LEAD} may be determined from the graph of Figure 41. This technique can be used in the circuit of Figure 36 to achieve stable operation at gains from unity to over 1000.

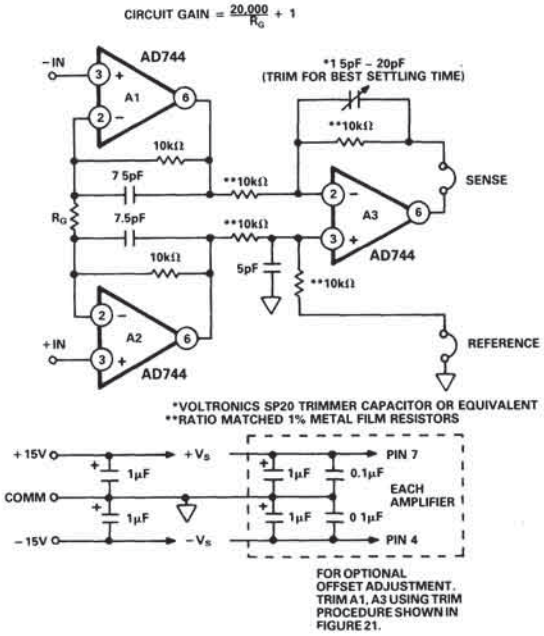


Figure 36. A High Performance, 3 Op Amp Instrumentation Amplifier Circuit

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	3.5MHz	1.5μs
2	20kΩ	2.5MHz	1.0μs
10	2.02kΩ	1MHz	2μs
100	202Ω	290kHz	5μs

Table IV. Performance Summary for the Three Op Amp Instrumentation Amplifier Circuit

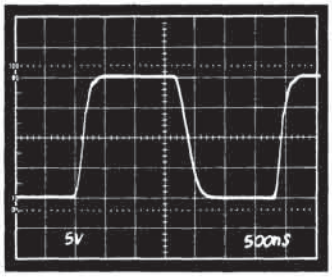


Figure 37. The Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5μs/div, Vertical Scale: 5V/div. (Gain = 10)

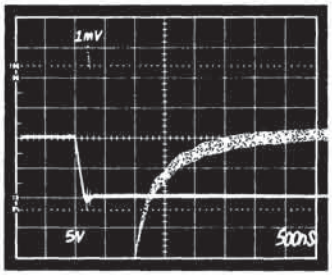


Figure 38. Settling Time of the 3 Op Amp Instrumentation Amplifier. Horizontal Scale: 500ns/div., Vertical Scale, Pulse Input: 5V/div. Output Settling: 1mV/div.

Minimizing Settling Time in Real-World Applications

An amplifier with a "single pole" or "ideal" integrator open-loop frequency response will achieve the minimum possible settling time for any given unity-gain bandwidth. However, when this "ideal" amplifier is used in a practical circuit, the actual settling time is increased above the minimum value because of added time constants which are introduced due to additional capacitance on the amplifier's summing junction. The following discussion will explain how to minimize this increase in settling time by the selection of the proper value for feedback capacitor, C_L.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency, f_O, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 39. This circuit models an op amp connected as an I-to-V converter.

Equation 1 would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects. Even considering these effects, the fine scale settling to <0.1% will be determined by the op amp's small signal behavior.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R\,(C_L + C_X)}{2\pi F_O}\,s^2 + \left(\frac{G_N}{2\pi F_O} + R\,C_L\right)s + 1}$$

Where F_O = the op amp's unity gain crossover frequency

G_N = the "noise" gain of the circuit $\left(1 + \frac{R}{R_O}\right)$

This Equation May Then Be Solved for C_L:

Equation 2.

$$C_L = \frac{2 - G_N}{R\,2\pi F_O} + \frac{2\sqrt{RC_X\,2\pi F_O + (1 - G_N)}}{R\,2\pi F_O}$$

In these equations, capacitance C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling an I-to-V converter application, the Norton equivalent circuit of Figure 39 can be used directly. Capacitance C_X is the total capacitance of the output of the current source plus the input capacitance of the op amp, which includes any stray capacitance at the op amp's input.

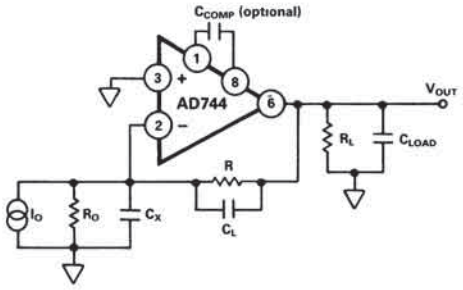


Figure 39. A Simplified Model of the AD744 Used as a Current-to-Voltage Converter

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier model of Figure 40 is created. Here capacitor C_X represents the input capacitance of the AD744 (5.5pF) plus any stray capacitance due to wiring and the type of IC package employed.

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp's output. If the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose the correct value for a small capacitor, C_L, which will optimize amplifier response. If the value of C_X is not known, C_L should be a variable capacitor.

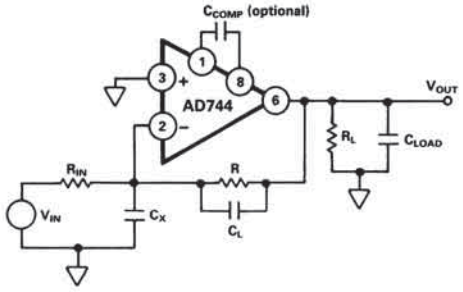


Figure 40. A Simplified Model of the AD744 Used as an Inverting Amplifier

As an aid to the designer, the optimum value of C_L for one specific amplifier connection can be determined from the graph of Figure 41. This graph has been produced for the case where the AD744 is connected as in Figures 39 and 40 with a practical minimum value for C_{STRAY} of 2pF and a total C_X value of 7.5pF.

The approximate value of C_L can be determined for almost any application by solving Equation 2. For example, the AD565/AD744 circuit of Figure 34 constrains all the variables of Equation 2 ($G_N = 3.25$, $R = 10k\Omega$, $F_O = 13MHz$, and $C_X = 32.5pF$). Therefore, under these conditions, $C_L = 10.5pF$.

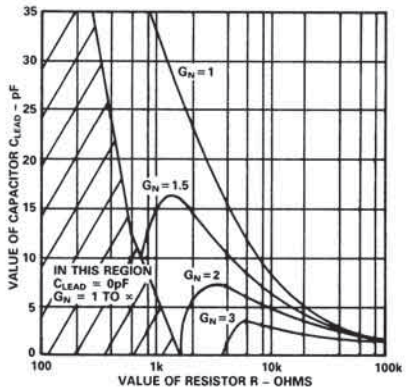


Figure 41. Practical Values of C_L vs. Resistance of R for Various Amplifier Noise Gains

Dual Precision, 500ns Settling BiFET Op Amp

AD746

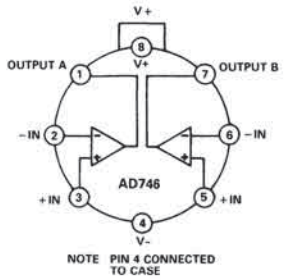
FEATURES

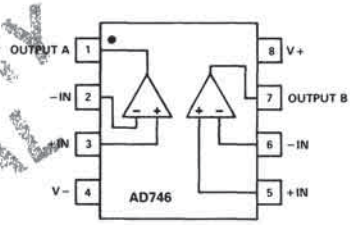
AC PERFORMANCE
- 500ns Settling to 0.01% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth

DC PERFORMANCE
- 0.25mV max Offset Voltage (AD746C)
- 3μV/°C max Drift (AD746C)
- 250V/mV min Open Loop Gain (AD746B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD746C)

APPLICATIONS
- Output Buffers for 12- and 14- Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters
- Available in 8-Pin Plastic SOIC, Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages.

AD746 CONNECTION DIAGRAMS





PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD746 is a dual fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD746 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater.

The single pole response of the AD746 provides fast settling: 500ns to 0.01%. This feature combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD746's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD746 is available in seven performance grades. The AD746J and AD746K are rated over the commercial temperature range of 0 to +70°C. The AD746A, AD746B and AD746C are rated over the industrial temperature range of −40°C to 85°C. The AD746S and AD746T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature range. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

PRODUCT HIGHLIGHTS

1. The AD746 is a dual high-speed, fast settling, BiFET op amp that offers excellent performance at competitive prices. The AD746 is offered in a standard dual pin out.
2. The AD746 offers excellent dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD746B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD746 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD746C).
5. The AD746 is available in an 8-pin small outline (SO) package, mini-DIP, cerdip and metal cans.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD746J/A/S Min	AD746J/A/S Typ	AD746J/A/S Max	AD746K/B/T Min	AD746K/B/T Typ	AD746K/B/T Max	AD746C Min	AD746C Typ	AD746C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0 3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	$T_{min}-T_{max}$			2.5/2.5/2.5			**1**			**0.50**	mV
vs. Temperature			12	20/20/**20**		5	**10**		2	**3**	µV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs Supply	$T_{min}-T_{max}$	82/82/**82**			**88**			**92**			dB
Long-Term Stability			15			15			15		µV/month
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM}=0V$		60	**150**		60	**150**		60	**150**	pA
Either Input @ T_{max}	$V_{CM}=0V$										
J, K	70°C		1.4	3.4		1.4	3.4				nA
A, B, C	85°C		3.8	9.6		3 8	9 6		3 8	6.4	nA
S, T	125°C		61	154		61	154				nA
Either Input	$V_{CM}=+10V$		80	250		80	**250**		80	**200**	pA
Offset Current	$V_{CM}=0V$		30	75		20	75		20	**40**	pA
Offset Current @ T_{max}	$V_{CM}=0V$										
J, K	70°C		0 7	1 7		0.4	1.7				nA
A, B, C	85°C		1.9	4 8		1.3	4 8		1.3	2.6	nA
S, T	125°C		31	77		20	77				nA
MATCHING CHARACTERISTICS[4]											
Input Offset Voltage				**1.5**			**0.5**			**0.3**	mV
Input Offset Voltage	T_{min} to T_{max}			2.5/2.5/2.5			**1.0**			**0.6**	mV
Input Offset Voltage	vs. Temp.			20/20/**20**			**10**			**5**	µV/°C
Input Bias Current				**50**			**50**			**20**	pA
Crosstalk @ 1kHz			120			120			120		dB
@ 100kHz			90			90			90		dB
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G=-1$	8	13		9	13		9	13		MHz
Full Power Response	$V_O=20V$ p-p		600			600			600		kHz
Slew Rate, Unity Gain	$G=-1$	**45**	75		**50**	75		**50**	75		V/µs
Settling Time to 0 01%[4]	$G=-1$		0.5	0.9		0.5	0.9		0.5	0.9	µs
Total Harmonic	f = 1kHz										
Distortion	R1≥2kΩ										
	$V_O=3V$ rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5 5		Ω‖pF
Common Mode			3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5 5		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11 5			+14.5, −11.5			+14.5, −11 5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio	$V_{CM}=\pm10V$	**78**	88		**82**	88		**86**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
	$V_{CM}=\pm11V$	**72**	84		**78**	84		**80**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		2			2			2	**4**	µV p-p
	f = 10Hz		45			45			45		nV/√Hz
	f = 100Hz		22			22			22		nV/√Hz
	f = 1kHz		18			18			18		nV/√Hz
	f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1kHz		0 01			0.01			0 01		pA/√Hz
OPEN LOOP GAIN[7]	$V_O=\pm10V$										
	$R_{LOAD}\geq2k\Omega$	**150**	300		**175**	300		**200**	300		V/mV
	T_{min} to T_{max}	75/75/**65**			**75**			**100**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq2k\Omega$	**+13, −12.5**	+13 9, −13.3		**+13, −12.5**	+13.9, −13 3		**+13, −12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13 1		**±12**	+13 8, −13.1		**±12**	+13 8, −13.1		V
Current	Short-Circuit		25			25			25		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			7.0	**10.0**		7 0	**8.0**		7 0	**8.0**	mA
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD746J			AD746K					
Industrial (−40°C to +85°C)			AD746A			AD746B			AD746C		
Military (−55°C to +125°C)			AD746S			AD746T					
PACKAGE OPTIONS[8]											
SOIC (R-8)			AD746JR								
Plastic (N-8)			AD746JN			AD746KN					
Cerdip (Q-8)			AD746AQ, AD746SQ			AD746BQ, AD746TQ			AD746CQ		
TO-99 (H-08A)			AD746AH, AD746SH			AD746BH, AD746TH			AD746CH		

PRELIMINARY TECHNICAL DATA

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A=+25°C$.

[2]PSRR test conditions $+V_S=15V$, $-V_S=12V$ to 18V and $+V_S=12V$ to 18V, $-V_S=-15V$.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A=+25°C$. For higher temperature, the current doubles every 10°C

[4]Matching is defined as the difference between parameters of the two amplifiers.

[5]Defined as voltage between inputs, such that neither exceeds ± 10V from ground

[6]Typically exceeding −14 1V negative common-mode voltage on either input results in an output phase reversal

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]See Section 16 for package outline information

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

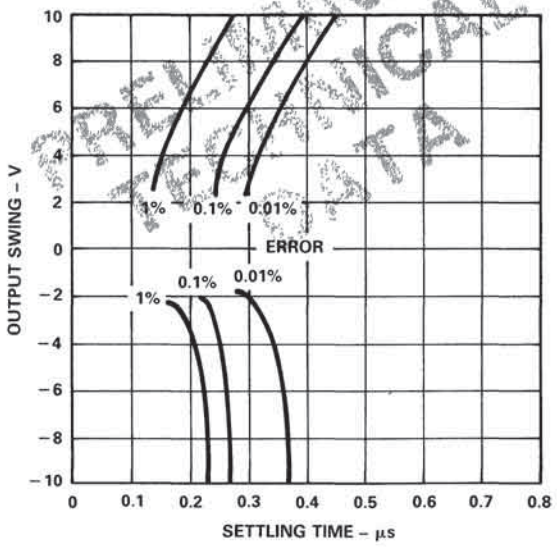
Supply Voltage	±18V
Internal Power Dissipation	500mW
Input Voltage[2]	±18V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD746J/K	0 to +70°C
AD746A/B/C	−40°C to +85°C
AD746S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

PRELIMINARY TECHNICAL DATA



Single Supply, Low Power Precision Op Amp

AD821

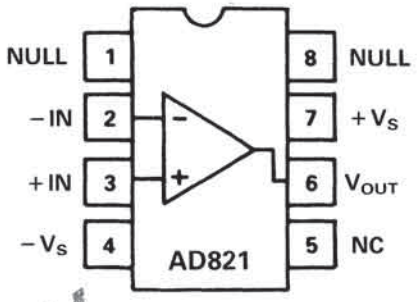
FEATURES

True Single Supply Operation:
Input and Output Voltage Ranges Include Ground
Output Voltage Swing to 50mV of Each Rail
Low Power: 400μA Supply Current max
250μV Input Offset Voltage
1.3MHz Gain Bandwidth Product
3V/μs Slew Rate
Single and Dual Supply Capability

APPLICATIONS

Battery Powered Precision Instrumentation
Strain Gage Signal Conditioners
Instrumentation Amplifiers
Thermocouple Amplifiers
Multiple Limit Threshold Detection
12- to 14-Bit Data Acqusition Systems
Available in 8-Pin Plastic Mini-DIP, SOIC and Hermetic Cerdip Packages
Dual Version – AD822, Quad Version – AD824 Also Available

AD821 FUNCTIONAL BLOCK DIAGRAM



8-Pin Plastic Mini-DIP SO and Cerdip

PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD821 is a precision, low power, FET input monolithic op amp that can operate from a single supply of +4.75V to +36V or dual supplies of ±2.4V to ±18V. It has true single supply capability with its input voltage range including the negative rail, allowing the AD821 to accommodate input signals down to ground in the single supply mode. Its output voltage swing extends to within 50mV of each rail providing the maximum possible output dynamic range to the user.

Low input offset voltage (250μV max), low offset voltage drift (3μV/°C max), low input bias current (<10pA) and low supply currents (400μA max) mark the AD821 with true dc precision at low power operating conditions. Combined with unity gain bandwidth of 1.3MHz and 3V/μs slew rate, the AD821 offers the best combination of ac and dc specs to the single supply op amp user. Performance in 12- to 14-bit applications is ensured with the AD821's low noise 26nV/$\sqrt{\text{Hz}}$), high open-loop gain (10^7V/mV) and 4μs settling to 0.01%.

The AD821 is an excellent choice for battery powered precision instrumentation applications – wherein the extended input and output ranges afford the AD821 its versatility in these applications.

The AD821 is available in five performance grades. The AD821J and AD821K are rated over the commercial temperature range of 0 to +70°C. The AD821A and AD821B are rated over the industrial temperature range of −40°C to +85°C. The AD821S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature range. PLUS screening includes a 168 hour burn-in, as well as other environmental and physical tests.

PRODUCT HIGHLIGHTS

1. True single supply operation – input voltage range includes the negative rail.
2. Output voltage range extends to 50mV of each rail.
3. Low power, low supply current.
4. Common-mode rejection of 90dB and open-loop gain of 10^7V/mV ensure 12- to 14-bit accuracy in high-speed data acquisition circuits.
5. Dual version – AD822, quad version – AD824 also available.

SPECIFICATIONS (@ +25°C unless otherwise noted)

Model	Conditions[1]	AD821J/A/S Min	AD821J/A/S Typ	AD821J/A/S Max	AD821B/K Min	AD821B/K Typ	AD821B/K Max	Units
INPUT CHARACTERISTICS								
Input Offset Voltage[2]	$V_{CM} = 0$							
	Condition 1, $V_O = 0V$		0.3	1*		0.1	0.25*	mV
	Condition 2, $V_O = 1.4V$		0.3	1*		0.1	0.25*	mV
	T_{min} to T_{max}			1.5/1.6/2*			0.4*	mV
Input Offset Voltage Drift				10*			3*	µV/°C
Input Bias Current[3]			15	30		10	20	pA
	T_{min} to T_{max}			0.68/2/30			0 5/1.3	nA
Input Offset Current			5	15		3	7	pA
	T_{min} to T_{max}			0.34/0.96/15			0.16/0.45	nA
Input Resistance	Differential		5×10			5×10		Ω
Input Capacitance			3			3		pF
Common-Mode Voltage Range	Condition 1	$-V_S$		$+V_S - 1$	$-V_S$		$+V_S - 1$	V
	Condition 2	$-V_S$		$+V_S - 1$	$-V_S$		$+V_S - 1$	V
Differential Voltge Range[4]	Condition 1	$-V_S - 0.6$		$+V_S + 0.6$	$-V_S - 0\ 6$		$+V_S + 0.6$	V
	Condition 2	$-V_S - 0.6$		$+V_S + 0.6$	$-V_S - 0\ 6$		$+V_S + 0.6$	V
Common-Mode Rejection	Condition 1 $V_{CM} = \pm 12V, V_O = 0V$	80*			90*			dB
	Condition 2 $V_{CM} = 0$ to 2.5V, $V_O = 1\ 4V$	80*			90*			dB
Power Supply Rejection Ratio	Condition 1	80*			90*			dB
	Condition 2 $4\ 5 < +V_S < 5.5, V_O = 1\ 4V$	80*			90*			dB
Input Noise Voltage	f = 10Hz		90			90		nV/√Hz
	f = 100Hz		90			90		nV/√Hz
	f = 1kHz		50			50		nV/√Hz
	f = 10kHz		33			33		nV/√Hz
	f = 100kHz		21			21		nV/√Hz
Input Noise Current	f = 1kHz		0.01			0.01		pA/√Hz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Condition 1, Condition 2							
	2kΩ Load		150mV max from Each Rail			150mV max from Each Rail		
	10kΩ Load		100mV max from Each Rail			100mV max from Each Rail		
	Condition 2							V
	1mA Sink		100mV max from Ground			100mV max from Ground		
Short-Circuit Current	Source or Sink		30			30		mA
GAIN								
Open Loop	Condition 1 $V_O = \pm 14V$							
	2kΩ Load	500	1,000		500	1,000		V/mV
	10kΩ Load	1,000	10,000		1,000	10,000		V/mV
	Condition 2 $V_O = 0.5V$ to 4.5V							
	2kΩ Load	500	1,000		500	1,000		V/mV
	10kΩ Load	1,000	10,000		1,000	10,000		V/mV
DYNAMIC CHARACTERISTICS								
Gain Bandwidth Product			1.3			1.3		MHz
Rated Performance								
Full Power Bandwidth			48			48		kHz
Slew Rate			3			3		V/µs
Settling Time	10V Step to 0.1%		4			4		µs
POWER SUPPLY								
Operating Voltage Range	Differential	+4*		+36*	+4*		+36*	V
Quiescent Current				400*			400*	µA
TEMPERATURE RANGE								
Rated Performance								
Commerical (0 to +70°C)			AD821JN, AD821JR			AD821KN		
Industrial (−25°C to +85°C)			AD821AQ			AD821BQ		
Military (−55°C to +125°C)			AD821SQ					
PACKAGE OPTIONS[5]								
Plastic (N-8)			AD821JN			AD821KN		
Cerdip (Q-8)			AD821AQ, AD821SQ			AD821BQ		
SOIC (R-8)			AD821JR					

NOTES
*Indicates parameter guaranteed and tested
[1]Condition 1 ± 15V power supply, Condition 2 +5V power supply
[2]Input offset voltage specifictions are guaranteed after 5minutes of operation at $T_A = 25°C$.
[3]Bias Current specifications are guaranteed maximum at either input after 5minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[4]Defined as voltage between inputs
[5]See Section 16 for package outline information
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±36V
Output Short-Circuit Duration	Indefinite
Internal Power Dissipation	
Plastic	TBD
Cerdip	1.6W
SOIC	TBD
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AD821J/R	0 to +70°C
AD821A/B	−40°C to +85°C
AD821S	−55°C to +125°C
Maximum Junction Temperature	+150°C
Lead Temperature Range (Soldering 10sec)	+260°C

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

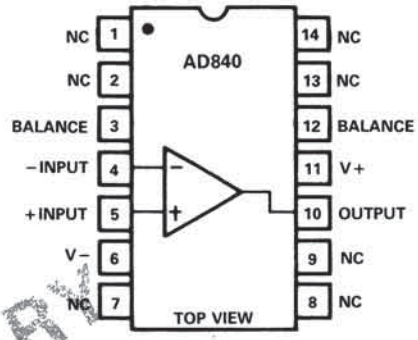
AC PERFORMANCE
- Gain Bandwidth Product: 400MHz (Gain = 10)
- Fast Settling: 100ns to 0.01%
- Slew Rate: 400V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4MHz for 20V p-p into a 500Ω Load

DC PERFORMANCE
- Input Offset Voltage: 0.5mV max
- Input Offset Drift: 5μV/°C max
- Input Voltage Noise: 3nV/$\sqrt{Hz}$
- Open-Loop Gain: 200V/mV into a 1kΩ Load
- Output Current: 50mA min
- Supply Current: 12mA max

APPLICATIONS
- Video and Pulse Amplifiers
- DAC and ADC Buffers
- Line Drivers
- Available in 14-Pin Plastic DIP and Hermetic Cerdip Packages
- Chips and MIL-STD-883B Parts Available

AD840 CONNECTION DIAGRAM

Plastic DIP (N) Package
and
Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high-speed/high-precision family includes, among others, the AD841, which is unity-gain stable and the AD842, which is stable at a gain of two or greater and has 100mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12mA maximum, a minimum output current drive capability of 50mA, a low input voltage noise of 3nV/$\sqrt{Hz}$, and a low input offset voltage of 0.5mV maximum.

The 400V/μs slew rate of the AD840, along with its 400MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high-frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high-speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

PRELIMINARY DATA

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers, and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the speed of the CB process allow the AD840 to settle to 0.01% in 100ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.5mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high-frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	**1**		0.2	**0.5**		0.2	**1**	mV
	$T_{min}-T_{max}$			1.5			**0.7**			**2**	mV
Offset Drift				10			5			10	μV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	μA
	$T_{min}-T_{max}$			10			**6**			**12**	μA
Input Offset Current			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	μA
	$T_{min}-T_{max}$			0.5			**0.3**			**0.6**	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**			**±10**			**±10**			V
Common-Mode Rejection	$V_{CM}=\pm10V$	**90**	110		**100**	110		**90**	110		dB
	$T_{min}-T_{max}$	85			**90**			85			dB
INPUT VOLTAGE NOISE	f = 1kHz		3			3			3		nV/√Hz
Wideband Noise	10Hz to 10MHz		10			10			10		μV rms
OPEN LOOP GAIN	$V_O=\pm10V$										
	$R_{LOAD}=1k\Omega$	**100**	200		150	200		**100**	200		V/mV
	$T_{min}-T_{max}$	50	80		75	100		**50**	80		V/mV
	$R_{LOAD}=500\Omega$	75			**100**			75			V/mV
	$T_{min}-T_{max}$	50			75			35			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq500\Omega$										
	$T_{min}-T_{max}$	**±10**			**±10**			**±10**			V
Current	$V_{OUT}=\pm10V$	**50**			**50**			**50**			mA
OUTPUT RESISTANCE	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	$V_{OUT}=90mV$ p-p										
	$A_{VCL}=10$		400			400			400		MHz
Full Power Bandwidth[2]	$V_O=20V$ p-p										
	$R1\geq500\Omega$	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	$A_{VCL}=10$		10			10			10		ns
Overshoot	$A_{VCL}=10$		20			20			20		%
Slew Rate	$A_{VCL}=10$	350	400		350	400		350	400		V/μs
Settling Time – 10V Step	$A_{VCL}=10$										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	– Overdrive		160			160			160		ns
	+ Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 3.58MHz		0.1			0.1			0.1		%
Differential Phase	f = 3.58MHz		0.1			0.1			0.1		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			11	**12**		11	**12**		11	**12**	mA
	$T_{min}-T_{max}$			14			**14**			**16**	mA
Power Supply Rejection Ratio	$V_S=\pm5V$ to $\pm15V$	**90**	100		**94**	100		**90**	100		dB
	$T_{min}-T_{max}$	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[3]		**0**		**+75**	**0**		**+75**	**−55**		**+125**	°C
PACKAGE OPTIONS[4]											
Cerdip (Q-14)			AD840JQ			AD840KQ			AD840SQ		
Plastic (N-14)			AD840JN			AD840KN					

PRELIMINARY TECHNICAL DATA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at $T_A = +25°C$.
[2]Full power bandwidth = slew rate/$2\pi V_{PEAK}$.
[3]"S" grade is tested with automatic test equipment at $T_A = -55°C$ and $T_A = +125°C$.
[4]See Section 16 for package outline information.

All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

Wideband, Unity-Gain Stable, Fast Settling Op Amp

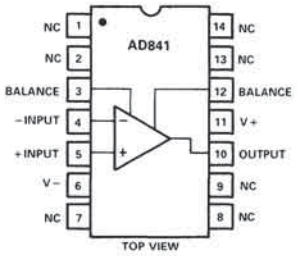
AD841

FEATURES
AC PERFORMANCE:
Unity-Gain-Bandwidth Product: 40MHz
Fast Settling: 110ns to 0.01%
Slew Rate: 300V/μs
Stable at Gains of 1 or Greater
Full Power Bandwidth: 4.7MHz

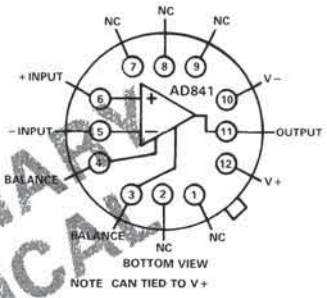
DC PERFORMANCE
Input Offset Voltage: 1mV max
Input Offset Drift: 25μV/°C
Input Voltage Noise: 13nV/$\sqrt{Hz}$
Open-Loop Gain: 50V/mV into a 500Ω Load
Output Current: 50mA min
Supply Current: 12mA max

APPLICATIONS
Video and Pulse Amplifiers
Active Filters
High-Frequency Signal Conditioning Circuitry
Available in Plastic DIP, Hermetic Metal Can and Hermetic Cerdip Packages
MIL-STD-883B Parts Available

AD841 CONNECTION DIAGRAMS



Plastic DIP (N) Package and Cerdip (Q) Package



TO-8 (H) Package

PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100mA output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to 40MHz unity-gain bandwidth, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 110ns for a 10 volt step.

The AD841 is remarkably easy to use: it only requires two 0.01μF decoupling capacitors, one for each power supply line. External compensation is *not* required. It remains stable over its full operating temperature range. The AD841 also offers a low quiesent current (12mA), high output current drive capablity (50mA), low input voltage noise (13nV/$\sqrt{Hz}$), and low input offset voltage (1mV).

The 300V/μs slew rate of the AD841, along with its 40MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high-frequency signal conditioning circuits and high-bandwidth active filters. The extremely rapid settling time of the AD841 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high-speed integrators and sample and hold circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for D/A, A/D, sample-and-hold amplifiers, high-speed integrators, and video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser wafer trimming reduces the input offset voltage to 1mV max, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for greater versatility.
4. Full differential inputs provide outstanding performance in all standard high-frequency op amp applications such as signal conditioning and active filters.
5. The AD841 is an enhanced replacement for the HA2541.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD841J Min	AD841J Typ	AD841J Max	AD841K Min	AD841K Typ	AD841K Max	AD841S Min	AD841S Typ	AD841S Max	Units
INPUT OFFSET VOLTAGE[1]			0.5	**1.5**		0.5	**1**		0.5	**1.5**	mV
	$T_{min}-T_{max}$			3.0			**2.0**			**4.5**	mV
Offset Drift				25			25			25	µV/°C
INPUT BIAS CURRENT			3.5	**8**		3 5	**5**		3 5	**8**	µA
	$T_{min}-T_{max}$			10			**6**			**12**	µA
Input Offset Current			0 1	**0.4**		0.1	**0.2**		0.1	**0.4**	µA
	$T_{min}-T_{max}$			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS											
Input Resistance			200			200			200		kΩ
Input Capacitance			1.0			1.0			1.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10V	**86**	100		**90**	100		**86**	100		dB
	$T_{min}-T_{max}$	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1kHz		13			13			13		nV/√Hz
Wideband Noise	10Hz to 10MHz		40			40			40		µV rms
OPEN LOOP GAIN	V_O = ±10V										
	$R_{LOAD} \geq 500\Omega$	**25**	50		**25**	50		**25**	50		V/mV
	$T_{min}-T_{max}$	12			**12**			**12**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 500\Omega$	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90mV		40			40			40		MHz
Full Power Bandwidth[2]	V_O = 20V p-p										
	$R_L \geq 500\Omega$	3 1	4.7		3.1	4 7		3 1	4.7		MHz
Rise Time	A_{VCL} = 1		10			10			10		ns
Overshoot	A_{VCL} = 1		20			20			20		%
Slew Rate	A_{VCL} = 1	200	300		200	300		200	300		V/µs
Settling Time – 10V Step	A_{VCL} = 1										
	to 0 1%		80			80			80		ns
	to 0 01%		110			110			110		ns
Differential Gain	f = 3 58MHz		0 1			0 1			0.1		%
Differential Phase	f = 3.58MHz		0 1			0 1			0.1		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	± 5		**±18**	±5		**±18**	V
Quiescent Current				**12**			**12**			**12**	mA
	$T_{min}-T_{max}$			14			**14**			**16**	mA
Power Supply Rejection Ratio	±5V to ±18V	**86**	100		**90**	100		**86**	100		dB
	$T_{min}-T_{max}$	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance		0		+ 75	0		+ 75	- 55		+ 125	°C
PACKAGE OPTIONS[3]											
Plastic (N-14)			AD841JN			AD841KN					
Cerdip (Q-14)			AD841JQ			AD841KQ			AD841SQ		
Metal Can (H-12A)			AD841JH			AD841KH			AD841SH		

PRELIMINARY TECHNICAL DATA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C
[2]FPBW = Slew Rate/2π V_{PEAK}
[3]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

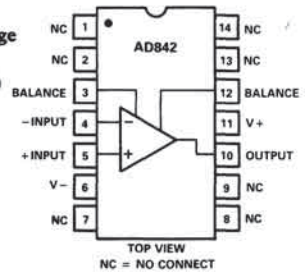
AC PERFORMANCE
- Gain Bandwidth Product: 80MHz (Gain = 2)
- Fast Settling: 100ns to 0.01%
- Slew Rate: 375V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0MHz

DC PERFORMANCE
- Input Offset Voltage: 1mV max
- Input Offset Drift: 10μV/°C max
- Input Voltage Noise: 9nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90V/mV into a 500Ω Load
- Output Current: 100mA min
- Quiescent Supply Current: 14mA max

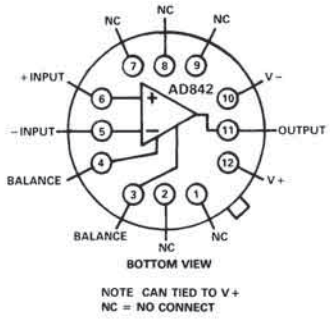
APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP, Hermetic Metal Can and Hermetic Cerdip Packages
- MIL-STD-883B Parts Available.

AD842 CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package)



TO-8 (H) Package



PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13mA, a high output current drive capablity (100mA min), a low input voltage noise of 9nV/$\sqrt{Hz}$ and a low input offset voltage (1mV).

The 375V/μs slew rate of the AD842, along with its 80MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and high-bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high-speed DAC and ADC buffer amplifiers and other wide-bandwidth circuitry.

PRELIMINARY TECHNICAL DATA

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffer amplifiers, line drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage to 1mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD842J Min	AD842J Typ	AD842J Max	AD842K Min	AD842K Typ	AD842K Max	AD842S Min	AD842S Typ	AD842S Max	Units
INPUT OFFSET VOLTAGE[1]			0.5	1.5		0.5	1		0.5	1.5	mV
	$T_{min}-T_{max}$			2.5			1.5			3.5	mV
Offset Drift				20			10			20	µV/°C
INPUT BIAS CURRENT			3.5	8		3.5	5		3.5	8	µA
	$T_{mun}-T_{max}$			10			6			12	µA
Input Offset Current			0.1	0.4		0.1	0.2		0.1	0.4	µA
	$T_{mun}-T_{max}$			0.5			0.3			0.6	µA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			1.0			1.0			1.0		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
Common-Mode Rejection	$V_{CM}=\pm 10V$	86	100		90	100		86	100		dB
	$T_{mun}-T_{max}$	80			86			80			dB
INPUT VOLTAGE NOISE	f = 1kHz		9			9			9		nV/√Hz
Wideband Noise	10Hz to 10MHz		28			28			28		µV rms
OPEN LOOP GAIN	$V_O=\pm 10V$										
	$R_{LOAD}\geq 500\Omega$	40	90		50	90		40	90		V/mV
	$T_{mun}-T_{max}$	20			25			20			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq 1k\Omega$	±10			±10			±10			V
Current	$V_{OUT}=\pm 10V$	100			100			100			mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	$V_{OUT}=90mV$										
	$A_{VCL}=2$		80			80			80		MHz
Full Power Bandwidth[2]	$V_O=20V$ p-p										
	$R1=100\Omega$	4.7	6		4.7	6		4.7	6		MHz
Rise Time	$A_{VCL}=2$		10			10			10		ns
Overshoot	$A_{VCL}=2$		20			20			20		%
Slew Rate	$A_{VCL}=2$	300	375		300	375		300	375		V/µs
Settling Time	10V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 3.58MHz		0.1			0.1			0.1		%
Differential Phase	f = 3.58MHz		0.1			0.1			0.1		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current				14			14			14	mA
	$T_{mun}-T_{max}$			16			16			19	mA
Power Supply Rejection Ratio	$V_S=\pm 5V$ to $\pm 15V$	86	100		90	100		86	100		dB
	$T_{mun}-T_{max}$	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[3]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ		
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		

PRELIMINARY TECHNICAL DATA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at $T_A = +25°C$.

[2]FPBW = Slew Rate/$2\pi V_{PEAK}$.

[3]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications marked in **boldface** are tested on all production units at final electrical test.

Precision 16MHz CBFET Op Amp

AD845

FEATURES

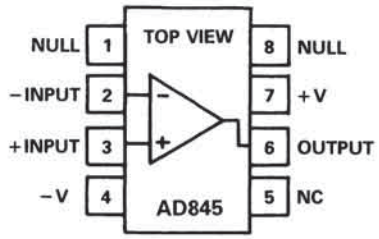
Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:
Settles to 0.01% in 350ns
100V/μs Slew Rate
12.8MHz min Unity-Gain Bandwidth
1.75MHz Full-Power Bandwidth at 20V p-p

DC PERFORMANCE:
0.25mV max Input Offset Voltage
5μV/°C max Offset Voltage Drift
0.4nA Input Bias Current
250V/mV min Open-Loop Gain
4μV p-p max Voltage Noise, 0.1Hz to 10Hz
94dB min CMRR
Available in Plastic Mini-DIP and Hermetic Cerdip Packages

AD845 CONNECTION DIAGRAM

8-Pin Plastic (N) and and Cerdip (Q) Packages



NOTE: PIN 4 CONNECTED TO CASE

PRELIMINARY DATA

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100V/μs, a stable unity-gain bandwidth of 16MHz, and a settling time of 350ns to 0.01% – while driving a parallel load of 100pF and 500Ω – represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar op amps.

The AD845 is ideal for use in applications such as active filters, high-speed integrators, photo diode preamps, sample and hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110dB over a ± 10V input voltage range represents exceptional performance for a JFET input high-speed op amp. This, together with an open-loop gain of 250V/mV ensures that 12-bit performance is achieved, even in unity gain buffer circuits.

The AD845 conforms to the standard 741 pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 to +70°C temperature range. AD845A and AD845B devices are specified for operation over the −40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of −55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high-speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, OP-42, OP-16, OP-17, LT1022, LT1056, HA2510, AD381, and AD382 can be upgraded in most cases.
3. The AD845 is unity-gain stable and is internally compensated.
4. The AD845 is specified while driving 100pF/500Ω loads.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	$T_{min}-T_{max}$			2.5			**0.4**			**2.0**	mV
Offset Drift				20		1.5	5.0			10	μV/°C
INPUT BIAS CURRENT[2]											
Initial	$V_{CM}=\pm10V$		500	**1000**		250	**400**		500	**1000**	pA
	$T_{min}-T_{max}$			30/65			**12/26**			**1100**	nA
INPUT OFFSET CURRENT											
Initial	$V_{CM}=\pm10V$		25	**100**		15	**50**		25	**100**	pA
	$T_{min}-T_{max}$			3/6.5			**1.2/2.6**			**110**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential		**±20**			**±20**			**±20**			V
Common Mode		**+10.5/−13**			**+10.5/−13**			**+10.5/−13**			V
Common-Mode Rejection	$V_{CM}=\pm10V$	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		4			4			4		μV p-p
	f = 10Hz		80			80			80		nV/√Hz
	f = 100Hz		60			60			60		nV/√Hz
	f = 1kHz		25			25			25		nV/√Hz
	f = 10kHz		18			18			18		nV/√Hz
	f = 100kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	$V_O=\pm10V$										
	$R_{LOAD}\geq2k\Omega$	**200**	500		**250**	500		**200**	500		V/mV
	$R_{LOAD}\geq500\Omega$	**100**	250		**125**	250		**100**	250		V/mV
	T_{min} to T_{max}	70			**80**			**70**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq500\Omega$	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop										Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	$V_O=\pm10V$										
	R1 = 500Ω		1.75			1.75			1.75		MHz
Rise Time											ns
Overshoot											%
Slew Rate		80	100		94	100		94	100		V/μs
Settling Time	10V Step										
	C_{LOAD} = 200pF										ns
	R_{LOAD} = 500ΩF										ns
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
Rejection Ratio	$V_S=\pm5$ to $\pm15V$	**88**	110		**98**	113		**88**	110		dB
Quiescent Current	$T_{min}-T_{max}$		10	**15**		10	**15**		10	**15**	mA
TEMPERATURE RANGE											
Operating, Rated Performance		0/−40		75/85	0/−40		75/85	−55		+125	°C
PACKAGE OPTIONS[4]											
Cerdip (Q-8)			AD845AQ			AD845BQ			AD845SQ		
Plastic Mini-DIP (N-8)			AD845JN			AD845KN					

PRELIMINARY TECHNICAL DATA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.
[3]FPBW = slew rate/2π V peak.
[4]See Section 16 for package outline information
Specifications subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Very High-Speed Operational Amplifier

AD846

FEATURES

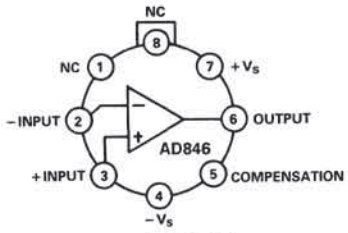
AC PERFORMANCE
- Small Signal Bandwidth: 46MHz ($A_V = -1$)
- Slew Rate: 450V/μs
- Full Power Bandwidth: 6.8MHz at 20V p-p, $R_L = 500\Omega$
- Fast Settling: for 10V Step: 110ns to 0.01%, 80ns to 0.1%
- Differential Gain: <0.1% @ 3.58MHz
- Differential Phase: <0.1° @ 3.58MHz
- Total Harmonic Distortion (THD): 0.0002% @ 100kHz
- Open-Loop Transimpedance: 500MΩ

DC PERFORMANCE
- Input Offset Voltage: 75μV max (K Grade)
- Input Offset Drift: 2μV/°C max (K Grade)
- Input Voltage Noise: 2nV/$\sqrt{Hz}$
- Output Current: 50mA min
- Quiescent Supply Current: 6mA max

APPLICATIONS
- High-Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

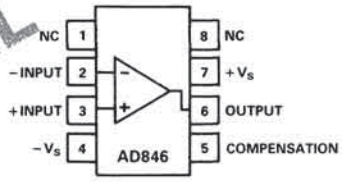
AD846 PIN CONFIGURATIONS

TO-99 (H) Package



NOTE CAN TIED TO V+
NC = NO CONNECT
TOP VIEW

Plastic DIP (N) Package and Cerdip (Q) Package)



NC = NO CONNECT

PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD846 is a monolithic, very high-speed operational amplifier offering high performance. Although technically classed as a transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high-speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog to digital converters.

Other advantages include: low input errors and high open-loop transresistance (500MΩ) into a 500Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high-speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846J and AD846K are rated over the commercial temperature range of 0 to +70°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in three types of 8-pin package: plastic mini-DIP, hermetic cerdip or TO-99 hermetic metal cans.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110ns to 0.01% for gains of −1 to −10, with a 450V/μs slew rate, while consuming only 5mA of supply current.
2. For closed-loop gains of −1 to −100, the high-speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD846J Min	AD846J Typ	AD846J Max	AD846K Min	AD846K Typ	AD846K Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**300**		25	**150**		25	**300**	μV
T_{min}–T_{max}			100	400		75	**250**		200	**800**	μV
vs. Temperature			2	10		1	**5**		2	**10**	μV/°C
vs. Supply	8V–18V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**104**	116		dB
vs. Common Mode	V_{CM} = ±10V										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**104**	116		dB
INPUT BIAS CURRENT[3]											
– Input Bias Current											
Initial			75	**450**		75	**250**		75	**450**	nA
T_{min}–T_{max}			375	900		325	**600**		2100	**2700**	nA
vs. Temperature			6.5	15		5.5	**10**		20	**30**	nA/°C
vs. Supply	8V–18V[2]										
Initial			5	**10**		4	**7**		5	**10**	nA/V
T_{min}–T_{max}			5	10		4	**7**		5	**20**	nA/V
vs. Common Mode	V_{CM} = ±10V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{min}–T_{max}			5	10		3	**5**		5	**20**	nA/V
+ Input Bias Current											
Initial			10	**20**		10	**15**		10	**20**	μA
T_{min}–T_{max}			12	**30**		12	**20**		14	**30**	μA
vs. Temperature			40	150		40	**75**		40	**150**	**nA**/°C
vs. Supply	8V–18V[2]										
Initial			10	**25**		7	**15**		10	**25**	nA/V
T_{min}–T_{max}			10	25		7	**15**		10	**25**	nA/V
vs. Common Mode	V_{CM} = ±10V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
– Input			67			67			67		Ω
+ Input			10			10			10		kΩ
Input Capacitance											
– Input			2			2			2		pF
+ Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1kHz		2			2			2		nV/√Hz
Wideband Noise	10Hz to 10MHz		5			5			5		μV rms
Input Current Noise											
– Input	1kHz		20			20			20		pA/√Hz
– Input	10Hz–10MHz		6			6			6		nA rms
+ Input	1kHz		6			6			6		pA/√Hz
+ Input	10Hz–10MHz		20			20			20		nA rms
OPEN LOOP											
Transresistance	V_{OUT} = ±10V										
	R_{LOAD} = 500Ω	**150**	500		**250**	500		**150**	500		MΩ
	T_{min}–T_{max}	100			**100**			**70**			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500Ω	**±10**			**±10**			**±10**			V
Current		**50**			**50**			**50**			mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = –1[4] R_F = 1k		46			46			46		MHz
(–3dB)	A_V = –10 R_F = 875Ω		31			31			31		MHz
	A_V = –30 R_F = 875Ω		15			15			15		MHz
FULL POWER BANDWIDTH[4]	V_{OUT} = 20V p-p										
	R_L = 500Ω	5.5	6.8		5.5	6.8		5.5	6.8		MHz
RISE TIME	A_V = –1		10			10			10		ns
Overshoot	A_V = –1		20			20			20		%
Slew Rate	A_V = –1	350	450		350	450		350	450		V/μs
Settling Time											
10V Step, A_V = –1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
THD[5]	F = 100kHz		0.0002			0.0002			0.0002		%

PRELIMINARY TECHNICAL DATA

Model		AD846J			AD846K			AD846S			
	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
DIFFERENTIAL GAIN	F = 3.58MHz		0 1			0.1			0.1		%
Differential Phase	F = 3.58MHz		0 1			0.1			0.1		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±6		±18	±5		±18	±5		±18	V
Quiescent Current	T_{min}–T_{max}		5	6		5	6		5	7	mA
TEMPERATURE RANGE											
Rated Performance		0		70	0		70	−55		+125	°C
PACKAGE OPTIONS[6]											
Plastic (N-8)			AD846JN			AD846KN					
Metal Can (H-08A)			AD846JH			AD846KH			AD846SH		
Cerdip (Q-8)			AD846JQ			AD846KQ			AD846SQ		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at $T_A = +25°C$.
[2]Test Conditions: $+V_S = 15V$, $-V_S = 8V$ to 18V and $+V_S = 8V$ to 18V, $-V_S = -15V$.
[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes at $T_A = +25°C$.
[4]FPBW = Slew Rate/$2\pi V_{PEAK}$.
[5]Total Harmonic Distortion.
[6]See Section 16 for package outline information.

Specifications marked in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
  TO-99 . . . . . 1.0W
  Plastic Package 1.6W
  Cerdip Package 1.5W
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±6V
Continuous Input Current
  Inverting or Noninverting 2.0mA
Storage Temperature Range H, Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
  AD846J/K . . . . . 0 to +70°C
  AD846S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]TO-99Package: $\theta_{JA} = 150°C/Watt$.
Plastic Package: $\theta_{JA} = 90°C/Watt$.
Cerdip Package: $\theta_{JA} = 100°C/Watt$.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Typical Characteristics

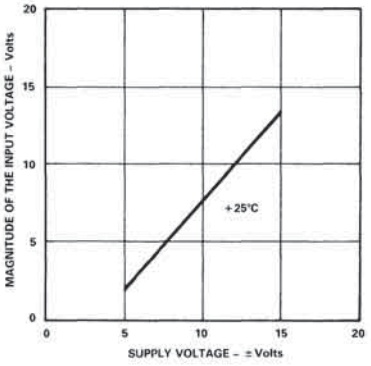


Figure 1. Input Voltage Swing vs. Supply

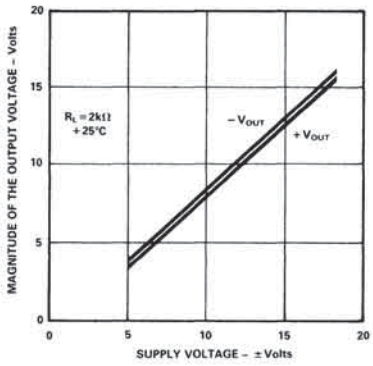


Figure 2. Output Voltage Swing vs. Supply

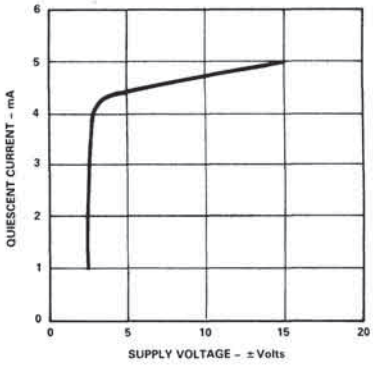


Figure 3. Quiescent Current vs. Supply Voltage

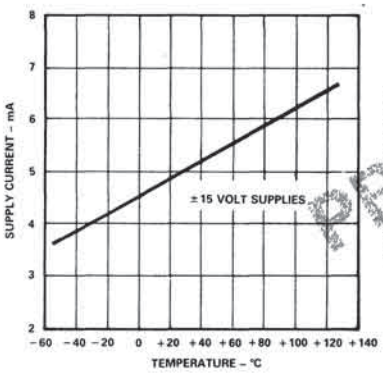


Figure 4. Quiescent Supply Current vs. Temperature

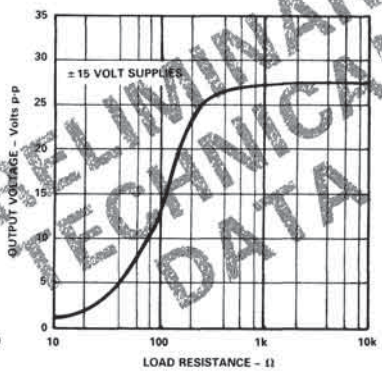


Figure 5. Output Voltage Swing vs. Resistive Load

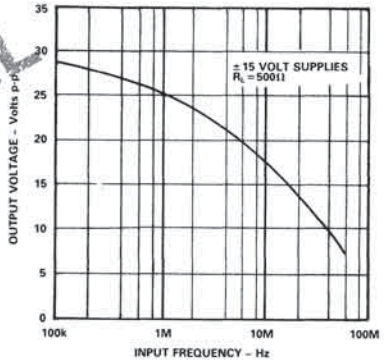


Figure 6. Large Signal Frequency Response

PRELIMINARY TECHNICAL DATA

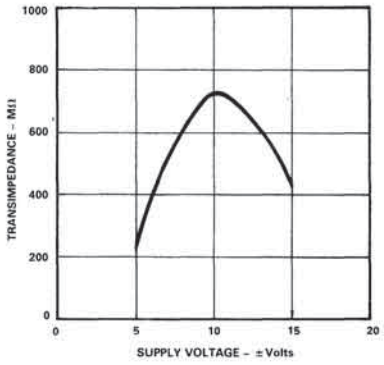


Figure 7. Open-Loop Trans-impedance vs. Supply

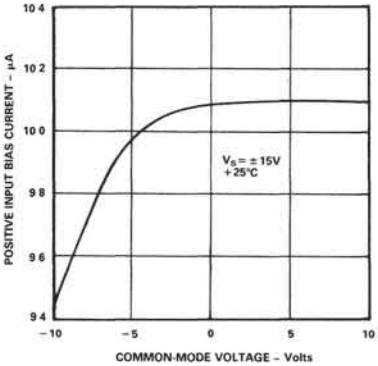


Figure 8. Positive Input Bias Current vs. Common-Mode Voltage

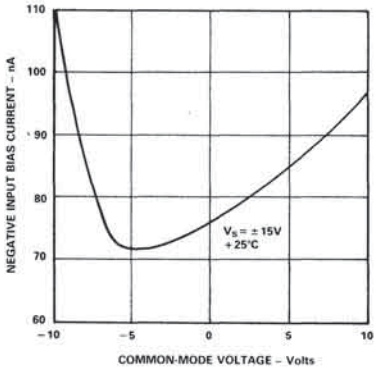


Figure 9. Negative Input Bias Current vs. Common-Mode Voltage

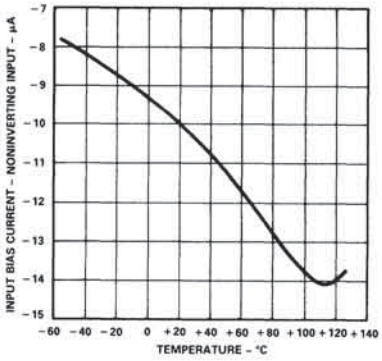


Figure 10. Positive Input Bias Current vs. Temperature

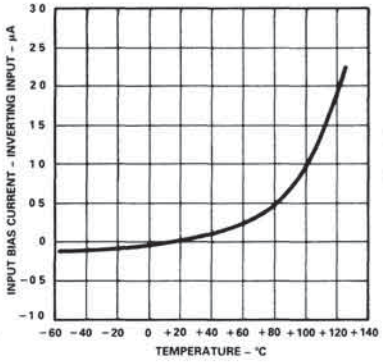


Figure 11. Negative Input Bias Current vs. Temperature

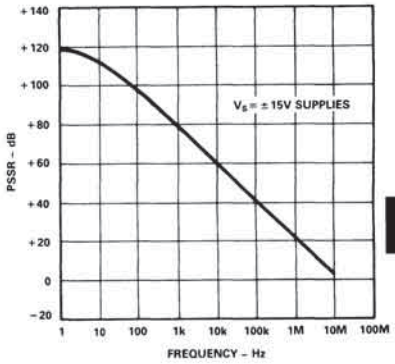


Figure 12. Power Supply Rejection vs. Frequency

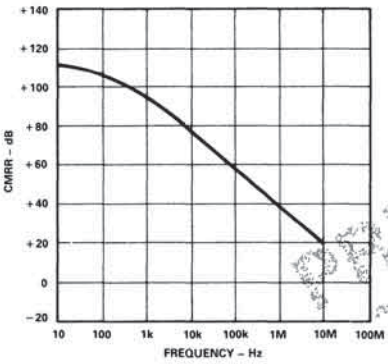


Figure 13. Common-Mode Rejection vs. Frequency

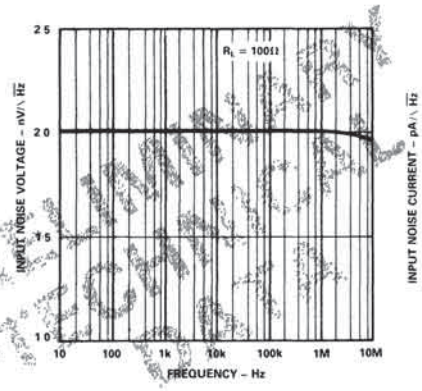


Figure 14. Input Noise Voltage Spectral Density

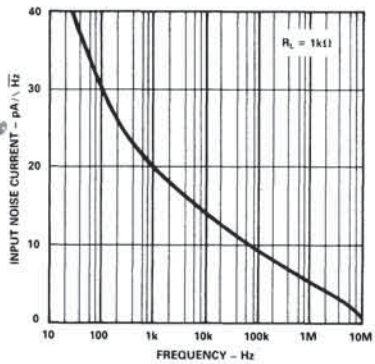


Figure 15. Input Noise Current Spectral Density

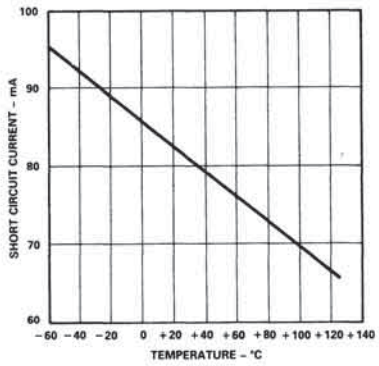


Figure 16. Short Circuit Current Limit vs. Temperature

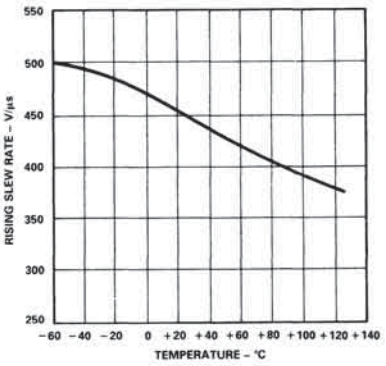


Figure 17. Slew Rate vs. Temperature

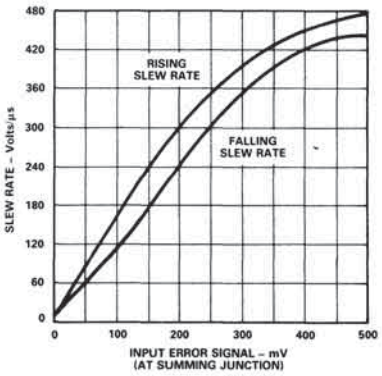


Figure 18. Slew Rate vs. Input Error Signal

Typical Characteristics, Inverting Gain of 1

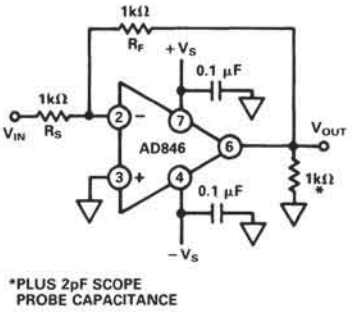


Figure 19a. Inverting Amplifier, Gain of 1

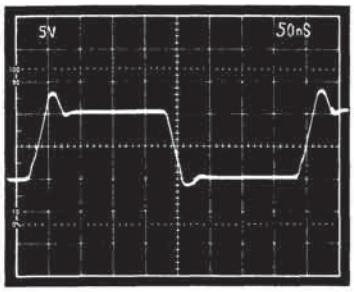


Figure 19b. Large Signal Pulse Response, Gain of 1

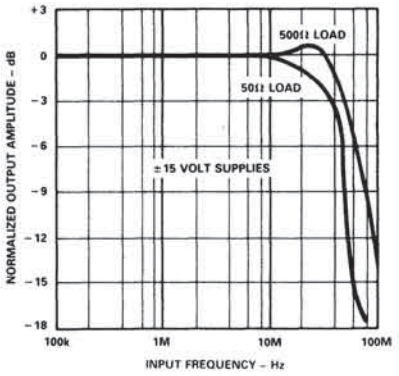


Figure 20. Close Loop Gain vs. Frequency vs. Load

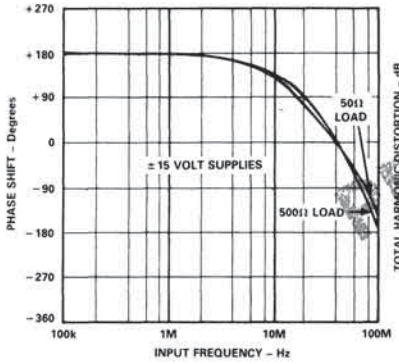


Figure 21. Phase vs. Frequency vs. Load

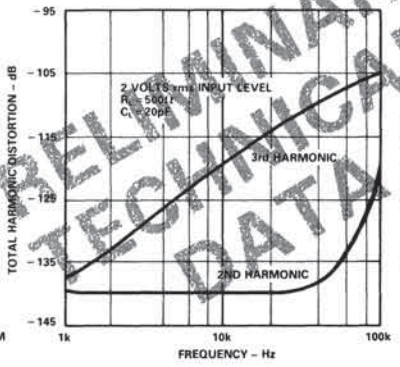


Figure 22. Harmonic Distortion vs. Frequency

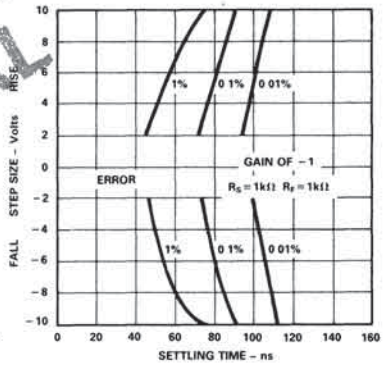


Figure 23. Settling Time vs. Step Size

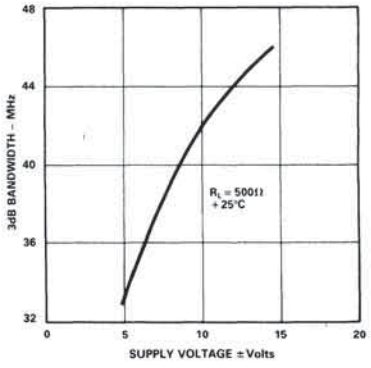


Figure 24. 3dB Bandwidth vs. Supply Voltage

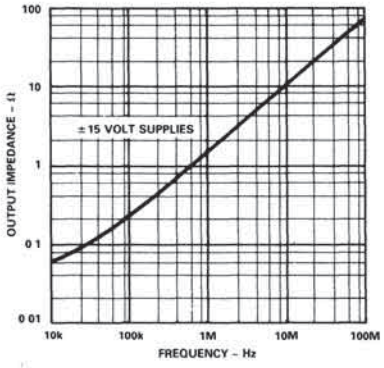


Figure 25. Output Impedance vs. Frequency

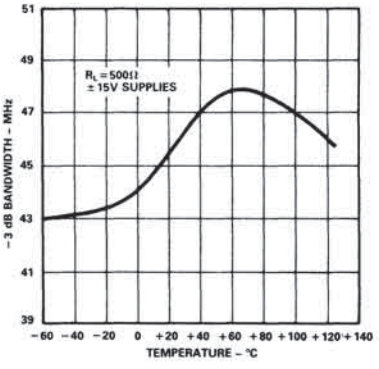


Figure 26. 3dB Bandwidth vs. Temperature

PRELIMINARY TECHNICAL DATA

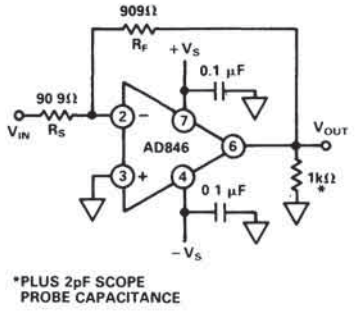


Figure 27a. Inverting Amplifier, Gain of 10.

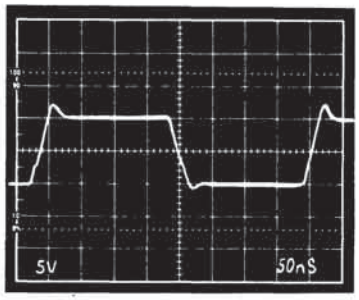


Figure 27b. Large Signal Pulse Response, Gain of 10

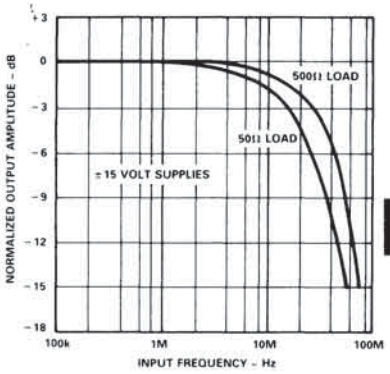


Figure 28. Closed-Loop Gain vs. Frequency vs. Load

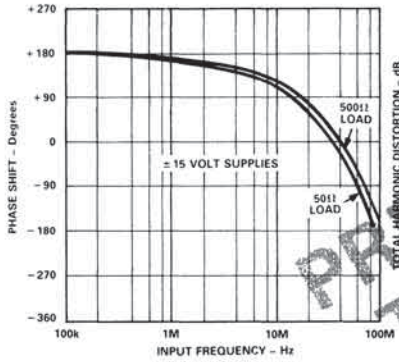


Figure 29. Phase vs. Frequency vs. Load

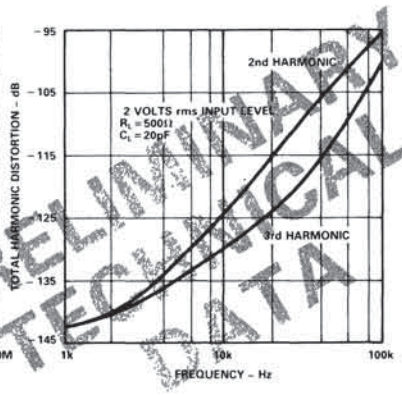


Figure 30. Harmonic Distortion vs. Frequency

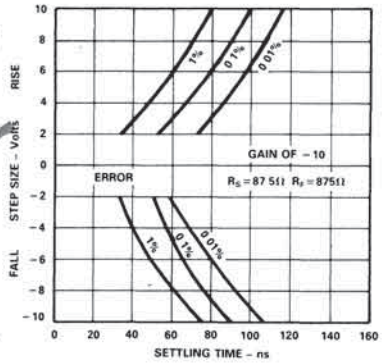


Figure 31. Settling Time vs. Step Size

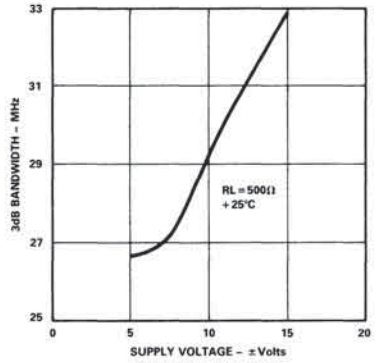


Figure 32. 32dB Bandwidth vs. Supply Voltage

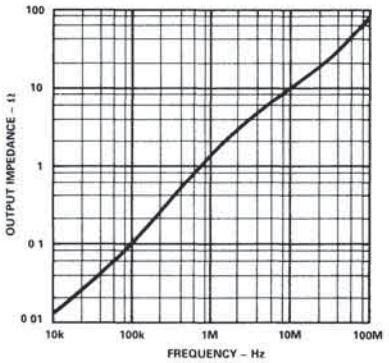


Figure 33. Output Impedance vs. Frequency

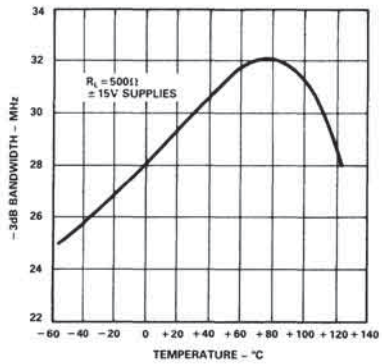


Figure 34. 3dB Bandwidth vs. Temperature

PRELIMINARY TECHNICAL DATA

Applying the AD846

POWER SUPPLY BYPASSING

The power supply connections to the AD846 must maintain a low impedance to ground over a bandwidth of 40MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 2.2μF electrolytic capacitor as shown in Figure 35 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

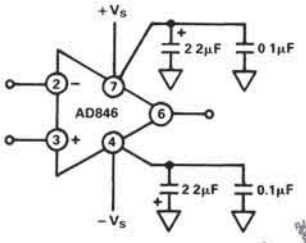


Figure 35. Recommended Power Supply Bypassing

THEORY OF OPERATION

The AD846 differs from conventional operational amplifiers in that it is a transimpedance device rather than a conventional voltage amplifier. Figure 36 is a simplified schematic of the AD846. The input stage consists of a pair of transistors, Q1 and Q2, which are biased by two diode-connected transistors, Q3 and Q4. Transistors Q1 and Q2 have their emitters connected together and this common point functions as the inverting input of the amplifier. Correspondingly, the common connection of the two biasing diodes acts as the noninverting input.

When operated as a closed-loop amplifier, feedback error current, I_{IN}, flows into the inverting input terminal and is conveyed via current mirrors (transistors Q5, Q6, Q7, and Q8) to the compensation capacitor, C_{COMP}. The voltage developed across C_{COMP} is buffered by the output stage, consisting of transistors Q9–Q12.

Because the input error signal developed is in the form of a current, not a voltage, the AD846 differs from conventional operational amplifiers. This also means that, unlike most operational amplifiers which rely on negative feedback to produce a "virtual ground" at the inverting input terminal, this terminal explicitly has a low impedance.

A unique circuit approach allows the AD846 to realize an open-loop transimpedance of close to 1GΩ. This is nearly three orders of magnitude greater than that of any other operational transimpedance amplifier and results in extremely high levels of dc precision.

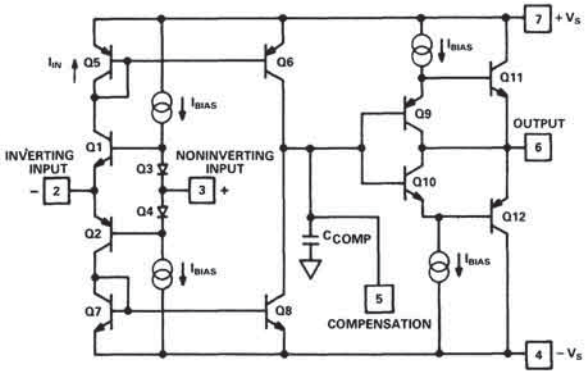


Figure 36. AD846 Simplified Schematic

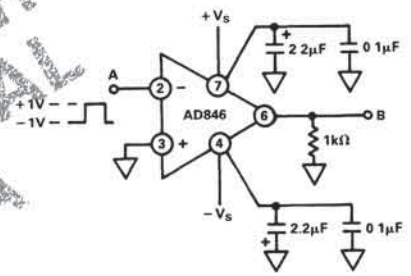


Figure 37. Overload Recovery Test Circuit

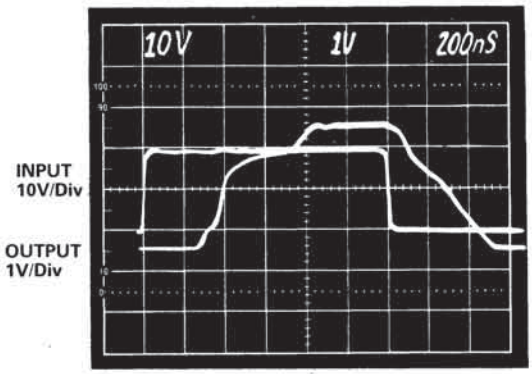


Figure 38. Overload Recovery Time Photo

As an example, the output voltage gain error is approximately equal to the value of the feedback resistor divided by the value of the open-loop transimpedance of the amplifier. That is, when using a 1kΩ feedback resistor, this error is one part in 500,000. For a transimpedance amplifier with 1MΩ transimpedance, this error is only one part in 1000; such an amplifier would barely be able to achieve 10-bit precision.

PRELIMINARY TECHNICAL DATA

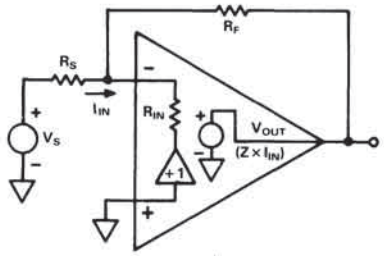


Figure 39. AD846 Three-Terminal Model

Figure 39 is a simplified three-terminal model for the AD846. Figure 40 is a simplified three-terminal model for a conventional voltage op amp. The action of current feedback serves to modify the behavior of the amplifier under closed-loop conditions. The feedback resistor, R_F, is somewhat analogous to the input stage transconductance of a conventional voltage amplifier; and therefore, if the value of R_F is held constant, the closed-loop bandwidth also remains virtually constant, independent of closed-loop voltage gain.

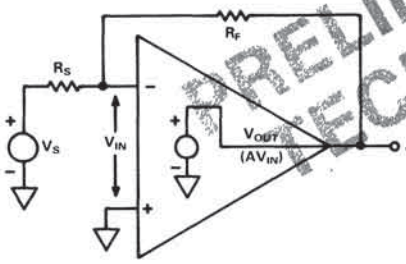


Figure 40. Op Amp Three-Terminal Model

A more detailed examination of the closed-loop transfer function of the AD846 results in the following equation:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{(1 + C_{COMP}[R_F + \left(1 + \frac{R_F}{R_S}\right) R_{IN}]s)}$$

Compare this to the equation for a convention op amp:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{(1 + \frac{C_{COMP}}{g_M}\left(1 + \frac{R_F}{R_S}\right) s)}$$

Where: C_{COMP} is the internal compensation capacitor of the amplifier; g_M is the input stage transconductance of the amplifier.

In the case of the voltage amplifier, the closed-loop bandwidth decreases directly with increasing values of $(1 + R_F/R_S)$, the closed-loop gain. However, for the transimpedance amplifier, the situation is different. At low gains, where $(1 + R_F/R_S)\ R_{IN}$ is small compared to R_F, the closed-loop bandwidth is controlled by the internal compensation capacitance of 3.3pF and the value of R_F, and not by the closed-loop gain. At higher gains, where $(1 + R_F/R_S)\ R_{IN}$ is much larger than R_F, the behavior is that of a conventional operational amplifier in which the input stage transconductance is equal to the inverting terminal input impedance of the transimpedance amplifier ($R_{IN} = 67\Omega$).

A simple equation can, therefore, be used to determine the bandwidth of an amplifier employing the AD846 in the inverting configuration.

$$\text{3dB Bandwidth} = \frac{48}{R_F + 0.067\ (1 + G)}$$

Where: The 3dB bandwidth is in MHz
G is the closed-loop inverting gain of the AD846
R_F is the feedback resistance in kΩ.

Figure 41 illustrates the closed-loop bandwidth vs. closed-loop gain of the AD846 for various values of feedback resistor. For comparison purposes, the characteristic of a conventional amplifier having a 46MHz unity gain bandwidth is also shown.

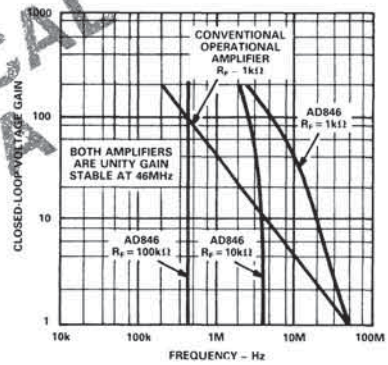


Figure 41. Closed-Loop Gain vs. Bandwidth for Various Values of R_F

For the case where $R_F = 1k\Omega$ and $R_S = 100\Omega$ (closed-loop gain of −10) then the closed-loop bandwidth becomes 28MHz. It should also be noted that the use of a capacitor to shunt R_F, a normal practice for stabilizing conventional op amps, will cause this amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

A similar approach can be taken to calculate the noise performance of the amplifier. A simplified noise model is shown in Figure 42.

The equivalent output noise voltage will equal:

$$V_{ON} = R_F\ I_{NN} + \left(1 + \frac{R_F}{R_S}\right) \sqrt{V_N^2 + (R_P\ I_{NP})^2}$$

Where: R_P is the external resistance placed in series with the noninverting input

R_F is the feedback resistor
R_S is the source resistor
I_{NN} is the noise current in the inverting input
I_{NP} is the noise current in the noninverting input
V_N is the input noise voltage.

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Typical values for these parameters (@ 1kHz) in pA/$\sqrt{Hz}$ are: I_{NN} = 20, I_{PN} = 6, V_N = 2.

Or, referring to the input, the equivalent input voltage noise is:

$$V_{IN} = R_S I_{NN} + \left(1 + \frac{R_S}{R_F}\right)\sqrt{V_N^2 + (R_P I_{NP})^2}$$

As can be seen from the above equation, the addition of R_P degrades the noise performance of the amplifier. In addition, the positive and negative input bias currents are unequal in the AD846. This means that the normal practice of adding resistor R_P to compensate for bias-current-induced-offset errors is highly undesirable and indeed R_P should be made as low as possible.

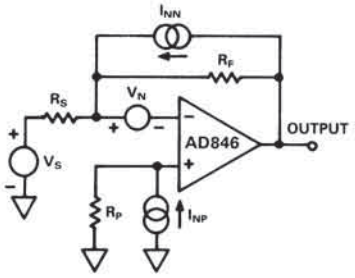


Figure 42. Op Amp Simplified Noise Model

NONINVERTING GAIN OPERATION

The AD846 can be used as a noninverting amplifier or voltage follower, operating at gains between 1 and 200. A minimum value of R_F equal to 1kΩ should be employed. For low gains (1 to 2), the input signal should be applied to the AD846's noninverting input through a 1kΩ series resistor; this will help reduce peaking. The best transient response will occur when the amplifier's output level is below 5V peak to peak.

At closed-loop gains of 3 or more, the input resistor is not required unless peak signals greater than 3V will be applied. The amplifier's bandwidth can be determined by using the inverting amplifier's bandwidth equation or from Figure 41. For example, at a gain of +10 (R_F = 1kΩ, R_S = 100Ω) the bandwidth of the AD846 will be approximately 20MHz; at a gain of +100, (R_F = 1kΩ, R_S = 10Ω) it will be 6MHz. At gains of 3 or greater, a small capacitor (2pF–5pF) connected across the feedback resistor will help reduce overshoot; but when operating at noninverting gains below 3, this same capacitance will cause instability.

USING THE COMPENSATION PIN OF THE AD846

Additional compensation may be provided for the AD846 by applying an external capacitance between Pin 5 and analog ground (Figure 43). The nominal value of the AD846's internal compensation capacitor is 3.3pF. For a given value of feedback resistance (R_F), any added external capacitance reduces the amplifier's slew rate and bandwidth proportionally.

In addition to providing for external compensation, Pin 5 may be used to clamp the output of the amplifier, as shown in Figure 44. The output can be clamped anywhere within the output range (approximately ±10V) of the amplifier. The input should also be clamped as a precaution again damaging the amplifier's input transistors.

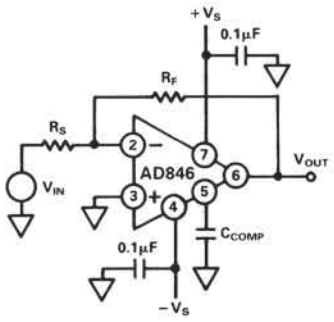


Figure 43. AD846 Inverting Amplifier Showing External Compensation Connection

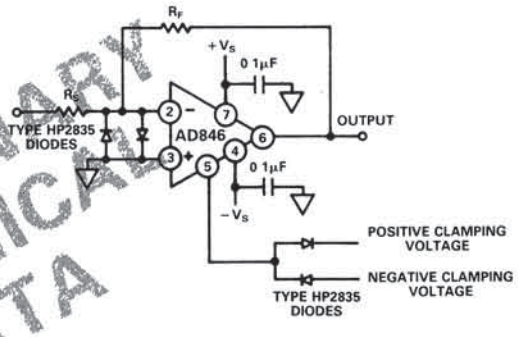


Figure 44. AD846 Used as a Clamped Amplifier

This compensation node may also be used as an additional output terminal as in the precision transconductance amplifier application of Figure 45.

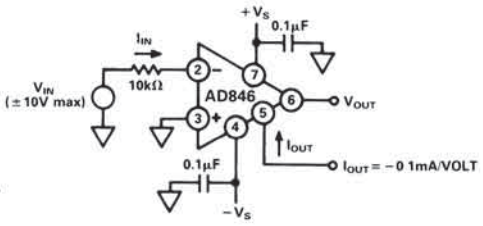


Figure 45. A Precision Transconductance Amplifier

The AD846 can be used in either the inverting transconductance mode as shown in Figure 45, or in a noninverting mode with R_S grounded and V_S applied to the noninverting terminal. The current output is essentially constant over a compliance range of ±10V at the compensation node. The output current is limited to about ±1mA due to internal saturation. Under these circumstances the normal output pin provides a buffered version of the compensation node output voltage. Output load impedance of 500Ω or greater will not affect the accuracy of the transconductance conversion.

PRELIMINARY TECHNICAL DATA

THE AD846 AS AN AUDIO AMPLIFIER

The extremely fast settling and highly linear input characteristics of the AD846 make it a superb audio amplifier. Figure 46 is a circuit for a phono (RIAA) preamplifier and line driver. In this circuit, open-loop servos are used to set the dc operating points of the amplifier.

Adequate power supply regulation is critical in this application, otherwise the performance of the AD846 will suffer. In addition, the deterioration of performance caused by the poor choice of decoupling components (such as the use of tantalum capacitors) is audible. For best performance, all capacitors should be polypropylene.

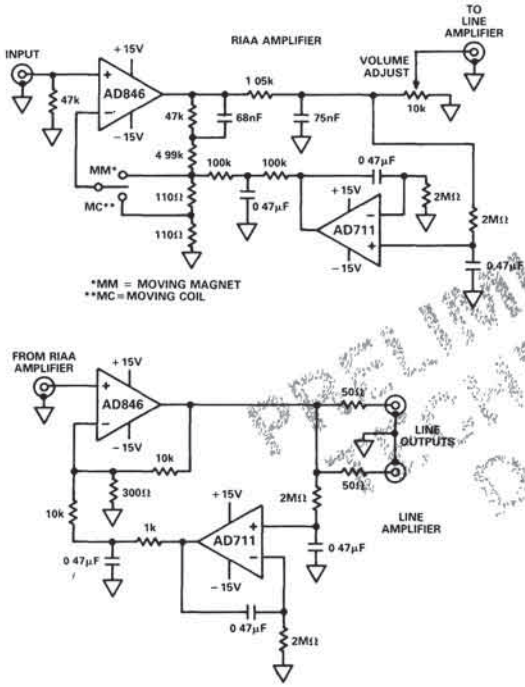


Figure 46. The AD846 RIAA Audio Preamplifier Circuit

THE AD846 AS AN OPEN-LOOP LEVEL SHIFTER

The AD846 can also be used for open-loop level shifting. As shown in Figure 47, resistor R_S is used to develop an input current which is proportional to the input voltage, V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (R_C is equal in value to resistor R_S) which, rather than being grounded, has one end tied to reference voltage V2. The voltage appearing at Pin 5 is, therefore, voltage V_{IN} plus voltage V2 and will directly follow changes in V_{IN}. By scaling resistor R_C, a level shift with voltage gain can be produced. In addition, the normal voltage output at Pin 6 is approximately equal to the voltage at Pin 5 thus providing a low impedance, buffered output for the level shifter.

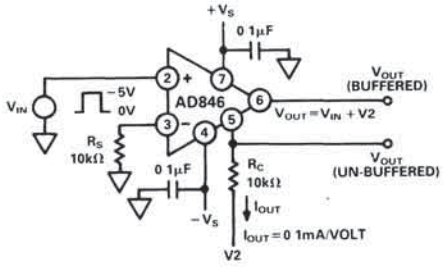


Figure 47. AD846 Connected as a Level Shift Amplifier

THE AD846 AS A HIGH-SPEED DAC BUFFER

The AD846 will enable the AD568 12-bit DAC to develop a 10V output step which settles to within 0.025 percent of its final value in about 100ns. This AD846/AD568 combination is shown in the circuit of Figure 48. Correct power supply decoupling is essential: a 2.2µF tantalum capacitor connected in parallel with a 0.1µF to 0.01µF ceramic disc capacitor is usually sufficient. These should be placed as close to the power supply pins as possible. Also, a ground plane should be employed; this ensures that there is a low impedance signal path to ground which allows the fastest possible output settling. In 12-bit systems with the AD846 operating at gains of 10 or less, inadequate supply decoupling can cause the output settling to degrade from 100ns to as much as 300ns, with a 10V output step applied.

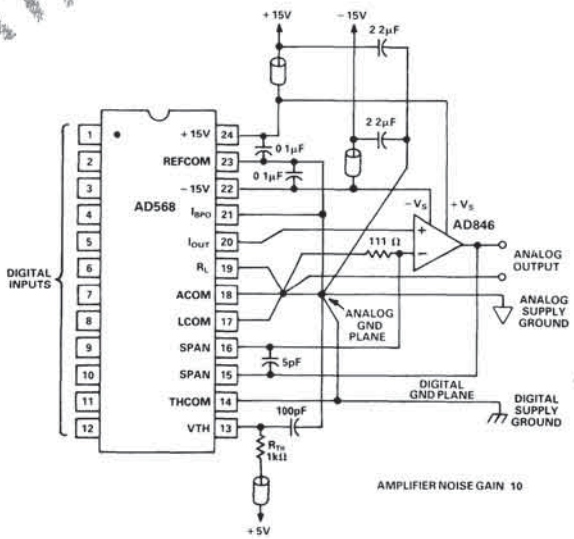


Figure 48. The AD846 Serving as a DAC Buffer

PRELIMINARY DATA

High-Speed, Low-Power Monolithic Op Amp

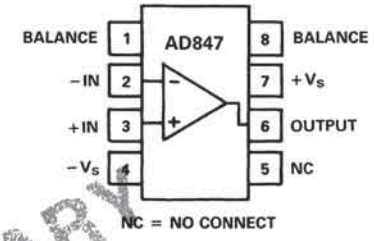
AD847

FEATURES
- 300V/μs Slew Rate
- 80ns Settling Time to 0.1%
- Unity Gain Stable
- 50MHz Gain Bandwidth Product with Only 5mA of Quiescent Current
- Stable Performance with Any Capacitive Load
- 0.5mV Offset Voltage
- Performance Specified for ±5V and ±15V Operation
- ±3V Output Swing into 150Ω Load
- 0.1dB Differential Gain
- 0.1dB Differential Phase
- Available in Plastic, Cerdip and SO Package
- Improved Replacement for National LM6161 Series

APPLICATIONS
- Unity Gain Buffer
- Video and R_F Amplification
- 8- and 10-Bit Data Acquisition Systems
- Cable Drivers

AD847 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP, Small Outline and Cerdip



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD847 is a high-speed, high-gain, low-power monolithic operational amplifier which achieves its performance by utilizing Analog Devices' unique junction isolated complementary bipolar process. It achieves its high speed while requiring only 5mA from the power supplies. This product is designed, specified and tested for ±5V to ±15V operation. For ±5V operation its output can swing ±3V into a 150Ω load. The AD847 is available in 8-pin plastic, cerdip and small outline packages. Options are available which operate over commercial, industrial and military temperature ranges.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±6V
Output Short-Circuit Duration	Indefinite
Internal Power Dissipation	
Plastic	TBD
Cerdip	1.6W
SOIC	TBD
Lead Temperature (Soldering 10sec)	+260°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	+150°C

PRODUCT HIGHLIGHTS

1. The AD847 high-speed monolithic operational amplifier achieves a remarkable 50MHz gain bandwidth product and 300V/μs slew rate while drawing only 5mA from the power supply lines.
2. The circuit is optimized and tested for ±5V and ±15V power supply voltages.
3. The AD847 is internally compensated for unity gain operation and remains stable when driving a capacitive load.
4. The amplifier can drive doubly terminated 75Ω coaxial transmission lines, making it ideal as a video and R_F cable driver.
5. The AD847 is one of a series of high-speed amplifiers featuring low standby power which utilize Analog Devices' proprietary complementary bipolar process. It is a direct replacement for National Semiconductor's LM 6161 series of amplifiers with greatly improved gain and dc performance.
6. The AD847 has applications in video and R_F amplification, as a buffer in high-speed 8- and 10-bit data acquisition systems and in optical memory servo systems. Its low power makes it ideal for high packaging density applications such as multiple pole active filters.

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD847J Min	AD847J Typ	AD847J Max	AD847A/S Min	AD847A/S Typ	AD847A/S Max	Units
INPUT CHARACTERISTICS								
Input Offset Voltage			0.5	**1**		0.5	**1**	mV
	T_{min} to T_{max}			2.5			**4**	mV
Input Offset Voltage Drift			15	30		15	30	μV/°C
INPUT BIAS CURRENT			2.5	**5**		2.5	**5**	μA
	T_{min} to T_{max}			6			**6**	μA
Input Offset Current			150	**300**		150	**300**	nA
	T_{min} to T_{max}			400			**400**	nA
Input Offset Current Drift			0.3			0.3		nA/°C
GAIN								
Open Loop	$V_S = \pm 5V$							
	$V_{OUT} = \pm 2.5V$							
	$R_L \geq 500\Omega$	**2**	3		**2**	3		V/mV
	$R_L = 150\Omega$		1			1		V/mV
	$V_S = \pm 15V$							
	$V_{OUT} = \pm 12V$							
	$R_L = 2k\Omega$	**3**			**3**	5		V/mV
	T_{min} to T_{max}	1.5			1.5			V/mV
Differential Gain			0.1			0.1		dB
Differential Phase			0.1			0.1		degree
DYNAMIC CHARACTERISTICS								
Gain Bandwidth Product	$f = 20MHz, V_S = \pm 15V$		50			50		MHz
	$V_S = \pm 5V$		35			35		MHz
Slew Rate	$V_S = \pm 15V$	225	300		225	300		V/μs
	$V_S = \pm 5V$		200			200		V/μs
Settling Time to 0.1%	$V_S = \pm 5V$		65			65		ns
	−2.5V to +2.5V							
	Step, $A_V = -1$							
	$R_L = 2k\Omega$							
	$V_S = \pm 15V$							
	10V Step		80			80		ns
Phase Margin	$V_S = \pm 15V$		50			50		degree
	$C_L = 10pF$							
	$R_L = 2k\Omega$							
INPUT RESISTANCE	Differential		300			300		kΩ
Input Capacitance	$f = 50MHz$		1.5			1.5		pF
COMMON-MODE VOLTAGE RANGE	$V_S = \pm 5V$		+4.3			+4.3		V
			−3.4			−3.4		V
	$V_S = \pm 15V$		+14.3			+14.3		V
			−13.4			−13.4		V
Common-Mode Rejection	$V_S = \pm 5V$							
	$V_{CM} = \pm 2.5V$	**86**	95		**86**	95		dB
	$V_S = \pm 15V$							
	$V_{CM} = \pm 12V$	**86**	95		**86**	95		dB
	T_{min} to T_{max}	80			80			dB
Power Supply Rejection Ratio		**80**	90		**80**	90		dB
Input Noise Voltage	$f = 10kHz$		15			15		$nV/\sqrt{Hz}$
Input Noise Current	$f = 10kHz$		1.5			1.5		$pA/\sqrt{Hz}$
OUTPUT CHARACTERISTICS								
Output Voltage Swing	$V_S = \pm 5V$							
	$R_L \geq 2k\Omega$	**±3.6**			**±3.6**			V
	$R_L = 150\Omega$	**±2.5**			**±2.5**			V
	$V_S = \pm 15V$							
	$R_L = 2k\Omega$	**±12**			**±12**			V
	$R_L = 500\Omega$	**±10**			**±10**			V
Short-Circuit Current			35			35		mA
POWER SUPPLY								
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			5	**6.0**		5	**6.0**	mA
	T_{min} to T_{max}			6.9			**7.2**	mA
TEMPERATURE RANGE								
Rated Performance								
Commercial (0 to +70°C)		AD847JN		AD847JR				
Military (−55°C to +125°C)						AD847SQ		
PACKAGE OPTIONS[1]								
Plastic (N-8)			AD847JN					
Cerdip (Q-8)						AD847AQ, AD847SQ		
SOIC (R-8)			AD847JR					

NOTE
[1]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications marked in **boldface** are tested on all production units at final electrical test.

PRELIMINARY TECHNICAL DATA

High-Speed, Low-Power Monolithic Op Amp

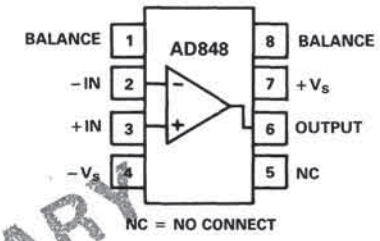
AD848

FEATURES
- 300V/μs Slew Rate
- 80ns Settling Time to 0.1%
- 175MHz Gain Bandwidth Product with Only 5mA of Quiescent Current
- Stable Performance with Any Capacitive Load
- Stable Operation with a Minimum Gain of 5
- 0.5mV Offset Voltage
- Performance Specified for ±5V and ±15V Operation
- ±3V Output Swing into 150Ω Load
- 0.1dB Differential Gain
- 0.1dB Differential Phase
- Available in Plastic, Cerdip and SO Package
- Improved Replacement for National LM6164 Series

APPLICATIONS
- High Bandwidth, High Gain Communication Systems
- Video and R_F Amplification
- 8- and 10-Bit Data Acquisition Systems
- Cable Drivers

AD848 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP,
Small Outline and Cerdip



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD848 is a high-speed, high-gain, low-power monolithic operational amplifier which achieves its performance by utilizing Analog Devices' unique junction isolated complementary bipolar process. It achieves its high speed while only requiring 5mA from the power supplies. This product is designed, specified and tested for ±5V to ±15V operation. For ±5V operation its output can swing ±3V into a 150Ω load. The AD848 is available in 8-pin plastic, cerdip and small outline packages. Options are available which operate over commercial, industrial and military temperature ranges.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage[2]	±6V
Output Short-Circuit Duration	Indefinite
Internal Power Dissipation	
Plastic	TBD
Cerdip	1.6W
SO	TBD
Lead Temperature (Soldering 10sec)	+260°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	+150°C

PRODUCT HIGHLIGHTS

1. The AD848 high-speed monolithic operational amplifier achieves a remarkable 175MHz gain bandwidth product and 300V/μs slew rate while drawing only 5mA from the power supply lines.
2. The circuit is optimized and tested for ±5V and ±15V power supply voltages.
3. The AD848 is internally compensated for operation with a gain of 5 and remains stable when driving a capacitive load.
4. The amplifier can drive doubly terminated 75Ω coaxial transmission lines, making it ideal as a video and R_F cable driver.
5. The AD848 is one of a series of high-speed amplifiers featuring low standby power which utilize Analog Devices' proprietary complementary bipolar process. It is a direct replacement for National Semiconductor's LM 6164 series of amplifiers with greatly improved gain and dc performance.
6. The AD848 has applications in video and R_F amplification, as a gain block in high-speed 8- and 10-bit data acquisition systems and in optical memory servo systems. Its low power makes it ideal for high packaging density applications such as multiple pole active filters.

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD848J Min	AD848J Typ	AD848J Max	AD848A/S Min	AD848A/S Typ	AD848A/S Max	Units
INPUT CHARACTERISTICS								
Input Offset Voltage			0.5	**1**		0.5	**1**	mV
	T_{min} to T_{max}			1.5			**2**	mV
Input Offset Voltage Drift			5	10		5	10	µV/°C
INPUT BIAS CURRENT			**2.5**	**5**		2.5	**5**	µA
	T_{min} to T_{max}			6			6	µA
Input Offset Current			150	**300**		150	**300**	nA
	T_{min} to T_{max}			400			**400**	nA
Input Offset Current Drift			0.3			0.3		nA/°C
GAIN								
Open Loop	$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	**10**	15		**10**	15		V/mV
	$R_L = 150\Omega$		5			5		V/mV
	$V_S = \pm 15V$, $V_{OUT} = \pm 12V$, $R_L = 2k\Omega$	**20**	30		**20**	30		V/mV
	T_{min} to T_{max}	10			**10**			V/mV
Differential Gain			0.1			0.1		dB
Differential Phase			0.1			0.1		degree
DYNAMIC CHARACTERISTICS								
Gain Bandwidth Product	$f = 20MHz$, $V_S = \pm 15V$		175			175		MHz
	$V_S = \pm 5V$		120			120		MHz
Slew Rate	$V_S = \pm 15V$	225	300		225	300		V/µs
	$V_S = \pm 5V$		200			200		V/µs
Settling Time to 0.1%	$V_S = \pm 5V$, −2.5V to +2.5V, $A_V = -5$, $R_L = 2k\Omega$		65			65		ns
	$V_S = \pm 15V$, 10V Step		80			80		ns
Phase Margin	$V_S = \pm 15V$, $C_L = 10pF$, $R_L = 2k\Omega$		50			50		degree
INPUT RESISTANCE	Differential		1,500			1,500		kΩ
Input Capacitance	f = 50MHz		1.5			1.5		pF
COMMON-MODE VOLTAGE RANGE	$V_S = \pm 5V$		+4.3			+4.3		V
			−3.4			−3.4		V
	$V_S = \pm 15V$		+14.3			+14.3		V
			−13.4			−13.4		V
Common-Mode Rejection	$V_S = \pm 5V$		105			105		dB
	$V_{CM} = \pm 2.5V$	**90**			**90**			
	$V_S = \pm 15V$		105			105		dB
	$V_{CM} = \pm 12V$	**90**			**90**			
	T_{min} to T_{max}	**86**			**86**			dB
Power Supply Rejection Ratio		**90**	100		**90**	100		dB
Input Noise Voltage	f = 10kHz		4			4		nV/√Hz
Input Noise Current	f = 10kHz		1.5			1.5		pA/√Hz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	$V_S = \pm 5V$, $R_L \geq 500\Omega$	**±3.6**			**±3.6**			V
	$R_L = 150\Omega$	**±2.5**			**±2.5**			V
	$V_S = \pm 15V$, $R_L = 2k\Omega$	**±12**			**±12**			V
	$R_L = 500\Omega$	**±10**			**±10**			V
Short-Circuit Current			35			35		mA
POWER SUPPLY								
Operating Voltage Range		**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			5	**6.0**		5	**6.0**	mA
	T_{min} to T_{max}			6.9			7.2	mA
TEMPERATURE RANGE								
Rated Performance								
Commercial (0 to +70°C)		AD848JN		AD848JR				
Industrial (+40°C to +85°C)						AD848SQ		
Military (−55°C to +125°C)						AD848SQ		
PACKAGE OPTIONS[1]								
Plastic (N-8)			AD848JN					
Cerdip (Q-8)						AD848AQ, AD848SQ		
SOIC (R-8)			AD848JR					

NOTE

[1]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications marked in **boldface** are tested on all production units at final electrical test.

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

High-Speed, Low-Power Monolithic Op Amp

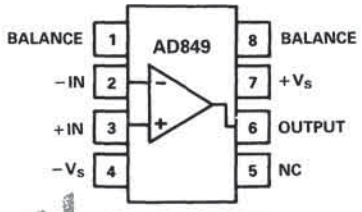
AD849

FEATURES
- 300V/μs Slew Rate
- 80ns Settling Time to 0.1%
- 750MHz Gain Bandwidth Product with Only 5mA of Quiescent Current
- Stable Performance with Any Capacitive Load
- Stable Operation with a Minimum Gain of 25
- 0.5mV Offset Voltage
- Performance Specified for ±5V and ±15V Operation
- ±3V Output Swing into 150Ω Load
- 0.1dB Differential Gain
- 0.1dB Differential Phase
- Available in Plastic, Cerdip and SO Package
- Improved Replacement for National LM6165 Series

APPLICATIONS
- High Gain, High Bandwidth Communication Systems
- Video and R_F Amplification
- 8- and 10-Bit Data Acquisition Systems
- Cable Drivers

AD849 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP, Small Outline and Cerdip



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD849 is a high-speed, high-gain, low-power monolithic operational amplifier which achieves its performance by utilizing Analog Devices' unique junction isolated complementary bipolar process. It achieves its high speed while requiring only 5mA from the power supplies. This product is designed, specified and tested for ±5V to ±15V operation. For ±5V operation its output can swing ±3V into a 150Ω load. The AD849 is available in 8-pin plastic, cerdip and small outline packages. Options are available which operate over commercial, industrial and military temperature ranges.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±6V
Output Short-Circuit Duration	Indefinite
Internal Power Dissipation	
Plastic	TBD
Cerdip	1.6W
SOIC	TBD
Lead Temperature (Soldering 10sec)	+260°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	+150°C

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. The AD849 high-speed monolithic operational amplifier achieves a remarkable 750MHz gain bandwidth product and 300V/μs slew rate while drawing only 5mA from the power supply lines.
2. The circuit is optimized and tested for ±5V and ±15V power supply voltages.
3. The AD849 is internally compensated for operation with a gain of 25 and remains stable when driving a capacitive load.
4. The amplifier can drive doubly terminated 75Ω coaxial transmission lines, making it ideal as a video and R_F cable driver.
5. The AD849 is one of a series of high-speed amplifiers featuring low standby power which utilize Analog Devices' proprietary complementary bipolar process. It is a direct replacement for National Semiconductor's LM 6165 series of amplifiers with greatly improved gain and dc performance.
6. The AD849 has applications in video and R_F amplification, as a gain block in high-speed 8- and 10-bit data acquisition systems and in optical memory servo systems. Its low power makes it ideal for high packaging density applications such as multiple pole active filters.

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD849J Min	AD849J Typ	AD849J Max	AD849A/S Min	AD849A/S Typ	AD849A/S Max	Units
INPUT CHARACTERISTICS								
Input Offset Voltage			0.5	**1**		0 5	**1**	mV
	T_{min} to T_{max}			**1.5**			**2**	mV
Input Offset Voltage Drift			1	5		1	5	µV/°C
INPUT BIAS CURRENT			**2.5**	**5**		2.5	**5**	µA
	T_{min} to T_{max}			6			**6**	µA
Input Offset Current			150	**300**		150	**300**	nA
	T_{min} to T_{max}			400			**400**	nA
Input Offset Current Drift			0 3			0 3		nA/°C
GAIN								
Open Loop	V_S = ±5V							
	V_{OUT} = ±2.5V							
	R_L = 500Ω	**30**	**45**		**30**	**45**		V/mV
	R_L = 150Ω		20			20		V/mV
	V_S = ±15V							
	V_{OUT} = ±12V							
	R_L = 2kΩ	**50**	80		**50**	80		V/mV
	T_{min} to T_{max}	25			**25**			V/mV
Differential Gain			0.1			0.1		dB
Differential Phase			0.1			0.1		degree
DYNAMIC CHARACTERISTICS								
Gain Bandwidth Product	f = 20MHz, V_S = ±15V		750			750		MHz
	V_S = ±5V		520			520		MHz
Slew Rate	V_S = ±15V	225	300		225	300		V/µs
	V_S = ±5V		200			200		V/µs
Settling Time to 0 1%	V_S = ±5V		65			65		ns
	−2.5V to +2 5V							
	A_V = −25							
	R_L = 2kΩ							
	V_S = ±15V							
	10V Step		80			80		ns
Phase Margin	V_S = ±15V		50			50		degree
	C_L = 10pF							
	R_L = 2kΩ							
INPUT RESISTANCE	Differential		15			15		kΩ
Input Capacitance	f = 50MHz		1.5			1.5		pF
COMMON-MODE VOLTAGE RANGE	V_S = ±5V		+4.3			+4 3		V
			−3.4			−3.4		V
	V_S = ±15V		+14.3			+14.3		V
			−13.4			−13 4		V
Common-Mode Rejection	V_S = ±5V	**100**	115		**100**	115		dB
	V_{CM} = ±2.5V							
	V_S = ±15V	**100**	115		**100**	115		dB
	V_{CM} = ±12V							
	T_{min} to T_{max}	95			**95**			dB
Power Supply Rejection Ratio		**100**	110		**100**	110		dB
Input Noise Voltage	f = 10kHz		4			4		nV/√Hz
Input Noise Current	f = 10kHz		1.5			1.5		pA/√Hz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	V_S = ±5V							
	R_L ≥ 500Ω	**±3.6**			**±3.6**			V
	R_L = 150Ω	**±2.5**			**±2.5**			V
	V_S = ±15V							
	R_L = 2kΩ	**±12**			**±12**			V
	R_L = 500Ω	**±10**			**±10**			V
Short-Circuit Current			35			35		mA
POWER SUPPLY								
Operating Voltage Range		**±4.5**		**±18**	±4.5		**±18**	V
Quiescent Current			5	**6.0**		5	**6.0**	mA
	T_{min} to T_{max}			6.9			**7.2**	mA
TEMPERATURE RANGE								
Rated Performance								
Commercial (0 to +70°C)		AD849JN		AD849JR				
Industrial (−40°C to +85°C)						AD849AQ		
Military (−55°C to +125°C)						AD849SQ		
PACKAGE OPTIONS[1]								
Plastic (N-8)			AD849JN					
Cerdip (Q-8)						AD849AQ, AD849SQ		
SOIC (R-8)			AD849JR					

NOTE

[1]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications marked in **boldface** are tested on all production units at final electrical test

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

Ultrahigh-Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

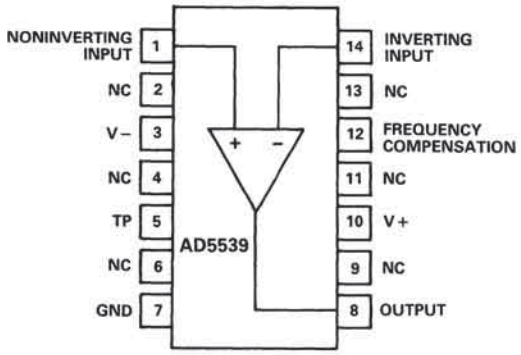
AC PERFORMANCE

- **Gain Bandwidth Product: 1.4GHz typ**
- **Unity Gain Bandwidth: 220MHz typ**
- **High Slew Rate: 600V/μs typ**
- **Full Power Response: 82MHz typ**
- **Open-Loop Gain: 47dB min, 52dB typ**

DC PERFORMANCE

- **All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages**
- **V_{OS}: 5mV max Over Full Temperature Range (AD5539J)**
- **I_B: 20μA max (AD5539J)**
- **CMRR: 70dB min, 85dB typ**
- **PSRR: 100μV/V typ**
- **MIL-STD-883B Parts Available**

AD5539 CONNECTION DIAGRAM
Plastic DIP (N) Package
or Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD5539 is an ultrahigh-frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low-cost solutions to many otherwise complex and expensive high-frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package.

PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50Ω and 75Ω loads directly.
3. Input voltage noise is less than $4nV\sqrt{Hz}$.
4. Low-cost RF and Video speed performance.
5. ±2 volt output range into a 150Ω load.
6. Low cost.
7. Chips available.

SPECIFICATIONS (@ +25°C and V_S = ±8V dc, unless otherwise noted)

Model	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	5		2	3	mV
T_{min} to T_{max}			6			5	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	2		0.1	1	μA
T_{min} to T_{max}			5			3	μA
INPUT BIAS CURRENT							
Initial[2]							
$V_{CM} = 0$		6	20		6	13	μA
Either Input							
T_{min} to T_{max}			40			25	μA
FREQUENCY RESPONSE							
$R_L = 150\Omega$[3]							
Small Signal Bandwidth		220			220		MHz
$A_{CL} = 2$[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26dB							
Full Power Response							
$A_{CL} = 2$[4]		68			68		MHz
$A_{CL} = 7$		82			82		MHz
$A_{CL} = 20$		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/μs
Large Signal Propogation Delay		4			4		ns
Total Harmonic Distortion							
$R_L = \infty$		0.010			0.010		%
$R_L = 100\Omega$[3]		0.016			0.016		%
V_{OUT} = 2V p-p							
$A_{CL} = 7$, f = 1kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f<10MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common-Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common-Mode Rejection Ratio							
$\Delta V_{CM} = 1.7V$							
$R_S = 100\Omega$	70	85		70	85		dB
T_{min} to T_{max}	60			60			dB
INPUT VOLTAGE NOISE							
Wideband rms Noise (RTI)		5			5		μV
BW = 5MHz; $R_S = 50\Omega$							
Spot Noise		4			4		$nV/\sqrt{Hz}$
F = 1kHz; $R_S = 50\Omega$							
OPEN LOOP GAIN							
$V_O = +2.3V, -1.7V$							
$R_L = 150\Omega$[3]	47	52	58	47	52	58	dB
$R_L = 2k\Omega$	47		58	48		57	dB
T_{min} to T_{max} – $R_L = 2k\Omega$	43		63	46		60	dB

Model	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
OUTPUT CHARACTERISTICS							
Positive Output Swing							
$R_L = 150\Omega$[3]	+2.3	+2.8		+2.3	+2.8		V
$R_L = 2k\Omega$	+2.3	+3.3		+2.5	+3.3		V
T_{min} to T_{max} with							
$R_L = 2k\Omega$	+2.3			+2.3			V
Negative Output Swing							
$R_L = 150\Omega$[3]		−2.2	−1.7		−2.2	−1.7	V
$R_L = 2k\Omega$		−2.9	−1.7		−2.9	−2.0	V
T_{min} to T_{max} with							
$R_L = 2k\Omega$			−1.5			−1.5	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	±4.5		+10	±4.5		+10	V
Quiescent Current							
Initial $I_{CC}+$		14	18		14	17	mA
T_{min} to T_{max}			20			18	mA
Initial $I_{CC}-$		11	15		11	14	mA
T_{min} to T_{max}			17			15	mA
PSRR							
Initial		100	1000		100	1000	μV/V
T_{min} to T_{max}			2000			2000	μV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0 to +70°C)	AD5539JN, AD5539JQ						
Military (−55°C to +125°C)				AD5539SQ			
PACKAGE OPTIONS[6]							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ			

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$.
[3]$R_X = 470\Omega$ to $-V_S$.
[4]Externally compensated.
[5]Defined as voltage between inputs, such that neither exceeds +2.5V, −5.0V from ground.
[6]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

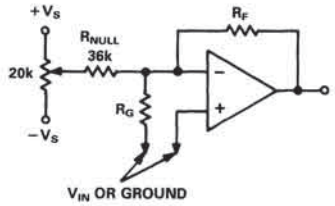
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±10V
Internal Power Dissipation	550mW
Input Voltage	+2.5V, −5.0V
Differential Input Voltage	0.25V
Storage Temperature Range Q	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD5539JN	0 to +70°C
AD5539JQ	0 to +70°C
AD5539SQ	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OFFSET NULL CONFIGURATION



OUTPUT NULL RANGE ≈ $+V_S\left(\frac{R_F}{R_{NULL}}\right)$ TO $-V_S\left(\frac{R_F}{R_{NULL}}\right)$

OFFSET NULL CONFIGURATION

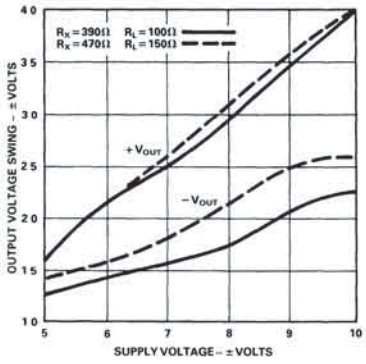


Figure 1. Output Voltage Swing vs. Supply Voltage

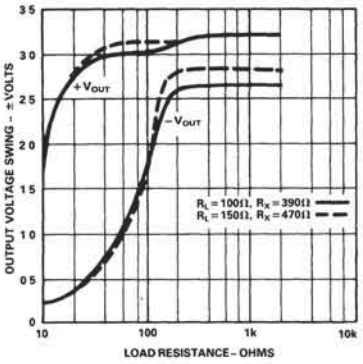


Figure 2. Output Voltage Swing vs. Resistive Load

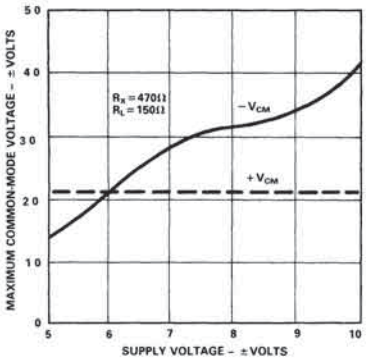


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

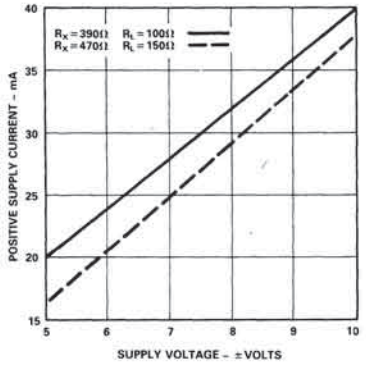


Figure 4. Positive Supply Current vs. Supply Voltage

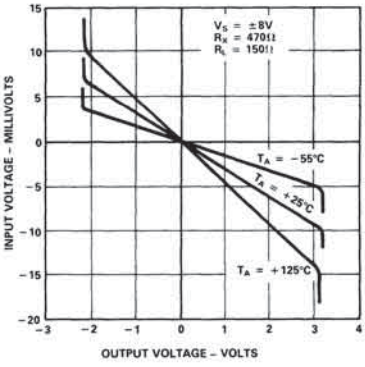


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

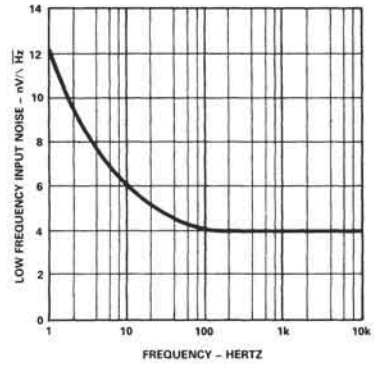


Figure 6. Low Frequency Input Noise vs. Frequency

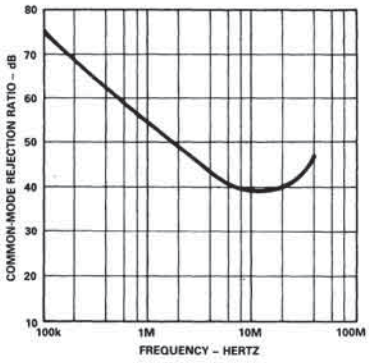


Figure 7. Common-Mode Rejection Ratio vs. Frequency

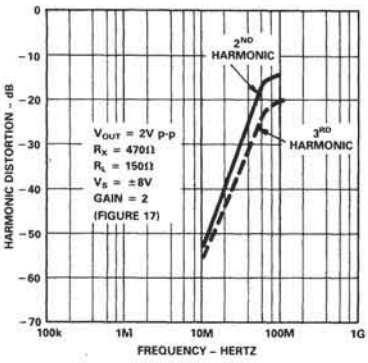


Figure 8. Harmonic Distortion vs. Frequency – Low Gain

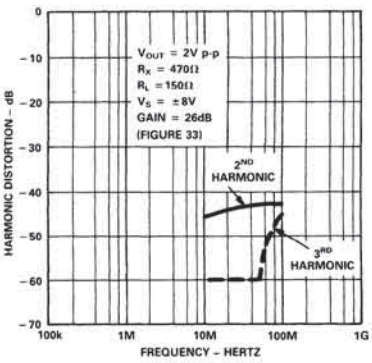


Figure 9. Harmonic Distortion vs. Frequency – High Gain

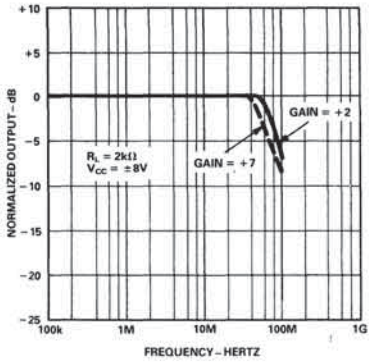


Figure 10. Full Power Response

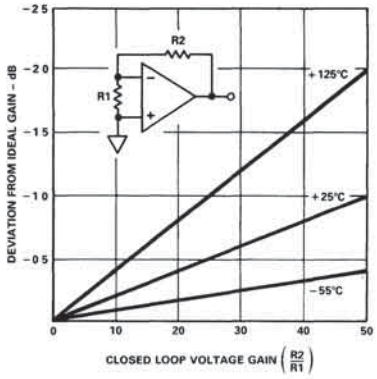


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

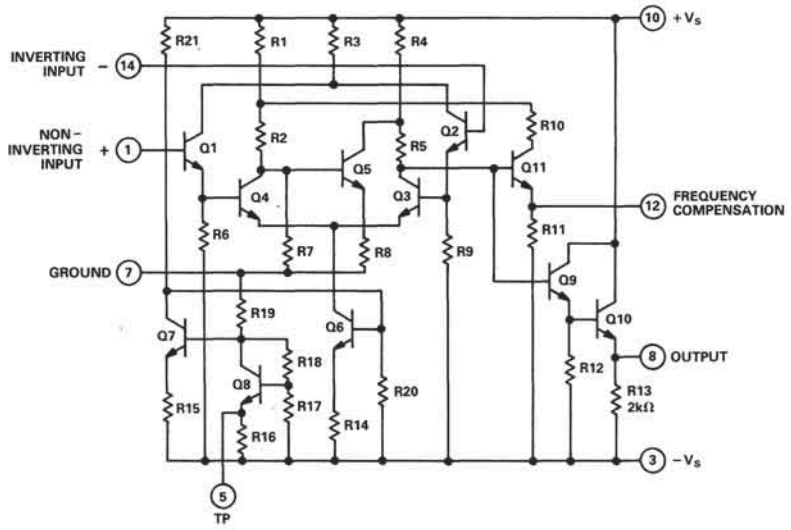


Figure 12. AD5539 Circuit

FUNCTIONAL DESCRIPTION

The AD5539 is a two-stage, very-high-frequency amplifier. Darlington input transistors Q1, Q4 – Q2, Q3 form the first stage – a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is then summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned, via a small resistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a Darlington voltage follower with a resistive pull-down. The bias section, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

SOME GENERAL PRINCIPLES OF HIGH-FREQUENCY CIRCUIT DESIGN

In designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved, some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low-profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50Ω line for telecommunications purposes and 75Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6dB), adequate for many applications.

All of the circuits here were built and tested in a 50Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small-signal frequency response as those shown in this data sheet.

APPLYING THE AD5539

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding −3dB bandwidths up to 390MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation), so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44MHz, independent of signal gain.

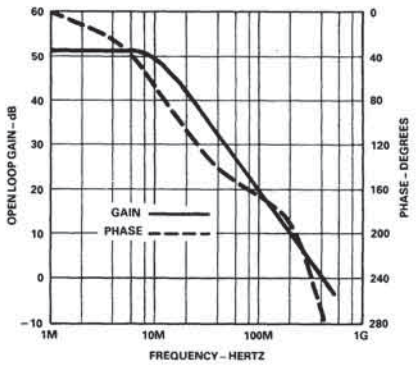


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10MHz (see Figure 13). At frequencies beyond 100MHz, phase shift increases such that the output lags the input by 180° – well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539 when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10dB of peaking at 150MHz.

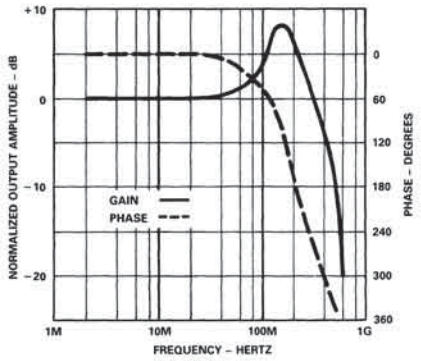


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high-frequency response. The stray capacitance between the amplifier summing junction and ground, C_X, represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring R_{LAG} and C_{LAG} for now): the feedback network, consisting of R2 and C_{LEAD}, has a pole frequency equal to:

$$F_A = \frac{1}{2\pi\,(C_{LEAD} + C_X)\,(R1 \parallel R2)} \qquad \text{Equation 1}$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi\,(R1 \times C_{LEAD})} \qquad \text{Equation 2}$$

Usually, frequency F_A is made equal to F_B; that is, $(R1C_X) = (R2\,C_{LEAD})$, in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency, F_A, will lie above the unity gain crossover frequency (440MHz), then the optimum location of F_B will be near the crossover

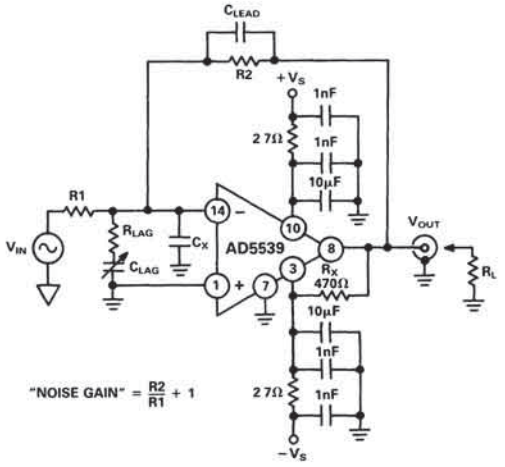


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

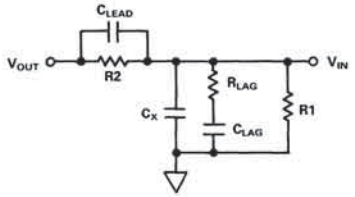


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

frequency. Both of these circuit techniques add a large amount of leading phase shift at the crossover frequency, greatly aiding stability.

The lag network (R_{LAG}, C_{LAG}) increases the feedback attenuation, i.e.: the amplifier operates at a higher noise gain, above some frequency, typically one tenth of the crossover frequency. As an example, to achieve a noise gain of 5 at frequencies above 44MHz, for the circuit of Figure 15, would require a network of:

$$R_{LAG} = \frac{R1}{(4R1/R2) - 1} \qquad \text{Equation 3}$$

and . . .

$$C_{LAG} = \frac{1}{2\pi\, R_{LAG}\, (44 \times 10^6)} \qquad \text{Equation 4}$$

It is worth noting that an R_{LAG} resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

SOME PRACTICAL CIRCUITS

The preceding general principles may now be applied to some actual circuits.

A General Purpose Inverter Circuit

Figure 17 is a general purpose inverter circuit operating at a gain of −2.

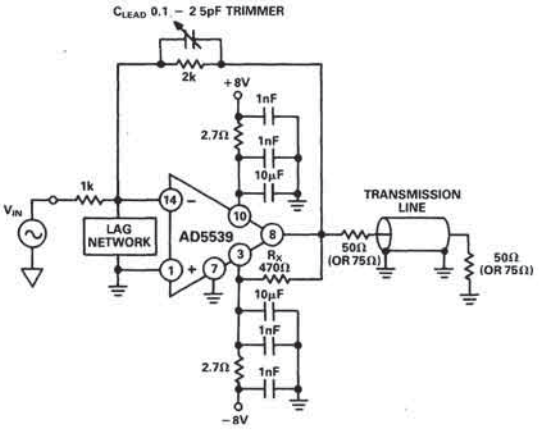


Figure 17. A General Purpose Inverter Circuit

For this circuit, the total capacitance at the inverting input is approximately 3pF; therefore, C_{LEAD} from Equations 1 & 2 needs to be approximately 1.5pF. As shown in Figure 17, a small trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within ±0.5dB to 170MHz and the −3dB bandwidth is 200MHz.

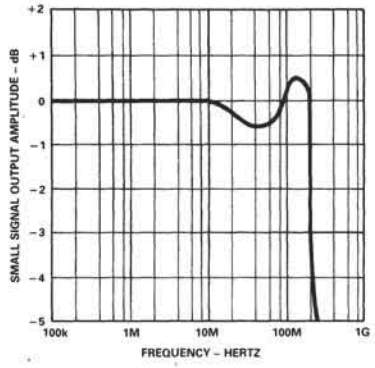


Figure 18. Response of the (Figure 17) Inverter Circuit Without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor C_{LEAD} adjustable; in some cases, C_{LAG} must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

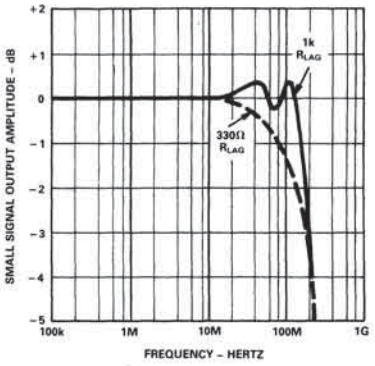


Figure 19. Response of the (Figure 17) Inverter Circuit With an R_{LAG} Compensation Network Employed

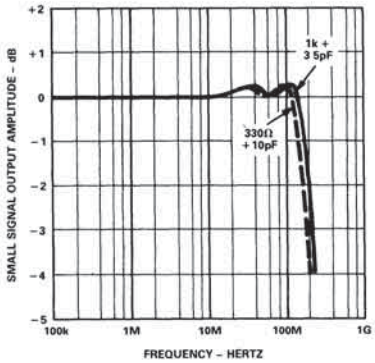


Figure 20. Response of the (Figure 17) Inverter Circuit With an R_{LAG} and a C_{LAG} Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with C_{LEAD} = 1.5pF, R_{LAG} = 330Ω and C_{LAG} = 3.5pF.

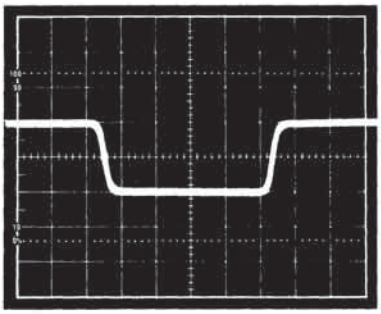


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit. Vertical Scale: 50mV/div; Horizontal Scale: 5ns/div.

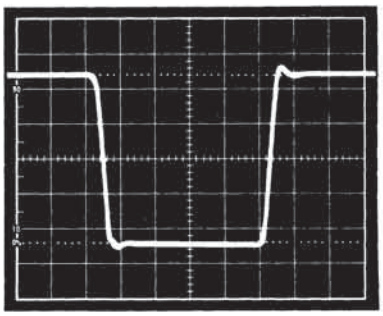


Figure 22. Large Signal Response of the (Figure 17) Inverter Circuit. Vertical Scale: 200mV/div, Horizontal Scale: 5ns/div.

A C_{LEAD} capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$(-3dB\ frequency = \frac{1}{2\pi R2C_{LEAD}})$.

If this option is selected, it is recommended that a C_{LEAD} be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350MHz) which would otherwise occur when using the circuit of Figure 17 with a C_{LEAD} of more than about 2pF.

Figure 24 shows the response of the circuit of Figure 23 for each connection of C_{LEAD}. Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting C_{LEAD} directly to the output, as was done in Figure 17.

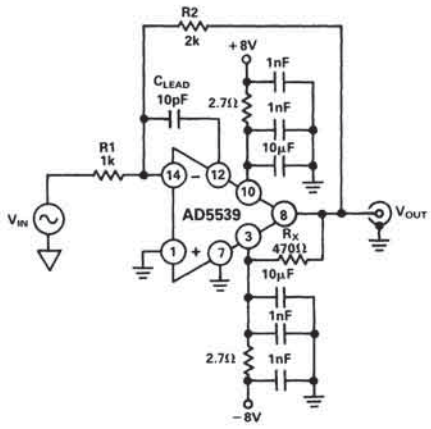


Figure 23. A Gain of 2 Inverter Circuit with the C_{LEAD} Capacitor Connected to Pin 12

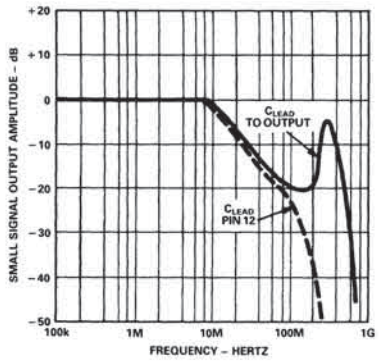


Figure 24. Response of the Circuit of Figure 23 with C_{LEAD} = 10pF

A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with C_{LEAD} connected normally (across the feedback resistor – Figure 25) will require a source resistance of 200Ω or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest −3dB frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

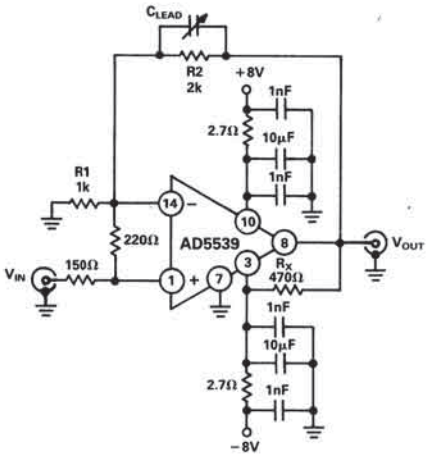


Figure 25. A Gain of 3 Follower with Both Lead and Lag Compensation

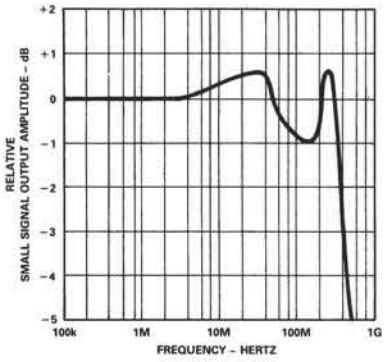


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the midband and low-frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

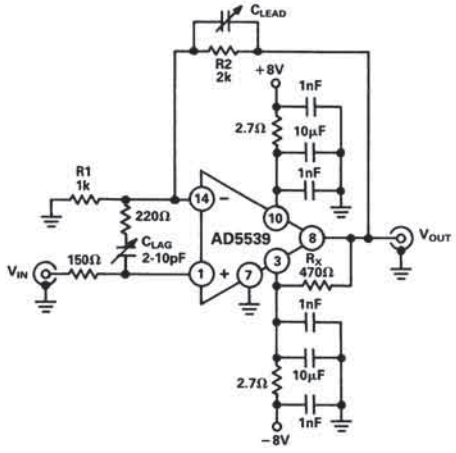


Figure 27. A Gain of 3 Follower Circuit with both C_{LEAD} and R_{LAG} Compensation

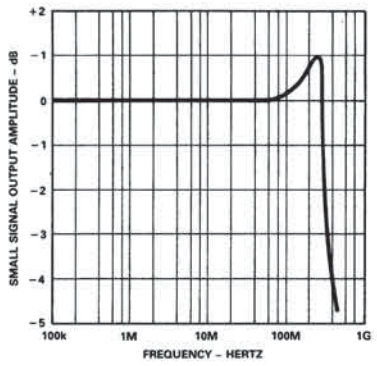


Figure 28. Response of the Gain of 3 Follower with C_{LEAD}, C_{LAG} and R_{LAG}

These same principles may be applied when capacitor C_{LEAD} is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of R_{LAG}. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the

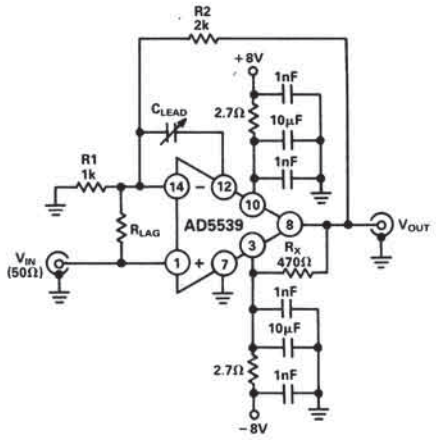


Figure 29. A Gain of 3 Follower Circuit with C_{LEAD} Compensation Connected to Pin 12

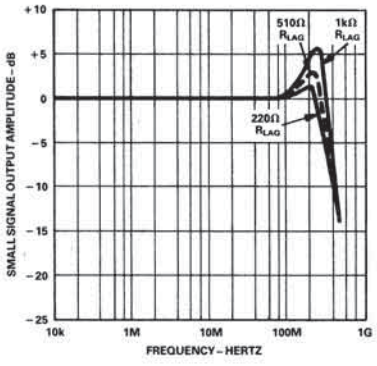


Figure 30. Response of the Gain of 3 Follower Circuit with C_{LEAD} Connected to Pin 12

value of R_{LAG}, the higher the noise gain). For example, with a 220Ω R_{LAG} and a 50Ω source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

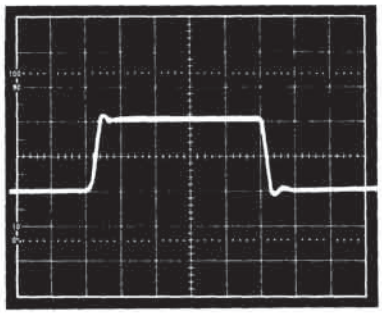


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12. Vertical Scale: 50mV/div.; Horizontal Scale: 5ns/div.

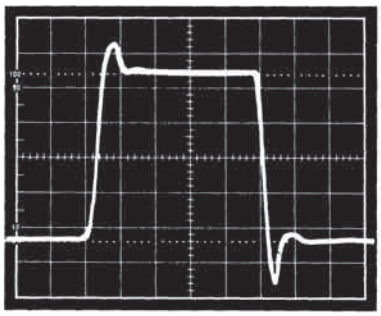


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12. Vertical Scale: 200mV/div; Horizontal Scale: 5ns/div.

A Video Amplifier Circuit with 20dB Gain (Terminated)
High gain applications (14dB and up) require only a small lead capacitance to obtain flat response. The 26dB (20dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5–1pF lead capacitance. Again, a small C_{LEAD} can be connected, either to the output or to Pin 12 with very little difference in response.

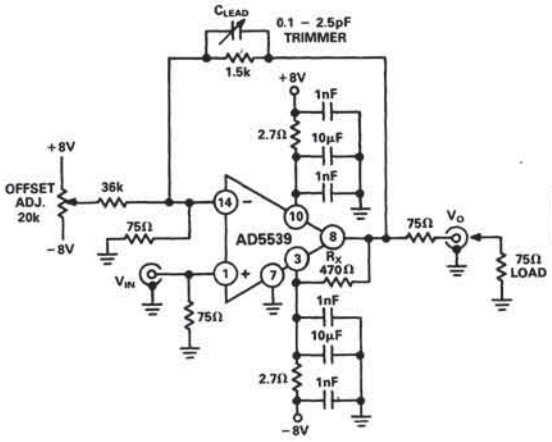


Figure 33. A 20dB Gain Video Amplifier for 75Ω Systems

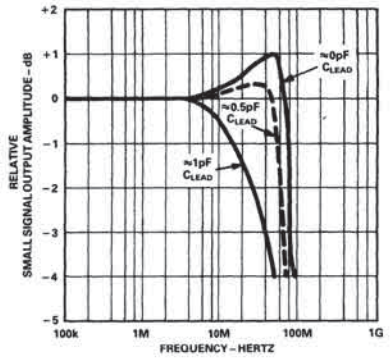


Figure 34. Response of the 20dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35, 36, 37 and 38 show the standard six-step modulated staircase waveform. The amplifier's response is plotted first by a vector scope, and then the magnified differential gain/differential phase target is plotted, first without the 20dB amplifier, then with the amplifier in the system.

Figures 37 and 38 have been expanded to provide the necessary resolution to show a differential gain of less than 0.5% and a differential phase less than 0.1°.

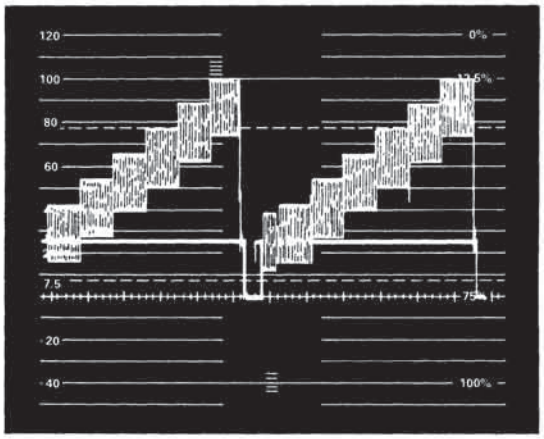


Figure 35. A Six-Step Modulated Staircase Waveform of the 20dB Video Amplifier Circuit

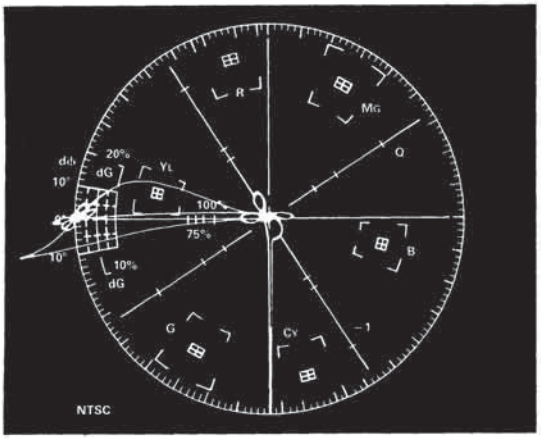


Figure 36. The 20dB Video Amplifier's Response Plotted on a Vector Scope

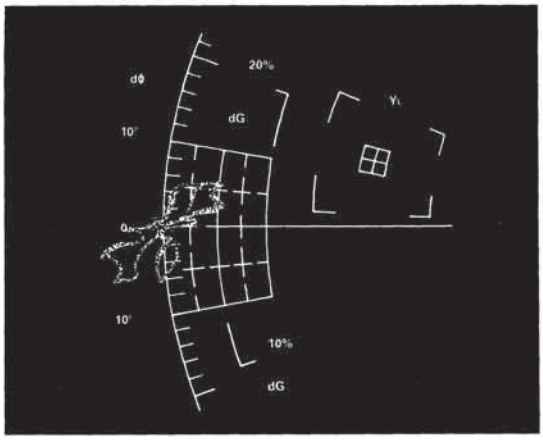


Figure 37. Differential Gain/Differential Phase Target with Generator Output Connected Directly to Vector Scope Input

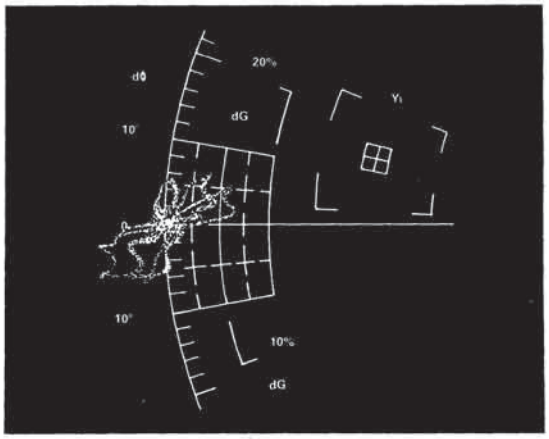


Figure 38. Differential Gain/Differential Phase Target with Generator Output Connected to Video Amplifier Input – Amplifier is Output Connected to Vector Scope Input

MEASURING AD5539 SETTLING TIME

Measuring the very rapid settling times associated with AD5539 can be a real problem for the designer; proper component layout must be used and appropriate test equipment selected. In addition, both cable dispersion (a function of cable losses) and the quality of termination (SWR) directly affect the measurement. The circuit of Figure 39 was used to make a "brute force" AD5539 settling time measurement. The fixture containing the circuit was connected directly – using a male BNC connector (but no cable) – onto the front of a 50Ω input oscilloscope preamp. A digital mainframe was then used to capture, average, and expand the error signal. Most of the small-scale waveform aberrations shown on the figure were caused by the oscilloscope itself, especially the glitch at 15ns. The pulse source used for this measurement was an EH–SPG2000 pulse generator set for a 1ns rise-time; it was coupled directly to the circuit using 18" of microwave 50Ω hard line.

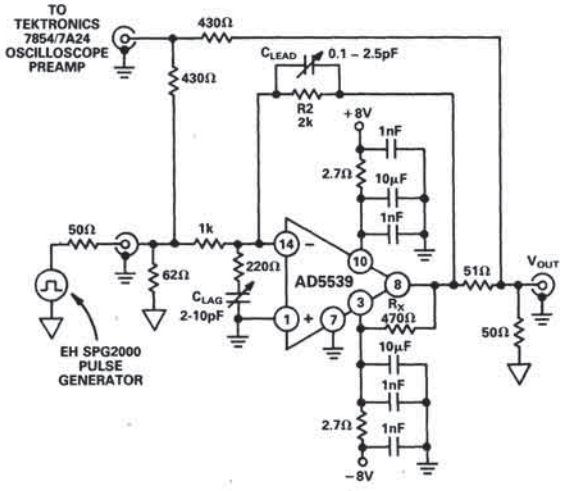


Figure 39. AD5539 Settling Time Test Circuit

APPLICATIONS SUMMARY CHART

	R1	R2[1]	R_{LAG}	C_{LAG}[2]	C_{LEAD}[2]	GAIN	GAIN FLATNESS (TRIMMED)	−3dB BANDWIDTH
Gain = −1 to −5 Circuit of Fig 17	$\frac{R2}{G}$	2k	$\leq \frac{R1}{4\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G}$	−2	±0.2dB	200MHz
Gain = −1 to −5 Circuit of Fig. 23	$\frac{R2}{G}$	2k	$\leq \frac{R1}{4\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G}$	−2	±1dB	180MHz
Gain = +2 to +5[3] Circuit of Fig 27	$\frac{R2}{G-1}$	2k	$\leq \frac{R1}{10\frac{R1}{R2}-1}$	$\geq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G-1}$	+3	±1dB	390MHz
Gain = +2 to +5[4] Circuit of Fig. 29	$\frac{R2}{G-1}$	2k	$\leq \frac{R1}{10\frac{R1}{R2}-1}$	NA	$\approx \frac{3pF}{G-1}$	+3	±0.5dB	340MHz
Gain < −5	$\frac{R2}{G}$	1.5k	NA	NA	Trimmer[5]	−20	±0.2dB	80MHz
Gain > +5	$\frac{R}{G-1}$	1.5k	NA	NA	Trimmer[5]	+20	±0.2dB	80MHz

G = Gain NA = Not Applicable
[1]Values given for specific results summarized here – applications can be adapted for values different than those specified
[2]It is recommended that C_{LEAD} and C_{LAG} be trimmers covering a range that includes the computed value above
[3]$R_{SOURCE} \geq 200\Omega$
[4]$R_{SOURCE} \geq 50\Omega$.
[5]Use Voltronics CPA20 1–2.5pF Teflon Trimmer Capacitor (or equivalent)

The photos of Figures 40 and 41 demonstrate how the AD5539 easily settles to 1% (1mV) in less than 12ns; settling to 0.1% (100μV) requires less than 25ns.

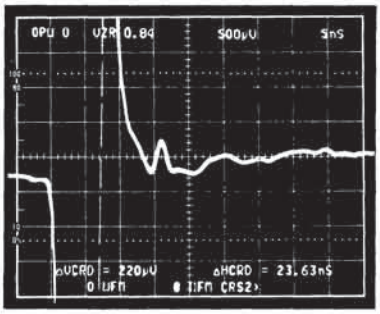


Figure 40. Error Signal from AD5539 Settling Time Test Circuit – Falling Edge. Vertical Scale: 5ns/div.; Horizontal Scale: 500μV/div.

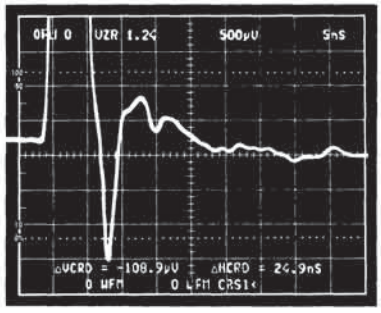


Figure 41. Error Signal from AD5539 Settling Time Test Circuit – Rising Edge. Vertical Scale: 5ns/div.; Horizontal Scale: 500μV/div.

Figure 42 shows the oscilloscope response of the generator alone, set up to simulate the ideal test circuit error signal (Figure 43).

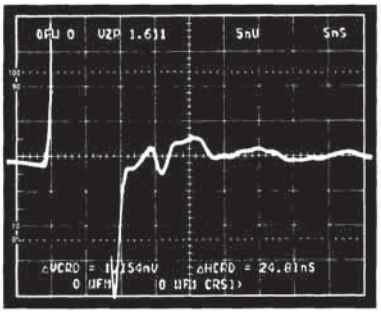


Figure 42. The Oscilloscope Response Alone Directly Driven by the Test Generator. Vertical Scale: 5ns/div.; Horizontal Scale: 500μV/div.

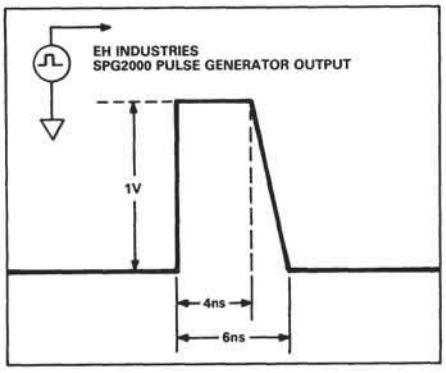


Figure 43. A Simulated Ideal Test Circuit Error Signal

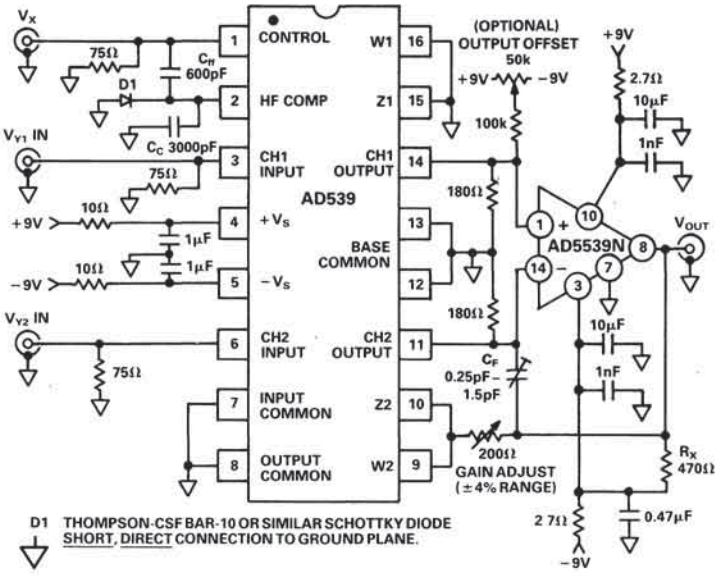


Figure 44. A Wide Bandwidth Voltage-Controlled Amplifier

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 44 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality video-speed applications. This circuit uses the AD5539 as an output amplifier for the AD539, a high bandwidth multiplier. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven ($V_X<0$ or $V_X>3.3V$). Secondly, it provides a choice of either noninverting or inverting responses, using either input V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X>0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If Pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

The bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 45 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from +10mV to +3.16V; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

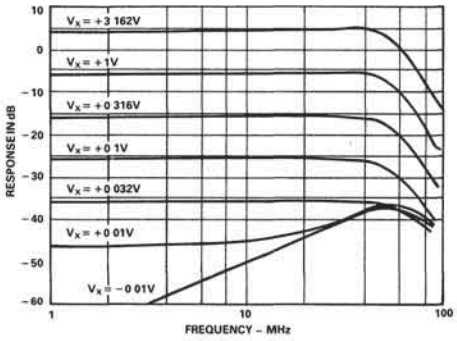


Figure 45. AC Response of the VCA at Different Gains $V_Y = 0.5V$ rms

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = +$ or $-1V$ is shown in Figure 46; with the VCA driving a 75Ω load. The rise and fall times are both approximately 7ns.

A few final circuit details: in general, the control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000pF (3nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high-frequency distortion, reduce the high-frequency crosstalk and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal.

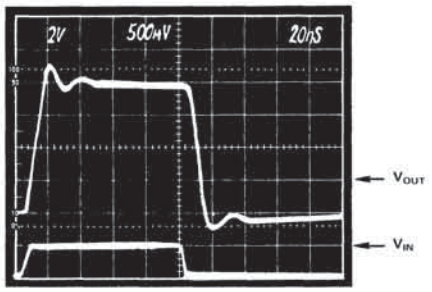


Figure 46. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts, $V_Y = \pm 1$ Volt

The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2MHz with a C_C of 0.01μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (Pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

Diode D1 clamps the logarithmic control node at Pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 47 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high-frequency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1V into a reverse-terminated 75Ω load (or ±2V into 150Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1V at either input generates ±1V (noninverting) or ∓1V (inverting) across the 75Ω load. The circuit provides a gain of about 1, when "ON", or zero when "OFF".

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step changes in the output current as the AD539 is gated on or off.

Figure 49 shows the response to a pulse of 0 to +1V on the signal channel. With the control input held at zero, the rise time is under 10ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05dB over a signal window of 0 to

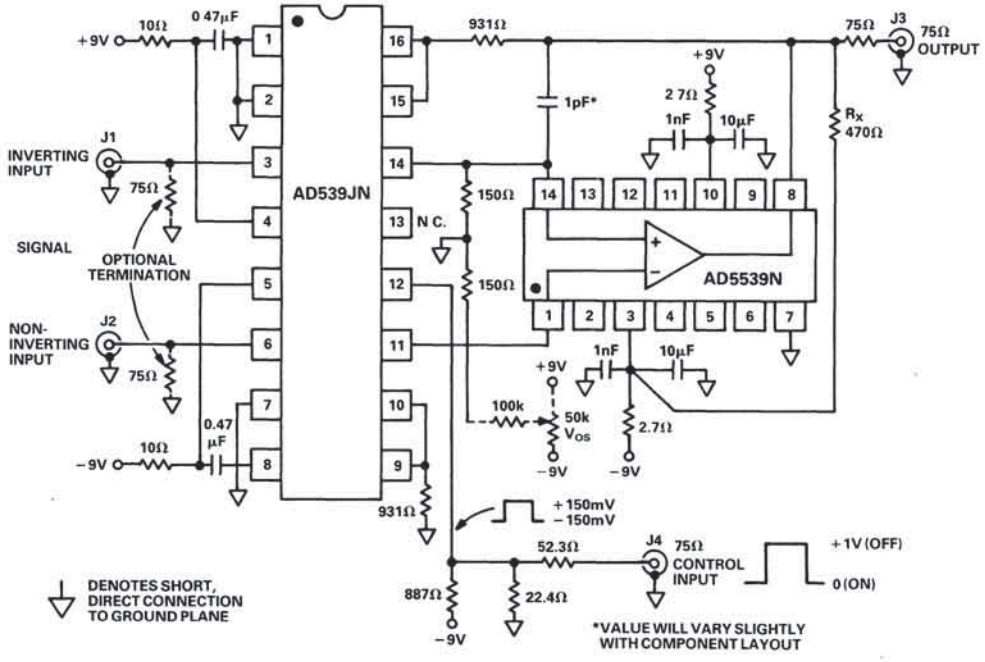


Figure 47. An Analog Multiplier Video Switch

+1V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58MHz. The noise level of this circuit measured at the 75Ω load is typically 200μV in a 0 to 5MHz bandwidth or approximately 100nV per root hertz. The noise spectral density is essentially flat to 40MHz.

The waveforms shown in Figures 48 and 49 were taken across a 75Ω termination; in both photos, the signal of 0 to +1V (in this case, an offset sine wave at 1MHz) was applied to the noninverting input. In Figure 48, the envelope response shows the output being fully switched in about 50ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1V or more. There is very little control-signal breakthrough.

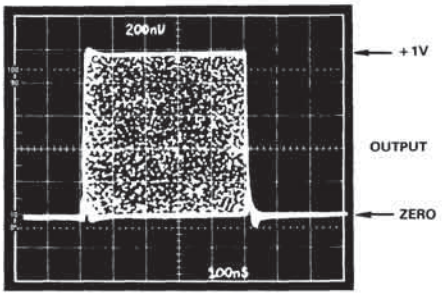


Figure 48. The Control Response of the Video Switcher

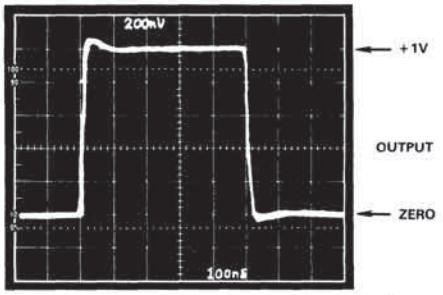


Figure 49. The Signal Response of the Video Switcher

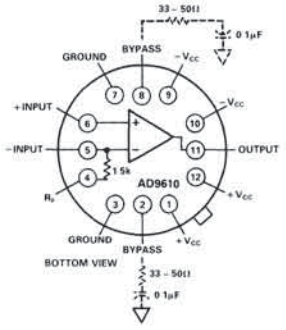
Wide-Bandwidth, Fast-Settling Operational Amplifier

AD9610

FEATURES
Ultrastable Unity Gain Bandwidth (100MHz)
18ns Settling Time to 0.1%
Superior dc Performance
Offset Voltage ±0.3mV
Bias Current 2μA
±21mA Supply Currents

APPLICATIONS
Driving Flash Converters
High-Speed DACs
Radar, IF Processors
Photodiode Preamps
ATE/Pulse Generators
Imaging/Display Drivers

AD9610 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

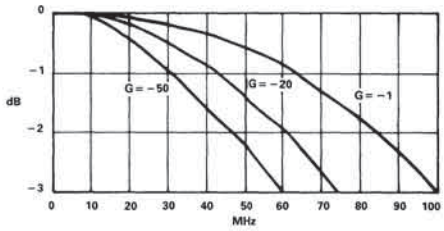
The AD9610 is a fast-settling, wide-bandwidth dc-coupled transimpedance operational amplifier which combines superior dc specifications and exceptional dynamic performance. That combination provides remarkable versatility and utility for high-speed designers.

Thin-film technology and innovative design techniques help assure stable operation over the complete operating temperature range. Input offset voltage temperature drift is typically 5μV/°C; input bias current drift is typically 70nA/°C.

Unique internal architecture keeps the AD9610 inherently stable over its complete gain range and assures wide bandwidth at all gain settings. With G = −1, 3dB bandwidth is 100MHz; with G = −10, bandwidth is 95MHz. When G = −20, 3dB bandwidth is an incredible 75MHz. Slew rate, rise time, fall time, and settling time are also independent of gain.

The design of the AD9610 makes it easy to apply. The unit is internally compensated and needs no external compensation. An internal 1.5kΩ feedback resistor is available to the user by connecting Pin 4 to output Pin 11. Pins 2 and 8 are bypass pins and should be connected to ground through 33 – 50Ω resistors and 0.1μF ceramic capacitors; effective decoupling of the power supplies is also important for proper operation.

Two temperature ranges are available. The AD9610BH is guaranteed over a case temperature range of −25°C to +85°C; the AD9610TH is for a range of −55°C to +125°C. Standard devices are produced in a MIL-STD-1772-certified facility; contact the factory for information on units screened to MIL-STD-883.



AD9610 Inverting Gain

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 1500\Omega$; $R_F = 15k\Omega$; No R_{LOAD})

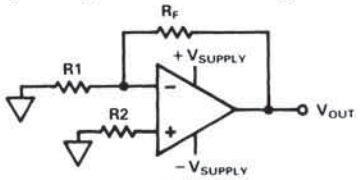
	Parameter (Conditions)	Sub-Group	AD9610BH/TH Typical @ +25°C	AD9610BH[1] Min/Max @ −25°C	AD9610BH[1] Min/Max @ +25°C	AD9610BH[1] Min/Max @ +85°C	AD9610TH[2] Min/Max @ −55°C	AD9610TH[2] Min/Max @ +25°C	AD9610TH[2] Min/Max @ +125°C	Units
√	Offset Voltage	1,2,3	±0.3	±4.0	±1.0	±2.5	±4.0	±1.0	±2.5	mV
√	Offset Voltage T_C[3]	2,3	±5				±25		±25	µV/°C
√	Input Bias Current									
	Inverting	1,2,3	±5	±56	±15	±35	±56	±15	±35	µA
	Noninverting	1,2,3	±15	±75	±50	±62	±75	±50	±62	µA
√	Input Bias Current T_C[3]									
	Inverting	2,3	±70				±330		±330	nA/°C
	Noninverting	2,3	±30				±200		±200	nA/°C
#	Inverting Impedance		20							Ω
#	Noninverting									
	Impedance		200k							Ω
	Capacitance		2							pF
#	Common-Mode Input		±5	±5	±5	±5	±5	±5	±5	V
√	Internal Feedback Resistor (R_F)		1500		1490/1510			1490/1510		Ω
#	R_F Temperature Coefficient			±25		±25	±25		±25	ppm/°C
√	Common-Mode Rejection Ratio (CMRR)[4]	4,5,6	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	CMRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 5V$)		>60							dB
√	Common-Mode Sensitivity (CMS),[5]									
	Referred to Input ($\Delta V_S = 5V$)									
	−CMS	4,5,6	3	8	8	8	8	8	8	µA/V
	+CMS	4,5,6	3	8	8	8	8	8	8	µA/V
	$CMS_{VOLTAGE}$	4,5,6	62	≥50	≥50	≥50	≥50	≥50	≥50	dB
#	Output Impedance (dc to 100kHz)		0.05							Ω
√	Output Voltage Swing ($R_{LOAD} = 200\Omega$)	1,2,3	±10	≥±9	≥±9	≥±9	≥±9	≥±9	≥±9	V
#	Output Current (Continuous)		±50	≥±50	≥±50	≥±50	≥±50	≥±50	≥±50	mA
√	Open Loop Transimpedance Gain (200Ω Load)	4,5,6	>1.5	≥0.7	≥0.9	≥0.7	≥0.7	≥0.9	≥0.7	MΩ
√	Supply Current[6]	1,2,3	21	≤27	≤25	≤27	≤27	≤25	≤27	mA
	Power Consumption[6]		630	≤810	≤750	≤810	≤810	≤750	≤810	mW
√	Power Supply Rejection Ratio (PSRR)[4]	4,5,6	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	PSRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 10V$)		>60							dB
√	Power Supply Sensitivity (PSS),[7]									
	Referred to Input ($\Delta V_S = 10V$)									
	$PSS_{VOLTAGE}$	4,5,6	65	50	50	50	50	50	50	dB
	−PSS	4,5,6	3	8	8	8	8	8	8	µA/V
	+PSS	4,5,6	3	8	8	8	8	8	8	µA/V

AC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 150\Omega$; $R_F = 1.5k\Omega$; $R_{LOAD} = 200\Omega$)

	Bandwidth (−3dB) (V_{OUT} = 100mV p-p)									
√	G = −10	4,5,6	>100	≥80	≥80	≥80	≥80	≥80	≥80	MHz
	Amplitude of Peaking:									
√	DC to 60MHz	4,5,6	0	≤0.4	≤0.2	≤1.0	≤0.4	≤0.2	≤1.0	dB
#	>60MHz		0	≤0.6	≤0.3	≤1.8	≤0.6	≤0.3	≤1.8	dB
#	Phase Nonlinearity (dc to 45MHz)		1							°
#	Rise (Fall) Time (V_{OUT} = 5V Step)		<3.5	≤4	≤4	≤4.3	≤4	≤4	≤4.3	ns
#	Slew Rate (V_{OUT} = 18V Step)		>3.5	≥3	≥3	≥2.4	≥3	≥3	≥2.4	kV/µs
#	Settling Time to 0.1% (G = −10; 5V Output Step)		18	≤29	≤25	≤29	≤29	≤25	≤29	ns
#	Settling Time to 0.02% (G = −10; 5V Output Step)		30							ns
#	Overshoot Amplitude (V_{OUT} = 5V Output Step)		<4	≤14	≤8	≤18	≤14	≤8	≤18	%
#	Propagation Delay		3.3	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	ns
√	Total Harmonic Distortion (Freq. = 20 MHz; Output Voltage = 2V p-p)	4,5,6	55	50	50	50	50	50	50	dB
#	Input Noise ($R_{LOAD} = 100\Omega$)									
	Voltage (5MHz to 150MHz)		0.7	≤1.2	≤1.5	≤2.0	≤1.2	≤1.5	≤2.0	$nV/\sqrt{Hz}$
	Current (5MHz to 150MHz)		23	≤29	≤30	≤35	≤29	≤30	≤35	$pA/\sqrt{Hz}$

Parameter	Sub-Group	AD9610BH/TH Typical @ +25°C	AD9610BH Min/Max @ −25°C	AD9610BH Min/Max @ +25°C	AD9610BH Min/Max @ +85°C	AD9610TH Min/Max @ −55°C	AD9610TH Min/Max @ +25°C	AD9610TH Min/Max @ +125°C	Units
OTHER INFORMATION									
Case to Ambient, θ_{CA}[8] (Still Air; No Heat Sink)		65	*	*	*	*	*	*	°C/W
Case to Ambient, θ_{CA}[8] (500 LFPM Air; No Heat Sink)		38	*	*	*	*	*	*	°C/W
MTBF[9]		$\geq 1.48 \times 10^6$	*	*	*	*	*	*	hours
PACKAGE OPTION[10]									
TO-8 (H-12A)			AD9610BH			AD9610TH			

NOTES
√ 100% tested (See Notes 1 and 2).
Specifications guaranteed by design; not tested.
*Specification same as AD9610BH/TH typical specification.
[1]AD9610BH parameters preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over the industrial temperature range (−25°C to +85°C) case temperature.
[2]AD9610TH parameters preceded by a check (√) are tested at 55°C case, +25°C ambient, and + 125°C case temperatures. Mil-processed versions are available.
[3]Offset voltage T_C and bias current T_C are guaranteed over the respective temperature ranges.
[4]CMRR and PSRR apply only for stated conditions.
[5]CMS values can be used to determine the CMRR for specific gain settings according to the following worst case relationships:



$$\Delta V_{OUT} = [-CMS]\,[R_F]\,[\Delta V_{SUPPLY}] + [+CMS]\,[R2]\left[1+\frac{R_F}{R1}\right]\,[\Delta V_{SUPPLY}] + [CMS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta -V_{SUPPLY} \text{ AND } \Delta +V_{SUPPLY}$$

$$CMRR = -20\ LOG\left[\left(\frac{\Delta V_{OUT}}{1+\frac{R_F}{R1}\chi\,\Delta V_{SUPPLY}}\right)\right]$$

[6]Supply current and power dissipation numbers are for quiescent operation (input is grounded). Values increase with higher frequency operation.
[7]PSS values can be used to determine the PSRR for specific gain settings according to the following worst case relationships (See diagram in 5 above):

$$\Delta V_{OUT} = [-PSS]\,[R_F]\,[\Delta V_{SUPPLY}] + [+PSS]\,[R2]\left[1+\frac{R_F}{R1}\right]\,[\Delta V_{SUPPLY}] + [PSS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta -V_{SUPPLY} \text{ OR } \Delta +V_{SUPPLY}$$

$$PSRR = -20\ LOG\left[\left(\frac{\Delta V_{OUT}}{1+\frac{R_F}{R1}\chi\,\Delta V_{SUPPLY}}\right)\right]$$

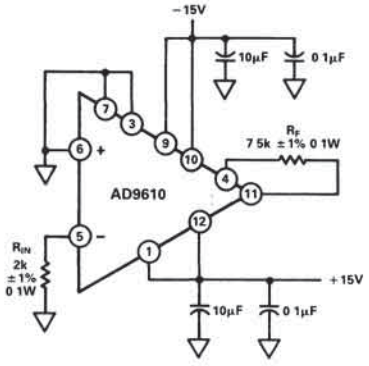
[8]Recommended maximum junction temperature is +165°C. See Thermal Model.
[9]MTBF calculated using MIL-HNBK 217D; Ground Fixed; Temperature (case) = +70°C.
[10]See Section 16 for package outline information.
Specifications subject to change without notice.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperatures.
Subgroup 11 – Switching tests at minimum rated temperatures.
Subgroup 12 – Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ($\pm V_S$) . . . . . ±18V
Operating Temperature Range (case)
AD9610BH . . . . . −25°C to +85°C
AD9610TH . . . . . −55°C to +125°C
Power Dissipation . . . . . See Thermal Model
Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C



THIS MICROCIRCUIT IS COVERED BY TECHNOLOGY GROUP (I) PER MIL-M-38510

AD9610 LIFE TEST/BURN-IN CIRCUIT

THEORY OF OPERATION

The advantages of the transimpedance AD9610 Operational Amplifier become easier to understand when its operation is compared to the operation of conventional high-speed op amps.

The operation of the AD9610 Operational Amplifier is similar to a standard voltage-input differential amplifier in terms of setting gain and calculating noise. The primary difference between the two types is a low-impedance inverting input on the AD9610; this causes the unit to use current feedback, rather than voltage feedback, to achieve signal amplification.

Figure 1 and the discussion which follows help make a comparison between the AD9610 and "conventional" devices.

Two equations are necessary to describe the amplifier shown in Figure 1.

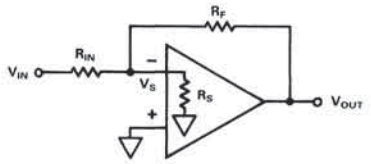


Figure 1.

One equation is a rudimentary amplifier transfer function:

$$-V_{OUT} = A(\omega)\, V_S \qquad \textit{(Equation A)}$$

and the other sums the currents at the inverting input:

$$\frac{V_S - V_{IN}}{R_{IN}} + \frac{V_S}{R_S} + \frac{V_S - V_{OUT}}{R_F} = 0 \qquad \textit{(Equation B)}$$

Rearranging and reducing Equation B; and substituting from Equation A results in a third equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A(\omega)R_S R_F \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)}{1 + A(\omega)R_{IN}R_S \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)} \qquad \textit{(Equation C)}$$

For purposes of discussion, assume the amplifier shown in Figure 1 exhibits a single-pole frequency response. When it does, $A(\omega) = A_O/(1 + j\omega\tau)$ where A_O = open loop gain; and $1/\tau$ = the roll-off frequency. When these terms are substituted into Equation C, the result is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_O R_S R_F \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)}{1 + j\omega\tau + \left[A_O R_{IN} R_S \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)\right]}$$

Based on the idea that

$$1 + \left[A_O R_{IN} R_S \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)\right]$$

is approximately equal to

$$A_O R_{IN} R_S \Big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)$$

and G (closed loop gain) = R_F/R_{IN}, it becomes possible to simplify and substitute terms in the above equation to obtain:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \dfrac{j\omega\tau R_F}{A_O}\left[\dfrac{1}{R_{IN}} + \dfrac{1}{R_S} + \dfrac{1}{R_F}\right]}$$

The fundamental difference between the AD9610 and traditional amplifiers becomes apparent at this point.

In traditional voltage-imput amplifiers, the input resistance (R_S) approaches infinity. Consequently, $1/R_S$ approaches zero; and the term $R_F\,(1/R_{IN} + 1/R_S + 1/R_F)$ simplifies to the term $R_F\,(1/R_{IN} + 1/R_F)$. The latter can be reduced further to $(G + 1)$. When substitutions are made, the gain/frequency relationship for a traditional amplifier design is expressed as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \dfrac{j\omega\tau}{A_O}[G + 1]}$$

There is a dramatically different result for the AD9610.

This difference is because the value of R_S in the transimpedance amplifier is only 20Ω. This is important when one realizes $R_S \parallel R_{IN} \parallel R_F$; and $R_S <<< R_{IN}$ and/or R_F. In this case, $(1/R_S + 1/R_{IN} + 1/R_F) \approx 1/R_S$. Substituting terms, a direct comparison with traditional amplifer relationships can be made:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \frac{j\omega\tau}{A_O}\left[\frac{R_F}{R_S}\right]}$$

Both amplifier types yield similar algebraic results, but there is one critical difference in how they are obtained.

As shown above, the closed loop gain (G) of the traditional amplifier is multiplied by the frequency-dependent term of the denominator; **this means increasing frequencies or closed loop gain accelerates the gain roll-off.**

In the AD9610, however, the constant R_F/R_S is multiplied by the frequency-dependent term; **this means bandwidth remains relatively constant for any given value of gain.**

Inside the AD9610, the design includes a 1.5kΩ feedback resistor to help reduce the effect of stray capacitances and make it easier to apply the amplifier. This internal R_F means *the gain of the AD9610 is set by varying R_{IN}.*

The differences in the architecture of the AD9610 vis-a-vis a traditional op amp cause its closed-loop frequency response to be considerably different from conventional units.

Figure 2 pictures a typical plot for a traditional single-pole amplifier.

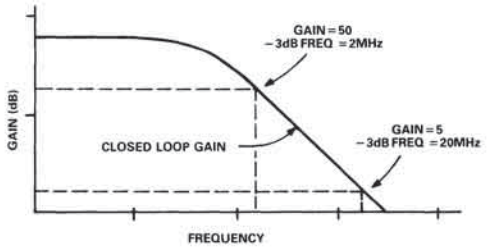


Figure 2.

As shown, increasing the closed loop gain of a traditional op amp decreases the bandwidth of the amplifier; the precise amount of change will be determined by the actual roll-off characteristics of the op amp.

By contrast, the frequency response of the AD9610 changes very little when the gain is changed. Refer to Figure 3.

Variations in gain (established by varying values of R_{IN}) have only a negligible effect on the bandwidth of the amplifier.

(NOTE: For a more complete explanation of the mathematics involved in comparing conventional op amps and the AD9610, refer to the Analog Devices application note entitled "Using the AD9610 Transimpedance Amplifier".)

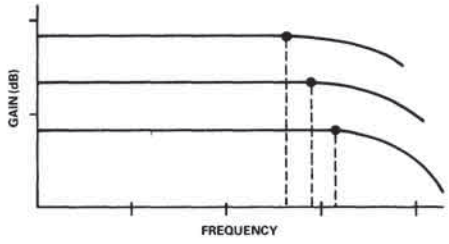


Figure 3.

AD9610 FUNCTIONAL DESCRIPTION

Refer to Figure 4, AD9610 Functional Circuit.

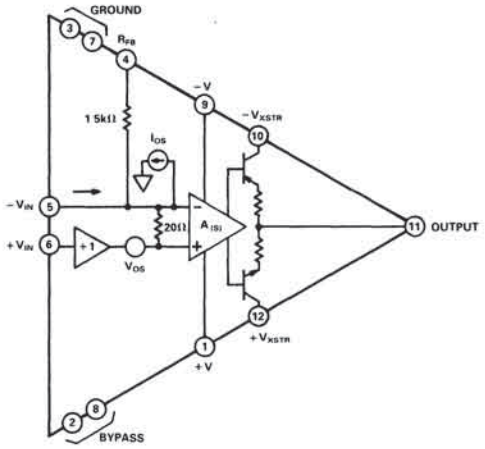


Figure 4. AD9610 Functional Circuit

The most prominent characteristic illustrated in this model of the unit is the combination of a high-impedance noninverting terminal and a low-impedance inverting terminal. This is achieved by buffering the noninverting terminal to create a high-impedance input; while maintaining a low impedance through the 20Ω characteristic of the inverting input.

Because of the low input impedance of the inverting input, all of the input signal voltage is impressed across the input resistor (R_{IN} in Figure 6); this causes a direct voltage-to-current conversion to take place.

Conventional op amps use a volts/volts transfer function, while the transfer function of the AD9610 is volts/μA (or resistance).

Signal current flowing in the inverting terminal (Pin 5) will flow through the 20Ω resistor. The voltage developed across this input impedance becomes the input signal for the internal amplifier.

As a result of this action, the input current is converted to an output voltage; this is the reason for the open loop transfer function being expressed in ohms.

To compensate for variations in offset voltage and current in the AD9610, both a voltage source and a current source are included in the unit. Input offset voltage (V_{OS}) is a dc error which appears at the output as $[V_{OS}\ (1+R_F/R_{IN})]$. In a similar fashion, the input bias current (I_{OS}) reflects as a dc error which appears at the output as $[I_{OS}\ (R_F)]$.

The current source connected to the inverting terminal effectively models the input offset current; and although bias currents flow in both terminals, the inverting input bias current is dominant. The combined actions of the internal voltage and current sources effectively compensate for discrepancies in offset voltage and current.

Power supply voltages applied to the AD9610 are separated, with one set of terminals designated for the output transistors (Pins 10 and 12) and another set for the internal amplifier (Pins 1 and 9). This splitting of the voltages makes it possible to limit voltage swings and current at the output, and helps regulate the junction temperatures of the output transistors.

APPLYING THE AD9610 OP AMP

In applying the AD9610 op amp, there are certain precautions which **must** be observed to protect the unit from damage:

1. Shorting either power supply input pin (Pin 10 or Pin 12) to the output (Pin 11) will destroy the device.
2. Shorting the output (Pin 11) to ground will destroy the device; no internal protection is provided.

As explained earlier, the noninverting input of the AD9610 Operational Amplifier is a high impedance. This requires that it be driven from a low-impedance source, or connected to ground. Driving this input from a high impedance detracts from the wide bandwidth performance; connecting it to ground avoids the possibility of closed-loop ac peaking.

Because the internal biasing network of the AD9610 is connected to the +V and −V supply pins, it is important that these pins have adequate decoupling. Nominal supply voltages for the AD9610 are ±15V, but this can be reduced to a lower limit of ±12V without serious degradation of high-speed performance. When ±12V supplies are used, output voltage swings from the amplifier must be reduced.

Bypass Pins 2 and 8 should be decoupled to ground through 33 – 50Ω resistors and 0.1μF capacitors to maintain stability on the bias network.

Feedback resistor R_F is internal to the AD9610 and has been precisely adjusted to allow the widest possible range of operating conditions. While it is possible to use an external feedback resistor for the device, the user is urged to avoid the temptation to "tune" performance with this technique because it will inevitably detract from ac performance.

A massive low-impedance ground plane is essential for optimum performance from the AD9610 because it provides a moderate level of shielding and helps reduce the effects of distributed capacitance.

But the benefits of a large ground plane can be diminished if components are grounded at multiple points on the ground plane. Single-point grounding is *always* preferred for high-speed circuits to avoid the possibility of voltage differentials which might result from multiple grounds.

The best high-frequency performance is obtained from the AD9610 when total output capacitance is minimized. Realistically, this is not always possible; but performance can be improved with a 5 – 30Ω resistor in series with the output as shown in Figure 5.

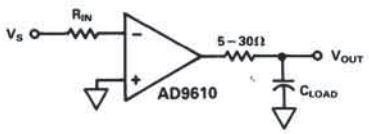


Figure 5.

Isolation provided by the series resistor makes it possible for the AD9610 to drive loads well outside its design limits, but at some loss of speed. Isolating the capacitive load from the output of the amplifier is particularly useful when driving flash A/D converters.

The power supplies for the AD9610 must be decoupled effectively to obtain maximum performance from the device. Recommended choices are a 0.1μF ceramic capacitor and a 10μF tantalum capacitor in parallel on each supply. These connections show up in Figures 6 and 7 which illustrate the connections for inverting and noninvertering operation, respectively. Decoupling components should always be connected as closely as possible to the amplifier's voltage supply pins.

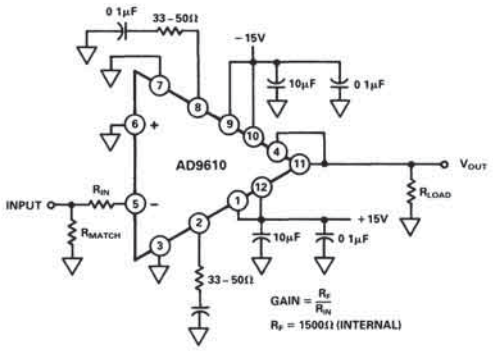


Figure 6. AD9610 Inverting Operation

If the expected output voltage swings are small, it is possible to operate the ouput stages from ±5V supplies; this will reduce power dissipation and junction temperatures on the output transistors. For this, the ±5V and ±15V supplies must be decoupled separately.

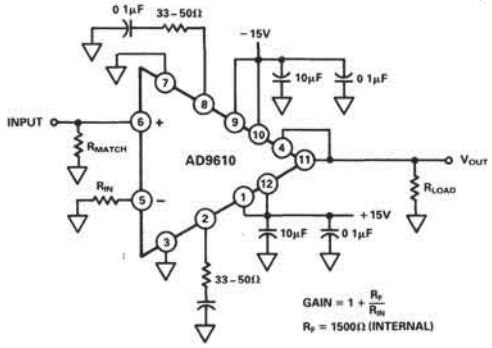


Figure 7. AD9610 Noninverting Operation

As shown in Figures 6 and 7, bypass pins 2 and 8 should be decoupled individually with a 33 – 50Ω resistor and 0.1μF capacitor in series to ground. Without this decoupling, power supply and common-mode rejection ratios (PSRR and CMMR) may be degraded. In some applications, the lack of this decoupling may show up as very high-frequency "ringing" on the output. R_{MATCH} in Figures 6 and 7 is used to match the output impedance of the driving source.

AD9610 POWER DISSIPATION

Quiescent power supply currents for the AD9610 are ±21mA. Supply currents this low allow the unit to be operated over a wide temperature range without damage. For high-temperature operation and long-term stability, however, the user is urged to use a heat sink. Two acceptable models for TO-8 packages are the Thermalloy 2240 and the IERC Up-TO8-48CB.

Refer to Figure 8.

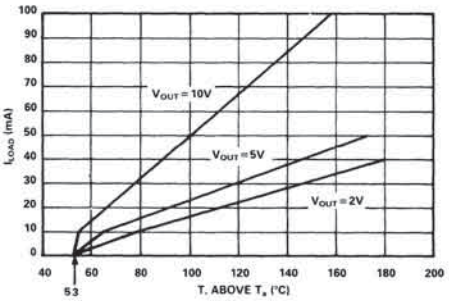
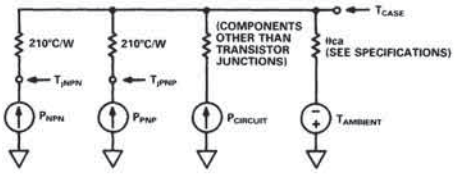


Figure 8. Junction Temp. Rise vs. Load Current

The data in this illustration are typical characteristics when the AD9610 is operated from ±15V supplies. Assume the desired output from the op amp is ±10V swings at ±50mA currents. For this combination, maximum junction temperature will be 100°C above the ambient temperature.

Since maximum allowable junction temperature is +165°C, the maximum ambient temperature which can be tolerated is +65°C. If there is a possibility the ambient may exceed this limit, heat sinking and/or heat removal is required. Additional details on the thermal characteristics of the unit are included in the AD9610 Thermal Model. *(For more information on thermal protection, consult the Analog Devices application note "Using the AD9610 Transimpedance Amplifier".)*



$P_{CIRCUIT} = I_{CC}[+V_{CC} - (-V_{CC})]$ WHERE I_{CC} = 21mA @ ±15V

$P_{XXX} = [(\pm V_{CC}) - V_{OUT} - I_{COL}(8)](I_{COL})$ (% DUTY CYCLE)

NOTE $_{XXX}$ = NPN OR PNP

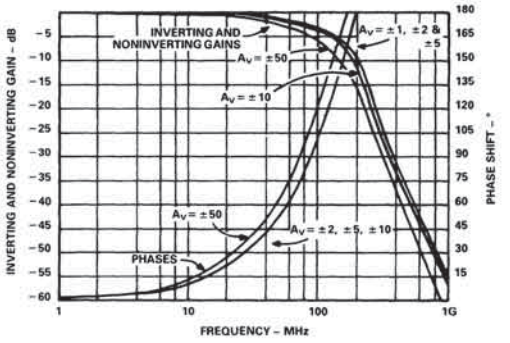
(FOR POSITIVE V_{OUT} AND V_{CC}, THIS IS POWER IN NPN OUTPUT STAGE
FOR NEGATIVE V_{OUT} AND V_{CC}, THIS IS POWER IN PNP OUTPUT STAGE
$I_{COL} = V_{OUT}/R_{LOAD}$ or 3 0mA, WHICHEVER IS GREATER
FEEDBACK RESISTOR R_F IS INCLUDED IN R_{LOA})

$T_{J(PNP)} = P_{PNP}(210 + \theta ca) + \{P_{CIRCUIT} + P_{NPN}\}(\theta ca) + T_A$ SIMILAR FOR $T_{J(NPN)}$

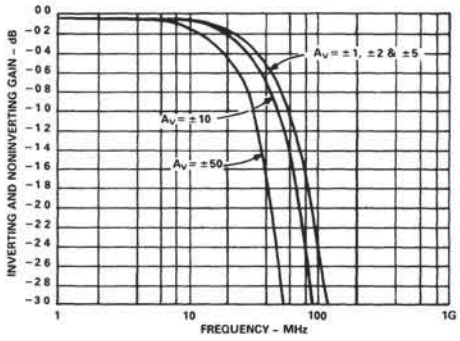
AD9160 Thermal Model

AD9610 PERFORMANCE

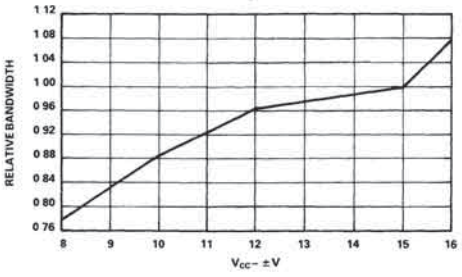
In the following section, graphs and photographs depict typical performance of the AD9610 for various characteristics.



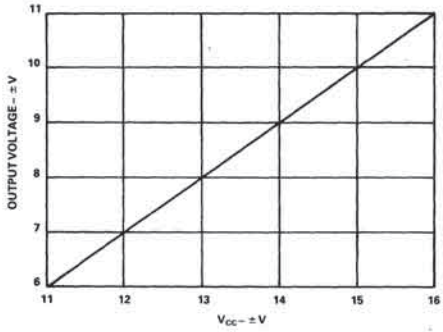
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



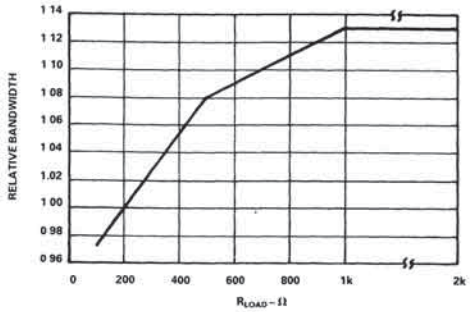
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



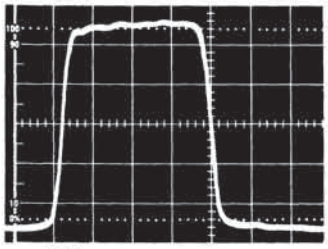
Bandwidth vs. V_{CC}



Output Voltage vs. V_{CC}

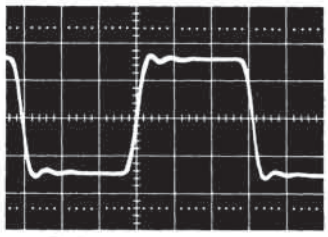


Bandwidth vs. Load



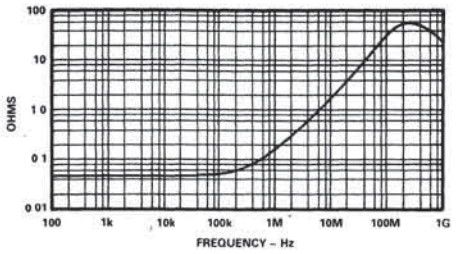
GAIN = – 10; 136mV/DIV; 10ns/DIV

AD9610 Small-Signal Pulse Response

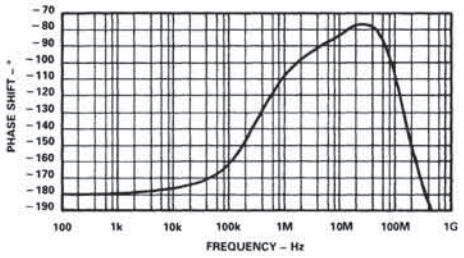


GAIN = – 10; 3.4V/DIV; 10ns/DIV

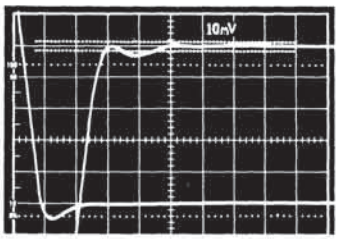
AD9610 Large-Signal Pulse Response



Small-Signal Output Resistance vs. Frequency (G = – 10)



Small-Signal Output Phase Shift vs. Frequency (G = – 10)



GAIN = – 10; 5V OUTPUT, ERROR WINDOW (±5mV) = 0 1%, 5ns/DIV

AD9610 Settling Time

ORDERING INFORMATION

Two models of the AD9610 Operational Amplifier are available. The AD9610BH is specified for operation over a case temperature range of – 25°C to + 85°C; the AD9610TH is intended for applications in which case temperature may be between – 55°C and + 125°C.

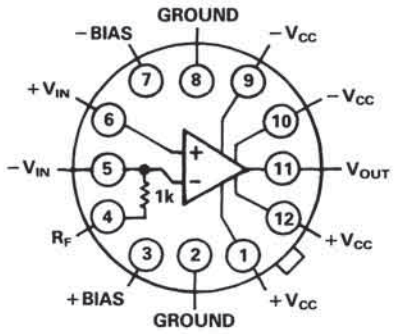
Wide Bandwidth, Fast-Settling Operational Amplifier

AD9611

FEATURES
Unity Gain Stable
Small-Signal Bandwidth 280MHz
Full Power Bandwidth 210MHz
Settling – 13ns to 0.1%
Rise/Fall Times 1.3ns/1.5ns
Offset Voltage ±0.5mV
Bias Current ±1μA
Power Dissipation Independent of Load

APPLICATIONS
Driving Flash Converters
High-Speed DACs
Radar, IF Processors
Baseband and Video Communications
Photodiode Preamps
ATE/Pulse Generators
Imaging/Display Applications

AD9611 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9611 is an ultrafast-settling, wide-bandwidth, dc-coupled operational amplifier that combines exceptional ac and dc specifications to establish a new standard of excellence in dc-coupled amplifiers.

Rise and fall times are 1.3ns and 1.5ns, respectively. The −3dB bandwidth is 280MHz (G = −5); the full-power bandwidth is 210MHz. The AD9611 settles to 0.1% in 13ns, and dc performance is also exceptional. Offset voltage is ±0.5mV and drifts only 5μV/°C. The inverting and noninverting bias currents are 1μA.

The AD9611 requires ±5V power supplies and employs an innovative current-steering output stage that keeps the total circuit power dissipation essentially constant regardless of output drive (for loads ≤100Ω). *Circuit power dissipation does not increase as the load is increased*; the unit can be operated up to +110°C in still air without heat sinking.

Current feedback is used instead of voltage feedback to provide dynamic performance that is relatively independent of gain settings. Flat gain and phase response combine with excellent noise and distortion performance to provide a unity-gain-stable amplifier especially well suited for use in digital communication systems. The AD9611 is an excellent choice for driving the newest generation of ultrahigh-speed flash converters when system SNR and effective number of bits are important.

The AD9611 is constructed with discrete transistors on a precision thin-film substrate. The AD9611BH is rated for case temperatures from −25°C to +85°C; the AD9611TH is guaranteed from −55°C to +125°C. Contact the factory for information about 883 grade parts. All units are built and tested in a MIL-STD-1772-certified facility.

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5V$; $A_V = -5$; $R_{IN} = 200\Omega$; $R_{FB} = 1k\Omega$; $R_{LOAD} = 100\Omega$)

	Parameter (Conditions)	Sub-Group	AD9611JBH/TH Typical @ +25°C	AD9611BH[1] Min/Max@ −25°C	AD9611BH[1] Min/Max@ +25°C	AD9611BH[1] Min/Max@ +85°C	AD9611TH[2] Min/Max@ −55°C	AD9611TH[2] Min/Max@ +25°C	AD9611TH[2] Min/Max@ +125°C	Units
√	Offset Voltage	1,2,3	±0.5	±5.0	±3.0	±4.3	±5.0	±3.0	±4.3	mV
#	Offset Voltage T_C[3]		±5				±20		±20	µV/°C
√	Input Bias Current									
	Inverting	1,2,3	±1	±40	±5	±19	±40	±5	±19	µA
	Noninverting	1,2,3	±1	±25	±5	±15	±25	±5	±15	µA
	Input Bias Current T_C[3]									
	# Inverting		±140				±275		±275	nA/°C
	# Noninverting		±75				±175		±175	nA/°C
	Noninverting									
	Impedance		150							kΩ
	Capacitance		3							pF
√	Common-Mode Input Range	1,2,3	±1.5	±1.4	±1.4	±1.25	±1.4	±1.4	±1.25	V
√	Internal Feedback Resistor (R_{FB})		1000	987/1013	990/1010	987/1013	987/1013	990/1010	987/1013	Ω
#	R_{FB} Temperature Coefficient			±25		±25	±25		±25	ppm/°C
√	Common-Mode Rejection Ratio ($\Delta V_{CM} = 0.5V$)[4]	4,5,6	42	≥32	≥34	≥32	≥32	≥34	≥32	dB
√	Common-Mode Sensitivity (CMS)[5]									
	Referred to Input									
	−CMS	4,5,6	5	≤24	≤20	≤24	≤24	≤20	≤24	µA/V
	+CMS	4,5,6	5	≤24	≤20	≤24	≤24	≤20	≤24	µA/V
	Output Impedance (dc to 1MHz)		0.03							Ω
	Output Impedance @ 100MHz		0.4/18							Ω/nH
√	Output Voltage Swing	1,2,3	±3	≥±2.8	≥±2.8	≥±2.5	≥±2.8	≥±2.8	≥±2.5	V
#	Output Current (continuous)		±50	≥±40	≥±40	≥±40	≥±40	≥±40	≥±40	mA
#	Open-Loop Transimpedance Gain (100Ω Load)		>0.35	≥0.1	≥0.2	≥0.2	≥0.1	≥0.2	≥0.2	MΩ
√	+Supply Current(5V)[6]	1,2,3	70	≤85	≤77	≤77	≤85	≤77	≤77	mA
√	−Supply Current(−5V)[6]	1,2,3	74	≤88	≤80	≤80	≤88	≤80	≤80	mA
	Power Consumption[6]		720	≤865	≤785	≤785	≤865	≤785	≤785	mW
√	Power Supply Rejection Ratio ($\Delta V_S = 0.5V$)[4]	4,5,6	46	≥35	≥37	≥35	≥35	≥37	≥35	dB
√	Power Supply Sensitivity (PSS)[7]									
	Referred to Input									
	−PSS	4,5,6	4	≤17	≤14	≤17	≤17	≤14	≤17	µA/V
	+PSS	4,5,6	4	≤17	≤14	≤17	≤17	≤14	≤17	µA/V

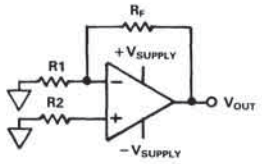
AC ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5V$; $A_V = -5$; $R_{IN} = 200\Omega$; $R_{FB} = 1k\Omega$; $R_{LOAD} = 100\Omega$ unless otherwise specified)

√	Bandwidth (−3dB) (V_{OUT} = 1V p-p)	4,5,6	>280	≥250	≥250	≥220	≥250	≥250	≥220	MHz
	Full Power Bandwidth (V_{OUT} = 3V p-p)		>210							MHz
	Slew Rate		1900							V/µs
	Amplitude of Peaking:									
√	dc to 70MHz (V_{OUT} = 1V p-p)	4,5,6	0	0.2	0.2	0.2	0.2	0.2	0.2	dB
√	>70MHz (V_{OUT} = 1V p-p)	4,5,6	0	≤0.8	≤0.8	≤1.6	≤0.8	≤0.8	≤1.6	dB
	Phase Nonlinearity (dc to 120MHz)		1							°
#	Rise Time (V_{OUT} = 1V Step)		1.3	≤1.5	≤1.5	≤1.7	≤1.5	≤1.5	≤1.7	ns
#	Fall Time (V_{OUT} = 1V Step)		1.5	≤1.7	≤1.7	≤1.9	≤1.7	≤1.7	≤1.9	ns
#	Rise Time (V_{OUT} = 3V Step)		1.4	≤1.6	≤1.8	≤2.1	≤1.6	≤1.8	≤2.1	ns
#	Fall Time (V_{OUT} = 3V Step)		1.6	≤2.0	≤2.0	≤2.1	≤2.0	≤2.0	≤2.1	ns
#	Settling Time to 1% (V_{OUT} = 1.5V Step)		7	≤12	≤12	≤13	≤12	≤12	≤13	ns
#	Settling Time to 0.1% (V_{OUT} = 3V Step; R_L = 50Ω)		13	≤19	≤19	≤22	≤19	≤19	≤22	ns
	Settling Time to 0.05% (V_{OUT} = 3V Step; R_L = 50Ω)		16							ns
#	Overshoot Amplitude (V_{OUT} = 2V Step)		4	≤14	≤14	≤18	≤14	≤14	≤18	%
	Overdrive Recovery to 1% (2X; 50ns)									
	Positive Rail to Linear Region		20							ns
	Negative Rail to Linear Region		40							ns
	Propagation Delay		2.1							ns
√	2nd Harmonic Distortion (f = 60MHz; V_{OUT} = 2V p-p)	4,5,6	−54	≤−50	≤−50	≤−42	≤−50	≤−50	≤−42	dB
√	3rd Harmonic Distortion (f = 60MHz; V_{OUT} = 2V p-p)	4,5,6	−58	≤−51	≤−51	≤−44	≤−51	≤−51	≤−44	dB

Parameter	Sub-Group	AD9611BH/TH Typical @ +25°C	AD9611BH Min/Max@ −25°C	AD9611BH Min/Max@ +25°C	AD9611BH Min/Max@ +85°C	AD9611TH Min/Max@ −55°C	AD9611TH Min/Max@ +25°C	AD9611TH Min/Max@ +125°C	Units
Noise									
# Voltage (5MHz to 280MHz)		1.0	≤1 4	≤1.4	≤1 7	≤1.4	≤1.4	≤1.7	nV/√Hz
# Current (5MHz to 280MHz)		21	≤25	≤25	≤28	≤25	≤25	≤28	pA/√Hz
# Equivalent Integrated Input (5MHz to 280MHz)		75	≤92	≤92	≤106	≤92	≤92	≤106	μV
Other Information									
Case to Ambient, θ_{CA}[8,9] (Still Air; No Heat Sink)		50	*	*	*	*	*	*	°C/W
Case to Ambient, θ_{CA}[8,9] (500 LFPM Air; No Heat Sink)		30	*	*	*	*	*	*	°C/W
MTBF (Mean Time Betwen Failures) (T_{CASE} = 70°C, Ground Fixed; per MIL-HDBK-217D)		≥1 96 × 10⁶	*	*	*	*	*	*	hours
PACKAGE OPTION[10]									
TO-8 (H-12A)				AD9611BH			AD9611TH		

For applications assistance, call Computer Labs Division @ (919) 668-9511

NOTES
√ 100% tested (See Notes 1 and 2)
Specifications guaranteed by design, not tested
*Specification same as AD9611BH/TH typical specification
[1]AD9611BH parameters preceded by a check (√) are tested at +25°C ambient temperature, performance is guaranteed over the industrial temperature range (−25°C to +85°C) case temperature
[2]AD9611TH parameters preceded by a check (√) are tested at −55°C case, +25°C ambient, and +125°C case temperatures
[3]Offset voltage T_C and bias current T_C are guaranteed over the respective temperature ranges
[4]CMRR and PSRR apply only for stated conditions
[5]CMS values can be used to determine the CMRR for specific gain settings according to the following worst case relationships



$$\Delta V_{OUT} = [-CMS][R_F][\Delta V_{CM}] - [+CMS][R2]\left[1 + \frac{R_F}{R1}\right][\Delta V_{CM}]$$

$$CMRR = -20\ LOG\left[\frac{\Delta V_{OUT}}{(\Delta V_{CM})}\right]$$

[6]Supply current and power dissipation numbers are for quiescent operation (V_{IN} = 0V). A proprietary output stage assures total circuit power dissipation does not increase as a function of output current and R_{LOAD}. (See Text)
[7]PSS values can be used to determine the PSRR for specific gain settings according to the following worst case relationships (See diagram in 5 above):

$$\Delta V_{OUT} = [-PSS][R_F][\Delta V_{SUPPLY}] - [+PSS][R2]\left[1 + \frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta - V_{SUPPLY} \text{ OR } \Delta + V_{SUPPLY}$$

$$PSRR = -20\ LOG\left[\frac{\Delta\ V_{OUT}}{(\Delta V_{SUPPLY})}\right]$$

[8]Recommended maximum junction temperature is +165°C.
[9]Bottom of unit raised approximately 0 125" (3 2mm) above surface of copper-clad board
[10]See Section 16 for package outline information.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (±V_S)	±6V
Analog Input	≤V_S
Inverting Input Sink Current	30mA
Continuous Output Current	±50mA
Operating Temperature Range (Case)	
AD9611BH	−25°C to +85°C
AD9611TH	−55°C to +125°C
Power Dissipation	See Thermal Model
Junction Temperature	+165°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C

EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C. (10% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperatures.
Subgroup 11 – Switching tests at minimum rated temperatures.
Subgroup 12 – Periodically sample tested.

THEORY OF OPERATION

The advantages of using the transimpedance AD9611 operational amplifier instead of a conventional high-speed op amp are based on the difference in the way the two types of amplifiers operate.

The AD9611 operational amplifier uses current feedback, rather than the voltage feedback common to traditional amplifiers. Current feedback amplifiers provide significantly more bandwidth at given gain settings than traditional amplifiers do.

Both types are similar in terms of setting gain and calculating noise, but there is a major difference in the input stages when comparing current feedback (transimpedance) amplifiers and voltage feedback amplifiers.

Traditionally, conventional amplifiers have two high-impedance inputs. Within the AD9611, however, the inputs are connected across a unity gain buffer; this causes the noninverting input to be a high impedance and the inverting input to be low impedance.

Under normal operating conditions, the inverting input current is very small. The AD9611 operation is similar to a traditional amplifier in that the voltage between the input terminals and the bias currents are, ideally, zero.

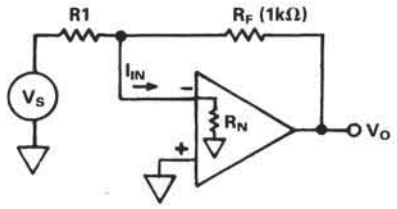


Figure 1.

Closed-loop bandwidth (CLBW) of the AD9611 is first-order independent of its closed-loop gain (G). Its transfer function can be expressed as:

$$1. \quad \frac{V_O}{V_S} \cong \frac{G}{\frac{R_F}{T(s)}\left(1 + \frac{R_N}{R1}\right) + 1}$$

where:
R_F is the internal feedback resistor; R_F = 1kΩ
R1 is the gain-setting input resistor
T(s) is the transimpedance gain as a function of frequency (s) and is independent of gain-setting resistors; $T(s) = V_O(s)/I_{IN}(s)$
$G = R_F/R1$ (closed-loop gain)
R_N is the open-loop input impedance (typically 22Ω in the 200MHz – 300MHz band)

When closed-loop gain is greatly increased, CLBW is only slightly diminished because of the low input impedance of R_N. The ratio of CLBW for any gain to CLBW at G = −0 can be determined using the following relationship:

$$2. \quad \frac{CLBW\ (G=x)}{CLBW\ (G=0)} \cong \frac{1}{\left[1 - \frac{R_N}{R_F} G\right]} = \frac{1}{(1 - 0.022G)}$$

As an example, when G = −20, the CLBW will be 70% of the CLBW when G = 0 (typically 310MHz).

In the AD9611, R_F is internal and has a value of 1kΩ; this design helps reduce the effect of stray capacitances and makes it easier to apply the amplifier. The low input impedance at the inverting input means all of the input signal voltage is impressed across R1; this causes a direct voltage-to-current conversion to take place.

Using only the feedback resistor within the unit means *the gain of the AD9611 can be set by varying only R1.*

APPLYING THE AD9611 OP AMP

In applying the AD9611 op amp, there are certain precautions which **must** be observed to protect the unit from damage:

1. Shorting either power supply input pin (Pins 9/10 or Pins 1/12) to the output (Pin 11) will destroy the device.
2. Shorting the output (Pin 11) to ground will destroy the device; no internal protection is included.

As noted earlier, the noninverting input of the AD9611 operational amplifier is a high impedance. This requires that it be driven from a low-impedance source, or connected to a low impedance when used in the inverting mode. Driving this input from a high impedance will reduce bandwidth. Feedback resistor R_F is internal to the AD9611 and has been precisely adjusted to allow a wide range of operating conditions. In some instances, the user may want to obtain higher closed-loop gains than those which can be achieved with only the internal feedback resistor.

It is possible to use an external feedback resistor in series with the internal 1kΩ R_F to achieve relatively higher gains, but bandwidth will be reduced. Table I lists typical bandwidths at G = −5 with varying amounts of feedback resistance. In this listing, the R_F which is shown is the total resistance, including the internal 1kΩ.

Value of R_F	−3dB Bandwidth
1kΩ	280MHz
1.5kΩ	175MHz
2kΩ	135MHz
2.5kΩ	125MHz

Table I

Good layout practices are always crucial to realize the full potential of the AD9611. A massive ground plane is strongly recommended. The ground plane provides a low impedance path for all power supply and signal currents, and suppresses EMI.

Ceramic 0.1μF decoupling capacitors should be placed as close to the specified pins shown in Figures 2 and 3 as possible; preferably, the distance should be less than 0.1 inch. The (10μF) tantalum capacitors for additional decoupling of each power supply should be placed within one inch of their specified pins.

Run lengths must be kept as short as possible; if the signal path must be longer than two or three inches, use terminated coaxial cable and/or microstrip techniques. Impedance mismatches will cause signal reflections and system distortion.

Output impedance of the driving source should equal $R_{MATCH} \| R1$ (inverting mode) or R_{MATCH} (noninverting mode). A suggested layout is shown on the last page of this data sheet.

Parasitic capacitance associated with ZIF (and other) device sockets will severely degrade the performance of the AD9611; if sockets **must** be used, individual pin sockets for each lead are strongly encouraged.

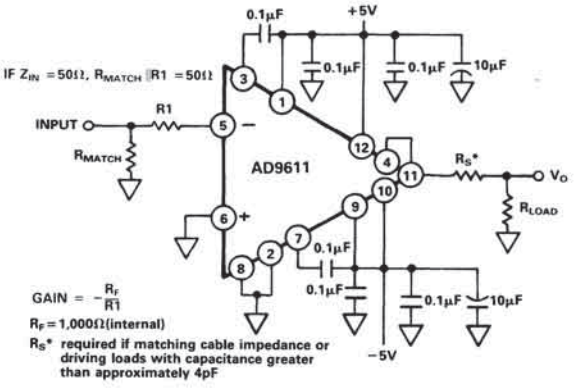


Figure 2. AD9611 Inverting Operation

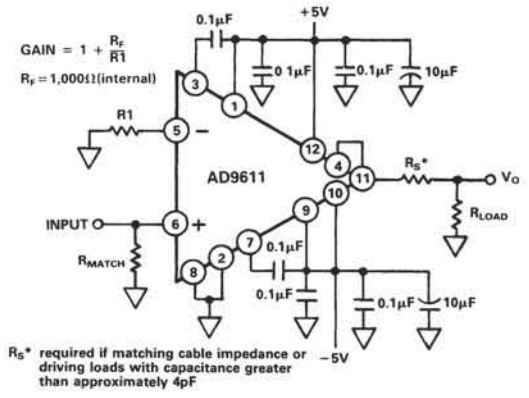


Figure 3. AD9611 Noninverting Operation

The best high-frequency performance of the AD9611 is achieved when total output capacitance (C_L) is at a minimum. Realistically, this is not always possible; but performance can be improved if a series resistor is used at the output of the amplifier, as shown in Figure 4.

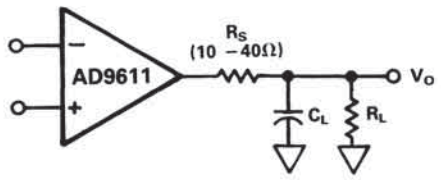


Figure 4. Isolating Capacitive Loads

The unit will drive capacitive loads without appreciable degradation in either settling time or pulse fidelity. For driving capacitive loads >8pF (if R_L = 50Ω) and >4pF (if R_L = 500Ω), isolation resistor R_S should be connected in series with the AD9611 output.

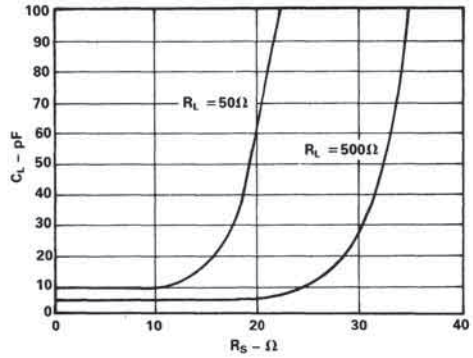


Figure 5. Output Capacitance vs. Compensation

Isolating the capacitive load from the amplifier's output is particularly useful when driving flash A/D converters.

REDUCING OUTPUT VOLTAGE DRIFT

The expected dc error at the output of the AD9611 is a function of input offset voltage (V_{IO}), and inverting and noninverting bias currents (I_{B-} and I_{B+}). The calculation is the same as it would be for conventional amplifiers.

Bias currents vary inversely with temperature and typically track to within 10% of each other at high temperatures (+25°C to +125°C); and within 30% at low temperatures (−55°C to +25°C).

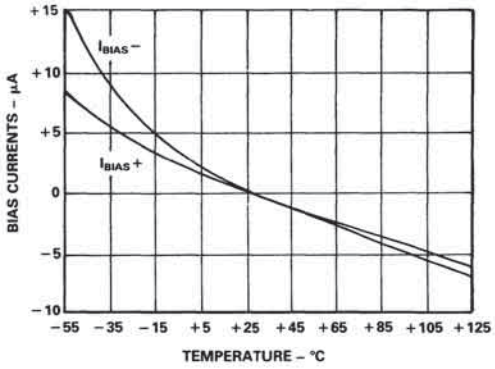


Figure 6. Bias Currents vs. Temperature

Output offset voltage drift (V_{OD}) in the inverting mode can be markedly reduced, especially at high temperatures, by inserting a resistor (R2) between the noninverting input (Pin 6) and ground. This connection is shown in Figure 7.

For this configuration, output offset voltage can be determined as follows:

$$V_O = V_{IO}\left(1 + \frac{R_F}{R1}\right) + I_{B+}(R2)\left(1 + \frac{R_F}{R1}\right) - I_{B-}(R_F)$$

where:

R1 = gain-setting resistor
R_F = internal feedback resistor (1kΩ)
R2 = R1||R_F
$C_S \geq (16{,}200/R2)$pF

A shunt capacitor (C_S) must be connected in parallel with R2 when using this technique to maintain the amplifier's maximum bandwidth, stability, and low-noise performance. The value of the shunt is shown above.

As an example, assume the AD9611 is set up for a gain of −5; R1 should be 200Ω; R2 should be 167; and C_S should be 97pF. Resistor R2 reduces V_{OD} by indirectly nulling the bias current drifts. The reduction in V_{OD} is dramatically reduced from what it would be by simply grounding Pin 6. At high gain settings, the reduction in V_{OD} becomes relatively less because V_{IO} starts to dominate.

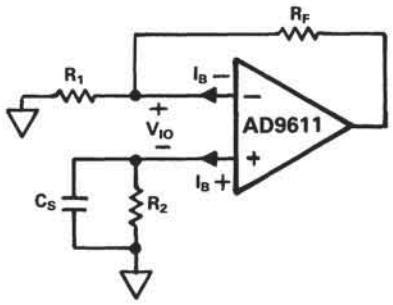
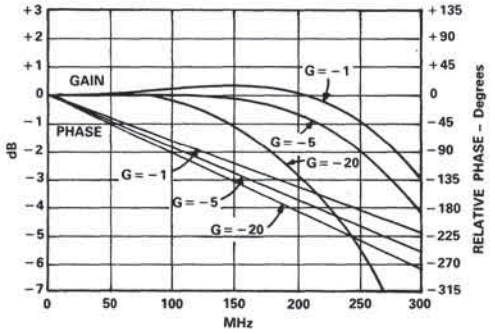


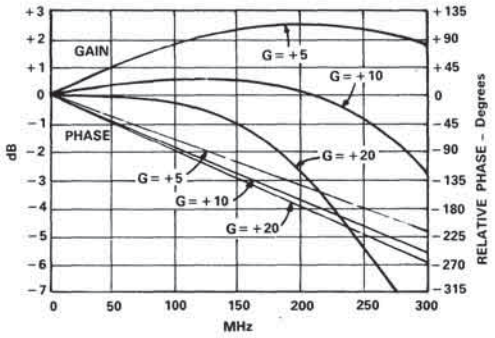
Figure 7. Reducing Offset Drift

AD9611 PERFORMANCE

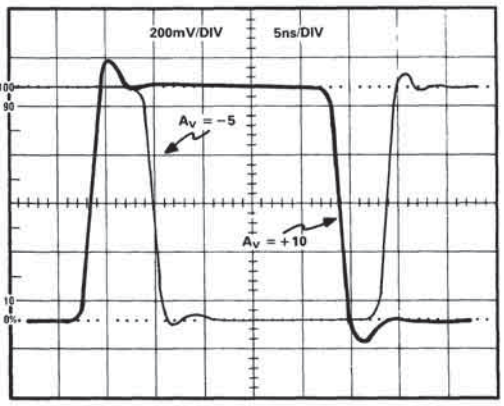
The following graphs and drawings provide additional information on the performance of the AD9611 transimpedance operational amplifier. The data which are shown are based on typical characteristics.



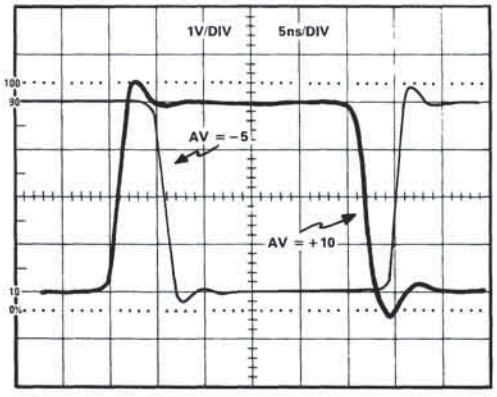
Gain and Phase vs. Frequency – Inverting



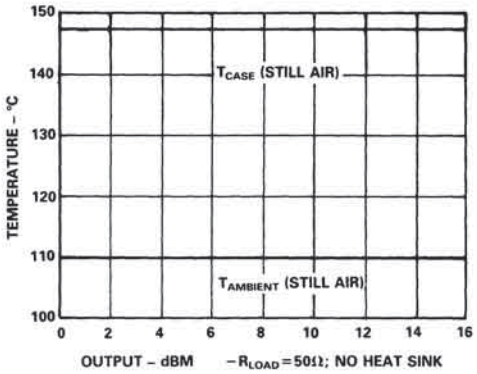
Gain and Phase vs. Frequency – Noninverting



Small-Signal Pulse Response



Large-Signal Pulse Response

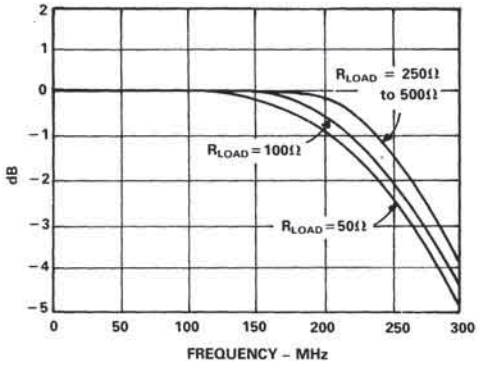


Maximum Temperatures vs. Output Power

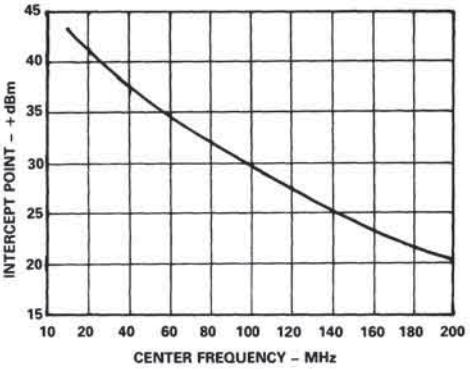
TEMPERATURE vs. OUTPUT POWER

The chart above illustrates an important characteristic of the AD9611 amplifier. A proprietary design feature of the output stage assures a constant case temperature regardless of the amount of output power. This is in marked contrast to most conventional amplifiers, in which increasing amounts of power raise the case temperature of the device as junction temperature increases.

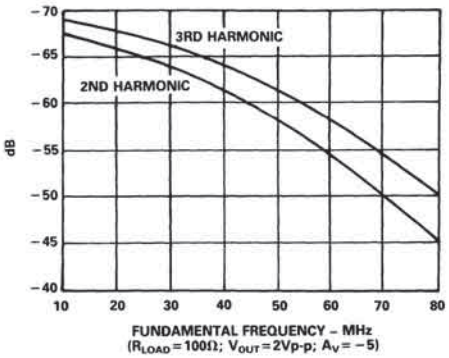
This unique feature of the unit means that no heat sinking is required in still air at ambient temperatures as high as +110°C; with air flow of 500 LFPM, the device can be operated to +125°C before heat sinking is necessary.



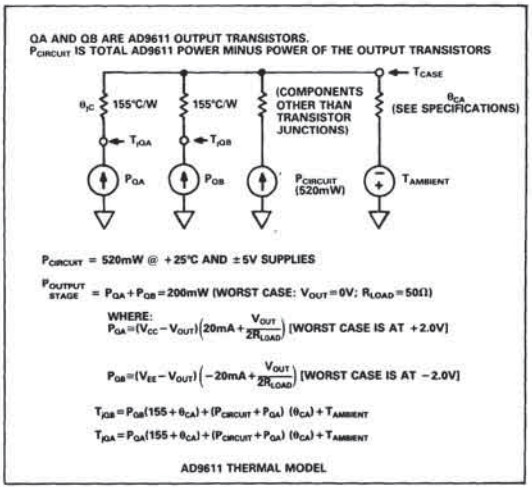
Bandwidth vs. R_{LOAD} ($A_V=-5$)



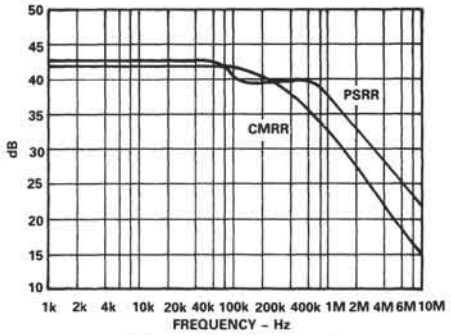
3rd Order Two-Tone Intermod Intercept (Gain = −5; $R_{LOAD}=50\Omega$)



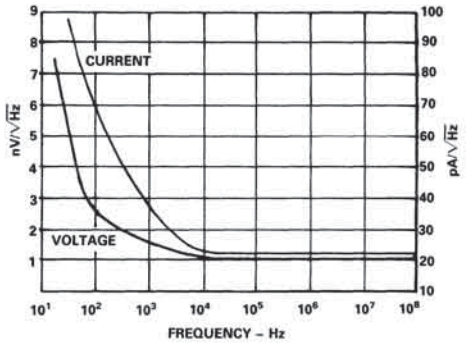
Harmonics vs. Frequency



AD9611 Thermal Model



AD9611 CMRR and PSRR



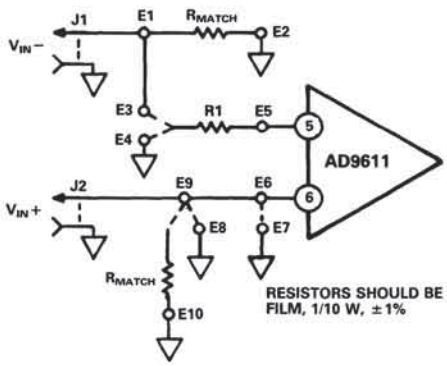
Noise vs. Frequency

AD9611 LAYOUT INFORMATION

The suggested layout of the AD9611 shown below is based on the proven performance of the AD9611 Evaluation Board. The user is urged to use a similar layout when incorporating the amplifier into the system in which it will operate.

In the layout, resistors are film; 0.1W; ±1%; 50ppm. Capacitors C1 and C2 are tantalum; 10μF; 20%; 35V. C3 – C8 are ceramic; 0.1μF; 20%; 50V. Connectors J1 – J3 are Amphenol BNC type; pin sockets are available from Amp as part number 6-330808-0 (closed end) or part number 6-330808-3 (open end).

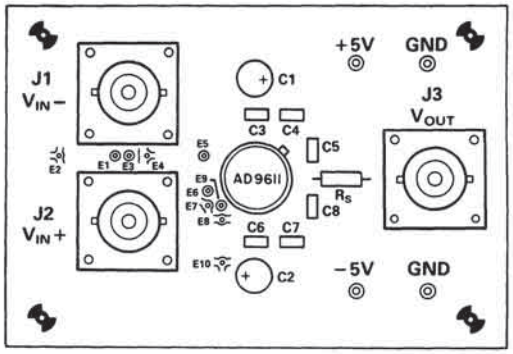
The input connections shown below are based on the layout of the evaluation board. Refer to Figure 2 (inverting operation) and Figure 3 (noninverting operation) for schematic details.



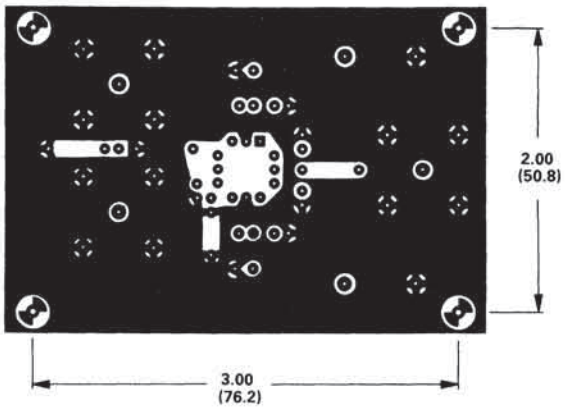
Suggested Layout Input Connections

Operating Mode	Connect	Between
Inverting	R_{MATCH}	E1 and E2
	R1	E3 and E5
	Strap	E6 and E7
	Strap	E8 and E9
Noninverting	R1	E4 and E5
	R_{MATCH}	E9 and E10

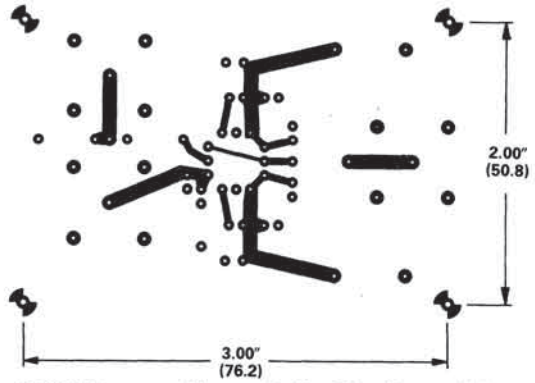
Table II.



AD9611 Suggested Layout Component Side, Viewed from Top



AD9611 Suggested Layout Component Side (Top) Viewed from Top



AD9611 Suggested Layout Solder Side (Bottom) Viewed from Top

ANALOG DEVICES

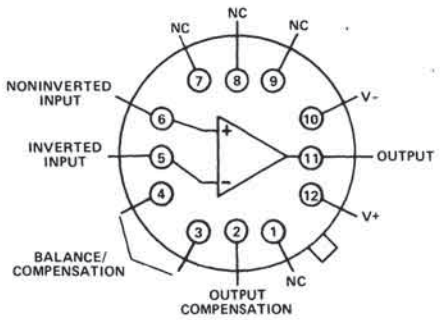
Ultrafast FET Operational Amplifiers

ADLH0032G/ADLH0032CG

FEATURES
- 2nd Source; Replaces All LH0032G
- High Slew Rate; 500V/μs
- Wide 70MHz Bandwidth
- Operation Guaranteed -55°C to +125°C (ADLH0032G)
- High Input Impedance of $10^{12}\,\Omega$
- 2mV Input Offset Voltage

APPLICATIONS
- ADC and SHA Input Buffers
- High Speed Integrators
- Video Amplifiers

ADLH0032G/ADLH0032CG PIN CONFIGURATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The ADLH0032G and ADLH0032CG are high slew rate, high input impedance, differential operational amplifiers, suitable for numerous applications in high-speed signal processing. These second-source devices are the same in every characteristic as other LH0032G/LH0032CG amplifiers.

Featuring a wide 70MHz bandwidth, high input impedance ($10^{12}\,\Omega$), and high output drive capacity, the ADLH0032G and ADLH0032CG have already been designed into such applications as summing amplifiers in high-speed DACs, Buffer Amps in ADCs and high-speed SHAs, as well as other applications normally reserved for special purpose video amplifiers.

The ADLH0032G is guaranteed over the extended temperature range from -55°C to +125°C, while the commercial grade ADLH0032CG is guaranteed from -25°C to +85°C. Both devices are packaged in a TO-8 metal can package.

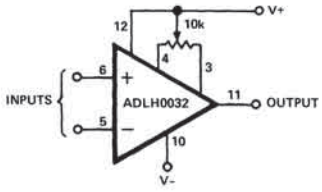


Figure 1. Offset Null

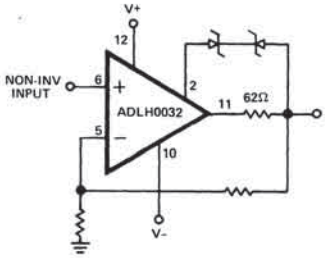


Figure 2. Output Short Circuit Protection

SPECIFICATIONS

Model		ADLH0032G, ADLH0032CG
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage		±18V
Power Dissipation		See Characteristic Curves
Differential Input Voltage		±30V
Input Voltage		$\pm V_S$
Operating Temperature Range	ADLH0032G	−55°C to +125°C
	ADLH0032CG	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10sec)		300°C

Parameter	Conditions	ADLH0032G Min	ADLH0032G Typ	ADLH0032G Max	ADLH0032CG Min	ADLH0032CG Typ	ADLH0032CG Max	Units
DC ELECTRICAL CHARACTERISTICS[1]								
Input Offset Voltage[2]	T_J = +25°C		2	5 10		5	15 20	mV
Input Offset Current[2]	T_J = +25°C		5	25 25		10	50 5	pA nA
Input Bias Current[2]	T_J = +25°C		10	100 50		25	200 15	pA nA
Average Offset Voltage Drift			25	50		25	50	µV/°C
Large Signal Voltage Gain	V_{OUT} = ±10V, F = 1kHz, R_L = 1kΩ, T_C = +25°C	60	70		60	70		dB
	V_{OUT} = ±10V, R_L = 1kΩ, F = 1kHz	57			57			dB
Input Voltage Range		±10	±12		±10	±12		V
Output Voltage Swing	R_L = 1kΩ	±10	±13.5		±10	±13		V
Power Supply Rejection Ratio	ΔV_S = ±10V	50	60		50	60		dB
Common Mode Rejection Ratio	ΔV_{IN} = 10V	50	60		50	60		dB
Supply Current	T_C = +25°C		18	20		20	22	mA
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	A_V = +1, ΔV_{IN} = 20V	350	500		350	500		V/µs
Settling Time to 1% of Final Value	A_V = −1, ΔV_{IN} = 20V		100			100		ns
Settling Time to 0.1% of Final Value	A_V = −1, ΔV_{IN} = 20V		300			300		ns
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V		8	20		8	20	ns
Small Signal Delay Time	A_V = +1, ΔV_{IN} = 1V		10	25		10	25	ns
MTBF								
Meantime Between Failures	1.0608×10^7							hours

NOTES
[1] These specifications apply for V_S = ±15V and −55°C to +125°C for the ADLH0032G and −25°C to +85°C for the ADLH0032CG.
[2] Due to high speed automatic test techniques employed these parameters are correlated to junction temperature.
[3] These specifications apply for V_S = ±15V, R_L = 1kΩ, T_C = +25°C.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range	Package Option*
ADLH0032CG	−25°C to +85°C	TO-8 (H-12A)
ADLH0032G	−55°C to +125°C	TO-8 (H-12A)

*See Section 16 for package outline information.

POWER SUPPLY DECOUPLING

The ADLH0032G/ADLH0032CG, like most high-speed circuits, are sensitive to stray capacitances and layout. Power supplies should be bypassed as near to ±V (Pins 10 and 12) as possible, using low inductance capacitors such as 0.01μF disc ceramics. Components for compensation should also be located close to the appropriate pins to reduce stray capacitances. A large ground plane area for low-impedance ground paths is highly recommended.

HEAT SINKING

The ADLH0032G/ADLH0032CG are specified for operation without any heat sink. Since internal power dissipation does create a significant temperature rise, improved bias current performance can be achieved by using a small heat sink such as the Thermalloy 2241 or equivalent. Since the case of the ADLH0032G/ADLH0032CG has no internal connection, it may be electrically connected to the heat sink. This, however, will affect the stray capacitances to all pins, therefore requiring adjustment of all circuit compensation values.

INPUT CAPACITANCE

Inverting Input:

For optimum performance, the inverting input should be compensated by a small capacitance, around 10pF, across the feedback resistor. This is because the 5pF input capacitance may cause significant time constants with high-value resistors. The capacitor value may be changed somewhat depending on the effects of layout and closed loop gain.

Noninverting Input:

To divert leakage currents away from the noninverting input and to reduce the effective input capacitance, it is desirable to bootstrap the case and/or a guard conductor to the inverting input. The resulting input capacitance of a unity gain follower configured this way will be less than 1 picofarad.

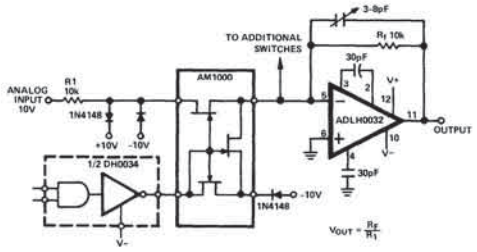


Figure 3. Current Mode Multiplexer

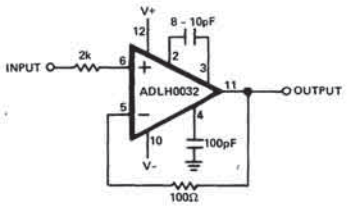


Figure 4. Unity Gain Follower

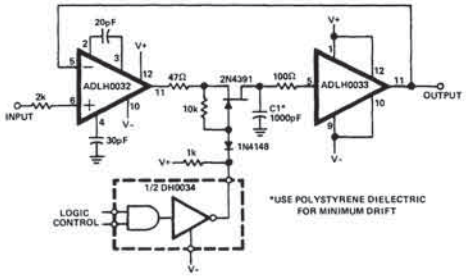
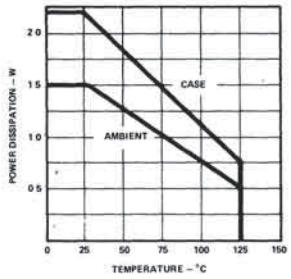
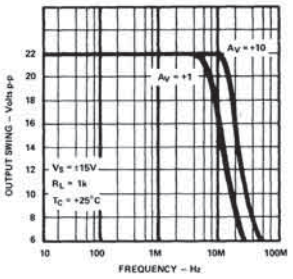


Figure 5. High Speed Sample and Hold

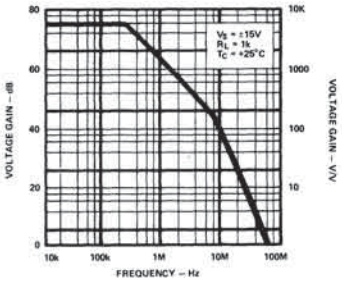
Typical Performance Curves



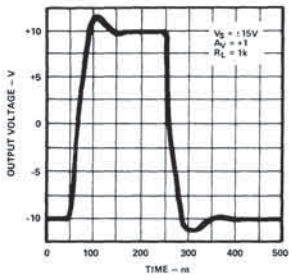
Maximum Power Dissipation



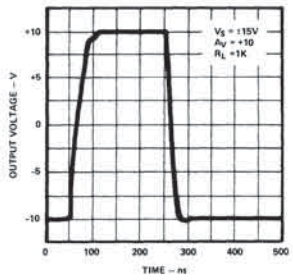
Large Signal Frequency Response



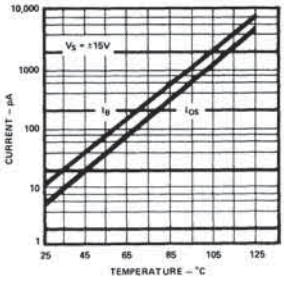
Open Loop Frequency Response



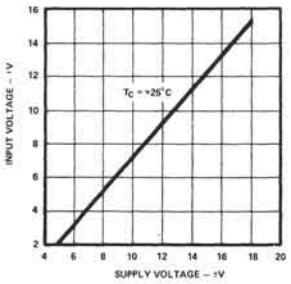
Large Signal Pulse Response



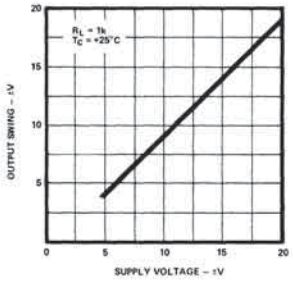
Large Signal Pulse Response



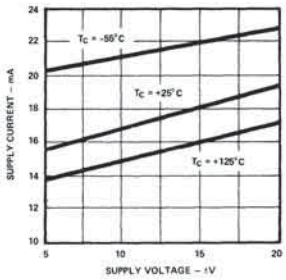
Input Bias and Offset Current vs. Temperature



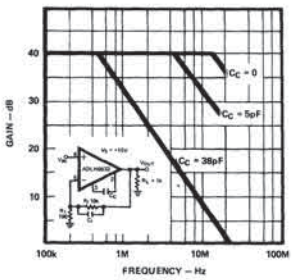
Input Voltage Range



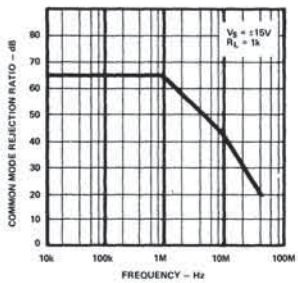
Output Swing



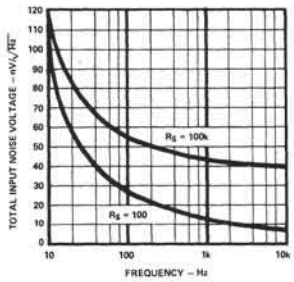
Supply Current vs. Supply Voltage



Closed Loop Frequency Response



Common Mode Rejection Ratio vs. Frequency



*Total Input Noise Voltage vs. Frequency**
**Includes Contribution From Source Resistance*

ANALOG DEVICES

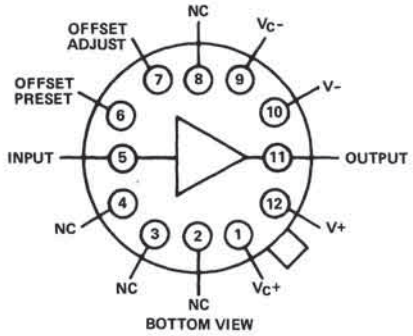
High Speed Buffer Amplifiers

ADLH0033G/ADLH0033CG

FEATURES
- 2nd Source—Replaces All LH0033G Series
- Wide Bandwidth—dc to 100MHz
- High Slew Rate—1500V/μs
- Operates on Single or Dual Power Supplies
- Operation Guaranteed -55°C to +125°C (ADLH0033G)
- High 10^{11} Ω Input Impedance

APPLICATIONS
- High-Speed Line Drivers
- Video Impedance Transformation
- High-Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive

ADLH0033G/ADLH0033CG
OUTLINE AND PIN DESIGNATIONS



GENERAL DESCRIPTION

The ADLH0033G and ADLH0033CG are superhigh speed (1500V/μs slew rate) and high input impedance (10^{11} Ω) buffer amplifiers, designed to replace all LH0033 series amplifiers in applications such as high-speed line drivers or as high impedance buffers for fast A/D converters and comparators.

The ADLH0033G is guaranteed over the temperature range of -55°C to +125°C, while the commercial grade ADLH0033CG is guaranteed over the range of -25°C to +85°C.

Guaranteed operation over temperature of the ADLH0033G is achieved by using specially selected junction FET's and the latest state-of-the-art laser trimming techniques. They are available in the industry standard 12 pin TO-8 metal can.

OPERATION WITHIN AN OP AMP LOOP

When using the ADLH0033G/ADLH0033CG as a current booster or isolation buffer with op amps such as LH0032, 118, 741, etc., an isolation resistor of at least 47Ω must be used between the op amp's output and the input of the ADLH0033G.

HEAT SINKING

To assure maximum output drive capability of the ADLH0033G/ADLH0033CG over temperature, heat sinks should be used. The cases are electrically isolated from the circuit and thus may be connected to system grounds.

POWER SUPPLY BYPASSING

To prevent oscillation, power supply bypassing is recommended. Use low-inductance ceramic disc caps, keeping lead lengths as short as possible (1/4" to 1/2" max from device package), connected between ground plane and each supply lead. Use one or two 0.1μF caps in parallel with a 4.7μF tantalum for best results.

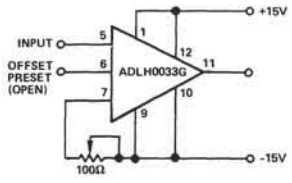


Figure 1. Offset Adjustment

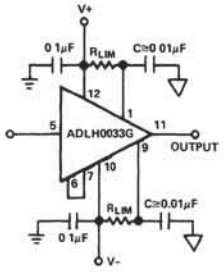


Figure 2. Short Circuit Protection Using Current Limiting Resistors (R_{LIM})

SPECIFICATIONS

	ADLH0033G	ADLH0033CG

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ – V–)		40V
Maximum Power Dissipation (see curves)		1.5W
Maximum Junction Temperature		175°C
Input Voltage		Equal to Supplies
Continuous Output Current		±100mA
Peak Output Current		±250mA
Operating Temperature	ADLH0033G	–55°C to +125°C
	ADLH0033CG	–25°C to +85°C
Storage Temperature Range		–65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

		ADLH0033G			ADLH0033CG			
Parameter	Conditions	min	typ	max	min	typ	max	Units
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	T_C = 25°C		0.1	0.15		0.15		nA
				10			5	nA
Input Impedance	R_L = 1kΩ	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Voltage Gain	V_{IN} = 1V rms, f = 1kHz, R_L = 1kΩ, R_S = 100kΩ	0.96	0.98	1.0	0.96	0.98	1.0	V/V
Output Offset Voltage	R_S = 100kΩ, T_C = 25°C		5	10		12	20	mV
	R_S = 100kΩ			15			25	mV
Output Offset Voltage TC	R_S = 100kΩ		50	100		50	100	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz		6	10		6	10	Ω
	R_S = 100kΩ, R_L = 1kΩ							
Output Voltage Swing	R_L = 1kΩ	±12	±13		±12	±13		V
	R_L = 100Ω, T_C = 25°C	±9			±9			V
Supply Current	V_{IN} = 0V, V_S = ±15V		20	25		21	25	mA
Power Consumption	V_{IN} = 0V, V_S = ±15V		600	660		630	720	mW
AC ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1kΩ)								
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms		100			100		MHz
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Rise Time	ΔV_{IN} = 0.5V		2.9		5	3.2	5	ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5		ns
Harmonic Distortion	f>1kHz		<0.1			<0.1		%
MTBF								
Meantime Between Failure	1.962×10^7							hours
PACKAGE OPTION[3]								
TO-8 (H-12A)		ADLH0033G			ADLH0033CG			

NOTES

[1] Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, –15V applied to pins 9 and 10, and pin 6 connected to pin 7.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the ADLH0033G, and $-25°C \leq T_C \leq +85°C$ for the ADLH0033CG. Typical values shown are for T_C = 25°C.

[3] See Section 16 for package outline information.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0033CG	–25°C to +85°C
ADLH0033G	–55°C to +125°C

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling, stray capacitance, and the like.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical.

OFFSET ADJUSTMENT

The ADLH0033G/ADLH0033CG are factory trimmed for output voltage offsets well within the guaranteed limits, thereby eliminating the need to calibrate each device individually. To use this feature, simply connect Pin 6 (OFFSET PRESET) to Pin 7 (OFFSET ADJUST).

When it is desirable to eliminate any errors due to output offsets, the circuit of Figure 1 may be used to adjust these errors to zero.

SHORT CIRCUIT PROTECTION

The circuit of Figure 2 is used to protect the ADLH0033G/ADLH0033CG from short circuits on the output. The value of R_{LIM} is determined by the following:

$$R_{LIM} \cong \frac{V+}{I_{sc}} = \frac{V-}{I_{sc}}$$

Where I_{sc} = Output Current under short circuit conditions ≤100mA.

Note that output voltage swing will also be somewhat limited in this configuration; however, decoupling of Pins 1 and 9 through disc type capacitors to ground as shown in Figure 2 will restore full output swing for transient pulses.

OPERATION WITH ASYMMETRICAL SUPPLIES

Since Symmetrical Power Supplies may not always be desirable or available, the ADLH0033G/ADLH0033CG is designed to operate on Asymmetrical Supplies. This causes an apparent output offset; however, this is because of the amplifier's gain of less than unity. To accurately predict the output voltage shift due to Asymmetrical Supplies, use the following formula:

$$A_{VO} \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\ (V+ - V-)$$

Where A_V = No Load Voltage Gain, typically 0.99
V+ = Positive Supply Voltage
V- = Negative Supply Voltage

Of course, these apparent offsets may be adjusted to zero by using the circuit shown in Figure 1, OFFSET ADJUSTMENT.

CAPACITIVE LOADING

The ADLH0033G/ADLH0033CG have been designed to drive capacitive loads of several thousand picofarads (such as coaxial cable) without oscillation. In these applications, peak current resulting from (C X dv/dt) should be limited below the absolute maximum peak current rating of ±250mA.

Also, power dissipation due to driving capacitive loads plus standby power should be kept below the total power rating of 1.5W.

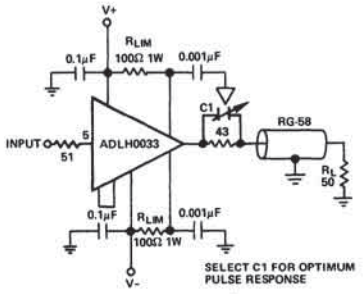


Figure 3. Coaxial Cable Drive

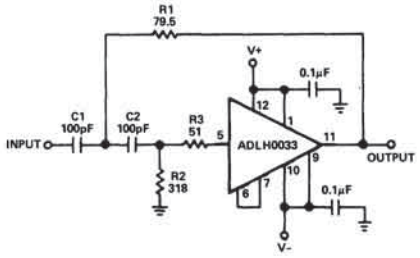


Figure 4. Wideband Two Pole High Pass Filter

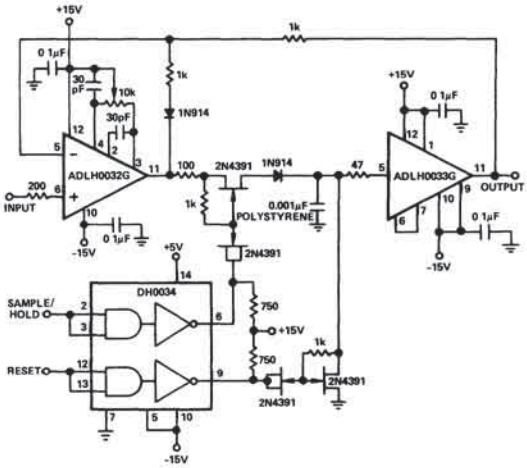


Figure 5. High Speed Peak Detector

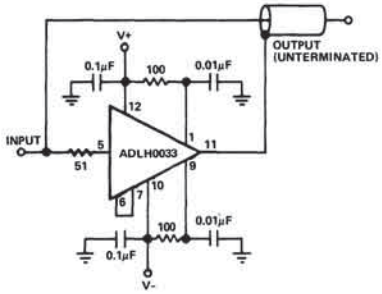
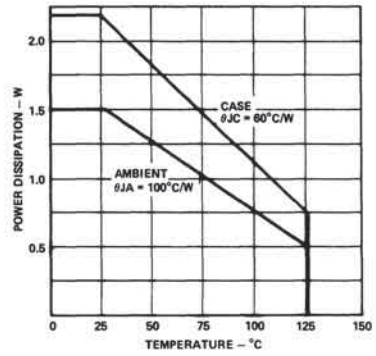
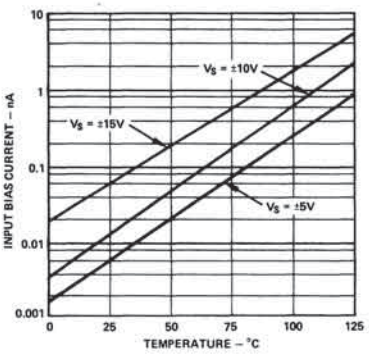


Figure 6. High Speed Shield/Line Driver

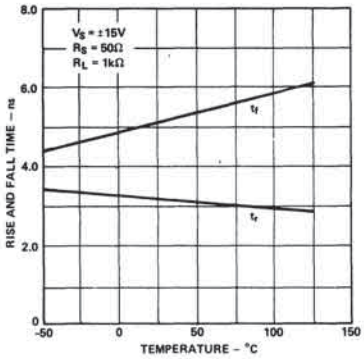
Typical Performance Curves



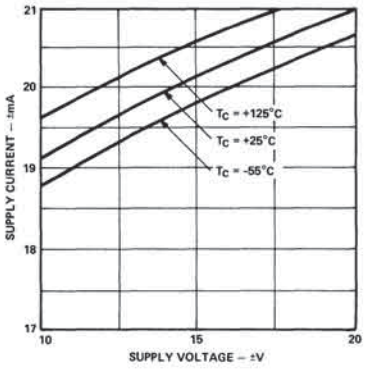
Power Dissipation vs Temperature



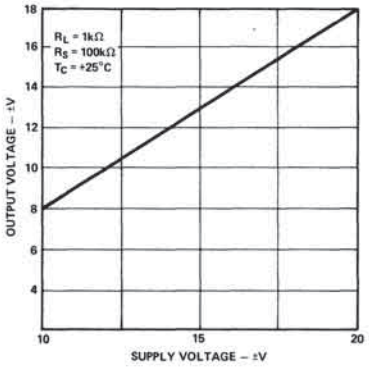
Input Bias Current vs Temperature



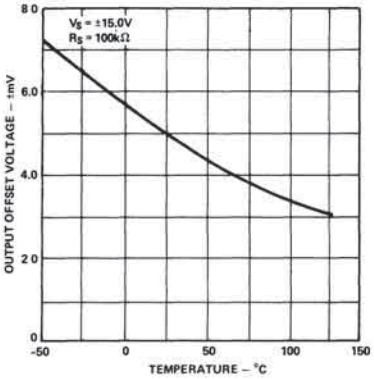
Rise and Fall Time vs Temperature



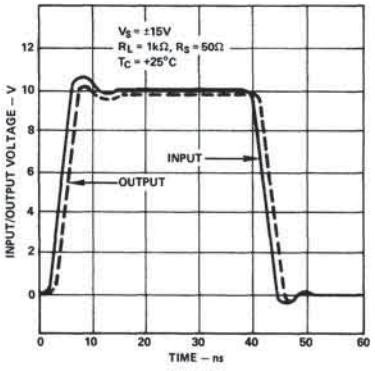
Supply Current vs Supply Voltage



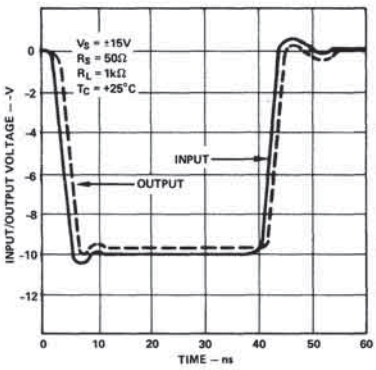
Output Voltage vs Supply Voltage



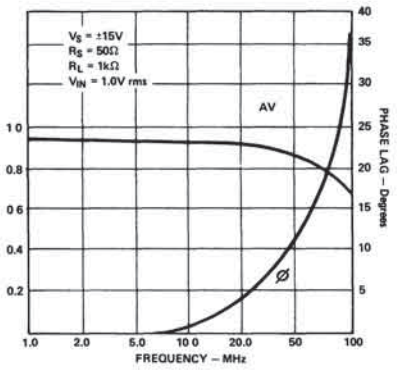
Output Offset Voltage vs Temperature



Positive Pulse Response



Negative Pulse Response



Frequency Response

Ultralow Offset Voltage Op Amp

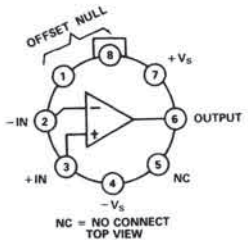
AD OP-07

FEATURES

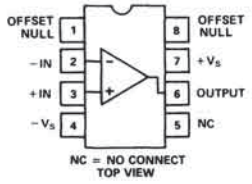
Ten Times More Gain than Other OP-07 Devices (3.0M min)
Ultralow Offset Voltage: 10μV
Ultralow Offset Voltage Drift: 0.2μV/°C
Ultrastable vs. Time: 0.2μV/°C
Ultralow Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common-Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets
Military Parts and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip, Small Outline or TO-99 Hermetic Metal Can
Available in Wafer-Trimmed Chip Form

AD OP-07 CONNECTION DIAGRAMS

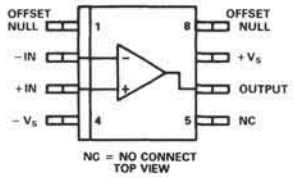
TO-99 (H) Package



Plastic Mini-DIP (N) Package and Cerdip (Q) Package



Small Outline (R) Package



PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed-loop gain applications. Typical input offset voltages as low as 10μV, typical bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C (typ) and long-term stability of 0.2μV/month (typ) eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common-mode input voltage range (±13V, min) common-mode rejection ratio (typically up to 126dB) and high differential input impedance (50MΩ typ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the industrail grades are also available in plastic 8-pin mini-DIPs and small outline packages.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultralow offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultralow input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

Model		AD OP-07E			AD OP-07C			AD OP-07D		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**2,000**	5,000		**1,200**	4,000		**1,200**	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	**±12.5**	±13.0		**±12.0**	±13.0		**±12.0**	±13.0	
		±12.0	±12.8		**±11.5**	±12.8		**±11.5**	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**75**		60	**150**		60	**150**
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift										
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	**3.8**		0.8	**6.0**		0.8	**6.0**
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8	35		12	50		12	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	**±4.0**		±1.8	**±7.0**		±2.0	**±12**
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35		18	50		18	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{INCM}		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±13.0**	±14.0		**±13.0**	±14.0		**±13.0**	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common-Mode Rejection Ratio	CMRR	**106**	123		**100**	120		**94**	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	**4.0**		3.5	**5.0**		3.5	**5.0**
Power Consumption	P_D		90	**120**		105	**150**		105	**150**
			6.0	**9.0**		6.0	**9.0**		6.0	**9.0**
Rejection Ratio	PSRR	**94**	107		**90**	104		**90**	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTIONS[3]										
Small Outline (R-8)						AD OP-07CR				
Plastic Mini-DIP (N-8)			AD OP-07EN			AD OP-07CN			AD OP-07DN	
Cerdip (Q-8)			AD OP-07EQ			AD OP-07CQ			AD OP-07DQ	
TO-99 (H-08A)			AD OP-07EH			AD OP-07CH			AD OP-07DH	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, the AD OP-07A offset voltage is guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested. 90% of units meet this specification.

[3]See Section 16 for package outline information.

AD OP-07A			AD OP-07				
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Test Conditions**	**Units**
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L = 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	25		30	75	Note 1	μV
	25	**60**[1]		60	**200**[1]	T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz	μV p-p
	10.3	18.0		10.3	18.0	$f_O = 10Hz$	nV/√Hz
	10.0	13.0		10.0	13.0	$f_O = 100Hz$	nV/√Hz
	9.6	11.0		9.6	11.0	$f_O = 1kHz$	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz	pA p-p
	0.32	0.80		0.32	0.80	$f_O = 10Hz$	pA/√Hz
	0.14	0.23		0.14	0.23	$f_O = 100Hz$	pA/√Hz
	0.12	0.17		0.12	0.17	$f_O = 1kHz$	pA/√Hz
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		$V_{CM} = \pm CMVR$	dB
106	123		**106**	123		$V_{CM} = \pm CMVR$, T_{min} to T_{max}	dB
	3.0	**4.0**		30	**4.0**	$V_S = \pm 15V$	mA
	90	**120**		90	**120**	$V_S = \pm 15V$	mW
	6.0	**8.4**		6.0	**8.4**	$V_S = \pm 3V$	mW
100	110		**100**	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		**94**	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
−55		+125	−55		+125		°C
AD OP-07AQ AD OP-07AH			AD OP-07Q AD OP-07H				

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

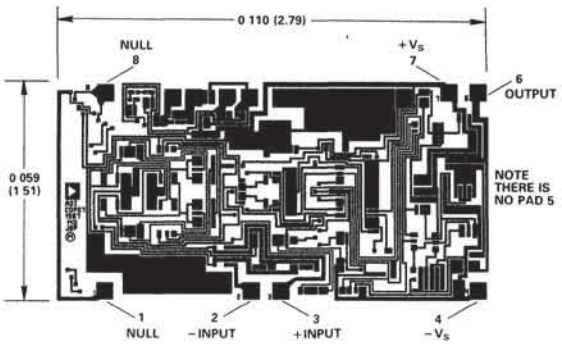
Supply Voltage . . . . . ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-07A, AD OP-07 . . . . . −55°C to +125°C
AD OP-07E, AD OP-07C, AD OP-07D . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
Note 1: Maximum package power dissipation vs. ambient temperature.

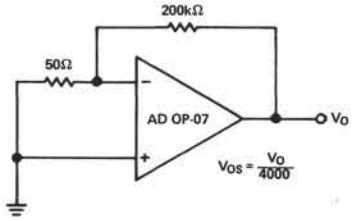
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

CHIP DIMENSIONS AND BONDING DIAGRAM

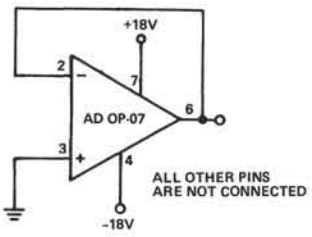
Dimensions shown in inches and (mm).



THE AD OP-07 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM FOR PRECISION HYBRIDS CONSULT THE FACTORY FOR DETAILS



Offset Voltage Test Circuit



Burn-In Circuit

AD OP-07 ORDERING GUIDE

Model	Package Option	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-07EH	TO-99	0 to +70	75	1.3
AD OP-07EN	Mini-DIP	0 to +70	75	1.3
AD OP-07EQ	Cerdip	0 to +70	75	1.3
AD OP-07CH	TO-99	0 to +70	150	1.8
AD OP-07CN	Mini-DIP	0 to +70	150	1.8
AD OP-07CQ	Cerdip	0 to +70	150	1.8
AD OP-07CR	Small Outline	0 to +70	150	1.8
AD OP-07DH	TO-99	0 to +70	150	2.5
AD OP-07DN	Mini-DIP	0 to +70	150	2.5
AD OP-07DQ	Cerdip	0 to +70	150	2.5
AD OP-07AH	TO-99	−55 to +125	25	0.6
AD OP-07AQ	Cerdip	−55 to +125	25	0.6
AD OP-07H	TO-99	−55 to +125	75	1.3
AD OP-07Q	Cerdip	−55 to +125	75	1.3

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

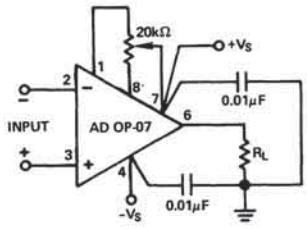


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

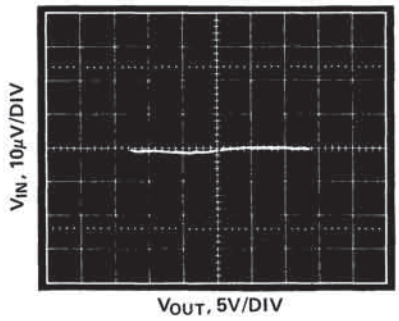
The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

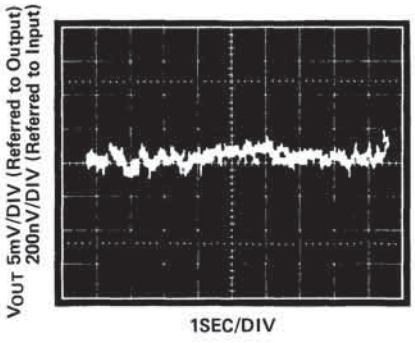
Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

2

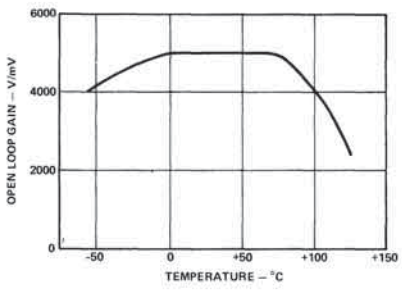
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



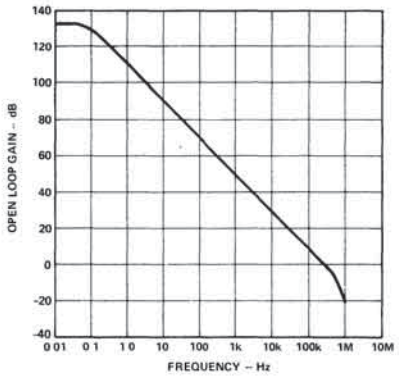
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

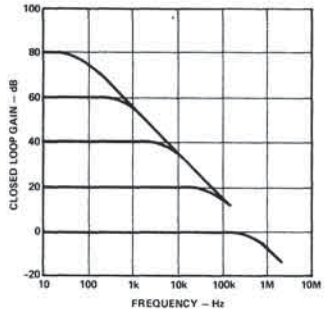


Open Loop Gain vs. Temperature

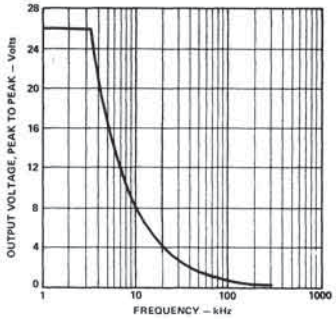


Open Loop Frequency Response

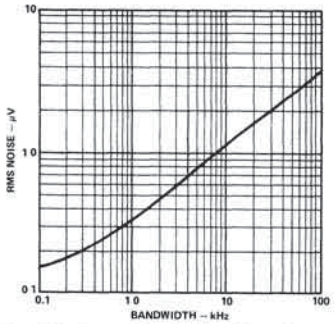
Typical Performance Curves



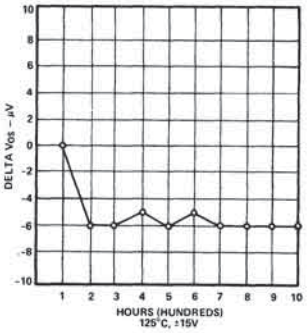
Closed Loop Response for Various Gain Configurations



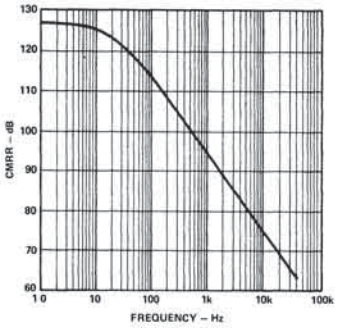
Maximum Undistorted Output vs. Frequency



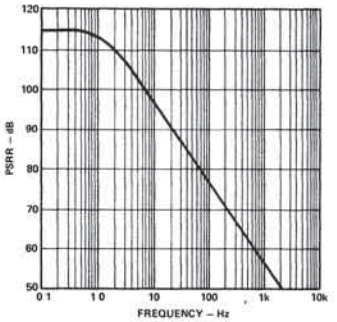
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



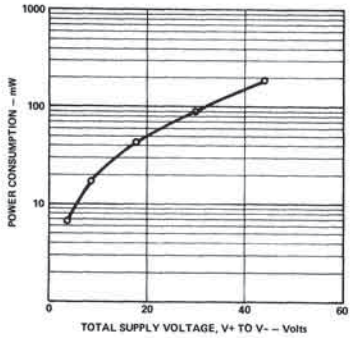
Offset Voltage vs. Time



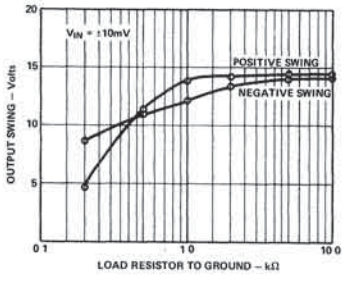
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Ultralow-Noise Precision Op Amp

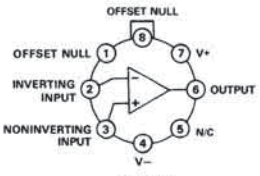
AD OP-27

FEATURES

- Ultralow Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
- Ultralow Offset Voltage Drift: 0.2μV/°C
- High Offset Stability Over Time: 0.2μV/month
- High Slew Rate: 2.8V/μs
- High Gain Bandwidth Product: 8MHz
- Low Offset Voltage: 10μV
- High CMRR: 126dB Over ±11V Input Voltage Range
- Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets
- Military Grade and Plus Parts Available
- 8-Pin Plastic Mini-DIP, Cerdip or TO-99 Hermetic Metal Can
- Available in Wafer-Trimmed Chip Form

AD OP-27 CONNECTION DIAGRAMS

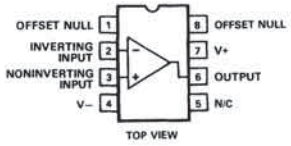
TO-99 (H) Package



TOP VIEW

NOTE PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs (typ) slew rate and an 8MHz (typ) gain bandwidth product are possible without sacrificing dc accuracy. Long-term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ±10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ±20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the E, F and G grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultralow input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

Model		AD OP-27G			AD OP-27F			AD OP-27E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	5.0	8.0		5.0	8.0		5.0	8.0	
Slew Rate	SR	1.7	2.8		1.7	2.8		1.7	2.8	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85
PACKAGE OPTIONS[3]										
Plastic Mini-DIP (N-8)			AD OP-27GN			AD OP-27FN			AD OP-27EN	
Cerdip (Q-8)			AD OP-27GQ			AD OP-27FQ			AD OP-27FQ	
TO-99 (H-08A)			AD OP-27GH			AD OP-27FH			AD OP-27EH	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[3]See Section 16 for package outline information.

Specifications subject to change without notice.

AD OP-27C			AD OP-27B			AD OP-27A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
5.0	8.0		5.0	8.0		5.0	8.0			MHz
1.7	2.8		1.7	2.8		1.7	2.8		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	nV/√Hz
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	nV/√Hz
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	nV/√Hz
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	pA/√Hz
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	pA/√Hz
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	pA/√Hz
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-27CQ AD OP-27CH			AD OP-27BQ AD OP-27BH			AD OP-27AQ AD OP-27AH				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-27A, AD OP-27B, AD OP-27C . −55°C to +125°C
AD OP-27E, AD OP-27F, AD OP-27G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

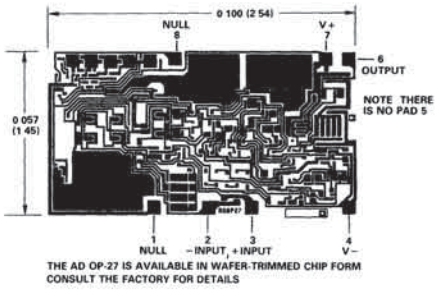
NOTES:
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD OP-27 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM
CONSULT THE FACTORY FOR DETAILS

AD OP-27 ORDERING GUIDE

Model	Package Option*	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-27GH	TO-99	−25 to +85	100	1.8
AD OP-27GN	Mini-DIP	−25 to +85	100	1.8
AD OP-27GQ	Cerdip	−25 to +85	100	1.8
AD OP-27FH	TO-99	−25 to +85	60	1.3
AD OP-27FN	Mini-DIP	−25 to +85	60	1.3
AD OP-27FQ	Cerdip	−25 to +85	60	1.3
AD OP-27EH	TO-99	−25 to +85	25	0.6
AD OP-27EN	Mini-DIP	−25 to +85	25	0.6
AD OP-27EQ	Cerdip	−25 to +85	25	0.6
AD OP-27CH	TO-99	−55 to +125	100	1.8
AD OP-27CQ	Cerdip	−55 to +125	100	1.8
AD OP-27BH	TO-99	−55 to +125	60	1.3
AD OP-27BQ	Cerdip	−55 to +125	60	1.3
AD OP-27AH	TO-99	−55 to +125	25	0.6
AD OP-27AQ	Cerdip	−55 to +125	25	0.6

*See Section 16 for package outline information.

APPLICATION NOTES FOR THE AD OP-27

The AD OP-27 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for optimum AD OP-27 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

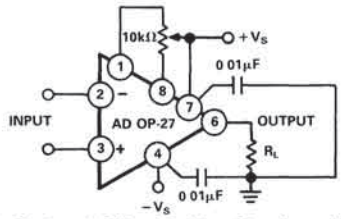


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-27. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature—a temperature close to the device's package.

Output stability with the AD OP-27 is possible with capacitive loads of up to 2000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-27 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

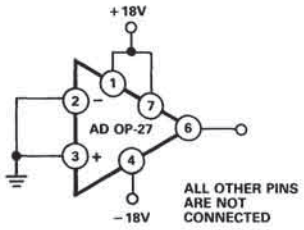


Figure 2. Burn-In Circuit

SLEW RATE DISCUSSION

In unity gain buffer applications with feedback resistances of less than 100Ω where the input is driven with a fast, large (greater than 1V) pulse, the output waveform will appear as in Figure 3.

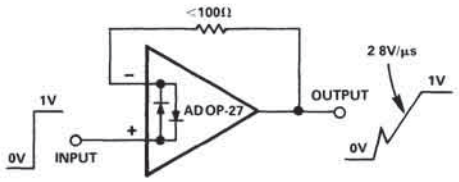


Figure 3. Unity Gain Buffer/Pulsed Operation

During the initial portion of the output slew the input protection back-to-back diodes effectively short the output to the input. A current limited only by the output short circuit protection will be drawn from the source. After the input diodes saturate, the amplifier will slew at its nominal 2.8V/μs. With feedback resistances of more than 500Ω the output is capable of handling the current requirements without limiting (less than 20mA at 10V) and the amplifier will stay in the linear region.

As with all operational amplifiers a feedback resistance of greater than 2kΩ will create a pole with the input capacitance (8pF). Additional phase shift will be introduced and the phase margin will be reduced. A small capacitor (20 to 50pF) in parallel with the feedback resistor will alleviate this problem.

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-27 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

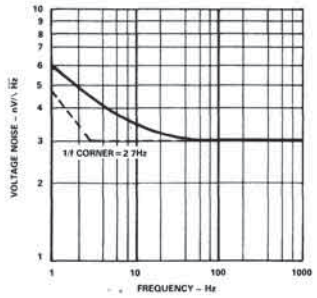
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

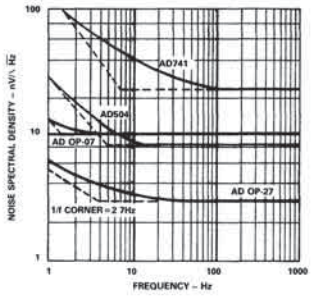
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

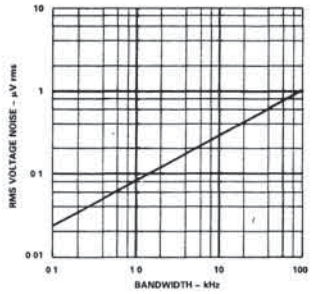
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



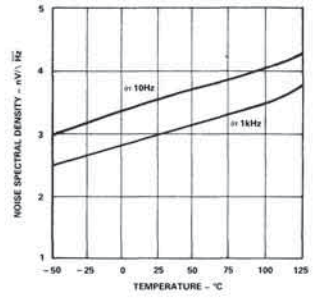
Input Voltage Noise Spectral Density



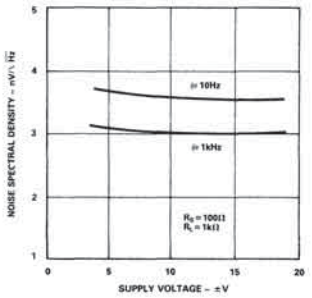
Comparison of Op Amp Input Voltage Noise Spectrums



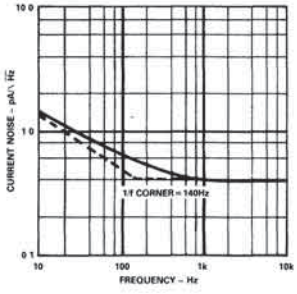
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



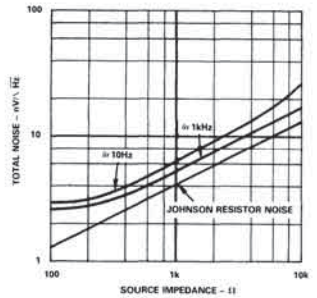
Input Voltage Noise vs. Temperature



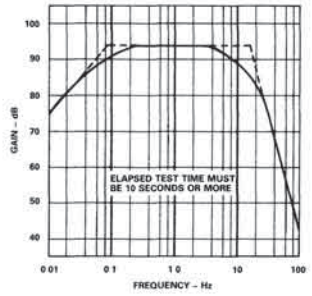
Input Voltage Noise vs. Supply Voltage



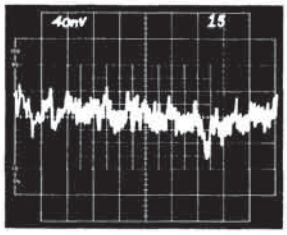
Input Current Noise Spectral Density



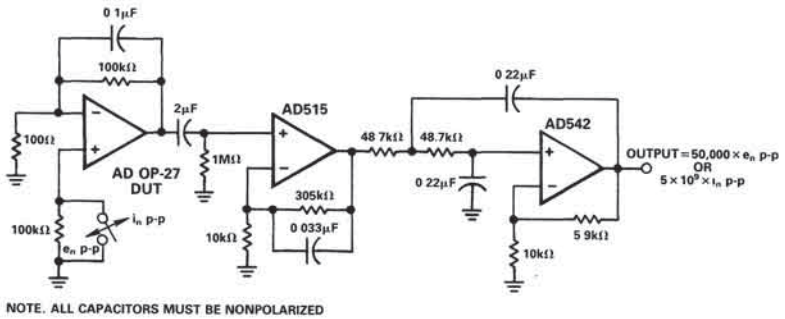
Total Noise vs. Source Impedance



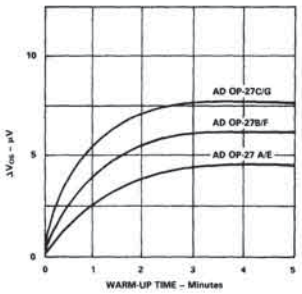
0.1Hz to 10Hz Noise Test Frequency Response



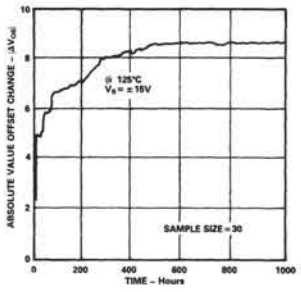
0.1Hz to 10Hz p-p Voltage Noise



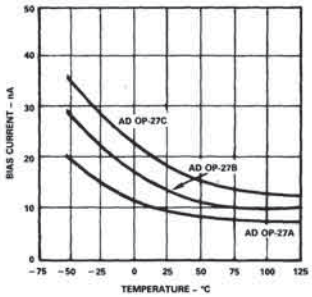
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



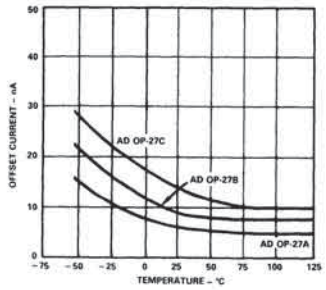
Input Offset Voltage Turn-On Drift vs. Time



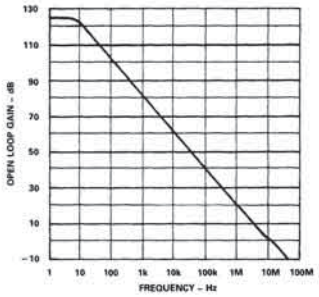
Long Term Offset Stability @ Temperature



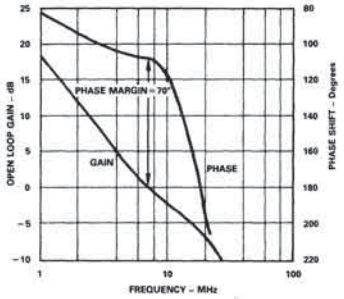
Input Bias Current vs. Temperature



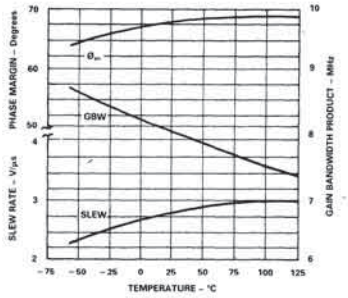
Input Offset Current vs. Temperature



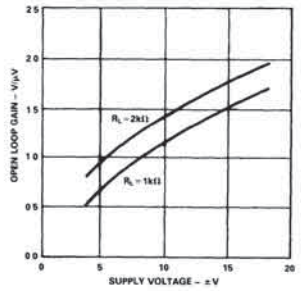
Open Loop Frequency Response



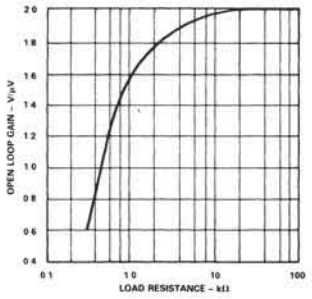
Open Loop Gain and Phase Shift vs. Frequency



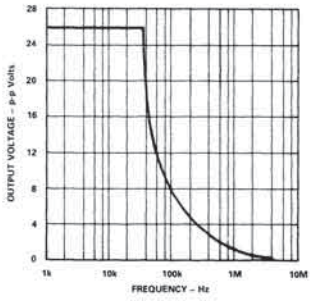
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



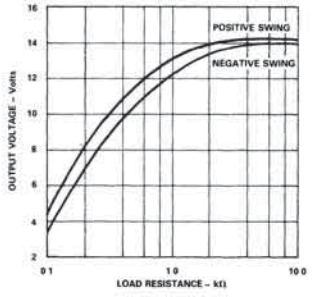
Open Loop Gain vs. Supply Voltage



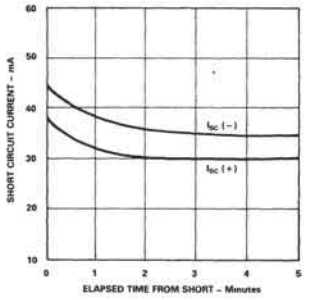
Open Loop Gain vs. Resistive Load



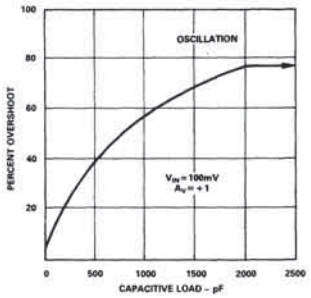
Undistorted Output Swing vs. Frequency



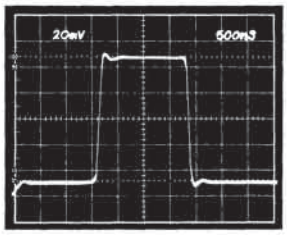
Output Swing vs. Resistive Load



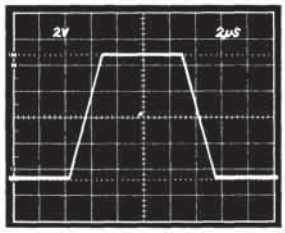
Output Short Circuit Current vs. Time



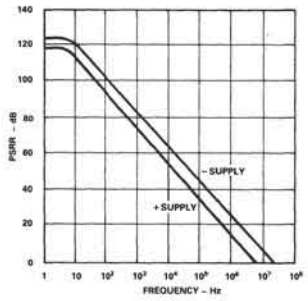
Small Signal Overshoot vs. Capacitive Load



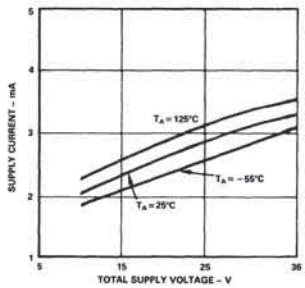
Unity Gain Follower Pulse Response (Small Signal)



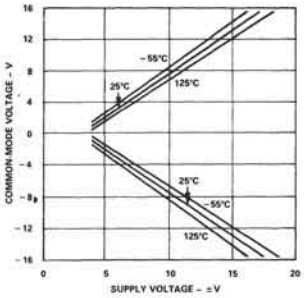
Unity Gain Follower Pulse Response (Large Signal)



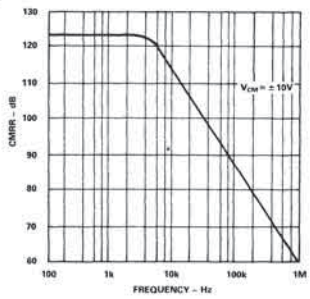
Power Supply Rejection Ratio vs. Frequency



Supply Current vs. Supply Voltage



Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency

Ultralow-Noise, High-Speed Precision Op Amp ($A_{VCL} \geq 5$)

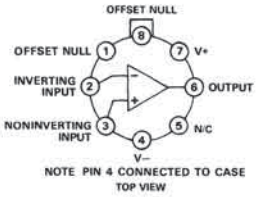
AD OP-37

FEATURES

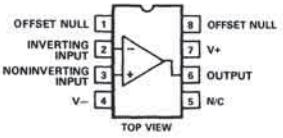
- Ultralow Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
- High Speed: 17V/μs
- High Gain Bandwidth Product: 63MHz
- Ultralow Offset Voltage Drift: 0.2μV/°C
- High Offset Stability Over Time: 0.2μV/month
- Low Offset Voltage: 10μV
- High CMRR: 126dB Over ±11V Input Voltage Range
- Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains ≥ 5
- Military Grade and Plus Parts Available
- 8-Pin Plastic Mini-DIP, Cerdip or TO-99 Hermetic Metal Can
- Available in Wafer-Trimmed Chip Form

AD OP-37 CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package and Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. High-speed accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than or equal to five. This instrumenation grade op amp features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a typical 17V/μs slew rate and a typical 63MHz gain bandwidth product. Long-term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the industrial grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains ≥ 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultralow input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultralow offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

Model		AD OP-37G			AD OP-37F			AD OP-37E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long-Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85
PACKAGE OPTIONS[3]										
Plastic Mini-DIP (N-8)			AD OP-37GN			AD OP-37FN			AD OP-37EN	
Cerdip (Q-8)			AD OP-37GQ			AD OP-37FQ			AD OP-37EQ	
TO-99 (H-08)			AD OP-37GH			AD OP-37FH			AD OP-37EH	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[3]See Section 16 for package outline information.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-37CQ AD OP-37CH			AD OP-37BQ AD OP-37BH			AD OP-37AQ AD OP-37AH				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:

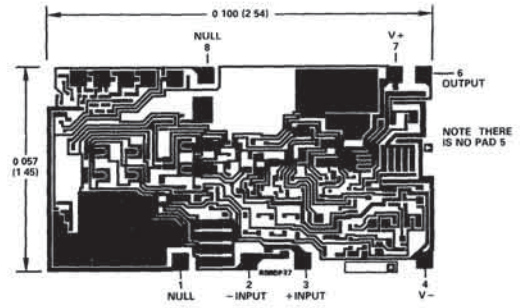
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD OP-37 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM. CONSULT THE FACTORY FOR DETAILS.

AD OP-37 ORDERING GUIDE

Model	Package*	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-37GH	TO-99	−25 to +85	100	1.8
AD OP-37GN	Mini-DIP	−25 to +85	100	1.8
AD OP-37GQ	Cerdip	−25 to +85	100	1.8
AD OP-37FH	TO-99	−25 to +85	60	1.3
AD OP-37FN	Mini-DIP	−25 to +85	60	1.3
AD OP-37FQ	Cerdip	−25 to +85	60	1.3
AD OP-37EH	TO-99	−25 to +85	25	0.6
AD OP-37EN	Mini-DIP	−25 to +85	25	0.6
AD OP-37EQ	Cerdip	−25 to +85	25	0.6
AD OP-37CH	TO-99	−55 to +125	100	1.8
AD OP-37CQ	Cerdip	−55 to +125	100	1.8
AD OP-37BH	TO-99	−55 to +125	60	1.3
AD OP-37BQ	Cerdip	−55 to +125	60	1.3
AD OP-37AH	TO-99	−55 to +125	25	0.6
AD OP-37AQ	Cerdip	−55 to +125	25	0.6

*See Section 16 for package outline information.

APPLICATION NOTES FOR THE AD OP-37

The AD OP-37 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for correct AD OP-37 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

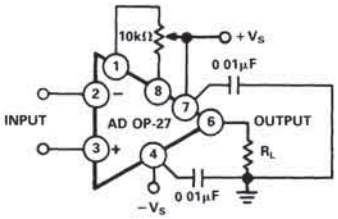


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-37. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature.

Output stability with the AD OP-37 is possible with capacitive loads of up to 1000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop.

Although the AD OP-37 features high-power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to Pins 4 and 7 of the AD OP-37 as possible, to load ground with a good quality 0.01μF ceramic capacitor as shown in Figure 1.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-37 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

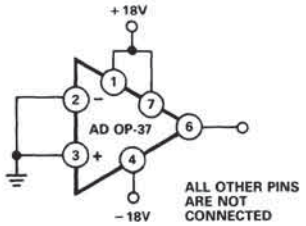


Figure 2. Burn-In Circuit

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-37 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

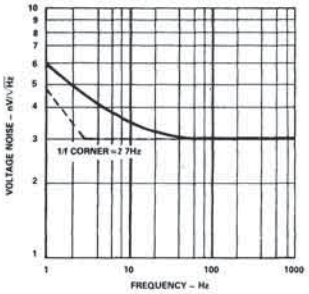
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

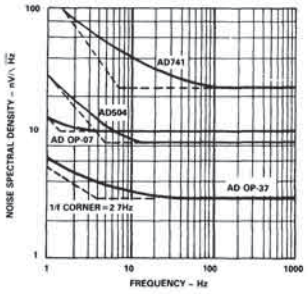
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

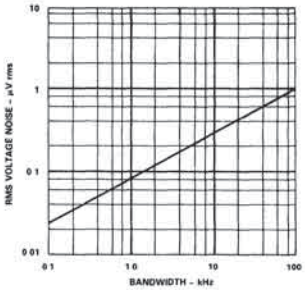
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



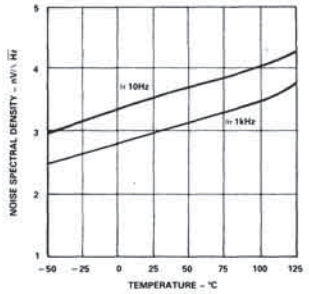
Input Voltage Noise Spectral Density



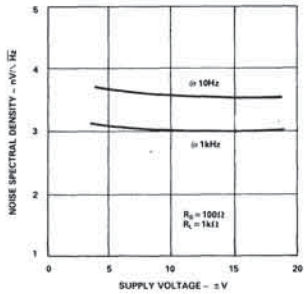
Comparison of Op Amp Input Voltage Noise Spectrums



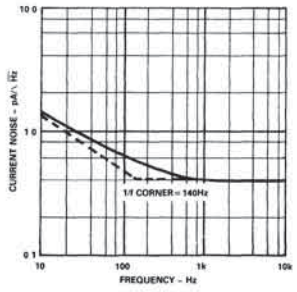
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



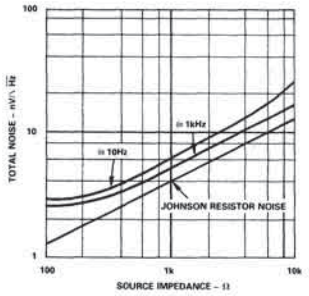
Input Voltage Nose vs. Temperature



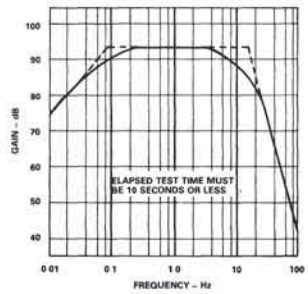
Input Voltage Noise vs. Supply Voltage



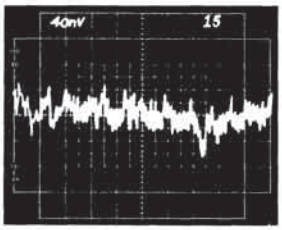
Input Current Noise Spectral Density



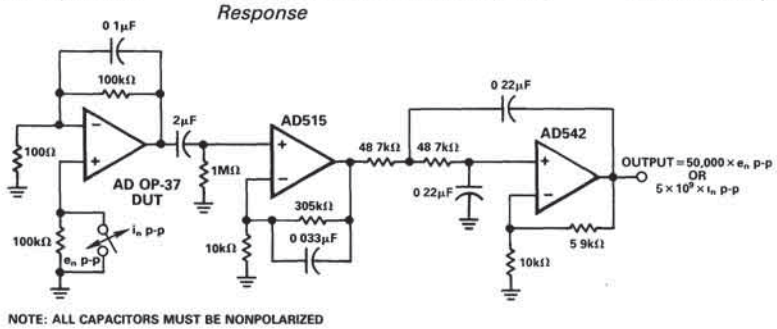
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

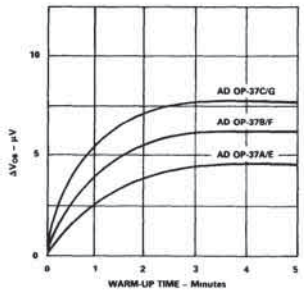


0.1Hz to 10Hz p-p Voltage Noise

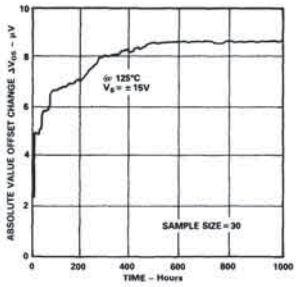


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

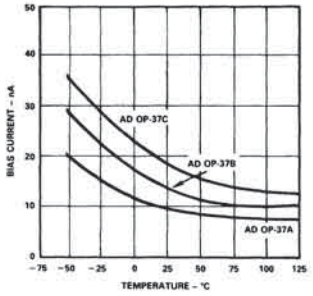
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



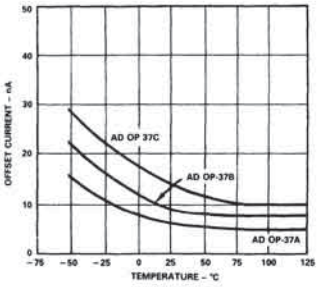
Input Offset Voltage Turn-On Drift vs. Time



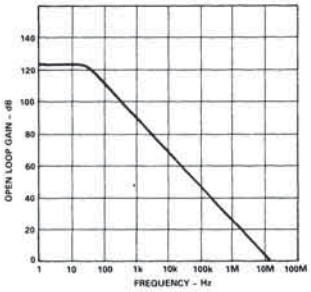
Long Term Offset Stability @ Temperature



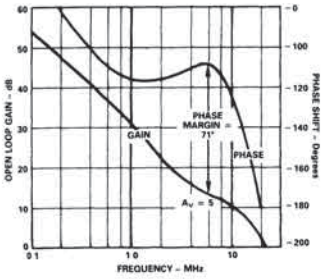
Input Bias Current vs. Temperature



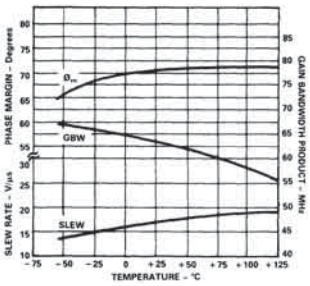
Input Offset Current vs. Temperature



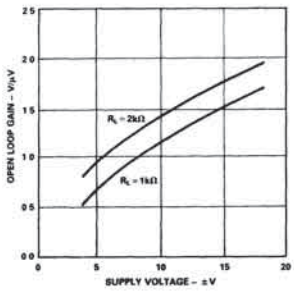
Open Loop Frequency Response



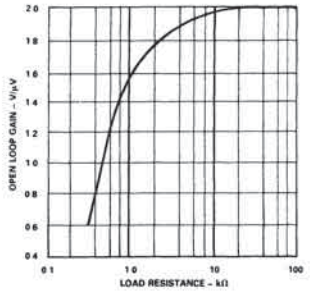
Open Loop Gain and Phase Shift vs. Frequency



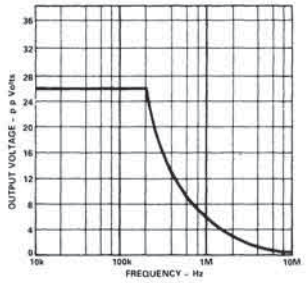
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



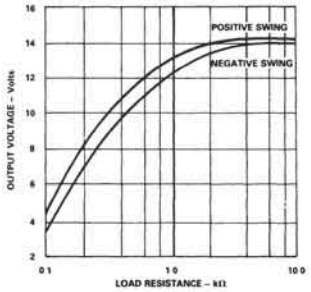
Open Loop Gain vs. Supply Voltage



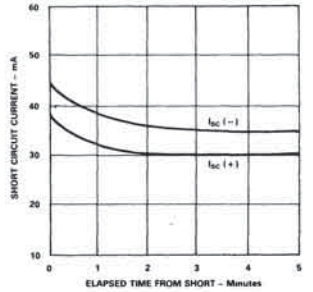
Open Loop Gain vs. Resistive Load



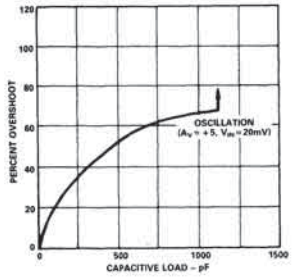
Undistorted Output Swing vs. Frequency



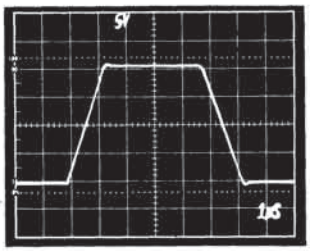
Output Swing vs. Resistive Load



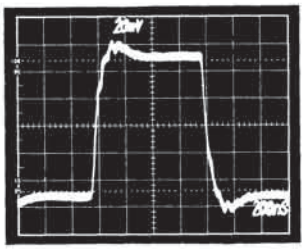
Output Short Circuit Current vs. Time



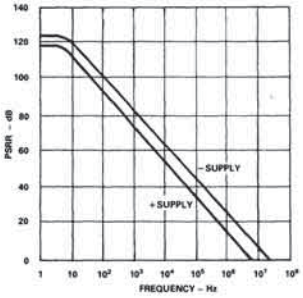
Small Signal Overshoot vs. Capacitive Load



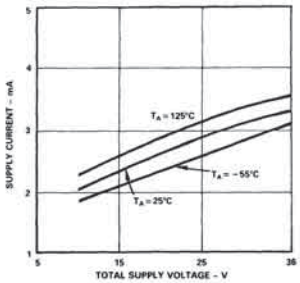
Large Signal Pulse Response (A_V = 5, R_L = 2k)



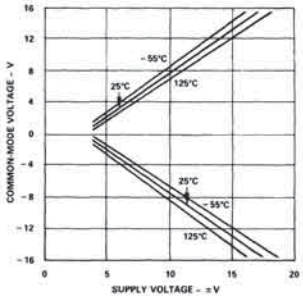
Small Signal Pulse Response (A_V = 5, R_L = 2k)



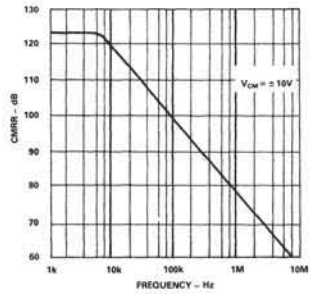
Power Supply Rejection Ratio vs. Frequency



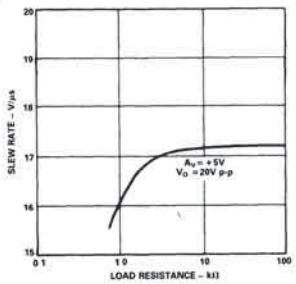
Supply Current vs. Supply Voltage



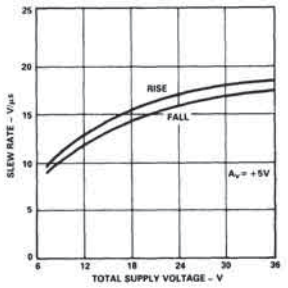
Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency



Slew Rate vs. Resistive Load



Slew Rate vs. Supply Voltage

ANALOG DEVICES

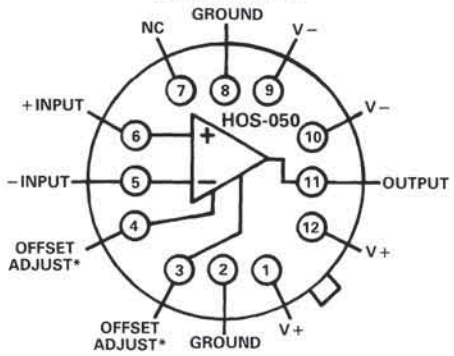
Fast Settling Video Operational Amplifiers

HOS-050/HOS-050A/HOS-050C

FEATURES
- 80ns Settling to 0.1%; 200ns to 0.01%
- 100MHz Gain Bandwidth Product
- 55MHz 3dB Bandwidth
- 100mA Output @ ±10V

APPLICATIONS
- D/A Current Converter
- Video Pulse Amplifier
- CRT Deflection Amplifier
- Wideband Current Booster

HOS-050/A/C PIN DESIGNATIONS
TO-8 PACKAGE



*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.
NC = NO CONNECT

BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-050, HOS-050A, and HOS-050C op amps are very high speed wideband operational amplifiers designed to complement the Analog Devices' lines of high speed data acquisition products. They feature a 100MHz gain bandwidth product; slew rate of 300V/μs; and settling time of 80ns to ±0.1%.

The HOS-050A, HOS-050, and HOS-050C have typical input offset voltages of 10mV, 25mV, and 45mV, respectively.

All models have a rated output of ±100mA minimum, and an exceptional noise spec of only 7μV rms, dc to 2MHz; they are ideally suited for a broad range of video applications.

FAST-SETTLING OP AMPS

At one time, operational amplifiers could be specified according to slew rates, bandwidth, and drive capability; and these parameters would be sufficient. Settling time was not considered until the use of high speed video D/A converters became widespread.

The conversion speed of the D/A can be limited by the settling time of the output amplifier, so it has become essential to select an op amp whose settling time is compatible with the D/A converter.

The increased emphasis on settling time has, in some cases, created a preoccupation with slew rates in the minds of some designers. But slew rate is only one component in establishing settling time.

The amount of overshoot, and the ringing which are present at the end of a step function change also have an effect. These parameters, in turn, are influenced by the bandwidth (or lack of it) when operating the op amp with closed loop gains greater than one.

(continued after Specifications)

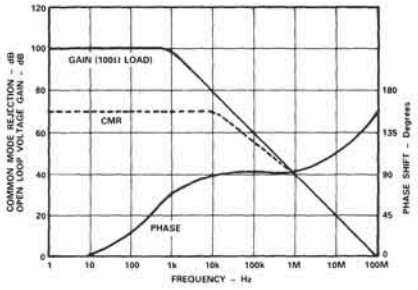


Figure 1. HOS-050 Frequency Response

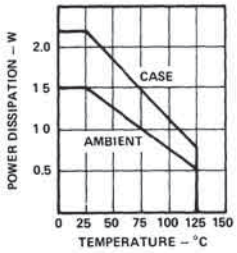


Figure 2. Power Dissipation vs. Temperature

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-050	HOS-050A	HOS-050C
ABSOLUTE MAXIMUM RATINGS			
Supply Voltages (V_S)	±18V	*	*
Power Dissipation	See Figure 2	*	*
Input Voltage	$\pm V_S$	*	*
Differential Input Voltage	$\pm V_S$	*	*
Operating Temperature Range (case)	−55°C to +125°C	*	−25°C to +85°C
Junction Temperature	175°C	*	*
Storage Temperature Range	−65°C to +150°C	*	*
Lead Temperature (soldering, 10 sec.)	300°C	*	*

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100			*			*		dB
Rated Output	R_L = >100Ω										
Voltage		+10/−8			*			*			V
Current											
(not short circuit protected)	R_L = >100Ω		±100			*			*		mA
Voltage	R_L = >200Ω	±10			*			*			V
Input Offset Voltage	Adjustable to Zero										
Initial	@ +25°C		25	35		10	15		45	65	mV
vs. Temperature			50	150		20	35		75	200	μV/°C
vs. Power Supply Voltage			0.5			*			*		mV/V
Input Bias Current											
Initial	@ +25°C		1	2		*	*		*	*	nA
vs. Temperature			Doubles			*			*		/10°C
Input Offset Current											
Initial	@ +25°C		±100			*			*		pA
Input Impedance											
Differential	}In parallel with 5pF		10^{10}			*			*		Ω
Common Mode			10^{10}			*			*		Ω
Input Voltage Range											
Common Mode		±10		±18	*		*	*		*	V
Differential				±18			*			*	V
Common Mode Rejection			70			*			*		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ										
dc to 100kHz			5			*			*		μV rms
dc to 2MHz			7			*			*		μV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω, Load = 100Ω		300			*			*		V/μs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 100Ω		320			*			*		V/μs
Overload Recovery	50% Overdrive		400			*			*		ns
Unity Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100			*			*		MHz
Small Signal Bandwidth, −3dB	A = −1, R_{FF} = R_{FB} = 500Ω		45			*			*		MHz
	A = −1, R_{FF} = R_{FB} = 1000Ω		35			*			*		MHz
	A = −2; R_{FF} = 500Ω, R_{FB} = 1000Ω		35			*			*		MHz
	A = −4, R_{FF} = 250Ω; R_{FB} = 1000Ω		30			*			*		MHz
Output Impedance				<1			*			*	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω, 100Ω load; 10pF capacitance										
	5-volt p-p output		25			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		55			*			*		MHz
	A = 3; R_{FF} = 500Ω; R_{FB} = 1000Ω; 100Ω, 1000Ω, or 2000Ω load; 10pF capacitance										
	10-volt p-p output		17			*			*		MHz
	5-volt p-p output		25			*			*		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued)		HOS-050			HOS-050A			HOS-050C			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FB} = 500Ω; R_{FB} = 2000Ω, 100Ω, 1000Ω, or 2000Ω load/10pF capacitance										
	5-volt p-p output		15			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		40			*			*		MHz
	1-volt p-p output		40			*			*		MHz
Full Power Bandwidth (−3dB)	Output = ±5V, A = −1, R_L = 100Ω		20			*			*		MHz
Settling Time to 0.1%	A = −1, R_{11} = R_{1B} = 500Ω										
Inverting	V_{OUT} = ±5V		100			*			*		ns
(See Figure 5)	V_{OUT} = ±2.5V		80			*			*		ns
Noninverting	A = 2, R_{FT} = R_{1B} = 500Ω Max Load capacitance = 75pF										
	V_{OUT} = ±5V		200			*			*		ns
	V_{OUT} = ±2.5V		135			*			*		ns
Harmonic Distortion (See Figure 9)	A = −1; Load = 1000Ω Signal = 4MHz, 2V output		−63			*			*		dB
Noninverting Harmonic Distortion (See Figure 10)	A = 2, R_{FT} = R_{FB} = 1000Ω, Load = 1000Ω, Signal = 4MHz, 2V output		−59			*			*		dB
Power Supply											
Voltage	Rated performance		±15			*			*		V dc
Voltage	Operating range	±12		±18	*		*	*		*	V dc
Current	Quiescent		±20	±25		*	*		*	*	mA
Power Consumption	Quiescent		0.6			*			*		W
Power Dissipation				1.25			*			*	W
Temperature Range											
Operating (Case)	(See Figure 2 for	−55		+125	*		*	−25		+85	°C
Storage	Derating Information)	−65		+150	*		*	*		*	°C
Meantime Between Failures (MTBF)	MIL-HNBK 217, Ground, Fixed; Case = 70°C				6.27 × 10^6						Hours
Package Option[2] TO-8 (H-12A)			HOS-050			HOS-050A			HOS-050C		

NOTES
*Specification same as HOS-050
[1]Specification for Inverting Mode unless otherwise noted
[2]See Section 16 for package outline information
Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0
Specifications subject to change without notice

PIN DESIGNATIONS

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	−INPUT
6	+INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V

(continued from Features page)

The HOS-050 Series stands up under close scrutiny of these characteristics because of its 100MHz gain bandwidth product. The use of these amplifiers in a wide variety of applications has confirmed their suitability for video circuits.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-050 are generally characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A converter output voltage amplification or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed forward resistor for the op amp.

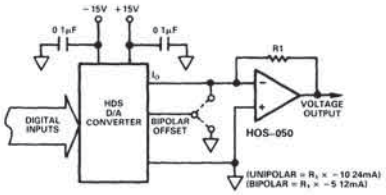


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The HDS Series D/A converters are fast-settling, current output D/As available in 8-, 10-, and 12-bit resolutions. Both TTL and ECL versions are available, and settling times range from 10ns for 8-bit units through 40ns for 12-bit units.

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and bipolar offset grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

An approximation of the total settling time for the D/A op amp combination is calculated by:

$$T_S = \sqrt{T_D^2 + T_O^2}$$

where T_D is D/A settling time and T_O is HOS-050 settling time.

This approximation is valid because both the D/A and the HOS-050 exhibit 6dB/octave roll-off charateristics (single pole response); and the combination of low D/A output capacitance and op amp input capacitance does not materially affect the formula.

The user of the HOS-050 should remember the current flowing in the feedback resistor (R1) must be subtracted from the output available from the HOS-050.

There is a tendency, because of this fact, to use a high value of feedback resistor to assure maximum current drive being available for driving low impedances; but this approach may create undesirable side effects.

Calculating the minimum load that can be driven under two conditions of feedback resistor values will serve to illustrate the difference.

Assume the feedback resistor value is 500Ω. If output voltage of the HOS-050 is 10 volts, and output current is 100mA, minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 20mA} = \frac{10V}{80mA} = 125\Omega \text{ minimum load}$$

where: E_O max = peak voltage needed
I_O max = maximum continuous current HOS-050 can produce
I_{RFB} = current in feedback resistor at peak voltage

Assume the feedback resistor value is 5,000Ω. Minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 2mA} = \frac{10V}{98mA} = 102\Omega \text{ minimum load}$$

Designs which strive for driving a minimum load (by increasing the feedback resistor) can create settling problems because of a fundamental characteristic of op amp circuits . . . the higher the feedback resistance, the slower the system response.

This phenomenon is the result of increased impedance for driving stray capacitances in the circuit employing the op amp, and fixed capacitances in the summing node.

Impedances need to be kept as low as possible consistent with low distortion; and stray capacitances need to be eliminated to the maximum possible extent. A large ground plane structure is recommended to help assure low ground impedances. In addition, 0.1μF ceramic capacitors and 3-10μF tantalum capacitors connected as close as possible to power supply inputs will decrease the potential for parasitic oscillations and other noise signals.

Another argument for limiting the size of the feedback resistor is because of its effect on bandwidth. Bandwidth of the HOS-050 op amp and the value of the feedback resistor are inversely related.

At any given gain of the op amp, the gain setting with the widest bandwidth will be the one which employs the lower value of feedback. As an example, a gain of 1 can be achieved with $R_{FF} = R_{FB} = 500\Omega$; or $R_{FF} = R_{FB} = 1{,}000\Omega$. Small-signal bandwidth for the first combination is typically 45MHz; bandwidth for the second is typically 35MHz.

OFFSET AND GAIN ADJUSTMENT

Figure 4 shows a method of using the HOS-050 op amp which allows adjusting the offset and gain of the output voltage.

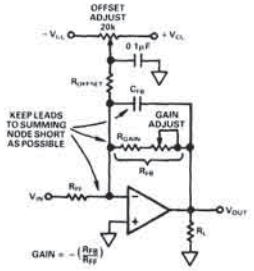


Figure 4. HOS-050 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right)$$

where R_{FB} is the total of R_{GAIN} and Gain Adjust.

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Assume $\pm V_{CC} = \pm 15V$; $R_{GAIN} = 900\Omega$; Gain Adjust = 100Ω; the desired change on the output = ± 1 volt.

Under these conditions, R_{OFFSET} will be $15k\Omega$:

$$R_{OFFSET} = -\left(\frac{15V \times [900 + 100]}{1V}\right)$$

$$R_{OFFSET} = -\left(\frac{15kV}{1V}\right)$$

$$R_{OFFSET} = 15{,}000\Omega$$

Figure 4 shows bipolar output operation. If unipolar output is desired, the appropriate V_{CC} should be removed from the Offset Adjust potentiometer.

The 0.1μF capacitor attached to the wiper arm of the Offset Adjust control isolates the control and helps prevent adjustment noise from appearing on the output of the HOS-050.

C_{FB} can be any value between 0 and 20pF, depending on the value of R_{GAIN}; and should be selected to optimize settling time for the particular circuit layout in which the HOS-050 is being used.

The Gain Adjust control should be a low value, low inductance cermet trimming potentiometer.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-050 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

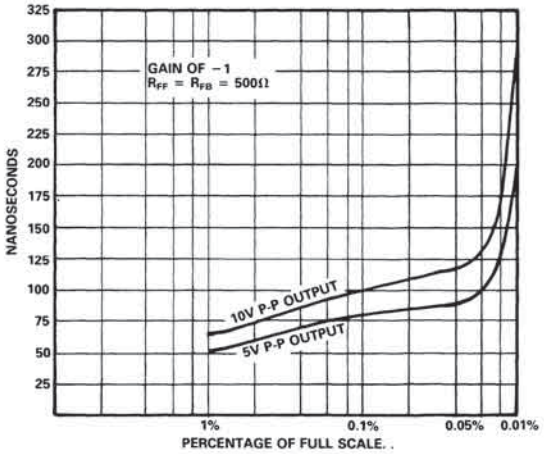


Figure 5. Settling Time – Inverting Mode

SETTLING TIME MEASUREMENT

Although there are some exceptions, most members of industry are in agreement on the description which says settling time is:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

The well-informed user needs to be alert to the consequences of settling time specs which do not meet that description.

This definition encompasses the major components which comprise settling time. They include (1) propogation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for his application.

Figure 6 is the test circuit for measuring settling time to 0.1%. This method creates a "false" summing junction and the error band is observed at that point.

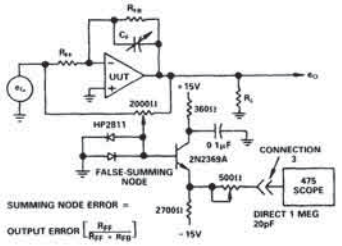


Figure 6. Settling Time Test Circuit for 0.1% Settling

If one were to attempt the measurement at the "true" summing junction of the op amp, the results would be misleading. All scope probes will add capacitance to the input and will change the response of the system. Making the measurement at the output of the amplifier is also impractical, since scope nonlinearities and reading inaccuracies caused by overdriving the scope preclude accurate measurements to the tolerances which are required.

The false summing junction method causes the amplifier to subtract the output from the input; only one-half the actual error appears at the false junction, and it can be measured to the required accuracies.

The false junction is clamped with diodes to limit the voltage excursion appearing at that point. This is necessary because the amplifier will be overdriven and one-half its input voltage will appear at the junction. Without the clamps, the scope used for making the measurement would be overdriven and its recovery time would mask the settling time of the amplifier.

The test circuit for measuring settling time to 0.01%, Figure 7, is simply an extension of the same basic technique. Measuring to the closer tolerance requires additional gain in the circuit driving the oscilloscope.

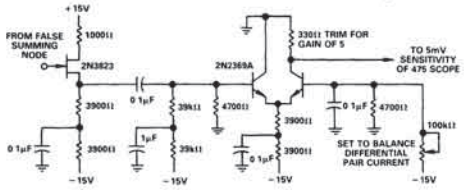


Figure 7. Settling Time Test Circuit for 0.01% Settling

IMPEDANCE MATCHING

The characteristics of the HOS-050 operational amplifier make it an ideal choice for matching the impedances of video circuits to the impedances of transmission lines.

In this application, source and load terminating resistors will cause the output voltage to be halved at the end of the cable

being driven by the op amp. This makes it necessary to set the gain of the circuit to provide twice the desired voltage.

Three different values of resistors and cables are "phantomed" into the figure as examples of possible characteristic impedances which might be used. Figure 8 is *not* meant to imply the HOS-050 can drive three cables simultaneously.

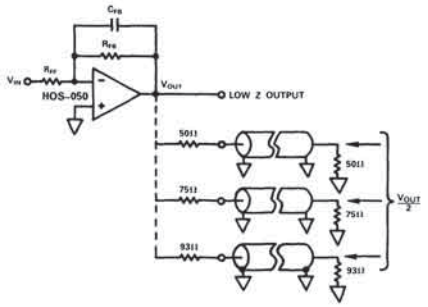


Figure 8. HOS-050 Impedance Matching

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by incresing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The overall input capacitance of the op amp is kept as low as possible in the design; and any mismatch in the capacitance of the two channels appears as an error in the output. Because of the inherently low total input capacitance of the op amp, even a small capacitive mismatch between channels shows up as a large effective error signal.

Decreasing the channel mismatch can be achieved only by complicating the design of the op amp with additional components, and rigorous selection of those components in the manufacturing process.

As a consequence, the mismatch is reduced to the smallest practical value consistent with the economics of producing and using the op amp. But it remains a mismatch, and manifests itself as a difference in performance in the inverting versus noninverting modes.

There are video op amps available at low cost which use a 741-type amplifier for high dc open loop gain in the noninverting channel. The user of these kinds of designs may sometimes gain an economic advantage, but at a high cost in performance. Bandwidths for noninverting applications are often measured in kHz, not MHz, for this approach.

A video op amp is acting as a voltage mode device at both inputs when operating in the noninverting mode. This contrasts with the inverting mode, where it is operating as a current mode device.

The Analog Devices HOS-050 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in many competing units.

The HOS-050 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

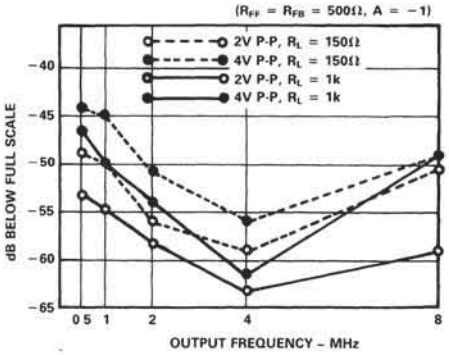


Figure 9. Harmonic Distortion – Inverting

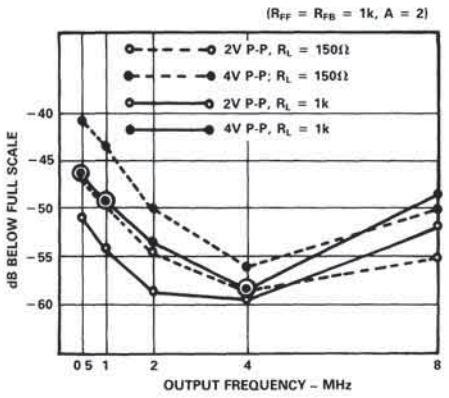


Figure 10. Harmonic Distortion – Noninverting

IN SUMMARY . . . A CAVEAT

Settling time specifications, bandwidth capabilities, harmonic distortion performance, and other parameters for video op amps cannot possibly include all possible situations and applications.

A multitude of seemingly insignificant conditions can have a major impact on the unit and its ability to operate in any given circuit.

The potential user is strongly urged to evaluate the effectiveness of the HOS-050 in the actual circuit in which it will be used. In many instances, the application conditions are different from the conditions used in specifying; there is no substitute for a trial in the proposed circuit to determine if the op amp will provide the desired results.

ANALOG DEVICES

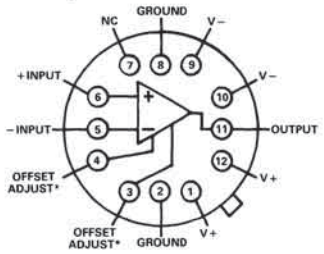
Low Offset, Fast Settling Video Operational Amplifier

HOS-060

FEATURES
<1mV V_{OS}
Low Drift
80ns Settling to 0.1%; 200ns to 0.01%
100mA Output @ ±10V

APPLICATIONS
D/A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

HOS-060 PIN DESIGNATIONS[1]
TO-8 (H-12A) Package



NOTES
[1]SEE SECTION 16 (H-12A) FOR PACKAGE OUTLINE INFORMATION
*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO + 15V

GENERAL DESCRIPTION

The HOS-060 Operational Amplifier is an extension of the proven hybrid technology used in the HOS-050 series of op amps.

The FET input and high-performance characteristics, including wide bandwidth and fast settling, make it useful for a variety of applications in the processing of video signals.

Recent innovations in circuit design have been incorporated into the HOS-060 to make it extremely useful to the designer who needs outstanding performance in current boosting, voltage amplification, impedance matching, or a multiplicity of other high-frequency requirements.

Voltage offset and its temperature coefficient have been dramatically improved in the HOS-060; offset is as low as most high performance monolithic op amps.

The HOS-060 op amp is pin-for-pin compatible with its forerunner HOS-050 and is useable in the same diversity of video requirements. The reader is strongly urged to refer to the six-page data sheet for the HOS-050 op amp to obtain additional insight and details on potential uses for the HOS-060.

The HOS-060 Operational Amplifier package is the industry standard TO-8 metal can and operates over a case temperature range of −55°C to +125°C; the model number for the standard unit is HOS-060SH.

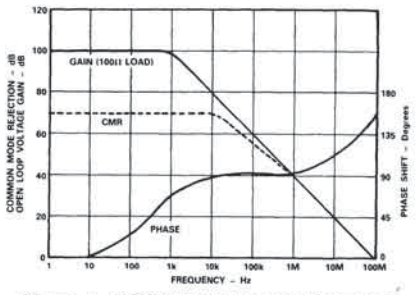


Figure 1. HOS-060 Frequency Response

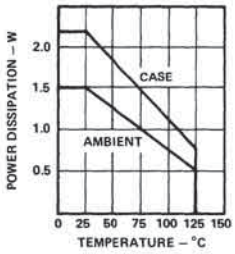


Figure 2. Power Derating

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-060SH
ABSOLUTE MAXIMUM RATINGS	
Supply Voltages (V_S)	±18V
Power Dissipation	See Figure 2
Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Operating Temperature Range (Case)	−55°C to +125°C
Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100		dB
Rated Output					
Current					
(Not Short-Circuit Protected)	R_L = >100Ω		±100		mA
Voltage	R_L = >200Ω	±10			V
Input Offset Voltage	Adjustable to Zero				
Initial	@ +25°C		±0.5	±1.5	mV
vs. Case Temperature					
−55°C to +125°C			35		µV/°C
vs. Power Supply Voltage			0.5		mV/V
Input Bias Current					
Initial	@ +25°C		1	2	nA
vs. Temperature			Doubles		/10°C
Input Offset Current					
Initial	@ +25°C			±100	pA
Input Impedance					
Differential	}In Parallel with 5pF		10^{10}		Ω
Common Mode			10^{10}		Ω
Input Voltage Range					
Common Mode		±10		±18	V
Differential				±18	V
Common-Mode Rejection			70		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ				
dc to 100kHz			5		µV rms
dc to 2MHz			7		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω;				
	Load = 100Ω		300		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω;				
	Load = 100Ω		320		V/µs
Overload Recovery	50% Overdrive		400		ns
Unity Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100		MHz
Small Signal Bandwidth, −3dB	A = −1; R_{FF} = R_{FB} = 500Ω		45		MHz
	A = −1; R_{FF} = R_{FB} = 1000Ω		35		MHz
	A = −2; R_{FF} = 500Ω;				
	R_{FB} = 1000Ω		35		MHz
	A = −4; R_{FF} = 250Ω;				
	R_{FB} = 1000Ω		30		MHz
Output Impedance				<1	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω;				
	100Ω Load; 10pF Capacitance				
	5V p-p Output		25		MHz
	4V p-p Output		30		MHz
	2V p-p Output		55		MHz
	A = 3; R_{FF} = 500Ω;				
	R_{FB} = 1000Ω;				
	Load = 100Ω, 1000Ω, or 2000Ω;				
	Capacitance = 10pF				
	10V Output		17		MHz
	5V p-p Output		25		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

		HOS-060SH			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Noninverting Bandwidth, −3dB (Continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ω Load/10pF Capacitance				
	5V p-p Output		15		MHz
	4V p-p Output		30		MHz
	2V p-p Output		40		MHz
	1V p-p Output		40		MHz
Full Power Bandwidth (−3dB)	Output = ±5V; A = −1; Load = 100Ω		20		MHz
Settling Time to 0.1%	A = −1; R_{FF} = R_{FB} = 500Ω				
Inverting	V_{OUT} = ±5V		100		ns
	V_{OUT} = ±2.5V		80		ns
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω Max Load Capacitance = 75pF				
	V_{OUT} = ±5V		200		ns
	V_{OUT} = ±2.5V		135		ns
Harmonic Distortion (See Figure 5)	A = −1; Load = 1000Ω Signal = 4MHz; 2V Output		−63		dB
Noninverting Harmonic Distortion (See Figure 6)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V Output		−59		dB
Power Supply					
Voltage	Rated Performance		±15		V dc
Voltage	Operating Range	±12		±18	V dc
Current	Quiescent		±20	±25	mA
Power Consumption	Quiescent		0.6		W
Power Dissipation				1.25	W
Temperature Range					
Operating (Case)	(See Figure 2 for	−55		+125	°C
Storage	Derating Information)	−65		+150	°C
Package Option[2] TO-8 (H-12A)					

NOTES
[1]Specification for Inverting Mode unless otherwise noted.
[2]See Section 16 for package outline information.

*Specifications same as HOS-060SH

Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.
Specifications subject to change without notice

PIN DESIGNATIONS

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	−INPUT
6	+INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-060 are characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A current to voltage conversion or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed-forward resistor for the op amp.

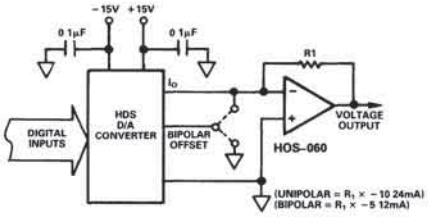


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and the bipolar offset pin grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

OFFSET AND GAIN ADJUSTMENT

The low value of offset may preclude the need for adjustment, but Figure 4 shows a method of adjusting both offset and gain.

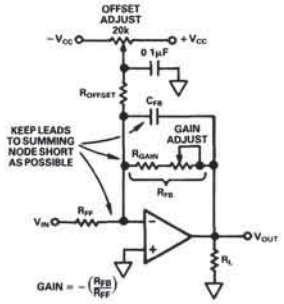


Figure 4. HOS-060 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right) \text{ where } R_{FB} = R_{GAIN} + \text{Gain Adjust.}$$

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-060 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by increasing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The Analog Devices HOS-060 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in the designs of competing units.

The HOS-060 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

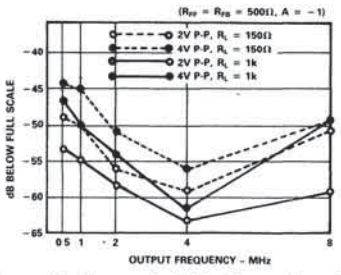


Figure 5. Harmonic Distortion – Inverting

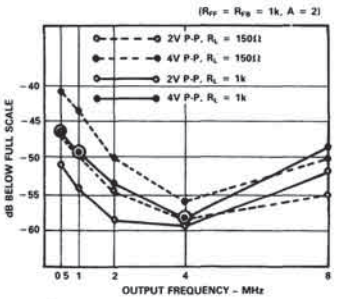


Figure 6. Harmonic Distortion – Noninverting

THE READER IS URGED TO CONSULT THE HOS-050 DATA SHEET FOR ADDITIONAL APPLICATIONS INFORMATION. THE HOS-060 IS PIN-FOR-PIN COMPATIBLE WITH THE HOS-050 SERIES AND CAN BE USED IN SIMILAR WAYS.

ANALOG DEVICES

Wide Bandwidth, High-Speed Buffer Amplifiers

HOS-100AH/HOS-100SH

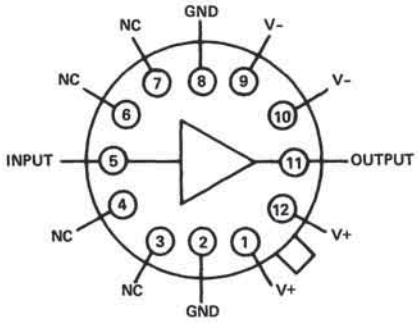
FEATURES

- Wide Bandwidth – dc to 125MHz
- High Slew Rate – 1500V/μs
- Operation Guaranteed -55°C to +125°C (SH)
- High Output Drive – ±10V with 100Ω Load

APPLICATIONS

- Current Boosters
- High Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive
- High Speed Line Drivers
- Video Impedance Transformation

HOS-100AH/HOS-100SH FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HOS-100SH and HOS-100AH Bipolar Buffer Amplifiers are high-speed, voltage follower/buffers designed to provide high-current drive at frequencies from dc to over 125MHz, as well as providing ±10mA into 1kΩ loads (±100mA peak) at slew rates of 1500V/μs. Both units also exhibit excellent phase linearity (2°), and low distortion (<0.1%).

For commercial temperature ranges the HOS-100AH is specified for operation over the range of -25°C to +85°C (case). The HOS-100SH is specified for operation over the military range of -55°C to +125°C (case).

The HOS-100SH and HOS-100AH are intended to fulfill a wide range of buffer applications, such as video impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high-speed line drivers and nuclear instrumentation amplifiers. Additionally, both amplifiers will continuously drive 50Ω coaxial cables or serve as yoke drives in high resolution CRT displays.

They are particularly well suited for current booster applications (Figure 3) within an op-amp loop where input impedance and bias current requirements are less stringent than in FET design.

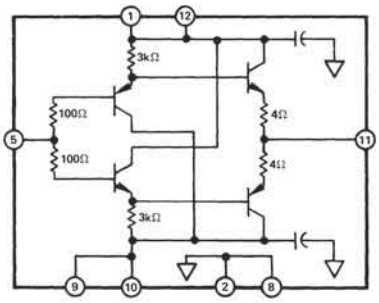


Figure 1. Schematic Diagram HOS-100

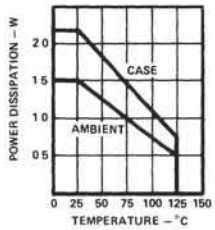


Figure 2. Power Derating

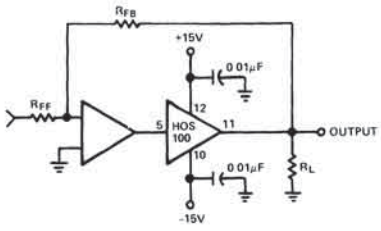


Figure 3. Current Booster

SPECIFICATIONS

PARAMETER	CONDITIONS	HOS-100SH MIN	HOS-100SH TYP	HOS-100SH MAX	HOS-100AH MIN	HOS-100AH TYP	HOS-100AH MAX	UNITS
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	T_C = 25°C		5	20		5	25	μA
				25				μA
Input Impedance	V_{IN} = 1V rms, f = 1kHz R_L = 1k, T_C = 25°C	100	200		100	200		kΩ
Voltage Gain	V_{IN} = 1V rms, f = 1kHz R_L = 1k, T_C = 25°C	0.95	0.97	1.0	0.94	0.96	1.0	V/V
Output Offset Voltage	R_S = 50Ω, T_C = 25°C		5	10		10	25	mV
				25			35	mV
Output Offset Voltage T_C	R_S = 50Ω		25	75		25	75	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz R_S = 500Ω, R_L = 1k		8	12		8	12	Ω
Output Voltage Swing	R_S = 50Ω, R_L = 1k	±12	±13		±12	±13		V
	V_S = ±5V, R_L = 1k		6			6		V
Supply Current	V_{IN} = 0V, T_C = 25°C							
	V_S = ±15		13	16		15	20	mA
	V_S = ±5		10			10		mA
Power Consumption	V_{IN} = 0V, V_S = ±15V T_C = 25°C		390	480		450	600	mW
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms	100	125		100	125		MHz
Rise Time	ΔV_{IN} = 0.5V		2	5		2	5	ns
Propagation Delay	ΔV_{IN} = 0.5V		1.5			1.5		ns
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Harmonic Distortion			<0.1			<0.1		%
MFBF			1.509×10^7 hours					

NOTES
[1] Unless otherwise noted, these specifications apply for +15V applied to Pin 12, and −15V applied to Pin 10.
[2] Unless otherwise noted, specifications apply over a temperature range, −55°C ≤ T_C ≤ +125°C for the HOS-100SH, and −25°C ≤ T_C ≤ +85°C for the HOS-100AH. Typical values shown are for T_C = +25°C.
[3] These specifications all measured with the following conditions: T_C = +25°C, V_S = ±15V, R_S = 50Ω, R_L = 1k.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ − V−) 40V
Maximum Power Dissipation 1.5W
Input Voltage . . . . . Equal to Supply Voltage
Maximum Continuous Output Current . . . . . ±100mA
Maximum Peak Output Current . . . . . ±250mA
Operating Temperature Range (Case) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Maximum Junction Temperature . . . . . +175°C

ORDERING INFORMATION

Model	Temperature Range	Package Options*
HOS-100AH	−25°C to +85°C	H-12A
HOS-100SH	−55°C to +125°C	H-12A

*See Section 16 for package outline information.

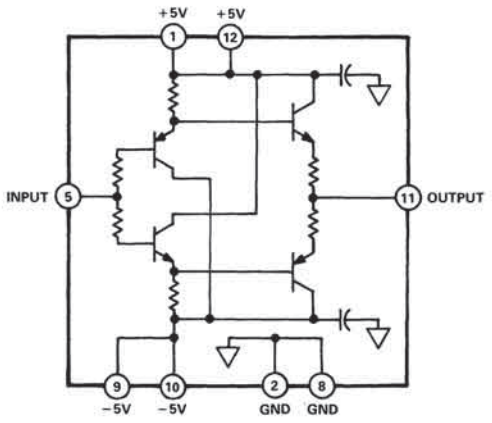
Wide Bandwidth, High-Speed Buffer Amplifier

HOS-200

FEATURES
Wide Bandwidth/Good Drive
Fast Rise Time
Low Power
±5V Supplies

APPLICATIONS
Current Boosters
High-Speed A/D Input Buffers
Instrumentation Amplifiers
Coaxial Cable Drivers
High-Speed Line Drivers

HOS-200 FUNCTIONAL BLOCK DIAGRAM



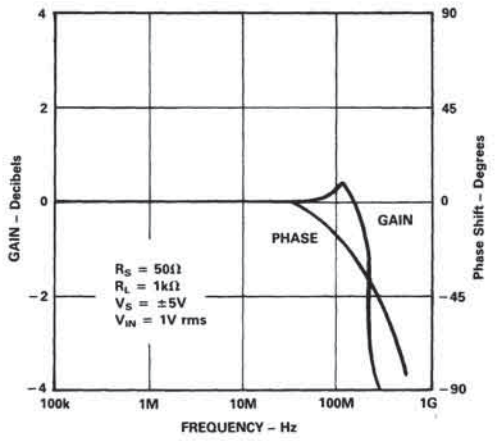
GENERAL DESCRIPTION

The HOS-200AH and HOS-200SH Buffer Amplifiers are high-speed, voltage follower/buffers designed to provide up to 100mA of continuous current at frequencies from dc to 200MHz. AC performance is enchanced with slew rates exceeding 1500V/μs. Both units exhibit excellent phase linearity and low distortion, making them ideal for raster graphic and other video-speed applications.

These devices are designed to fit into a broad range of buffer applications, such as video impedance transformation; high-impedance input buffers for A/D converters and comparators; and high-speed line drivers for nuclear instrumentation amplifiers. The HOS-200 will drive 50Ω and 75Ω cables, and can serve as a yoke driver in high-resolution CRT displays.

The versatility of the HOS-200 makes it particularly well suited for use with the Analog Devices series of raster graphic video DACs, such as the monolithic AD9700 and the hybrid HDG Series. The HOS-200 follower/buffer can also economically enhance the output drive of monolithic op amps.

MIL-STD-1772 approval has been granted to the Analog Devices manufacturing facility that produces the parts, which are also available with MIL processing. The HOS-200AH operates from −25°C to +85°C; the HOS-200SH is specified for −55°C to +125°C.



HOS-200 Phase and Gain Response

SPECIFICATIONS (typical @ +25°C with $\pm V_S$ = ±5V unless otherwise specified)

Model	HOS-200AH	HOS-200SH
ABSOLUTE MAXIMUM RATINGS		
Peak Voltage Between Supply Terminals (V_S+ to V_S−)	30V	*
Continuous Voltage Between Supply Terminals (V_S+ to V_S−)	16V	*
Power Dissipation	See Derating Graph	*
Input Voltage	$\pm V_S$	*
Continuous Output Current	±100mA	*
Peak Output Current	±250mA	*
Operating Temperature Range (Case)	−25°C to +85°C	−55°C to +125°C
Junction Temperature	+150°C	*
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature (soldering, 10sec)	+300°C	*

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	−55°C	+25°C	+125°C	Units
Input Bias Current	V_{IN} = 0V; R_S = 10kΩ		8	25	30 (max)	20 (max)	20 (max)	µA
Input Impedance	V_{IN} = 1V rms; f = 1kHz; R_L = 1k	100	200			100(min)		kΩ
Voltage Gain	V_{IN} = 1V; R_L = 1k	0.975	0.985		0.975 (min)	0.975 (min)	0.975 (min)	V/V
	V_{IN} = 1V; R_L = 100Ω	0.900	0.915			0.900 (min)		V/V
Offset Voltage	R_S = 50Ω		12	25	18 (max)	15 (max)	15 (max)	mV
Offset Voltage T_C[1]	R_S = 50Ω		25		25 (typ)	5 (typ)	5 (typ)	µV/°C
Output Impedance	V_{IN} = 1V rms; f = 1kHz R_S = 500Ω; R_L = 1kΩ		8	12		12 (max)		Ω
Output Voltage Swing	R_S = 500Ω; R_L = 1kΩ	4.0	4.25		3.75 (min)	4.0 (min)	4.0 (min)	V
Output Current (Continuous)	V_{OUT} = 0V	100				100 (min)		mA
Supply Current	V_{IN} = 0V; V_S = ±5V		12	16	16 (max)	16 (max)	20 (max)	mA
Power Consumption	V_{IN} = 0V; V_S = ±5V		120	160	160 (max)	160 (max)	200 (max)	mW
Power Supply Rejection Ratio (PSRR)	ΔV_S = ±2.5V	40	45			40 (min)		dB

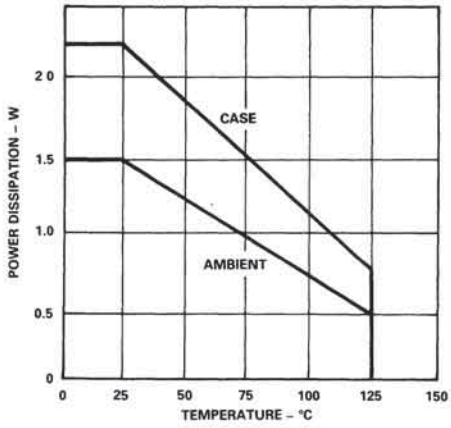
AC ELECTRICAL CHARACTERISTICS[2]

Parameter	Conditions	Min	Typ	Max	−55°C	+25°C	+125°C	Units
Slew Rate	V_{IN} = ±2.5V	1000	1500			1000 (min)		V/µs
Bandwidth (−3dB)	V_{IN} = 1V rms		200			200		MHz
Rise Time	ΔV_{IN} = 0.5V		1.5			1.5		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.5			1.5		ns
Phase Nonlinearity	BW = 1 to 20MHz		2			2		degree
Harmonic Distortion			<0.1			<0.1		%
THERMAL RESISTANCE[3]								
Junction to Air, θ_{JA} (Free Air)			90			90		°C/W
Junction to Case, θ_{JC}			40			40		°C/W
MTBF[4]						>1.1 × 10^7		hours
PACKAGE OPTION[5] TO-8 (H-12A)								

NOTES
[1]Input offset voltage T_C is typically less than 5µV/°C from +25°C to high temperature extreme.
[2]These specifications measured under following conditions: T_C = +25°C; ±V_S = ±5V; R_S = 0Ω, R_L = 1kΩ.
[3]Recommended maximum junction temperature is +150°C.
[4]MTBF calculated using MIl Handbook 217, Ground; Fixed; Temperature (case) = 35°C.
[5]See Section 16 for package outline information.
Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1	V+
2	GROUND
3	NC
4	NC
5	INPUT
6	NC
7	NC
8	GROUND
9	V−
10	V−
11	OUTPUT
12	V+



HOS-200 Power Derating

ENHANCING HOS-200 PERFORMANCE

The HOS-200 is an excellent building block in high slew rate, pulse-oriented systems. Output loading in these types of systems is often highly capacitive because of coaxial cables and twisted pair lines; but the powerful drive capability of the HOS-200 makes it a good choice for inclusion in the system.

Its effectiveness can be extended further through the use of a small series resistance (5Ω–300Ω) in the output of the unit. This has two effects: it shields the HOS-200 from the load capacitance, which might otherwise be outside the design limits of the amplifier; and also tailors the pulse response. The output response can also be enhanced with a small (100pF–300pF) capacitor connected between the input and output.

LAYOUT CONSIDERATIONS

Like any high-speed device, the HOS-200 amplifier will benefit from the use of good high-frequency design practices. The undesirable effects of stray capacitance and high frequency coupling can be minimized with close attention to circuit layout.

A low-impedance ground plane under the HOS-200 can reduce the effects of distributed capacitance; and provide a greater degree of shielding for the device. Lead lengths in and out of the HOS-200 should be kept as short as practicable to minimize impedances and limit the effects of signal reflections.

Direct soldering of the unit into the circuit is recommended to avoid the inter-lead capacitance of sockets and the reduction in performance which can result. If socket mount *must* be used, individual pin sockets are preferable to device sockets.

The HOS-200 contains internal power supply decoupling capacitors, but further improvement in performance can often be achieved with external decoupling capacitors connected as closely as possible to the power supply pins of the amplifier. Typically, a combination of a 0.1μF ceramic disk capacitor and a 100pF tantalum capacitor is connected to each supply pin.

Each power supply voltage has been provided with two pins on the HOS-200; +5V is connected to pins 1 and 12, and −5V is connected to pins 9 and 10. Each pair of pins is connected internally, but should also be connected externally to its mate and the appropriate power supply. Pins 2 and 8 are ground pins which are connected internally, but should also be connected together externally before the connection to the low-impedance ground recommended above.

HEAT SINKING

An efficient heat sink is required for the HOS-200SH if the user expects to obtain maximum output drive at temperatures up to +125°C. One possibility is the Thermalloy-2204A, but other appropriate devices are also available.

The case of the HOS-200 is electrically isolated from the circuit containing the amplifier. This means the case can be connected to system ground(s) for additional heat dissipation, and shielding. Pins 3, 4, 6, and 7 are designated as "no connection" and can also be connected to the low-impedance ground to help dissipate heat.

SUGGESTED APPLICATIONS

Figures 1 and 2 are possible application ideas using the HOS-200 amplifier. The circuits which are shown are not intended as the only possible applications for this device; they are simply intended to illustrate some possibilities offered by the unit.

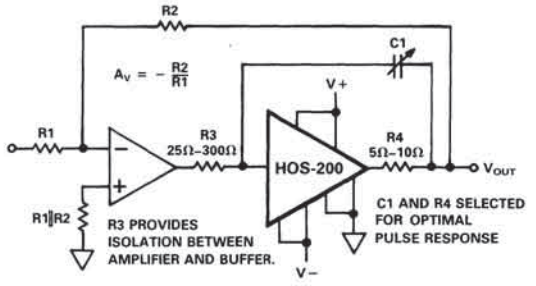


Figure 1. Increased Output Current Drive

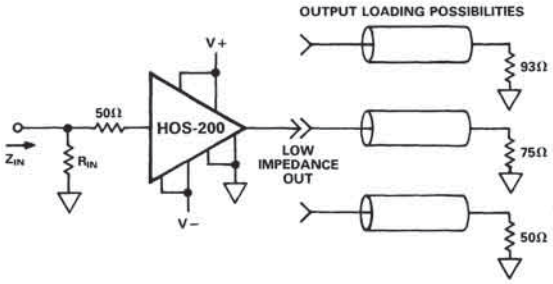


Figure 2. Impedance Transformations for 50Ω, 75Ω, and 93Ω Cables

PERFORMANCE GRAPHS

Figures 3 through 9 depict typical performance of the HOS-200 amplifier for a number of characteristics. As in the parameters shown in the SPECIFICATIONS section of the data sheet, the data shown in the graphs are typical performance at +25°C, unless noted otherwise.

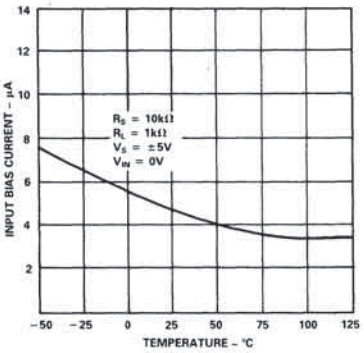


Figure 3. Input Bias Current vs. Temperature

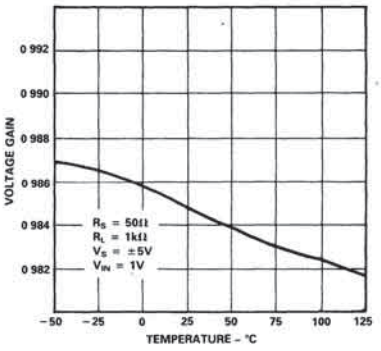


Figure 4. Gain vs. Temperature

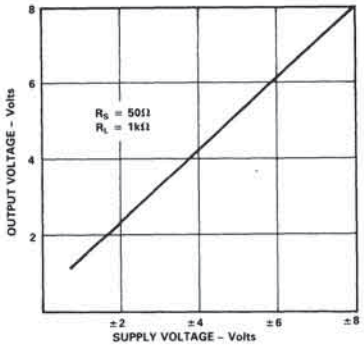


Figure 5. Output Voltage vs. Supply Voltage

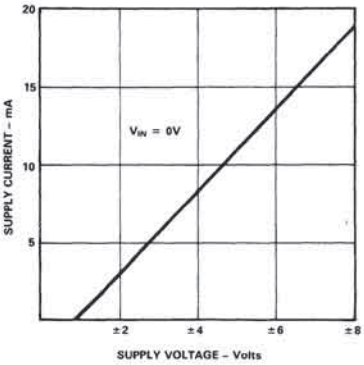


Figure 6. Supply Current vs. Supply Voltage

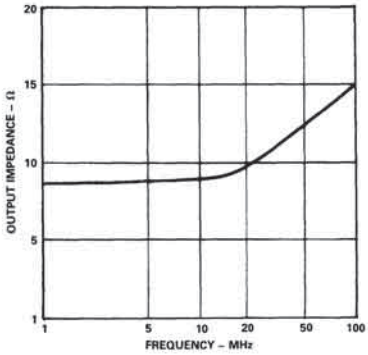


Figure 7. Output Impedance vs. Frequency

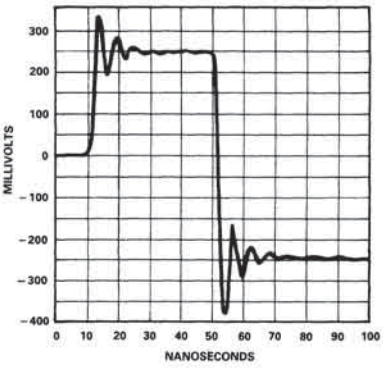


Figure 8. Small-Signal Settling (±250mV Square Wave Input)

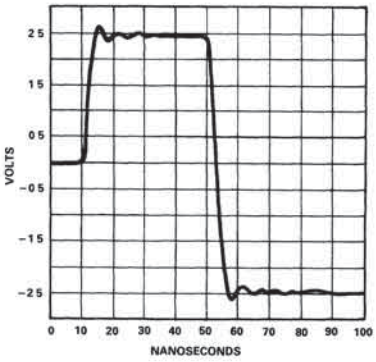


Figure 9. Large-Signal Settling (±2.5V Square Wave Input)

ORDERING INFORMATION

The model HOS-200AH operates over an industrial temperature range of −25°C to +85°C. The model HOS-200SH is designed for a military temperature range of −55°C to +125°C. The Computer Labs Division of Analog Devices, which produces the HOS-200 has been certified as meeting the standards established by MIL-STD-1772. Contact the division for details regarding parts with MIL processing.

Comparators
Contents

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AD9685/9687 – High Speed Comparators . . . . . 3 – 9
AD9686 – High Speed TTL Voltage Comparator . . . . . 3 – 13
AD96685/96687 – Ultrafast Comparators . . . . . 3 – 17

3

Selection Guide
Comparators

Model	Prop Delay ns	Latch	Interface Logic	Page	Notes
AD790	35	X	TTL	3 – 5	
AD9685	2.2	X	ECL	3 – 9	
AD9686	7	X	TTL	3 – 13	
AD9687	2.7	X	ECL	3 – 9	Dual
AD96685	2.5	X	ECL	3 – 17	
AD96687	2.5	X	ECL	3 – 17	Dual

Orientation
Comparators

A voltage comparator compares two voltages and provides an output that is a function of their difference. For the products in this section, the output of an ideal comparator has two stable states representing the *sign* of the difference. Thus, the output will be a logic "1" if the voltage at the input labelled "+" is greater than the voltage at the input labelled "–," and logic "0" for the opposite case.

A comparator is used wherever some action depends on whether a voltage is – or becomes – greater or less than another voltage – usually a reference. Since it is in effect a 1-bit A/D converter, the comparator is the basic element of virtually all A/D converters, as well as a sign-magnitude adjunct. Because the voltage that is compared with a reference can be the linearly varying output of an integrator with constant input, a comparator can be used in analog-based event timing. The comparator is also an element of pulse-width modulators, peak detectors, delay generators, switch drivers, etc.

A comparator is essentially a fast, high-gain amplifier whose output is always at an upper or lower limit, except when switching. The simplest comparator would be an open-loop-connected, uncompensated, high-gain, high-slew-rate op amp with excellent offset & drift characteristics, fast recovery from overdrive and an overdrive-protected input.

In addition, practical comparators have a small amount of hysteresis (internal or external) to help keep noise from causing the output to bounce around, and most have a *latch*, which makes it possible to freeze the output at the state it has at a given instant of time, in response to a logic signal. Since the comparator is producing a digital decision, its outputs are generally compatible with either TTL or ECL.

Aside from its op-amp related specifications, such as bias current, offset & drift and the various logic-related timing and interface specs, the key comparator spec is *propagation delay*: the time required for the output to reach the 50% point of a transition, after the net input has crossed the offset voltage – when driven by a square wave to a prescribed value of input overdrive, usually 5mV or 10mV.

The Selection Guide classifies Analog Devices comparators by propagation delay, presence or absence of a latch and interface logic compatibility. It also indicates the presence of *dual* comparators, each comprising two independent comparators on a single monolithic chip. Since pairs of comparators jointly have four possible states, they may be used for high-accuracy 2-bit ADCs and for *window* measurements, as well as for simple two-in-one space-saving.

Fast Single Supply Comparator

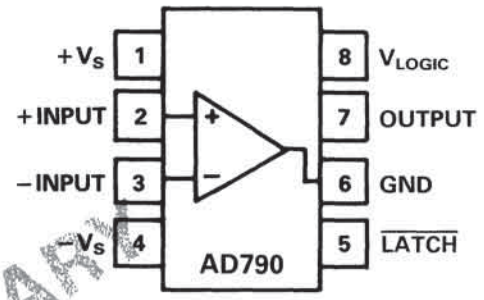
AD790

FEATURES
- 35ns max Response Time
- Single +5V Supply Operation
- CMOS or TTL Logic Capability
- 250μV max Input Offset Voltage
- 1mV Input Voltage Resolution
- 15V max Differential Input Voltage
- Latching Function Capability
- Glitch Free Output Stage
- 60mW Power Dissipation

APPLICATIONS
- Oversampling A/D Converters
- Single Supply Line Receiver
- MOS Switch Drivers
- Pulse Width Modulator
- Peak Detector
- Single Supply Ground Crossing Detector
- Time Delay Generator
- Available in Plastic, Mini-DIP, Hermetic Cerdip Packages

AD790 FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and Cerdip



PRELIMINARY DATA SHEET

PRODUCT DESCRIPTION

The AD790 is a fast (35ns) precise voltage comparator. It has a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from a single +5V supply or a dual ±15V supply. In the single supply mode, the AD790's inputs may be referenced to "ground," a feature not found in most other comparators. In the dual supply mode it has the unique advantage of handling a maximum differential voltage of 15V across its input terminals, easing interfacing of the input to large amplitude and dyanamic signals.

This device is fabricated using Analog Devices' complementary bipolar (CB) process – offering benefits such as fast response time (35ns), low input offset voltage (250μV) and high input voltage resolution (1mV). To preserve its speed, the AD790 incorporates a "low glitch" output stage which does not exhibit large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances which would tend to feed back to the input causing undesired oscillations or hysteresis. The AD790 has a latching function which makes it ideal for applications requiring synchronous detection – wherein the latch is activated by forcing the latch pin low with either a CMOS or TTL gate.

The high-speed, high-precision, low-power and glitch-free operation performances brought together in the AD790, make it the optimum choice for 12-bit high-speed applications.

The AD790 is available in five performance grades. The AD790J and the AD790K are rated over the commercial temperature range of 0 to +70°C. The AD790A and AD790B are rated over the industrial temperature range of −40°C to +85°C. The AD790S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

Extened reliability PLUS screening is available, specified over the commercial and industrial temperature range. PLUS screening includes a 168 hour burn-in, as well as other environmental and physical tests.

PRODUCT HIGHLIGHTS

1. The AD790 is a fast, high precision, easy to use voltage comparator.
2. True single supply operation plus dual supply capability allow usage in many design environments.
3. CMOS or TTL compatible output stage.
4. 60mW power dissipation is the lowest in its class.
5. Glitch-free output stage minimizes oscillation and hysteresis.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc, V_{LOGIC}, unless otherwise noted)

Model	Conditions	AD790J/A/S Min	AD790J/A/S Typ	AD790J/A/S Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	Units
RESPONSE TIME								
Propagation Delay	5mV Overdrive		30	35		30	35	ns
Latch Response Time			15	20		15	20	ns
Latch Setup Time			10	15		10	15	ns
OUTPUT CHARACTERISTICS								
Output HIGH Voltage	100µA Sink	**4.7**	4.8		**4.7**	4.8		V
	$T_{min}-T_{max}$	4.6/4.6/**4.6**	4.8		**4.6**	4.8		V
Output Low Voltage	8mA Sink		0.44	**0.5**		0.44	**0.5**	V
	$T_{min}-T_{max}$		0.44	0.5/0.5/**0.5**		0.44	**0.5**	V
INPUT CHARACTERTISTICS								
Input Offset Voltage[1]			200	**1000**		50	**500**	µV
	$T_{min}-T_{max}$[1]			**1.5**			**0.75**	mV
Hysteresis[2,3]	$T_{min}-T_{max}$	**300**	400	**600**	**300**	400	**500**	µV
Voltage Resolution	$T_{min}-T_{max}$		0.8	**1.2**		0.8	**1.0**	mV
Input Bias Current	Either Input		2	**5**		1.3	**3**	µA
	$T_{min}-T_{max}$			6/6/**8**			**4**	µA
Input Offset Current			0.05	**0.25**		0.01	**0.15**	µA
	$T_{min}-T_{max}$			0.3/0.3/**0.4**			**0.2**	µA
PSRR		**80**	**90**		**88**	100		dB
	$T_{min}-T_{max}$	76/76/**76**	**88**		**85**	96		dB
INPUT VOLTAGE RANGE								
Differential Input Voltage	$\pm V_S <= \pm 15V$			**$\pm V_S$**			**$\pm V_S$**	V
Common-Mode Input		**$-V_S$**		**$+V_S-2$**	$-V_S$		$+V_S-2$	V
CMRR	$-10<V_{CM}<+10$	**80**	95		**90**	100		dB
	$T_{min}-T_{max}$	76/76/**76**			**88**			dB
LATCH CHARACTERISTICS[2]								
LOW Input Level	$T_{min}-T_{max}$			**0.8**			**0.8**	V
HIGH Input Level	$T_{min}-T_{max}$	**1.6**			**1.6**			V
Latch Input Current			2	**5**		2	**5**	µA
	$T_{min}-T_{max}$			6/6/**8**			**6**	µA
SUPPLY CHARACTERISTICS								
Differential Supply Voltage[2,4]	V_{LOGIC} = 5V	**4.5**		**36**	**4.5**		**36**	V
Logic Supply	T_{min} to T_{max}	4		6	4		6	V
Quiescent Current								
$+V_S$	$+V_S$ = +15V		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = −15V		4	**5**		4	**5**	mA
V_{LOGIC}	V_{LOGIC} = +5V		2	**3**		2	**3**	mA
Power Dissipation	±15V Operation			**240**			**240**	mW

PRELIMINARY TECHNICAL DATA

NOTES
[1]Defined as the average of the low to high and high to low transition input voltages.
[2]Guaranteed over full temperature range although not 100% tested at temperature for J/A grades. 100% tested on all other grades.
[3]Defined as half the magnitude between low to high and high to low transition input voltages.
[4] $+V_S$ must be no less than 0.5V below V_{LOGIC} in any supply operating conditions.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

SPECIFICATIONS (@ +25°C and Single +5V Supply, unless otherwise noted)[1]

Model	Conditions	AD790J/A/S Min	AD790J/A/S Typ	AD790J/A/S Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	Units
RESPONSE TIME								
Propagation Delay	5mV Overdrive		35	40		35	40	ns
Latch Response Time			20	25		20	25	ns
Latch Setup Time			15	20		15	20	ns
OUTPUT CHARACTERISTICS								
Output HIGH Voltage	100μA Sink	**4.7**	4.8		**4.7**	4.8		V
	$T_{min}-T_{max}$	4.6/4.6/**4.6**	4.8		**4.6**	4.8		V
Output LOW Voltage	8mA Sink		0.44	**0.5**		0.44	**0.5**	V
	$T_{min}-T_{max}$		0.44	0.5/0.5/**0.5**		0.44	**0.5**	V
INPUT CHARACTERTISTICS								
Input Offset Voltage[2]			200	**1000**		50	**250**	μV
	$T_{min}-T_{max}$			1.5/1.5/**1.5**			**0.75**	mV
Hysteresis[3,4]	$T_{min}-T_{max}$	**300**	450	**700**	**300**	450	**600**	μV
Voltage Resolution	$T_{min}-T_{max}$		0.9	1.2		0.9	**1.2**	mV
Input Bias Current	Either Input		2	5		1.3	**3**	μA
	$T_{min}-T_{max}$			6/6/**8**			**4**	μA
Input Offset Current			0.05	**0.25**		0.01	**0.15**	μA
	$T_{min}-T_{max}$			0.3/0.3/**0.4**			**0.2**	μA
PSRR	$4.5<V_S<5.5$	**80**	90		**86**	100		dB
	$T_{min}-T_{max}$	76/76/**76**	88		**82**	96		dB
INPUT VOLTAGE RANGE[4]								
Differential Input Voltage				**$+V_S$**			**$+V_S$**	V
Common-Mode Input		**0**		$+V_S-2$	0		$+V_S-2$	V
LATCH CHARACTERISTICS[4]								
LOW Input Level	$T_{min}-T_{max}$			**0.8**			**0.8**	V
HIGH Input Level	$T_{min}-T_{max}$	**1.6**			**1.6**			V
Latch Input Current			2	5		2	5	μA
	$T_{min}-T_{max}$			6/6/**8**			**6**	μA
SUPPLY CHARACTERISTICS								
Single Supply Range		3.5		7	3.5		7	V
Quiescent Current	$+V_S=+5V$			**12**			**12**	mA
Power Dissipation	$+V_S=+5V$ Operation			**60**			**60**	mW
PACKAGE OPTIONS[5]								
Plastic (N–8)			AD790JN			AD790KN		
Cerdip (Q–8)			AD790AQ, AD790SQ			AD790BQ		

NOTES
[1]Pin 1 tied to Pin 8 = +5V, and Pin 4 tied to Pin 6 = 0V.
[2]Defined as the average of the low to high and high to low transition input voltages.
[3]Defined as half the magnitude between low to high and high to low transition input voltages.
[4]Guaranteed over full temperature range although not 100% tested at temperature for J/A grades. 100% tested on all other grades.
[5]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation	500mW
Differential Input Voltage[2]	±15V
Output Current	20mA
Storage Temperature Range N, Q	−65°C to +125°C
Operating Temperature Range	
AD790J/K	0 to +70°C
AD790A/B	−40°C to +85°C
AD790S	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

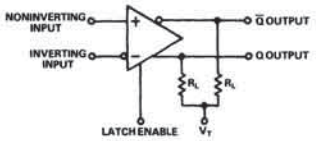
High-Speed Comparators

AD9685/AD9687

FEATURES
- 2.7ns Propagation Delay
- 0.5ns Latch Setup Time
- 90dB CMRR
- +5V, −5.2V Supply Voltages

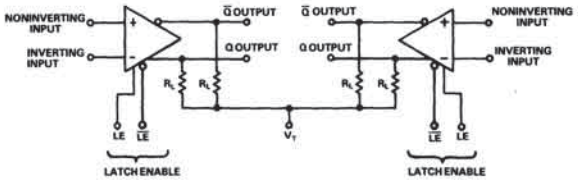
APPLICATIONS
- High-Speed Triggers
- High-Speed Line Receivers
- Peak Detectors
- Threshold Detectors

AD9685/AD9687 FUNCTIONAL BLOCK DIAGRAMS



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2 0V, OR 200Ω–2000Ω CONNECTED TO −5 2V

AD9685



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200ΩCONNECTED TO −2 0V, OR 200Ω–2000Ω CONNECTED TO −5 2V

AD9687

GENERAL DESCRIPTION

The AD9685 and the AD9687 are high-speed voltage comparators. The AD9685 and the AD9687 are manufactured in a high performance bipolar process which allows improved speed and dc accuracy. The AD9685 is a single comparator with a 2.7ns propagation delay, and the AD9687 is a dual comparator of equal performance.

Both devices employ a high precision differential input stage with a common-mode range of ±2.5V. The AD9685 and the AD9687 provide complementary digital outputs which are fully ECL compatible. The output stage is capable of driving 50Ω terminated transmission lines given the 30mA output drive capacity. In addition to this, a latch enable input is provided, allowing operation in either a sample-hold mode or a track-hold mode.

The AD9685 and the AD9687 are both available as an industrial grade device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. The AD9685 is available in a 10-pin TO-100 metal can, or a 16-pin ceramic package. The AD9687 is available in a 16-pin ceramic package.

ORDERING INFORMATION

Device	Type	Temperature Range	Description	Package Options*
AD9685BD	Single	−25°C to +85°C	16-Pin DIP, Industrial	D-16
AD9685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD9685TD	Single	−55°C to +125°C	16-Pin DIP, Extended Temperature	D-16
AD9685TH	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD9687BD	Dual	−25°C to +85°C	16-Pin DIP, Industrial	D-16
AD9687TD	Dual	−55°C to +125°C	16-Pin DIP, Extended Temperature	D-16

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Input Voltage . . . . . ±5V
Differential Input Voltage 5.5V
Latch Enable Voltage . . . . . $-V_S$ to 0V
Output Current 30mA
Power Dissipation AD9685 . . . . . 500mW
AD9687 . . . . . 600mW

Operating Temperature Range[2]
AD9685/87/BD/BH . . . . . −25°C to +85°C
AD9685/87/TD/TH . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

		Industrial Temp. Range −25°C to +85°C						Military Temp. Range −55°C to +125°C						
		AD9685BD/BH			AD9687BD			AD9685TD/TH			AD9687TD			
Parameter	Temp	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS														
Input Offset Voltage[3]	+25°C		1	5		1	5		1	5		1	5	mV
	Full			7			7			7			7	mV
Input Offset Drift	Full		20			20			20			20		µV/°C
Input Bias Current	+25°C		3	15		3	15		3	15		3	15	µA
	Full			20			20			20			20	µA
Input Offset Current	+25°C		0.5	3		0.5	3		0.5	3		0.5	3	µA
	Full			5			5			5			5	µA
Input Resistance	+25°C		200			200			200			200		kΩ
Input Capacitance	+25°C		3			3			3			3		pF
Input Voltage Range	Full	−2.5		+2.5	−2.5		+2.5	−2.5		+2.5	−2.5		+2.5	V
Common-Mode Rejection Ratio	Full	75	90		75	90		80	90		80	90		dB
ENABLE INPUT														
Logic "1" Voltage	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full			60			60			60			60	µA
Logic "0" Current	Full			5			5			5			5	µA
DIGITAL OUTPUTS[4]														
Logic "1" Voltage	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[4]														
Propagation Delays[5]														
Input to Output HIGH	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Input to Output LOW	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable to Output HIGH	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable to Output LOW	+25°C		2.7	3.0		2.7	4.0		2.7	3.0		2.7	4.0	ns
Latch Enable														
Minimum Pulse Width	+25°C		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[6]														
Positive Supply Current (+5.0V)	Full		16	23		31	42		16	23		31	42	mA
Negative Supply Current (−5.2V)	Full		30	34		67	75		30	34		67	75	mA
Power Supply Rejection Ratio[7]	Full		60			60			60			60		dB

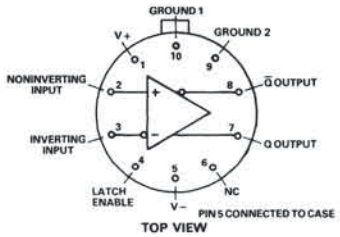
NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Typical thermal impedances . . .
AD9685 Metal Can $\theta_{ja} = 172°C/W; \theta_{jc} = 52°C/W$
AD9685 Ceramic $\theta_{ja} = 115°C/W; \theta_{jc} = 57°C/W$
AD9687 Ceramic $\theta_{ja} = 102°C/W; \theta_{jc} = 45°C/W$
[3]$R_S = 100\Omega$.
[4]Outputs terminated through 50Ω to −2.0V.
[5]Propagation delays measured with 100mV pulse; 5mV overdrive.
[6]Supply voltages should remain stable within ±5% for normal operation.
[7]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

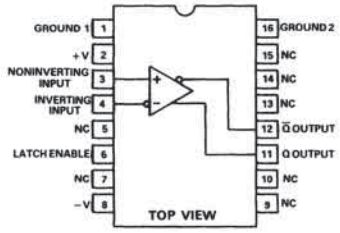
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD9687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be drive in conjunction with LATCH ENABLE for the AD9687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs, Q will be at logic HIGH, if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD9687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW, if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD9687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

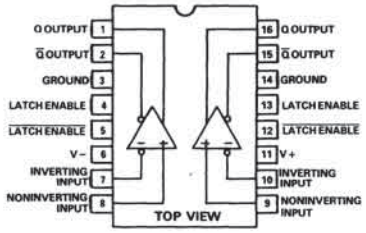
Pin Configuration



AD9685BH

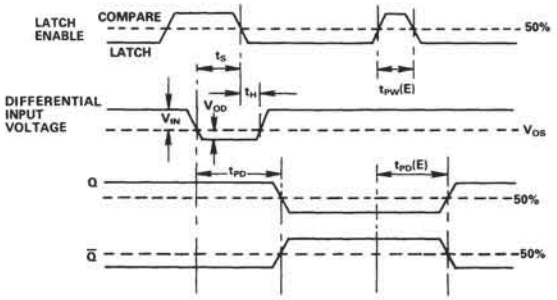


AD9685BD



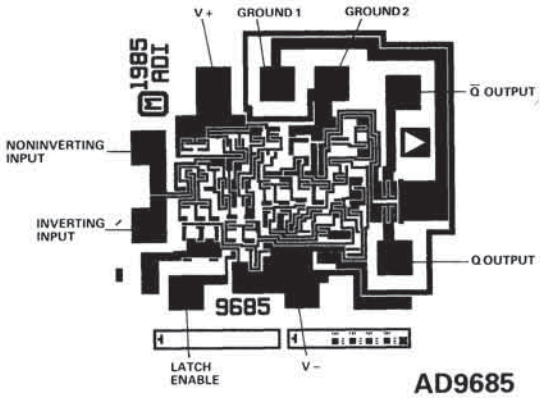
AD9687BD

SYSTEM TIMING DIAGRAM

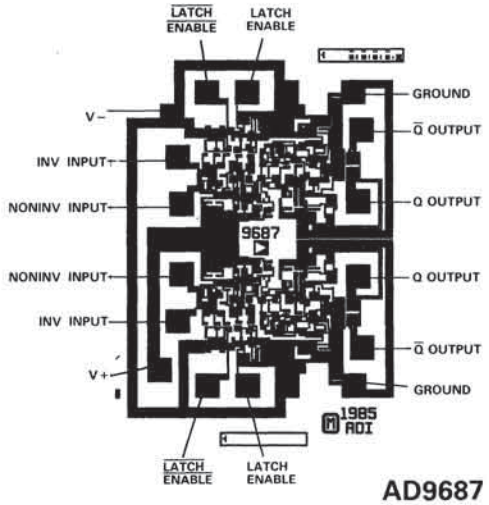


t_S	– Minimum Setup Time
t_H	– Minimum Hold Time
t_{PD}	– Input-to-Output Delay
$t_{PD}(E)$	– LATCH ENABLE to Output Delay
$t_{PW}(E)$	– Minimum LATCH ENABLE Pulse Width
V_{OS}	– Input Offset Voltage
V_{OD}	– Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION



AD9685



AD9687

Die Dimensions	AD9685	54 × 50 × 15 (±2) mils
	AD9687	84 × 62 × 15 (±2) mils
Pad Dimensions		4 × 4 mils
Metalization		10,000Å, Aluminum
Backing		None
Substrate Potential		$-V_S$
Passivation		10,000Å, Nitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum, Ultrasonic Bonding or 1 mil, Gold, Gold Ball Bonding

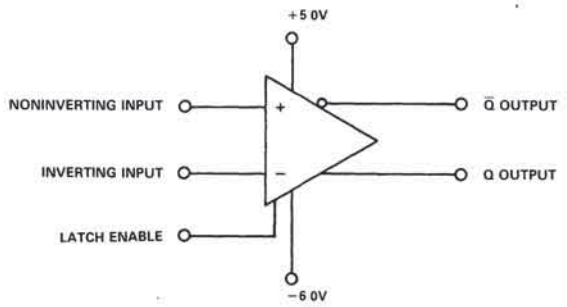
High-Speed TTL Voltage Comparator

AD9686

FEATURES
- 7ns Propagation Delay
- Complementary TTL Outputs
- 85dB CMRR
- +5V, −6V Supply Voltages

APPLICATIONS
- High-Speed Triggers
- High-Speed Line Receivers
- Peak Detectors
- Threshold Detectors

AD9686 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD9686 is a high-speed voltage comparator with complementary TTL outputs. The AD9686 is manufactured in a high-performance bipolar process which provides an excellent match between high-speed ac switching and dc accuracy. The AD9686 operates with a propagation delay of only 7ns.

The AD9686 incorporates a Latch Enable control line providing operation in either a sample-hold mode or a track-hold mode. The Latch Enable setup times are less than 2ns which allows very high-speed voltage sampling.

The precision differential input stage has less than 2mV of offset voltage and requires an input bias current of only 4μA. This combined with the 85dB common-mode rejection ratio, makes the AD9686 especially well suited for high-speed analog signal processing.

The AD9686 is offered as both an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both versions are available packaged in a TO-100 metal can and in a ceramic DIP. The extended temperature range device is also available in a ceramic LCC package.

ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9686BH	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD9686BQ	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD9686TE	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9686TH	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD9686TQ	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . . −7V
Input Voltage Range[2] . . . . . ±5V
Differential Input Voltage 6.0V
Latch Enable Voltage . . . . . 0V to $+V_S$
Output Current Sourcing 4mA
Sinking 14mA

Power Dissipation 600mW
Operating Temperature Range[3]
AD9686BH/BQ . . . . . −25°C to +85°C
AD9686TE/TH/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −6.0V and +5.0V, unless otherwise stated)

Parameter	Mil[4] Sub Group	Temp	Industrial −25°C to +85°C AD9686BH/BQ Min	Typ	Max	Military −55°C to +125°C AD9686TE/TH/TQ Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Input Offset Voltage[5]	1	+25°C		1.0	2.0		1.0	2.0	mV
	2,3	Full			3.0			3.0	mV
Input Offset Drift		Full		10			10		µV/°C
Input Bias Current	1	+25°C		4	10		4	10	µA
	2,3	Full			13			13	µA
Input Offset Current	1	+25°C		0.4	1.0		0.4	1.0	µA
	2,3	Full			1.3			1.3	µA
Input Resistance		+25°C		100			100		kΩ
Input Capacitance		+25°C		3			3		pF
Input Voltage Range	1,2,3	Full	−3.3		+4.5	−3.3		+4.5	V
Common-Mode Rejection Ratio		Full		85			85		dB
ENABLE INPUT									
Logic "1" Voltage	1,2,3	Full			2.0			2.0	V
Logic "0" Voltage	1,2,3	Full	0.8			0.8			V
Logic "1" Current	1,2,3	Full			100			100	µA
Logic "0" Current	1,2,3	Full			100			100	µA
DIGITAL OUTPUTS									
Logic "1" Voltage (Source 1mA)	1,2,3	Full	2.4	3.5		2.4	3.5		V
Logic "0" Voltage (Sink 10mA)	1,2,3	Full		0.3	0.4		0.3	0.4	V
SWITCHING PERFORMANCE									
Propagation Delays									
Input to Output HIGH		+25°C		7			7		ns
Input to Output LOW		+25°C		7			7		ns
Latch Enable to Output HIGH		+25°C		7			7		ns
Latch Enable to Output LOW		+25°C		7			7		ns
Delta Delay Between Outputs		+25°C		2			2		ns
Latch Enable									
Minimum Pulse Width	12	+25°C		2	3		2	3	ns
Minimum Setup Time	12	+25°C		1	2		1	2	ns
Minimum Hold Time	12	+25°C		1	2		1	2	ns
POWER SUPPLY[6]									
Positive Supply Current (+5.0V)	1,2,3	Full		30	35		30	35	mA
Negative Supply Current (−6.0V)	1,2,3	Full		26	32		26	32	mA
Power Supply Rejection Ratio[7]		Full		65			65		dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedance . . .
AD9686 Metal Can $\theta_{JA} = 172°C/W; \theta_{JC} = 52°C/W$
AD9686 Ceramic $\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD9686 LCC $\theta_{JA} = 102°C/W; \theta_{JC} = 45°C/W$

[4]Military subgroups apply to military qualified devices only.

[5]$R_S = 100\Omega$.

[6]Supply voltage should remain stable within ±5% for normal operation.

[7]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

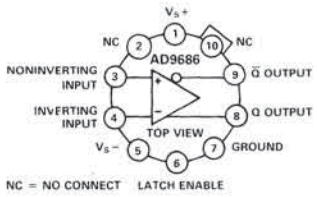
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated oper. temp.
Subgroup 3 – Static tests at min rated oper. temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated oper. temp.
Subgroup 6 – Dynamic tests at min rated oper. temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated oper. temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated oper. temp.
Subgroup 11 – Switching tests at min rated oper. temp.
Subgroup 12 – Periodically sample tested.

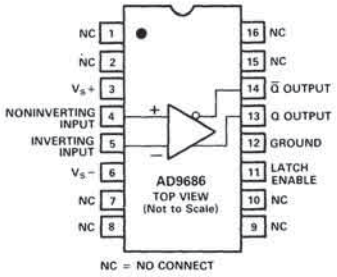
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
$-V_S$	– Negative supply terminal, nominally −6.0V.
LATCH ENABLE	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode.
GROUND	– Analog and digital ground.
Q OUTPUT	– One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE for additional information.
$\overline{Q}$ OUTPUT	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE for additional information.
NC	– "NO CONNECT" pins are not internally connected.

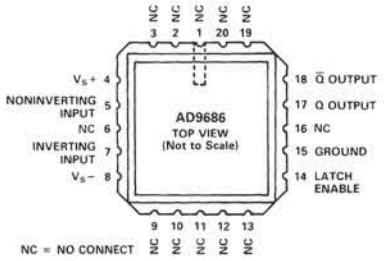
PINOUT CONFIGURATIONS



TO-100
10-Pin Can

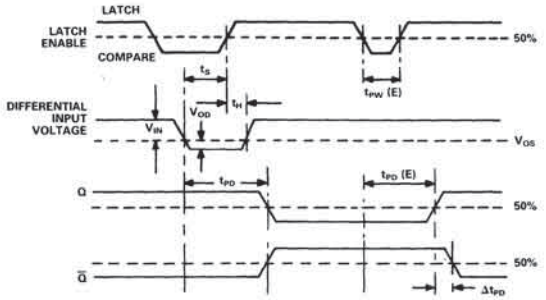


16-Pin DIP



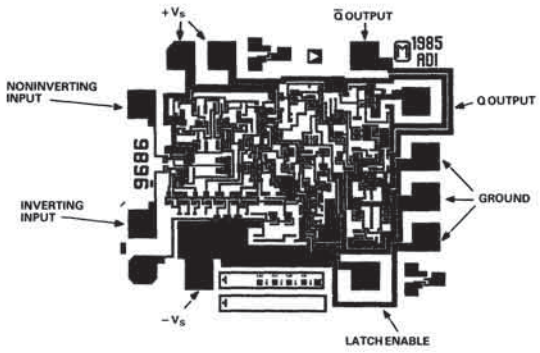
20-Pin LCC

SYSTEM TIMING DIAGRAM



t_S – Minimum Setup Time
t_H – Minimum Hold Time
t_{PD} – Input to Output Delay
$t_{PD}(E)$ – LATCH ENABLE to Output Delay
$t_{PW}(E)$ – Minimum LATCH ENABLE Pulse Width
V_{OS} – Input Offset Voltage
V_{OD} – Overdrive Voltage
Δt_{PD} – Delta Delay Between Complementary Outputs

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	59×50×18 (max) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

ANALOG DEVICES

Ultrafast Comparators

AD96685/AD96687

FEATURES
2.5ns Propagation Delay
0.5ns Latch Setup Time
90dB CMRR
+5V, −5.2V Supply Voltages

APPLICATIONS
High-Speed Triggers
High-Speed Line Receivers
Peak Detectors
Threshold Detectors

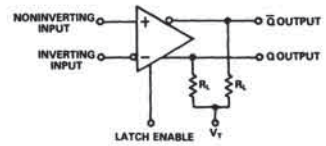
GENERAL DESCRIPTION

The AD96685 and the AD96687 are ultrafast voltage comparators. The AD96685 and the AD96687 are manufactured in a high-performance bipolar process which allows improved speed and dc accuracy. The AD96685 is a single comparator with a 2.5ns propagation delay, 50ps dispersion, and the AD96687 is an equally fast dual comparator.

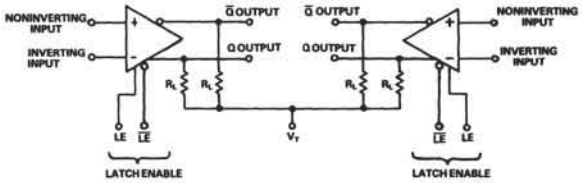
Both devices employ a high-precision differential input stage with a common-mode range from −2.5V to +5.0V. The AD96685 and the AD96687 provide complementary digital outputs which are fully ECL compatible. The output stage is capable of driving 50Ω terminated transmission lines given the 30mA output drive capacity. In addition to this, a latch enable input is provided, allowing operation in either a sample-hold mode or a track-hold mode.

The AD96685 and the AD96687 are both available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. The AD96685 is available in a 10-pin TO-100 metal can, and a 16-pin ceramic package. The AD96687 is available in a 16-pin ceramic package. Both comparators are also available in an extended temperature range LCC package.

AD96685/AD96687 FUNCTIONAL BLOCK DIAGRAMS



AD96685



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V, OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD96687

ORDERING INFORMATION

Device	Type	Temperature Range	Description	Package Options*
AD96685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BQ	Single	−25°C to +85°C	16-Pin Cerdip, Industrial	Q-16
AD96685TE	Single	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96685TH	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD96685TQ	Single	−55°C to +125°C	16-Pin Cerdip, Extended Temperature	Q-16
AD96687BQ	Dual	−25°C to +85°C	16-Pin Cerdip, Industrial	Q-16
AD96687TE	Dual	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96687TQ	Dual	−55°C to +125°C	16-Pin Cerdip, Extended Temperature	Q-16

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6.5V
Negative Supply Voltage ($-V_S$) . . . . . −6.5V
Input Voltage Range[2] . . . . . ±5V
Differential Input Voltage 5.5V
Latch Enable Voltage . . . . . $-V_S$ to 0V
Output Current 30mA
Power Dissipation AD96685 . . . . . 500mW
AD96687 . . . . . 600mW

Operating Temperature Range[3]
AD96685/87/BH/BQ . . . . . −25°C to +85°C
AD96685/87/TE/TH/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

			Industrial Temp. Range −25°C to +85°C						Military Temp. Range −55°C to +125°C						
			AD96685BH/BQ			AD96687BQ			AD96685TE/TH/TQ			AD96687TE/TQ			
Parameter	Mil[4] Sub Group	Temp	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS															
Input Offset Voltage[5]	1	+25°C		1	2		1	2		1	2		1	2	mV
	2,3	Full			3			3			3			3	mV
Input Offset Drift		Full		20			20			20			20		µV/°C
Input Bias Current	1	+25°C		7	10		7	10		7	10		7	10	µA
	2,3	Full			13			13			13			13	µA
Input Offset Current	1	+25°C		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	2,3	Full			1.2			1.2			1.2			1.2	µA
Input Resistance		+25°C		200			200			200			200		kΩ
Input Capacitance		+25°C		2			2			2			2		pF
Input Voltage Range[6]	1,2,3	Full	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	V
Common-Mode Rejection Ratio	1,2,3	Full	80	90		80	90		80	90		80	90		dB
ENABLE INPUT															
Logic "1" Voltage	1,2,3	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	1,2,3	Full			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	1,2,3	Full			40			40			40			40	µA
Logic "0" Current	1,2,3	Full			5			5			5			5	µA
DIGITAL OUTPUTS[7]															
Logic "1" Voltage	1,2,3	Full	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	1,2,3	Full			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[7]															
Propagation Delays[8]															
Input to Output HIGH	9	+25°C		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	9	+25°C		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	9	+25°C		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	9	+25°C		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersion[9]		+25°C		50			50			50			50		ps
Latch Enable															
Minimum Pulse Width	12	+25°C		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	12	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	12	+25°C		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[10]															
Positive Supply Current (+5.0V)	1,2,3	Full		8	9		15	18		8	9		15	18	mA
Negative Supply Current (−5.2V)	1,2,3	Full		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[11]	1,2,3	Full	60	70		60	70		60	70		60	70		dB

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Under no circumstances should the input voltages exceed the supply voltages.
[3]Typical thermal impedances . . .
AD96685 Metal Can $\theta_{ja} = 172°C/W, \theta_{jc} = 52°C/W$
AD96685 Ceramic $\theta_{ja} = 115°C/W; \theta_{jc} = 57°C/W$
AD96685 LCC $\theta_{ja} = 172°C/W; \theta_{jc} = 65°C/W$
AD96687 Ceramic $\theta_{ja} = 115°C/W; \theta_{jc} = 57°C/W$
AD96687 LCC $\theta_{ja} = 82°C/W; \theta_{jc} = 31°C/W$
[4]Military subgroups apply to military qualified components only.
[5]$R_S = 100\Omega$.
[6]Input Voltage Range can be extended to −3.3V if $-V_S = -6.0V$.
[7]Outputs terminated through 50Ω to −2.0V.
[8]Propagation delays measured with 100mV pulse (10mV overdrive), to 50% transition point of the output.
[9]Change in propagation Delay from 100mV to 1V input overdrive.
[10]Supply voltages should remain stable within ±5% for normal operation.
[11]Measured at ±5% of $+V_S$ and $-V_S$.
Specifications subject to change without notice.

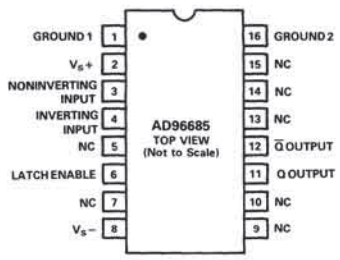
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated oper. temp.
Subgroup 3 – Static tests at min rated oper. temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated oper. temp.
Subgroup 6 – Dynamic tests at min rated oper. temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated oper. temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated oper. temp.
Subgroup 11 – Switching tests at min rated oper. temp.
Subgroup 12 – Periodically sample tested.

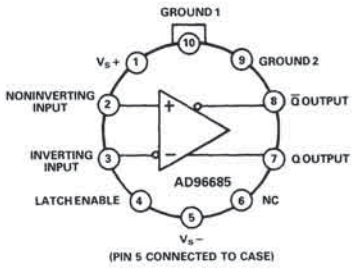
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

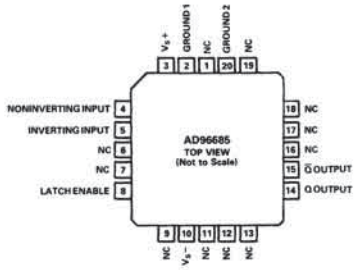
PIN DESIGNATIONS



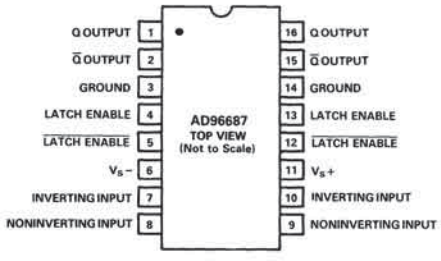
AD96685BQ/TQ
TOP VIEW



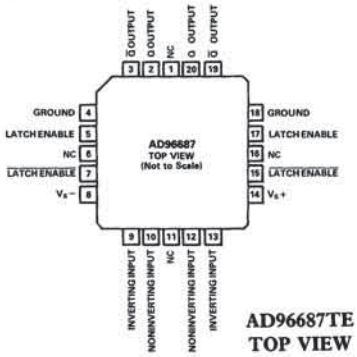
AD96685BH/TH
TOP VIEW



AD96685TE
TOP VIEW

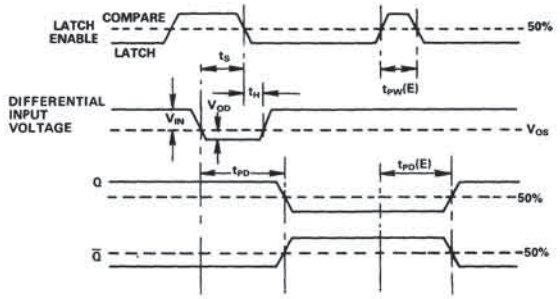


AD96687BQ/TQ
TOP VIEW



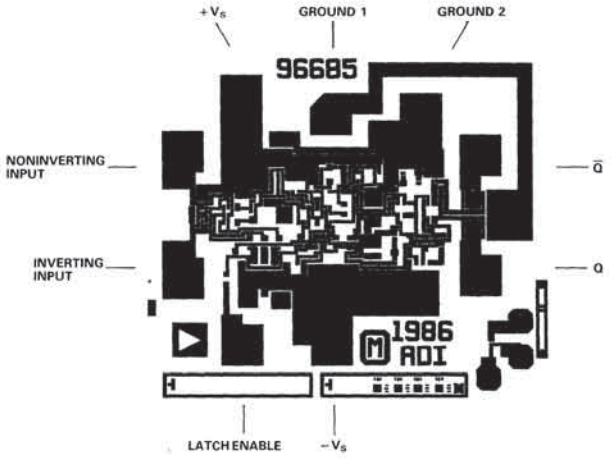
AD96687TE
TOP VIEW

SYSTEM TIMING DIAGRAM

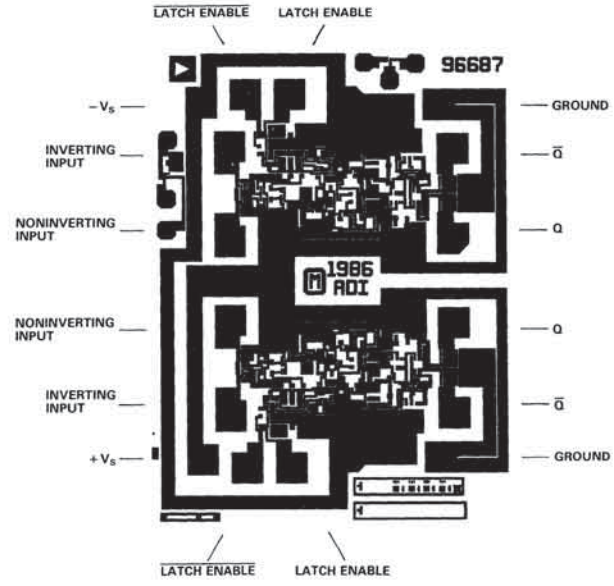


t_S	–	Minimum Setup Time
t_H	–	Minimum Hold Time
t_{PD}	–	Input to Output Delay
$t_{PD}(E)$	–	LATCH ENABLE to Output Delay
$t_{PW}(E)$	–	Minimum LATCH ENABLE Pulse Width
V_{OS}	–	Input Offset Voltage
V_{OD}	–	Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	AD96685	44 × 50 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		$-V_S$
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding



Die Dimensions	AD96687	77 × 60 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		$-V_S$
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding

APPLICATIONS INFORMATION

The AD96685/87 comparators are very high-speed devices. Consequently, high-speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD96685/87 design is the use of a low impedance ground plane.

Another area of particular importance is power supply decoupling. Normally, both power supply connections should be separately decoupled to ground through 0.1μF ceramic and 0.001μF mica capacitors. The basic design of comparator circuits makes the negative supply somewhat more sensitive to variations. As a result more attention should be placed on insuring a "clean" negative supply.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The $\overline{\text{LATCH ENABLE}}$ input of the AD96687 should be tied to −2.0V or left "floating", to disable the latching function. An alternate use of the LATCH ENABLE input is as a hysteresis control input. By varying the voltage at the LATCH ENABLE input for the AD96685 and the differential voltage between both latch inputs for the AD96687, small variations in the hysteresis can be achieved.

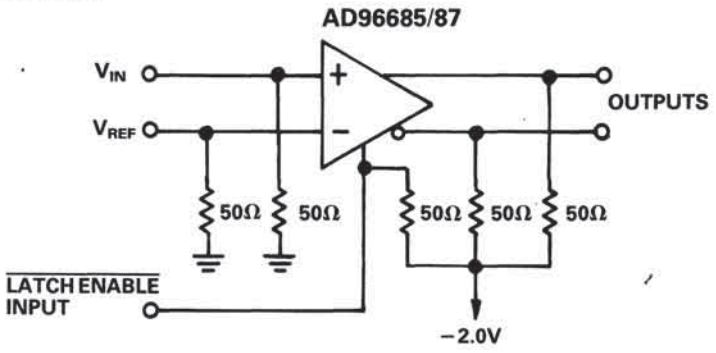
Occasionally, one of the two comparator stages within the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float". The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LATCH ENABLE input.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD96685/87 are designed to be terminated through 50Ω resistors to −2.0V, or any other equivalent ECL termination. If high-speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

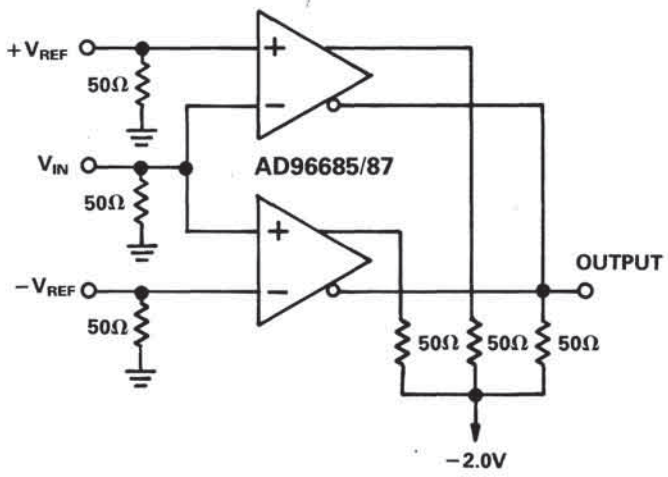
The AD96685/87 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100mV to 1V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD96685/87 is far less sensitive to input variations than most comparator designs.

Typical Applications

HIGH-SPEED SAMPLING CIRCUIT



HIGH-SPEED WINDOW COMPARATOR



Instrumentation Amplifiers
Contents

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AD522 – High Accuracy, Data Acquisition Instrumentation Amplifier . . . . . 4 – 21
AD524 – Precision Instrumentation Amplifier . . . . . 4 – 25
AD526 – Software Programmable Gain Amplifier . . . . . 4 – 37
AD624 – Precision Instrumentation Amplifier . . . . . 4 – 49
AD625 – Programmable Gain Instrumentation Amplifier . . . . . 4 – 61

4

Selection Guide
Instrumentation Amplifiers

Model	Offset Voltage μV	Offset Drift μV/°C	Bias Current nA	GBWP MHz	Gain Ranges	Page	Notes
AD365	200	2	50	20	1, 10, 100, 500	4 – 7	Digitally programmable, w/T/H
AD521	1000	2	40	40	0.1 – 10000	4 – 15	Resistor programmable
AD522	100	2	25	0.3	1 – 1000	4 – 21	Resistor programmable
AD524	50	0.5	15	25	1, 10, 100, 1000	4 – 25	Pin programmable
AD526	250	–	0.15	6	1, 2, 4, 8, 16	4 – 37	Digitally programmable, μP interface, single-ended
AD624	25	0.25	15	25	1, 100, 200, 500, 1000	4 – 49	Pin programmable
AD625	25	0.25	15	25	1 – 10000	4 – 61	Resistor programmable, low cost

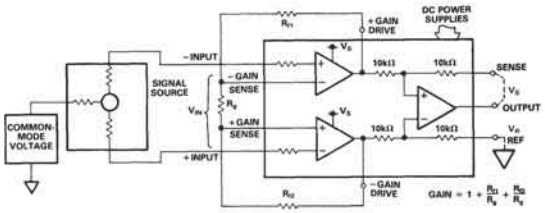
4

Orientation
Instrumentation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal differential instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.



R_{G1}, R_{G2}, R_G ARE EXTERNAL GAIN-SETTING RESISTORS

An amplifier circuit which is optimized for performance as an instrumentation amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts and biological probes; preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition; and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Single-ended software-programmable gain amplifiers, such as the AD526, with fixed binary gains of 1, 2, 4, 8, etc., are often listed with instrumentation amplifiers. They are used in systems having a "clean" signal ground to provide appropriate amounts of digitally controlled gain to normalize the level of the output signal to correspond to a large fraction of the input range of an A/D converter; they can thus be used as components of a floating-point A/D conversion system to preserve accuracy over a wide dynamic range. See also "Data-Acquisition Subsystems" in the *Data Conversion Products Databook*.

Instrumentation amplifiers are usually chosen in preference to user-assembled op-amp circuitry because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consider an *isolation amplifier*.

NOTES

[1]Application Note: "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, available upon request.

[2]*Transducer Interfacing Handbook*, D.H. Sheingold, ed., 1980. $14.50, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2]

INSTRUMENTATION AMPLIFIER ARCHITECTURE

Basic Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain programming, an "output" terminal and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim. Gain is programmable in three ways:

- The gain of basic amplifiers, such as the AD521, AD522 and AD625, is established by connecting resistors externally. Such circuits are generally used for dedicated fixed-gain applications.
- Pin-programmable amplifiers, such as the AD524 and AD624, have a set of internal resistors; a limited set of fixed gains in the range of 1 to 1,000 are chosen by appropriately interconnecting the resistors via external pins. The connections can be fixed or switched via DIP switches or reed relays (if CMOS switches are used, the *on* resistance of the switches must be considered in series with the internal gain resistors).
- Digitally (or "software-") programmable amplifiers are completely self-contained, with gains set by a 2-, 3- or 4-bit digital control word. These devices include the AD365 (with gains of 1, 10, 100, 500) and the AD526 (with binary gains of 1-16, cascadable to 256).

Except for the AD521, the differential input amplifiers use variations of the well known three-op-amp configuration, consisting of a differential input-output gain stage and a subtractor stage. Gain ($\ll$1V/V) is set by the choice of a single gain-setting resistor, R_G. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The V_S and V_R terminals may be used for remote sensing – to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances) when driving the V_S and V_R inputs,

in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $R_L = 2k\Omega$, and $T_A = +25°C$, unless otherwise specified." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be in the middle of a distribution.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN: These specifications refer to the linear transfer function of the device; for example, the AD524 gain equation is:

$$G = 1 + \frac{40{,}000}{R_G} \text{ V/V}$$

The value of R_G for a given gain value is:

$$R_G = \frac{40{,}000}{G-1} \ \Omega$$

For example, if G is to be 200V/V,

$$R_G = 201 \text{ ohms.}$$

Gain Range: Specified at 1 to 1,000, for example, resistor-programmable devices may work at higher gains (1V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy"): The number given by this specification describes deviation from the gain equation when R_G is at its nominal value. The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to A/D converter.

Nonlinearity (or Gain Nonlinearity): Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best-straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature: These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range, and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing) and thermal gradients (long tails).

GAIN-BANDWIDTH PRODUCT (GBWP) – the product of the highest gain and its corresponding bandwidth – is a rough figure of merit for bandwidth as an aid to the preliminary screening process. However, since gain and bandwidth are not necessarily in exact inverse proportion, it can be a misleading specification, especially at the lower gains, if interpreted literally.

VOLTAGE OFFSET: Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[1] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1,000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1,000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1,000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1,000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset."

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD624C is specified at 0.25μV/°C. Thus, the output drift is (0.25μV/°C × G) + 10μV/°C at any gain, G, in the range.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

[1]**There is a good explanation of the specification of offset in the Application Note: "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, available upon request.**

INPUT BIAS AND OFFSET CURRENTS: Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction leakage of FETs. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

> *Important Note*
> Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used.

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV) at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = $20 \log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common-mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

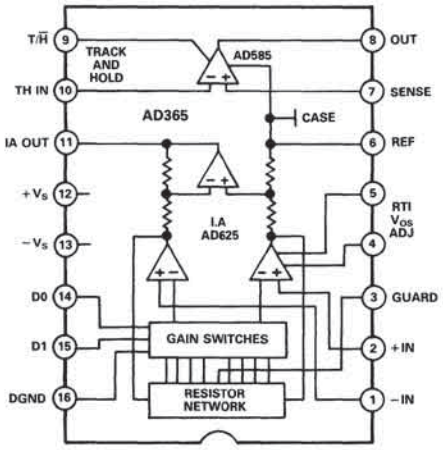
Programmable Gain & T/H DAS Amplifier

AD365

FEATURES
Software Programmable Gain (1, 10, 100, 500)
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP

APPLICATIONS
Digitally Controlled Gain Amplifier
Auto-Gain Ranging Amplifier
Wide Dynamic Range Measurement System
Gain Selection/Channel Amplifier
Transducer/Bridge Amplifier
Test Equipment

AD365 FUNCTIONAL BLOCK DIAGRAM



HIGHLIGHTS

The AD365 is a two stage data acquisition system (DAS) front end consisting of a digitally selectable gain amplifier followed by an independent track/hold amplifier. The programmable gain amplifier features differential inputs for excellent common-mode rejection, high open loop gain for superior linearity, and fast settling for use in multiplexed high speed systems. The track/hold amplifier features high open loop gain for 12-bit compatible linearity, internal hold capacitor for high reliability, and fast acquisition time for use with multichannel systems. Both amplifiers are capable of being used separately and are specified as independent function blocks.

GENERAL DESCRIPTION

The AD365 is comprised of the AD625 monolithic precision instrumentation amplifier to provide a precision differential input, the AD7502 monolithic CMOS multiplexer to handle gain switching, a precision thin-film resistor network, and the AD585 monolithic track and hold amplifier with internal hold capacitor.

The input stage provides high common-mode rejection, low noise, fast settling at all gains, and low drift over temperature. The gains of 1, 10, 100, and 500 are digitally selected with the two gain control lines which are 5V CMOS compatible.

The track and hold amplifier section is ideally suited for high speed 12-bit applications where fast settling, low noise, and low sample-to-hold offset are critical. The T/H mode is controlled with a single input line which can be tied to the status output line of the accompanying A/D converter.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

AD365AM	Min	Typ	Max	Units
PGA GAIN				
Inaccuracy[1]				
@ G = 1, 10, 100		0.02	0.05	%
@ G = 500		0.04	0.1	%
Nonlinearity				
@ G = 1, 10, 100			0.005	%
@ G = 500			0.01	%
Drift				
@ G = 1		1	5	ppm/°C
@ G = 10, 100, 500		3	10	ppm/°C
PGA OFFSET (May be Nulled at Input and Output)				
Input Offset Voltage (RTI)		25	200	µV
vs. Temperature		0.1	2	µV/°C
vs. Common-Mode Voltage		0.5	3.2	µV/V
vs. Supply Voltage		1	10	µV/V
Output Offset Voltage (RTO)		1	5	mV
vs. Temperature		30	150	µV/°C
vs. Common-Mode Voltage		60	316	µV/V
vs. Supply Voltage		60	316	µV/V
PGA INPUT				
Common- Mode and Differential Impedance		$10^9 \| 5$		Ω|pF
Differential Input Voltage, Linear	10	12		V
Common-Mode Voltage, Linear		$12 - V_{DIFF} \times G/2$		V
Input Stage Noise 0.1 to 10Hz		0.2		µV p-p
Input Stage Noise Density @ 1kHz		4		$nV/\sqrt{Hz}$
Bias Current		5	50	nA
vs. Temperature		50		pA/°C
Offset Current		2	20	nA
vs. Temperature		20		pA/°C
Noise Current (0.1 to 10Hz)		60		pA p-p
PGA OUTPUT				
Voltage 2kΩLoad	10	12		V
Output Impedance		0.2		Ω
Short Circuit Current		25		mA
Capacitive Load		500		pF
Output Stage Noise 0.1 to 10Hz		10		µV p-p
Output Stage Noise Density @ 1kHz		75		$nV/\sqrt{Hz}$
Guard Voltage		$(V_{+IN} + V_{-IN})/2$		V
Guard Offset		−550		mV
PGA DYNAMIC RESPONSE				
Small Signal − 3dB				
G = 1		800		kHz
G = 10		400		kHz
G = 100		150		kHz
G = 500		40		kHz
Full Power Bandwidth G = 1 @ V_O = 20V p-p		60		kHz
Slew Rate		4		V/µs
Settling Time to 0.01% @ V_O = 20V p-p				
G = 1, 10		8	10	µs
G = 100		12	15	µs
G = 500		40	50	µs
Gain Switching Time		1.5		µs
Overdrive Recovery Time V_{IN} = 15V @ G = 1		7		µs
PGA DIGITAL INPUTS				
Logic Low	0		0.8	V
Logic High	3.0		$+V_S$	V
Current, I_{INH} or I_{INL}		0.01	1	µA

AD365AM	Min	Typ	Max	Units
TRACK AND HOLD AMPLIFIER SECTION				
TRANSFER CHARACTERISTICS				
Open Loop Gain V_O = 10V, R_L = 2k	100k	200k		V/V
Nonlinearity @ G = +1			0.005	% FSR
Output Voltage R_L = 2kΩ	10	12		V
Capacitive Load		100		pF
Short Circuit Current		25		mA
TRACK MODE DYNAMICS				
Acquisition Time to 0.01% 10V Step		2	3	µs
20V Step		4	5	µs
Small Signal Bandwidth −3dB		2		MHz
Full Power Bandwidth (20V p-p)		120		kHz
Slew Rate		10		V/µs
TRACK/HOLD SWITCHING				
Aperture Time		35		ns
Aperture Uncertainty		0.5		ns
Switching Transient		40		mV
Settling Time to 2mV		0.5		µs
HOLD MODE				
Droop Rate @ +25°C		0.3	1	V/sec
from $T_{AMBIENT}$ to T_{MAX}		Doubles/10°C		V/sec
Feedthrough		25		µV/V
Pedestal, Offset @ +25°C		2	3	mV
Over Temperature		3		mV
T/H ANALOG INPUT				
Bias Current		0.1	2	nA
Over Temperature		0.2	5	nA
Offset Voltage			2	mV
Over Temperature			3	mV
vs. Common Mode		25	100	µV/V
vs. Supplies		100	316	µV/V
Input Impedance		10^{12}‖10		Ω‖pF
Noise Density @ 1kHz		50		nV/√Hz
Noise 0.1Hz to 10Hz		10		µV p-p
T/H DIGITAL INPUT CHARACTERISTICS				
Logic Low (Hold Mode)	0		0.8	V
Logic High (Track Mode)	2.0		$+V_S$	V
Input Current		10	50	µA
AD365 POWER REQUIREMENTS				
Positive Supply Range	+11		+17	V
Negative Supply Range	−11		−17	V
Quiescent Current		12	16	mA
Power Dissipation		360	550	mW
Warm-Up Time to Specification		5		Minutes
Ambient Operating Temperature	−25		+85	°C
Package Thermal Resistance (θ_{ja})		60		°C/W
AD365 ABSOLUTE MAXIMUM RATINGS				
Positive Supply $+V_S$	−0.3		+17	V dc
Negative Supply $-V_S$	+0.3		−17	V dc
Analog Input Voltage	$-V_S$		$+V_S$	V
Analog Input Current	−10		+10	mA
Digital Input Voltage	−0.3		$+V_S$	V
T/H Differential V_{IN}			±30	V
Storage Temperature	−65		+150	°C
Lead Soldering, 10 Sec			300	°C
Short Circuit Duration		Indefinite		
PACKAGE OPTION[2] DH-16B				

NOTE
[1]Gain = 10, 100 and 500 are trimmed and tested ratiometric to G = 1.
[2]See Section 16 for package outline information.
Specifications subject to change without notice.

TYPICAL CHARACTERISTICS (@ +25°unless otherwise noted)

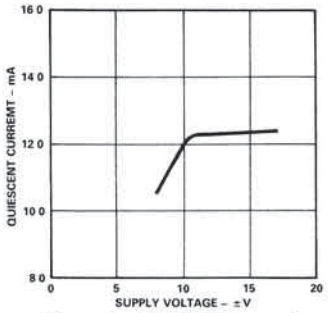


Figure 1. AD365 Quiescent Current vs. Supply Voltage

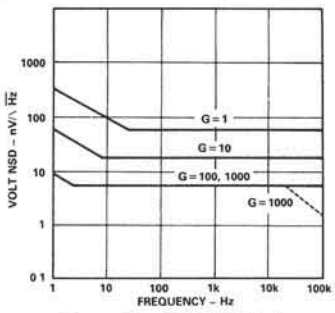


Figure 2. PGA RTI Noise Spectral Density vs. Gain

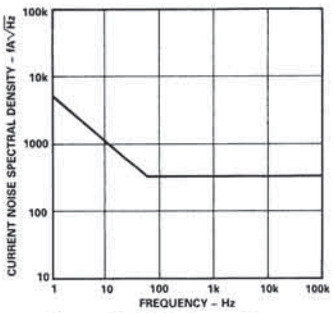


Figure 3. PGA Input Current Noise

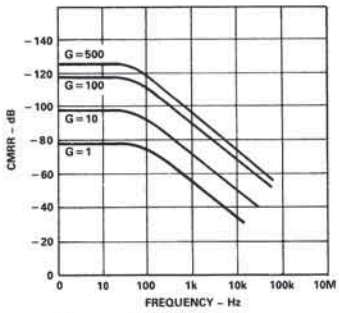


Figure 4. PGA CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

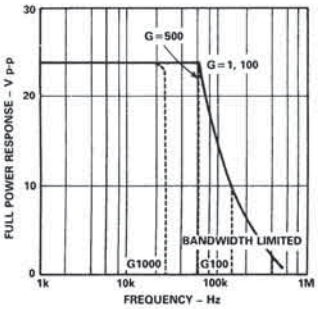


Figure 5. PGA Large Signal Frequency Response

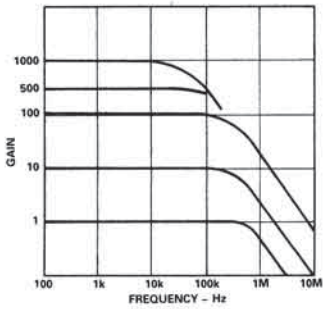


Figure 6. PGA Gain vs. Frequency

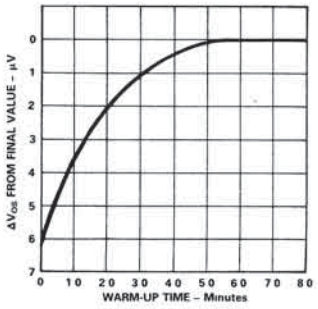


Figure 7. PGA Offset Voltage, RTI, Turn On Drift

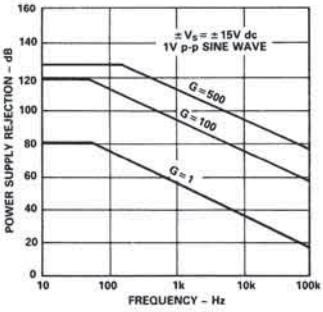


Figure 8. PGA PSRR vs. Frequency

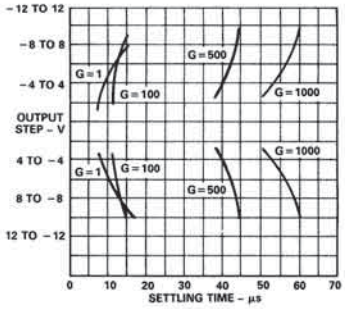


Figure 9. PGA Settling Time to 0.01%

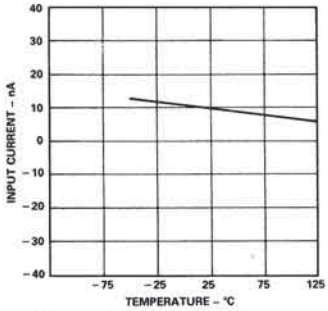


Figure 10. PGA Input Bias Current vs. Temperature

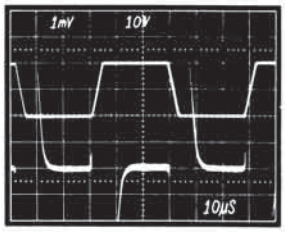


Figure 11. PGA Large Signal Pulse Response and Settling Time, G = 100

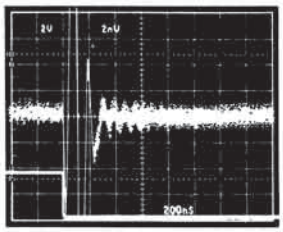


Figure 12. Sample-to-Hold Settling Time

The AD365 PGA section uses the AD625 monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp stage (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G$ + 1) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

Digital gain control is provided using the D0 and D1 inputs (pins 14 and 15) which are decoded internally in the gain switching AD7502 as shown in Figure 15 below. The switch selects the resistance R_G from the laser trimmed resistor network according to the following gain select table.

D1	D0	PGA GAIN
0	0	1
0	1	10
1	0	100
1	1	500

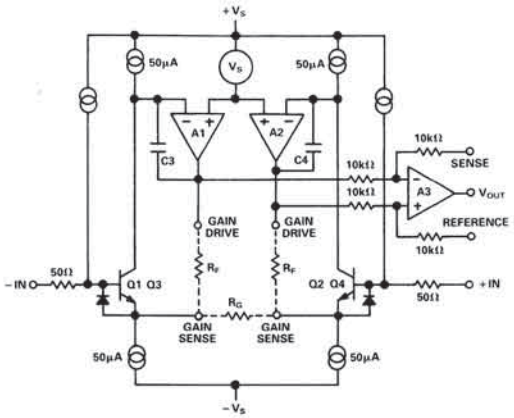


Figure 13. Simplified Circuit of the PGA

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the PGA; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is (R_G + 300)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 80Ω @ G = 500), the maximum overload voltage the PGA can withstand, continuously, is approximately ±5V. Figure 14 shows the external components

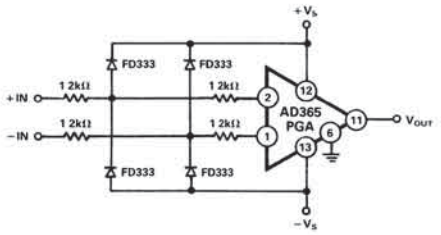


Figure 14. Input Protection Circuit for PGA

necessary to protect the PGA under all overload conditions at any gain. The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered.

4

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±2V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered, however, that the total output swing, to be shared between signal and reference offset, should be ±10 volts (from ground).

The PGA section reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625, a reference source resistance will unbalance the CMR trim by the ratio of 10kΩ/R_{REF}. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 15. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

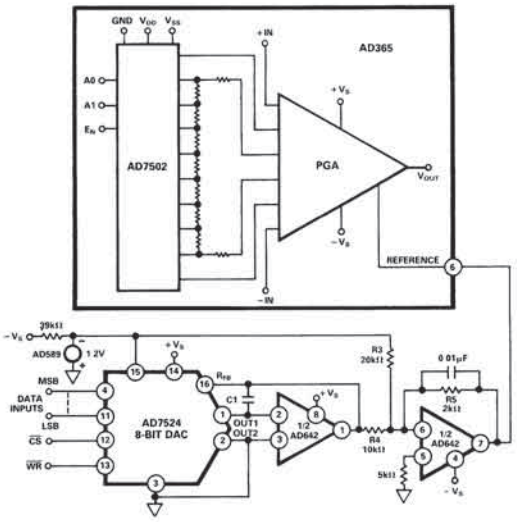


Figure 15. Software Controllable Offset

The circuit of Figure 15 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$. To be symmetrical about 0V, R_3 must be equal to $2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 15 is ±120mV, and the offset is incremented in steps of 0.9375mV/LSB.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains. Input errors dominate at high gains and output errors dominate at low gains.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain ×input error) + output error

The AD365 provides for input offset voltage adjustment (see Figure 16). This simplifies nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

Output offset adjustment is normally provided by the A/D converter offset adjustment which will compensate for the output offset of the PGA, offset of the T/H amplifier, and offset of the A/D.

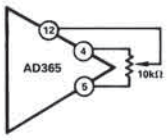


Figure 16. Input Voltage Offset Adjustment

COMMON-MODE REJECTION

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 17 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

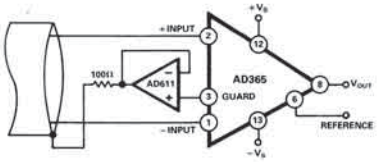


Figure 17. Common-Mode Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 18). Since the AD365 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

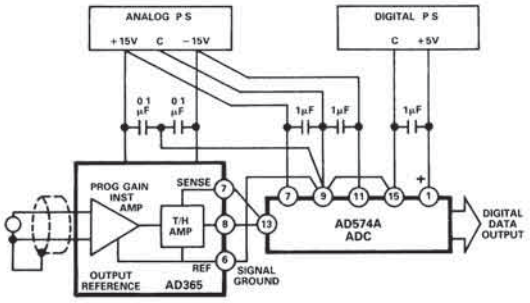


Figure 18. Basic Grounding Practice

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 19.

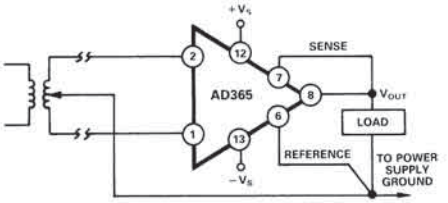


Figure 19a. Ground Returns for Bias Currents with Transformer Coupled Inputs

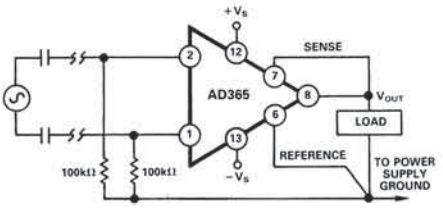


Figure 19b. Ground Returns for Bias Currents with ac Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 20 provides a hardware solution.

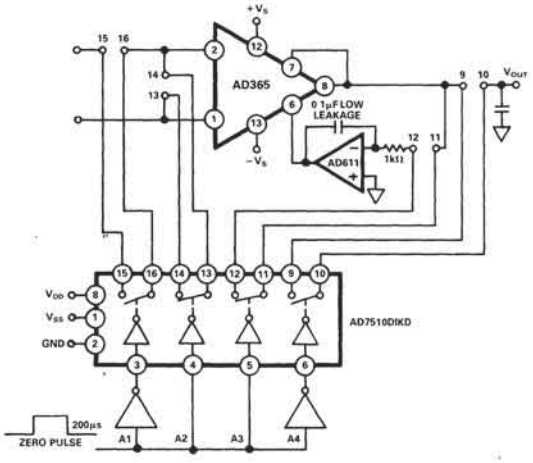


Figure 20. Auto-Zero Circuit

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD365) remain isothermal. This includes the input leads (1, 2). In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. In the case of a resistive transducer, a capacitor across the input working against the internal resistance of the transducer may suffice to provide an RC filter. These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 1 and 2, to preserve high ac CMR.

THEORY OF OPERATION – T/H SECTION

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 21 shows pictorially the track-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Track-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Track Transition.

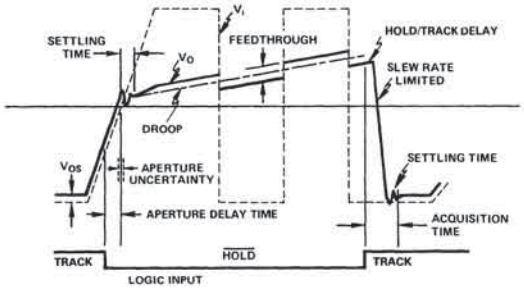


Figure 21. Pictorial Showing Various T/H Characteristics

TRACK-TO-HOLD TRANSITION

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 22 will result.

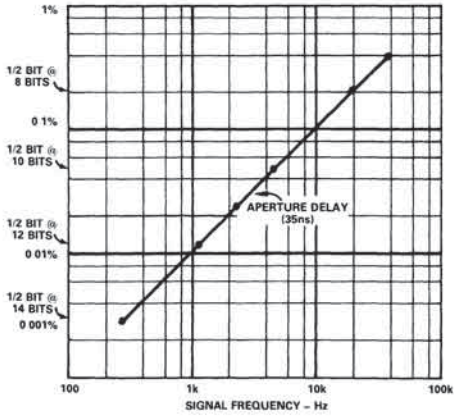


Figure 22. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the track-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then T/H trigger uncertainty/jitter and internal aperture jitter which are the variations in aperture delay time from sample-to-sample remain. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi \text{ (Aperture Jitter)}}$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5\times10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V\text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt.

$$\frac{dV\text{ max}}{dt} = \frac{\Delta V\text{ max}}{t_{CONV}}$$

The maximum $\frac{dV\text{ max}}{dt}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \le \frac{dV\text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

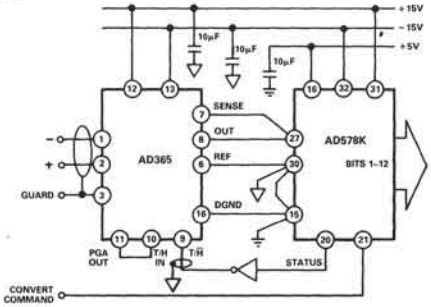


Figure 23. A/D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

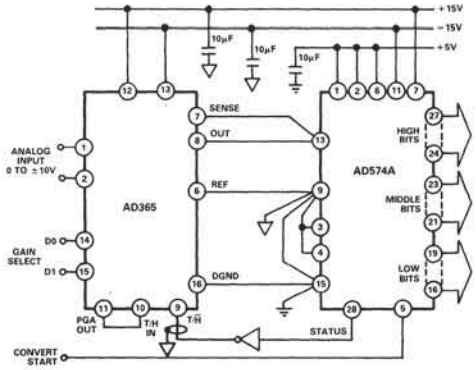


Figure 24. 12-Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

ANALOG DEVICES

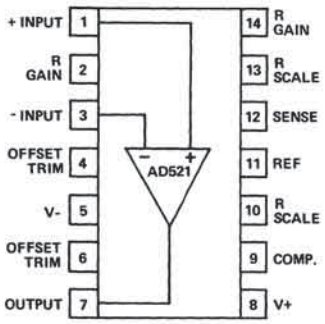
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

- Programmable Gains from 0.1 to 1000
- Differential Inputs
- High CMRR: 110dB min
- Low Drift: 2μV/°C max (L)
- Complete Input Protection, Power ON and Power OFF
- Functionally Complete with the Addition of Two Resistors
- Internally Compensated
- Gain Bandwidth Product: 40MHz
- Output Current Limited: 25mA
- Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
- Chips are Available

AD521 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521SD/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G$ V/V	*	*	*
Error from Equation	(±0 25–0 004G)%	*	*	*
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	*	0 1% max	*
Gain Temperature Coefficient	±(3 ±0 05G)ppm/°C	*	*	±(15 ±0 4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0 1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1 0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1 5mV max (0 5mV typ)	1 0mV max (0 5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	0 005V_{OS_O}/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	3 x 10^9Ω‖1.8pF	*	*	*
Common Mode Input Impedance (Note 8)	6 x 10^{10}Ω‖3 0pF	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0 1Hz to 10Hz (Note 10)	$\sqrt{(0\ 5G)^2 + (225)^2}$ μV	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1\ 2G)^2 + (50)^2}$ μV	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTION[1]				
Ceramic (D-14)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES
[1] See Section 16 for package outline information.

*Specifications same as AD521JD.
**Specifications same as AD521KD

Specifications subject to change without notice

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S –0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 seperate 10 second periods with the test circuit of Figure 8.

4

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

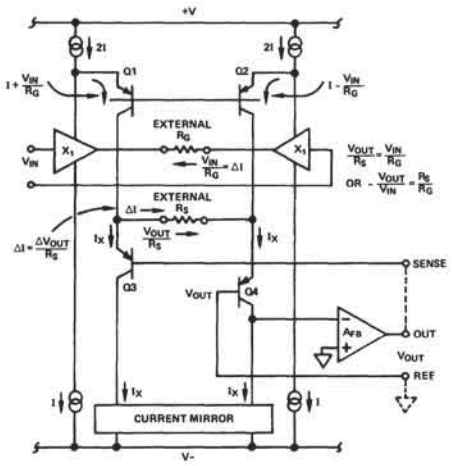


Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V especially for gain equal to or less than 1.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

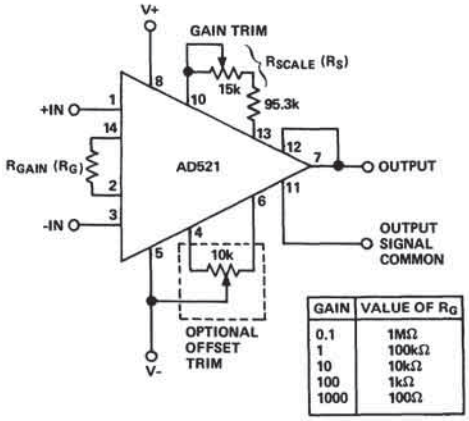
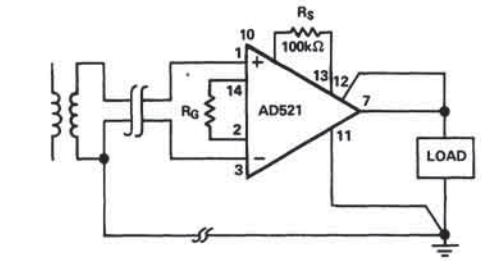


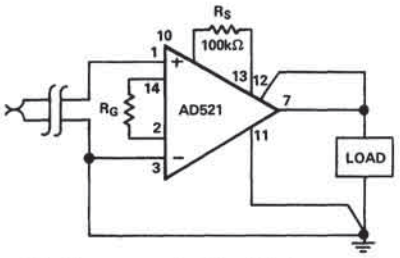
Figure 2. Operating Connections for AD521

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

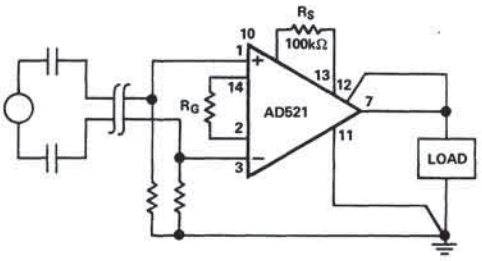
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

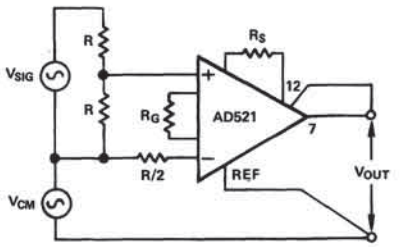


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$

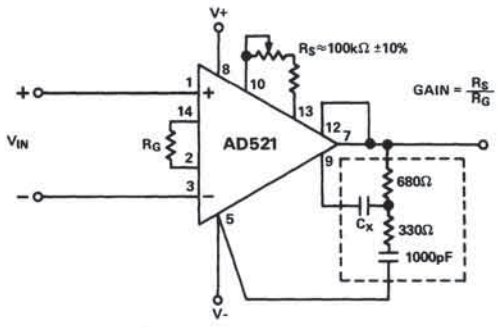
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V- to the output with little or no attenuation. Therefore, it is advisable to decouple the V- supply line to the output common or to pin 11.[1]



$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

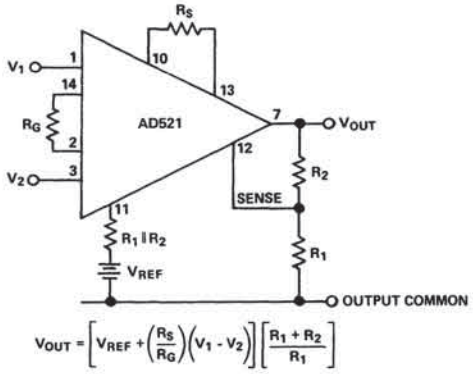
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)(V_1 - V_2)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

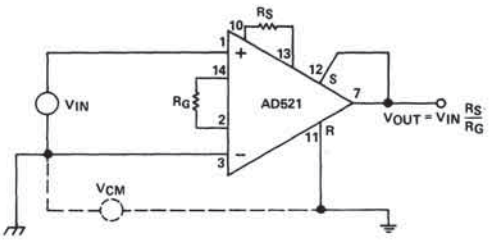


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

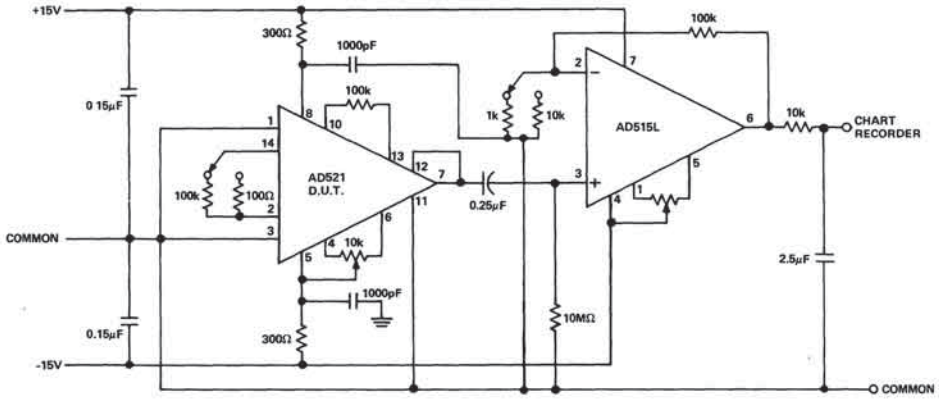


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

Versatility

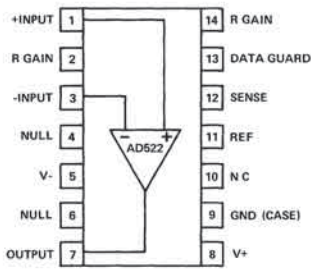
- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

AD522 FUNCTIONAL BLOCK DIAGRAM

14-PIN DIP



PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gages, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\,\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the extended aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

SPECIFICATIONS[1] (typical @ +V_S = ±15V, R_L = 2kΩ & T_A = +25°C unless otherwise specified)

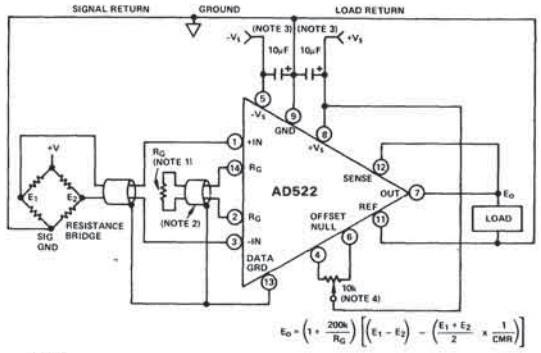
MODEL	AD522AD	AD522BD	AD522SD
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0 2% max	0.05% max	**
G = 1000	1.0% max	0 2% max	**
Nonlinearity, max (see Fig 4)			
G = 1	0 005%	0 001%	**
G = 1000	0 01%	0 005%	**
vs Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1 5kHz	*	*
Slew Rate	0 1V/μs	*	*
Settling Time to 0 1%, G = 100	0 5ms	*	*
to 0 01%, G = 100	5ms	*	*
to 0 01%, G = 10	2ms	*	*
to 0 01%, G = 1	0 5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs Temperature, max (see Fig 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
1 < G < 1000	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0 2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	*	*
vs Temperature	±100pA/°C	*	*
Input Offset Current			
Initial max, +25°C	±20nA	*	*
vs Temperature	±100pA/°C	*	*
INPUT			
Input Impedance			
Differential	$10^9\Omega$	*	*
Common Mode	$10^9\Omega$	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rjection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig 4)			
0 1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1 5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	**
PACKAGE OPTIONS[2]			
Ceramic[3] (DH-14A)	AD522AD	AD522BD	
Metal (DH-14B)			AD522SD

NOTES
[1] Specifications guaranteed after 10 minute warm-up.
[2] See Section 16 for package outline information.
[3] Analog Devices reserves the right to ship metal package in lieu of the standard ceramic packages for A and B grades.

*Specifications same as AD522A
**Specifications same as AD522B
Specifications subject to change without notice

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



$$E_O = \left(1 + \frac{200k}{R_G}\right)\left[(E_1 - E_2) - \left(\frac{E_1 + E_2}{2} \times \frac{1}{CMR}\right)\right]$$

NOTES
1 GAIN RESISTOR R_G SHOULD BE ~5ppm/°C (VISHAY TYPE RECOMMENDED)
2 SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS WHEN NOT USED THE DATA GUARD PIN CAN BE LEFT UNCONNECTED
3 POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS
4 NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202 Y 10k) IS RECOMMENDED

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table I)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec Sheet and Fig 4)	±0.002	±0 002
Voltage Drift	$\frac{25\mu V/^\circ C}{Gain}$ + 2 0µV/°C = 4 5µV/°C R T.I. = 0 00055%/°C (from Spec Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs F vs. G, typical curve)	±0 005	±0 005
Noise, R.T.O. (0 1 to 100Hz)	15µV (p-p) R T O (from Spec Sheet, Noise vs G typical curve)	±0 0015	±0 0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec Sheet) = ±50µV/°C = ±1 25µV R T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table I. Error Sources