

Low-Power RF-ICs in Wireless Transceivers

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Introduction

It is anticipated that about 300 million portable consumer wireless devices will be in use by the year 2000 [1]. What IC technologies will enable the RF front-end of these devices? Do miniaturization and long battery-life call for architectural innovations in transceivers? What new circuit design styles will evolve in response?

There is much curiosity and speculation on these matters, yet little is known in general terms about RF-IC design, and the impact of large-scale integration and power-reduction strategies in front-ends of wireless transceivers. This paper presents a brief survey of the highlights in the application of IC technology to radios since the 1970s, and follows this with trends of what the author considers is the shape of things to come in wireless transceivers over the next few years. RF-ICs are roughly defined as integrated circuits operating in the band of frequencies from 100 MHz to 2000 MHz which covers most consumer wireless devices. MMICs, by contrast, are small-scale ICs operating at tens of GHz which are almost exclusively fabricated on III-V compound semiconductor substrates. Driven by defence applications over the past decade, they have become an established discipline. RF-ICs are principally driven by consumer needs. They are, and will continue to be, fabricated mostly in mature silicon technologies, combining analog and digital functions at relatively large levels of integration. It is the authors belief that in response to pressing demands for ubiquitous wireless access, the day of the "VLSI radio" is not that far off.

ICs in Broadcast Radio Receivers

Integrated circuits are used in one form or another in the front-end of most of today's broadcast receivers. However, it is fair to say that aside from contributing building blocks as the double-balanced mixer and the phase-locked loop, IC technology has *not* caused a profound re-thinking of radio receivers, whose architecture still resembles post-World War II radios. Some recent advances in this respect are now described.

The two most important specifications of a receiver are its *selectivity* and its *sensitivity*. Selectivity is the receiver's ability to reject adjacent channels and image frequencies, while sensitivity is its ability to detect weak input signals. The noise properties of the transistors in the front-end mainly set the sensitivity, whereas the receiver's frequency-allocation plan and quality of filters determine its selectivity. The frequency-allocation plan consists of the choice of the intermediate frequencies (IF) and of filtering to obtain a desired image suppression. In an FM receiver, for instance, as it is

difficult to make high selectivity filters at RF, a first IF of 10.7 MHz is used to ensure that the unwanted image that will superpose itself on the desired channel lies outside the FM band of 88-108 MHz, and is inherently rejected by the detector. Passive crystal filters with a 150 kHz passband centered at 10.7 MHz then reject adjacent channels. In designing a low-power, miniature FM receiver, Kasperkovitz [2] at Philips realized there are many advantages in eliminating the RF and IF filters, and implementing the required selectivity on-chip. As it was impossible to integrate the RF filters on-chip with spiral monolithic inductors, or to replace the 10.7 MHz IF crystal filters with active gyrator filters, the key step in solving this problem was to *lower the IF* from 10.7 MHz to 70 kHz. Aside from a small off-chip inductor which provides a minimum of RF filtering, the channel bandwidth is mainly defined on-chip by high-order active RC filters. The power dissipation in these filters for a given dynamic range scales down with the IF [3], as does the required operating current in the IF amplifier. The image frequency, instead of lying outside the FM band, now lies *between* FM channels (Fig.1), so it only superposes noise on to the desired signal. However, a consequence of this choice is that the ± 75 kHz frequency deviation of the desired FM channel may alias around DC to create distortion, so it is compressed to ± 15 kHz by a negative frequency feedback. This single-chip FM mono receiver [4] requires only 15 small capacitors and two inductors, making it possible to fit the entire system within a wristwatch. The IC drains 8 mA from a 4.5V battery supply.

The same idea of low-IF has been pursued at Sony for their personal entertainment broadcast receivers. The bipolar RF-ICs operate at single-battery supplies as low as 0.95 V. A recent FM radio IC implements an unusual double-superheterodyne architecture [5]. At 30 MHz, the first IF is high enough for image-suppression by a fixed, low-selectivity bandpass filter after the antenna spanning the entire broadcast range from 88 to 108 MHz; no on-chip filter is used. Then, after amplification at the 30 MHz IF which comes readily in a state-of-the-art bipolar technology, a second *image-rejection mixer* (Fig.2) converts to a low IF of 150 kHz, and thereafter on-chip filtering is implemented by a 9th order active RC lowpass section. The RF amplifier transistors are integrated on-chip, although they require off-chip inductors for the load, and the local oscillator needs an off-chip LC tuned circuit. This receiver drains about 15 mA in either FM or AM mode.

ICs in Wireless Paging Receivers

Paging receivers have been in continuous development since the early 1960's, and have evolved into today's wide-area pagers which use digital signalling. The modern pager signals anywhere from 500 to 1200 b/s by encoding data with a simple positive or negative offset of the carrier frequency — the binary frequency-shift keyed (FSK) modulation. Paging receivers up to the early 1980's did not

The UCLA Low-Power Wireless Transceiver Project is supported by the US Advanced Research Projects Agency, and by a consortium of semiconductor companies under the State of California MICRO Program.

exploit the powerful simplifications this signaling scheme implied. Vance at Standard Telecommunication Laboratories realized how to simplify an FM receiver on to one chip with a quadrature downconversion mixer combined with *zero-IF*. Although this might not be suitable for a broadcast FM receiver, it was exactly the right solution for the binary-FSK digital paging receiver [6]. The remarkably simple receiver (Fig. 3) consists only of a quadrature demodulator, lowpass filters in each arm, limiters, and a D-type flip-flop detector, and when integrated on one bipolar chip, it drains 2.5 mA from 1.8 V when active; in standby the drain falls to a mere 50 μ A. More sophisticated detectors may be used to gain better noise rejection. Zero-IF means that the image is entirely eliminated. DC offsets in the receiver or flicker noise now fall in-band, however, but as the data is encoded in frequencies ± 4.5 kHz away from the carrier, the receiver may be AC coupled. The 10 kHz lowpass filters serve to eliminate out-of-band noise and blocking signals which would degrade the signal-to-noise ratio at the detector.

Single-chip bipolar zero-IF paging receivers are now quite common. A prominent feature they all share is that much of the die area is taken up by the capacitors for the on-chip lowpass filters and AC coupling [7, 8]. When active, these receivers consume only 1 to 2 mA from a single-battery, which is the typical specification for pagers. This example shows how the zero-IF, direct conversion architecture proved to be a good match to pager signalling.

ICs in Cellular Telephone Transceivers

Mobile and handheld cellular telephones are the first widespread two-way radios for consumer use, for which cordless telephones were a prelude. To be acceptable to the consumer, radio telephones must meet stringent demands for low weight and volume, long battery life, and low-cost. Further, to support a large numbers of users in a crowded radio spectrum, radio telephones require more signal processing than do other common transceivers. They must therefore use high levels of integration in the electronics.

The first generation of ICs for use in cellular telephones contained the frequently occurring building blocks used in conventional receivers, such as the mixer and local oscillator, or the IF amplifier chain and signal-strength indicator. Analog cellular telephones typically use the double-conversion architecture (Fig. 6), assembled with these building blocks, often using GaAs ICs at the receiver and transmitter modules, silicon building blocks in the IF, surrounded by an impressive collection of discrete resonator filters and antenna duplexers [9].

Circuits to implement the complex modulation formats in the new generation of digital mobile telephones, with their greater requirements to withstand nearby blocking signals, require yet greater integration of the RF and IF electronics. In a 900 MHz transmitter silicon bipolar IC from Siemens [10], a precision quadrature-upconversion mixer implements the phase-shift keyed modulation specified in the European GSM system to produce a single-sideband, suppressed-carrier output. The IC, which includes an output stage to drive a separate power amplifier, drains 40 mA. The companion receiver IC includes a first mixer, with buffers to drive an IF off-chip bandpass SAW filter, and a quadrature downconversion mixer to detect the single-sideband input at

baseband. Including an AGC with 70 dB range operating at the 40 to 90 MHz IF and a signal-strength indicator, the receiver drains 24 mA. Although the on-chip gain may become as large as 80 dB, it is distributed in different frequency bands and as a result there is little on-chip crosstalk.

Yet greater miniaturization is attained at Alcatel by integrating the transmitter and receiver sections together on one silicon bipolar chip. The zero-IF architecture makes this possible [11]. An off-chip low-noise amplifier drives directly into quadrature (I-Q) mixers, whose dynamic range is wide enough to withstand large blocking signals 3 MHz away from the carrier without producing significant intermodulation. Large (650 pF) off-chip capacitors constitute an anti-alias filter. The downconverted signals are sent to a baseband CMOS IC, containing a high-order switched capacitor lowpass filter to remove the blocking signals, and a demodulator. An RC and CR network with off-chip trimming shifts the local oscillator phase by $\pm 45^\circ$ to produce the quadrature drive to the mixers. Separate upconversion mixers in the transmitter drive a power amplifier module. The chip drains 25 mA from 5V in the receive mode, and 45 mA in the transmit mode, rather comparable to the Siemens chip set. It also suppresses the image and carrier by about 40 dB.

ICs for Spread-Spectrum Wireless Transceivers

As cellular telephones saturate the available radio frequency allocations, spread-spectrum techniques are being deployed in cordless telephones and wireless modems. These usually operate in the two lower bands allocated by the FCC for the industrial, scientific, and medical (ISM) communities for unlicensed spread-spectrum communications: 902 to 928 MHz, and 2.4 to 2.83 GHz. A ubiquitous wireless environment is envisioned, in which mobile users, wherever they are, may access data and communications services through an intricate network of base stations. The greatest hardware challenge is in developing the low-power, miniature handset.

A notable recent example of a miniature spread-spectrum transceiver is the 700 kb/s frequency-hopped device from Plessey, which operates in the 2.4 GHz band, and is assembled on 2" $\times$ 3" PCMCIA card for insertion into notebook computers [12]. It communicates by binary frequency-shift keying of the carrier, and to spread the spectrum, the carrier frequency, in turn, is slowly hopped across the entire band by a variable-modulus PLL synthesizer. All the active devices in the transceiver are on *three* ICs, consisting of a GaAs RF front-end, a silicon bipolar IF receiver, and a CMOS IC for the hopping frequency-synthesis. Nevertheless, the transceiver requires 50 passive components, including six rather bulky passive components such as filters, and it dissipates more than 1 W while transmitting 100 mW.

The single-chip GaAs IC front-end in this transceiver [13] is one of the most highly integrated, as it includes the power amplifier and drivers for 2-GHz passive filters in the transmit and receive paths. Otherwise, it is a conventional double-superheterodyne architecture. In its first version, the IC has more than 20 on-chip spiral inductors, probably the largest number found on any MMIC! In receive mode, the IC drains 30 mA from a 5 V supply, and it selects one of two antennas with an on-chip RF switch for *spatial diversity*.

ICs to Enable Future Transceivers

What might the portable wireless communicator of the future look like? We may draw some conclusions from the foregoing summary of RF-IC developments. The crowded spectrum means that wireless communicators will predominantly use spread-spectrum techniques, and that the need for low power dissipation will force yet higher levels of integration. Much of the filtering will be done on-chip at low frequencies, with perhaps only one RF passive filter off-chip. The author with his colleagues and their graduate students at UCLA is investigating the architecture and circuit design of a frequency-hopped, binary frequency-shift keyed, zero IF, all-CMOS two-chip transceiver capable of delivering up to 160 kb/s (the base ISDN rate) in the 900 MHz ISM band (Fig.5) [14]. This approach is to a large degree inspired by the modern paging receiver, which is perhaps the lowest-energy wireless device in wide use. The transceiver ICs freely mix analog and digital circuits, making CMOS the IC technology of choice for the entire transceiver, including the RF front-end. These blocks will be implemented in an unmodified standard production 1- μ m CMOS process.

Low-power operation requires that the entire system should operate on a 3V supply, which cannot be any lower because of the analog sections, and the unmodified FET threshold voltages. The power otherwise wasted in driving pad and trace parasitic capacitances is avoided with the use of on-chip inductors, whose self-resonance after the process of selective removal of the silicon substrate (Fig.6) [15] is as high as it is on semi-insulating GaAs substrates. Thus, a 1- μ m CMOS 900 MHz RF amplifier (Fig.6) has 30 dB gain and drains only 3 mA. The input FETs are biased at low $V_{GS}-V_t$ to attain a large g_m/I_D . The mixer in a direct-conversion receiver must be very linear to suppress intermodulation by interferers, and must not let the local oscillator signal leak out of the antenna. Both these problems are circumvented by an unusual, uniquely CMOS solution: a sub-sampling downconversion mixer (Fig.7) [16]. The circuit draws 4 mA to acquire samples of a 900 MHz modulated waveform at a 50 MHz rate which it directly translates to baseband. The linearity, as measured by a third-order intercept of +22 dBm, exceeds that of most continuous-time 900 MHz monolithic mixers.

Key to a frequency-hopped transceiver is a low-power, agile frequency synthesizer with high spectral purity. The requirements of purity and wideband agility are at odds in a VCO-based PLL synthesizer. In this work, a direct-digital frequency synthesizer (DDFS) produces digital words representing accurate samples of a sinewave, whose frequency is set anywhere from DC to half the clock rate by an 11b input control word. A low-power 50 MHz 10b D/A Converter follows to produce a baseband spread-spectrum. A CMOS implementation of the DDFS-DAC synthesizes sinewaves up to 13 MHz with spurious levels lower than -57 dBc while dissipating only 40 mW from 3 V (Fig.8) [17]. A fixed frequency 915 MHz local oscillator, consisting of a four-stage MOS ring oscillator (Fig.9) locked in a PLL to a lower frequency crystal reference, then upconverts this spectrum to the 902-928 MHz band. The PLL bandwidth is principally optimized to suppress oscillator noise. Quadrature outputs at 915 MHz for the image-reject mixers are tapped off at diametrically opposite points to within a phase accuracy of a couple of degrees. The power amplifier consists of a binary-weighted array of FETs biased near

threshold, followed by a matching network. FETs in the array are digitally selected to deliver power levels as high as 20 mW to the antenna with a 45% conversion efficiency [18].

Such a "VLSI radio" would represent a major step forward in the gradual evolution of the low-power integrated radio as described in this paper.

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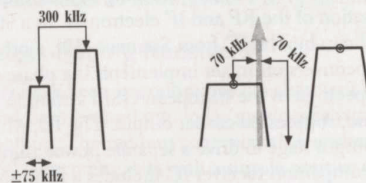


Fig.1. Channel spacing in the broadcast FM band, and the image frequency when the IF is reduced to 70 kHz.

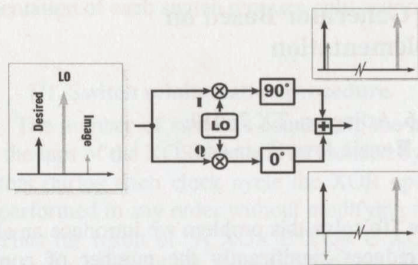


Fig.2. The image-cancelling mixer. This electronic alternative to a highly selective bandpass filter has only become practical on ICs, as the extent of image suppression depends on the matching of the two arms.

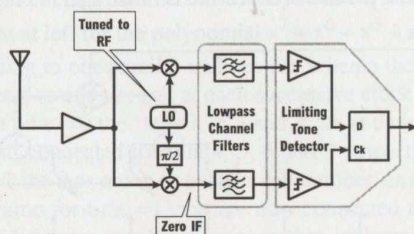


Fig.3. A simple zero IF receiver for binary-FSK signals. Including the lowpass channel filters, this may be readily integrated on a single IC.

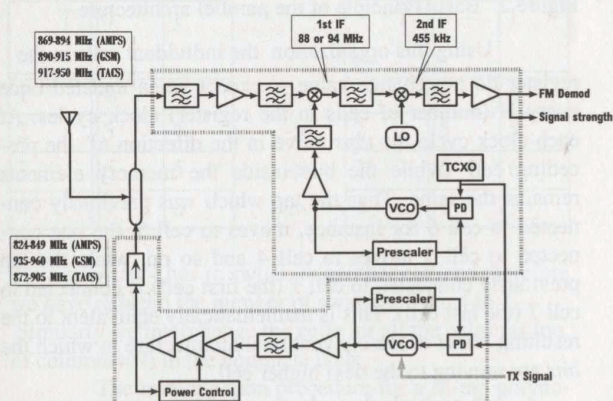


Fig.4. Architecture of a cellular telephone receiver and transmitter. Double conversion affords high selectivity, but at the expense of a large number of discrete filters.

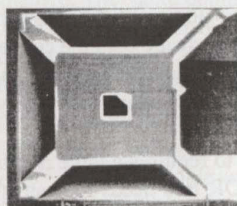


Fig.6. A 100 nH spiral inductor suspended over the silicon substrate. Self-resonance frequency is 3 GHz. A balanced CMOS RF amplifier affords 30 dB gain, 4 dB noise figure at 915 MHz.

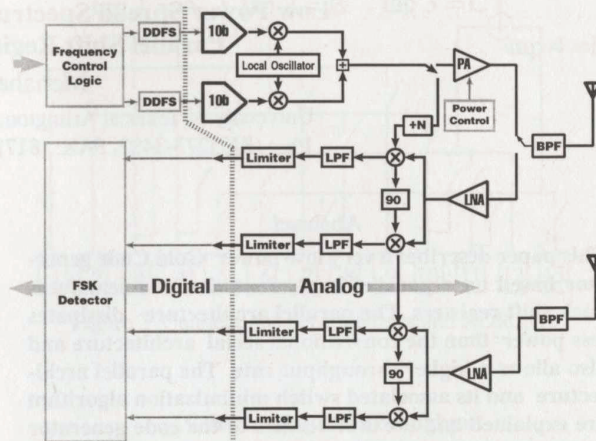
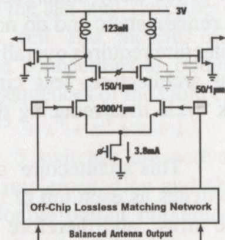


Fig.5. Architecture of the UCLA Frequency-Hopped FSK Transceiver. Two entire receive channels connected to the antennas help to combat multipath fading with spatial diversity.

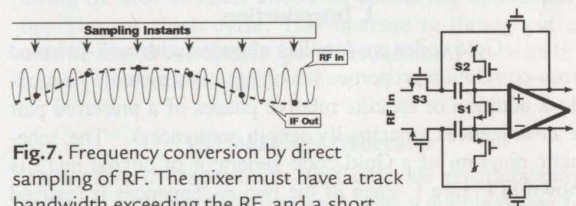


Fig.7. Frequency conversion by direct sampling of RF. The mixer must have a track bandwidth exceeding the RF, and a short sampling aperture.

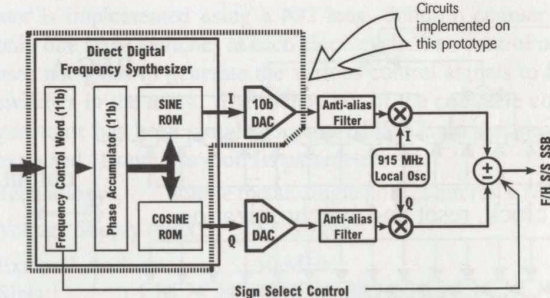


Fig.8. An agile frequency source using direct-digital frequency synthesis. Image reject mixer produces single-sideband, suppressed carrier output. Sign of summation at mixer outputs selects upper or lower sideband, so DDFS need only span 0 to 13 MHz to cover 902-928 MHz.

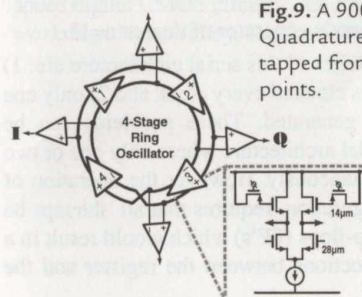


Fig.9. A 900 MHz CMOS VCO. Quadrature phases at any frequency tapped from diametrically opposite points.

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PRINTED IN THE UNITED STATES OF AMERICA

Volume I

IEEE Cat. No. 94TH0669-2
ISBN 0-7803-1953-2 Softbound
ISBN 0-7803-1954-0 Microfiche
Library of Congress Number 9476715

Editor: John H. Wuorinen

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