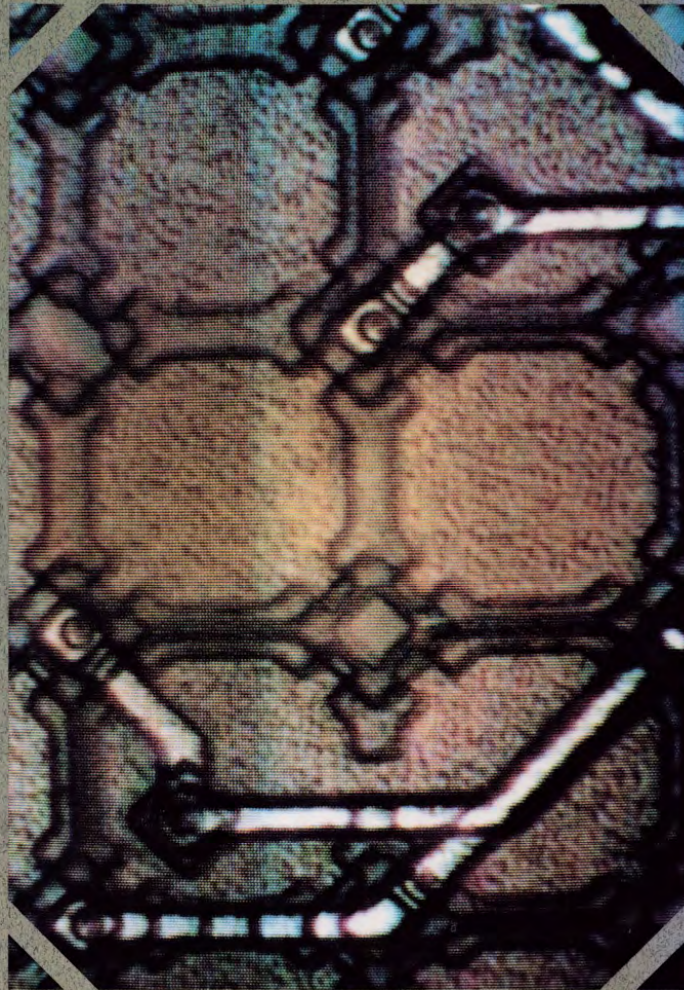


Second Edition

DESIGN OF ANALOG-DIGITAL VLSI CIRCUITS FOR TELECOMMUNICATIONS AND SIGNAL PROCESSING



JOSÉ E. FRANCA / YANNIS TSIVIDIS, Editors

FRANCA / TSIVIDIS

**DESIGN OF ANALOG-DIGITAL VLSI CIRCUITS
FOR TELECOMMUNICATIONS AND SIGNAL PROCESSING**

Second Edition

Engin.
TK7874
.D475
1994



PRENTICE
HALL

Second Edition

DESIGN OF ANALOG-DIGITAL VLSI CIRCUITS FOR TELECOMMUNICATIONS AND SIGNAL PROCESSING

JOSÉ E. FRANCA / YANNIS TSIVIDIS, Editors

VLSI is revolutionizing telecommunications and signal processing. To help readers keep pace, this volume examines the techniques that make this possible. **José E. Franca** and **Yannis Tsividis** enlist the aid of other top scientists, researchers, and educators to offer readers state-of-the-art theories, applications, and advances. The book covers circuits and systems.

Coverage includes:

- Circuit-Level Models for VLSI Components
- CMOS Operational Amplifiers
- Micropower Techniques
- Dynamic Analog Techniques
- Optical Receivers
- Continuous-Time Filters
- Switched-Capacitor Filter Synthesis
- Multirate Switched-Capacitor Filters
- Analog-Digital Conversion Techniques for Telecommunications Applications
- Delta-Sigma Data Converters
- Layout of Analog and Mixed Analog-Digital Circuits
- System Architectures and VLSI Circuits for Telecommunications
- Integrated Circuits for the ISDN
- VLSI Architectures and Circuits for Visual Communications
- Digital Television
- VLSI Architectures and Circuits for Digital Coding of High Definition Television
- IC Solutions for Mobile Telephones

PRENTICE HALL
Englewood Cliffs, NJ 07632



A000021938627

ISBN 0-13-203639-8



9 780132 036399



90000



ENGINEERING

8161

DESIGN OF ANALOG-DIGITAL VLSI CIRCUITS FOR TELECOMMUNICATIONS AND SIGNAL PROCESSING

Second Edition

José E. Franca and Yannis Tsividis, editors



Prentice Hall, Englewood Cliffs, New Jersey 07632

Library of Congress Cataloging-in-Publication Data

Design of analog-digital VLSI circuits for telecommunications and signal processing / José Franca and Yannis Tsividis, editors. -- 2nd ed.

p. cm.

Rev. ed. of: Design of MOS VLSI circuits for telecommunications. c1985.

Includes bibliographical references and index.

ISBN 0-13-203639-8

1. Integrated circuits--Very large scale integration.

2. Semiconductors. 3. Telecommunication--Equipment and supplies.

I. Franca, José. II. Tsividis, Yannis. III. Title: Design of MOS

VLSI circuits for telecommunications.

TK7874.D475 1994

621.39'5--dc20

93-1982

CIP

Publisher: Alan Apt

Production Editor: Mona Pompili

Copy Editor: Shirley Michaels

Prepress Buyer: Linda Behrens

Manufacturing Buyer: Dave Dickey

Editorial Assistant: Shirley McGuire



© 1994 by Prentice-Hall, Inc.

A Simon & Schuster Company

Englewood Cliffs, New Jersey 07632

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-203639-8

PRENTICE-HALL INTERNATIONAL (UK) LIMITED, London

PRENTICE-HALL OF AUSTRALIA PTY. LIMITED, Sydney

PRENTICE-HALL CANADA, INC., Toronto

PRENTICE-HALL HISPANOAMERICANA, S.A., Mexico

PRENTICE-HALL OF INDIA PRIVATE LIMITED, New Delhi

PRENTICE-HALL OF JAPAN, INC., Tokyo

SIMON & SCHUSTER ASIA PTE. LTD, Singapore

EDITORIA PRENTICE-HALL DO BRASIL, LTDA., Rio de Janeiro

Contents

1. Circuit-Level Models for VLSI Components	1
F.M. Klaassen	
Introduction 1	
1. MOSFET Modelling, 1	
1.1. Threshold voltage, 1	
1.2. Drain current at strong inversion, 4	
1.3. Subthreshold current, 6	
1.4. Saturation mode, 7	
1.5. Charges and capacitances, 9	
1.6. Parasitics and model extensions, 10	
2. Bipolar Modelling, 11	
2.1. Carrier transport, 11	
2.2. Collector current, 12	
2.2.1. Charge control approach, 12	
2.2.2. Carrier control approach, 13	
2.3. Base current, 14	
2.4. Charges and capacitances, 14	
2.5. Quasi-saturation, 16	
2.6. Parasitics and model extensions, 17	
3. Parameters, 20	
3.1. Parameter acquisition, 20	
3.2. Geometry and process dependence, 21	
3.3. Statistics of parameters, 22	
References, 23	

2. CMOS Operational Amplifiers	27
<i>Daniel Senderowicz</i>	
1. General Considerations for VLSI of Amp Design,	27
2. The Differential Circuit Approach,	28
3. The Number of Internal Stages,	31
4. Cascode Op Amps,	31
4.1. The folded-cascode OTA,	34
4.2. The telescopic-cascode OTA,	35
4.3. Comparisons between the folded and telescopic cascode OTAs,	36
4.3.1. Simulations,	37
4.4. Single-ended versions of the cascode OTAs,	38
5. Multiple Stage Op Amps,	39
5.1. The differential class-A two stage op amp,	40
5.2. The resistor driving class-AB op amp, version I,	42
5.3. The resistor driving class-AB op amp, version II,	44
6. Bias Circuits,	47
7. Layout Techniques,	49
References,	51
3. Micropower Techniques	53
<i>Eric A. Vittoz</i>	
1. Introduction,	53
2. Technology,	54
3. Devices,	55
3.1. MOS transistors,	55
3.2. CMOS compatible bipolar transistors,	67
3.3. Passive devices,	69

3.4. Parasitic effects,	70
4. Basic Circuit Techniques,	70
4.1. Current mirrors,	70
4.2. Differential pair,	71
4.3. Voltage gain cells,	72
4.4. Low-voltage cascoding,	75
4.5. Current references,	77
4.6. Voltage references,	78
4.7. Analog switches,	79
4.8. Dynamic CMOS gates,	80
5. Examples of Building Blocks,	81
5.1. Operational transconductance amplifiers (OTAs),	81
5.2. Quartz crystal oscillators,	87
5.3. Sequential logic building blocks,	91
6. Conclusions,	92
7. References,	93
4. Dynamic Analog Techniques	97
<i>Eric A. Vittoz</i>	
1. Introduction,	97
2. Sample-and-Hold,	97
2.1. Principle,	97
2.2. Transfer function,	98
2.3. Noise sampling,	99
2.4. Charge injection by the switch,	101
2.5. Sample-and-hold used as a time differentiator (autozero circuit),	105
3. Offset Compensation of Operational Amplifiers,	108
3.1. First order compensation,	108
3.2. Compensation by a low-sensitivity auxiliary input,	108
4. Dynamic Biasing of CMOS Inverter-Amplifiers,	112

5. Dynamic Comparators, 114	
5.1. Basic circuit, 114	
5.2. Multistage comparators, 117	
6. Dynamic Current Mirrors, 118	
6.1. Principle and limitations, 118	
6.2. Examples of practical implementations, 120	
7. Conclusion, 122	
8. References, 122	
5. Optical Receivers	125
<i>David J.T. Heatley</i>	
1. Introduction, 125	
2. Receiver Design, 126	
3. Receiver bandwidth, 127	
3.1. Low impedance receiver, 127	
3.2. High impedance receiver, 128	
3.3. Transimpedance receiver, 130	
4. Receiver Noise, 132	
4.1. Photodiode noise, 132	
4.2. Resistor noise, 133	
4.3. Amplifier noise, 134	
4.4. 2nd Stage noise, 136	
4.5. Total noise power spectral density, 136	
4.5.1. Low impedance receiver, 137	
4.5.2. High impedance receiver, 140	
4.5.3. Transimpedance receiver, 143	
4.5.4. Comparison of all receiver configurations, 144	
5. Signal-to-Noise Ratio, 147	
5.1. SNR from the low impedance receiver, 148	
5.2. SNR from the high impedance receiver, 151	

5.3.	SNR from the transimpedance receiver,	151
5.4.	Comparison of SNRs,	152
6.	Receiver Sensitivity,	155
6.1.	Analogue transmission system,	155
6.2.	Digital transmission system,	156
6.3.	Transmission distances,	161
7.	Dynamic Range,	164
8.	Developments in Receiver Design,	166
8.1.	Coherent detection receivers,	167
8.2.	Optically pre-amplified direct detection receivers,	170
8.3.	The transmission engineer's dream,	171
	References,	171
	Appendix A,	175

6. Continuous-Time Filters

177*Yannis Tsividis and Venugopal Gopinathan*

1.	Introduction,	177
2.	MOSFET-C Filters,	179
2.1.	The MOSFET as a voltage-controlled resistor,	179
2.2.	Cancellation of nonlinearities,	181
2.3.	MOSFET-capacitor filters based on balanced structures,	183
2.3.1.	Principle,	183
2.3.2.	Filter synthesis,	185
2.3.3.	Accuracy,	188
2.3.4.	Distortion and dynamic range,	189
2.3.5.	Parasitic capacitance,	189
2.4.	Worst-case design,	191
3.	Transconductor-C Filters,	192
3.1.	Introduction,	192
3.2.	Transconductor design,	193

3.2.1. Designs that are based on MOSFET characteristics in the saturation region, 194	
3.2.2. Designs that are based on MOSFET characteristics in the non-saturation region, 196	
3.3. Gm-C filter synthesis, 199	
4. MOSFET-C vs Transconductor-C Filters, 201	
5. On-Chip Tuning Schemes, 202	
6. A Warning Concerning Computer Simulations, 206	
7. Conclusion, 206	
References, 207	
 7. Switched-Capacitor Filter Synthesis	213
<i>Adel S. Sedra and Martin Snelgrove</i>	
1. Introduction, 213	
2. First-Order Building Blocks, 215	
2.1. Basic operation, 215	
2.2. Exact transfer functions and the LDI variable, 217	
2.3. Damped integrators, 221	
2.4. General form of the first-order building block, 223	
2.5. Switch design, 224	
2.6. Differential circuits, 225	
3. Biquadratic Sections and Cascade Design, 225	
3.1. Circuit generation via equivalent resistors, 226	
3.2. Exact transfer function: LDI design, 228	
3.3. Capacitive damping, 230	
3.4. Biquads for exact design: the bilinear variable, 231	
3.5. Biquad circuits for exact design, 232	
3.6. Differential biquads, 234	
3.7. Cascade design, 236	
4. Ladder Filters, 237	

4.1. Circuit generation,	238
4.2. Design,	241
4.3. A general exact design method,	242
5. Concluding Remarks,	246
6. References,	247
8. Multirate Switched-Capacitor Filters	251
<i>José E. Franca and R.P. Martins</i>	
1. Introduction,	251
2. FIR SC Decimators and Interpolators,	252
2.1. Direct-form polyphase SC structure for decimation,	252
2.2. Direct-form polyphase SC structure for interpolation,	258
2.3. Multi-amplifier FIR SC decimators,	262
3. IIR SC Decimator Building Blocks,	266
3.1. First-order SC decimator building block,	268
3.2. Second-order SC decimator building block,	271
3.3. Nth.-order SC decimator building block,	277
4. IIR SC Interpolator Building Blocks,	281
5. Conclusions,	285
References,	286
9. Analog-Digital Conversion Techniques for Telecommunications Applications	289
<i>Paul Gray and Robert R. Nepp</i>	
1. Introduction,	289
2. The Role of A/D Converters in Telecommunications Systems,	290
3. Classification of A/D Conversion Techniques,	292

4. Circuit Building Blocks for A/D Converters, 296	
4.1. High-speed DACs in MOS technology, 296	
4.1.1. Current-switched MOS DACs, 296	
4.1.2. Resistor-string DACs, 297	
4.1.3. Charge-redistribution DACs, 297	
4.1.4. Component mismatch effects in monolithic DACs, 302	
4.2. Monolithic sample/hold amplifiers, 307	
4.3. Monolithic voltage comparators, 309	
Summary, 313	
References, 314	
10. Delta-Sigma Data Converters	317
<i>Gabor C. Temes</i>	
1. Introduction, 317	
2. Noise-Shaping A/D Converters, 320	
2.1. Quantization noise, 320	
2.2. The delta-sigma modulator, 322	
2.3. Higher-order single-stage converters, 325	
2.4. Multi-stage (cascade) converters, 327	
2.5. Modulators with multibit quantizers, 329	
3. Noise-Shaping D/A Converters, 335	
4. Conclusions, 337	
Acknowledgement, 338	
5. References, 338	
11. Layout of Analog and Mixed Analog-Digital Circuits	341
<i>Franco Maloberti</i>	
1. Introduction, 341	
2. Differences Between Layout and Circuit, 342	

3. Absolute and Relative Accuracies, 343	
4. Layout of MOS Transistors, 344	
5. Layout of Resistor, 348	
6. Layout of Capacitors, 351	
7. Stacked Layout for Analog Cells, 354	
8. Digital Noise Coupling, 356	
9. Floor Planning of Mixed Analog-Digital Blocks, 363	
10. Concluding Remarks, 366	
11. References, 366	
12. System Architectures and VLSI Circuits for Telecommunications	369
<i>Guenter Weinberger</i>	
1. Introduction, 369	
2. System Structure, 370	
3. Communication ICs for Digital Exchange Systems, 371	
3.1. PCM switching network components, 371	
3.2. Serial communication controllers, 372	
3.3. Line card functions and architectures, 374	
3.3.1. Line card functions, 375	
3.3.2. Line card architectures, 375	
3.4. Line card controller, 376	
3.5. Analog subscriber line card devices, 378	
3.5.1. Line card functions, 378	
3.5.2. Codec and filter devices, 380	
3.5.3. Subscriber line interface circuit (SLIC), 384	
3.6. Digital subscriber line card devices, 386	
3.6.1. Line card functions, 386	
3.6.2. ISDN transceiver devices, 387	

4. Analog Telephone Sets, 387
5. ISDN Subscriber Equipment, 390
 - 5.1. ISDN terminals and terminal adaptors, 391
 - 5.1.1. ISDN layer-2 terminal controller, 391
 - 5.1.2. ISDN codec filter, 392
 - 5.1.3. ISDN terminal adaptors, 392
 - 5.2. ISDN network terminations (NT1), 393
6. DSP in Telecommunications, 394
 - 6.1. Introduction, 394
 - 6.2. DSP design methodology, 396
7. Conclusion, 397
8. References, 398

13. Integrated Circuits for the ISDN

401*Peter Adams*

1. Introduction, 401
2. ISDN Fundamentals, 401
 - 2.1. ISDN access functional blocks, 403
3. S/T-Bus Transceivers, 404
4. D-Channel Controllers, 405
5. Digital Subscriber Loop Transceivers, 406
 - 5.1. Key loop characteristics, 408
 - 5.2. 2-wire duplex operation, 410
 - 5.3. Choice of line code, 410
 - 5.4. Transceiver architecture, 411
 - 5.5. Transmitter implementation, 413
 - 5.6. Receiver implementation, 414
 - 5.7. Echo canceller implementation, 418
 - 5.8. DSP implementation issues, 421
 - 5.9. Transceiver examples, 423

6. Conclusion,	425
7. References,	425
14. VLSI Architectures and Circuits for Visual Communications	429
<i>P. Pirsch and T. Wehberg</i>	
1. Introduction,	429
2. Source Coding Algorithms,	430
2.1. Algorithms for redundancy reduction,	430
2.2. Quantization,	433
2.3. Variable word length coding,	434
2.4. Source coding for different applications,	435
3. VLSI Implementation Strategies,	437
4. Programmable Multiprocessor Systems,	441
4.1. Architecture of SIMD and MIMD multiprocessors,	442
4.2. SIMD system based on multiprocessor IC,	443
4.3. MIMD system based on multiprocessor IC,	445
5. Key Components for Functional Blocks,	450
5.1. Dedicated realizations of discrete cosine transform,	451
5.2. Dedicated realizations of block matching,	455
References,	459
15. Digital Television	463
<i>A. Rothermel</i>	
1. Introduction,	463
2. TV Tuner,	464
3. Audio Processing,	467
4. Video Signal Processing,	470
4.1. Coding principles,	470

4.2. Implementation issues, 473	
4.2.1. The luminance channel, 475	
4.2.2. The chrominance channel, 477	
5. Scan Control Processing, 481	
5.1. Tasks and problems, 481	
5.2. Deflection processor, 482	
5.3. Picture geometry correction, 483	
6. Quality Improvements, 484	
6.1. Improved luma/chroma separation, 484	
6.2. Flicker reduction, 487	
6.3. Format control, 490	
7. Conclusion, 492	
8. References, 493	
16. VLSI Architectures and Circuits for Digital Coding of High Definition Television	495
<i>P. Pirsch and K. Gröger</i>	
1. Introduction, 495	
2. Source Coding Algorithms for HDTV, 496	
2.1. HD-MAC coding, 496	
2.2. DPCM coding, 498	
2.3. DCT coding, 499	
2.4. Subband coding, 500	
3. VLSI Implementation Aspects, 502	
4. VLSI Architecture for 2D DPCM, 502	
4.1. Implementation problems of DPCM, 502	
4.2. Parallel DPCM processors, 503	
4.3. Modified DPCM structure, 505	
4.4. Parallel processing and delayed decision, 506	
4.5. Comparison of DPCM architectures, 507	
4.6. CMOS circuit technique for DPCM, 508	

Circuit-Level Models for VLSI Components

- 4.6.1. Adder realization, 508
- 4.6.2. Realization of XOR, 509
- 4.7. Table look-up realization, 509
- 4.8. Realization of line delay, 511
- 4.9. Example of a DPCM processing element for HDTV, 514

5. Subband Filterbanks, 515

- 5.1. Hardware requirements, 515
- 5.2. Nonrecursive wave digital filter (NRWDF), 516
- 5.3. Transversal FIR filter, 517
- 5.4. Polyphase structure, 517
- 5.5. Expansion in time by subsampling, 520
- 5.6. Architectures for quadrature mirror filterbanks (QMFs), 521
 - 5.6.1. Filter characteristics, 521
 - 5.6.2. Filter structures for QMFs, 521
- 5.7. Realization of arithmetic blocks, 522
 - 5.7.1. Realization of multipliers, 522
 - 5.7.2. Multioperand adders for FIR-filter, 524
- 5.8. Complexity of filterbank VLSI-implementation, 525

6. References, 525

17. IC Solutions for Mobile Telephones 529

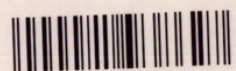
Juha Rapeli

- 1. Introduction, 529
- 2. Mobile Communication Systems, 529
- 3. Functional Blocks of a Cellular Telephone, 533
 - 3.1. Receiving Function (RX), 537
 - 3.2. Frequency synthesis, 539
 - 3.3. TX-function, 547
 - 3.4. Signalling function, 548
 - 3.5. Speech and audio processing, 548
 - 3.6. Control functions, 548
- 4. Digital Mobile Phones, 549

- 4.1. Speech coding, 549
- 4.2. Modulation, 550
- 4.3. Symbol decoder (demodulator) and channel codec, 552
5. Future developments in mobile communication, 556
 - 5.1. CDMA technology, 558
 - 5.2. 2-GHz developments, 561
 - 5.3. Integration of new features into mobile phones, 561
6. IC Technology, 565
 - 6.1. FDMA, TDMA and CDMA from integrations point of view, 565
 - 6.2. Integration technologies, 565
 - 6.3. ASICs versus Standard ICs, 566
7. Conclusions, 566
- References, 567

Index**569**

✓
2-24-94



A000021938627

ENGINEERING

- (1) Avoid the use of internal resistors. These can appear as op amp loads, forcing the need for complex buffer stages.
- (2) Constrain the function around an op amp to an inverting configuration, avoiding such functions as voltage followers. The noninverting configuration requires an amplifier with large input common-mode range.
- (3) Avoid configurations which use MOS switches around the feedback path of an op amp. This restriction is based on similar arguments as those applying to rule (2).
- (4) Design the systems in such a way as to accommodate for a wide spread in the DC voltage gain. This uncertainty is mostly due to inaccuracies in the modelling of the MOS transistors in the simulators.
- (5) In the case of analog-to-digital (ADC) or digital-to-analog converters (DAC), choose *sequential* techniques whenever possible. This approach, which is somehow opposed to the idea of parallelism, generally simplifies the amount of analog circuitry at the expense of some added digital complexity and reduced speed of operation.
- (6) Design the systems using differential circuitry whenever possible. The op amps will be simpler, and most importantly, this may be the only way to achieve the desired specifications of dynamic range. The cost for this is an increased amount of internal elements and busing.

2. The Differential Circuit Approach

Digital circuitry generates a large amount of switching noise which appears in the power lines, the common substrate, and as parasitic capacitive coupling between the internal interconnections. This scenario imposes as one of the main goals for the designer that all the necessary precautions be taken in order to make the analog circuit highly immune to this noise coupling. Differential circuitry is a technique which provides a way to achieve this immunity. Furthermore, differential circuitry doubles the effective signal swing which increases the dynamic range, a very important feature in high-density technology where the maximum operating supply is limited to 5 volts or less. The use of differential circuits for the analog paths generally implies a larger number of components and interconnections. However, as will be seen later, op amps with comparable functionality are considerably simpler. Another

advantage of differential circuits is that the signal is immune to noise in the internal reference node (e.g., $1/2(V_{DD} - V_{SS})$), a feature which is very important in single supply systems.

For certain applications such as those requiring the processing of an input current (or charge), the use of differential circuitry cannot be easily implemented. In these cases, single-ended circuitry is the only practical alternative. However, if there is a significant amount of signal post-processing, one can always implement a single-ended to differential conversion as close to the input as possible, aiming at keeping the amount of single-ended circuitry to a minimum. With this consideration in mind, the need for single-ended op amps also arises, which in general will have to be subject to similar minimization arguments as those applying to their differential counterparts.

In a differential amplifier there is an additional *degree of freedom* over a single-ended amplifier. While the differential output should be proportional to a differential input signal, the average voltage of these two outputs should also be controllable with another input signal. This is usually referred to as the common-mode input. Fig. 1 shows a representation of a differential op amp where the inner amplifier represents the common-mode path.

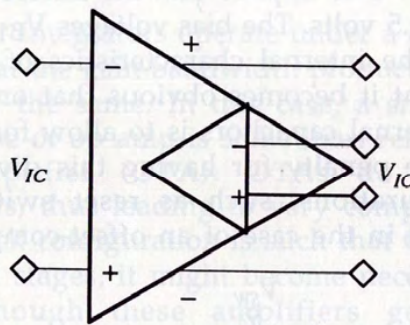


Fig. 1: Differential op amp.

In most applications, the common-mode input is fed with a signal derived from the average of the two outputs. However, it could also be possible to superimpose another signal to that average which may or may not be directly related to the differential signal. Fig. 2 shows a differential switched-capacitor integrator with the averaging of the two outputs implemented by means of an additional set of switched-capacitors. C_U is usually the unit capacitor, while C_X has to be large enough to keep the common-mode switching noise within acceptable levels.

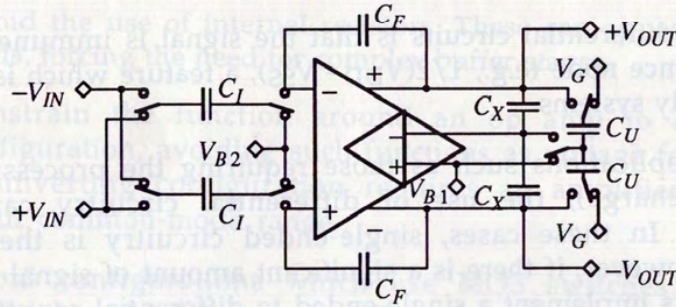


Fig. 2: Differential switched-capacitor integrator.

It should be noted that in Fig. 2 the bias point of the differential switched-capacitors can be chosen arbitrarily. In fact, V_{B2} and V_G do not have to be the same, and they can both be different from V_{B1} , the bias point for the common-mode switched-capacitors. This flexibility in choosing these bias points results in the possibility of superimposing DC voltages to the signal in order to avoid level-shifting operations inside the op amp. A numerical example can illustrate this idea: V_G is chosen to maximize the swing; therefore, for a single voltage supply of 5 volts, $V_G=2.5\text{V}$. This implies that the differential voltage V_{OUT} will have an average value of 2.5 volts. The bias voltages V_{B1} and V_{B2} can be chosen in such a way as to fit the internal characteristics of the amplifier or other requirements. At this point it becomes obvious that one of the main goals of level-shifting with the external capacitors is to allow for op amps with limited input common-range. The penalty for having this diversity of bias voltages precludes certain configurations, such as reset switches in parallel with capacitors, which is found in the case of an offset-compensated amplification-module (Fig. 3).

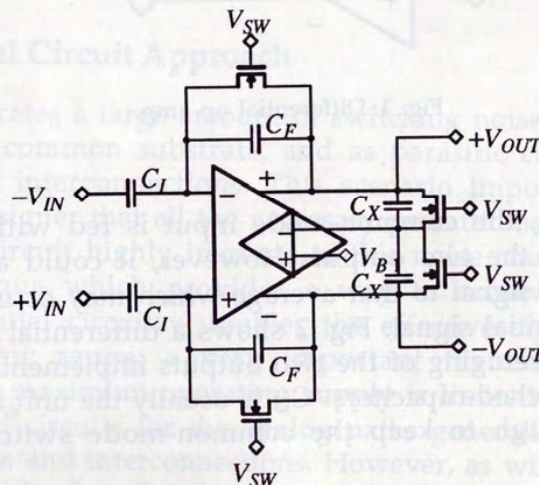


Fig. 3: Amplifier with MOS reset switch.

Fig. 4 describes a simplified schematic for an alternative solution that avoids the use of MOS switches while still performing the discharging of the feedback capacitor C_F . After examining the characteristics of different amplifiers, the reasons for avoiding certain configurations will become more obvious.

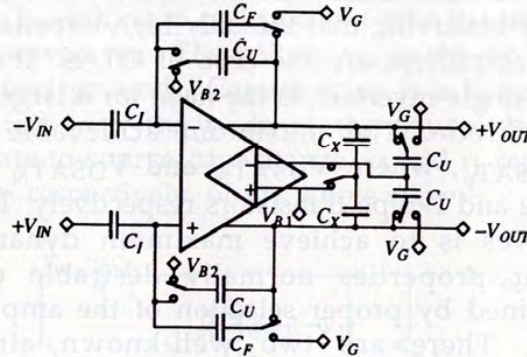


Fig. 4: Feedback reset without switch.

3. The Number of Internal Stages

Most switched-capacitor integrators operate under a condition in which $C_F \gg C_I$ (Fig. 2). This implies that the gain-bandwidth products of the integrator and the op amp are essentially the same. In this case, a single voltage-gain stage is recommended. This type of op amp is sometimes referred to as an operational transconductance amplifier (OTA). OTAs do not require additional compensation capacitors, thus leading to very compact circuits. On the other hand, when the feedback configuration is such that $C_D \ll C_I$ (Fig. 3), such as in high-gain amplification stages, it might become necessary to have a multiple-stage amplifier. Although these amplifiers generally require phase-compensation, this can be reduced to minimum capacitance due to the low amount of feedback.

Another instance in which multiple-stage op amps are required is when heavy resistive and/or capacitive loads need to be driven, as in the case of off-chip drivers. These amplifiers can become very complex because of the limitations of MOS transistors as current drivers. Examples of these will be given later.

4. Cascode Op Amps

Fig. 5 shows a typical implementation of a simple cascode amplifier. It is well known from single amplifier theory that cascode stages increase the voltage gain by means of boosting their effective output impedance. This boost is