

IPR2024-00936
U.S. Patent No. 9,118,528
Patent Owner's Response

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INC.,
Petitioner,

v.

PARKERVISION, INC.
Patent Owner

U.S. Patent No. 9,118,528

Issue Date: August 25, 2015

Title: METHOD AND SYSTEM FOR DOWN-CONVERTING AN
ELECTROMAGNETIC SIGNAL, AND TRANSFORMS FOR SAME, AND
APERTURE RELATIONSHIPS

Inter Partes Review No. IPR2024-00936

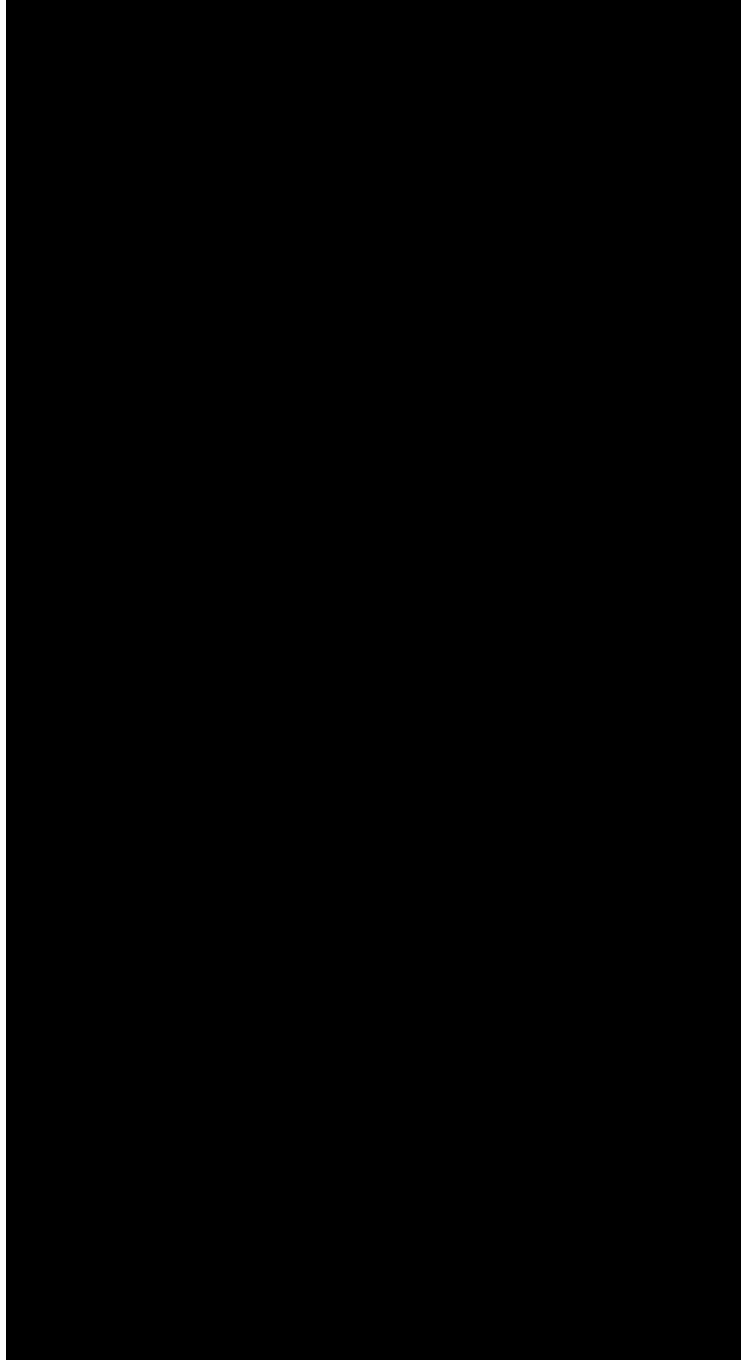
DECLARATION OF DAVID SORRELLS

I, David Sorrells, have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, would testify under oath as follows:

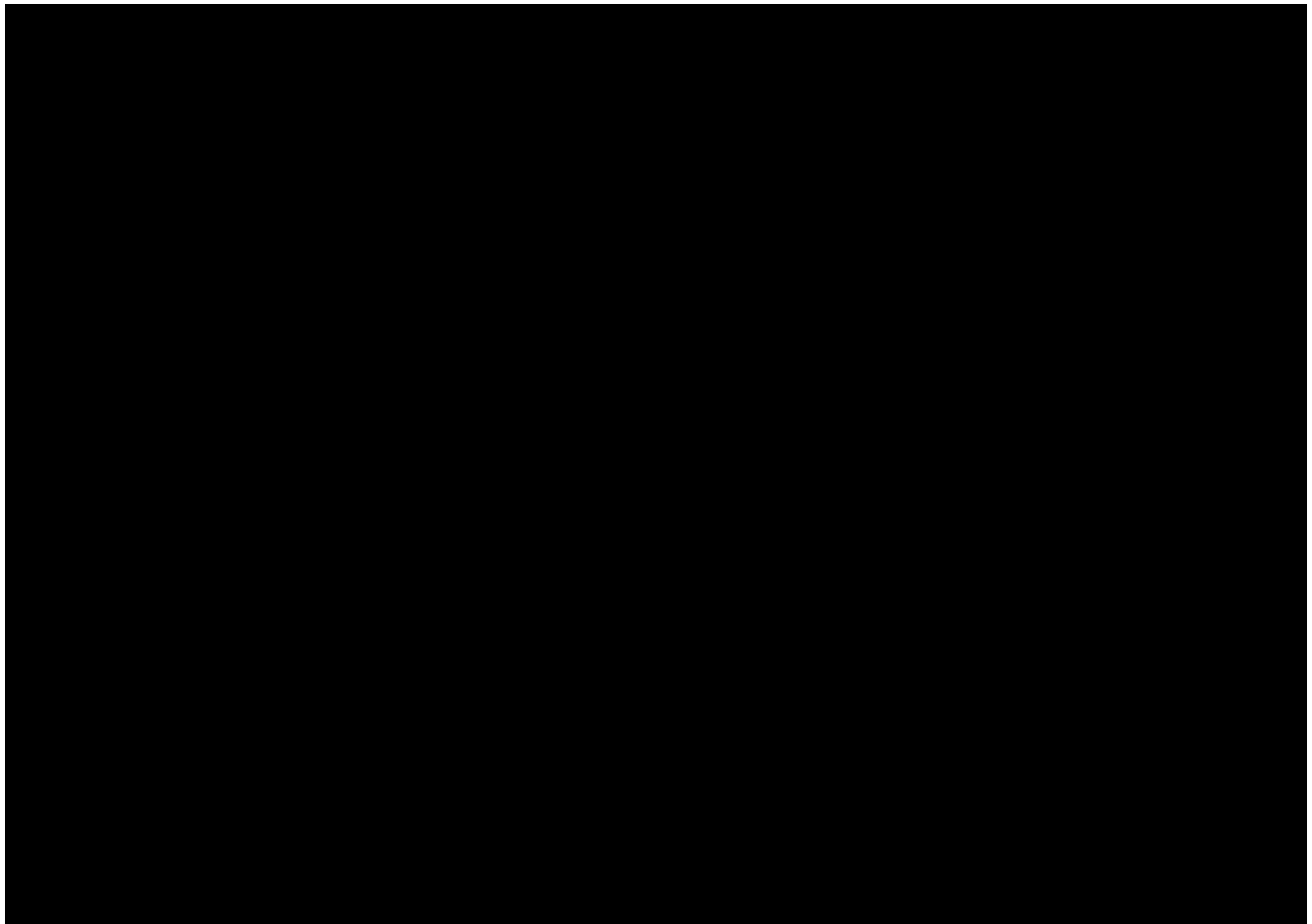
1. I am over eighteen years old.
2. I am currently the Senior Technical Strategist of ParkerVision, Inc. (“ParkerVision”). During my 34-year tenure at ParkerVision, I have held the positions of Director of Engineering and Chief Technology Officer (CTO). I was ParkerVision’s CTO from September 1996 to the beginning of 2020.
3. I am one of the named inventors of U.S. Patent No. 9,118,528.
4. In 1997 and 1998, I led the research, design, development, evaluation, and testing of ParkerVision’s down-conversion technology.
5. In the summer of 1996, ParkerVision began to design its first integrated circuit (IC) chip called “Eddie.” ParkerVision completed the design of the Eddie chip by early 1997. The Eddie chip [REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
6. By early 1997, ParkerVision completed the layout for the Eddie chip.
7. [REDACTED]

██████████ (Exhibit 2012).

8. The layout (GDSII file) of the Eddie chip can be seen below. In this declaration, I used a white background (below) for the layout to show features more clearly. The black and white versions are the same diagram.

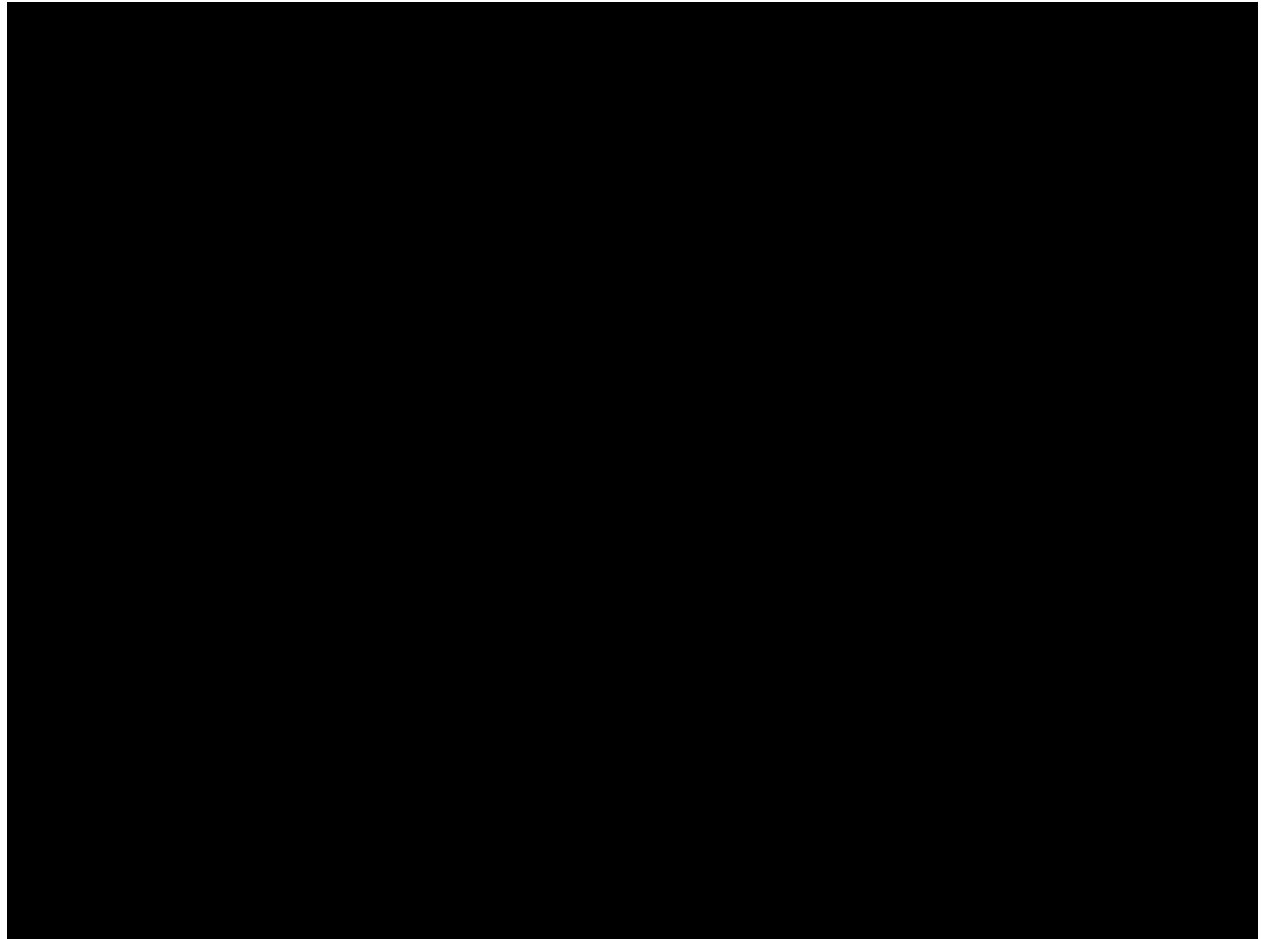


9. As can be seen (below left) in the properties of the [REDACTED] this file shows that it was last modified on March 6, 1997. As can be seen (below right) in the metadata from a Relativity database, it also shows that the file was last modified on March 6, 1997. This date is consistent with the time that the ParkerVision team and I were working on the layout of the Eddie chip.

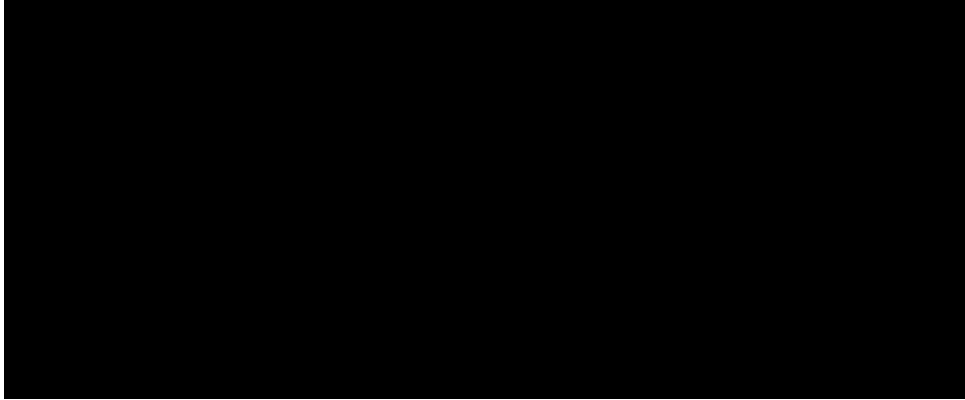


10. As shown above, file explorer also shows a create date of March 6, 1997.

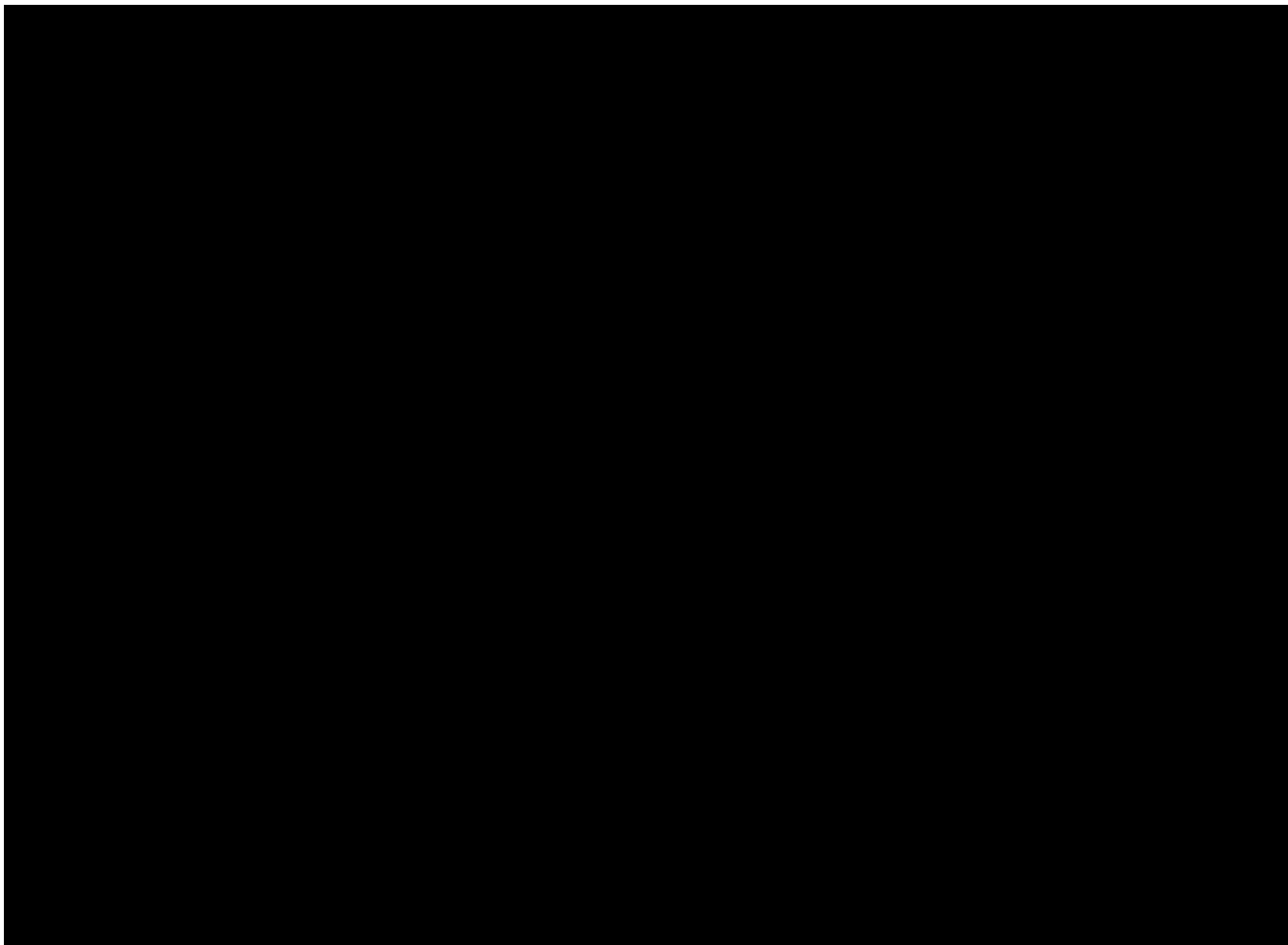
11. Below is a schematic of an early version of a circuit board (Exhibit 2014) that ParkerVision designed for mounting the Eddie chip.



12. As can be seen below in the bottom right corner of the schematic (expanded below), it has a date of August 21, 1997 on its face. It was our practice at the time to date our schematics with the actual date the schematic was created. This date is consistent with the time that the ParkerVision team and I were working on the schematic of an early circuit board for the Eddie chip.



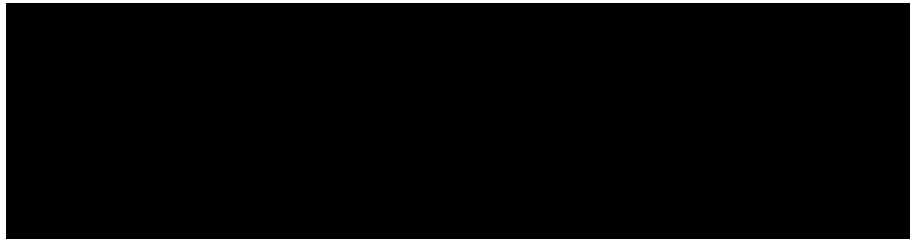
13. As shown below, by January 20, 1998, ParkerVision designed the final schematic for a circuit board (Exhibit 2011) for mounting the Eddie chip. The schematic for the circuit board can be found in a file [REDACTED] ParkerVision fabricated, built, and populated the circuit board shown in this file.



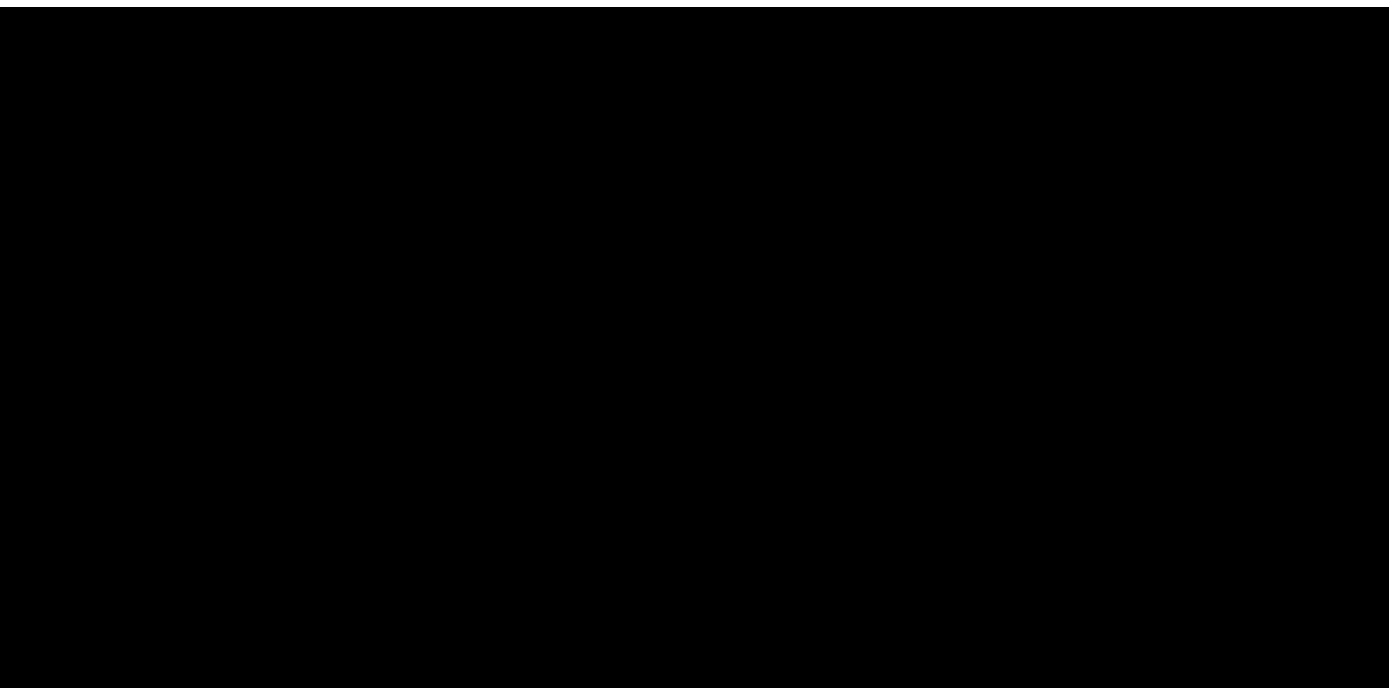
14. As can be seen below in the bottom right corner of the schematic (expanded below), it has a file name of [REDACTED] and date of January 20, 1998 on its face. It was our practice at the time to date our schematics with the actual date the schematic was created. This date is consistent with the time that the ParkerVision team and I were working on the schematic of the circuit board for the Eddie chip.



15. As can be seen below in the metadata from a Relativity database, the file [REDACTED] was last modified on February 26, 1998. This date is consistent with the time that the ParkerVision team and I were working on the schematic of the circuit board for the Eddie chip.



16. The layout of the circuit board (Exhibit 2013) can be seen below left and the schematic of the circuit board can be seen below right. Part 63 is shown both on the circuit board layout and schematic and represents the location of the Eddie chip on the circuit board. The layout of the circuit board was created in 1997.



17. In 1997, ParkerVision chose [REDACTED] as its foundry to build the Eddie chip. The [REDACTED] agreement is shown in Exhibit 2027.

18. By no later than the first quarter of 1998, [REDACTED] provided ParkerVision with a [REDACTED]

19. When ParkerVision received the [REDACTED] ParkerVision [REDACTED]
[REDACTED]

20. By the first quarter of 1998, ParkerVision tested and evaluated the combined Eddie chip and circuit board. By the first quarter of 1998, ParkerVision issued press releases discussing testing/evaluation of the Eddie chip including the

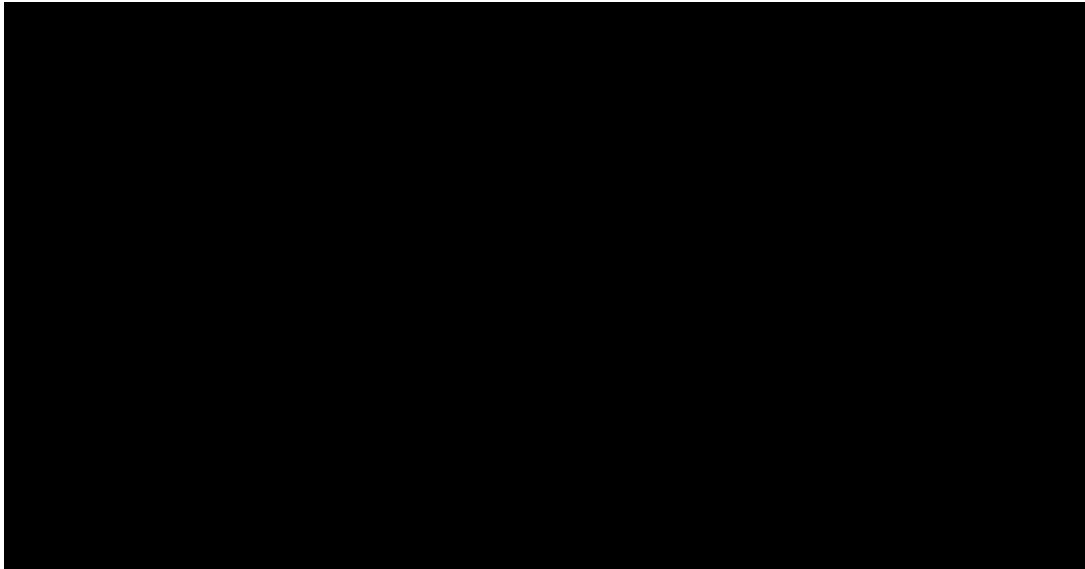


24. The test results confirmed the performance of the Eddie chip and circuit board. The [REDACTED] report confirmed ParkerVision's testing/evaluation and also showed that the combined Eddie chip and circuit board worked for its intended purpose of down-converting an RF signal.

25. As shown below, the combined Eddie chip and circuit board ("Device Under Test" (blue)) were tested and [REDACTED]

[REDACTED]

[REDACTED]



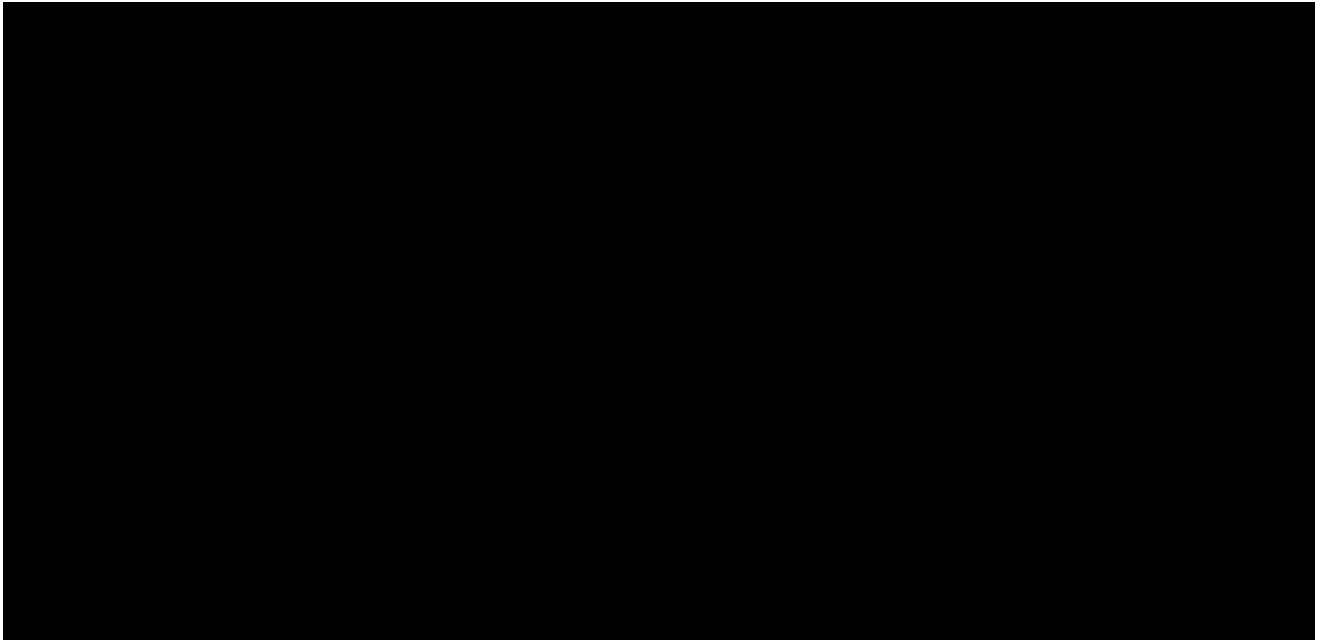
26. Below is an annotated version of [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

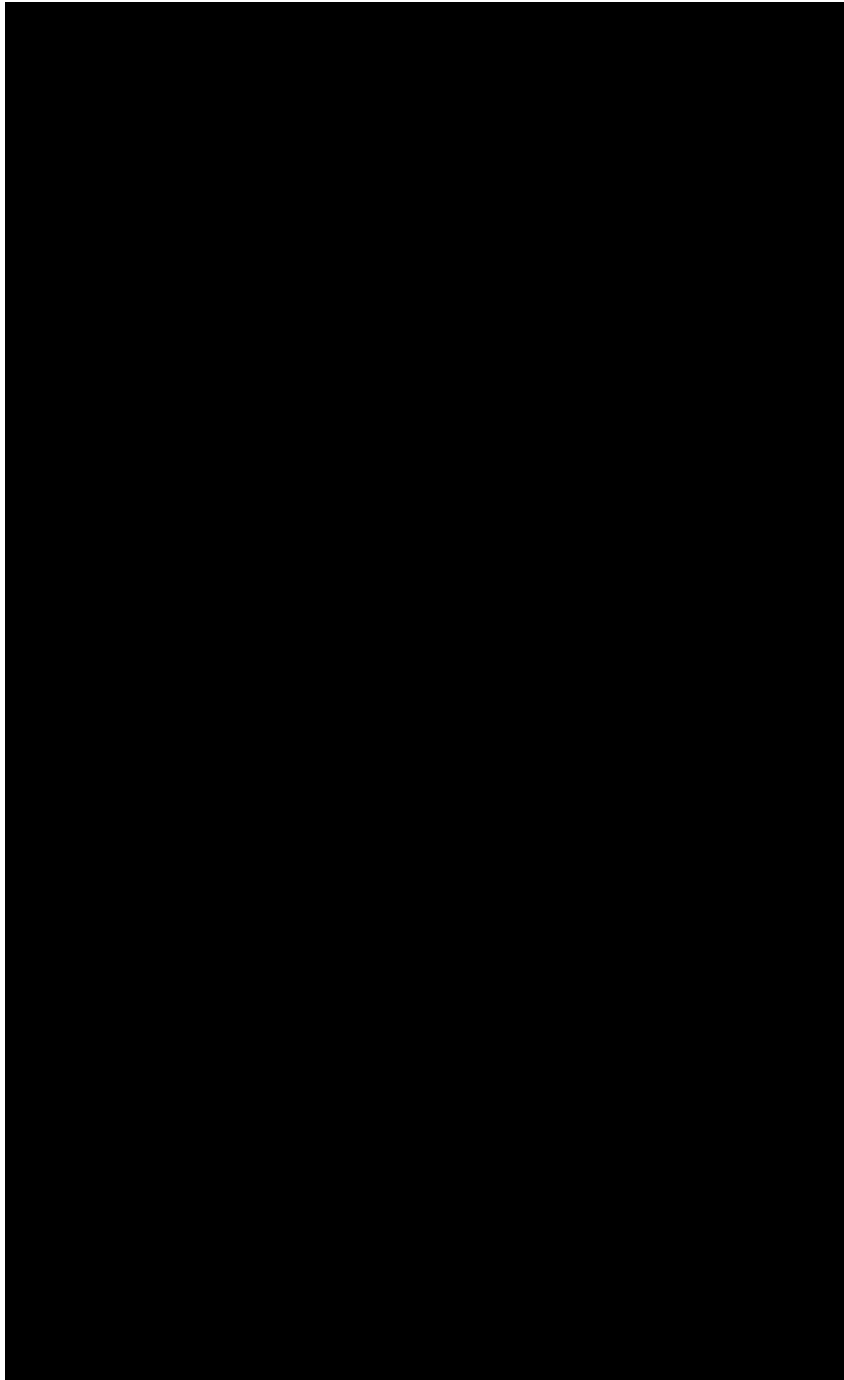


27. I am familiar with the files set forth above. The files (and their corresponding exhibits) set forth above are true and correct copies of ParkerVision's business records that were created, kept, and maintained in the ordinary course of ParkerVision's business. As part of its business, ParkerVision created, kept, and maintained records of this type. The technical files were created under my supervision and/or direction and created as of the dates shown above. With regard to the layout and schematic files above, they were created at or around the time that the designs they reflect were implemented by individuals with knowledge of those designs and as directed by me. I had knowledge of the reflected designs at that time. The making of these layouts and schematics was a regular practice of ParkerVision at the time. With regard to all of the other documents listed above, they were created at or around the time that the testing/evaluation that they relate to occurred by individuals with knowledge of the testing/evaluation. I had knowledge of the testing/evaluation, press releases, and agreements discussed in these documents at that time. Testing/evaluation, issuing press releases, and entering into agreements was a regular practice of ParkerVision at the time.

28. From at least March 6, 1997 through the filing of U.S Patent No. 6,061,551 (from which the '528 patent claims priority) on October 21, 1998, ParkerVision employees worked consistently on the design, development, testing,

and/or evaluation of the Eddie Chip. From at least January 20, 1998 through October 21, 1998, ParkerVision employees worked consistently on the design, development, testing, and/or evaluation of the Eddie Chip and the circuit board into which the Eddie chip was incorporated.

29. ParkerVision files related to the design, development, testing, and/or evaluation of the Eddie chip and circuit board discussed above are maintained in a Relativity database. The Relativity database shows the metadata including file extension, file name, and last modified date of these files. A search of the database was run. Below is an excerpt from the search.



30. The results of the search were exported to a excel spreadsheet which is shown in Exhibit 2029. The files in the spreadsheet reflects ParkerVision's continuous work from at least January 1997 through October 1998 related to designing and developing the Eddie chip and circuit board.

31. The files reflected in the Relativity database are true and correct copies of ParkerVision's business records that were created, kept, and maintained in the ordinary course of ParkerVision's business. As part of its business, ParkerVision created, kept, and maintained records of this type. The files were created under my supervision and/or direction and created as of the dates shown in Exhibit 2029. These files were created at or around the time shown by individuals with knowledge of the design/development of the Eddie chip and circuit board and as directed by me. I had knowledge of the reflected design/development at that time. The making of these files was a regular practice of ParkerVision at the time.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge.

Dated: April 4, 2025



David Sorrells