A 3.5 GHz 25 W Silicon LDMOS RFIC power amplifier for WiMAX applications

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***Abstract* — This paper presents a 25 W Silicon LDMOS 2 stage RF integrated circuit (IC) designed for WiMAX at 3.5GHz. This IC is capable of handling the full 3.3 to 3.8 GHz band with flat RF performances. This paper details RF performances in the 3.4 to 3.6 GHz band. Under a 1 tone CW stimulus, this power amplifier delivers 29 W with a power added efficiency of 36.7 % and 26 dB linear gain. Under a 1 carrier WiMAX signal and at 36 dBm average output power, the device has a RCE better than -33.5 dBc and a 14 % drain efficiency typical.**

***Index Terms* — broadband amplifiers, integrated circuit, linear amplifiers, power amplifiers, Silicon.**

I. INTRODUCTION

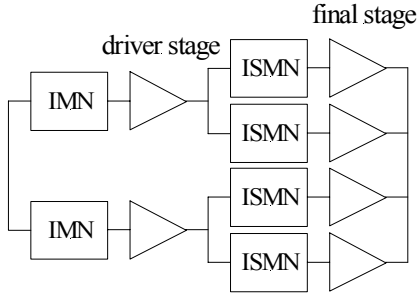
WiMAX base station systems requires power amplifiers with high output power, low distortion and high efficiency [3]. Moreover, cost is critical in this challenging market. High power LDMOS RFICs in over molded plastic packages have been developed to provide simple, low cost, reliable and competitive solution for base station amplifier systems. It is taking advantage of the over molded plastic technology which enables ease of use and has tight mechanical tolerances. Efforts have been put in device technology, modeling, packaging and design to provide first pass working RFICs for WiMAX at 3.5 GHz.

This paper presents a 25W Silicon LDMOS 2 stage integrated circuit with excellent RF performances over the 3.4 to 3.6 GHz band. This is the first report demonstrating this type of Silicon LDMOS multistage amplifier performances at 3.5 GHz and at such a power level.

II. DESIGN STRATEGY AND TOPOLOGY

This 2 stage IC has been designed with Freescale's HV7IC technology. Active part has been optimized to achieve high RF performances for frequencies higher than 2.2 GHz. Unit gate width has been chosen to maximize maximum available gain and transition frequency. Also, HV7IC passives provide improved performances compared to earlier IC generations.

Simulations have been done with an electro thermal model (MET) especially extracted, fitted and validated for this 3.5 GHz application. Design strategy has been to limit the scaling of the active part as much as possible from the extracted and validated size. This limited scaling has major advantages such as confidence in the model used. Moreover, splitting the final stage into small chunks allows taking care of the thermal distribution across the fingers. The design topology is shown on Fig1. Final stage is split into 4 active blocks and the driver stage into 2 active blocks. This allows a better feeding for all the final stage fingers across the active tubs. There is an output pre-matching made with a high pass shunt L network.



ISMN: inter stage matching network
IMN: input matching network

Fig.1 design topology

An extensive use of electromagnetic (EM) simulations for the integrated passives and full wave EM simulations for the wire arrays allowed accurately centering the design and getting a first pass working IC.

III. PULSE LOAD PULL PERFORMANCES

Pulse load pull has been done using a Maury system with passive tuners, pulse width was set to 9 us with a 10% duty cycle [4].

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	Gain (dB)			Efficiency (%)			P1dB (W)		
Frequency (GHz)	3.4	3.6	3.8	3.4	3.6	3.8	3.4	3.6	3.8
25W IC simulation	25.5	25.0	23.3	43.1	42.3	42.0	40.7	38.5	36.7
25W IC measured	26.3	25.4	22.8	43.7	41.7	40.1	38.0	37.4	37.5

Table 1 summary of pulse load pull performances at P1dB and at maximum efficiency location

Table 1 shows pulse load pull performances between 3.4 and 3.8 GHz at P1dB and at maximum efficiency location. The IC was biased at 28V Vd, 70mA stage 1 quiescent current (Idq1) and 280mA stage 2 quiescent current (Idq2). These bias conditions have been chose in order to capture the right P1dB thanks to a small gain expansion versus power. These results show that the simulation is very close to the measured load pull results. The IC is capable of good performances in the full 3.4 to 3.8 GHz band with a flat PAE and output power. In order to maximize the performances, 2 dedicated boards have been tuned in the 3.4 to 3.6 GHz band and in the 3.6 to 3.8 GHz band.

IV. RF BROADBAND PERFORMANCES

Load pull data show that the IC is capable of handling the full 3.4 to 3.8 GHz bandwidth. The following data are focusing on the 3.4 to 3.6 GHz band. A demonstration board has been generated with TACONIC RF35 material (relative permittivity = 3.5, substrate thickness = 20 mils) and tuned on a power bench for best 1 tone CW P1dB performances across the band. The strategy was to use as few chip components as possible and print most of the RF matching and fundamental decoupling networks. This allowed minimizing the insertion losses of the matching networks. Fundamental decoupling network on the drain supply lines uses a printed butterfly that allows a very good and broadband decoupling (isolation better than -30 dB between 3.2 and 3.9 GHz). A dual feeder is used to maximize the video bandwidth. Input and output pre-matching are done inside the package. Remaining input matching is done on the board. That showed to be quite useful to fine-tune the gain flatness and, moreover, it gives to the user another level of flexibility.

A. Small signal data

Small signal response of gain and input return loss versus frequency is shown on Fig.2. The IC is biased in class AB with Vd1=Vd2=28V, Idq1=110mA and Idq2=240mA (WiMAX bias conditions). In the 3.4 to 3.6 GHz band, gain is 26 dB with flatness better than 0.5 dB. Input return loss is very broadband and is better than -13 dB.

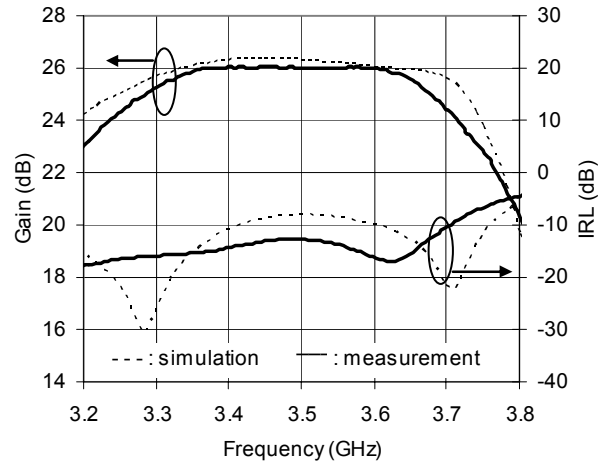

Fig.2. Gain and input return loss versus frequency with device biased at 28V Vd, 110mA Idq1 and 240mA Idq2.

Gain and IRL are in good agreement with the simulation as well as the behavior over frequency.

B. 1 tone CW P1dB data

Some 1-tone CW drive-ups of gain and power added efficiency versus output power are shown on Fig.3 and Fig.4. Data have been taken at 3.4 GHz and 3.6 GHz. The IC is biased in class AB with Vd1=Vd2=28V, Idq1=70mA and Idq2=280mA (P1dB bias conditions).

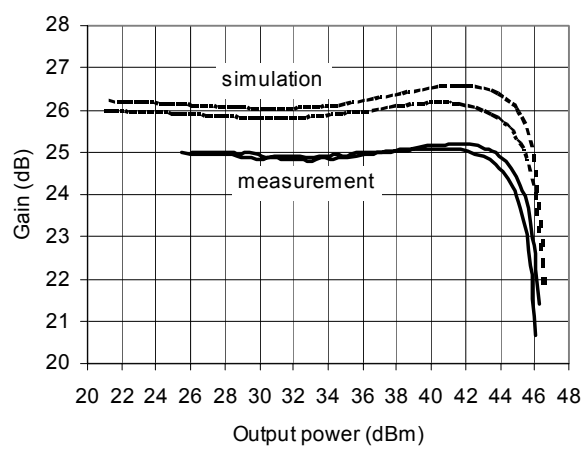

Fig.3. Gain versus output power with device biased at 28V Vd, 70mA Idq1 and 280mA Idq2 at the 2 edges of the band.

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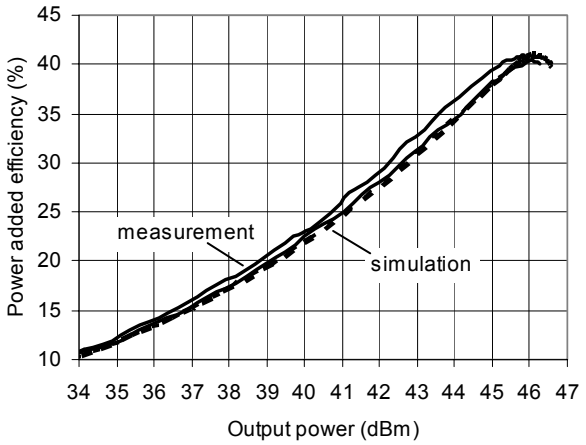

Fig.4. PAE versus output power with device biased at 28V Vd, 70mA Idq1 and 280mA Idq2 at the 2 edges of the band.

P1dB is higher than 29W and power added efficiency higher than 36.7% for the 2 stages.

Simulation prediction was also very good with PAE being only 2% higher in simulation at P1dB. Moreover, power prediction is good, being less than 0.5 dB higher in simulation.

C. Video bandwidth data

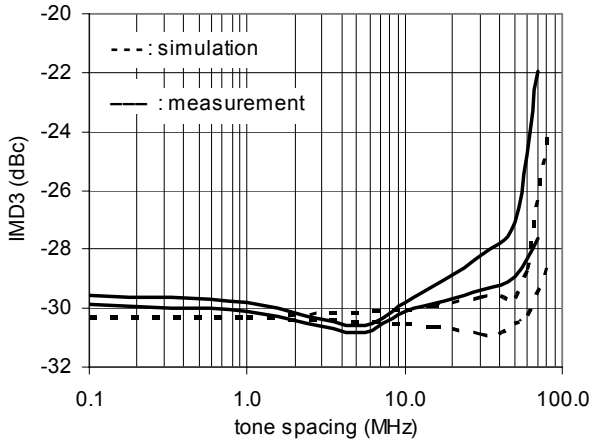

Fig.5. IMD3 versus tone spacing at 15W average output power with device biased at 28V Vd, 110mA Idq1 and 240mA Idq2, center frequency = 3.5 GHz.

Video bandwidth is critical for WiMAX. Carrier bandwidths can go from 1.75 MHz to 28 MHz, therefore, the corresponding amplifiers need a wide instantaneous video bandwidth. This test has been run on this IC. A 2-tone CW signal has been used and the IC delivered 15W average output power at -30 dBc IMD3. The tone separation has been varied from 100 kHz to 80 MHz at this power level with the center frequency being set at 3.5 GHz. Result of IMD3 upper and lower versus tone spacing is shown on Fig.5. The IMD3 resonance occurs at 60MHz. This video bandwidth value is in line with expectations for an amplifier of this power range.

D. WiMAX characterization

WiMAX is supported by 2 main standardization bodies: IEEE and ETSI. Both aims to offer high data rate based on OFDM type of transmission in various frequency range, mainly around 2.5 and 3.6 GHz. The WiMAX signal is characterized by its signal bandwidth (from 1.75 to 28 MHz), its type of modulation (BPSK, QAM…) and its Peak To Average Ratio (PAR). Depending on signal configuration, 75 Mbit/s can be achieved.

Quality of the transmitted signal thru the RFPA is characterized by Relative Constellation Error measurement [1]. In addition, the signal has to fulfill Mask emission requirement according to local rule.

For this study, we have used 7 MHz bandwidth signal and 64 QAM-3/4 modulation according 802.16d standard. The PAR of the signal is 9.5 dB at 0.01% probability.

As already mentioned, the IC is designed to give the flexibility to get best performances. In addition to the load line optimization capability, it offers the possibility to fine tuning the Idq of each stage to maximize the performances, e.g. driver stage or final stage in a line up. Previous characterization demonstrated that the most stringent parameter to meet is the RCE, consequently the mask data are not presented.

In Fig.6 is presented the gain, efficiency and RCE versus frequency for a final stage tuning at Pout = 36 dBm average.

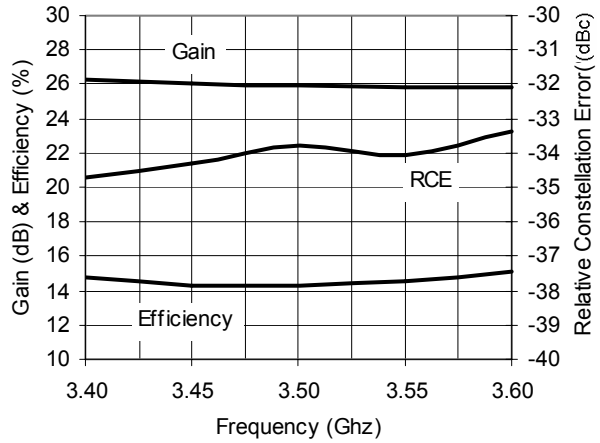

Fig.6. Gain, RCE and Efficiency versus frequency with device biased at 28V Vd, 110mA Idq1 and 240mA Idq2.

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RCE and efficiency versus average output power are presented for 2 different Idq tunings at 3.6 GHz in Fig.7.

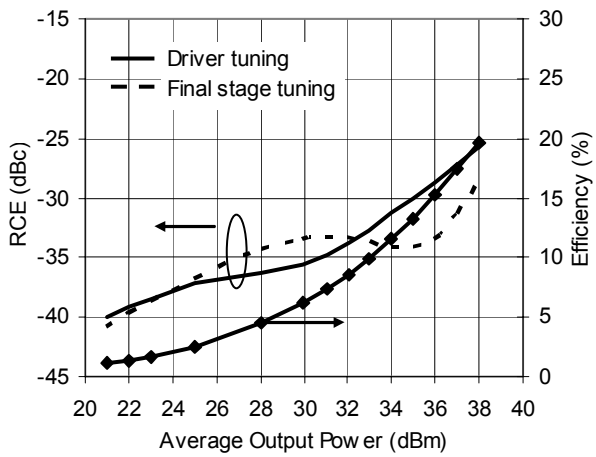

Fig.7. RCE and Efficiency versus Average Output Power.

Characterization demonstrated that the IC is able to deliver 36 dBm average power with 26 dB gain, 14% efficiency and excellent linearity. Those performances are competitive against discrete type of line-up.

E. Linearization

For a 36 dBm average output power, the -31 dBc RCE specification is met with a little margin. In the real life, the designer will choose to operate at 9~10 dB back off to take into account performance variation over temperature range, manufacturing spread… At such a back off, the efficiency falls around 10 **%.**

The natural step forward consists in improving the system efficiency, which impacts both equipment cost (cooling, power supply, weight,…) and the operational cost (energy bill). There are several paths to increase the efficiency. One possibility consists in implementing a linearization system like Digital Pre-Distortion.

The IC has been characterized with a WiMAX signal of 7 MHz bandwidth at 3.6 GHz. The pre-distortion algorithm uses a polynomial description to model the PA. The corrected RCE is shown on Fig.8. Digital Pre Distortion improves this RCE by 10 dB at 36 dBm average output power, or allows reducing the back-off by 2 dB while still meeting the standard specifications.

DPD allows the IC to work at a higher average output power. For example, at a constant linearity of -33.5 dBc RCE, the output power jumps from 36 dBm to 40 dBm. The associated efficiency jumps from 14 % to 24 %.

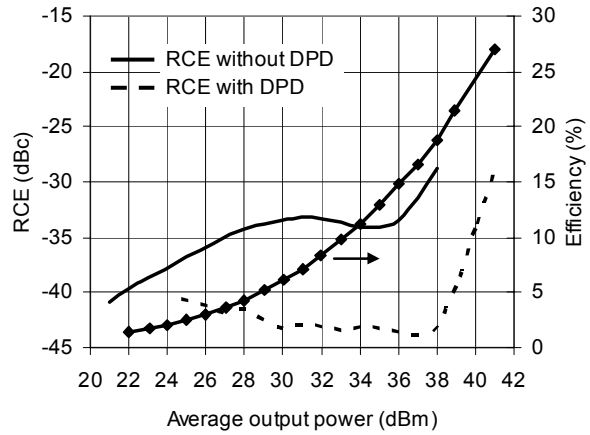

Fig.8. RCE and Efficiency versus Average Output Power with DPD.

V. CONCLUSION

A realization of a Silicon LDMOS 2 stage integrated power amplifier working from 3.3 to 3.8 GHz has been presented. In the 3.4 to 3.6 GHz band, this amplifier is able to deliver more than 29W and 36.5% power added efficiency at P1dB. Small signal gain is 26 dB with less than 0.5dB flatness. Video bandwidth is in the range of 60 MHz and WiMAX performances show 14% drain efficiency and -33.5 dBc RCE at 36 dBm average output power. At this particular linearity level, a DPD linearization system allows to get 24 % efficiency.

We can highlight that performances are quite close to discrete ceramic parts and this IC is a first pass working design thanks to accurate electro magnetic simulations and models.

To our knowledge, this is state of art performances for a Silicon LDMOS integrated power amplifier working at those frequencies.

REFERENCES

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