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A High-Performance Digital Color Video Camera

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ABSTRACT

Typical one-chip color cameras use analog video processing circuits. An improved digital camera architecture has been developed using a dual-slope A/D conversion technique, and two full custom CMOS digital video processing ICs, the "CFA processor" and the "RGB post-processor". The system uses a 768 x 484 active element interline transfer CCD with a new "field-staggered 3G" color filter pattern and a "lenslet" overlay, which doubles the sensitivity of the camera. The digital camera design offers improved image quality, reliability, and manufacturability, while meeting aggressive size, power, and cost constraints. The CFA processor digital VLSI chip includes color filter interpolation processing, an optical black clamp, defect correction, white balance, and gain control. The RGB post-processor digital IC includes a color correction matrix, gamma correction, two-dimensional edge-enhancement, and circuits to control the black balance, lens aperture, and focus.

1. INTRODUCTION

A significant amount of signal processing is needed to obtain high-quality color video images from a one-chip color CCD sensor. A wide variety of color filter array (CFA) patterns can be used to provide color images.[1] In current single-sensor color cameras and camcorders, the video signal processing is accomplished with analog circuits.[2-5] The constraints of analog video processing places practical limitations on the sophistication of the image processing which can be implemented in such systems. This constrains the choice of CFA patterns that can be used, and compromises image quality.

Digital processing offers many system advantages, but can result in large, expensive, and power-hungry cameras, unless digital VLSI techniques are used. Digital processing has been employed in a commercially available three-sensor camera,[6] and numerous digital designs for two-sensor[7] and single-sensor[8-10] cameras have been described in the literature. The first operational one-chip color CCD imaging system using full custom VLSI digital processors has been reported previously.[11,12] This paper describes the application of these VLSI video processing ICs in a higher performance camera system, using a newly developed CCD image sensor with an improved color filter array pattern, and a dual-slope A/D conversion technique.

Figure 1 shows a simplified block diagram of the digital color camera. The camera lens focuses the image onto the color CCD image sensor. The sensor output signal is digitized at a 14.318 MHz sample rate. The digitized signal from the CCD sensor is processed by two full-custom CMOS ICs, the "CFA Processor", and the "RGB Post-Processor". The processing is pipelined, and operates at the same pixel rate as the image sensor, so that a framestore is not required. The ICs have been designed to operate with a variety of image sensors and color filter options. To minimize the chip areas, the signal processing has been carefully designed to eliminate the need for multipliers and to reduce the amount of line delay memory required.

2. IMAGE SENSOR

The sensor is a high-performance silicon charge-coupled device (CCD) with an interline transfer architecture and 2:1 interlaced readout. The device is built with an advanced true two-phase, two-polysilicon, NMOS CCD technology. The p+npn- photodetector elements operate in a fully depleted mode. Therefore, charge from the photodiodes is completely transferred to the vertical CCDs (VCCD), eliminating the image lag seen with conventional np photodiodes. A p-well vertical overflow drain structure allows antiblooming protection. A close proximity refractory metal lightshield greatly reduces image smear. The active area is 8.9 mm (H) x 6.6 mm (V), and the total chip size is 9.9 mm (H) x 7.7 mm (V).

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Figure 2 is a functional block diagram of the sensor, which consists of 371,712 active photodiodes, 768 vertical (parallel) CCD shift registers, one horizontal (serial) CCD shift register and one output amplifier. Both registers incorporate two-level polysilicon and true two-phase buried channel CCD technology,[13] as shown in Fig. 3. The pixels are arranged in a 768 (H) x 484 (V) array in which an additional 12 columns and 5 rows of light shielded pixels are added as a dark reference. The pixel architecture is shown in Fig. 4. An image is acquired when incident light, in the form of photons, falls on the array of photodiodes and creates electron-hole pairs within the silicon substrate. This charge is collected locally by the formation of potential wells created at each photodiode site. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and nonlinearly dependent on wavelength. When the photodiode charge capacity is reached, excess electrons are discharged to the substrate, to prevent blooming.

The accumulated or integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transported from the photodiodes to the vertical shift registers by applying a large positive voltage to one of the vertical clocks. This reads out every other row of photodiodes, thus transferring one of the two interlaced fields into the vertical CCD registers. The charge is then transported from the vertical CCD registers in a line-by-line or parallel fashion to the horizontal CCD register. Finally, the horizontal CCD register transports this 'line' of charge in a pixel-by-pixel or serial fashion to the output amplifier. The remaining field is clocked out in a similar fashion by applying a positive voltage to the other vertical clock phase, thus completing interlaced readout of one frame. Both the horizontal and vertical shift registers use traditional complementary clocking for charge transport. Transfer to the horizontal CCD begins when ØV2 is brought high and ØV1 is brought low, causing charge from the ØV1 and ØV2 gates to transfer a line of charge into the horizontal shift register. The sequence ends when ØV2 is brought low while the horizontal CCD reads out the first line of charge.

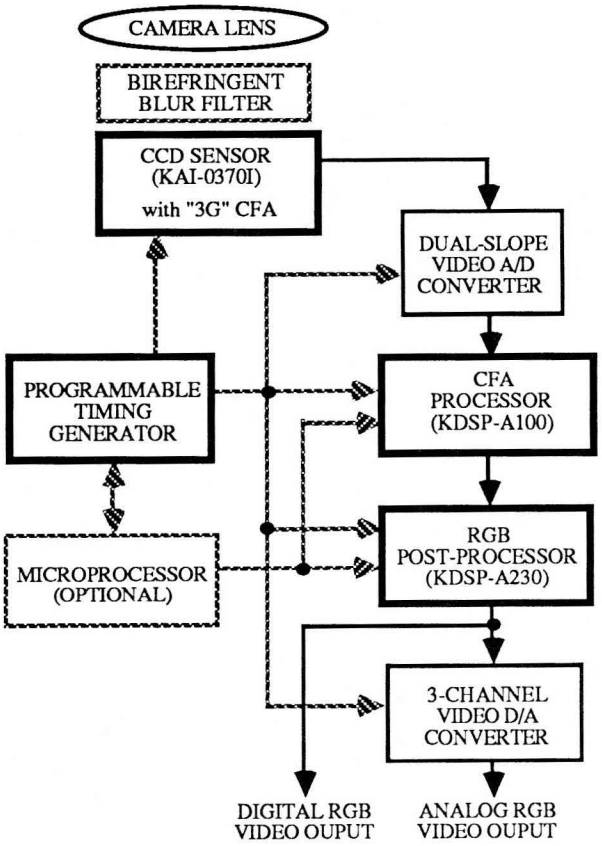


Fig. 1 Digital Camera Block Diagram

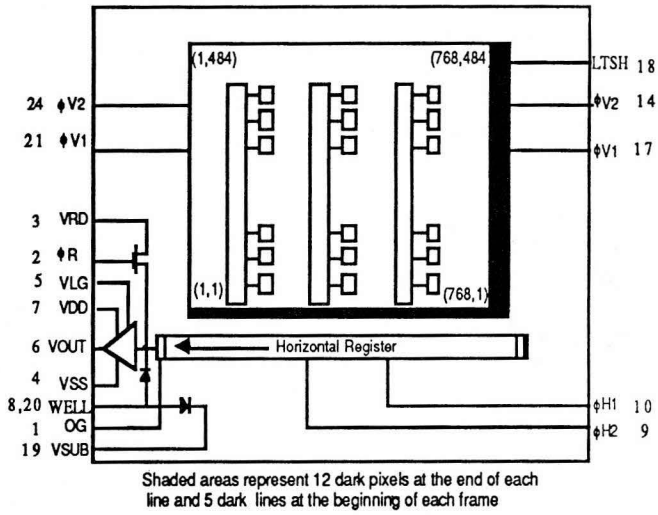


Fig. 2 CCD Sensor Block Diagram

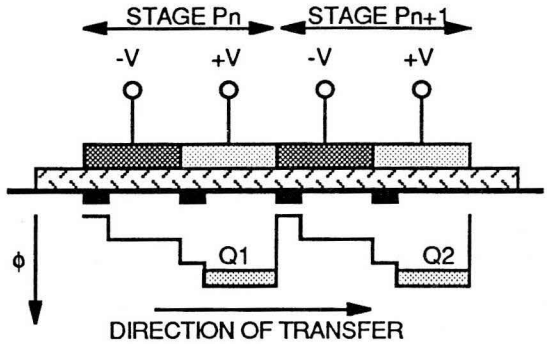


Fig. 3 True Two-Phase CCD Cross Section

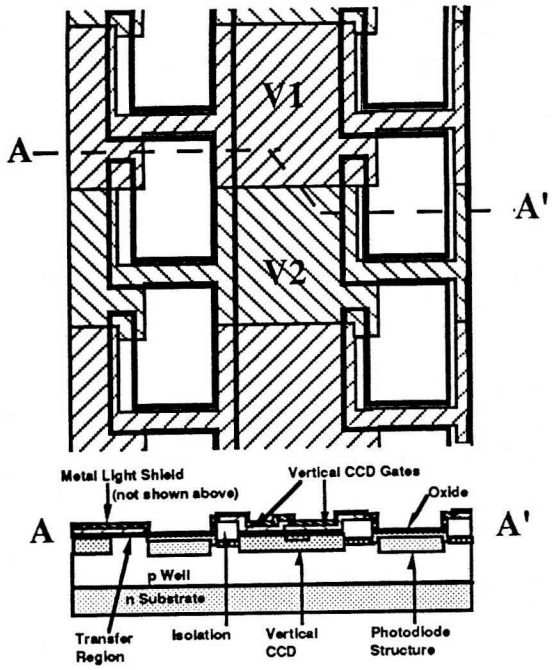


Fig. 4 CCD Pixel Architecture

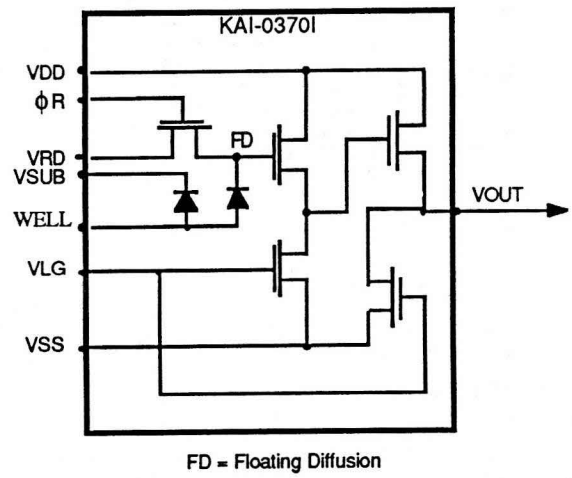


Fig. 5 CCD Output Schematic

A schematic of the output structure is shown in Fig. 5. On each falling edge of ØH2, a charge packet is dumped over the output gate (OG in Fig. 2) onto the output node or floating diffusion (FD in Fig. 5). The potential of the floating diffusion varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression

$$\Delta V_{fd} = \Delta Q / C_{fd}, \qquad (1)$$

where ΔV_{fd} is the change of the floating diffusion voltage, ΔQ is the charge transferred onto the floating diffusion, and C_{fd} is the capacitance of the floating diffusion. The translation from electrons to voltage is called the output sensitivity or charge-to-voltage conversion. After the charge has been sensed off-chip, the reset clock (ØR) removes the charge from the floating diffusion via the reset drain (VRD). This in turn returns the floating diffusion potential to the reference level determined by the reset drain voltage. A two-stage source-follower amplifier is used to provide the video output signal (VOUT).

3. COLOR FILTER ARRAY

The image sensor is overlayed with the new "field-staggered 3G" color mosaic filter pattern shown in Fig. 6. The CFA contains 75% green (G) photosites and 25% red (R) and blue (B) photosites. By devoting most of the photosites to luminance, the scene is sampled in a manner compatible with the human visual system, which is more sensitive to high spatial frequency luminance variations than to high spatial frequency chrominance variations[14]. When the proper image processing is used to reconstruct RGB values for each photosite,[15,16] the "3G" CFA pattern can provide images that are sharper, yet have reduced color aliasing, compared to images from other stripe or mosiac CFA patterns. Because of the complexity of the required reconstruction processing, digital signal processing techniques are more appropriate than analog processing circuits. A birefringent blur filter[17,18] helps to eliminate aliasing and provides color co-incidence between the chrominance samples and the adjacent luminance samples.

Field 1	G	G	G	R
Field 2	G	R	G	G
Field 1	G	G	G	B
Field 2	G	B	G	G

Fig. 6 Field Staggered 3G CFA

Field 1	G	G	G	R
Field 2	G	G	G	R
Field 1	G	B	G	G
Field 2	G	B	G	G

Fig. 7 Line Staggered 3G CFA

The newly developed "field-staggered 3G" CFA is an improvement on the "line-staggered 3G" CFA shown in Fig. 7, which was used in earlier cameras.[12] In interlaced video applications, every second line of the CCD sensor is read out during field 1, while the remaining lines are read out during field 2. The color filter pattern must be designed to operate properly with this interlaced readout. If, for example, red photosites were located only on every second (odd) line of the sensor, while blue photosites were located only on the remaining (even) lines, red would then be sampled only during field 1, and blue would be sampled only during field 2. The resulting image would exhibit a severe 30 Hz yellow-cyan hue flicker, which would produce an unacceptable level of visual discomfort,[19] unless a chrominance field store were used.

In order to accommodate interlaced readout, the "line-staggered 3G" CFA in Fig. 7 is arranged so that each line is repeated twice, thus the field 1 and field 2 sampling is identical. This means that the red and blue sampling occurs only in every fourth column of pixels in the horizontal direction. The locations at which red and blue are sampled are offset in the horizontal direction by 2 pixels. The "field-staggered 3G" CFA in Fig. 6 is arranged so that the lines of field 2 are shifted horizontally by two pixels relative to the lines of field 1. This allows red and blue to be sampled at every second column of pixels in the horizontal direction. This creates a more checkerboard-like chrominance sampling pattern that provides improved chrominance resolution in the horizontal direction.[20] Because the two digital processing ICs were designed with flexibility in mind, the new "field-staggered 3G" CFA can be accommodated with only a minor change in the external timing signals that control the CFA processor IC.

The image sensor includes a lenticular array, fabricated on top of the CFA, which is integrated above the photosensors.[21] These "lenslets" are an array of convex lenses formed above each photosite, as shown in Fig. 8. The lenslets focus the light away from the opaque light shields and into the center of the photodiodes. This increases the sensitivity by a factor of more than two, since most of the photons which would normally hit the light shields and be "wasted" are now collected by the photodiodes. This also slightly decreases aliasing and reduces smear. A photomicrograph of the pillow-shaped lenses which form the lenslet overlay are shown in Photo 1.

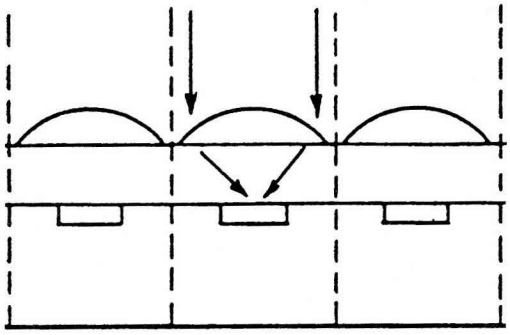


Fig. 8 Lenslet Structure

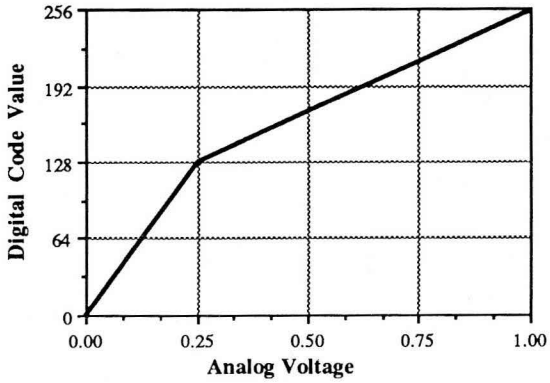


Fig. 9 Dual-Slope A/D Characteristic

4. A/D CONVERSION

The sensor output is processed by a conventional clamp / sample-and-hold circuit that implements correlated double sampling.[22] This circuit forms a continuous analog video signal, while eliminating the noise associated with resetting the CCD floating diffusion output and suppressing low frequency noise such as the 1/f noise from the on-chip source follower amplifiers. The processed sensor output signal is digitized with a commercially available 8 bit parallel "flash" A/D converter,[23] which allows access to the mid-point of the resistor ladder. The voltage on the mid-point ladder pin has been set to provide the conversion characteristic shown in Fig. 9. This technique provides the equivalent of a 10-bit digital conversion at low signal levels, and a 7-bit digital conversion at high signal levels. The dual-slope quantizer is designed to reduce the quantization distortion in the gamma-corrected output signal relative to the quantizaton distortion using a linear 8-bit quanitizer. The digitized sensor signal is input to the "CFA processor".

5. CFA PROCESSOR IC

A simplified block diagram of the functions performed by the CFA processor chip[24] is shown in Fig. 10. The first on-chip operation is an optical black reference clamp. The dark current of CCD image sensors is very dependent on the operating temperature. The purpose of the black reference clamp is to subtract off the average dark current value of the sensor. The digital implementation is more stable and less expensive than an analog implementation, but slightly reduces the useful operating range of the A/D converter. The sensor defect concealment allows defective photosites to be concealed, by substituting the values of the previous horizontally adjacent pixels of the same color. Next, the chip incorporates a novel architecture, which interpolates the missing green (luminance) pixels using a linear quantization space finite impulse response (FIR) filter, and then reconstructs the missing red and blue pixels by interpolating the chrominance to luminance ratios in a logarithmic quantization space. This technique greatly reduces color edge artifacts, compared to linearly interpolating the red and blue values without utilizing the green signal.[25]

A more detailed diagram of the CFA processor implementation is shown in Fig. 11. The digitized pixel inputs (PIXIN(10)) from the A/D converter can be either a linearly quantized signal with a maximum of 10 bits, or a nonlinearly quantized signal with a maximum of 8 bits. The FORCE(2) control lines allow the input to be clipped to white or black values, in order to handle A/D overflow conditions or provide input image blanking. The chip includes an 8 bit-to-10 bit ROM look-up table (LUT), which is selected when the nonlinear A/D is used, and can be mask programmed to convert the 8-bit dual-slope characteristic shown in Fig. 9 to a 10-bit linear quantization chracteristic. The black reference clamp works by summing 512 pixel values from "black" photosites located in a line at the top of the image, using a hard-wired shift to obtain the average, and subtracting the average value from the rest of the image pixel values. Defective pixels are concealed using multiplexers controlled by the DEF(2) signals to substitute values from the appropriate pixels delays.

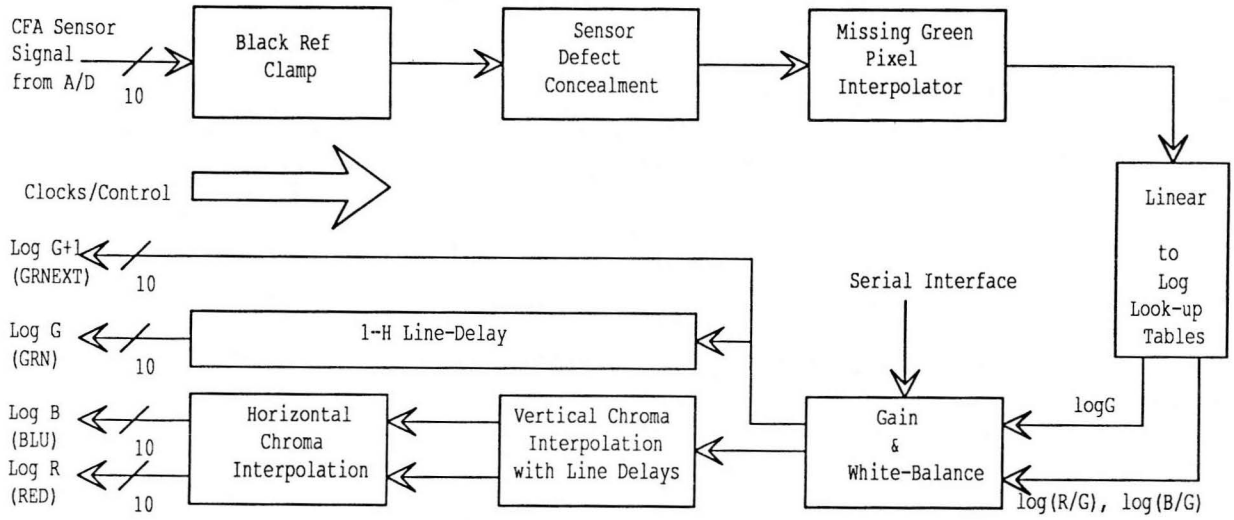


Fig. 10 CFA Processor Functions

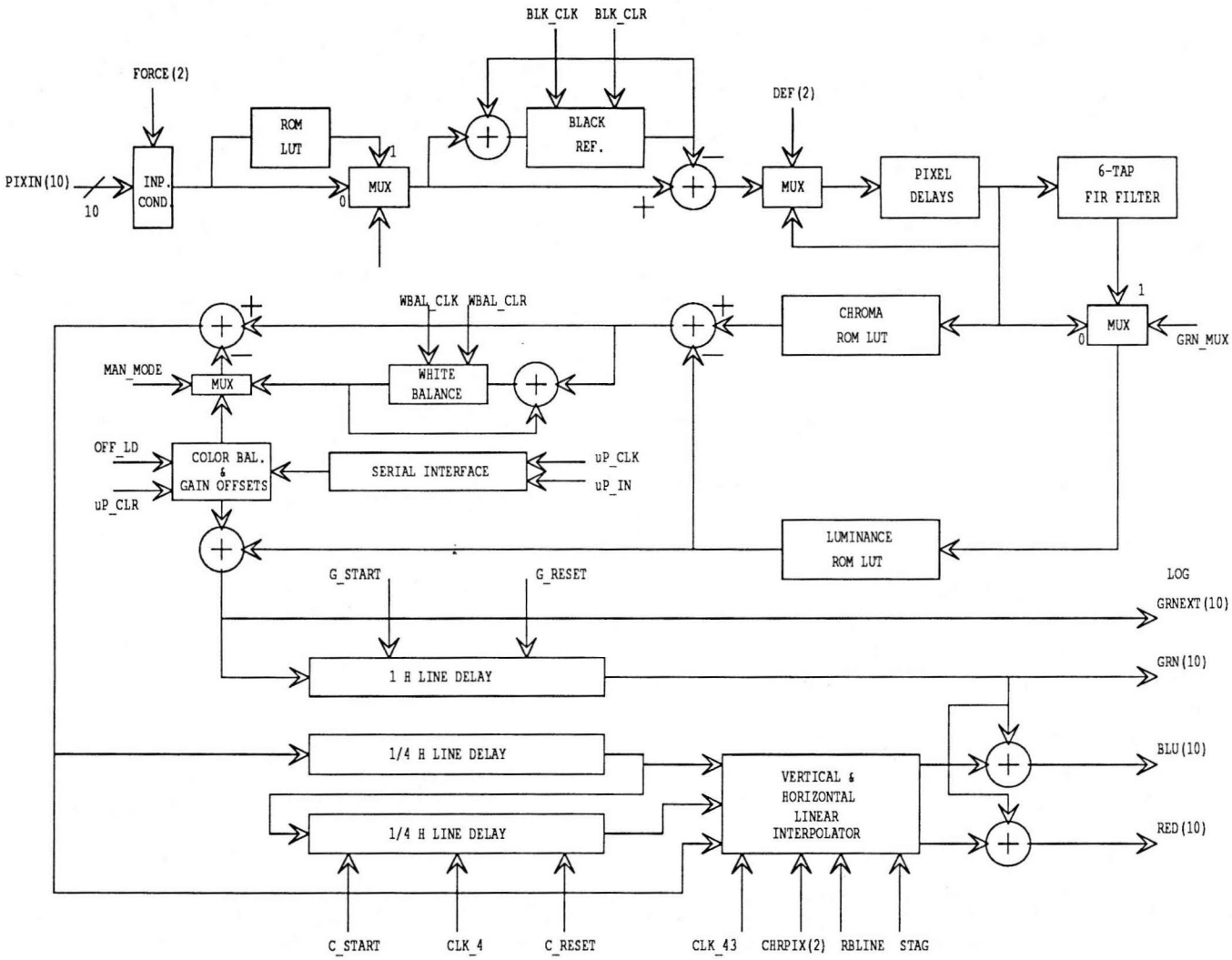


Fig. 11 CFA Processor Implementation

Values for the green signal at spatial locations corresponding to red and blue photosites are calculated using a 7-tap FIR interpolation filter. The filter impulse response is given by

$$y = \sum_{i=-3}^{+3} a_i x_i \qquad (2)$$

where a_i are the co-efficients and x_i are the "known" horizontally adjacent green pixel values centered about the "missing green" (red or blue) pixel locations. The filter is designed so that the point spread function of the missing green elements equals the point spread function of the green photosites.[16] The center (a_0) co-efficient equals zero and the filter is symmetric, so only three fixed co-efficient multiplications are required. The multiplications are implemented using hardwired shift and add or shift and subtract circuits, so that the entire filter requires only ten adders, an enormous area savings compared to multipliers.

The combination of the optical pre-filter and the missing green interpolation filter provides nearly perfect color co-incidence between the red or blue value and the interpolated green value at the same red or blue photosite. This allows the blue-to-green and red-to-green color ratios to be accurately determined. If the coarsely sampled red and blue records were independently interpolated, very disturbing false color artifacts would occur at luminance edge transitions. However, by linearly interpolating the blue-to-green and red-to-green color ratios, the colored edge artifacts can be almost completely eliminated.

The data is demultiplexed into green and line sequential red/blue channels and transformed using on-chip luminance and chroma ROMs programmed to provide logarithmic curveshapes. The blue-to-green and red-to-green ratios are formed by subtracting the log space signals, since the difference of two logarithmically quanitized signals equals the log of the ratio of the signals. The CFA processor chip includes a gain control circuit and a white balance circuit, which can operate automatically or under microprocessor control. These operate by adding log space offset values, rather than by using multipliers. The gain control works by adding or subtracting a value from the log green signal. This "gain offset value" is input to the CFA processor via a simple two-wire serial interface from a microprocessor, using data line uP_IN and clock line uP_CLK. Two "color balance offset values", which are added to the log R/G and log B/G values to obtain proper white balance, can also be input via the serial interface. Alternatively, proper white balance can be obtained using the on-chip white balance circuit, which averages the log R/G and log B/G signals when signaled by the WBAL_CLK and WBAL_CLR lines as the camera images a white card, and then subtracts the average values from the normal image.

The log color difference signals are linearly interpolated first in the vertical direction using on-chip line delays, and then in the horizontal direction using hardwired shift and add circuits. The linear interpolation circuits use a polyphase structure based on the commutative model.[26] Implementing the vertical interpolation before the horizontal interpolation reduces the size of the two red/blue line delays by a factor of four. The linearly interpolated log R/G and the log B/G signals are summed with the delayed log G signal to provide log R and log B values for each pixel of the array. These red and blue signals contain low spatial frequency color information and high spatial frequency luminance detail information derived from the green channel. The undelayed log G signal is also output and is used in the RGB post-processor edge enhancement circuit.

A photomicrograph of the CFA processor is shown in Photo 2. The chip is 10 mm x 10 mm with 94,000 transistors, and dissipates 330 mW at 5 volts. Both the CFA processor and the RGB post-processor chips were designed and fabricated in-house using a 2-micron CMOS single-poly, double metal process, and are packaged in standard 84-pin packages. The largest circuit block on the CFA processor is the green 1-H line delay, which is required to spatially align the green pixel data with the vertically interpolated red and blue data.

6. RGB POST-PROCESSOR IC

The logarithmically quantized 10-bit RGB outputs of the CFA processor are connected to the inputs of the second VLSI chip, the "RGB post-processor".[27] A simplified block diagram of the functions performed by this chip are shown in Fig. 12, and a more detailed diagram of the chip architecture is shown in Fig. 13. The logarithmically quantized RGB data from the CFA processor is first converted to linearly quantized data by three ROM look-up tables, prior to black level correction and matrixing. The average picture levels (APLs) for red, green, and blue are computed by three accumulators, and output to a microprocessor via a two-wire serial output interface, using data output line uP_OUT and clock line uP_OUT_CLK. The microprocessor can input RGB black level offset values, via data input line uP_IN and clock line uP_IN_CLK, to correct for lens flare or to adjust for user preferences.

A mask-programmable 3 x 3 color correction matrix is used to improve the color reproduction by correcting the camera responsivities properly for the display phosphor chomaticities. Figure 14 shows the measured color sensitivities of the CCD camera prior to matrixing. Notice that the CCD responsivity at any wavelength must always be positive, since a negative response to light is physically impossible. Figure 15 shows the optimum camera sensitivities for CRT displays incorporating SMPTE C phosphors with a D65 white point.[28]

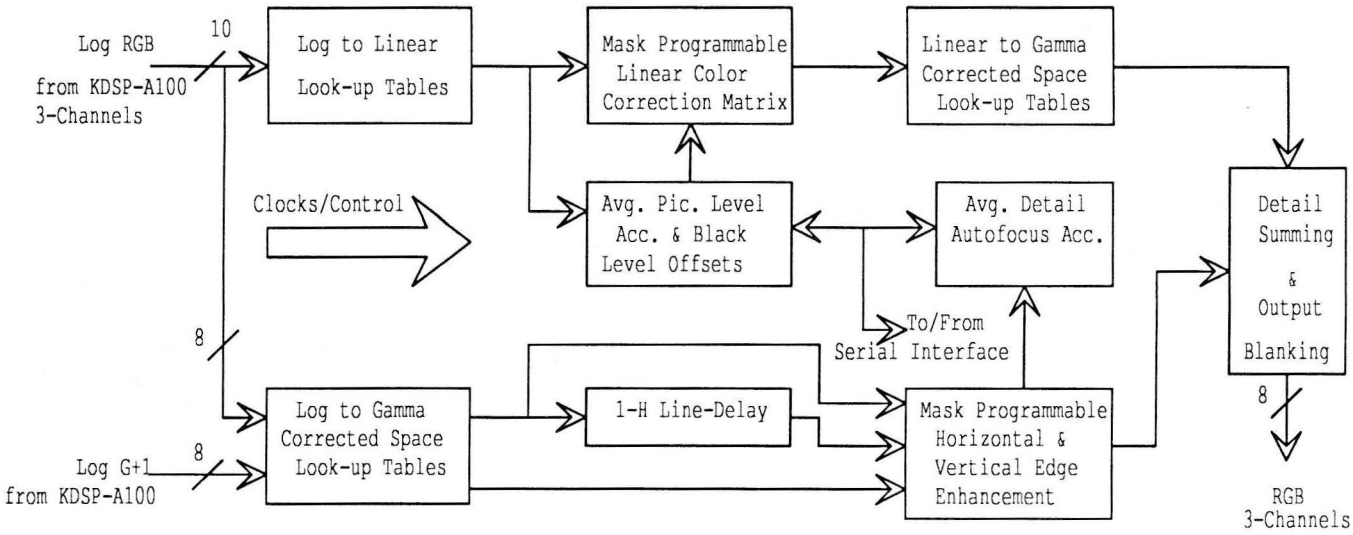


Fig. 12 RGB Post-Processor Functions

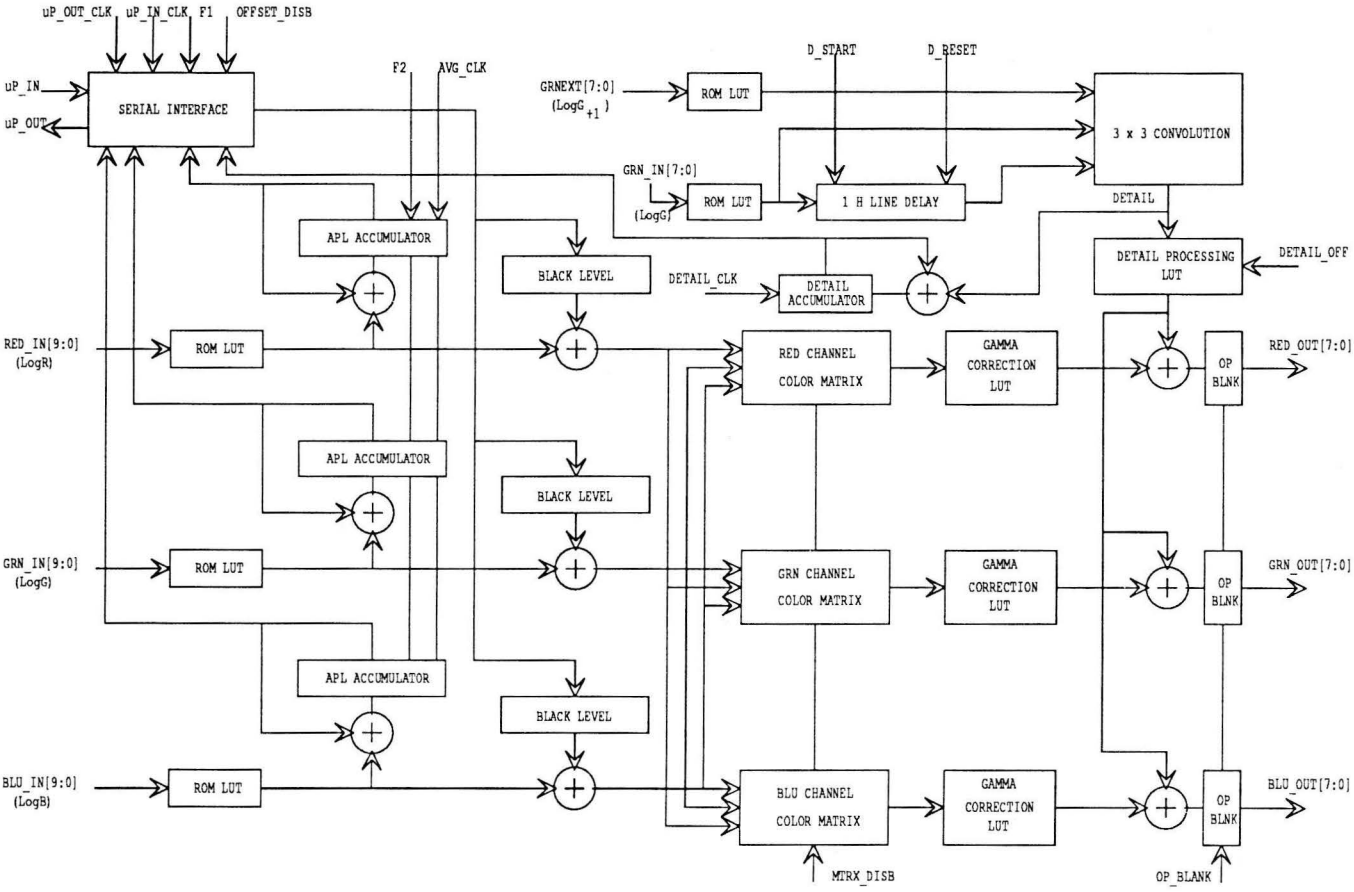


Fig. 13 RGB Post-Processor Implementation

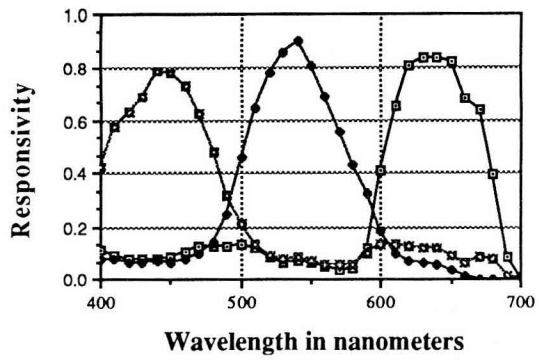


Fig. 14 CCD Camera Color Responsivities

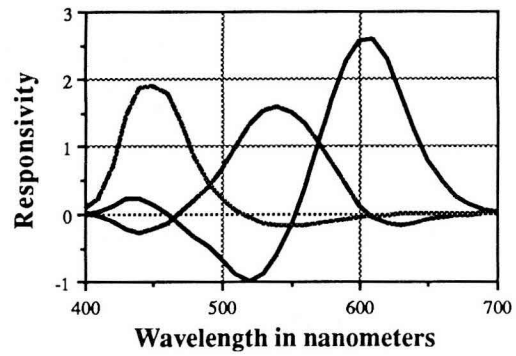


Fig. 15 Optimum Camera Responsivities

In order to achieve the required negative camera sensitivities, the 3 x 3 matrix shown below can be used

$$\begin{aligned} R_o &= a_{11} R_i + a_{12} G_i + a_{13} B_i \\ G_o &= a_{21} R_i + a_{22} G_i + a_{23} B_i \\ B_o &= a_{31} R_i + a_{32} G_i + a_{33} B_i. \end{aligned} \tag{3}$$

R_i, G_i and B_i are the linearly quantized, interpolated signals from the CFA processor, and R_o, G_o, and B_o are the color corrected matrix outputs. The co-efficients a_{ij} depend on the color-mixture functions of the phosphors used in the television display, and the responsivities of the RGB signals prior to matrixing, which includes the lens, infrared blocking filter, and color sensor.[29] Using the matrix listed below, the color responsivities of the camera can be corrected to appear as shown in Fig. 16

$$\begin{aligned} R_o &= 1.75 R_i - 0.19 G_i - 0.56 B_i \\ G_o &= -0.03 R_i + 1.25 G_i - 0.22 B_i \\ B_o &= -0.12 R_i - 0.38 G_i + 1.50 B_i. \end{aligned} \tag{4}$$

The negative off-diagonal matrix terms significantly increase the color saturation of the image. The matrix is implemented using cascaded metal-mask programmable shift and add or subtract (MPSAS) circuit modules. The red channel of the matrix is shown in Fig. 17. The green and blue channels have an identical form, but a different input signal mapping. Cascading the MPSAS modules as shown allows sufficient co-efficient accuracy to be maintained while using a minimum number of adders.

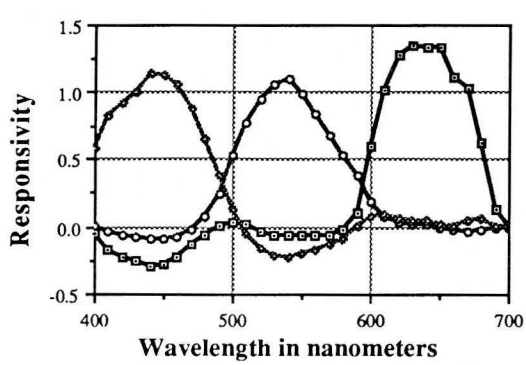


Fig. 16 Matrixed Camera Responsivities

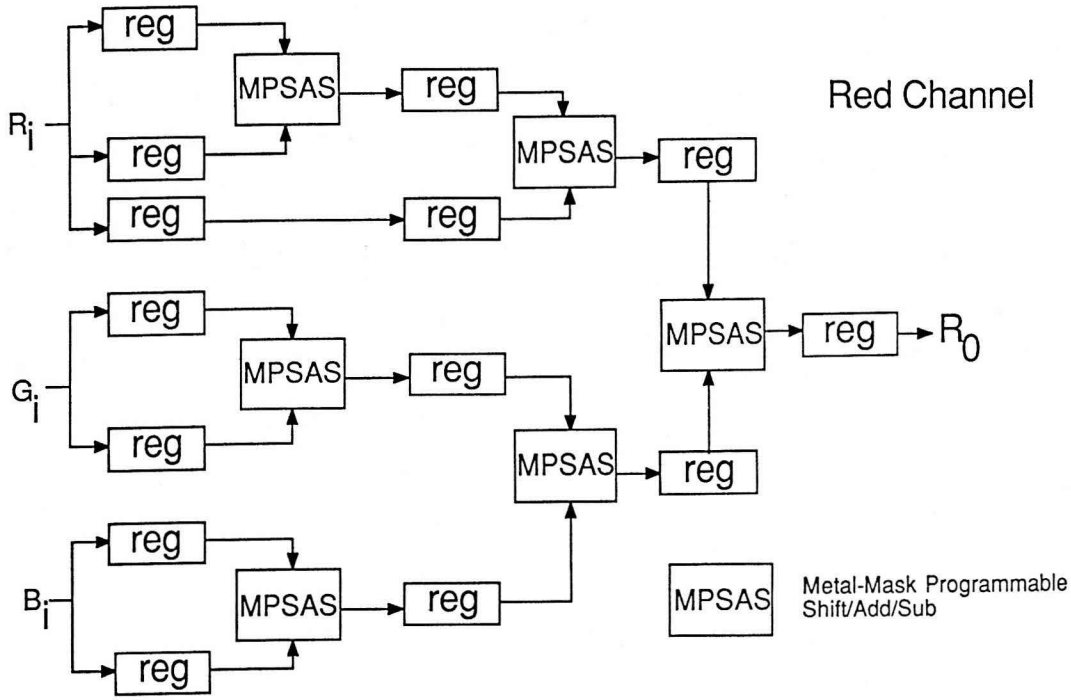


Fig. 17 Red Channel Matrix Implementation

The matrixed RGB signals are gamma-corrected using three on-chip ROM look-up tables, which are programmed using the SMPTE 240-M opto-electronic transfer equation[30]

$$C_{out} = 1.1115\ C_{in}^{0.45} - 0.1115 \text{ for } C_{in} >= 0.0228 \qquad (5)$$
$$C_{out} = 4.0\ C_{in} \text{ for } C_{in} < 0.0228$$

where C_{in} is the input code value normalized between zero and one, and C_{out} is the normalized output code value.

The RGB post-processor includes the novel edge-enhancement circuit[31] shown in Fig. 18. The vertical and horizontal high frequency edge "details" are extracted from the green channel, processed, and added back to the red, green, and blue video signals. This technique improves the subjective "crispness" of the image.[32] The unmatrixed green signal is used by the edge enhancement circuit to keep from introducing slight noise and artifacts into the detail channel as a result of matrixing. The chip includes an on-chip green signal line delay and makes use of the line delays on the CFA processor to provide symmetric three-line vertical edge enhancement. The vertical "detail" signal, which carries the high frequency edge information from the "-0.5 +1 -0.5" vertical filter, is horizontally filtered before being summed with the horizontal "-1 +2 -1" detail signal, in order to prevent double enhancement of diagonal edges. The horizontal details receive more boost than the vertical details, in order to compensate for the horizontally oriented optical pre-filter.

The horizontal and vertical detail signals are summed and processed by the detail processing ROM look-up table curve shown in Fig. 19. Low-level detail signals, which typically correspond to noise, are clipped to zero. Higher amplitude details are amplified, and very large edge signals are gradually suppressed to prevent over-enhancement. The detail signal is extracted and processed using a "lightness" type quantization characteristic, so that uniform sharpening occurs throughout the luminance range.[33]

A photomicrograph of the RGB post-processor chip is shown in Photo 3. The chip is 11.5 mm x 11.2 mm, with 115,000 transistors. The digital RGB output signals from the post-processor are converted to analog video signals using an off-the-shelf triple D/A converter.

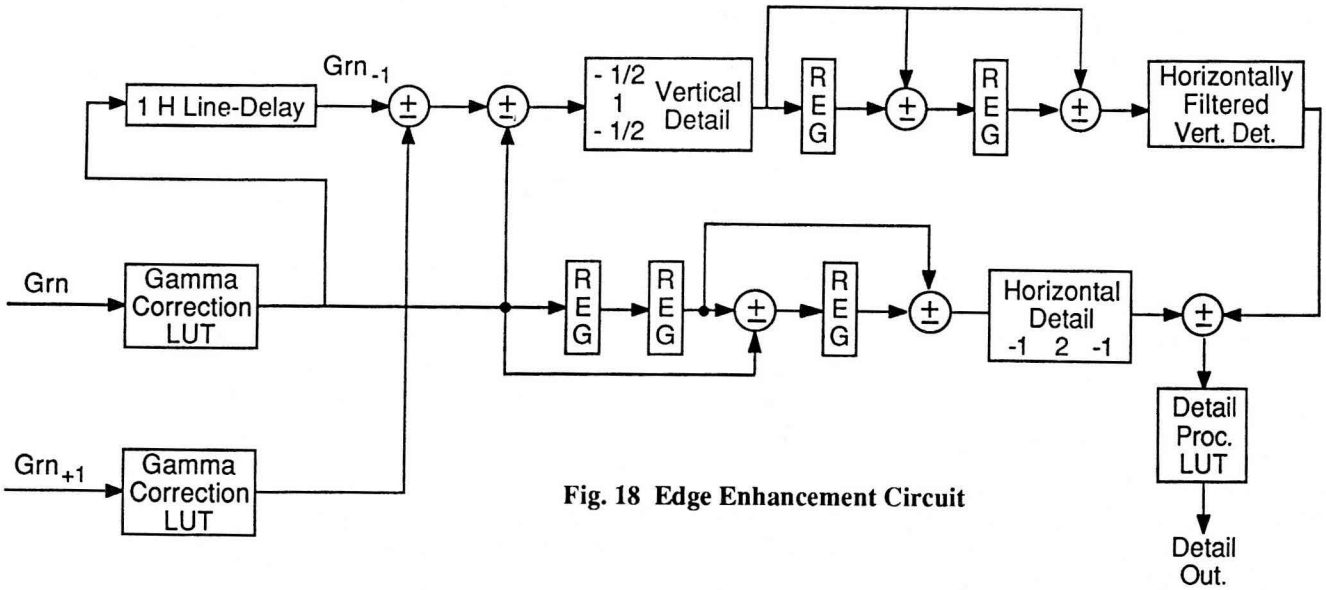
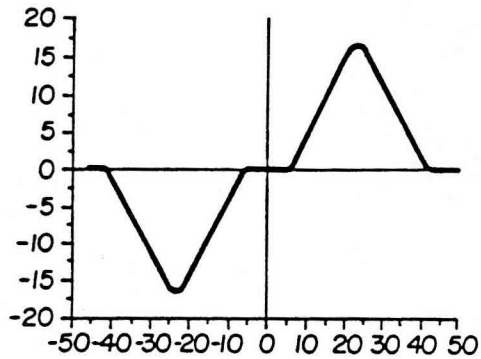


Fig. 18 Edge Enhancement Circuit

Fig. 19 Detail Processing LUT



7. SYSTEM DESIGN

All of the digital camera circuits, including the sensor and the two DSP chips, are controlled by a custom Programmable Timing Generator IC.[34] The chip is based on three custom EPROM NOR-planes, and incorporates pixel and line counters, 16 state-variable flip-flops, and 28 output flip-flops. A PC-based timing generation program allows the timing to be quickly developed or modified. The chip, which is 6.5 mm x 7.5 mm, was fabricated in a 1.6-micron CMOS process that includes n-channel EPROM transistors.

The CFA processor and RGB post-processor ICs were developed using software "emulation" rather than by constructing large hardware prototypes composed of off-the-shelf digital devices. This reduced the development time and allowed a large number of image processing options to be tested. The output of a single-chip color image sensor was digitized and stored in a custom image memory with a very flexible architecture. Images were loaded into an image processing computer, where the processing algorithms, chip architectures, and data path word lengths were optimized. Still images and short image sequences were then loaded back into the custom image memory and displayed on a video monitor.

The design of the chips was done entirely with a silicon compiler tool set, except for the ROMs and line delays which were designed using conventional tools and imported into the compiler environment. The data paths are designed with simple ripple-carry adders and dynamic registers. All data-path cells were obtained from internally developed parameterized generators.

Although the present prototype cameras use sensors with 768 horizontal pixels and a clock rate of 14.3 MHz, the CFA processor and RGB post-processor chips have been tested at clock frequencies between 1 and 15 MHz, making the chips suitable for NTSC and PAL video standards, as well as lower frequency still camera systems. The chips include resettable line delays to support sensors with a smaller number of photosites per line, and can be used with interlaced or progressive scan sensors.

8. SUMMARY

An operational digital camera has been developed using a high-performance image sensor incorporating lenslets and two full custom VLSI video processor chips. Photo 4 shows an black-and-white photograph from a color monitor display of an image from the digital CCD camera. Digital video processing offers higher image quality compared to analog approaches, and provides reliable, manufacturable, drift-free systems. The CMOS VLSI digital circuits offer real-time video operation while meeting the size, power, and cost constraints of one-chip cameras, and providing the flexibility needed for many different applications.

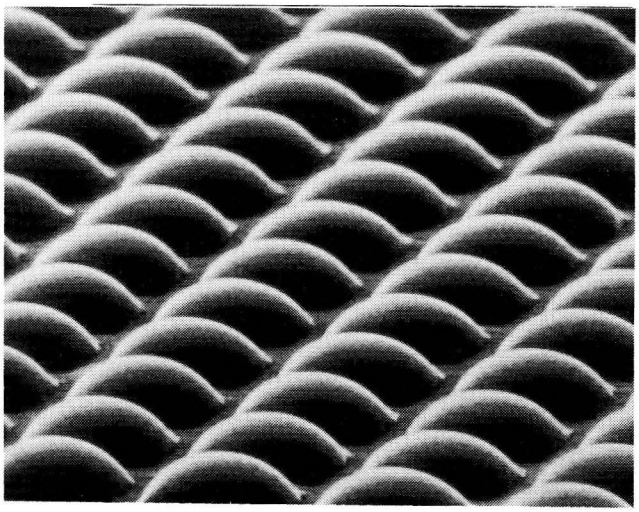


Photo 1 Lenslets

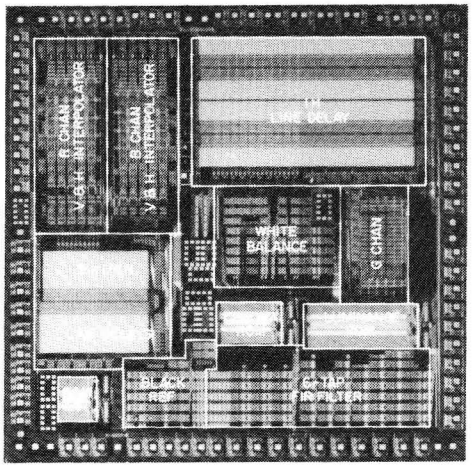


Photo 2 CFA Processor Layout

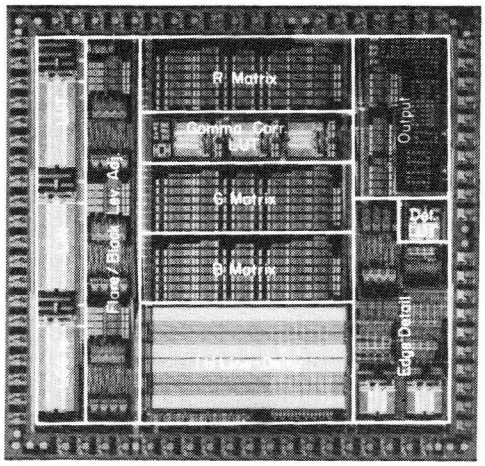


Photo 3 RGB Post-Processor Layout

Photo 4 Monitor Photo of Camera Output

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