

Unexamined Patent Application 2005-309874

(P2005-309874A)

(43) Publication Date: November 4, 2005 (2005.11.4)

(51) Int. Cl. ⁷		F1			Theme Code (Reference)	
G06F	17/50	G06F	17/50	658K	5B046	
		GO6F	17/50	658V		
Examination Request: Not yet requested No. of Claims 3 OL (Total 24 pages)						
(21) Application No.:	Japanese Patent Application No. 2004-127259 (P2004-127259)			(71) Applicant:	000004547 Niterra Co., Ltd. 14-18, Takatsuji-cho, Mizuho-ku, Nagoya, Aichi, Japan	
(22) Filing date	April 22, 2004 (2004.4.22)			(74) Agent:	100095751 SUGAWARA Masamichi, Patent Attorney	
				(72) Inventor	ONO Tomoshige 14-18, Takatsuji-cho, Mizuho-ku, Nagoya, Aichi, Japan c/o Niterra Co., Ltd.	
				(72) Inventor	OHNO Hiroshi 14-18, Takatsuji-cho, Mizuho-ku, Nagoya, Aichi, Japan c/o Niterra Co., Ltd.	
				F Term (Reference)	5B046 AA08 BA06	

(54) Title of Invention: CAD System For Electronic Circuit Boards, Computer Program Used In The System, And Method For Manufacturing Electronic Circuit Boards

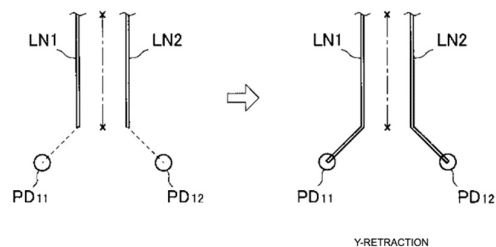
(57) Abstract

Problem: To provide a CAD system suitable for designing electronic circuit boards including differential wiring, a computer program for achieving functions of the CAD system on a computer, and a method for manufacturing electronic circuit boards based on CAD data designed by the CAD system for electronic circuit boards.

Solution: Wiring LN1 and LN2, which constitute differential wiring, have mutually different wiring nets. These wiring nets are pre-registered to a net group.

One set of wiring nets can belong to only one net group. Wirings LN1 and LN2 are generated simultaneously by entering a midpoint of both in a width direction on a drafting layer. When these wirings LN1 and LN2 approach the pad up to a preset distance, a retraction process to the pad or a drafting support process is performed.

Selected Drawing: FIG. 22



CAD SYSTEM FOR ELECTRONIC CIRCUIT BOARDS, COMPUTER PROGRAM USED IN THE SYSTEM, AND METHOD FOR MANUFACTURING ELECTRONIC CIRCUIT BOARDS

5 DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL FIELD

[0001] The present invention relates to a CAD system for electronic circuit
10 boards, a computer program used in the system, and a manufacturing method
for electronic circuit boards.

BACKGROUND ART

15 [0002] As semiconductor chips such as ICs and microprocessors are rapidly
becoming more integrated in recent years, the number of terminals in the
input/output section of chips is also increasing dramatically. In response,
electronic circuit boards for connecting these chips have also seen a rapid
increase in the number of wirings, and an increase in the number of multilayer
20 package boards with multilayer wirings built in using insulating layers such as
polymeric materials and ceramics. Recently, design systems using computer
drafting processes, so-called computer-aided design (CAD) systems have
been used to efficiently design these electronic circuit boards (Patent
Document 1). This is achieved by opening a drafting screen on a display device
25 and drafting board elements such as wiring, surface conductor patterns for
grounding or power, vias that connect different wiring layers together, or pads
and lands that form wiring terminal sections, as CAD data on the drafting layer
using a mouse or other input device to obtain a board design diagram.

30 [0003] Incidentally, it is well known that single-ended and differential signal
transmission methods are used in electronic circuits. TTL interfaces and
CMOS interfaces, which are widely used in general, are one-wire (single-end)

for transmitting signals on a single wire, except for ground. The single-end method conveys whether the signal is at level H or level L based on the potential difference between the ground level and the wiring. On the other hand, the differential method always uses two wirings for a single signal transmission. Unwanted radiation noise from the transmission line can be reduced by having each wiring transmit signals with the same amplitude and opposite phase.

Patent Document 1: Japanese Unexamined Patent Application Publication
2000-276505

Disclosure of the Invention

Problem to be Solved by the Invention

[0004] Even with a differential system, the actual wirings are separate, so each wiring will have a mutually different wiring net (also referred to simply as net) in the CAD data which is the design data of the electronic circuit board. Therefore, in order to generate differential wiring in a conventional CAD system for electronic circuit boards, first one net is specified and one wiring is drafted, followed by performing net switching input, and then the other wiring is drafted. In other words, it is necessary to perform drafting using the same procedure as for single-end wiring.

[0005] Furthermore, there is a problem of how to connect the wiring to the pad. In differential wiring, it is important to make the difference in length between the two wirings as small as possible so that the difference in signal arrival time is within the allowable range, while at the same time, to make the ratio of parallel portions of the wiring (parallel wiring unit) (parallel wiring ratio) as high as possible to reduce radiation noise. In other words, one key point is how to connect the wiring to the pads. In such cases, manual input operations are

very complicated, and this is one of the factors that hinders shortening of the design period for electronic circuit boards.

[0006] An object of the present invention is to provide a CAD system suitable
5 for designing electronic circuit boards including differential wiring, a computer program for achieving functions of the CAD system on a computer, and a method for manufacturing electronic circuit boards based on CAD data designed by the CAD system for electronic circuit boards.

10 Means to Solve The Problem And Effect Of The Invention

[0007] In order to resolve the aforementioned problem, the present invention provides a CAD system for electronic circuit boards for creating design data for an electronic circuit board to be manufactured, including: drafting layer
15 setting means for setting a plurality of drafting layers corresponding to a conductor layer and an insulation layer to be formed on the electronic circuit board; CAD data inputting means for inputting CAD data for specifying design dimensions, shapes, and placement positions of those board elements constituting the electronic circuit board which are predetermined to be drafting
20 target elements, on the drafting layer; wiring net registering means for performing attribute registration of a set of mutually different wiring nets that belong on a CAD data basis to a differential wiring constituted by a pair of wirings having mutually parallel portions to a database before the differential wiring is input to the drafting layer as the drafting target element; net group
25 registering means that groups together differential wiring nets that have been registered by the wiring net registering means, and performs attribute registration in a database as a net group; and retraction process executing means for performing a retraction process in order to individually connect the drafting target elements that express a via pad or a terminal pad (also referred
30 to simply as pad), so that the difference in the wiring length calculated with reference to the net group is within a predetermined range, with regard to a

pair of parallel wirings input onto the drafting layer as the drafting target elements that constitute the differential wiring.

[0008] With the present invention, a new attribute called net group is established for the differential wiring. In other words, an attribute of common net group is established for one set of the wiring constituting the differential wiring in order to provide a mutual association to the two wirings. On the other hand, as described above, there is a need to equalize the wiring length in differential wiring as much as possible. In this CAD system, the difference in wiring length (amount of wiring length deviation) is calculated based on reference to registered net groups. When drafting differential wiring, two wirings are drafted to be parallel partway, and both ends of each wiring are connected to a pad. Next, the process of retracting to the pad should be performed so that the amount of wiring length deviation is within a set range (preferably so that the wiring lengths are equal). This configuration prevents a large amount of wiring length deviation due to input errors, or the like, and thus enables accurate drafting of differential wiring. Therefore, this CAD system is expected to dramatically shorten the design period of electronic circuit boards.

[0009] In a suitable manner, the retraction process executing means can be configured to start the retraction process when the parallel portion of the differential wiring input to the drafting layer is extended to a position where the distance from the pad reaches a predetermined retraction start distance. In other words, the drafting program for the retraction process should be started when the parallel wirings are sufficiently close to the pad. In this manner, it is not necessary to input every single command or the like in order to execute the retraction process.

[0010] Furthermore, differential wiring generation means can be provided to simultaneously generate two wirings constituting a differential wiring on the drafting layer based on end points, and allocate a first wiring net specified by an input to one wiring of the aforementioned wirings and a second wiring net

belonging to the same net group as the first wiring net to a second wiring, if an instruction to perform drafting, on the drafting layer, of the differential wiring for which a net group has been registered by the net group registering means is provided and one of the wiring nets of the differential wiring is specified and the aforementioned pair of end points are input on the drafting layer. For example, a differential wiring drafting command is provided, and an input to execute this command activates the differential wiring generating means. The operator first specifies only one of the two wiring nets of the differential wiring. A pair of endpoints is then input. The differential wiring is then simultaneously drafted based on the endpoints. A first wiring of the two drafted wirings is provided with the wiring net specified by the operator, and a second wiring is automatically provided with the wiring net that forms a group with the wiring net specified by the operator, and these are written to the drawing database. This configuration allows the operator to accurately draft the differential wiring using simple input operations. Therefore, the design period is expected to be even further shortened.

[0011] Furthermore, the aforementioned differential wiring generating means can be configured to generate two parallel wirings on the drafting layer as a portion of the differential wiring, where the locus connecting the input pair of end points represents a set of midpoints in the width direction. In other words, two wirings are generated with left right symmetry across the locus connecting the pair of end points. For example, the endpoints (coordinates) of the two wirings can be specified by a process that offsets to the left or right a line segment connecting the input endpoints. This is very convenient because it eliminates the need to input the coordinates of the wirings separately.

[0012] On the other hand, the aforementioned retraction process may be a process of extending and connecting while diagonally converting the direction of the wiring constituting the differential wiring toward the pad, or extending and connecting while converting at a near right angle the direction of the wiring constituting the differential wiring toward the pad. These configurations

eliminate the need to consider the retraction form of the wiring each time the differential wiring is drafted, which contributes to increasing the speed of the retraction process.

5 [0013] Furthermore, the retraction process may include an automatic drafting process that automatically connects a first wiring of the two wirings that constitute the differential wiring to the pad of the same wiring net, and a drafting support process that supports drafting by manual input in order to connect a
10 second wiring to the pad of the same wiring net so that the amount of wiring length deviation in the differential wiring is within a preset range. In other words, the first wiring should be retracted by automatic drafting, leaving room for drafting by manual input of the second wiring. However, manual drafting may cause the amount of wiring length deviation to increase more than necessary, so it is recommended that support processing be performed during
15 manual drafting, such as issuing a warning or the like when drafting is performed in a manner that the amount of wiring length deviation deviates from the preset range.

[0014] In addition, a line width and line spacing registering means can also be
20 provided to register the line width of the differential wiring and the line spacing of the parallel portions prior to generation of the differential wiring. In this case, the differential wiring generating means can be configured to simultaneously generate the differential wiring by referring to the line width data and line spacing data registered by the line width and line spacing registering means.
25 Making the line width capable of being predetermined is convenient because the line width will not have to be determined for each simultaneous occurrence of the differential wiring. Furthermore, if the line spacing of the wiring can be predetermined, the line segment (locus) connecting the end points together can be captured as a shape by referring to the line spacing, and the process
30 of offsetting can be easily performed.

[0015] In one other suitable aspect, the following retraction process can be performed. In other words, for each wiring that constitutes the differential wiring, the difference in wiring length of the portion already drafted is calculated, the retraction reference position used as the reference position for
5 connecting each wiring to the pad is found and set at the position where the difference in the wiring length is zero, and the input cursor is retracted (automatically moved) to the set retraction reference position. Thereby the wiring length can very easily be made uniform without checking the wiring length on a graph or the like.

10

[0016] Furthermore, it is also possible to provide differential wiring checking means for finding a set of wirings that have been input to the drafting layer using CAD data inputting means and that constitute the differential wiring by referring to a net group and generating wiring length deviation information
15 related to the difference in length of the two wirings, and information outputting means for display output or print output of the wiring length deviation information generated by the differential wiring checking means. In this manner, the length of wiring belonging to the same net group can easily be individually read (calculated) and the differences in length can easily be
20 compared. This eliminates the need to individually check the wiring lengths when checking differential wiring lengths, and the like, and thus contributes to shortening the design period of electronic circuit boards.

[0017] Furthermore, the aforementioned differential wiring checking means
25 can be configured to calculate, as wiring length deviation information, the amount of wiring length deviation defined by the difference between the length of the longer wiring and the length of the shorter wiring, of the two wirings constituting the differential wiring, and to determine whether the calculated amount of wiring length deviation is within a preset allowable range. With this
30 configuration, a differential wiring with minimal signal skew (signal arrival time difference) can be easily drafted, shortening the design period, and improving the quality of the wiring board which is the product.

- [0018] Furthermore, the aforementioned differential pair wiring checking means may be configured to calculate the parallel wiring ratio, which is defined as the value obtained by dividing the wiring lengths of the parallel portions of the two wirings constituting the differential wiring by the total wiring length of each wiring, and to determine whether the calculated parallel wiring ratio is within the preset allowable range. With this configuration, the parallel wiring ratio of the differential wiring can be increased reliably and easily.
- 5
- [0019] Furthermore, the computer program of the present invention for solving the problem is primarily characterized by, when installed on a computer, causing the computer to function as each of the means constituting the aforementioned CAD system for electronic circuit boards.
- 10
- [0020] Furthermore, the method of manufacturing an electronic circuit board of the present invention in order to solve the problem is primarily characterized by including:
- 15
- a step of designing an electronic circuit board for creating design information of the electronic circuit board as a set of CAD data by inputting the drafting target elements required for the electronic circuit board to be obtained as CAD data on the drafting layer, using the CAD system for electronic circuit boards according to claim 1; and an electronic circuit board manufacturing step of creating CAM data based on the CAD data, controlling electric circuit manufacturing equipment based on the CAM data, and manufacturing the electronic circuit board.
- 20
- 25

Best Mode for Carrying Out the Invention

- [0021] An embodiment of the present invention will be described below while referencing the attached drawings.
- 30
- FIG. 2 is a block diagram depicting the overall configuration of an embodiment of a CAD/CAM system 100 for electronic circuit boards of the present invention

(hereinafter simply referred to as CAD/CAM system or CAD system). The CAD/CAM system 100 is equipped with a computer main body 112 including a CPU 103, ROM 104, RAM 105, input/output interface 102, and the like, to which are connected as peripheral equipment, input means such as a keyboard 106 or mouse 107, recording media reading means such as a CD-ROM drive 108 or flexible disk drive 109, and the like, hard disk drive (hereinafter referred to as HDD) 110, monitor 113 connected via a monitor control unit 111, printer 114, and the like. The CAD/CAM system 100 for electronic circuit boards is of course also simply the CAD system 100 for electronic circuit boards.

[0022] Note that the CPU 103 primarily includes drafting layer setting means, CAD data inputting means, CAM data converting means, wiring net registering means, net group registering means, differential wiring generating means, line width and line spacing registering means, differential wiring moving means, retraction process executing means, differential wiring checking means, CAM data outputting means, and the like. Furthermore, the keyboard 106 or mouse 107, together with the CPU 103, is the main CAD data inputting means. Furthermore, the input/output interface 102 functions as a drawing outputting means for print outputting the design drawing of the electronic circuit board after drafting is completed, as well as CAM data outputting means for outputting CAM data that has been converted and created based on CAD data by the CAM data converting means.

[0023] The HDD 110 contains an operating system program (hereinafter referred to as "OS") 61 and an application program (hereinafter referred to as "application") 62. The application 62 is a computer program for realizing the functions of the CAD/CAM system 100, and operates on the OS 61 with the application work memory 52 as the work region. The application is stored in a computer-readable form on, for example, a CD-ROM 120 or the like, and installed in a predetermined storage region on the HDD 110. Furthermore, the HDD 110 stores a data file (CAD data file) 63 of the drafted drawing and a

CAM data file 64 that has been converted and generated based on the CAD data file. On the other hand, work memory 51 for the OS 61 and work memory 52 for applications are both formed in the RAM 105.

5 [0024] FIG. 1 depicts a cross-sectional structure of an example of an electronic circuit board to which the CAD/CAM system 100 is applied (this electronic circuit board 1 is configured as an organic board, but the present invention is not limited to this, and can also be applied to ceramic boards). In other words, the electronic circuit board 1 has core conductor layers M1 and M11 formed in
10 a predetermined pattern on both surfaces of a board-shaped core material 2 made of a heat-resistant resin board (for example, bismaleimide-triazine resin board) and a fiber-reinforced resin board (for example, glass fiber reinforced epoxy resin). These core conductor layers M1 and M11 are formed as a surface conductor pattern covering most of the surface of the core material 2,
15 and are used as a power supply layer or ground layer. On the other hand, the core material 2 has through holes 12 drilled by drilling, or the like, and through-hole conductors 30 that provide mutual conduction between the core conductor layers M1 and M11 on the inner wall surface. Furthermore, the through-holes 12 are filled with a resin hole-filling material 31 such as epoxy
20 resin or the like.

[0025] Furthermore, the first via layers (insulating layer or build-up layer) V1 and V11, composed of photosensitive resin composition 6, are formed on the upper layer of the core conductor layers M1 and M11, respectively.
25 Furthermore, the first wiring conductor layers M2 and M12 with wiring units 7 are formed on a surface thereof by Cu plating. It should be noted that the core conductor layers M1 and M11 and the first wiring conductor layers M2 and M12 are interlayer connected by vias 34, respectively. Similarly, the second via layers (insulating layer or build-up layer) V2 and V12 are formed on the upper
30 layers of the second wiring conductor layers M2 and M12, respectively, using photosensitive resin composition 6. The second wiring conductor layers M3 and M13 are formed on the surface by Cu plating, respectively. The first wiring

conductor layers M2 and M12 and second wiring conductor layers M3 and M13 are also connected between layers by vias 34 respectively. As depicted in FIG. 7, the via 34 has a via conductor 34s provided in the via hole 34h and the inner circumferential surface thereof, a via pad 34p provided on the bottom surface side to cause conduction with the via conductor 34s, and a via land 34l protruding outward from the opening periphery of the via conductor 34h on the opposite side of the via pad 34p.

[0026] Next, returning to FIG. 1, a surface wiring conductor layer M3 is formed on the second via layer V2 on the first main surface side of the core material 2, where a plurality of solder lands 10 and a wiring unit 7 that conducts to a portion thereof are provided. These solder lands 10 are arranged in a square shape in the approximate center portion of the board by electroless Ni-P plating and Au plating, and together with the solder bumps 11 formed thereon, form the chip mounting part 40 (FIG. 4).

[0027] On the other hand, the back surface wiring conductor layer M13 is formed on the second via layer V12 on the second main surface side of the core material 2. The back surface wiring conductor layer M13 has a plurality of lands 17 for connecting the board 1 to a main board such as a motherboard in a well-known connection configuration, such as a ball grid array (BGA) or pin grid array (PGA) and the like. Furthermore, solder resist layers 8 and 18 (SR1, SR11) made of a photosensitive resin composition are formed on the front wiring conductor layer M3 and the back wiring conductor layer M13, respectively. The solder resist layer 8 on the front surface side has openings 8a corresponding one-to-one to the 10 solder lands in order to expose the 10 solder lands, and solder bumps 11 are provided inside the openings in a form that conducts with the 10 solder lands.

[0028] Herein, the via layers V1, V12, V2, V12, and the solder resist layers 8, 18 can be produced as follows. In other words, a photosensitive adhesive film made from a film of photosensitive resin composition varnish is laminated

(applied on), and a transparent mask (for example, a glass mask) with a pattern corresponding to the via holes 34h is superimposed and exposed. The film portions other than via holes 34h are cured by this exposure, while the via hole 34h portion remains uncured, so it is easy to form via holes 34h in the desired pattern by dissolving this portion in a solvent and removing (a so-called photovia process).

[0029] The operation of the CAD/CAM system 100 is described below in detail. When the application program 62 in FIG. 2 is started, the monitor 113 (FIG. 2) displays the drafting screen 40, as depicted in FIG. 4. The application program 62 in this embodiment is constructed as a draw-type graphics software similar to a known CAD system, and the drafting work proceeds by individually inputting the shapes of the board elements (hereinafter also called elements) of the electronic circuit board 1 as CAD data by operating a mouse 107 on the drafting screen 40. In the present embodiment, when the drafting screen 40 of a new drawing is launched, the drafting screen 40 displays a four-sided reference area 51 corresponding to the main surface outline lines of the board to be designed and drafted based on the display data separately stored in the HDD 110, and the like, and shapes of board elements generally formed on the board surface (in this embodiment, pads 53 and 55) are displayed as default element shapes. In this case, it is convenient if a default element data storage unit is provided in the HDD 10, for example, to associate and store default element data by part number, and if the corresponding default element data can be read out and displayed on the drafting screen by inputting the part number using the keyboard 106 (or soft button clicking on the screen with the mouse 107), in order to immediately draft and input shapes such as standard formed board elements like the wiring unit 54 or the like.

[0030] Here, the board to be designed is a package board or the like, in which a plurality of wiring layers are stacked through an insulating layer. Furthermore, a plurality of drafting layers corresponding to the wiring layers to be formed are set on the drafting screen 40. These drafting layers (hereafter simply referred

to as layers) are visually indistinguishable in FIG. 4 due to overlapping. Furthermore, although the shapes drawn on each layer are overlaid on the drafting screen 40, it is possible to display only the shapes on a specific layer, or to display the shapes differently from those on other layers by changing the color, brightness, shading, fill pattern, and the like.

[0031] FIG. 12 is a flowchart depicting the flow of the drafting process. First, in S1, a layer is selected on which the element is to be drawn. This layer selection can be performed, for example, by using the mouse 107 (FIG. 2) to click on a soft button (not depicted) for layer selection displayed on the screen. Furthermore, the shapes that can be input include the aforementioned elements and via shapes for connecting elements between different layers, and in S2 and S8, a command input determines which of the above elements and vias are to be selected. This command input can also be performed by mouse clicking on a soft button (not depicted) that selects the element input or via input.

[0032] Once the element input is selected, the process proceeds from S2 to S3 to perform element drawing. During element drawing, different drawing tools are provided for each type of element to be drawn, such as wiring drawing, pad and land drawing, or surface conductor pattern drawing, similar to known CAD system software. Drawing tools can also be selected by mouse clicking on the drawing tool selecting button (not depicted), which is formed as a soft button on the screen. Once the desired drawing tool is selected, as depicted in FIG. 4, the elements are drawn by moving the pointer P, which indicates the drafting position, using the mouse, while combining mouse clicking, dragging (moving the mouse while holding down the mouse button) and the like. In FIG. 4, the shape of the wiring unit connecting each pad 53 and 55 is depicted as an element that has been completely drawn.

[0033] As depicted in FIG. 6, each time an element is finished drawing, the shape data which is the element description data, is stored in the drawing data

memory 52g in FIG. 2 in a form that corresponds to the element specific data (for example, element code) and layer specific data (for example, layer number). As depicted in FIG. 5, for example, the element description data is displayed as a set of vector data, function formula data, or dimensional specific data including coordinates of a specific reference point as well as radius and length, in order to define the shape, size, and drawing position of the elements OB11, OB12, OB13, OB14, and the like on a coordinate plane set on the screen 40 (FIG. 4). For example, element OB11 is expressed as a data set of coordinates of the end points of vectors A11(x1, y1), A11(x2, y2), A11(x3, y3), and A11(x0, y0) in that order, while circumventing around the reference point A11(x0, y0) in the specified direction (for example, clockwise). The same is true for element OB12. Furthermore, the circular element OB13, which represents a pad, land, or the like, is expressed as a data pair including the center coordinate C13 and the radius r13. Furthermore, for example, element OB14, which is a shape of a wiring unit of constant width W, can be expressed as a data set including coordinates of the starting point position B14 (x0, y0), end point position B14 (x1, y1), and the line width W14. Note that in FIG. 5, all four elements OB11, OB12, OB13, and OB14 are drawn on the same layer (M1).

20 [0034] On the other hand, if a via input is selected in Fig. 12, the process proceeds to S9 for via input processing. As depicted in FIG. 7, a via V connects different wiring layers, and in the present embodiment, the input of the via V shape is performed in units of via layers, and a via spanning a plurality of via layers is input in the form of a stacked via, in which a plurality of vias are stacked. Therefore, one via unit can be entered by specifying the via layer in which the via should be input. When three or more via layers are provided and a via spanning three or more via layers is to be input, the via in the middle layer may be automatically generated by specifying the via start layer and the via end layer. Furthermore, the data of this via shape (which is also one of the board elements) is then stored in the drawing data memory 52g as a set of the via position data and the layer identification information (via formation layer

VLY# #) corresponding to the via layer, as depicted in FIG. 8, in a form corresponding to the via identification data (for example, via code).

[0035] Returning to FIG. 12, when the element is drawn, the process proceeds to S4 to determine if there is an inputted element OB11 that partially overlaps (or in other words, is connected to) that inputted element OB12 in the same layer, as depicted in FIG. 9. If No, the process proceeds to S5 to determine if there is connection to another element OB31 by interlayer connection through the via VA11 as depicted in FIG. 10. If this response is also No, the process proceeds to S6 and the element OB12 is registered as a wiring net shape, for example, by writing only the element specific information into the wiring net data registration memory 52i (FIG. 3) in the drawing data memory 52g as new net data with the net specific information (for example, net number) added, which is then registered.

[0036] Furthermore, if the response to S4 or S5 in FIG. 12 is Yes, the element is incorporated into the registered wiring net shape to which the element to be connected belongs, or in other words, the element identification data of the newly drawn element is added to the corresponding net data in the wiring net data registration memory 52i (S4 to S7). Furthermore, in the case of connection by via, the via specific data is also added to the net specific information (S5→S7). Therefore, as depicted in FIG. 3, the wiring net data registration memory 52i stores net data associated with each of the net specific information net1, net2, ... and the specific data OB11, OB12, ... or the via specific data VA11, VA12, ... of the element belonging to that wiring net.

[0037] On the other hand, as depicted in FIG. 11, when overlapping elements occur between different layers, the element specific data are not added to the net data of the overlapping target. However, if wiring net shapes that are connected to each other by newly input via shapes are generated in S10 of FIG. 12, the process proceeds to S11, where the net data of those wiring net shapes are integrated (merged) together and re-registered as net data of a

single wiring net shape. In this case, the net specific information may be left corresponding to one of the wiring net shapes before integration and the other may be deleted and treated as a missing number, or both sets of net specific information may be deleted and new net specific information may be assigned.

5

[0038] If the drafting work is finished after repeating the above drafting input of element and via inputs, the process proceeds from S12 to S13 where a file name is assigned to the shape data stored in the drawing data memory 52g, or in other words, the drawing data and the net data in the wiring net data registration memory 52i, and then written and stored in the drawing data file 63 in HDD 110 (FIG. 2).

[0039] The CAD data for each element (drafting target element) created as described above is converted to CAM data. CAM data is shape data that specifies the dimensions, shape, and placement position for manufacturing the element to be manufactured, which includes the element or an additional element formed on the electronic circuit board 1 in a form associated with the element (for example, solder bumps formed on the solder lands that form the element), or specifies the dimensions, shape, and placement position of a portion corresponding to the element to be manufactured of a jig used for manufacturing the element (for example, a mask for exposing a via pattern or wiring pattern, a mask for applying solder paste used to form solder bumps, and the like).

[0040] Incidentally, the example in FIG. 4 depicts single-end wiring in which signals are transmitted over one wiring, but differential wiring in which signals are transmitted over two wirings is often concomitantly used on the same circuit board 1 (depending on the IC to be mounted). With differential wiring, it is important to make the difference in wiring length as small as possible so that the difference in signal arrival time does not increase, and to make the ratio (parallel wiring ratio) of parallel portions (parallel wiring) of the wiring to be as high as possible to reduce unwanted radiation noise. However, the two wirings

that make up the differential wiring have mutually different wiring nets. Therefore, a conventional CAD system configuration drafts the wirings separately for differential wirings as well as for single-end wirings. In contrast, with the CAD system 100 of the present invention, the differential wirings can
5 be generated simultaneously on the drafting layer using a single input, without frequently switching the wiring nets. The details are described below.

[0041] First, in layer M1 for which the elements that make up the conductor layer of the electronic circuit board 1 are described, one set of wirings LN1 and
10 LN2 which constitute a differential wiring, are arranged as depicted in FIG. 13. One wiring LN1 which constitutes the differential wiring is connected to the pads PD₁₀ and PD₁₁ for connections with ICs and relay boards or for interlayer connections. Similarly, the other wiring LN2 is connected to pads PD₂₀ and PD₁₂. These wirings LN1 and LN2 may be configured with a plurality of
15 elements or a single element. Furthermore, the wirings LN1 and LN2 have mutually parallel portions (parallel wiring) and a portion retracted to the pad (retracted wiring).

[0042] Elements representing wiring LN1 and elements representing wiring
20 LN2 are stored in the drawing data memory 528 (drawing database) having a form that includes attribute data such as element specific data, layer specific data, and element description data, and the like, as described in FIG. 6. Furthermore, the wiring nets of wirings LN1 and LN2, which constitute differential wiring, are registered as net specific information in the wiring net
25 data registration memory 52i, as described in FIG. 3. Each wiring net data (net1, net2...) depicted in FIG. 3 is to be registered in advance before the elements are described. In other words, the wiring nets assigned to elements that are successively described can be registered in advance (CPU 103: wiring net registering means). In describing the differential wiring, one set of wiring
30 nets that are mutually different is registered.

[0043] Herein, with this CAD system 100, of the wiring nets registered as net specific information in the wiring net data registration memory 52i as depicted in FIG. 3, the wiring nets of the differential wiring are grouped, and as depicted in FIG. 14, the attribute data referred to as the net group is registered in the net group data registration memory 52k (CPU 103: net group registering means). By referring to the registered net groups, it is possible to specify one set of wiring nets of the differential wiring. In other words, by specifying a first wiring net of the differential wiring, it is possible to find a second wiring net that belongs to the same net group as the first wiring net. This is because only one set of wiring nets can belong to one net group, and the wiring pair that constitutes the differential wiring always has unique net groups. By registering the net group attributes in advance, the differential wiring drafting process can proceed as follows.

[0044] For example, a case is considered where wiring LN1 and wiring LN2, which constitute a differential pair as depicted in FIG. 13, are drafted on layer M1. Wiring LN1 and wiring LN2 which constitute the differential wiring have different wiring nets net11 and net12, respectively. Prior to drafting the differential wiring, wiring nets net11 and net12 are registered in the wiring net data registration memory 52i depicted in FIG. 3, and furthermore, the net group NT₁ of the wiring nets net11 and net12 should be registered in the net group data registration memory 52k depicted in FIG. 14. In addition, the pads (via pads and terminal pads) are connected to both ends of the differential wiring, for example. Therefore, it is sufficient to input and set the placement position or planned placement position of the pads connected to the differential wiring in advance on the drafting layer, and register the element attributes of these pads and the like in the drawing data memory 52g (see FIG. 6) and the wiring net data registration memory 52i (see FIG. 3).

[0045] Next, a program for generating differential wiring on the drafting layer (differential wiring drafting process) is first initiated by inputting commands when drafting the differential wiring. FIG. 15 depicts a flowchart depicting a

drafting process using the program. When the drafting program is initiated, the first pad pair PD₁₀, PD₁₁ and the second pad pair PD₂₀, PD₁₂, to be connected by the differential wiring, and the temporary connection lines, indicating that the pad pairs are not yet connected, are first displayed on the drafting layer,
5 as depicted in the upper figure in FIG. 16. The first pad pair PD₁₀, PD₁₁, which are connected by this temporary connection line, are elements having the same wiring net. Similarly, the second pad pair PD₂₀, PD₁₂ are elements with the same wiring net.

10 [0046] Next, one wiring net of the differential wiring net is specified by clicking on one of the pairs of the temporary connection lines displayed on the drafting layer. The wiring nets specified here are temporarily stored in RAM 105 or the like (ST1 in FIG. 15). Next, a determination is made as to whether one pair of endpoints (final end points) has been input on the drafting layer (ST2). In the
15 differential wiring drafting process in the CAD system 100 of the present invention, as depicted in the middle figure of FIG. 16, two wirings (elements) constituting the differential wiring are simultaneously generated at symmetrical points 40 on the left and right of a line segment (locus) connecting a pair of input end points (ST4). Specifically, two parallel wirings having a locus
20 connecting the input endpoints representing a collection of midpoints in the width direction are generated on the drafting layer as parallel portions of the differential wiring. However, if it is determined in ST3 that the drafted wiring extends within the retraction range to the pad, two mutually parallel wirings will be simultaneously drafted while executing the retraction process in ST5 (refer
25 to the lower figure in FIG. 16). The retraction process is used to connect the differential wiring to the pad (details are described below).

[0047] Furthermore, in the present embodiment, as depicted in FIG. 17, the wiring widths of each of the wirings LN1, LN2 which constitute the differential
30 wiring, are set in advance prior to drafting the differential wiring. Furthermore, during the differential wiring drafting process, each element is drafted at the set wiring width, and the wiring width can be stored in the drawing data memory

52g as element description data. Furthermore, the line spacing (clearance) of the parallel portions of the wirings LN1, LN2 can be set in advance before drafting the differential wiring (CPU103: line width and line spacing registering means). Furthermore, when the differential wirings are simultaneously generated, elements (wirings) are placed on the left and right of the locus connecting the two end points that are input, with reference to the set line spacing data. Note that the set wiring width and line spacing may be temporarily stored in RAM, such as the drawing data memory 52g, or may be rewritable and stored in a setting file or the like associated with the differential wiring drafting program.

[0048] After simultaneous generation of differential wiring on the drafting layer, one wiring LN1 of the wirings that constitute the differential wiring is assigned a specific wiring net in advance. Furthermore, the other wiring net belonging to the same net group as the wiring net is automatically assigned to the other wiring LN2. In other words, wiring nets belonging to the same group as the first wiring net input and specified in advance by the operator are found by referring to (searching) the database (net group registration data memory 52k: see FIG. 13), and these wiring nets are automatically assigned to each pair of wirings LN1 and LN2 described in the drafting layer (ST6, ST7). Specifically, the element specific data of the newly drawn wiring is added as differential wiring to the corresponding net data in the wiring net data registration memory 52i.

[0049] As described above, differential wiring is input by inputting a locus on the drafting layer that passes exactly midway between the two wirings LN1 and LN2 that constitute the differential wiring. On the other hand, as depicted in FIG. 16, the differential wiring is connected between pads while changing the orientation at an angle of, for example, 45° . In such a case, the following procedure can be adopted, for example, in order to generate the wirings LN1 and LN2 as differential wirings with the input endpoints (coordinate points) as the midpoint in the width direction.

[0050] One method, as depicted in the conceptual diagram in FIG. 18, basically generates parallel wirings (elements) on the left and right sides of the locus connecting the input coordinate points together. As described above, a preset value is referenced for the wiring spacing (clearance) at this time. Furthermore, if a coordinate point (represented by input point 3 in FIG. 18) is input at a position where a corner must be formed, the same procedure as above is used to generate elements on the left and right sides of the locus connecting the coordinate points, and to perform extension and shortening processes to connect the parallel wirings that form one corner without excess or deficiency. Thereby, the wirings LN1 and LN2, which constitute the differential wiring, are generated.

[0051] One other method, as depicted in the conceptual diagram in FIG. 19, is to take the line segment connecting the input coordinate points as the locus between differential wirings, capture this locus as a shape, and offset the shape to the left and right. If the locus is offset while adjusting the line length according to the angle θ formed by the locus connecting each input point, the X-Y coordinates for specifying the wirings LN1 and LN2 can be obtained. With this procedure, as depicted in FIG. 20, the parallel wiring specified by line width D_2 , clearance D_1 , and coordinate points P_{11} to P_{15} and P_{21} to P_{25} is drafted without interruption.

[0052] Returning to FIG. 15, a determination is made in ST8 as to whether the connecting process (retraction process) between the pads and the wiring that constitutes the differential wiring has been completed in ST5. If the retraction process has not been completed, the process proceeds to ST2 and enters a standby state until the end points are input to extend the wiring to the positions necessary to connect to the pads. On the other hand, the retraction process being complete means that the differential wiring input is complete, so the drawing data stored in the drawing data memory 52g is saved in the drawing data file 63 and the process ends (ST9).

[0053] The drafting process is performed as described above, and a set of wirings LN1, LN2 constituting the differential wiring is input on the drafting layer and written to the drawing data memory 52g (see FIG. 6). This eliminates the need to input elements while frequently switching the wiring nets, allowing the operator to quickly draft the differential wiring.

[0054] Next, the process of moving the differential wiring on the drafting layer after drafting has been completed will be described. For example, if an error occurs during design rule checking or the like, one of the differential wirings may be the cause of the error in design rule checking. However, moving only one wiring of the differential wiring is inconceivable based on the design. In particular, the parallel portions (parallel wiring) must always be moved in pairs. In this case, the CAD system 100 is preferably configured so that the parallel portion of one wiring LN1 moves simultaneously in response to moving the parallel portion of the other wiring LN2, because this eliminates mistakes such as moving only one wiring and forgetting to operate the other wiring, or forgetting to perform the wiring length adjustment.

[0055] As described above, the wirings LN1 and LN2, which constitute the differential wiring, have mutually different wiring nets. Therefore, some form of association must be made between one wiring LN1 and the other wiring LN2 in the drawing data. With this CAD system 100, each individual differential wiring has a unique attribute called a net group. Therefore, when a move instruction for the first wiring LN1 is input, the second wiring LN2 is identified by referring to the net group, and a process is executed to move the second wiring at the same time as the first wiring LN1 for which the move instruction was provided.

[0056] Specifically, the above move process can be performed by the following steps. First, when an instruction to move the differential wiring is input and one of the wirings to be moved is specified, the other wiring is specified by referring to the net group based on the wiring net of the specified wiring. Next, a process

is executed to move the shape (wiring) in a form where the first wiring LN1 pushes away the second wiring LN2, as depicted in FIG. 21, in response to an input to move the wiring using a command line or by an operation of dragging or the like using the mouse. In this CAD system 100, the parallel portions of the two wirings LN1 and LN2, which constitute the differential wiring, are programmed to move in the orthogonal direction. In other words, when moving one of the wirings, the other wiring is identified by referring to the net group and is moved in the same direction and over the same distance (CPU 103: differential wiring moving means).

10

[0057] Furthermore, the wirings LN1 and LN2 maintain their pad-to-pad connection before and after their respective movements. In other words, as depicted in FIG. 21, the X-Y coordinates of the element (element description data) in the drawing data memory 52g are rewritten so that the coordinates are not interrupted as shapes. Furthermore, the change in wiring length between the first wiring LN1 and the second wiring LN2 must be equal before and after such a move. In other words, as depicted in FIG. 21, the two points P_{12} and P_{13} for describing the wiring LN1 are moved to the two points P'_{12} and P'_{13} , and the two points P_{22} and P_{23} for describing wiring LN2 are moved to the two points P'_{22} and P'_{23} . The movement is processed so that the amount of change in the wiring length specified between the two points (element specific data) is equal. The coordinate data (element description data) of the element is rewritten in the drawing data memory 52g in response to the movement process. Note that the simultaneous movement may be limited to the parallel portions of the two wirings LN1 and LN2.

[0058] In the above description, it was assumed that the grouping of the wiring nets is registered before the differential wiring is drafted. However, for a pair of wirings input on the drafting layer as separate wirings with different wiring nets, it is possible to designate the wirings as differential wiring and register a net group that groups the wiring nets of each wiring. Thereby the wiring drafting process can be performed sequentially one by one as in the single-end case,

30

or the process for movement can be performed simultaneously as differential wiring registered as a group.

[0059] Next, the differential wiring retraction process is described. As described above, the retraction process is a process of connecting both ends of a pair of parallel wirings LN1 and LN2, which are input on the drafting layer as elements constituting the differential wiring, to elements PD₁₁ and PD₁₂ representing the pads individually (CPU 105: retraction process executing means). As depicted in FIG. 22, the first wiring LN1 and the second wiring LN2, which constitute the differential wiring, are first drafted close to the pads PD₁₁ and PD₁₂ (at a predetermined distance from the pads) in a form that maintains parallelism. Drafting is in response to the input of the midpoint in the width direction between the wirings LN1 and LN2, as described above.

[0060] As described in ST3 of the flowchart in FIG. 15, when a determination is made that the drafted wirings LN1 and LN2 are located within the retraction range to the pads PD₁₁ and PD₁₂, the retraction process of ST5 in the flowchart is performed. In this embodiment, the retraction process starts when the parallel portions of the wirings LN1 and LN2 are extended to the position where the distance from the pads PD₁₁ and PD₁₂ reaches the predetermined retraction start region. By matching the center coordinates of pads PD₁₁ and PD₁₂ on the drafting layer with the end points of wirings LN1 and LN2, connections are made between the wirings LN1 and LN2 and the pads PD₁₁ and PD₁₂. Note that the retraction process may be started when at least one of the first wiring LN1 and the second wiring LN2 reaches the predetermined retraction start region TA (trigger area). The related details are described below.

[0061] Several connection configurations between the wiring and the pads can be exemplified for the above retraction process. For example, the example depicted in FIG. 22 depicts a Y-shaped retraction in which the direction of wiring LN1 and LN2 is extended and connected while converting diagonally

toward the pads PD₁₁ and PD₁₂, respectively. This Y-shaped retraction can be suitably employed in situations where the approaching direction of each wiring LN1, LN2 is perpendicular to the line segment connecting the centers of the pad pair (including pad PD₁₁ and pad PD₁₂) to which the differential wiring should connect. For example, assume A to be a vector parallel to the line segment connecting the centers of the pad pair. Assume B to be a vector parallel to the wiring direction at the end of which ever of wiring LN1 and wiring LN2 is closer to the pad pair. By calculating the inner product ($A \cdot B$), it is possible to determine whether the approaching direction of the wirings LN1 and LN2 is perpendicular to the line segment connecting the centers of the pad pairs. If the inner product is zero, both vectors are perpendicular to each other. If they are not perpendicular, the Y-retraction process described above should be started after the automatic wiring process that changes the orientation of the differential wiring to become perpendicular.

15 [0062] Furthermore, the example depicted in FIG. 24 depicts a T-shaped retraction, in which the two wirings LN1 and LN2 are extended and connected while converting their directions at right angles toward pads PD₁₁ and PD₁₂, respectively. Similar to the Y-shaped retraction, the present embodiment can be suitably employed in a situation where the direction of approach of each wiring LN1, LN2 is perpendicular to the line segment connecting the centers of the pad pair. In other words, wiring LN1 and LN2 remain parallel and are extended until intersecting the line segment connecting the centers of the pad pairs, and from there they change direction toward each pad. However, if there is a design rule that the inner angle of the wirings LN1 and LN2 that make up the corner must be, for example, 135 degrees (this is recommended for the differential wiring to prevent an increase in impedance mismatch), as depicted in FIG. 24, the automatic drafting process is preferably performed for the T-shape retraction, and then the corner of the line segment connecting the centers of the pad pairs is cut (shortened). The wiring length of the portion to be cut may, for example, be determined based on preset parameters, or may

be set in the form of n times (n : a natural number) the wiring width of the wirings LN1 and LN2.

[0063] Furthermore, as depicted in FIG. 25, the region of radius R from the center coordinates of the pads PD_{11} and PD_{12} , which are to be connected to the differential wiring, can be defined as the retraction start region TA (trigger area). The parallel portions of the wirings LN1 and LN2 are simultaneously drafted based on the input of the midpoints in the width direction as described above until the wirings reach the retraction start region TA, while the retraction process can be configured to start when wirings LN1 and LN2 are reached in the retraction start area TA by drafting. Specifically, as depicted in FIG. 25, after performing the drafting process to connect the first wiring LN1 to the corresponding pad PD_{11} , the drafting process can be performed to connect the second wiring LN2 to the pad PD_{12} . Ideally, the differential wiring should have no amount of wiring length deviation (wiring length difference), or in other words, should be equal-length wiring. Therefore, after executing the automatic drafting process for connecting the first wiring LN1 to the pad PD_{11} , the automatic drafting process for connecting the second wiring LN2 to the pad PD_{12} should be performed so that the wiring length of wiring LN1 is equal to that of the wiring LN2. However, because of space and design rule issues, automatic drafting may be performed so that the amount of wiring length deviation falls within a predetermined range.

[0064] Furthermore, the following methods can also be suitably employed for the retraction process to ensure equal wiring lengths. First, as depicted in the upper diagram in FIG. 26, a parallel portion of the differential wiring is drafted based on input midpoints in the width direction (such as D_0 or the like in the diagram). This point has already been described. Next, for each wiring LN1 and LN2, the wiring length of the portion already drafted is calculated based on the XY attribute data (element description data in FIG. 6). Next, the difference in wiring lengths up to the already calculated portion can be determined.

[0065] Next, as depicted in the middle figure in FIG. 26, the retraction reference position used as the reference position for retracting each wiring into the pad is determined and set at the position where the difference in the above wiring lengths is zero. The present embodiment depicts a design in which the parallel portions of the differential wiring approach perpendicular to the line segment connecting the center coordinates of a pair of pads, and a T-shape retraction is performed. Therefore, the aforementioned retraction reference position FP_0 can be found on the line segment connecting the pads. Therefore, the input cursor is retracted into the identified retraction reference position. As depicted in the lower diagram in FIG. 26, drafting is performed to connect wiring LN1 to pad PD₁₁ and wiring LN2 to pad PD₁₂, thereby completing the retraction process.

[0066] In the upper diagram in FIG. 26, when the line segment passing through the midpoint (for example, D_0) in the width direction of wirings LN1 and LN2 that form the differential wiring being drafted is extended straight, it can be hypothesized that the intersection of the line segment connecting the pads and the extended line is not the retraction reference position to achieve equal wiring lengths. In this case, when the line segment passing through the midpoint in the width direction of the wirings LN1 and LN2 to be retracted is extended straight, the wirings LN1 and LN2 are moved parallel to the width direction so that the retracted reference position FP_0 is on the extended line, as depicted in the middle and lower diagrams in FIG. 26. As depicted in FIG. 27, the parallel shift process is performed without any change in the difference in wiring length by creating new width direction midpoints D_0' , D_1 , and D_2 .

[0067] Furthermore, as depicted in FIG. 28, the line segment passing through the midpoint in the width direction of wirings LN1 and LN2 extends straight, and the intersection between the extended line and the line segment connecting the pads is set as the tentative retraction reference position FP. The wiring length of the wiring LN1 and the wiring length of the wiring LN2 are

determined for the case where T-shaped retraction is performed based on the retraction reference position FP, and the following processes (a) to (c) can be performed to make the difference in wiring length zero.

(a) If "length of wiring LN1" > "length of wiring LN2", move the retraction
5 reference position FP closer toward the wiring LN1.

(b) If "length of wiring LN1" < "length of wiring LN2", move the retraction reference position FP closer toward the wiring LN2.

(c) If "length of wiring LN1" = "length of wiring LN2", maintain that retraction reference position.

10 When performing processes (a) and (b) above, the parallel shift process of the wirings LN1 and LN2 depicted in FIG. 27 is also performed. The allowable range of movement of the retraction reference position FP should be limited to a section WL narrower than the width of the pads PD₁₁ and PD₁₂.

15 [0068] If the aforementioned retraction reference processes are performed to ensure equal wiring lengths, the need to check the wiring lengths on a graph or the like can be eliminated, significantly reducing the time required for drafting. In addition, since wiring boards are manufactured based on CAD data that reliably guarantees equal wiring lengths, the quality of the wiring boards
20 themselves can be improved.

[0069] However, automatic drafting as described above is not mandatory, and support processing may be performed to facilitate equal-length drafting of the differential wiring. In other words, drafting to connect the differential wiring to
25 the pad itself can be performed based on the input of the operator, and at this time, the support process for equal-length wiring can be performed so that the operator can specify the amount of wiring length deviation (display output to a monitor). For example, as depicted in FIG. 29, the connection to the pad PD₁₁ is automatically drafted for the first wiring LN1 of the wirings LN1 and LN2,
30 while the second wiring LN2 is drafted by manual input. At this time, the ratio of the length of wiring LN2 not connected to the pad PD₁₂ to the length of wiring LN1 connected to the pad PD₁₁ can be expressed by an equal wiring length

indicator or as a percentage. Furthermore, the pattern or color of the wiring length indicator displayed on the monitor, or a combination of the two, may be used to inform the operator that the amount of wiring length deviation has deviated from an acceptable value. In this manner, the operator can easily perform drafting by manual input.

[0070] As described above, a configuration is possible where the retraction process may include an automatic drafting process that automatically connects a first wiring of the two wirings that constitute the differential wiring to the pad of the same wiring net, and where a drafting support process that supports drafting by manual input in order to connect a second wiring to the pad of the same wiring net so that the difference in wiring length in the differential wiring is within a preset range. Note that, basically, the retraction process may be manual input including the aforementioned support process, or only the Y-retraction and T-retraction depicted in FIG. 22 and FIG. 23 may be executed by command input.

[0071] Incidentally, when connecting the wiring LN1 and LN2 to the pads, care should be taken to prevent the amount of wiring length deviation from becoming large, as described above. Since the allowable amount of wiring length deviation depends on the frequency of the signal and the like, it is recommended that the amount be set in advance before the differential wiring is drafted. The amount of wiring length deviation is defined by the difference between the length of the longer wiring and the length of the shorter wiring of the two wirings that constitute the differential wiring. In other words, in order to determine the length of the two wirings that constitute the differential wiring, it is necessary to be able to recognize which wirings are differential to each other. In this CAD system 100, two wirings LN1 and LN2 that constitute the differential wiring can be specified by referring to the net group as described above, and the lengths of these wirings LN1 and LN2 are obtained from the element description data (X-Y attribute S). Therefore, the aforementioned amount of wiring length deviation can be easily obtained.

[0072] Furthermore, the wiring length deviation rate can be calculated by comparing the wiring lengths of both wirings LN1 and LN2 and dividing the smaller value by the larger value, which can then be displayed on a monitor or the like. Furthermore, the calculated amount of wiring length deviation and the wiring length deviation rate can be stored in the drawing database (drawing data memory) as attribute data that the two wirings constituting the differential wiring have in common in a manner similar to net groups. Furthermore, a determination is made as to whether the calculated amount of wiring length deviation and the wiring length deviation rate are within the preset tolerance range and a warning (error indication) can be displayed on the drafting layer, for example, as depicted in FIG. 30(a).

[0073] Furthermore, a configuration is possible where the parallel wiring ratio is calculated, defined as the value obtained by dividing the wiring lengths of the parallel portions of the two wirings LN1, LN2 constituting the differential wiring by the total wiring length of the longest wiring, and then a determination is made as to whether the calculated parallel wiring ratio is within the preset allowable range. Furthermore, as in the case of the wiring length deviation rate, a warning may be displayed (see FIG. 30(b)). If a warning is issued along with the wiring length deviation rate, time and effort can be saved when making drafting corrections. If the wiring length deviation rate or parallel wiring rate deviates from the preset tolerance range, the drafting may be corrected manually or automatically. The above "total wiring length" can be considered in two cases: (1) the entire wiring belonging to the same net, and (2) the entire wiring connecting between the pads.

[0074] There are two methods for configuring differential wiring: the so-called edge-coupled structure and the broadside-coupled structure. An edge-coupled structure, in which the wirings are arranged parallel to each other in a plane, has a great advantage that it is relatively easy to ensure wiring symmetry, and

this has become mainstream. All differential wiring in this specification refers to edge-coupled wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

5

[0075] FIG. 1 is a cross-sectional view depicting an example of an electronic circuit board.

FIG. 2 is a block diagram depicting an electrical configuration of a CAD system for electronic circuit boards of the present invention.

10 FIG. 3 is a map depicting contents of a wiring net data registration memory.

FIG. 4 is an explanatory diagram of the operation process on a drafting screen in the CAD system for electronic circuit boards of the present invention.

FIG 5 is a conceptual diagram of an element.

FIG. 6 is a conceptual diagram of CAD data for an element.

15 FIG. 7 is a conceptual diagram of a via.

FIG. 8 is a conceptual diagram of CAD data for the via shape.

FIG. 9 is a first explanatory diagram of an overlapping connection state of an element.

20 FIG. 10 is a second explanatory diagram of the overlapping connection of an element.

FIG. 11 is a explanatory diagram of a via connection state of an element.

FIG. 12 is a flowchart depicting the flow of a drafting process.

FIG. 13 is a conceptual diagram of differential wiring.

FIG. 14 is a conceptual diagram of the net group data registration memory.

25 FIG. 15 is a flowchart depicting the differential wiring drafting process.

FIG. 16 is a conceptual diagram depicting the differential wiring generating process.

FIG. 17 is a conceptual diagram of a form for registering differential wiring line width and clearance settings.

30 FIG. 18 is a conceptual diagram for describing the detailed differential wiring generating process.

FIG. 19 is a continuation of FIG. 18.

- FIG. 20 is a partial enlarged conceptual diagram of the differential wiring.
- FIG. 21 is a conceptual diagram for describing a process for moving differential wiring.
- FIG. 22 is a conceptual diagram of Y-retraction.
- 5 FIG. 23 is a conceptual diagram of T-retraction.
- FIG. 24 is a continuation of FIG. 23.
- FIG. 25 is a conceptual diagram depicting an example of setting a retraction start region.
- FIG. 26 is a conceptual diagram for describing the equal wiring length
- 10 retraction process.
- FIG. 27 is a conceptual diagram depicting the parallel shift of wiring that accompanies the retraction process.
- FIG. 28 is, similarly, a conceptual diagram describing the equal wiring length retraction process.
- 15 FIG. 29 is a diagram depicting an example of the support process.
- FIG. 30 is a diagram depicting the differential wiring error display.

DESCRIPTION OF CODES

- 20 [0076] 1 ELECTRONIC CIRCUIT BOARD
- 2 CORE MATERIAL
- 34 VIA
- 100 CAD SYSTEM FOR ELECTRONIC CIRCUIT BOARDS
- 102 INPUT/OUTPUT INTERFACE (INFORMATION OUTPUTTING MEANS)
- 25 103 CPU (Drafting layer setting means, CAD data inputting means, CAM data converting means, wiring net registering means, net group registering means, differential wiring generating means, line width and line spacing registering means, differential wiring moving means, retraction process executing means, differential wiring checking means, CAM data outputting means)
- 30 105 RAM
- 106 Keyboard
- 107 Mouse (Cad Data Inputting Means)

- 108 CD-ROM Drive
- 110 Hard Disk Drive (Storage Means)
- 112 Computer Main Body
- 120 CD-ROM
- 5 M1, M11, M3, M13 Conductor Layer (Power Layer, Ground Layer)
V1, V11, V2, V12 Insulation Layer

Claims

1. A CAD system for electronic circuit boards for creating design data for an electronic circuit board to be manufactured, comprising:
 - 5 drafting layer setting means for setting a plurality of drafting layers corresponding to a conductor layer and an insulation layer to be formed on the electronic circuit board;
CAD data inputting means for inputting CAD data for specifying design dimensions, shapes, and placement positions of those board elements
10 constituting the electronic circuit board which are predetermined to be drafting target elements, on the drafting layer;
wiring net registering means for performing attribute registration of a set of mutually different wiring nets that belong on a CAD data basis to a differential wiring constituted by a pair of wirings having mutually parallel
15 portions to a database before the differential wiring is input to the drafting layer as the drafting target element;
net group registering means that groups together differential wiring nets that have been registered by the wiring net registering means, and performs attribute registration in a database as a net group; and
20 retraction process executing means for performing a retraction process in order to individually connect the drafting target elements that express a via pad or a terminal pad (also referred to simply as pad), so that the difference in the wiring length calculated with reference to the net group is within a predetermined range, with regard to a pair of parallel wirings input onto the
25 drafting layer as the drafting target elements that constitute the differential wiring.
2. A computer program that, when installed on a computer, causes the computer to function as each of the means constituting the CAD system for
30 electronic circuit boards according to claim 1.
3. The electronic circuit board manufacturing method, comprising:

a step of designing an electronic circuit board for creating design information of the electronic circuit board as a set of CAD data by inputting the drafting target elements required for the electronic circuit board to be obtained as CAD data on the drafting layer, using the CAD system for electronic circuit
5 boards according to claim 1; and

an electronic circuit board manufacturing step of creating CAM data based on the CAD data, controlling electric circuit manufacturing equipment based on the CAM data, and manufacturing the electronic circuit board.

Abstract

Problem

- 5 To provide a CAD system suitable for designing electronic circuit boards including differential wiring, a computer program for achieving functions of the CAD system on a computer, and a method for manufacturing electronic circuit boards based on CAD data designed by the CAD system for electronic circuit boards.

10

Solution

Wiring LN1 and LN2, which constitute differential wiring, have mutually different wiring nets. These wiring nets are pre-registered to a net group.

15

One set of wiring nets can belong to only one net group. Wirings LN1 and LN2 are generated simultaneously by entering a midpoint of both in a width direction on a drafting layer. When these wirings LN1 and LN2 approach the pad up to a preset distance, a retraction process to the pad or a drafting support process is performed.

20

Selected Drawing: FIG. 22

FIG. 1

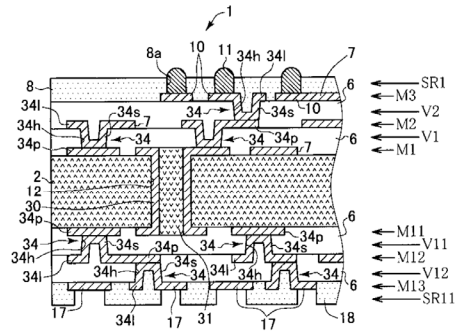


FIG. 2

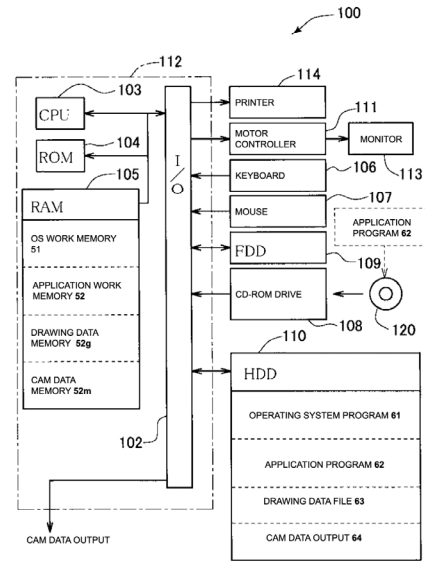


FIG. 3

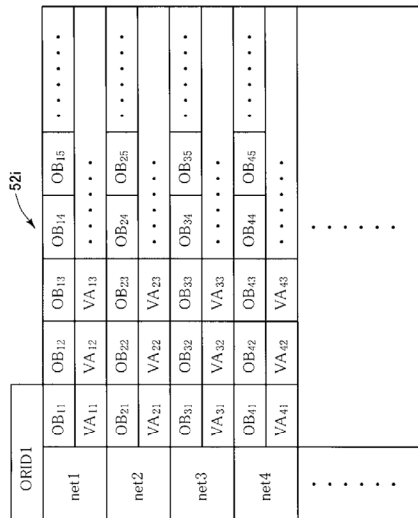


FIG. 4

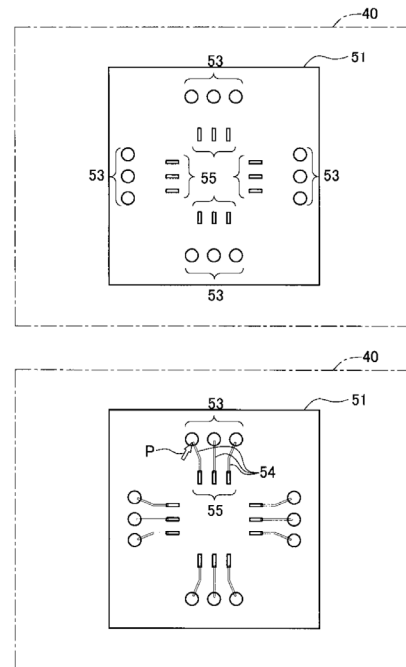


FIG. 5

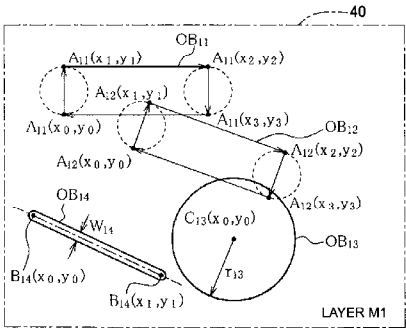


FIG. 7

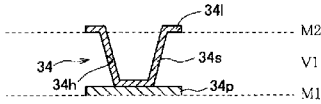


FIG. 8

VIA SPECIFIC DATA	VIA POSITION DATA	VIA FORMATION DATA
VA11	V11(x0,y0)	VLY11
VA12	V12(x0,y0)	VLY12
⋮	⋮	⋮

FIG. 6

ELEMENT SPECIFIC DATA	LAYER SPECIFIC DATA	ELEMENT DESCRIPTION DATA
OB11	LY1	A11(x0,y0), A11(x1,y1), A11(x2,y2), A11(x3,y3)
OB12	LY2	A12(x0,y0), A12(x1,y1), A12(x2,y2), A12(x3,y3)
OB13	LY3	C13(x0,y0), r13
OB14	LY4	B14(x0,y0), B14(x1,y1), W14
⋮	⋮	⋮

LY1=LY2=LY3=LY4=LAYER M1

FIG. 9

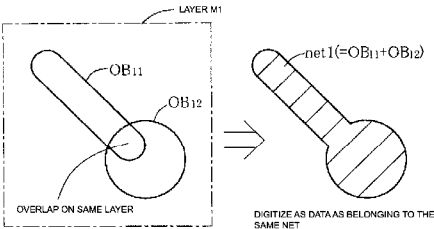


FIG. 11

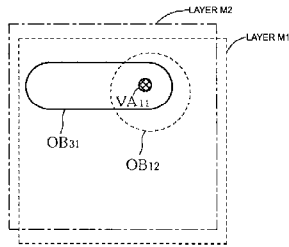


FIG. 10

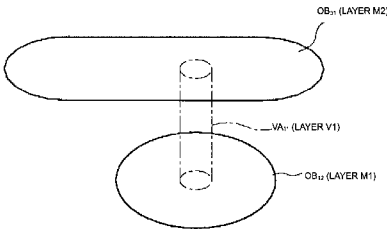
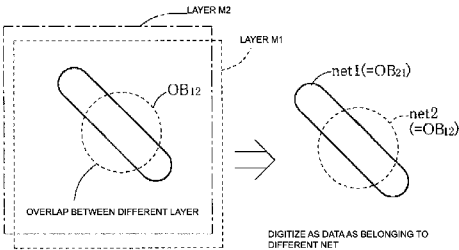


FIG. 12

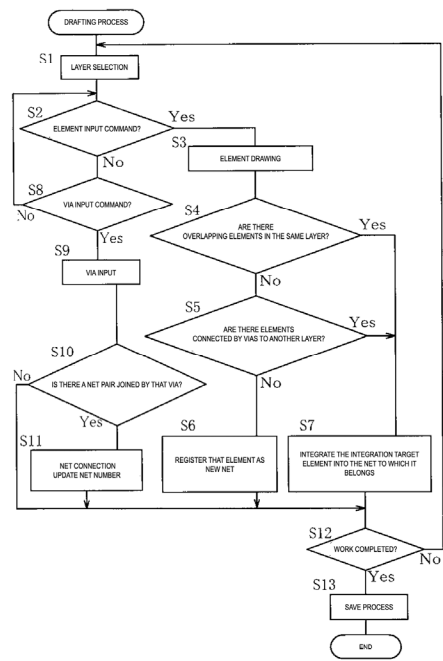


FIG. 13

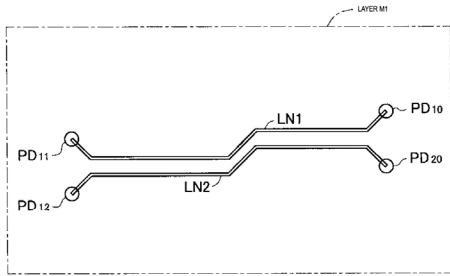


FIG. 14

NET GROUP DATA		52k
NT ₁	net11,net12	
NT ₂	net13,net14	
NT ₃	net15,net16	
⋮	⋮	

FIG. 15

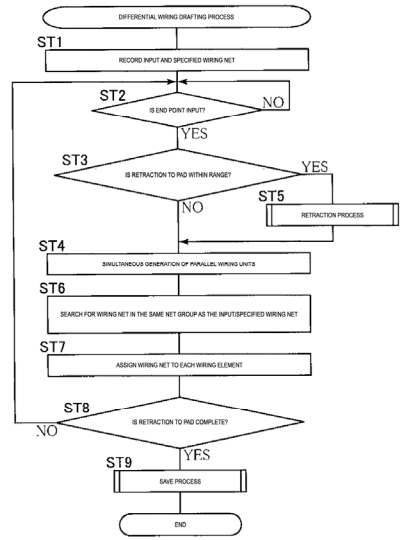


FIG. 16

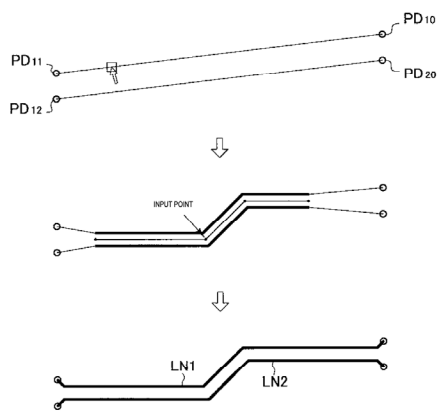


FIG. 17

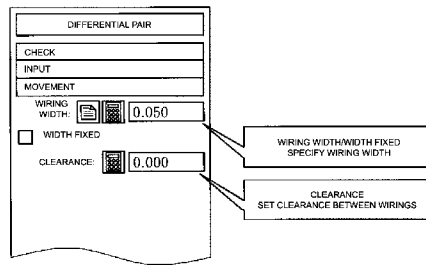


FIG. 19

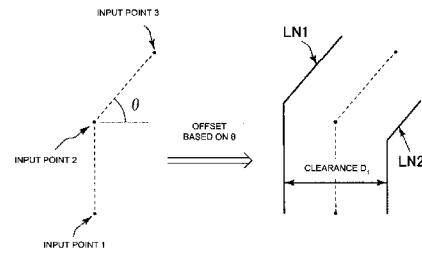


FIG. 18

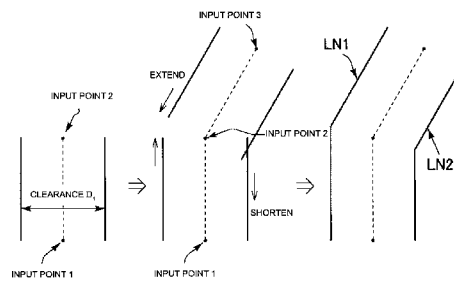


FIG. 20

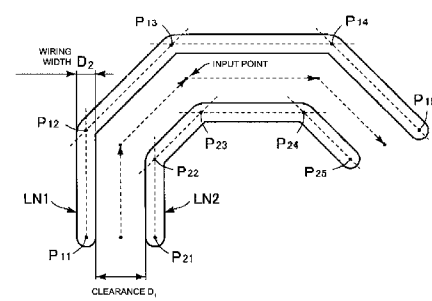


FIG. 21

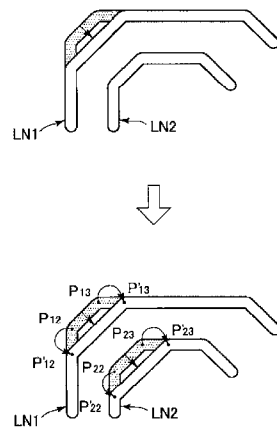


FIG. 22

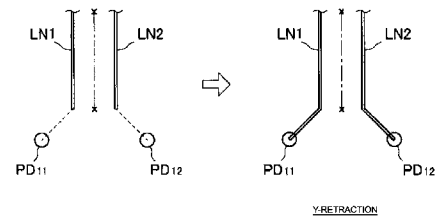


FIG. 23

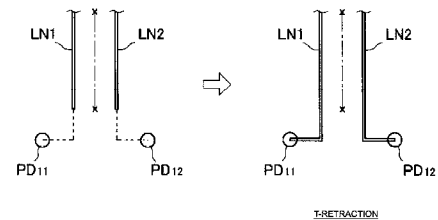


FIG. 24

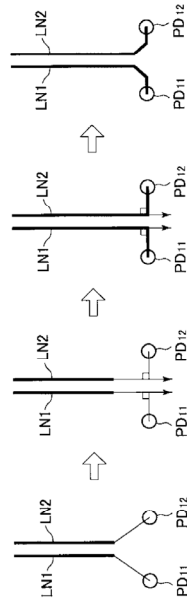


FIG. 25

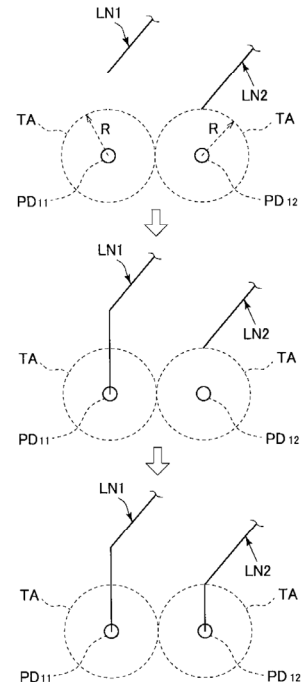


FIG. 26

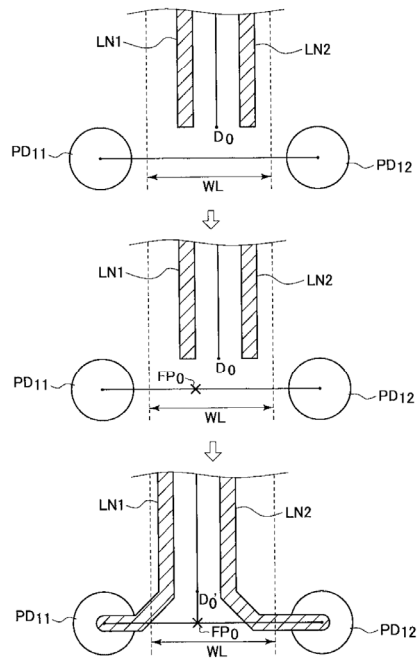


FIG. 27

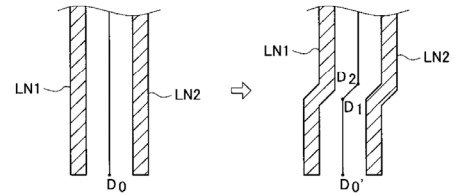


FIG. 28

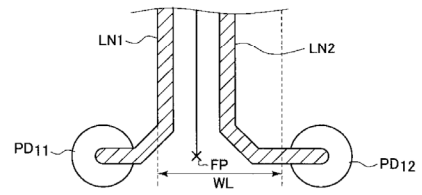


FIG. 29

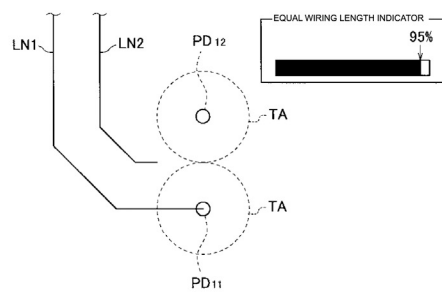


FIG. 30a

ERR[length-gap:15.8%]

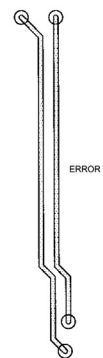
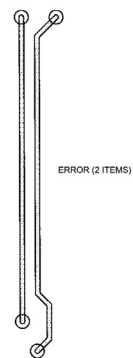


FIG. 30b

ERR[parallel:75% length-gap:17%]





CERTIFICATE OF TRANSLATION

Questel-Orbit, Incorporated
2331 Mill Road, Suite 600
Alexandria, VA 22314, U.S.A.
www.questel.com

Client Name: Fish & Richardson
Source Language: Japanese
Target Language: English
Project Number: FRPC2410007UT-L_Q

The document identified below was reviewed and verified by Questel-Orbit, Incorporated, through its translation subsidiary MultiLing Corporation or Morningside Translations, LLC. On behalf of the translating entity, the undersign certifies the following:

- 1) it is a professional translation company of multiple languages, including the source and target languages noted above;
- 2) to the best of its knowledge, information, and belief, the translated document is accurate as a publication quality translation; and
- 3) the above statements were made with the knowledge that willful false statements are punishable by fine or imprisonment under Section 1001 of Title 18 of the United States Code.

Original Document Identifier: #95503_JP2005309874A_original.pdf
Translated Document Identifier: #95503 57721-0003IP1-Bisenius_Drawings_en-US.docx & #95503 57721-0003IP1-Bisenius_Application_en-US.docx

Signed this 3rd day of April 2024

Name: Beverly Santamaria
Title: Project Manager