PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Attorney Docket No.: 122872.01

Date: May 6, 2009

Customer Number: 25944

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CONTINUING APPLICATION TRANSMITTAL
RULE 1.53(b)

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a

☒ Continuation ☐ Divisional ☐ Continuation-in-Part

application of prior pending Application No. 11/101,450 filed April 8, 2005.

For (Title): SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

By (Inventors): Yutaka KOBASHI

1. ☒ A Declaration of the inventor(s) is attached. The attached Declaration is:

   ☒ a. A copy of the Declaration from the parent application. (Used with the same or fewer inventors and (a) a copy of the prior application or (b) a revised, reformatted or edited version of the prior application that does not contain new matter.)

   ☐ b. A new Declaration. (Used with the same, fewer or additional inventors and (a) a copy of the prior application, (b) a revised, reformatted or edited version of the prior application that does not contain new matter, or (c) a new specification.)

2. ☒ A Power of Attorney is attached. The attached Power of Attorney is:

   ☒ a. A copy of the Power of Attorney from the parent application.

   ☐ b. A new Power of Attorney.

   ☐ The Power of Attorney is a General Power of Attorney.

   A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached, and

   A copy of the Assignment ☐ is attached to the Transmittal or ☐ was recorded at Reel _____ Frame _____.

   ☐ The Power of Attorney is a Specific Power of Attorney for this application.

   A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached, and

   A copy of the Assignment ☐ is attached to the Transmittal or ☐ was recorded at Reel _____ Frame _____.

   ☒ The Power of Attorney is in a combined Declaration/Power of Attorney.

   ☒ a. The Power of Attorney identifies no more than ten attorneys.

   ☐ b. The Power of Attorney identifies more than ten attorneys, and a separate Designation of Attorneys for Power of Attorney is filed herewith.

   ☐ c. The Power of Attorney is to the attorneys associated with a Customer Number.

BOE Tech. Group Exhibit 1002

3. ☒ The fees due upon filing are being paid electronically with this filing. The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) associated with this communication to Deposit Account No. 15-0461.

4. ☒ Application Data Sheet is attached.

5. ☒ Formal drawings (Figs. 1-11) are attached.

☐ Use Figure for front page of Publication.

6. ☒ Priority of foreign application No. 2004-198040 filed July 5, 2004 in Japan is claimed under 35 U.S.C. §119 and/or §365(b).

☒ The certified copy was filed in prior Application No. 11/101,450 on April 8, 2005.

☐ An electronic copy of the above foreign application(s) was received by the PTO in prior Application No. _____.

☐ A certified copy of the above foreign application(s) is filed herewith.

☐ A copy of the priority document was transmitted by the International Bureau in prior Application No. _____.

☐ An electronic copy of the above foreign application should be automatically retrieved by the PTO in accordance with the electronic priority document exchange service.

7. ☐ Priority of U.S. Provisional Application(s) No. _____ filed _____ is claimed under 35 U.S.C. §119.

(A Preliminary Amendment is attached to reflect the claim of benefit in the specification if not already present.)

8. ☒ The prior application is assigned of record to Seiko Epson Corporation, Tokyo, Japan and recorded at Reel 016459, Frame 0071.

9. ☐ This application is filed by fewer than all the inventors named in the prior application (37 C.F.R §1.53(b)(1)). Delete the following inventor(s) named in the prior application:

_____ _____

_____ _____

10. ☐ A Preliminary Amendment is attached. The Preliminary Amendment amends the specification to reflect the continuation data. Claims added by this Amendment are properly numbered consecutively beginning with the number next following the highest numbered claim in the application and claims canceled are identified in the listing of claims.

11. ☒ An Information Disclosure Statement is attached.

12. ☐ Small entity status:

☐ a. Entitlement to small entity status is asserted.

☐ b. Small entity status is no longer claimed.

13. ☐ Other: _____

14. ☐ As also indicated in the attached Request, this application is NOT to be published under 35 U.S.C. 122(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jarrett L. Silver
Registration No. 60,239

JAO:JZS/axl

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Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka KOBASHI
Filer:	Thomas J. Pardini/Alexandra Lynard
Attorney Docket Number:	122872.01
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1090

Electronic Acknowledgement Receipt	
EFS ID:	5286241
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka KOBASHI
Customer Number:	25944
Filer:	Thomas J. Pardini/Alexandra Lynard
Filer Authorized By:	Thomas J. Pardini
Attorney Docket Number:	122872.01
Receipt Date:	06-MAY-2009
Filing Date:	
Time Stamp:	14:32:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1090
RAM confirmation Number	707
Deposit Account	150461
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	050609_Appdata.pdf	1202851 e7d157027b04eeabcfb837a6f3b2affeee2d0538	no	4
Warnings:					
Information:					
2		050609_Spec.pdf	1445768 c013ab1fc2827214517b336c2b808d3f62591910	yes	30

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	16
Claims	17	20
Abstract	21	21
Drawings-only black and white line drawings	22	27
Oath or Declaration filed	28	30

Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	050609_IDS.pdf	114382 aa63d3f53ba6aebe24e9df681672e9a92d35ea6f	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Transmittal of New Application	050609_AppTrans.pdf	101791 a999099b1595490becf6fd527a2d67bb663fdd6f	no	3
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	33125 595b24b985806bc6a19596299c8719cccd159989	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2897917		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yutaka		KOBASHI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Fujimichou	Country Of Residence[i]	JP
Citizenship under 37 CFR 1.41(b)[i]	JP		

Mailing Address of Applicant:

Address 1	
Address 2	

City		State/Province	
Postal Code		Country[i]	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	25944		
Email Address	email@oliff.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS		
Attorney Docket Number	122872.01	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	25944		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	11/101450	2005-04-08

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
2004-198040	JP	2004-07-05	◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

If the Assignee is an Organization check here. ☒			
Organization Name	Seiko Epson Corporation		
Mailing Address Information:			
Address 1	4-1, Nishi-shinjuku 2-chome, Shinjuku-ku		
Address 2			
City	Tokyo	**State/Province**	
Country [i]	JP	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Jarrett L. Silver/ for James A. Oliff			Date (YYYY-MM-DD)	2009-05-06
First Name	Jarrett	Last Name	Silver	Registration Number	60239

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

This is a Continuation of Application No. 11/101,450 filed April 8, 2005. The disclosure of the prior application is hereby incorporated by reference herein in its entirety.

BACKGROUND

[0001] The present invention relates to a semiconductor device, display device and electronic apparatus, and more particularly, to a display device having a driving circuit provided on an active matrix substrate.

[0002] In a semiconductor device, it is important to take measure against the electro-static damages (ESD) when a high voltage caused by a static electricity or a various noise phenomenon is unintentionally applied to the inside of the device to damage an insulating film, thereby causing a fatal damage to the device. In order to prevent the problem, various protective circuits have been proposed. For example, in Patent Documents 1 and 2, it has been proposed that an abnormal voltage applied to lines is discharged to GND, etc. by proper combination of diodes. However, since general semiconductor devices are formed on a silicon wafer made of conductive material, there are little chances of being electrified within the semiconductor device, so that it is a key issue to prevent the damage when a static electricity flows through input terminals. To solve such a problem, conventionally, protective circuits are formed between input terminals and the semiconductor device forming a circuit, i.e., immediately after the input terminals, so that it is prevented that the high voltage from the input terminals is transmitted to the device.

[0003] On the other hand, in a display device using an active element such as a thin film transistor (TFT), which has been rapidly spread in recent years, a device is formed on an insulating substrate. As a result, there is a problem in that it is easy that the device is easily electrified by static electricity, and that the electro-static damage is generated during the manufacturing process. On this account, for example, an electro-static measure is taken by forming an antistatic line, called as a guide ring or a short ring, at the periphery of an active matrix circuit.

[0004] In recent years, a display device having a built-in driving circuit has been widely spread, in which an improvement of a definition, a cost reduction and better reliability

are realized by using a polysilicon TFT having polysilicon serving as an active layer. In such a device, as a measure against the static electricity of the driving circuit, a conventional method used in a semiconductor on a silicon wafer is applied as it is, so that only protective circuits for preventing the static electricity from the input terminals are built in, and a conventional method of a display device not having the built-in driving circuit is used to protect the active matrix circuit from the static electricity. Hereinafter, the conventional art relating to the protection of the driving circuit will be described in detail with respect to FIG. 11.

[0005] FIG. 11 is a view illustrating a configuration of an active matrix substrate of a VGA-LCD using polysilicon TFT by the conventional art. Reference numerals 201-1 to 201-480 indicate scanning lines of the active matrix circuit, driven by a scanning line driving circuit 800. Reference numerals 202-1 to 202-1920 indicate data lines, and pixel transistors 401 composed of n-type transistors and pixel electrodes 402 are formed at intersections of the scanning lines and the data lines, respectively, to drive a liquid crystal device.

[0006] Reference numerals 801-1 to 801-480 indicate scanning line driving unit circuits composed of 480 stages, which form the scanning line driving circuit 800, and each of them is composed by a CMOS circuit. A specific configuration of the scanning line driving unit circuits 801-1 to 801-n is shown in FIG. 5.

[0007] Each of the scanning line driving unit circuits 801-1 to 801-480 is connected to a low potential power line 750 and a high potential power line 751, through which power is supplied. The low potential power line 750 is connected to a low potential power terminal 650, the high potential power line 751 is connected to a high potential power terminal 651. Also, the low potential power terminal 650 and the high potential power terminal 651 are connected to a power IC through a FPC, and they are supplied with reference potentials of a potential VS and a potential VD, respectively. Herein, VS is less than VD.

[0008] Further, a signal (for example, a clock signal) required for the operation of each of the scanning line driving unit circuits 801-1 to 801-480 are supplied from an external IC through signal lines 701 and 702 and signal terminals 601 and 602.

[0009] Here, in order to prevent TFTs constituting each of the scanning line driving unit circuits 801-1 to 801-480 from being damaged by the static electricity or noise current input through the low potential power terminal 650, the high potential power terminal 651

and the signal terminals 601 and 602, static electricity protection circuits ESD1 to ESD4 are provided between the input terminals 601, 650 and 651 and the scanning line driving unit circuits 801-1 to 801-480, respectively. A specific configuration of the static electricity protection circuit ESD1 to ESD4 is shown in Patent Document 1 and Patent Document 2.

[0010] [Patent Document 1] Japanese Patent No. 2884946

[0011] [Patent Document 2] Japanese Patent No. 3141511

[0012] However, in the driving circuit on an insulating substrate, it is difficult for charges to escape as compared to the circuit on silicon wafer, and it is easy to be electrified. In addition, in the case that the driving circuit of the display device is formed on a glass substrate, the area of the circuit is larger as compared to the IC formed on a general silicon wafer. Therefore, in such a configuration, there is a problem in that a protection of the wiring lines far from the input terminals against the static electricity is not sufficient, especially during a manufacturing process. Specifically, since there is a possibility that the static electricity is electrified on a certain location on the substrate during the manufacturing process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation. Such a problem is the same in a semiconductor device using a SOI substrate.

[0013] Further, in a case of an insulating substrate, a large current may flow in the wiring lines by electrostatic induction when strong electrostatic discharge occurs in the outside of the substrate even in a finished product state after completion of the manufacturing process. Even in such a case, there is a possibility that a circuit located far from the terminal is damaged.

[0014] Furthermore, the present invention provides a measure against the problem in that potentials on the wiring lines are instantaneously changed, when a large amount of current flows in the wiring lines through a circuit.

SUMMARY

[0015] In order to solve the above problems, it is proposed that a semiconductor circuit be disposed between protective circuits and input terminals. More specifically, it is proposed that an electrical resistance between a connection part connecting the semiconductor

circuit to wiring lines and input terminals be lower than an electrical resistance between a connection part connecting the protective circuits to the wiring lines and the input terminals.

[0016] Thus, there is an effect that the protection against the static electricity is sufficiently obtained even in a place far from the terminal, by providing internal protective circuits in an area which is not connected to the input terminals of the wiring lines as well as providing the protective circuits around the input terminals as in the conventional art.

[0017] Further, it is proposed that a plurality of the protective circuits are arranged on the wiring lines and the semiconductor circuit is interposed between the protective circuits. Thereby, it is possible to prevent the static electricity or noise input from the input terminals, and to protect a semiconductor circuit far from the input terminals. In addition, it is preferable that the plurality of the protective circuits be arranged with a predetermined gap therebetween, thereby the entire part of the semiconductor circuit connected to the wiring lines can be protected.

[0018] Furthermore, in the present invention, it is proposed that the wiring line include a low potential power line and a high potential power line, and the protective circuits between power sources connected to both of the low potential power line and the high potential power line is comprised. In this configuration, the protective circuit can be easily formed by a diode element, etc., and since all are power lines, it is difficult to be affected by the noise. Also, in general, the power line is remarkably lengthened within a circuit, so that it requires a static protection more than other lines. Therefore, the effect is remarkable. In addition to this, for a signal line, it is proposed that the protective circuits between signal power sources be formed between the power lines. Since it is easy to be affected by the noise between the signal lines, it is possible to reduce an adverse influence by providing the protective circuit between the power source and the signal line. Also, it is proposed that the capacitance of the protective circuits between signal power sources be lower than the capacitance of the protective circuits between the power sources. In this way, it is possible to minimize an influence on the power line by the signal.

[0019] Further, in the present invention, the capacitive component between the wiring lines in the protective circuits is not less than $I \times t \times 0.1$ (F) when the maximum current flowing in the low potential power line or the high potential power line is I (A) and the maximum tolerable time when a voltage drop in power line occurs is t (second). t is

preferably below 10^{-8} (second) in consideration of general operation time in a polysilicon TFT. Thereby, when a large amount of current flows in the circuit and a supply from the outside is not sufficient to follow it to generate instantaneous voltage changes on the wiring lines, there is an effect that the voltage changes are reduced by the capacitive components within the protective circuits.

[0020] Further, in the present invention, it is proposed that the protective circuit between power sources or the protective circuit between signal power sources include a diode element, and one end of the diode element is connected to the power line. In this configuration, the static electricity or the noise current is easily discharged, so that the protective performance is remarkably improved.

[0021] Further, in the present invention, it is proposed that contents of the invention described above is applied to a so-called CMOS type semiconductor device, which is composed of an n-channel type field effect transistor and a p-channel type field effect transistor. Because the CMOS type semiconductor device requires at least 2 types of reference power source, the number of power line is increased, so that the effect of this invention is remarkable. Particularly, in the CMOS type semiconductor device composed of the polysilicon thin film transistor, the substrate is an insulating substrate, and thus electrification easily occurs under a state in which there is no protective circuit, so that the effect of the present invention is more prominent. Further, when an active matrix used in a TFT-LCD or TFT-OLED and a driving circuit thereof are formed on the insulating substrate, the driving circuit is configured to surround the active matrix, so that it becomes larger and accordingly its line is also lengthened. As a result, the effect of the present invention is more remarkable.

[0022] Further, in the present invention, it is proposed that, when the active matrix is applied to the present invention, internal protective circuits are arranged at corners far from the input terminals among four corners of the active matrix. By such a configuration, it is possible to arrange large-sized protective circuits without making the peripheral area large.

[0023] Moreover, in a display device using the semiconductor device of the present invention and an electronic apparatus having the display device, the electro-static damage is difficult to be generated during a manufacturing process, so that it is advantageous in terms of

cost, and it is difficult that the voltage drop at the power source occurs, so that there is an effect that the display quality is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Fig. 1 is a view illustrating a configuration of an active matrix substrate for explaining a first embodiment of the present invention;

[0025] FIG. 2 is a view illustrating a scanning line driving circuit for explaining a second embodiment of the present invention;

[0026] FIG. 3 is a view illustrating a configuration of an active matrix substrate for explaining a third embodiment of the present invention;

[0027] FIG. 4 is a view illustrating a protective circuit for explaining embodiments of the present invention;

[0028] FIG. 5 is a view illustrating a scanning line driving unit circuit for explaining embodiments of the present invention;

[0029] FIG. 6 is a perspective view (partially sectional view) of a liquid crystal display device for explaining the first embodiment of the present invention;

[0030] FIG. 7 is a view illustrating a buffer circuit for explaining the third embodiment of the present invention;

[0031] FIG. 8 is a view illustrating a buffer circuit for explaining another example of the third embodiment of the present invention;

[0032] FIG. 9 is a view illustrating a protective circuit for explaining the third embodiment of the present invention;

[0033] FIG. 10 is a graph illustrating a simulation result of a reference potential change for explaining the third embodiment of the present invention; and

[0034] FIG. 11 is a view illustrating a configuration of an active matrix substrate for explaining the conventional example.

DETAILED DESCRIPTION OF EMBODIMENTS

[0035] FIG. 1 is a view illustrating a configuration of an active matrix substrate having a built-in scanning line driving circuit according to a first embodiment in which a liquid crystal display device using a scanning line driving circuit of the present invention is implemented. 480 scanning lines 201-1 to 201-480 and 1920 data lines 202-1 to 202-1920 are provided orthogonally to each other on an active matrix substrate 101, and 480

capacitance lines 203-1 to 203-480 are alternately arranged in parallel to the scanning lines 201-1 to 201-480. The data lines 202-1 to 202-1920 are connected to data line input terminals 302-1 to 302-1920. The capacitance lines 203-1 to 203-480 are short-circuited from one another to be connected to a common potential input terminal 303. An opposite conductive part 304 is also connected to the common potential input terminal 303.

[0036] A pixel switching element 401-n-m composed of n-channel type electric field effect thin film transistor is formed at each intersection of the scanning line 201-n and the data line 202-m. Also, its gate electrode is connected to the scanning line 201-n, and its source and drain electrodes are connected to the data lines 202-m and pixel electrodes 402-n-m, respectively. The pixel electrode 402-n-m constitutes a capacitance line 203-n and an auxiliary capacitor, and forms a capacitor together with an opposing substrate electrode COM with a liquid crystal element therebetween when it is assembled as a liquid crystal display device.

[0037] The scanning lines 201-1 to 201-480 are connected to the scanning line driving circuit 800, which is formed by integrating polysilicon thin film transistors on the active matrix substrate, thereby being supplied to a drive signal. Herein, the scanning line driving circuit is composed of 480 scanning line driving unit circuits 801-1 to 801-480, which are connected to each of the scanning lines. In the present invention, the semiconductor circuit in the scope of claims is the scanning line driving circuit 800. Further, the wiring lines in the scope of claims represents a CLK signal line 701, a SP signal line 702, a high potential power source line 751, and a low potential power source line 750.

[0038] The CLK signal line 701, the SP signal line 702, the high potential power source line 751, and the low potential power source line 750 are connected to the scanning line driving circuit 800, to which a clock start pulse signal and the respective power source potentials are supplied. Herein, the CLK signal line 701, the SP signal line 702, the high potential power source line 751 and the low potential power source line 750 are connected to the CLK signal terminal 601, the high potential power source terminal 651 and the lower potential power source terminal 650, and the terminals are connected to an external IC through a FPC, etc. to supply a desired signal and a power source potential.

[0039] First to fourth protective circuits ESD1 to ESD4 are connected to a connecting line between the CLK signal terminal 601 and the CLK signal line 701, a

connecting line between a SP signal terminal 602 and a SP signal line 702, a connecting line between the high potential power terminal 651 and the high potential power source line 751, and a connecting line between the low potential power terminal 650 and the low potential power source line 750, respectively, thereby preventing TFTs within the scanning line driving circuit 800 from being damaged when the static electricity or noise current is input from each of the terminals 601, 602, 651 and 650.

[0040] In addition, fifth to seventh protective circuits ESD11 to ESD13 are disposed at far end of the opposite side, as seen from the CLK signal terminal 601 on CLK signal line 701, the high potential power source terminal 651 on the high potential power source line 751, and the low potential power source terminal 650 on the low potential power source line 750, with a scanning line driving circuit 800 therebetween. Thereby, it is possible to suppress that a unit, (for example, n = 1, etc.), located far from a terminal, among scanning line driving unit circuits 801-n, is damaged by the static electricity during manufacturing the active matrix substrate. Further, the fifth to seventh protective circuits ESD11 TO ESD13 can be arranged without making the substrate area larger, if arranged at the corner part of the active matrix substrate, particularly, at the corner opposite to the input terminals.

[0041] FIG. 4 is a view illustrating an example of a specific circuit configuration of protective circuits ESD1 to ESD13. A source electrode and a gate electrode of a p-type transistor 504 are connected to a high potential power source VH, and its drain electrode is connected to a wiring line being protected. A source electrode and a gate electrode of an n-type transistor 502 are connected to a low potential power source VL, and its drain electrode is connected to a wiring line being protected. Here, a signal level given to the wiring line being protected has to be not more than VH and not less than VL. When the potential of the power source being protected is out of the range of VH to VL by static electricity, etc., the n-type transistor 502 or the p-type transistor 504 is turned on, thereby an abnormal current runs through a reference potential VH line or a reference potential VL line. Also, by a protective resistor 503, it is possible to suppress that the potentials of the wiring lines rapidly increase to damage the n-type transistor 502 or the p-type transistor 504. Here, as VH and VL, the highest power source and the lowest power source are used within the circuit, respectively; however, VH = VD and VL = VS are also acceptable.

[0042] Further, the protective circuits ESD1 to ESD13 are the same configuration; however, it is possible that each of the protective circuits has a different circuit configuration according to its necessity. Particularly, compared to internal protective circuits ESD11 to ESD13, the protective circuits ESD1 to ESD4 of input part are required to have relatively high protective performance. On this account, for example, it is preferable that the first protective circuit ESD1 has a circuit configuration having protective performance higher than that of the fifth protective circuit ESD11. Specifically, it is preferable that the first protective circuit ESD1 is made to be larger than the fifth protective circuit ESD11 with respect to channel widths of the n-type transistor 502 and the p-type transistor 504.

[0043] FIG. 5 is a view illustrating an example of a configuration of scanning line driving unit circuits 801-1 to 801-480, which is composed of a NAND circuit, a NOT circuit, and a static type shift register using two clock inverters. Further, an OUT terminal of the scanning line driving unit circuit 801-n at the nth stage ($n < 480$) is connected to an IN terminal of the scanning line driving unit circuit 801-n-1 at the (n-1)th stage, and the IN terminal of the scanning line driving unit circuit 801-480 at the 480th stage is connected to the SP signal line 702.

[0044] FIG. 6 is a perspective view (partial cross-sectional view) illustrating a configuration of a transmissive liquid crystal display device according to a first embodiment. The active matrix substrate 101 shown in FIG. 1 is attached to an opposite substrate 901, in which common electrodes are formed by creating ITO on a color filter, by sealant 920, and nematic liquid crystal materials 910 are injected therebetween. Further, conductive materials are disposed in the opposite conductive part 304 provided on the active matrix substrate 101, and short-circuit the common electrodes of the opposite substrate 901.

[0045] A data line input terminals 302-1 to 302-1920, the common potential input terminal 303, the CLK signal terminal 601, the SP signal terminal 602, the high potential power source terminal 651, the lower potential power source terminal 650 are connected to one or a plurality of external ICs 940 through a FPC 930 mounted on the terminals to be supplied with a necessary electrical signal and potential.

[0046] Furthermore, an upper deflection plate 951 is disposed at the external side of the active matrix substrate, and a lower deflection plate 952 is disposed at the external side of the opposite substrate. They are disposed in such a way that polarizing directions thereof are

perpendicular to each other (crossed-Nicol). Also, a backlight 960 is attached to the lower deflection plate 952, so a liquid crystal display device is completed. The back light 960 may be a cold cathode tube to which a light guiding plate or a dispersion plate is attached, or a unit where an entire surface emits light by an EL element. Although it is not shown, the surrounding may be covered by an outer shell, or a protective glass or an acryl plate may be attached above the upper deflection plate, as needed.

[0047] In the liquid crystal display device, as compared to the conventional art, it is difficult that the electrostatic damage caused by the static electricity, etc. is generated during the manufacturing process or after the completion thereof. Therefore, the yield is good and the reliability is high.

[Second Embodiment]

[0048] FIG. 2 is a view illustrating a configuration of a driving circuit in a second embodiment implementing a liquid crystal display device using the scanning line driving circuit of the present invention. The figure is a diagram corresponding to the inside of the frame indicated by broken lines A of FIG. 1.

[0049] In the present embodiment, not only the input part protective circuits ESD1 to ESD3 between the terminals 601, 650 and 651 and the scanning line driving circuit 800, and the internal protective circuits ESD11 to ESD13 located at the far end with the driving circuit 800 therebetween as seen from the input terminals 601, 605 and 651, but also eighth to tenth protective circuits ESD21 to ESD23 are provided between the unit driving circuit 801-240 at the 240th stage, which is an intermediate stage of the driving circuit 800, and the unit driving circuit 801-241 at the 241st stage. Thereby, it is possible to suppress the damage caused by static electricity in the vicinity of the intermediate stage (n = 240), which is far from both the vicinity of the terminal and the far end of the terminal. In the present embodiment, the protective circuits are added only to the intermediate stage, but it is possible to increase the number of the protective circuits to be interposed in accordance with the size, etc. of the circuit. For example, in addition to the locations of the present embodiment, more preferably, the protective circuits are interposed between the 120th stage (801-120) and the 121st stage (801-121), and between the 360th stage (801-360) and the 361st stage (801-361). Most preferably, the protective circuits are interposed between all stages if there is no problem in the circuit area. However, in any case, a distance when interposing the protective

circuits should be approximately equal; otherwise, it is easy that the electro-static damage occurs only in a place where the distance is large.

[0050] With respect to the configuration of the active matrix substrate and the details of the protective circuits or the driving circuit in a place other than the above specified place, the second embodiment is the same as the first embodiment. Also, for the liquid crystal display device using the active matrix substrate including the circuit shown in FIG. 2, the configuration is the same as in the first embodiment, so the explanation is omitted.

[Third Embodiment]

[0051] FIG. 3 is a view illustrating a configuration of an active matrix substrate having formed with a scanning line driving circuit in a first embodiment implementing a liquid crystal display device using the scanning line driving circuit of the present invention.

[0052] In the present embodiment, different from the first and second embodiments, a CLK signal and a SP signal applied to the scanning line driving circuit 800 are not directly input from the CLK signal terminal 601 and the SP signal terminal 602, but, after driving capability is temporarily amplified at buffer circuits 810-1 and 810-002, they are input to the scanning line driving circuit 800. By such a configuration, even if the signal driving capability of the external IC is not so high, it is possible to drive the signal without a significant delay even in a panel having a large area.

[0053] FIG. 7 is a detailed view illustrating a configuration of the buffer circuits 810-1 and 810-2 in a third embodiment. A first NOT circuit 821 and a second NOT circuit 822 are connected in series by two stages. The transistor constituting the second NOT circuit 822 has a channel width (W) wider than the transistor constituting the first NOT circuit 821. For example, the first NOT circuit 821 is set to be W = 250 mm, and the second NOT circuit 822 is set to be W = 1000 mm. A power line 850 is a branch line branching from the low potential power source line 750 of FIG. 3, and the power source line 851 is a branch line branching from the high potential power source line 751 of FIG. 3. White circles indicate branching point directions, and eleventh and twelfth circuits ESD41 and ESD42 are disposed at the opposite side, i.e., at the end of the branch lines 850 and 851, with the buffer circuits 810-1 and 810-2 interposed therebetween.

[0054] In such a configuration, the buffer circuits 810-1 and 810-2 are connected to a part between the first protective circuit ESD11 and the eleventh protective circuit ESD 41

on the low potential power source line 750 and the a part between the second protective circuit ESD12 and the twelfth protective circuit ESD 42 on the high potential power source line 751, so the protective performance when the static electricity is charged within the buffer circuit 810-1 and 810-2 is remarkably improved as compared to the case in which there is only the first protective circuit ESD11.

[0055] FIG. 8 is a detailed view illustrating another example of a configuration of the buffer circuits 810-1 and 810-2 in the third embodiment. As compared to the configuration of FIG. 7, a 13th protective circuit ESD51 and a 14th protective circuit ESD 52 are added on the wiring line connecting a connection point of a first NOT circuit 821 with a connection point of a second NOT circuit 822 provided on the low potential power source line 750 and the high potential power source line 751. The other configuration is the same as in FIG. 7. As such, there are also internal protective circuits in the intermediate points between circuits, and thus the protective performance is more improved.

[0056] Further, in this embodiment, there is another effect that the voltage change in power source is suppressed. The resistance of the power source line is limited. Thus, when a large current is instantaneously consumed in a complementary circuit, the voltage is changed even if it is partial and instantaneous. According to the present embodiment, the channel width of the second NOT circuit 822 is W = 1000 mm, which is extremely large, and an extremely large current instantaneously flows to change the potential of the power source when the input signal is inverted (the time depends on the capacitance value of the wiring line to which the output terminal of the second NOT circuit 822 is connected).

[0057] FIG. 10 is a view illustrating a simulation result of potential change with respect to time in the buffer circuit of FIG. 7 and FIG. 8. Hereinafter, the present embodiment will be described in detail by referring to FIG. 10. Graph 880 shows a waveform of the signal which is output from the first NOT circuit 821 and input to the second NOT circuit 822, in which the potential is changed from VS to VD. At this time, the n-type transistor constituting the second NOT circuit 822 is turned on to apply the potential of the output terminal to VS. At this time, a large current flows in the low potential power source line 850, so a voltage gradient is generated. As a result, the potential instantaneously increases slightly. In order to suppress this, it is preferable to widen the line width of the low potential power source line 850, but it may be limited due to the circuit area. The graph 881

shows the potential around the second NOT circuit 822 of the low potential power source line 850, when the low potential power source line 850 is fixed as a predetermined line width, especially, when countermeasures are not taken, and it can be seen that the voltage instantaneously increases.

[0058] When such a phenomenon occurs, the driving capability of the buffer circuit is deteriorated, and it is possible to have an adverse effect on other circuits connected to the low potential power source line 850. In other words, the voltage drop as in graph 881 is transmitted to other circuits through the low potential power source line 850, thereby causing malfunction in the worst case. As a result, it affects the output precision in the case of an analog circuit. Such a problem is more conspicuous in a TFT circuit on an insulating substrate, which has a circuit area larger than that of a circuit on a silicon wafer, especially, in the driving circuit of the display device.

[0059] Next, the graph 882 shows a result of the case in which an appropriate capacitative element is added to the low potential power source line. In this case, the current instantaneously flowing is supplied from the capacitative element to some degree, so the voltage drop is small. In other words, in order to reduce the voltage drop, the capacitative element is preferably added to the power source line. The larger the capacitance of the capacitative element is, the greater the effect of reducing the voltage drop is. However, according to the inventor of the present invention, if the maximum current flowing in the power source line is I (A) and the tolerance time when a voltage drop occurs is t (second), the capacitative element having a capacitance not less than I x t x 0.1 (F) was effective on the voltage drop. On the other hand, the capacitative element having a capacitance not more than I x t x 0.1 (F) was not significantly effective on the voltage drop. Here, the tolerance time t when the voltage drop is generated is determined by the maximum operation speed of a logical circuit or sampling time of an analog circuit. Generally, in the TFT using a polysilicon, the operation speed is not so high and the limit of the maximum operation is several 10 MHz at most. In other words, the power source voltage change not more than 10n second almost causes no problem. Further, the maximum current flowing in the power source is the same as the maximum instantaneous current consumption of the circuit.

[0060] Accordingly, when the maximum current consumption in the circuit is I (A) and the tolerance time when the voltage drop is generated is t (second), it is effective on

reduction of the voltage drop if a capacitance not less than I x t x 0.1 (F) to the power source. At that time, the time is preferably t £ 10-8 (second). Further, it is preferable that another power source line of which the potential is not changed is connected to the capacitance. However, when such a capacitance is provided, the circuit area increases. As such, when a plurality of protective circuits are disposed on the power line as in this embodiment, a capacitance is generated between the power source line being protected and the reference potential power source lines VH and VL by the capacitative components on the protective circuits. In this case, since the circuit also functions as a protective circuit or as a measure against the power source potential change, it is significantly advantageous in terms of the circuit area.

[0061] When a reduction of such a power source potential drop change is expected, it is necessary to provide the protective circuits near the circuit of which a current consumption is large. Otherwise, a voltage change still occurs by the power source line resistance between the circuit having a large current consumption and the protective circuits. Specifically, the distance (X) of the power source line from the circuit having a large current consumption to the protective circuits should be smaller than the distance (Y) of the power source line from the circuit having a large current consumption to the input terminals.

[0062] The specific configurations of the first to second, and the eleventh to fourteenth protective circuits ESD1 to ESD2, and ESD11 to ESD14, respectively, is preferably the same as in FIG. 4 or 9. The explanation on the circuit configuration of FIG. 4 is omitted since it is the same as in the first embodiment. However, even in this configuration, the capacitance is added between the wiring line protected by the gate-drain capacitance component of the transistor and the high potential power source VH and the lower potential power source VL. In the configuration of FIG. 9, compared to the configuration of FIG. 4, the first capacitance 505 and the second capacitance 506 are added. Thus, when a strong voltage is instantaneously applied, they are combined with the protective resistor 503 to operate as a CR circuit. Thereby, a function is improved, which suppresses the n-type transistor 502 and the p-type transistor 504 from being damaged. Also, since the capacitances between the protective line and the high potential power source VH, and between the protective line and the low potential power source VL can be adjusted by the first

capacitance 505 and the second capacitance 506. Thus, it is an effective configuration as a measure against the power source voltage drop.

[0063] Furthermore, in such a configuration, the capacitance of the protective circuits ESD1, ESD2, ESD11 and ESD12 connected to the low potential power source line 750 and the high potential power source line 751 should be smaller than the capacitance of the protective circuits ESD3, ESD4 and ESD13 connected to the signal lines 701 and 702. The reason is that the potential of the signal line is changed, so if the capacitance between the signal line and the protective circuit is too large, a cross-talk is generated between the protective circuit and the reference power source line connected to the signal line. Specifically, if the configuration of the protective circuits is the same as in FIG. 9, the first capacitance 505 and the second capacitance 506 of the protective circuits (ESD1, ESD2, ESD11, and ESD12) connected to the low potential power source line 750 and the high potential power source line 751 are preferably set to be larger than the first capacitance 505 and the second capacitance 506 of the protective circuits ESD3, ESD4 and ESD13 connected to the signal lines 701 and 702.

[0064] Even in a case of forming a complementary circuit other than the buffer circuit described in the present embodiment, such as a data line driving circuit, DAC circuit, power circuit, level shift circuit, memory circuit, etc. on the active matrix substrate, it is preferable to provide the protective circuits at the end or intermediate of a branched power line, and it is more preferable that all circuits are located on the power line between protective circuits. Also, it is preferable in terms of reduction of the power noise that protective circuits having a capacitance not less than a predetermined value are provided at the front and rear ends of the circuit having high current consumption. Specifically, when the current consumption of the circuit is I and the tolerable time when the voltage drop occurs (typically, $t \leq 10^{-8}$ (second)), it is preferable to have the capacitance not less than I x t x 0.1 (F)).

[0065] With respect to the configuration of the active matrix substrate and the details of the protective circuits or the driving circuit in a place other than the above specified place, the third embodiment is the same as the first embodiment. Also, for the liquid crystal display device using the active matrix substrate shown in FIG. 3, the configuration is the same as in the first embodiment, so that the explanation is omitted.

[0066] Further, in the first embodiment, only the protective circuit of FIG. 4 has been described, however, it is possible to obtain the same effect as in the third embodiment by providing the protective circuit of FIG. 9.

[Industrial Applicability]

[0067] The present invention is not limited to the above-mentioned embodiments, but it can be also applicable to a liquid crystal display using an active matrix substrate formed with a data line driving circuit, a DAC, a power circuit, etc. In this case, the present invention may be applicable to each of the circuits, or it may be applied to some of the circuits if there is any problem in layout, and so on. In case of applying it to the scanning line driving circuit, various sequential selection circuits as well as the shift register circuit as in the embodiment are possible.

[0068] Further, the protective circuits can have the same configuration as in the embodiment and foregoing examples, and any configurations which have been suggested so far can be used.

[0069] Further, instead of a polysilicon transistor, an amorphous silicon thin film transistor may be used. Also, instead of a thin film transistor formed on the insulating substrate, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is formed on a crystal silicon wafer.

[0070] Further, as a liquid crystal display device, it may be a reflective type or a transflective type instead of the transmission type, and it may be a projection type light value instead of a direct viewing type light value. Also, a normally black mode can be used instead of a normally white mode as in the embodiment. Especially, in this case, a vertical alignment mode or a horizontal electric field switching mode may be possible as an alignment mode of the liquid crystal.

WHAT IS CLAIMED IS:

1. A display device, comprising:

a semiconductor circuit;

a wiring line electrically connected to the semiconductor circuit;

an input terminal electrically connected to the wiring line to supply an electrical signal; and

a first protection circuit and a second protection circuit that are electrically connected to the wiring line to protect the semiconductor circuit;

the first protection circuit being electrically connected to the wiring line between (i) a connecting portion of the semiconductor circuit and the wiring line and (ii) the input terminal; and

the semiconductor circuit being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line.

2. The display device as set forth in claim 1, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being arranged on the wiring line between at least one set of two consecutive semiconductor circuits of the plurality of semiconductor circuits to protect the plurality of semiconductor circuits.

3. The display device as set forth in claim 1, the wiring line being at least one of a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the semiconductor circuit.

4. The display device as set forth in claim 1, the wiring line being a signal input wiring line that transmits a signal to the semiconductor circuit.

5. The display device as set forth in claim 1, further comprising:

a substrate;

the semiconductor circuit being arranged on the substrate;

the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

6. An electronic device provided with the display device as set forth in claim 1.

7. A semiconductor device, comprising:

a wiring line over a first terminal portion to which an electrical signal is supplied from outside and a second terminal portion to which an electrical signal is not supplied from outside;

a semiconductor circuit electrically connected to the wiring line;

a first protection circuit being arranged on the wiring line between the semiconductor circuit and the first terminal portion to protect the semiconductor circuit;

a second protection circuit being arranged on the wiring line between the semiconductor circuit and the second terminal portion to protect the semiconductor circuit; and

a buffer circuit being arranged on the wiring line between the first terminal portion and the semiconductor circuit.

8. The semiconductor device as set forth in claim 1, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being arranged on the wiring line between adjacent sets of the semiconductor circuits of the plurality of semiconductor circuits to protect the plurality of semiconductor circuits.

9. The semiconductor device as set forth in claim 7, further comprising:

a first power source wiring line branched from a high potential power source wiring line;

a second power source wiring line branched from a low potential power source wiring line;

the buffer circuit being arranged between the first and second power source wiring lines;

a fourth protection circuit that sandwiches the buffer circuit of the first power source wiring line being arranged opposite to a branching point from the high potential power source wiring line to protect the buffer circuit; and

a fifth protection circuit that sandwiches the buffer circuit of the second power source wiring line being arranged opposite to a branching point from the low potential power source wiring line to protect the buffer circuit.

10. The semiconductor device as set forth in claim 7, further comprising:

the buffer circuit including a first NOT circuit to which the electrical signal is input and a second NOT circuit electrically connected to the first NOT circuit in series;

a sixth protection circuit being arranged on the first power source wiring line between a point of connection with the first NOT circuit and a point of connection with the second NOT circuit to protect the buffer circuit; and

a seventh protection circuit being arranged on the second power source wiring line between a point of connection with the first NOT circuit and a point of connection with the second NOT circuit to protect the buffer circuit.

11. The semiconductor device as set forth in claim 7,

the buffer circuit including a first NOT circuit to which the electrical signal is input and a second NOT circuit electrically connected to the first NOT circuit in series;

each of the first and second NOT circuits consisting of a complementary-type transistor; and

a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit.

12. The semiconductor device as set forth in claim 7,

the wiring line comprising a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the semiconductor circuit.

13. The semiconductor device as set forth in claim 7,

the wiring line comprising a signal input wiring line that transmits a signal to the semiconductor circuit.

14. The semiconductor device as set forth in claim 7, further comprising:

a substrate on which the semiconductor circuit is arranged;

the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

15. A display device provided with the semiconductor device as set forth in claim 7.

16. An electronic device provided with the display device as set forth in claim 7.

ABSTRACT

To prevent an electrostatic damage on a display device formed with a driving circuit. Protective circuits are provided not only at input terminal parts, but also at intermediate parts of a circuit or at the ends of wiring lines. Otherwise, the protective circuits are provided at the ends of the wiring lines and at the places immediately before and after the input terminals, respectively, and then the circuit is interposed therebetween. Further, the protective circuits are provided around a circuit with a large current consumption.

FIG. 1

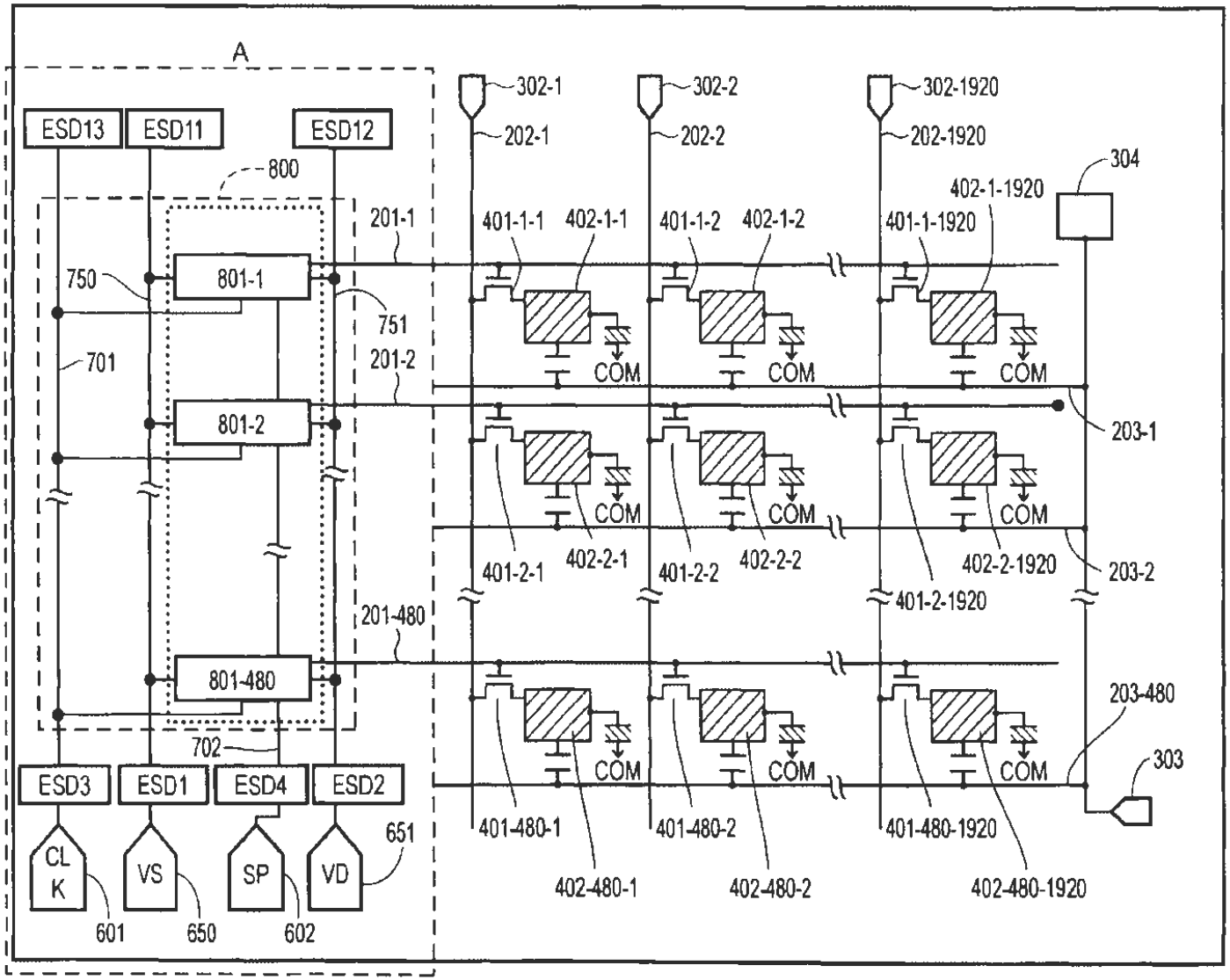

A
ESD13
ESD11
ESD12
800
201-1
750
801-1
751
701
201-2
801-2
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
CL K
VS
SP
VD
651
601
650
602
302-1
302-2
302-1920
202-1
202-2
202-1920
304
402-1-1920
401-1-1
402-1-1
401-1-2
402-1-2
401-1-1920
COM
203-1
401-2-1
402-2-1
401-2-2
402-2-2
402-2-1920
203-2
401-2-1920
203-480
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401-480-2
401-480-1920
402-480-1
402-480-2
402-480-1920

FIG.2

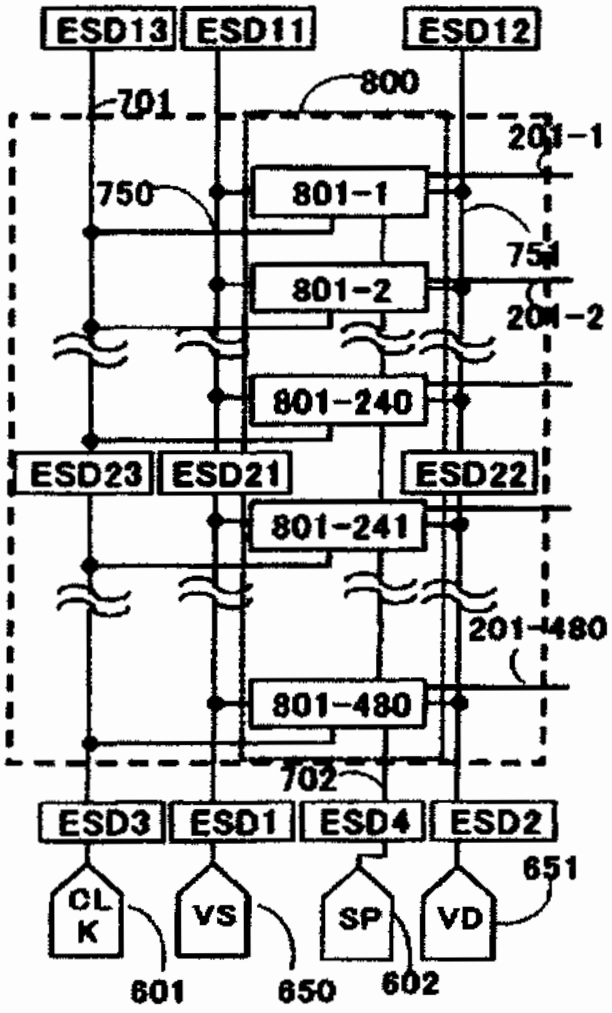

ESD13
ESD11
ESD12
701
800
201-1
750
801-1
751
801-2
201-2
801-240
ESD23
ESD21
ESD22
801-241
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602

FIG.3

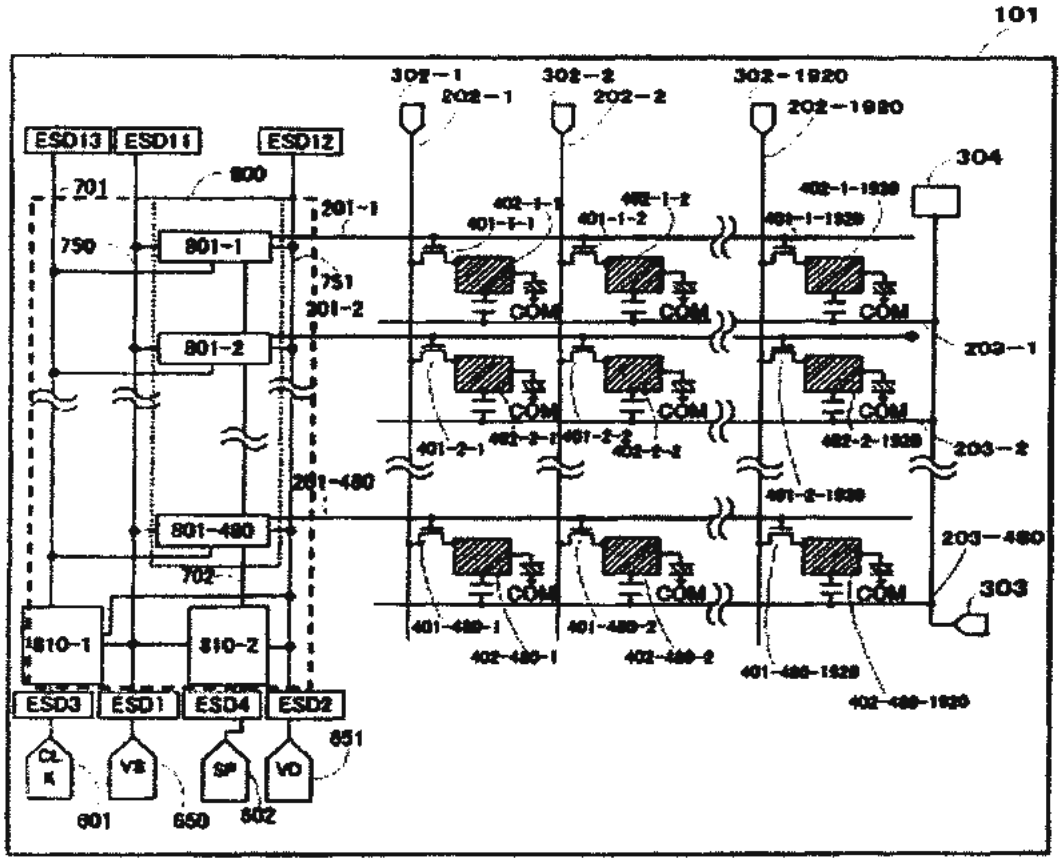

101
302-1
302-2
302-1920
202-1
202-2
202-1920
304
ESD13
ESD11
ESD12
701
800
201-1
750
801-1
751
201-2
801-2
201-480
801-480
702
810-1
810-2
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VO
601
650
502
COM
202-1
203-2
203-480
303

FIG.4

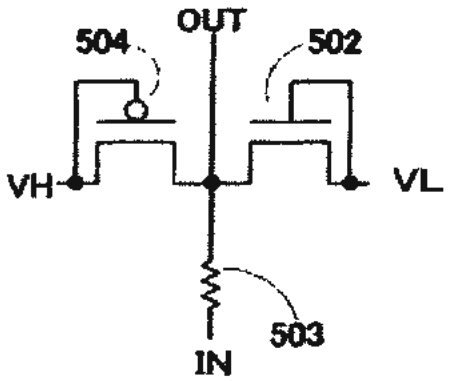

OUT
504
502
VH
VL
503
IN

FIG.5

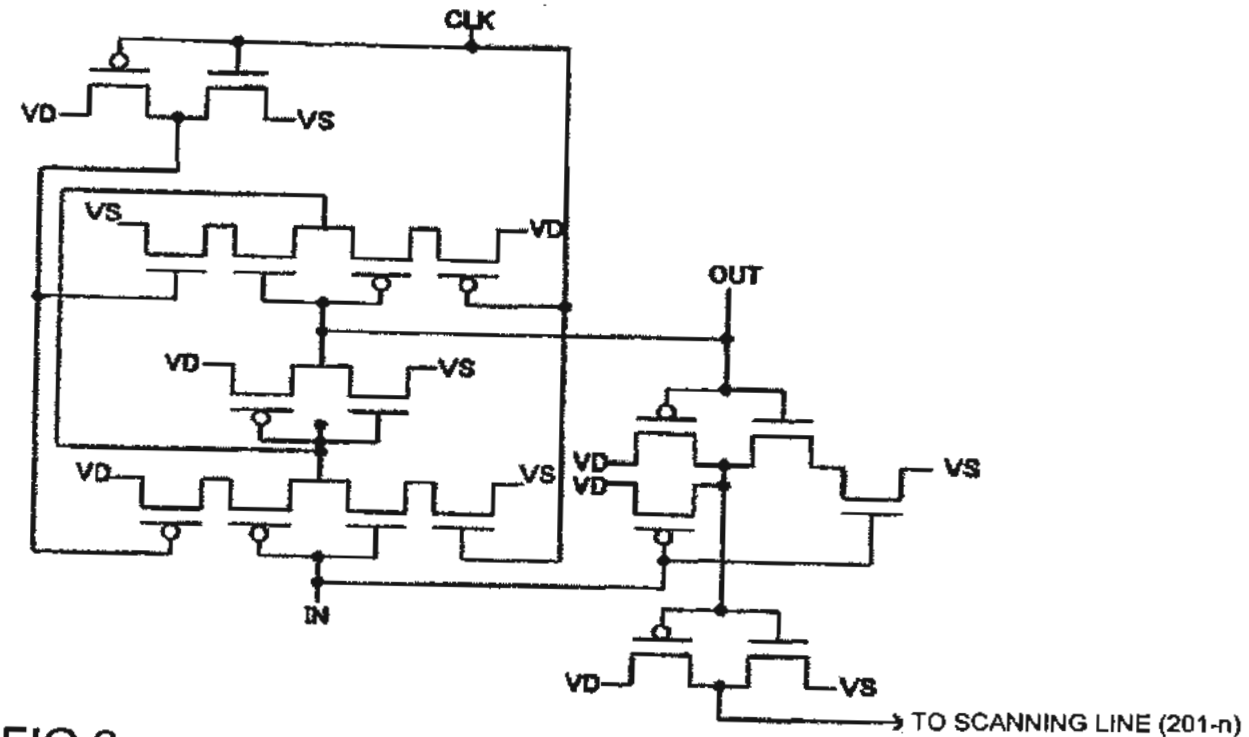

CLK
VD
VS
VS
VD
OUT
VD
VS
VD
VS
VD
VD
VS
IN
VD
VS
TO SCANNING LINE (201-n)

FIG.6

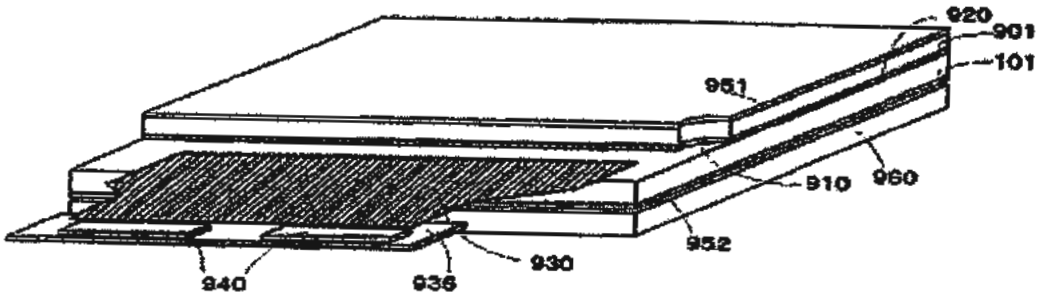

920
901
101
951
910
960
952
930
940
936

FIG.7

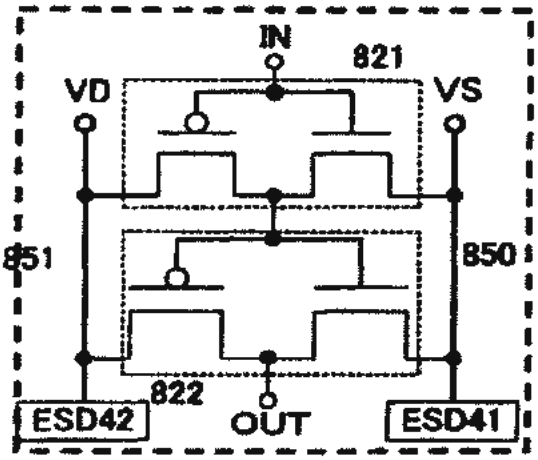


FIG.8

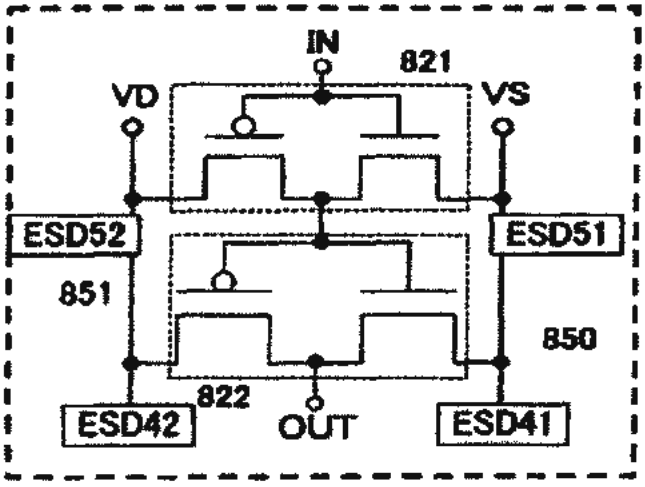


FIG.9

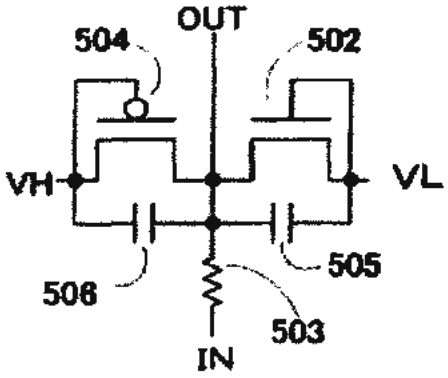


FIG.10

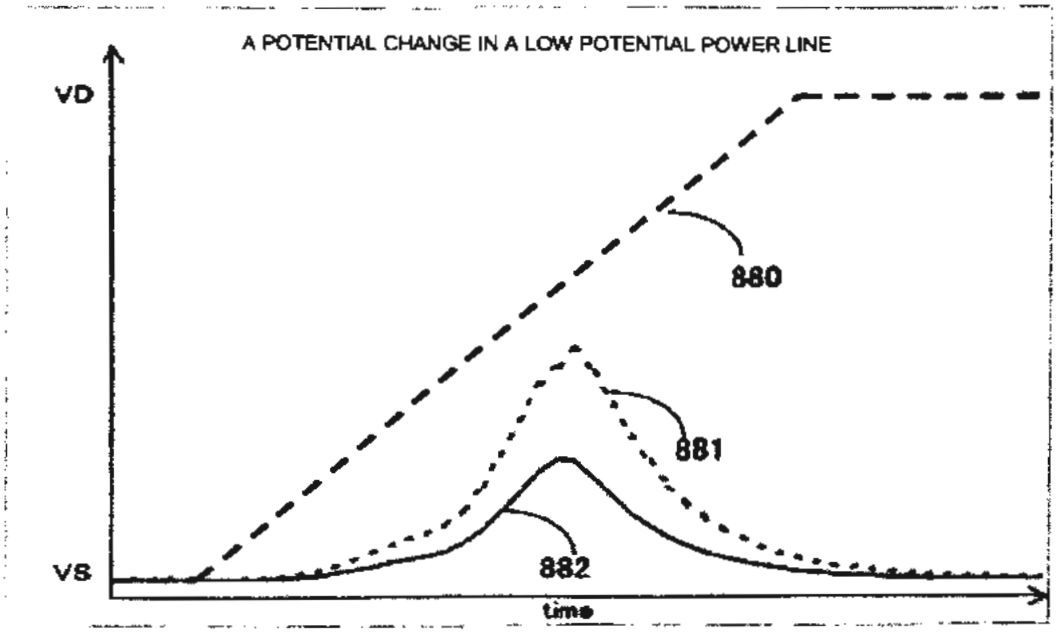
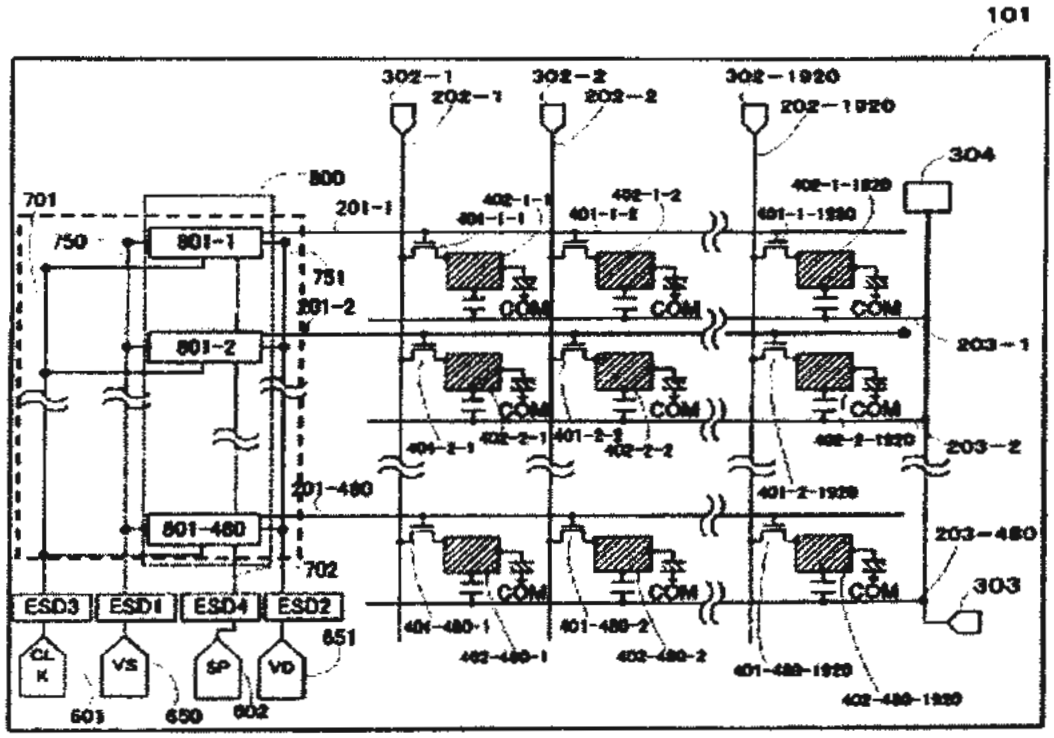

A POTENTIAL CHANGE IN A LOW POTENTIAL POWER LINE
VD
VS
880
881
882
time

FIG.11


101
302-1
302-2
302-1920
202-1
202-2
202-1920
304
800
701
201-1
750
801-1
751
801-2
203-1
203-2
201-480
801-480
203-480
702
303
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
603
650
602
COM

PTO/SB/105 (8-96)
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Seiko Epson Ref. No.: J0111137US01 Attorney's Ref. No.: 122872

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。	As a below named inventor, I hereby declare that:
私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。	My residence, post office address and citizenship are as stated next to my name.
下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
半導体装置、表示装置及び電子機器	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、	the specification of which is attached hereto unless the following box is checked:
☐ _____に提出され、米国出願番号または特許協定条約 国際出願番号を _____ とし、（該当する場合） _____ に訂正されました。	☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).
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私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。	I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
2004-198040	Japan	05/July/2004	☐
			☐

私は、第３５編米国法典１１９条（ｅ）項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条（ｃ）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１章５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106 (8-96)
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James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

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直接電話連絡先：（名前及び電話番号） OLIFF & BERRIDGE, PLC (703) 836-6400	Direct Telephone Calls to: *(name and telephone number)* OLIFF & BERRIDGE, PLC (703) 836-6400
唯一または第一発明者名 小橋 裕	Full name of sole or first inventor Yutaka KOBASHI
発明者の署名 日付 小橋 裕 2005年3月28日	Inventor's signature Date Yutaka Kobashi March 28, 2005
住所 日本国, 長野県, 富士見町	Residence Fujimichi-machi, Nagano, Japan
国籍 日本	Citizenship Japan
私書箱 392-8502 日本国長野県諏訪市大和3丁目3番5号 セイコーエプソン株式会社内	Post Office Address c/o Seiko Epson Corporation 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan
第二共同発明者	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所 日本国, _____, _____	Residence _____, _____, Japan
国籍	Citizenship
私書箱	Post Office Address
（第三以降の共同発明者についても同様に記載し、署名をすること）	(Supply similar information and signature for third and subsequent joint inventors.)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Application No.: New U.S. Continuation Patent Application

Filed: May 6, 2009 Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. One or more reference cited herein was cited by or submitted to the Office in parent application No. 11/101,450 filed April 8, 2005, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, no copy of any such reference is attached. 37 CFR §1.98(d). See References 1-29.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jarrett L. Silver
Registration No. 60,239

JAO:JZS/axl

Date: May 6, 2009

OLIFF & BERRIDGE, PLC
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Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 122872.01	APPLICATION NO. New U.S. Continuation Patent Application
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yutaka KOBASHI	
		FILING DATE May 6, 2009	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	1	2002/0057392 A1	05/16/2002	Ha
	2	6,795,143 B1	09/21/2004	Fukushima
	3	2003/0030054 A1	02/13/2003	Hector et al.
	4	2005/0151706 A1	07/14/2005	Lifka et al.
	5	2002/0068388 A1	06/06/2002	Murakami et al.
	6	5,786,616	07/28/1998	Fukumoto et al.
	7	5,610,427	03/11/1997	Shida
	8	6,175,394 B1	01/16/2001	Wu et al.
	9	6,623,990 B2	09/23/2003	Watanabe et al.
	10	2002/0009890 A1	01/24/2002	Hayase et al.
	11	6,791,632 B2	09/14/2004	Lee et al.
	12	6,028,465	02/22/2000	So
	13	6,157,361	12/05/2000	Kubota et al.
	14	6,329,694 B1	12/11/2001	Lee et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	15	JP-B2-3141511	03/05/2001	Japan		
	16	JP-B2-2884946	04/19/1999	Japan		
	17	WO 03/088199 A1	10/23/2003	WIPO		
	18	CN 1396656 A	02/12/2003	China		
	19	JP-A-2003-308050	10/31/2003	Japan		

OTHER DOCUMENTS

Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: May 6, 2009

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	APPLICANT Yutaka KOBASHI	
	FILING DATE May 6, 2009	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	20	6,351,364 B1	02/26/2002	Chen et al.
	21	2004/0264080 A1	12/30/2004	Yang et al.
	22	5,719,647	02/17/1998	Fujikawa et al.
	23	2004/0085284 A1	05/06/2004	Chen et al.
	24	6,108,056	08/22/2000	Nakajima et al.
	25	4,654,865	03/31/1987	Sunazuka et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	26	JP-A-02-307258	12/20/1990	Japan		
	27	JP-A-2001-298157	10/26/2001	Japan		
	28	TW 441069B	06/16/2001	Taiwan		
	29	TW 441073B	06/16/2001	Taiwan		

OTHER DOCUMENTS

Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED

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Date: May 6, 2009

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Filing Date: **05/06/09**

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**16** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**2** minus 3 =	*	x$110			x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL			TOTAL	**1090**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/436,335	05/06/2009	2811	1090	122872.01	16	2

CONFIRMATION NO. 5191

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

FILING RECEIPT



Date Mailed: 05/29/2009

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Applicant(s)

Yutaka Kobashi, Fujimichou, JAPAN;

Assignment For Published Patent Application

Seiko Epson Corporation, Tokyo, JAPAN

Power of Attorney:

James Oliff--27075
Kirk Hudson--27562
William Berridge--30024
Thomas Pardini--30411
Edward Walker--31450
Robert Miller--32771
Mario Costantino--33565

Domestic Priority data as claimed by applicant

This application is a CON of 11/101,450 04/08/2005

Foreign Applications

JAPAN 2004-198040 07/05/2004

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 05/18/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/436,335**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/436,335	05/06/2009	Yutaka Kobashi	122872.01

CONFIRMATION NO. 5191

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ALEXANDRIA, VA 22320-4850

FORMALITIES LETTER

OC000000036037511

Date Mailed: 05/29/2009

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings have a line quality that is too light to be reproduced (weight of all lines and letters must be heavy enough to permit adequate reproduction) or text that is illegible (reference characters, sheet numbers, and view numbers must be plain and legible) see 37 CFR 1.84(l) and (p)(1)); See Figure(s) 10.
  - Numbers, letters, and reference characters on the drawings must measure at least 0.32 cm (1/8 inch) in height. See Figure(s) 3,11.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

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OIPE
JUN 22 2009
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

MAIL STOP MISSING PARTS

Yutaka KOBASHI

Application No.: 12/436,335

Filed: May 6, 2009 Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS WITH FORMAL DRAWINGS

Commissioner for Patents
P.O. Box 1450
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Sir:

In response to the Notice to File Corrected Application Papers - Filing Date Granted (copy attached) mailed on May 29, 2009, submitted herewith are 8 sheets of formal drawings (Figs 1-11) in compliance with 37 C.F.R. 1.84.

Entry of this document should complete all of the filing formalities and fully satisfy all requirements of the Notice to File Corrected Application Papers. Examination and allowance of this application in due course are respectfully solicited.

The Commissioner is hereby authorized to charge any fee (or credit any overpayment) associated with this communication to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jarrett L. Silver
Registration No. 60,239

JAO:JZS/cdk

Date: June 22, 2009

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/436,335	05/06/2009	Yutaka Kobashi	122872.01

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Date Mailed: 05/29/2009

DUE DATE
JUL 29 2009

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  - Numbers, letters, and reference characters on the drawings must measure at least 0.32 cm (1/8 inch) in height. See Figure(s) 3,11.

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DOCKETED
By CT on 6/1 2009
and
By clm on 06/01 2009
Oliff & Berridge

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FIG. 1

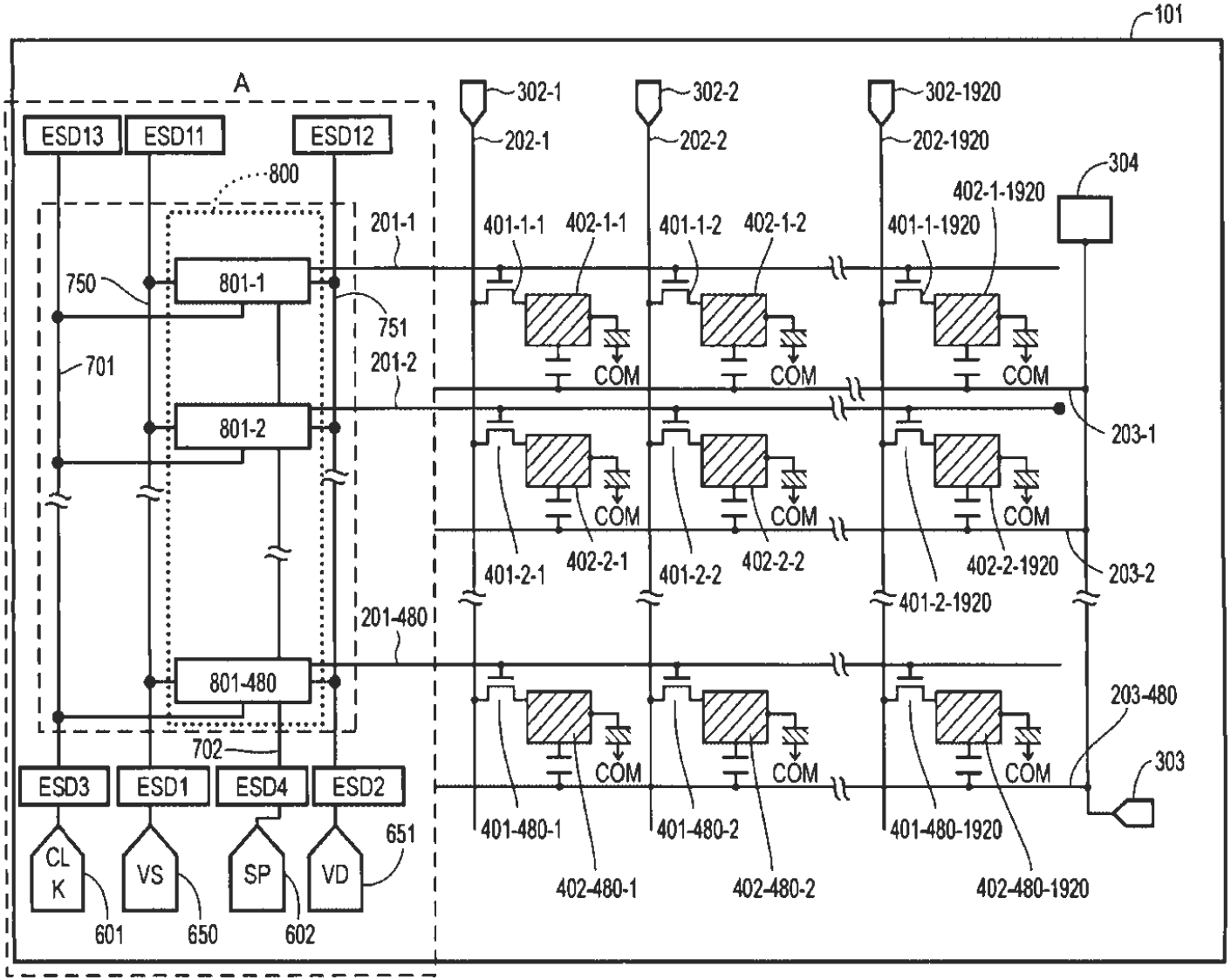
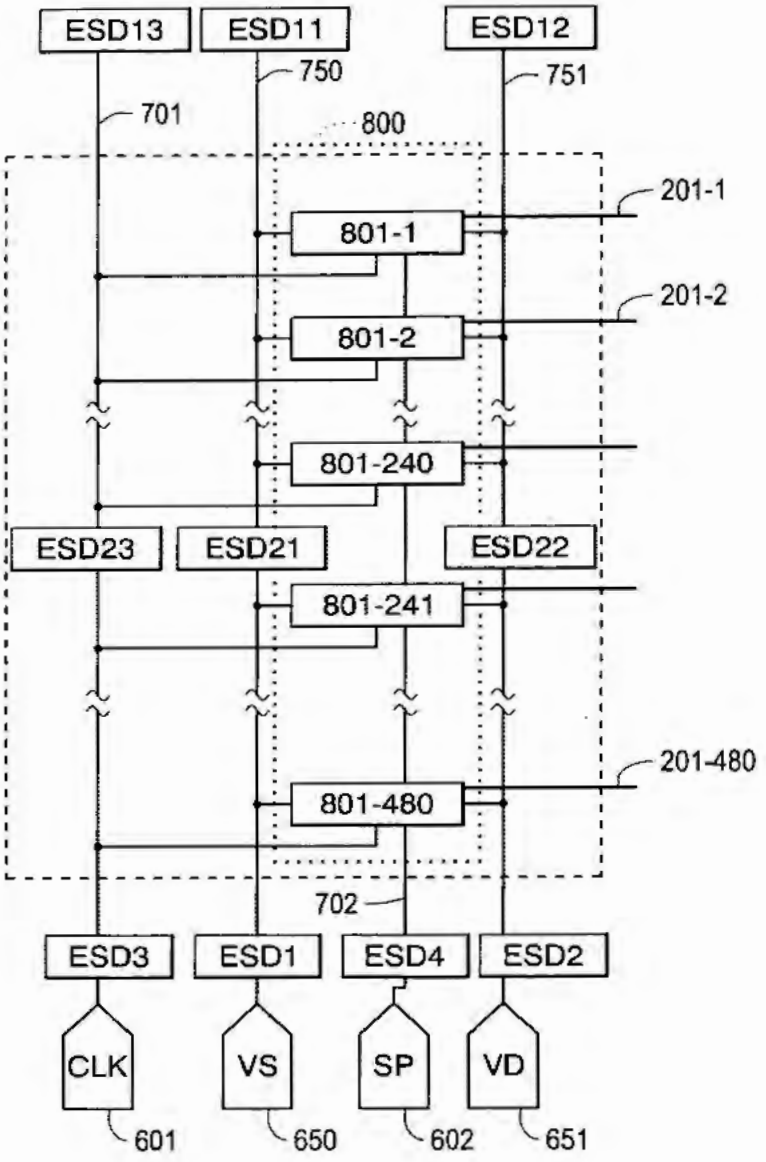

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A
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ESD11
ESD12
800
201-1
750
801-1
751
701
201-2
801-2
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602
302-1
302-2
302-1920
202-1
202-2
202-1920
304
402-1-1920
401-1-1
402-1-1
401-1-2
402-1-2
401-1-1920
COM
203-1
401-2-1
402-2-1
401-2-2
402-2-2
402-2-1920
203-2
401-2-1920
203-480
303
401-480-1
401-480-2
401-480-1920
402-480-1
402-480-2
402-480-1920

FIG. 2


ESD13
ESD11
ESD12
750
751
701
800
201-1
801-1
201-2
801-2
801-240
ESD23
ESD21
ESD22
801-241
201-480
801-480
702
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ESD1
ESD4
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VS
SP
VD
601
650
602
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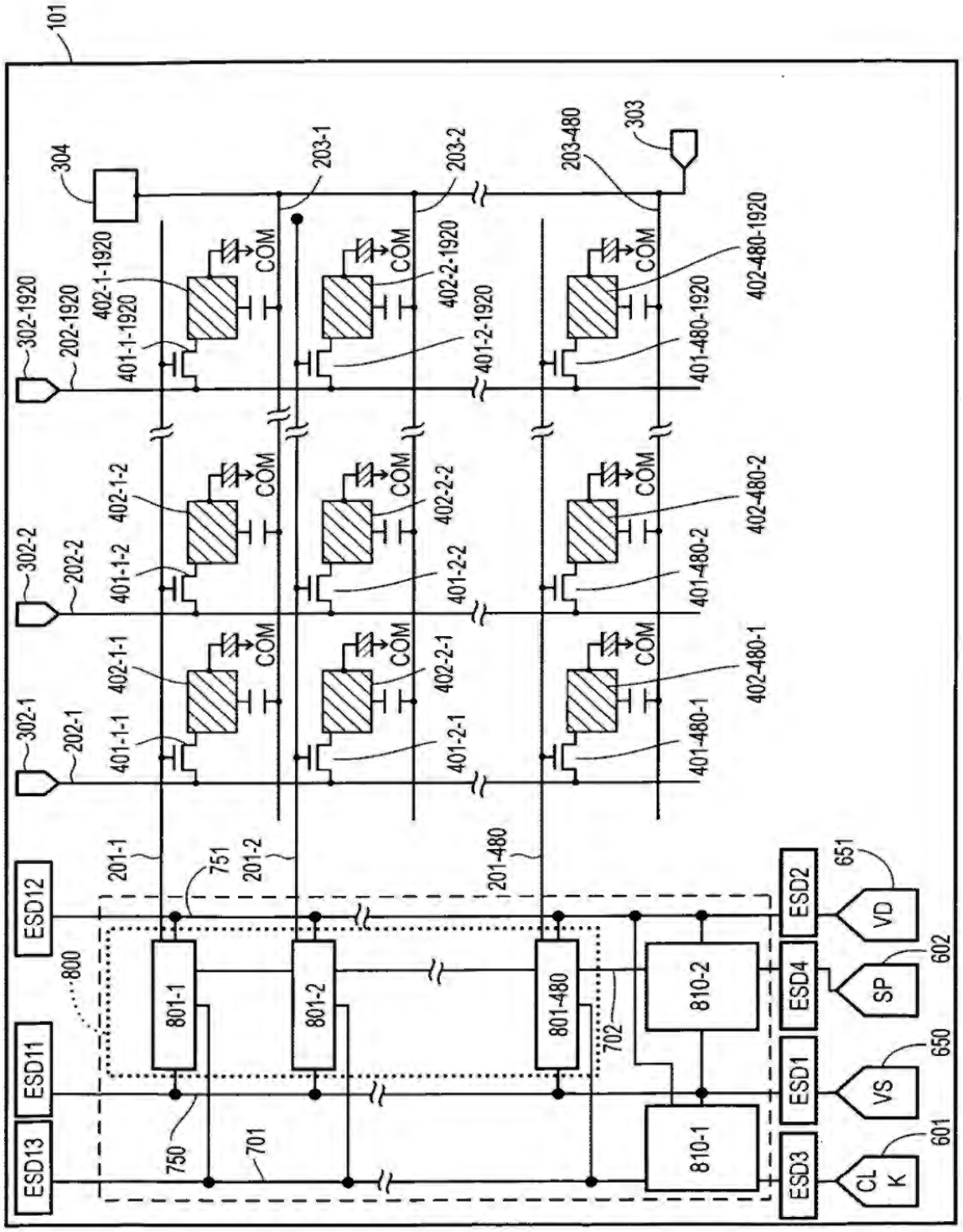

101
304
303
203-1
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401-2-1
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702
810-2
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ESD12
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FIG. 3

FIG. 4

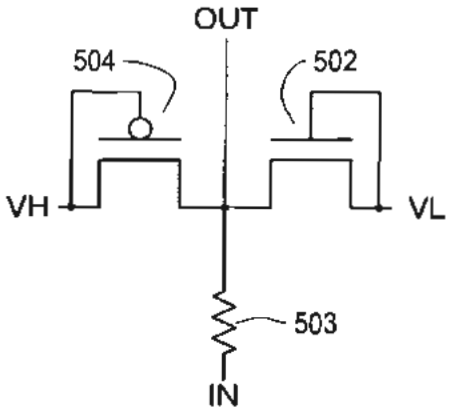


FIG. 5

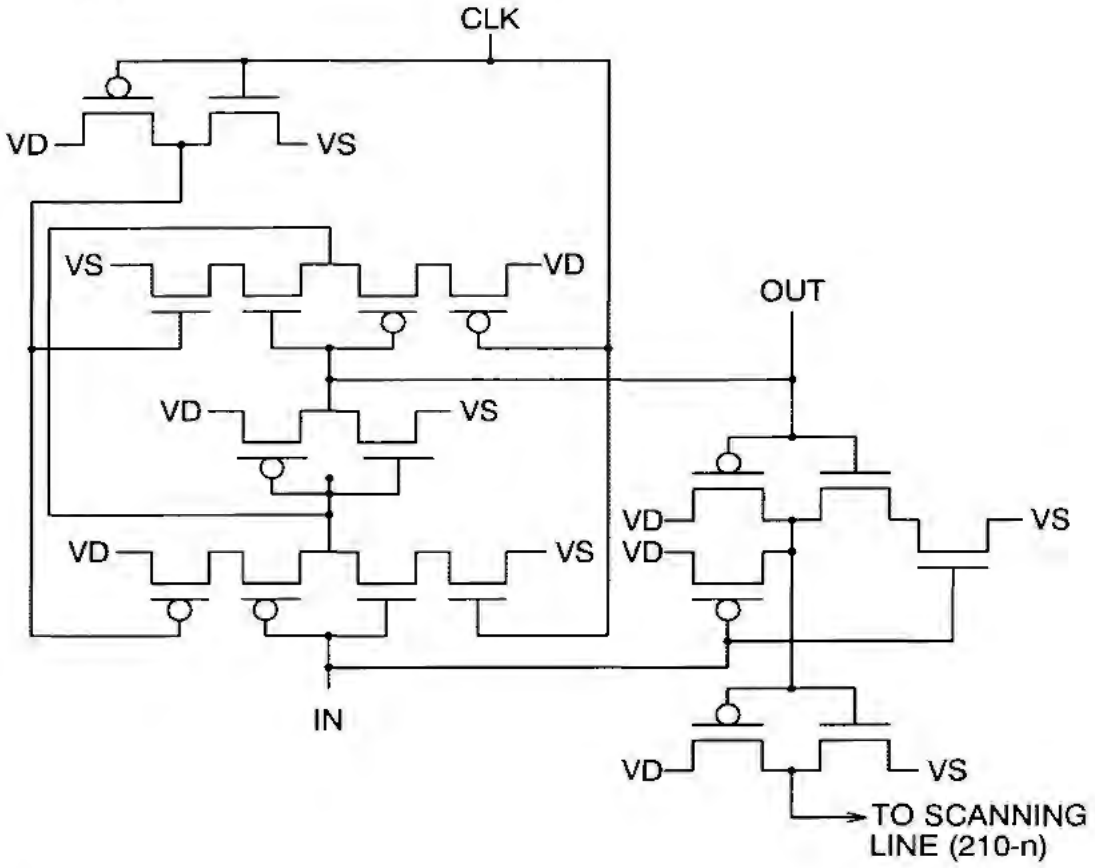

CLK
VD
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VD
VS
TO SCANNING
LINE (210-n)

FIG. 6

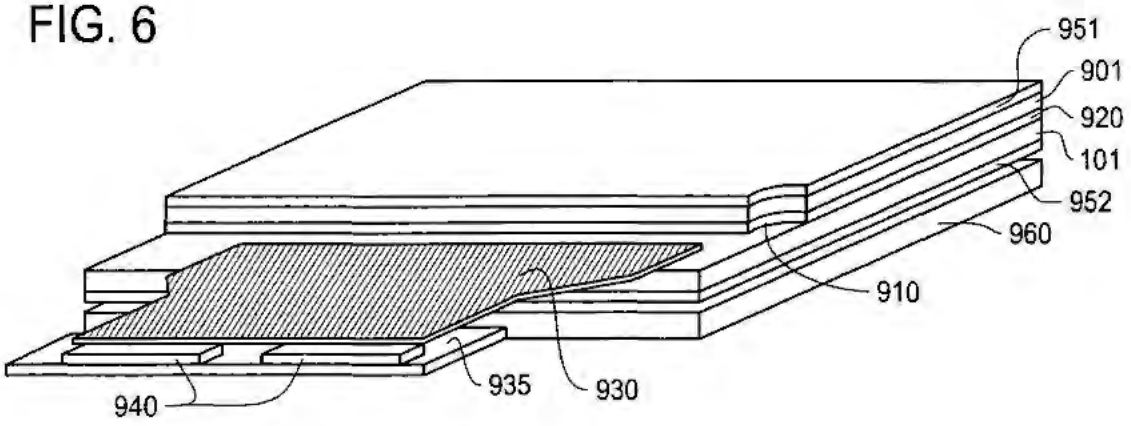

951
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FIG. 7

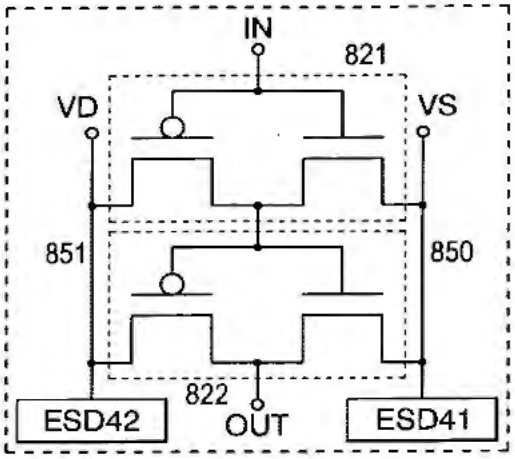


FIG. 8

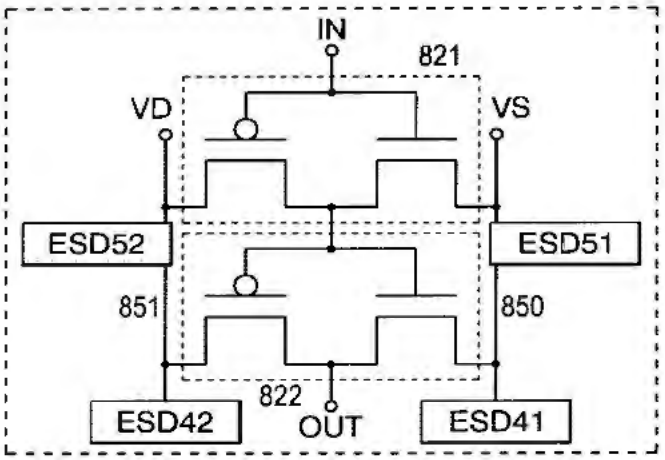
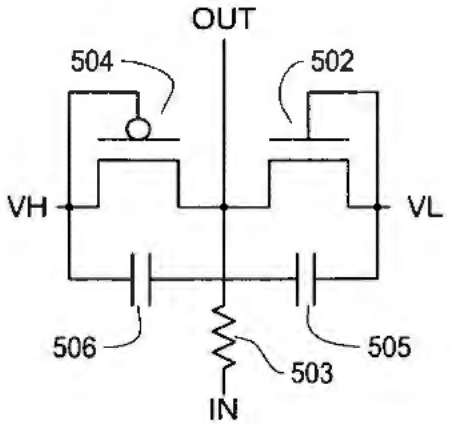


FIG. 9



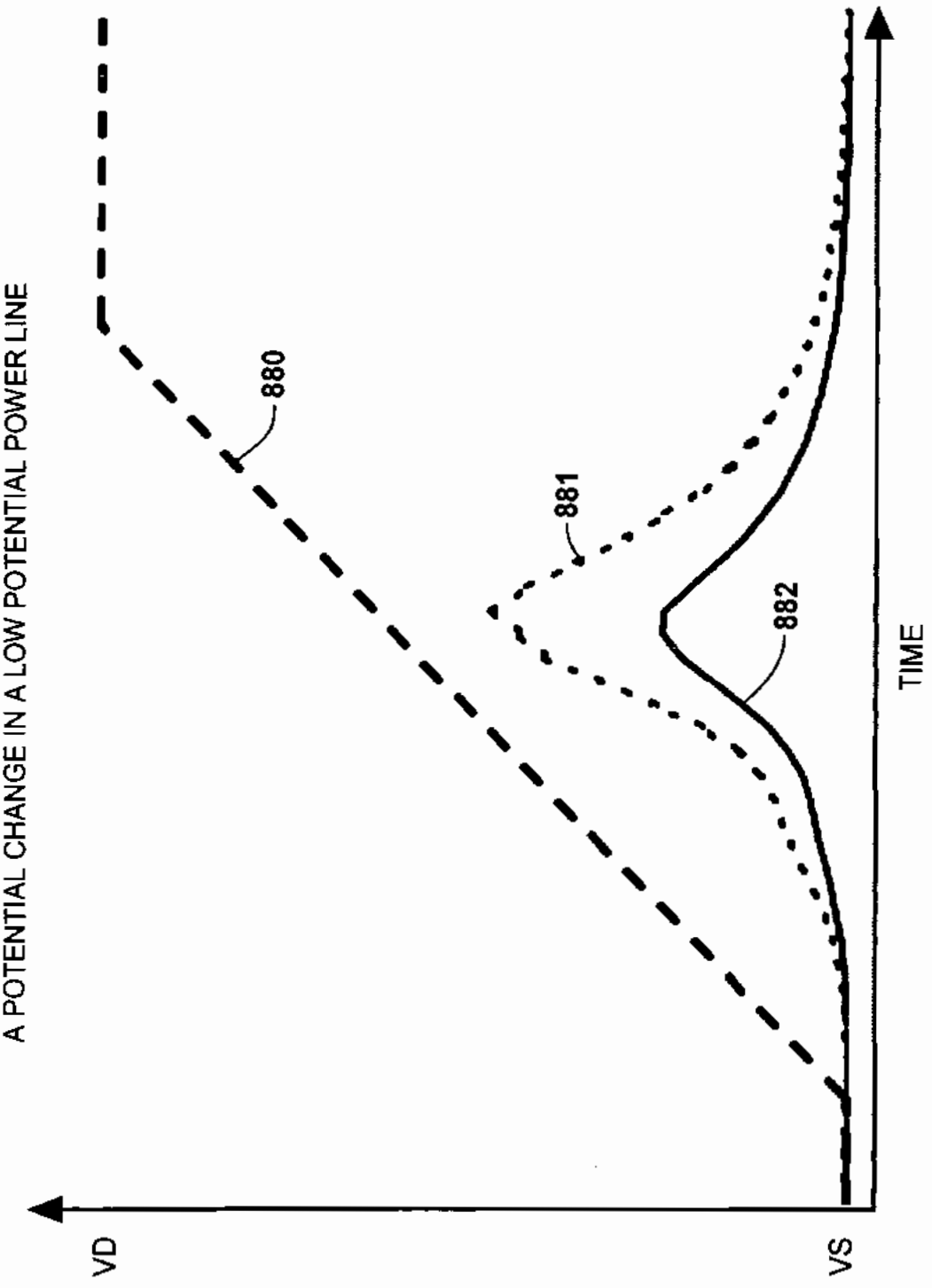

A POTENTIAL CHANGE IN A LOW POTENTIAL POWER LINE
880
881
882
VD
VS
TIME

FIG. 10

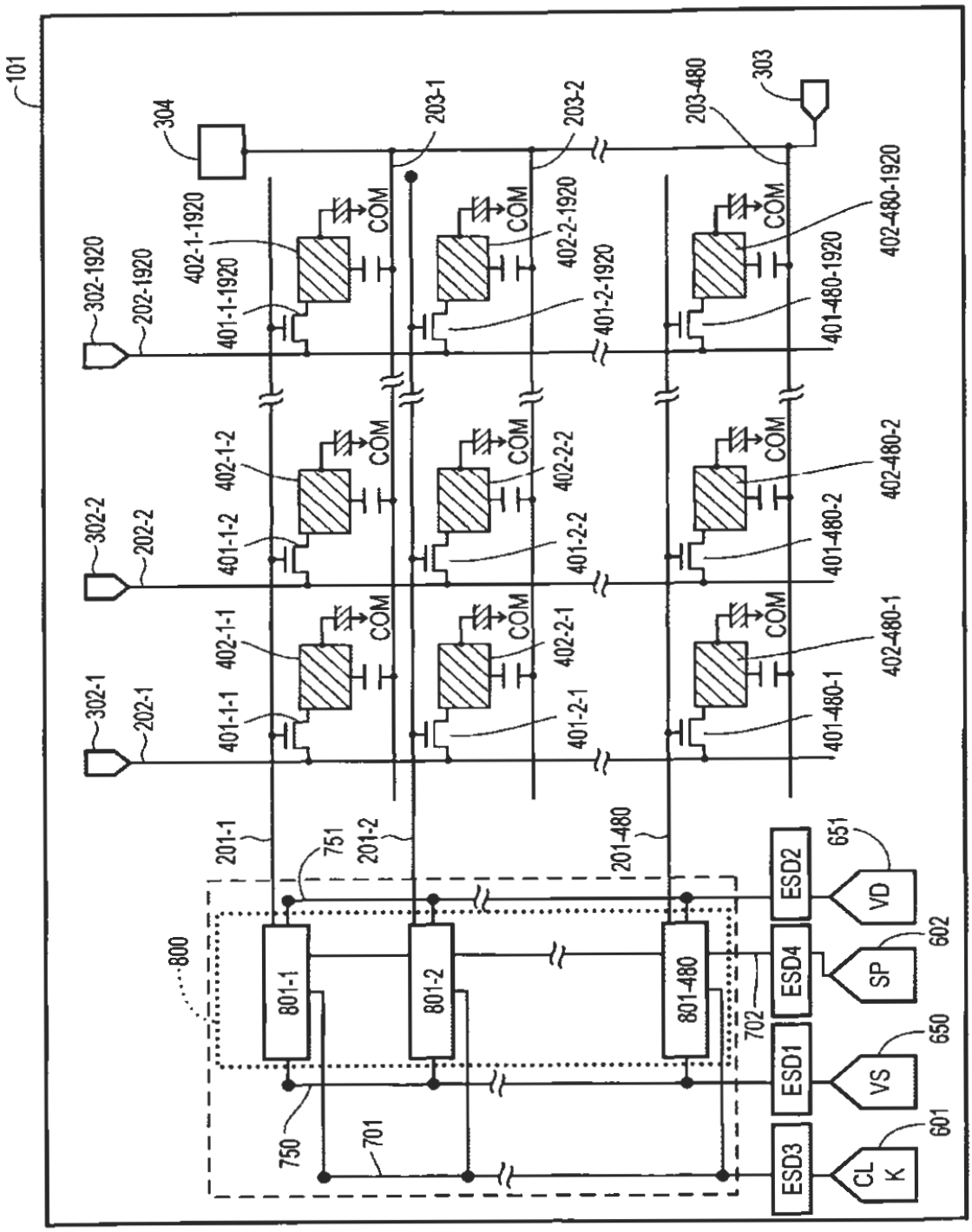

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401-480-1
COM
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201-2
201-480
751
800
801-1
801-2
801-480
750
701
702
ESD1
ESD2
ESD3
ESD4
VD
SP
VS
CL
K
651
602
650
601

FIG. 11

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CONFIRMATION NO. 5191

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Applicant(s)

Yutaka Kobashi, Fujimichou, JAPAN;

Assignment For Published Patent Application

Seiko Epson Corporation, Tokyo, JAPAN

Power of Attorney:

James Oliff--27075
Kirk Hudson--27562
William Berridge--30024
Thomas Pardini--30411
Edward Walker--31450
Robert Miller--32771
Mario Costantino--33565

Domestic Priority data as claimed by applicant

This application is a CON of 11/101,450 04/08/2005

Foreign Applications

JAPAN 2004-198040 07/05/2004

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/436,335**

Projected Publication Date: 10/08/2009

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

Preliminary Class

257

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【書類名】特許請求の範囲
【請求項１】
基板上に複数の半導体回路と、前記複数の半導体回路に電気的に接続された配線と、
電気信号を供給するため前記配線に電気的に接続された入力端子と、静電気やノイズから前記配線や前記半導体回路を保護するための前記配線に接続された保護回路により構成された半導体装置であり、前記複数の半導体回路のうち少なくとも一つの前記半導体回路が前記入力端子と前記保護回路の間に配置されてなることを特徴とする半導体装置。
【請求項２】
前記複数の半導体回路のうち少なくとも一つの前記半導体回路の前記配線との接続部から前記配線と前記入力端子との接続部までの間の電気抵抗値が、前記保護回路の前記配線との接続部から前記配線と前記入力端子との接続部までの間の電気抵抗値よりも小さいことを特徴とする請求項１に記載の半導体装置。
【請求項３】
前記保護回路は複数配置されてなり、前記複数の半導体回路のうち少なくとも一つの前記半導体回路が前記保護回路の間に配置されてなることを特徴とする請求項１から２に記載の半導体装置。
【請求項４】
前記複数の保護回路は概略一定の間隔で配置されてなる事を特徴とした請求項３に記載の半導体装置
【請求項５】
前記配線は少なくとも相対的に低い基準電位を供給する低電位電源配線と、相対的に高い基準電位を供給する高電位電源配線を含み、前記保護回路の少なくとも一つは前記低電位電源配線と前記高電位電源配線の両方にそれぞれ接続されてなる電源間保護回路である事を特徴とした請求項１から４に記載の半導体装置。
【請求項６】
前記入力配線は少なくとも固定された基準電位でない信号を伝達する信号入力配線を含み、前記保護回路の少なくとも一つは前記低電位電源配線と前記高電位電源配線の少なくともいずれか一方と、前記信号配線とに接続されてなる信号電源間保護回路である事を特徴とした請求項５に記載の半導体装置。
【請求項７】
前記低電位電源配線と前記高電位電源配線との間、または前記信号配線と前記低電位配線との間、または前記信号配線と前記高電位配線との間の少なくともいずれかには容量素子が設けられており、容量素子の容量値は、前記低電位電源配線もしくは前記高電位電源配線に流れる最大電流をＩ（Ａ）、前記低電位電源配線もしくは前記高電位電源配線の電圧降下が発生する許容時間の小さい方をｔ（秒）とした時、Ｉ×ｔ×０．１（Ｆ）以上であることを特徴とした請求項５から６に記載の半導体装置
【請求項８】
ｔは10^{-8}（秒）以下であることを特徴とした請求項７に記載の半導体装置。
【請求項９】
前記信号入力配線と前記低電位電源配線または前記高電位電源配線との容量は、前記低電位電源配線と前記高電位電源配線間の容量より小さい事を特徴とした請求項６から８に記載の半導体装置。
【請求項１０】
前記電源間保護回路又は信号電源間保護回路の少なくとも一つはダイオード素子を含み、前記ダイオード素子はその一端が低電位電源配線と高電位電源配線のいずれかに接続されてなる事を特徴とした請求項１から９に記載の半導体装置。
【請求項１１】
前記複数の半導体回路はｎチャネル型電界効果トランジスターである第一のトランジスターとｐチャネル型電界効果トランジスターである第二のトランジスターを含み、前記第一のトランジスターの少なくとも一部は前記低電位電源配線に接続されてなり、前記第二

のトランジスターの少なくとも一部は前記高電位電源配線に接続されてなる事を特徴とした請求項５から１０に記載の半導体装置。
【請求項１２】
前記第一のトランジスターおよび前記第二のトランジスターはポリシリコン薄膜を能動層としたトランジスターであり、前記基板は絶縁基板である事を特徴とした請求項１１に記載の半導体装置。
【請求項１３】
前記基板上にはマトリクス状に配列された複数のアクティブ素子が形成されてなり、前記複数の半導体回路の少なくとも一部は前記複数のアクティブ素子に駆動信号を入力するための駆動回路を構成してなる事を特徴とした請求項１から１２に記載の半導体装置。
【請求項１４】
前記内部保護回路は前記マトリクス状に配列された複数のアクティブ素子の４隅のうち、前記入力端子より遠い側の隅に配置されることを特徴とした請求項１３に記載の半導体装置。
【請求項１５】
請求項１から１４に記載の半導体装置が形成された第１の基板と、該第１の基板に対向する第２基板と、前記第１の基板と前記第２の基板の間に液晶層を封入することにより構成された表示装置。
【請求項１６】
請求項１から１４に記載の半導体装置上に有機ＥＬ素子を形成する事により構成された表示装置。
【請求項１７】
請求項１５から１６に記載の表示装置を用いた電子機器。

【書類名】明細書
【発明の名称】半導体装置、表示装置及び電子機器
【技術分野】
【０００１】
本発明は半導体装置、表示装置及び電子機器に関するものであり、特に駆動回路をアクティブマトリクス基板上に内蔵した表示装置に関するものである。
【背景技術】
【０００２】
半導体装置において、静電気あるいは各種ノイズ現象による意図しない高電圧が装置内に印加され、絶縁膜を破壊することによって復帰不能なダメージを受ける静電破壊（ＥＳＤ）対策は重要な課題であり、これを防止するための様々な保護回路が考案されている。例えば特許文献１、特許文献２などではダイオードを適宜組み合わせる事で配線に印加された異常電圧をＧＮＤなどに放電する回路が提案されている。しかし、通常の半導体装置は導電体であるシリコンウェハー上に形成するため、半導体装置内で帯電することは少なく、入力端子を通じて静電気が侵入したときの対策が主であり、入力端子と回路を構成する半導体素子の間、すなわち入力端子直後に保護回路を形成することで、入力端子から侵入した高電圧が素子へ伝播する事を防ぐような構成をとるのが一般的である。
【０００３】
一方、近年急速に普及している薄膜トランジスター（ＴＦＴ）などのアクティブ素子を用いた表示装置などでは絶縁基板上に装置が形成されているため、静電気により自身が帯電しやすく、製造工程中で静電破壊が起こりやすいという課題を有している。このため、例えばアクティブマトリクス回路の外周にガードリングまたはショートリングと称する帯電防止用の配線を形成するなどして静電気対策を施している。
【０００４】
最近になって、ポリシリコンを能動層としたポリシリコンＴＦＴを用い、表示装置の駆動回路を内蔵することで精細度向上・コスト低減・信頼性確保を実現した駆動回路内蔵型の表示装置が実用化され、普及している。このような装置においては、駆動回路の静電気対策はシリコンウェハー上の半導体で従来もちいられている手法をそのまま適用しているため、入力端子からの静電気を保護するための保護回路のみを内蔵し、アクティブマトリクス回路の静電保護には従来の駆動回路非内蔵型の表示装置の手法を用いている。以下、駆動回路の保護に関する従来技術の詳細について図１１を用いて説明する。
【０００５】
図１１は従来の技術によるポリシリコンＴＦＴを用いたＶＧＡ－ＬＣＤ用アクティブマトリクス基板のブロック図である。２０１－１～４８０がアクティブマトリクス回路の走査線であり、８００で示した走査線駆動回路により駆動される。２０２－１～１９２０がデータ線であり、各走査線とデータ線の交差部にはｎ型ＴＦＴよりなる画素トランジスター（４０１）、画素電極（４０２）が形成されて液晶素子を駆動するようになっている。
【０００６】
８０１－１～４８０は走査線駆動回路（８００）を構成する４８０段の走査線駆動ユニット回路で、ＣＭＯＳ回路により構成されている。具体的な走査線駆動ユニット回路（８０１－１～ｎ）の回路構成例としては例えば図５を参照のこと。
【０００７】
各走査線駆動ユニット回路（８０１－１～４８０）は低電位電源配線（７５０）及び高電位電源配線（７５１）に接続されており、これらを通じて電力を供給される。低電位電源配線（７５０）は低電位電源端子（６５０）に、高電位電源配線（７５１）は高電位電源端子（６５１）にそれぞれ接続されており、低電位電源端子（６５０）及び高電位電源端子（６５１）にはＦＰＣ等を介して電源ＩＣが接続され、それぞれ電位ＶＳ及び電位ＶＤの基準電位が供給される。ここでＶＳ＜ＶＤである。
【０００８】
さらに各走査線駆動ユニット回路（８０１－１～４８０）の動作に必要な信号（例えば

クロック信号）が信号配線（７０１，７０２）および信号端子（６０１，６０２）を通じて外部ＩＣより供給される。

【０００９】

ここで低電位電源端子（６５０）、高電位電源端子（６５１）および信号端子（６０１，６０２）を通じて静電気やノイズ電流が侵入し、各走査線駆動ユニット回路（８０１－１～４８０）を構成するＴＦＴが破壊されることを防ぐため、静電気保護回路（ＥＳＤ１～４）を各入力端子（６０１，６５０，６５１）から各走査線駆動ユニット回路（８０１－１～４８０）までの間に設ける。静電気保護回路（ＥＳＤ１～４）の具体的構成としては例えば特許文献１および特許文献２などがあげられる。

【００１０】

【特許文献１】特許第２８８４９４６号公報

【特許文献２】特許第３１４１５１１号公報

【発明の開示】

【発明が解決しようとする課題】

【００１１】

しかしながら、絶縁基板上の駆動回路はシリコンウェハー上の回路に比べ電荷が逃げにくく、帯電しやすい。加えて、表示装置の駆動回路をガラス基板上に内蔵する場合は一般的なシリコンウェハー上に製造するのＩＣに比べ回路面積が大きいためにこのような構成では入力端子より遠い配線上での静電気に対する保護が特に製造中の工程において十分でないという課題を有している。というのも、製造工程内では静電気が基板上の任意の位置に帯電する可能性があり、帯電した位置から静電気保護回路までの距離が長く、配線抵抗が高い場合には静電気保護回路が動作する前により手近な回路内のトランジスターを静電破壊してしまう場合があるためである。このような問題はＳＯＩ基板を用いた半導体装置の場合でも共通の課題となる。

【００１２】

また、絶縁基板の場合、製造工程完了後の完成品状態でも基板外部で強い静電気放電が起こった時に静電誘導により配線上に大きな電流が流れる事があり、このような場合にも端子より遠い場所の回路を破壊する可能性がある。

【００１３】

またさらに、本発明では回路を通じて多大な電流が配線上を流れた時に、配線上の電位が瞬間的に変動してしまうという課題についても対策を示すものである。

【課題を解決するための手段】

【００１４】

本発明は上記の問題点を解決するため、半導体回路を保護回路と入力端子の間に配置する事を提案する。より具体的かつ定量的な表現をすると、半導体回路と配線の接続部から入力端子までの配線に沿った電気抵抗が、保護回路と配線の接続部から入力端子までの配線に沿った電気抵抗よりも小さくなるように設置することを提案する。

【００１５】

従来技術のように入力端子近辺に設置した保護回路だけではなく、配線の入力端子に接続されていない部位に内部保護回路を設置することにより、静電気に対する保護が端子より離れた個所でも十分に得られるという効果を有する。

【００１６】

さらに、保護回路を配線上に複数設置し、半導体回路を保護回路の間に挟みこむようにして設置する事を提案する。これにより、入力端子からの静電気やノイズを防止すると共に、入力端子から遠い半導体回路も保護できる。また、複数の保護回路を概略一定の間隔で配置することにより、配線上に接続された半導体回路がまんべんなく保護できてより望ましい。

【００１７】

さらに本発明では、配線に低電位の電源配線と高電位の電源配線が含まれ、その両方に接続された電源間保護回路を有する事を提案する。このように構成すると、ダイオード素

子などにより容易に保護回路を形成できる上に、お互いが電源配線であるためにノイズの影響を受けにくい。また、電源配線は一般的に回路内で非常に長くなるため、他の配線に比べ静電保護が特に必要であり、効果は一層顕著である。これに加えて信号配線については電源配線との間に信号電源間保護回路を形成する事を提案する。信号線同士ではノイズの影響をうけやすいため、電源との間に保護回路を設置すると悪影響を低減できる。さらに、信号電源間保護回路の容量は電源間保護回路の容量に比べ小さくすることを提案する。このようにすることにより信号が電源線へ与える影響を最小限に出来る。

【００１８】

また、本発明では、低電位電源配線もしくは高電位電源配線に流れる最大電流をＩ（Ａ）、電源配線の電圧降下が発生する許容時間の上限をｔ（秒）とした時、保護回路における配線同士の容量成分が、Ｉ×ｔ×０．１（Ｆ）以上であることを特徴とする。ｔはポリシリコンＴＦＴにおける一般的な動作時間を考慮して10^{-8}（秒）以下であることが好ましい。このようにすることにより、回路に大きな電流が流れて外部からの供給が追いつかず、配線上で瞬間的な電圧変動が発生した時に、保護回路内の容量成分によってこれを低減する効果を有するものである。

【００１９】

さらに本発明では、電源間保護回路又は信号電源間保護回路はダイオード素子を含み、その一端が電源配線に接続されていることを提案する。このような構成により、静電気やノイズ電流の放電が容易に可能になり、保護性能が著しく向上する。

【００２０】

さらに本発明では、上で述べた発明内容をｎチャネル型電界効果トランジスター及びｐチャネル型電界効果トランジスターで構成されるいわゆるＣＭＯＳ型の半導体装置に適用する事を提案する。ＣＭＯＳ型の半導体装置では少なくとも２種類の基準電源を要するために電源配線が多くなるために本発明の効果は顕著である。特にポリシリコン薄膜トランジスターによるＣＭＯＳ型の半導体装置においては、基板が絶縁基板であるために保護回路が無い状態では帯電がおこりやすく、本発明の効果はますます顕著である。また特にＴＦＴ－ＬＣＤやＴＦＴ－ＯＬＥＤなどに用いられるアクティブマトリクスとその駆動回路を絶縁基板上に構成した場合、駆動回路がアクティブマトリクスを囲むように構成されるために大きくなり、それに伴って配線も長くなるために本発明の効果はますます顕著である。

【００２１】

さらに本発明では、アクティブマトリクスに本発明を応用する場合、アクティブマトリクスの４隅のうち、入力端子から遠い隅に内部保護回路を配置することを提案する。このような位置に配置する事で、アクティブマトリクスの周辺部サイズ（額縁）を大きくすることなく大きな保護回路を配置できるので都合がよい。

【００２２】

また、本発明の半導体装置を用いた表示装置及びその表示装置を搭載した電子機器は工程中の静電破壊が起こりにくいためにコスト的に有利であり、電源の電圧降下が起こりにくいために表示品位も高いという効果を有する。

【発明を実施するための最良の形態】

【００２３】

以下、本発明の実施形態を図面に基づいて説明する。

【実施例１】

【００２４】

図１は本発明の走査線駆動回路を用いた液晶表示装置を実現する第一の実施例での走査線駆動回路内蔵型のアクティブマトリクス基板の構成図である。アクティブマトリクス基板（１０１）上には４８０本の走査線（２０１－１～４８０）と１９２０本のデータ線（２０２－１～１９２０）が直交して形成されており、４８０本の容量線（２０３－１～４８０）は走査線（２０１－１～４８０）と並行かつ交互に配置されている。データ線（２０２－１～１９２０）はデータ線入力端子（３０２－１～１９２０）に接続されている。

容量線（２０３－１～４８０）は相互に短絡されてコモン電位入力端子（３０３）に接続される。対向導通部（３０４）もまた、コモン電位入力端子（３０３）に接続される。

【００２５】

走査線（２０１－ｎ）とデータ線（２０２－ｍ）の各交点にはＮチャネル型電界効果薄膜トランジスターよりなる画素スイッチング素子（４０１－ｎ－ｍ）が形成されており、そのゲート電極は走査線（２０１－ｎ）に、ソース・ドレイン電極はそれぞれデータ線（２０２－ｍ）と画素電極（４０２－ｎ－ｍ）に接続されている。画素電極（４０２－ｎ－ｍ）は容量線（２０３－ｎ）と補助容量コンデンサーを形成し、また液晶表示装置として組み立てられた際には液晶素子をはさんで対抗基板電極（ＣＯＭ）とやはりコンデンサーを形成する。

【００２６】

走査線（２０１－１～４８０）はアクティブマトリクス基板上にポリシリコン薄膜トランジスターを集積することで形成された走査線駆動回路（８００）に接続されて駆動信号を与えられる。ここで走査線駆動回路は走査線毎に接続された４８０個の走査線駆動ユニット回路（８０１－１～４８０）によって構成されている。本発明において、特許請求の範囲における半導体回路は走査線駆動回路（８００）である。また、特許請求の範囲における配線は、ＣＬＫ信号配線（７０１）、ＳＰ信号配線（７０２）、高電位電源配線（７５１）、低電位電源配線（７５０）などを示している。

【００２７】

走査線駆動回路（８００）にはＣＬＫ信号配線（７０１）、ＳＰ信号配線（７０２）、高電位電源配線（７５１）、低電位電源配線（７５０）が接続され、クロック・スタートパルス信号及び各電源電位が供給される。ここでＣＬＫ信号配線（７０１）、ＳＰ信号配線（７０２）、高電位電源配線（７５１）、低電位電源配線（７５０）はＣＬＫ信号端子（６０１）、高電位電源端子（６５１）、低電位電源端子（６５０）に接続され、これらの端子は外部ＩＣにＦＰＣ等を通じて接続されることで所望の信号・電源電位を供給される。

【００２８】

ＣＬＫ信号端子（６０１）、ＳＰ信号端子（６０２）、高電位電源端子（６５１）、低電位電源信号端子（６５０）とＣＬＫ信号配線（７０１）、ＳＰ信号配線（７０２）、高電位電源配線（７５１）、低電位電源配線（７５０）の間の接続配線には第一から第四の保護回路（ＥＳＤ１～４）が接続され、各端子（６０１，６０２，６５１，６５０）から静電気やノイズ電流が流れた時に走査線駆動回路（８００）内のＴＦＴが破壊される事を防止する。

【００２９】

さらにＣＬＫ信号配線（７０１）、高電位電源配線（７５１）、低電位電源配線（７５０）上のＣＬＫ信号端子（６０１）、高電位電源端子（６５１）、低電位電源信号端子（６５０）からみて走査線駆動回路（８００）を隔てた逆側の末端にも第五から第七の保護回路（ＥＳＤ１１～１３）が配置される。これにより、走査線駆動ユニット回路（８０１－ｎ）のうち、端子から遠い位置にあるユニット（例えばｎ＝１など）がアクティブマトリクス基板製造中に静電気で破壊されるような事態を防止できる。また、第五から第七の保護回路（ＥＳＤ１１～１３）はアクティブマトリクス基板のコーナー部、特に入力端子とは逆の隅に配置すれば基板面積を大きくする事無く配置可能である。

【００３０】

図４は保護回路（ＥＳＤ１～１３）の具体的な回路構成例である。ｐ型トランジスター（５０４）のソース電極及びゲート電極が高電位電源ＶＨに、ドレイン電極が保護される配線に接続され、ｎ型トランジスター（５０２）のソース電極及びゲート電極が低電位電源ＶＬに、ドレイン電極が保護される配線に接続されている。ここで保護される配線に与えられる信号レベルはＶＨ以下ＶＬ以上でなくてはならない。静電気等により、保護される電源の電位がＶＨ～ＶＬの範囲外に触れるとｎ型トランジスター（５０２）又はｐ型トランジスター（５０４）がＯＮし、異常電流を基準電位ＶＨ配線または基準電位ＶＬ配線

へ逃す。また、保護抵抗（５０３）により、配線の電位が急速に上昇してｎ型トランジスター（５０２）又はｐ型トランジスター（５０４）が破壊されることを防止できる。ここでＶＨ及びＶＬは回路内で最も高い電源と低い電源を使うのが一般的であるが、ＶＨ＝ＶＤ、ＶＬ＝ＶＳでも良い。

【００３１】

なお、ここでは保護回路（ＥＳＤ１～１３）は同一の構成としたが、無論おのおのの保護回路はその必要性に応じて別の回路構成であっても構わない。特に内部の保護回路（ＥＳＤ１１～１３）に対し、入力部の保護回路（ＥＳＤ１～４）は比較的高い保護性能が要求される。このため、例えば第一の保護回路（ＥＳＤ１）は第五の保護回路（ＥＳＤ１１）より高い保護性能を有した回路構成とするとよく、具体的にはｎ型トランジスター（５０２）およびｐ型トランジスター（５０４）のチャネル幅を第一の保護回路（ＥＳＤ１）の方が大きいようにすれば良い。

【００３２】

図５は走査線駆動ユニット回路（８０１－１～４８０）の構成例であり、クロックインバーター２つを用いたスタティック型シフトレジスタとＮＡＮＤ回路、ＮＯＴ回路を組み合わせた構成になっている。なお、ｎ段目（ｎ＜４８０）の走査線駆動ユニット回路（８０１－ｎ）のＯＵＴ端子はｎ－１段目の走査線駆動ユニット回路（８０１－ｎ－１）のＩＮ端子に接続され、４８０段目の走査線駆動ユニット回路（８０１－４８０）のＩＮ端子はＳＰ信号配線（７０２）へ接続される。

【００３３】

図６は第一の実施例を示した透過型液晶表示装置の斜視構成図（一部断面図）である。図１に示したアクティブマトリクス基板（１０１）と、カラーフィルター上にＩＴＯを成膜することでコモン電極を形成した対抗基板（９０１）をシール材（９２０）により貼り合わせ、その中にネマティック液晶材料（９１０）を封入している。また、アクティブマトリクス基板（１０１）上の対向導通部（３０４）には導通材が配置され、対抗基板（９０１）のコモン電極と短絡されている。

【００３４】

データ線入力端子（３０２－１～１９２０）、コモン電位入力端子（３０３）、ＣＬＫ信号端子（６０１）、ＳＰ信号端子（６０２）、高電位電源端子（６５１）、低電位電源端子（６５０）は端子に実装されたＦＰＣ（９３０）を通じて１ないし複数の外部ＩＣ（９４０）に接続され、必要な電気信号・電位を供給される。

【００３５】

さらにアクティブマトリクス基板の外側には上偏向板（９５１）を、対抗基板の外側には下偏向板（９５２）を配置し、互いの偏光方向が直行するよう（クロスニコル）に配置する。さらに偏向板下にバックライト（９６０）を取り付けて完成する。バックライト（９６０）は冷陰極管に導光板や散乱板をとりつけたものでも良いし、ＥＬ素子によって全面発光するユニットでもよい。図示しないが、さらに必要に応じ、周囲を外殻で覆うあるいは上偏向板のさらに上に保護用のガラスやアクリル版を取り付けても良い。

【００３６】

この液晶表示装置は従来のものに比べ、製造工程中あるいは完成後の静電気等による静電破壊が発生しにくいため、歩留りが良くかつ信頼性が高い。

【実施例２】

【００３７】

図２は本発明の走査線駆動回路を用いた液晶表示装置を実現する第二の実施例での駆動回路を示す構成図である。本図は図１の鎖線Ａ枠内に相当する図である。

【００３８】

本実施例では端子（６０１，６５０，６５１）から走査線駆動回路（８００）までの間の入力部保護回路（ＥＳＤ１～３）や入力端子（６０１，６５０，６５１）からみて駆動回路（８００）を隔てた末端の内部保護回路（ＥＳＤ１１～１３）のみならず、駆動回路（８００）の中間段である２４０段目のユニット駆動回路（８０１－２４０）と２４１段

目のユニット駆動回路（８０１－２４１）の間にも第八から第十の保護回路（ＥＳＤ２１～２３）を設けている。これにより、端子近辺及び末端いずれからも遠い中間段（ｎ＝２４０）近辺での静電気破壊を防止できる。本実施例では中間段のみに保護回路を追加しているが、回路の規模・大きさ等に応じ、途中にいれる保護回路の数を増やしていってもよい。例えば本実施例の場所に加え、１２０段目（８０１－１２０）と１２１段目（８０１－１２１）の間及び３６０段目（８０１－３６０）と３６１段目（８０１－３６１）の間にも保護回路をいれればさらに好ましく、回路面積さえ問題なければ、全ての段の間に全て保護回路をいれれば最も望ましい。ただし、いずれのケースでも保護回路をいれる間隔はほぼ一定であるべきであり、さもないと間隔が広くなっている個所でのみ静電破壊が起こりやすくなる。

【００３９】

上記に記載の個所以外でのアクティブマトリクス基板の構成、保護回路や駆動回路の詳細などは第二の実施例は第一の実施例と全く同様であり、図２のような回路を含むアクティブマトリクス基板を用いた液晶表示装置も第一の実施例と同じ構成で差支えないので説明を省略する。

【実施例３】

【００４０】

図３は本発明の走査線駆動回路を用いた液晶表示装置を実現する第一の実施例での走査線駆動回路内蔵型のアクティブマトリクス基板の構成図である。

【００４１】

本実施例では第一および第二の実施例と異なり、走査線駆動回路（８００）に与えられるＣＬＫ信号、ＳＰ信号がＣＬＫ信号端子（６０１）、ＳＰ信号端子（６０２）から直接入力されるのではなく、バッファー回路（８１０－１、８１０－２）で一旦、駆動能力が増幅されてから走査線駆動回路８００に入力される構成となっている。このような構成により、外部ＩＣの信号駆動能力がさほど高くなくても大面積のパネルでも信号を大きな遅延無く駆動できる。

【００４２】

図７は第三の実施例におけるバッファー回路（８１０－１、８１０－２）の具体的な回路構成である。第一のＮＯＴ回路（８２１）及び第二のＮＯＴ回路（８２２）を二段直列に接続した構成になっており、第一のＮＯＴ回路（８２１）を構成するトランジスターより第二のＮＯＴ回路（８２２）を構成するトランジスターの方がチャネル幅（Ｗ）が大きく、例えば第一のＮＯＴ回路（８２１）のＷ＝２５０μｍ、第二のＮＯＴ回路（８２２）のＷ＝１０００μｍのように設定する。電源配線８５０は図３の低電位電源配線７５０より分岐している枝配線であり、電源配線８５１は図３の高電位電源配線７５１より分岐している枝配線であって、白丸が分岐点方向を示しているが、バッファー回路（８１０－１、８１０－２）を挟んで逆側（すなわち枝配線８５０、８５１の末端）には第十一及び第十二の保護回路（ＥＳＤ４１、ＥＳＤ４２）が配置されている。

【００４３】

このような構成により、低電位電源配線（７５０）上の第一の保護回路（ＥＳＤ１１）と第十一の保護回路（ＥＳＤ４１）に挟まれた部分および高電位電源配線（７５１）上の第二の保護回路（ＥＳＤ１２）と第十二の保護回路（ＥＳＤ４２）に挟まれた部分とバッファー回路（８１０－１、８１０－２）が接続されている事になり、第一の保護回路（ＥＳＤ１１）しか無い場合に比べ、バッファー回路（８１０－１、８１０－２）内に静電気が帯電した場合の保護性能が著しく向上する。

【００４４】

図８は第三の実施例におけるバッファー回路（８１０－１、８１０－２）の具体的な回路構成の別の例である。図７の構成と比較すると、低電位電源配線（７５０）及び高電位電源配線（７５１）上の第一のＮＯＴ回路（８２１）の接続点と第二のＮＯＴ回路（８２２）の接続点を結ぶ線上に第十三の保護回路（ＥＳＤ５１）および第十四の保護回路（ＥＳＤ５１）が追加されている。その他の構成については図７と同様である。このように回

路と回路の中間点にも内部保護回路があることで、さらに保護性能は向上する。

【００４５】

また、本実施例では電源の電圧変動を防止するという別の効果も有する。電源配線の抵抗は有限であり、従って瞬間的に大きな電流を相補型回路で消費する場合に電源配線は部分的かつ瞬間的にではあるが電圧が変動する。本実施例でいうと、第二のＮＯＴ回路（８２２）のチャネル幅はＷ＝１０００μｍと非常に大きく、入力信号が反転した際に非常に大きな電流が瞬間的に流れて電源の電位が変動する（その時間は第二のＮＯＴ回路（８２２）の出力端子が接続されている配線の容量値による）。

【００４６】

図１０は図７、図８の構成のバッファー回路での電位の時間変動をシミュレーションした結果であり、これを用いて具体的に説明を行う。グラフ８８０は第一のＮＯＴ回路（８２１）から出力され、第二のＮＯＴ回路（８２２）に入力される信号波形で、電位がＶＳからＶＤへと変化している。この時、第二のＮＯＴ回路（８２２）を構成するｎ型トランジスターがＯＮし、出力端子の電位をＶＳに書き込む。この際、低電位電源配線（８５０）上に大きな電流が流れ、電圧勾配が生じて瞬間的に電位が少し上がる。これを防止するためには低電位電源配線（８５０）の配線幅を太くすれば良いが、回路面積の関係で制限される場合がある。低電位電源配線（８５０）がある配線幅に固定され、特に対策を講じなかった場合の低電位電源配線（８５０）の第二のＮＯＴ回路（８２２）近傍での電位を示したグラフが８８１であり、瞬間的に電圧が上昇していることがわかる。

【００４７】

このような現象が生じると、バッファー回路の駆動能力が低下するのみならず、低電位電源配線（８５０）に繋がった別の回路に悪影響を及ぼすことがある。すなわち、低電位電源配線（８５０）を通じてグラフ８８１のような電圧降下が他の回路にも伝わり、最悪の場合誤作動を引き起こし、アナログ回路の場合は出力精度へ影響を及ぼす。このような問題はシリコンウェハー上の回路に比べ回路面積が大きくなる絶縁基板上のＴＦＴ回路、特に表示装置の駆動回路ではより顕著となる。

【００４８】

次にグラフ８８２は低電位電源配線に適当なる容量素子を加えた場合の結果である。この場合、瞬間的に流れる電流はある程度まで容量素子から供給されるため、電圧降下はより少なくて済む。すなわち、電圧降下を低減するためには容量素子を電源配線に加えればよい。容量素子の容量が大きいほど電圧降下を低減する効果が高いが、筆者の検討した結果では、電源配線に流れる最大電流をＩ（Ａ）、電圧降下が発生する許容時間をｔ（秒）とした時、Ｉ×ｔ×０．１（Ｆ）以上の容量素子をおけば電圧降下に効果があり、これ以下では大きな効果がみられなかった。ここで電圧降下が発生する許容時間ｔは論理回路の動作最大速度や、アナログ回路のサンプリング時間により決定される。一般的にポリシリコンを用いたＴＦＴでは動作速度はさほど高くなく、せいぜい数１０ＭＨｚくらいでの動作が上限である。すなわち、１０ｎ秒以下の電源電圧変動はほとんど問題が無い。また、電源を流れる最大電流とは、回路の最大瞬間消費電流と等しい。

【００４９】

従って、回路の消費する最大電流をＩ（Ａ）、電圧降下が発生する許容時間をｔ（秒）とした時、Ｉ×ｔ×０．１（Ｆ）以上の容量を電源に付加すれば電圧降下低減に効果があり、この時、$t \leqq 10^{-8}$（秒）とすれば良い。また、容量を接続する相手としては電位が変動しない、別の電源配線である事が望ましい。しかしながら、このような容量を配置すると回路面積が増大する。そこで、本実施例のように保護回路を電源配線上に複数個配置すると、保護回路上の容量成分により、保護される電源配線と保護回路内の基準電位電源配線（ＶＨ，ＶＬ）との間に容量が出来る。この場合、回路は保護回路としても電源電位変動対策としても機能するから、回路面積の面で著しく有利である。

【００５０】

このような電源電位変動低減降下を期待する場合、消費電流の大きな回路の近傍に保護回路を設ける必要があり、さもないと消費電流の大きな回路から保護回路までの電源配線

抵抗によってやはり電圧変動が発生してしまう。具体的には消費電流の大きな回路から保護回路までの電源配線に沿った距離（Ｘ）が消費電流の大きな回路から入力端子までの電源配線に沿った距離（Ｙ）より小さくなるようにすべきである。

【００５１】

第一～二、第十一～十四の保護回路（ＥＳＤ１～２，１１～１４）の具体的構成は図４又は図９のようにすればよい。図４の回路構成の説明については第一の実施例と同様であるので省略するが、この構成でもトランジスターのゲートードレイン容量成分により保護される配線と高電位電源ＶＨ及び低電位電源ＶＬの間で容量が付加される。図９の構成では図４の構成に比べて第一の容量（５０５）及び第二の容量（５０６）を追加することで、強い電圧が瞬間的に印加された時に保護抵抗（５０３）との組み合わせてＣＲ回路として動作してｎ型トランジスター（５０２）及びｐ型トランジスター（５０４）が破壊される事を防止する機能が向上しており、かつ保護される配線と高電位電源ＶＨ及び低電位電源ＶＬの容量を第一の容量（５０５）及び第二の容量（５０６）によって調整可能であるため、電源電圧降下対策としてより効果のある構成となっている。

【００５２】

またこのような構成にする際には、低電位電源配線（７５０）及び高電位電源配線（７５１）に接続される保護回路（ＥＳＤ１，２，１１，１２）の容量は信号配線（７０１，７０２）に接続される保護回路（ＥＳＤ３，４，１３）の容量より小さくするべきである。というのも、信号配線は電位が変動するのであまり信号配線との容量が大きいと保護回路で信号線と接続される基準電源配線との間にクロストークが生じためである。具体的には、保護回路の構成が図９のようであるならば、低電位電源配線（７５０）及び高電位電源配線（７５１）に接続される保護回路（ＥＳＤ１，２，１１，１２）の第一の容量（５０５）・第二の容量（５０６）を信号配線（７０１，７０２）に接続される保護回路（ＥＳＤ３，４，１３）の第一の容量（５０５）・第二の容量（５０６）より大きくなるように設定すれば良い。

【００５３】

本実施例で述べたようなバッファー回路以外の相補型回路、例えばデータ線駆動回路・ＤＡＣ回路・電源回路・レベルシフト回路・メモリー回路などをアクティブマトリクス基板上に内蔵する場合にも同様に枝電源配線の末端及び途中に保護回路を設けることが望ましく、全ての回路が保護回路と保護回路の間の電源配線上に置かれていればなお好ましい。また、消費電流が大きな回路前後段に一定以上の容量を有する保護回路を設置すれば電源ノイズ低減の観点からも好ましく、具体的には回路の消費電流をＩ、電圧降下が発生する許容時間ｔ（典型的にはｔ≦10^{-8}（秒））とすると、Ｉ×ｔ×０．１（Ｆ）以上の容量を目安とすればよい。

【００５４】

上記に記載の個所以外のアクティブマトリクス基板の構成、保護回路や駆動回路の詳細などは第三の実施例は第一の実施例と全く同様であり、図３のようなアクティブマトリクス基板を用いた液晶表示装置も第一の実施例と同じ構成で差支えないので説明を省略する。

【００５５】

また、実施例１では、図４の保護回路のみにより説明したが、図９の保護回路を設けることにより、実施例３と同様の効果を得ることができる。

【産業上の利用可能性】

【００５６】

本発明は前述の実施の形態に限定されるものではなく、データ線駆動回路やＤＡＣ、電源回路などを内蔵したアクティブマトリクス基板を使用した液晶表示装置でも構わない。この場合、本発明の内容を各回路にそれぞれ適用しても構わないし、レイアウト等の問題があれば一部の回路のみ適用しても良い。走査線駆動回路に適用する場合でも、実施例のようなシフトレジスタ型だけでなく、各種の順次選択回路でも良い。

【００５７】

また、保護回路として実施例及び先行例のような構成のみならず、今まで提案された各種保護回路のうち、どのような構成を用いても問題ない。

【００５８】

また、トランジスターとしてポリシリコンでなくアモルファスシリコン薄膜トランジスターを用いてもよい。また、絶縁基板上に薄膜トランジスターを形成するのではなく、結晶シリコンウェハー上に画素スイッチング素子や駆動回路を作りこんだアクティブマトリクス基板でも良い。

【００５９】

また、液晶表示装置として実施例のような透過型で無く反射型や半透過型としてもよいし、直視型で無く投影用のライトバルブとしてもよい。さらに実施例のようにノーマリー・ホワイトモードのみならず、ノーマリー・ブラックモードを使用してもよい。特にこの場合は液晶の配向モードとして垂直配向モードあるいは横電界スイッチングモードにしてもよい。

【図面の簡単な説明】

【００６０】

【図１】本発明の第一の実施例を説明するためのアクティブマトリクス基板構成図。

【図２】本発明の第二の実施例を説明するための走査線駆動回路図。

【図３】本発明の第三の実施例を説明するためのアクティブマトリクス基板構成図。

【図４】本発明の実施例を説明するための保護回路図。

【図５】本発明の実施例を説明するための走査線駆動ユニット回路図。

【図６】本発明の第一の実施例を説明するための液晶表示装置の斜視図（一部断面図）。

【図７】本発明の第三の実施例を説明するためのバッファ回路図。

【図８】本発明の第三の実施例の別の実施形態を説明するためのバッファ回路図。

【図９】本発明の第三の実施例を説明するための保護回路図。

【図１０】本発明の第三の実施例を説明するための基準電位変動をシミュレーションした結果のグラフ。

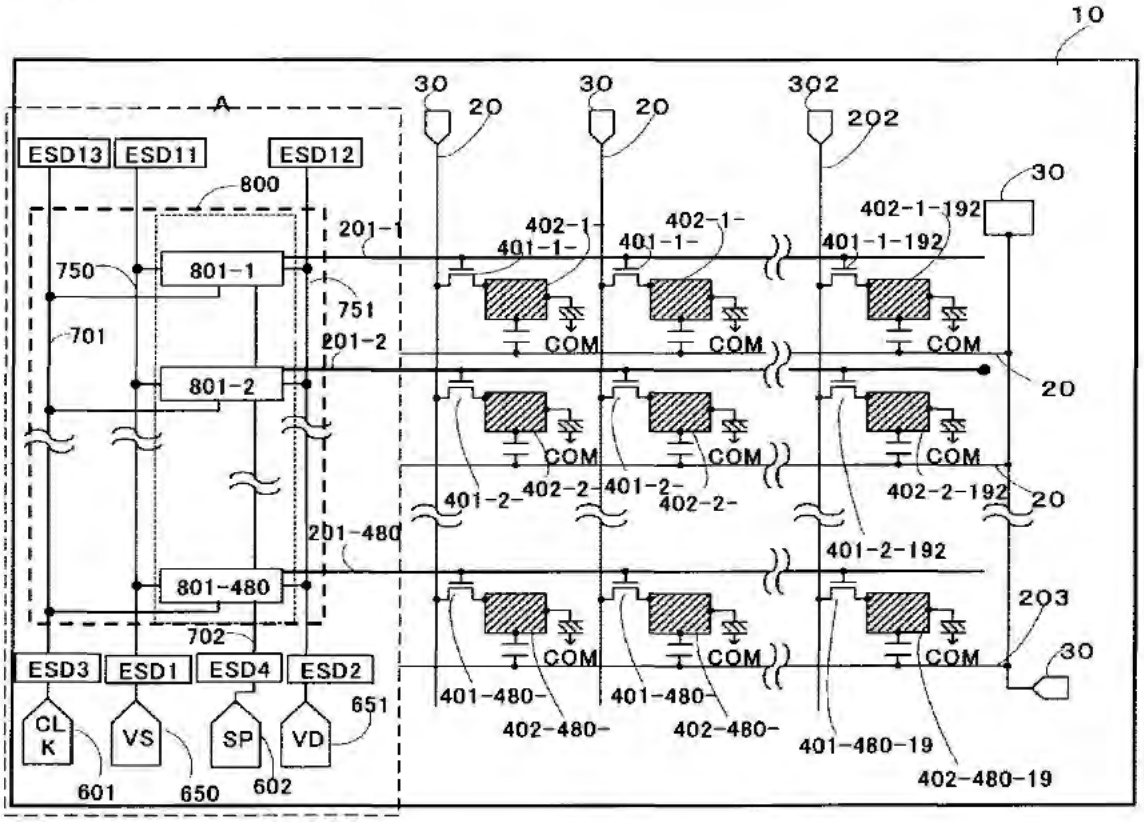
【図１１】従来例を説明するためのアクティブマトリクス基板構成図。

【符号の説明】

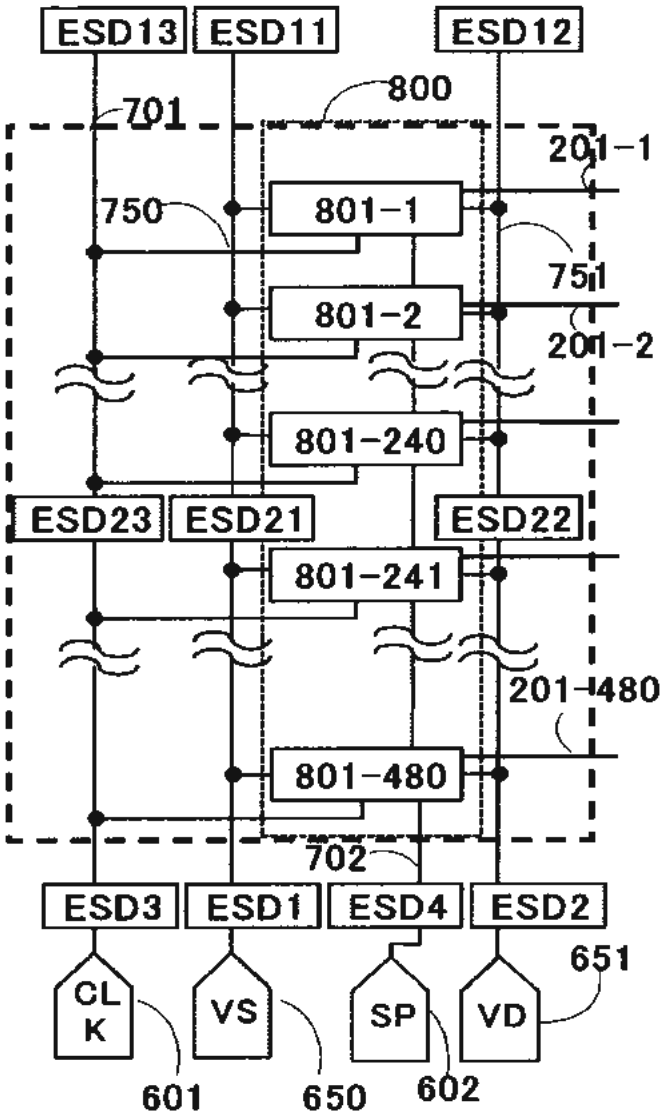
【００６１】

１０１：アクティブマトリクス基板
２０１－１～４８０：走査線１～４８０
２０２－１～１９２０：データ線１～１９２０
ＥＳＤ１～４：第一～第四の保護回路
ＥＳＤ１１～１３：第五～第七の保護回路
ＥＳＤ２１～２３：第八～第十の保護回路
８００：走査線駆動回路
８０１－１～４８０：走査線駆動ユニット回路

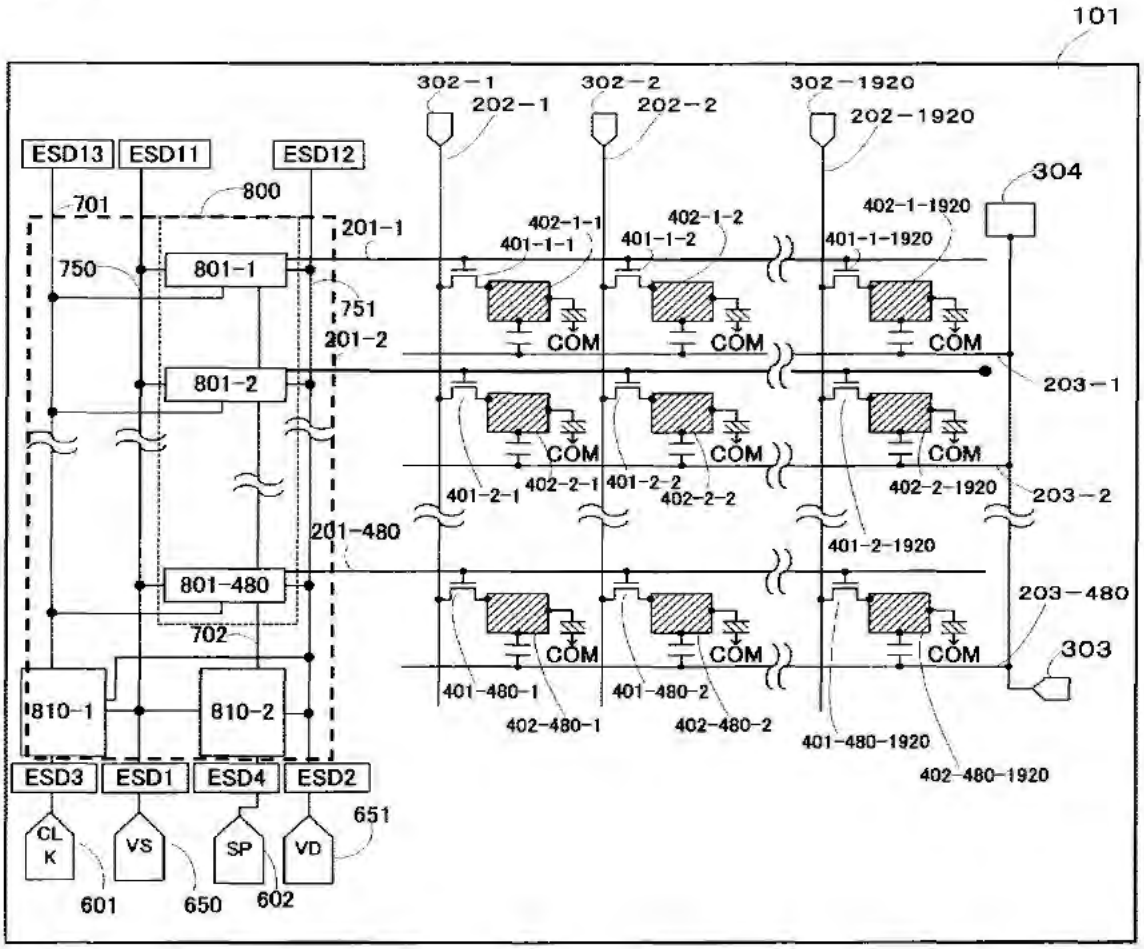
【書類名】図面
【図１】


10
A
30
20
302
202
ESD13
ESD11
ESD12
800
201-1
750
801-1
751
701
201-2
801-2
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602
402-1-
401-1-
402-1-192
401-1-192
COM
20
401-2-
402-2-
402-2-192
401-2-192
203
401-480-
402-480-
401-480-19
402-480-19
30

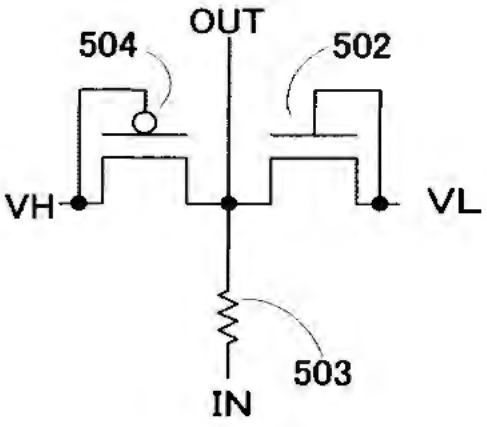
【図２】


ESD13
ESD11
ESD12
701
800
201-1
750
801-1
751
801-2
201-2
801-240
ESD23
ESD21
ESD22
801-241
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
651
CL
K
VS
SP
VD
601
650
602

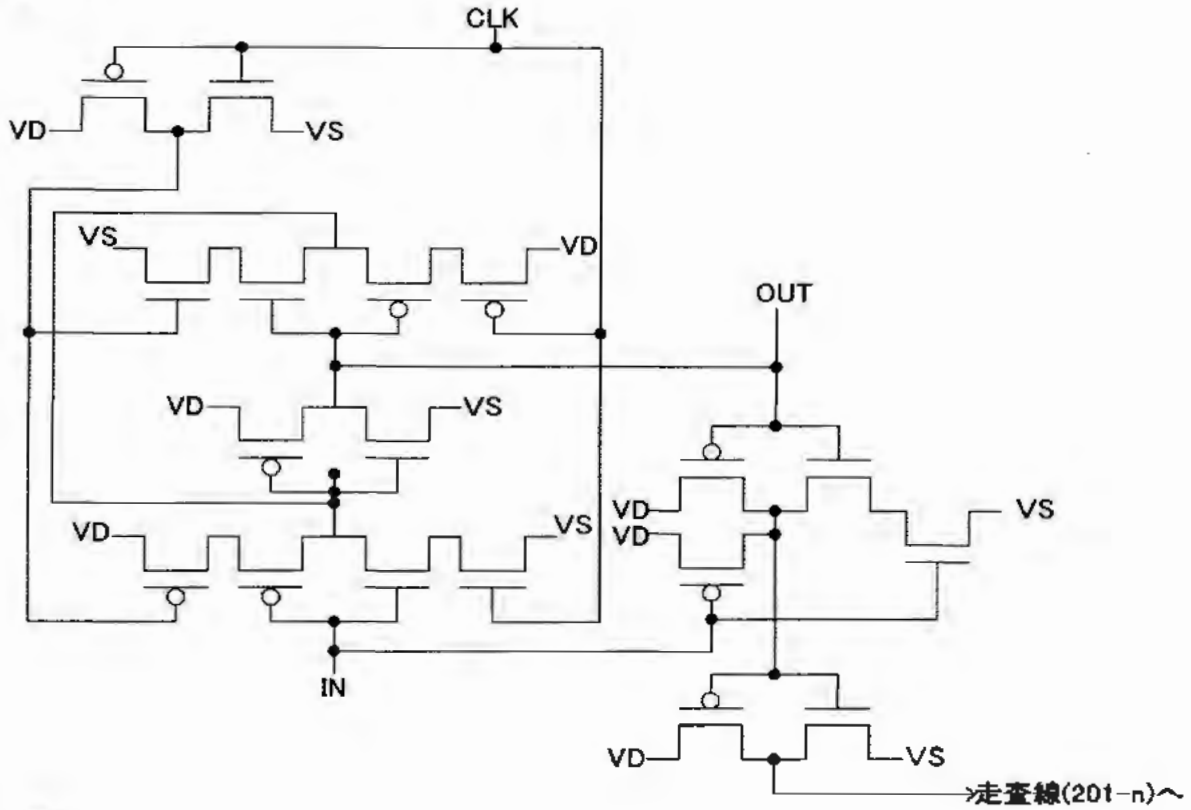
【図３】


101
302－1
202－1
302－2
202－2
302－1920
202－1920
304
ESD13
ESD11
ESD12
800
701
201－1
750
801－1
751
201－2
801－2
801－480
702
810－1
810－2
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602
402－1－1
401－1－1
402－1－2
401－1－2
402－1－1920
401－1－1920
COM
203－1
203－2
203－480
303
401－2－1
402－2－1
401－2－2
402－2－2
401－2－1920
402－2－1920
401－480－1
402－480－1
401－480－2
402－480－2
401－480－1920
402－480－1920

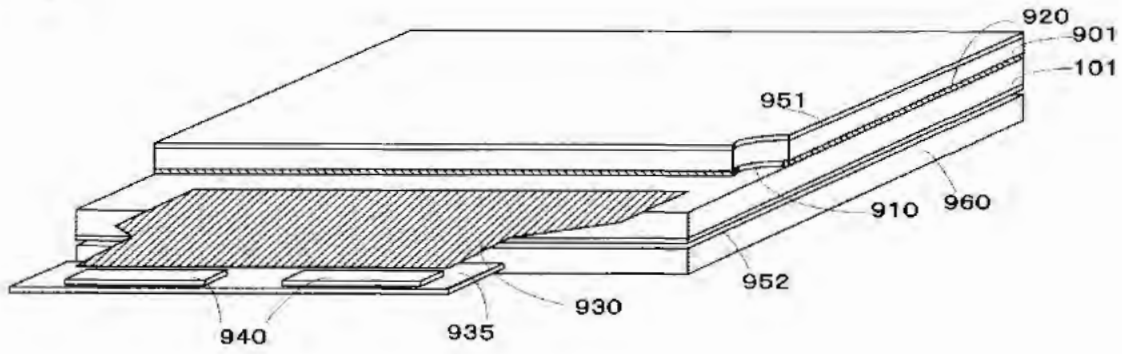
【図４】


OUT
504
502
VH
VL
503
IN

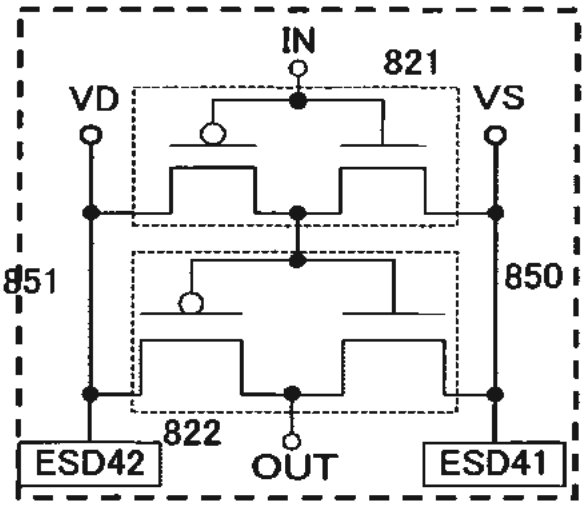
【図５】


CLK
VD
VS
VS
VD
OUT
VD
VS
VD
VS
VD
VD
VS
IN
VD
VS
走査線(201−n)へ

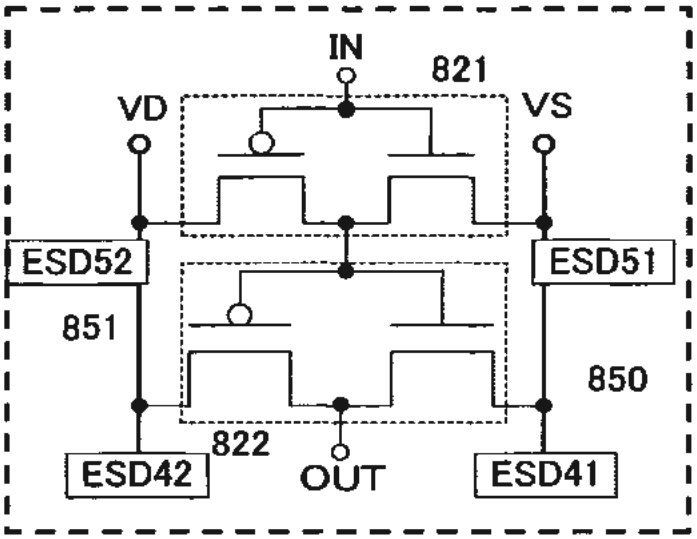
【図６】


920
901
101
951
910
960
952
930
940
935

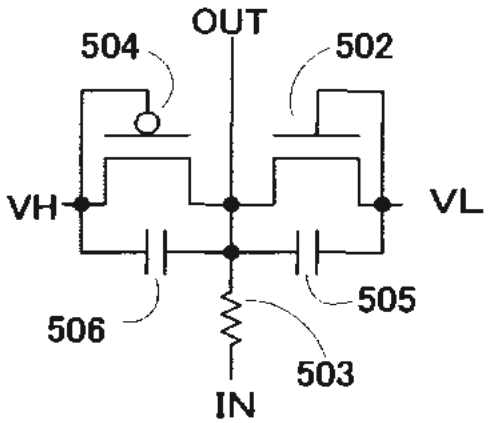
【図７】


IN
821
VD
VS
851
850
822
ESD42
OUT
ESD41

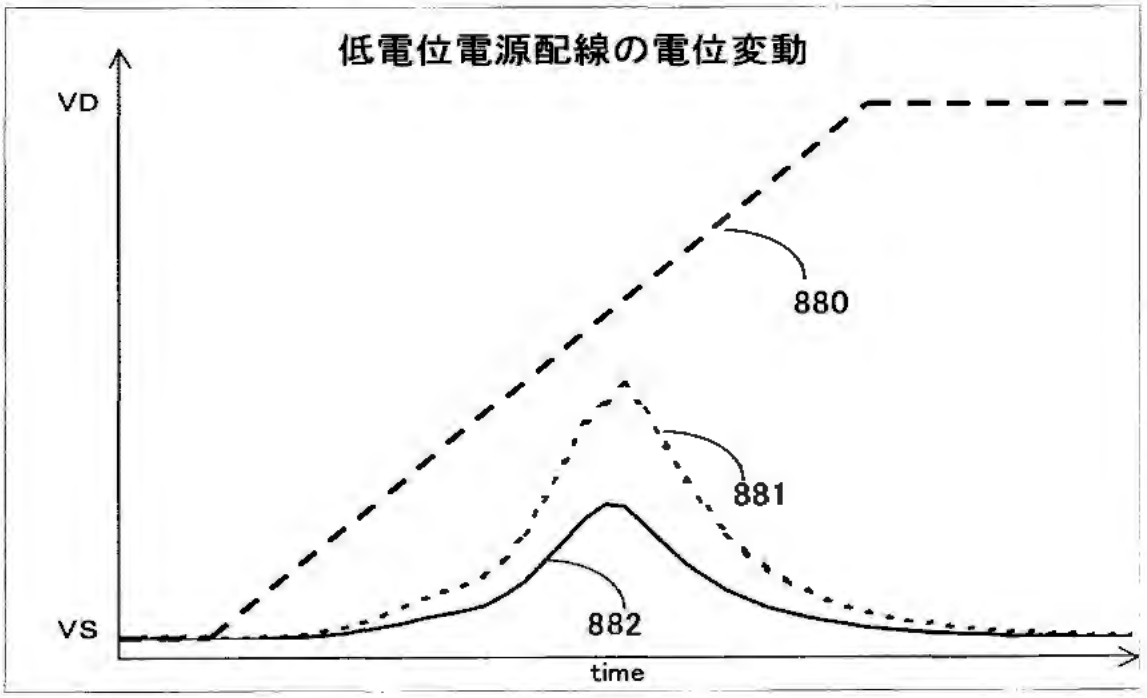
【図８】


IN
821
VD
VS
ESD52
ESD51
851
850
822
ESD42
OUT
ESD41

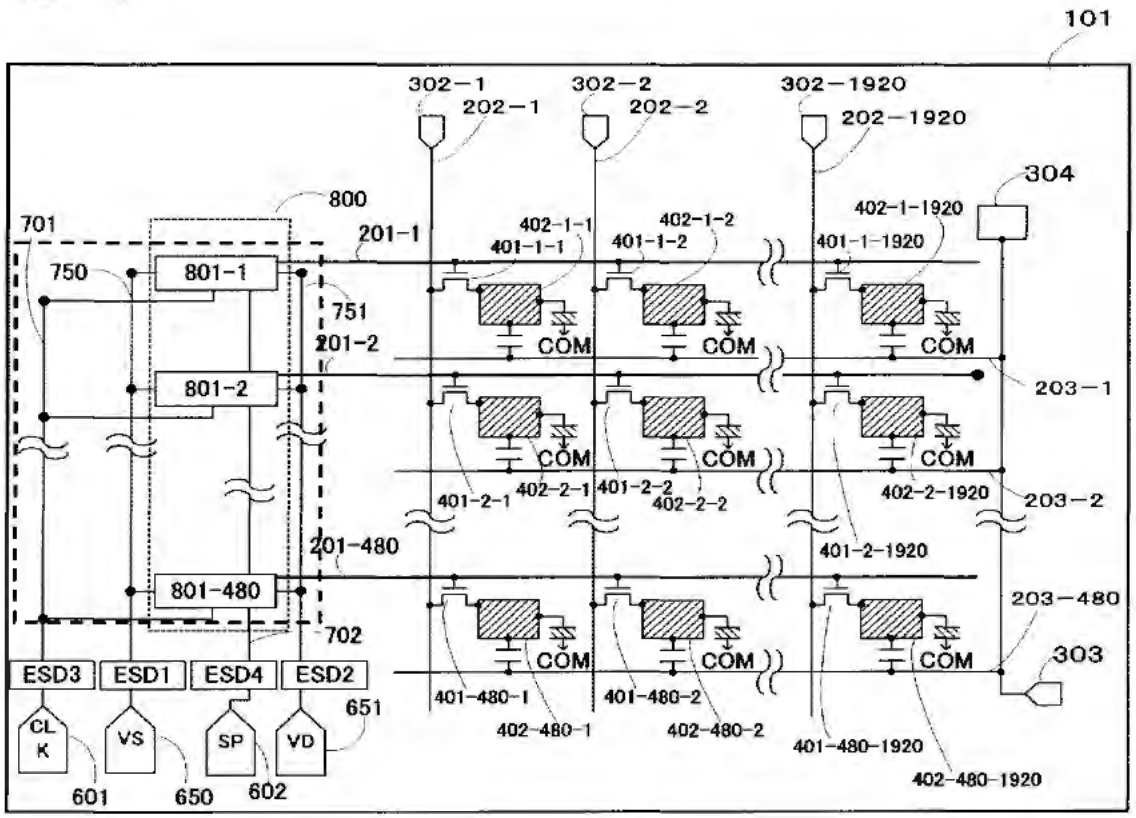
【図９】


OUT
504
502
VH
VL
505
506
503
IN

【図１０】


低電位電源配線の電位変動
VD
VS
880
881
882
time

【図１１】


101
302−1
302−2
302−1920
202−1
202−2
202−1920
304
800
701
201−1
402−1−1
401−1−1
402−1−2
401−1−2
402−1−1920
401−1−1920
750
801−1
751
201−2
COM
203−1
801−2
401−2−1
402−2−1
401−2−2
402−2−2
402−2−1920
203−2
201−480
401−2−1920
801−480
203−480
702
303
ESD3
ESD1
ESD4
ESD2
651
401−480−1
402−480−1
401−480−2
402−480−2
401−480−1920
402−480−1920
CL K
VS
SP
VD
601
650
602

【書類名】要約書
【要約】
【課題】駆動回路内蔵表示装置における静電破壊を防止する。
【解決手段】保護回路を入力端子部だけでなく、回路中あるいは配線末端にも配置する。あるいは入力端子直後と配線末端にそれぞれ保護回路を設置し、その間に回路を挟む。さらに消費電流の大きな回路の周囲に保護回路を設置する。
【選択図】　　図２

【書類名】　　手続補正書
【整理番号】　　J011113701
【提出日】　　平成20年 3月10日
【あて先】　　特許庁長官殿
【事件の表示】
　【出願番号】　　特願2004-198040
【補正をする者】
　【識別番号】　　000002369
　【氏名又は名称】　セイコーエプソン株式会社
【代理人】
　【識別番号】　　100125689
　【弁理士】
　【氏名又は名称】　大林　章
　【電話番号】　　03-3518-8058
【発送番号】　　003049
【手続補正1】
　【補正対象書類名】　特許請求の範囲
　【補正対象項目名】　全文
　【補正方法】　　変更
　【補正の内容】
　　【書類名】特許請求の範囲
　　【請求項１】
　電気信号が外部から供給される第１端部と電気信号が外部から供給されない第２端部とにわたる配線と、
　前記配線に接続された半導体回路と、
　前記配線のうち前記半導体回路と前記第１端部との間に配置されて前記半導体回路を保護する第１保護回路と、
　前記配線のうち前記半導体回路と前記第２端部との間に配置されて前記半導体回路を保護する第２保護回路と
　を具備する半導体装置。
　　【請求項２】
　前記配線に複数の半導体回路が接続され、
　前記配線のうち前記各半導体回路の間に配置されて前記複数の半導体回路を保護する第３保護回路
　を具備する請求項１の半導体装置。
　　【請求項３】
　前記配線は、前記半導体回路に電源電位を供給する低電位電源配線または高電位電源配線である
　請求項１または請求項２の半導体装置。
　　【請求項４】
　前記配線は、前記半導体回路に信号を伝達する信号入力配線である
　請求項１または請求項２の半導体装置。
　　【請求項５】
　前記半導体回路が配置された基板を具備し、
　前記配線は、前記基板の周縁に沿うように当該基板の第１隅部から第２隅部にわたって形成され、
　前記第１保護回路は、前記基板の前記第１隅部に配置され、
　前記第２保護回路は、前記基板の前記第２隅部に配置される
　請求項１から請求項４の何れかの半導体装置。
　　【請求項６】

請求項１から請求項５の何れかの半導体装置を具備する表示装置。
【請求項７】
請求項６の表示装置を具備する電子機器。

【手続補正2】
【補正対象書類名】　明細書
【補正対象項目名】　００１４
【補正方法】　変更
【補正の内容】
【００１４】
本発明に係る半導体装置は、電気信号が外部から供給される第１端部と電気信号が外部から供給されない第２端部とにわたる配線と、配線に接続された半導体回路と、配線のうち半導体回路と第１端部との間に配置されて半導体回路を保護する第１保護回路と、配線のうち半導体回路と第２端部との間に配置されて半導体回路を保護する第２保護回路とを具備する。

【手続補正3】
【補正対象書類名】　明細書
【補正対象項目名】　００１５
【補正方法】　変更
【補正の内容】
【００１５】
電気信号が外部から供給される第１端部の近辺に設置した第１保護回路だけではなく、配線の電気信号が外部から供給されない第２端部に第２保護回路を設置することにより、静電気に対する保護が、電気信号が外部から供給される第１端部から離れた個所でも十分に得られるという効果を有する。

【手続補正4】
【補正対象書類名】　明細書
【補正対象項目名】　００１６
【補正方法】　変更
【補正の内容】
【００１６】
さらに、配線に複数の半導体回路が接続され、配線のうち各半導体回路の間に配置されて複数の半導体回路を保護する第３保護回路を具備する構成を提案する。これにより、入力端子からの静電気やノイズを防止すると共に、入力端子から遠い半導体回路も保護できる。また、複数の保護回路を概略一定の間隔で配置することにより、配線上に接続された半導体回路がまんべんなく保護できてより望ましい。

【手続補正5】
【補正対象書類名】　明細書
【補正対象項目名】　００１７
【補正方法】　変更
【補正の内容】
【００１７】
本発明の好適な態様において、配線は、半導体回路に電源電位を供給する低電位電源配線または高電位電源配線、あるいは、半導体回路に信号を伝達する信号入力配線である。

【手続補正6】
【補正対象書類名】　明細書
【補正対象項目名】　００１９
【補正方法】　変更
【補正の内容】
【００１９】
さらに本発明では、保護回路はダイオード素子を含み、その一端が電源配線に接続されていることを提案する。このような構成により、静電気やノイズ電流の放電が容易に可能になり、保護性能が著しく向上する。

【手続補正7】
【補正対象書類名】　明細書
【補正対象項目名】　００２１
【補正方法】　変更
【補正の内容】
【００２１】
さらに本発明の好適な態様に係る半導体装置は、半導体回路が配置された基板を具備し、配線は、基板の周縁に沿うように当該基板の第１隅部から第２隅部にわたって形成され、第１保護回路は、基板の第１隅部に配置され、第２保護回路は、基板の第２隅部に配置される。このような位置に保護回路を配置する事で、基板の周辺部のサイズ（額縁）を大きくすることなく大きな保護回路を配置できるので都合がよい。

【書類名】　　手続補正書
【整理番号】　　J011113701
【提出日】　　平成20年 9月 8日
【あて先】　　特許庁長官殿
【事件の表示】
　【出願番号】　　特願2004-198040
【補正をする者】
　【識別番号】　　000002369
　【氏名又は名称】　セイコーエプソン株式会社
【代理人】
　【識別番号】　　100125689
　【弁理士】
　【氏名又は名称】　大林　章
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　【補正対象項目名】　全文
　【補正方法】　　変更
　【補正の内容】
　　【書類名】特許請求の範囲
　　【請求項１】
　基板上に設けられた半導体回路と、
　前記半導体回路に接続された配線と、
　電気信号を供給するために前記配線に電気的に接続された入力端子と、
　前記配線に接続されて前記半導体回路を保護する第１保護回路及び第２保護回路とを有し、
　前記配線のうち、前記半導体回路と前記配線との接続部と、前記入力端子との間で、前記第１保護回路が前記配線に接続され、
　前記配線のうち、前記第１保護回路と前記配線との接続部と、前記第２保護回路と前記配線との接続部との間で、前記半導体回路が前記配線に接続されている
　ことを特徴とする表示装置。
　　【請求項２】
　前記配線に複数の半導体回路が接続され、
　前記配線のうち前記各半導体回路の間に配置されて前記複数の半導体回路を保護する第３保護回路
　を具備する請求項１の表示装置。
　　【請求項３】
　前記配線は、前記半導体回路に電源電位を供給する低電位電源配線または高電位電源配線である
　請求項１または請求項２の表示装置。
　　【請求項４】
　前記配線は、前記半導体回路に信号を伝達する信号入力配線である
　請求項１または請求項２の表示装置。
　　【請求項５】
　前記配線は、前記基板の周縁に沿うように当該基板の第１隅部から第２隅部にわたって形成され、
　前記第１保護回路は、前記基板の前記第１隅部に配置され、
　前記第２保護回路は、前記基板の前記第２隅部に配置される
　請求項１から請求項４の何れかの表示装置。

【請求項６】
請求項１から請求項５の何れかの表示装置を具備する電子機器。

【手続補正2】
【補正対象書類名】　明細書
【補正対象項目名】　００１４
【補正方法】　変更
【補正の内容】
【００１４】
本発明に係る表示装置は、基板上に設けられた半導体回路と、前記半導体回路に接続された配線と、電気信号を供給するために前記配線に電気的に接続された入力端子と、前記配線に接続されて前記半導体回路を保護する第１保護回路及び第２保護回路とを有し、前記配線のうち、前記半導体回路と前記配線との接続部と、前記入力端子との間で、前記第１保護回路が前記配線に接続され、前記配線のうち、前記第１保護回路と前記配線との接続部と、前記第２保護回路と前記配線との接続部との間で、前記半導体回路が前記配線に接続されている。

【手続補正3】
【補正対象書類名】　明細書
【補正対象項目名】　００１５
【補正方法】　変更
【補正の内容】
【００１５】
従来技術のように入力端子近辺に設置した第１保護回路だけではなく、配線の入力端子に接続されていない部位に第２保護回路を設置することにより、静電気に対する保護が入力端子から離れた個所でも十分に得られるという効果を有する。

【手続補正4】
【補正対象書類名】　明細書
【補正対象項目名】　００２１
【補正方法】　変更
【補正の内容】
【００２１】
さらに本発明の好適な態様において、配線は、基板の周縁に沿うように当該基板の第１隅部から第２隅部にわたって形成され、第１保護回路は、基板の第１隅部に配置され、第２保護回路は、基板の第２隅部に配置される。このような位置に保護回路を配置する事で、基板の周辺部のサイズ（額縁）を大きくすることなく大きな保護回路を配置できるので都合がよい。

【手続補正5】
【補正対象書類名】　明細書
【補正対象項目名】　００２２
【補正方法】　変更
【補正の内容】
【００２２】
また、本発明の表示装置及びその表示装置を搭載した電子機器は工程中の静電破壊が起こりにくいためにコスト的に有利であり、電源の電圧降下が起こりにくいために表示品位も高いという効果を有する。

出願人履歴

０００００２３６９

19900820

新規登録

５９２０５２４２７

東京都新宿区西新宿２丁目４番１号

セイコーエプソン株式会社

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/436,335	05/06/2009	Yutaka Kobashi	122872.01

CONFIRMATION NO. 5191

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

PUBLICATION NOTICE

OC000000038186876

Title:SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

Publication No.US-2009-0251834-A1
Publication Date:10/08/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
12/436,335		2836	



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 27049 on 10/20/2009

- **Correspondence Address**
- **Power of Attorney Address**

The address of record for Customer Number 27049 is:

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PART 1 - ATTORNEY/APPLICANT COPY
page 1 of 1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 09/24/2010

OLIFF & BERRIDGE, PLC
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EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
09/24/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2009* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 11/101450.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/06/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Application number 12/436335 for "Semiconductor Device, Display Device and Electronic Apparatus" filed 05/06/2009 has been examined.

Claim Objections

2. Applicant is advised that should claim 2 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicated or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP 706.03(k).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 7, 9 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 3 and 12; it is not understood what is meant by "the wiring line being at least one of a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the semiconductor circuit." While claim 1 requires the wiring line supply the electrical signal. The electrical signal and power

potential source are two different species as stated in the instant application signal terminals (601 and 602) and power terminal (650 and 651) differ from each other.

6. Claim 7; it is not clear what is meant by "a wiring line over a first terminal portion to which an electrical signal is supplied from outside and a second terminal portion to which an electrical signal is not supplied from outside; a second protection circuit being arranged on the wiring line between the semiconductor circuit and the second terminal portion to protect the semiconductor circuit". The term “over” is totally unclear. It is totally unclear what is "an electrical signal from outside applies to a second terminal portion”. None of the figures shows an electrical signal applied from outside the apparatus. It is not clear which terminal portion applicant meant to be "a second terminal portion to which a second protection circuit arranged in between the second terminal portion and the semiconductor circuit". For purpose of examination, the above limitations are interpreted in accordance figure 1.

7. Claim 9, it is not understood what is meant by “a fourth protection circuit that sandwiches the buffer circuit; and a fifth protection circuit that sandwiches the buffer circuit". The term "sandwich" is totally unclear since detailed description does not explain the definition of the term "sandwich". For purpose of examination, it is interpreted as "each of the buffer circuit protected by one of the protection circuit.”

8. Claim 10 recites the limitation "the first power source wiring line and the second power source wiring line" in lines 4 and 7-8, respectively. There is insufficient antecedent basis for this limitation in the claim. For purpose of examination, claim 10 is assumed depending on claim 9.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2 4-6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee32 et al. (US 6,791,632, "Lee32").

11. **Regarding claim 1**, Lee32 discloses protection circuit and method from electrostatic discharge (ESD) of TFT-LCD, the apparatus (fig. 4) comprising: a semiconductor circuit (pixel positioned near crossing of a data line (D1-D3072) and a gate line (G1-G768)); a wiring line (vertical line on the most left in the figure) electrically connected to the semiconductor circuit; an input terminal (GSL) electrically connected to the wiring line to supply an electrical signal (data); and a first protection circuit (GESD1); and a second protection circuit (GESD2-GESD768) electrically connected to the wiring line to protect the semiconductor circuit, wherein the first protection circuit being electrically connected to the wiring line between (i) a connecting portion of the semiconductor circuit and the wiring line and (ii) the input terminal; and the semiconductor circuit being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line.

12. **Regarding claims 2 and 8**, Lee32 discloses a plurality of semiconductor circuits (each pixel positioned near crossing of the data line (D1-D3072) and the gate line (G1-

G768)) electrically connected to the wiring line; and a third protection circuit arranged on the wiring line between at least one set of two consecutive semiconductor circuits of the plurality of semiconductor circuits to protect the plurality of semiconductor circuits (see fig. 4).

13. **Regarding claim 4**, Lee32 discloses that the wiring line (control gate line) being a signal input wiring line that transmits a signal to the semiconductor circuit.

14. **Regarding claim 5**, Lee32 discloses a substrate (TFT substrate); the semiconductor circuit arranged on the substrate; the wiring line being formed over a first corner portion (upper portion) and a second corner portion (lower portion) of the substrate so as to follow a periphery of the substrate (see fig. 2); the first protection circuit arranged in the first corner portion of the substrate; and the second protection circuit arranged in the second corner portion of the substrate (see fig. 4).

15. **Regarding claim 6**, Lee32 discloses that the display device is an electronic device.

16. Claims 7 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,936,687, “Lee87”).

17. **Regarding claim 7**, Lee87 discloses liquid crystal display (LCD) having an electrostatic discharge protection circuit and a method for testing display quality using the circuit, the apparatus (fig. 11) comprising: a wiring line (450-480) electrically connected to a first terminal portion (490) and a second terminal portion (not shown on the other end of the respective wiring line); a semiconductor circuit (pixel) electrically

connected to the wiring line; a first protection circuit (d43) arranged on the wiring line between the semiconductor circuit and the first terminal portion to protect the semiconductor circuit; a second protection circuit (d57) connected to the other end of the wiring line; and a buffer circuit (inverter) arranged on the wiring line between the first terminal portion and the semiconductor circuit.

18. **Regarding claim 13**, Lee87 discloses the wiring line comprising a signal input wiring line that transmits a signal to the semiconductor circuit (col. 5, lines 45-64).

19. **Regarding claim 14**, Lee87 discloses a substrate (col. 1, line 19) on which the semiconductor circuit arranged; the wiring line being formed at first and second corner portion of the substrate so as to follow a periphery of the substrate; the first protection circuit arranged in the first corner portion of the substrate; and the second protection circuit being arranged in the second corner portion of the substrate (see fig. 11).

20. **Regarding claim 15**, Lee87 discloses the apparatus is a display device (title).

21. **Regarding claim 16**, Lee87 discloses the apparatus comprising an electronic device (gate and data driver circuits).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee32 in view of Ker (US 6,075,686, "Ker").

Lee32 discloses the limitations as discussed above. Lee32 does not explicitly disclose ESD protection circuit connected to a power line to protect against ESD event. Ker discloses an ESD protection circuit (140) connected between a first power supply line (VDD) and a second power supply line (VDDA) to provide ESD protection between the two power supply lines; another ESD protection circuit (150) connected between the first power supply line (VDD) and a reference power supply line (VSS) to provide ESD protection between the first power supply line and the reference supply line. It is well known in the art that VDD line, VSS line and I/O pad are subjected to attack by ESD pulses. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee32 ESD protection circuit and utilize protection the power supply line, as taught by Ker, in order to protect VDD line because the VDD line is needed to be protected against ESD pulses.

24. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee87 in view of Hector et al. (US 2003/0030054, “Hector”) and Ker.

25. **Regarding claim 9**, Lee87 discloses the limitations as discussed above. Lee87 does not explicitly disclose power supply lines including a high potential power source and a low potential power source. Hector discloses a power supply (76) having a high potential line (78) and a low potential line (80); a first protection circuit (70) connected between the high potential line and the low potential line; a second protection circuit

(upper ESD 34 and 36 as shown in fig. 1); wherein the first and second protection circuits configure to protect a semiconductor circuit (pixel 12) against ESD ([0044], [0045], [0056] and [0057]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee87 LCD and utilize protection circuit, as taught by Hector, in order to protect power supply lines against ESD pulses.

26. The combination of Lee87 and Hector does not explicitly disclose the buffer circuit arranged between the first and second power source; this is viewed to be rearrangement of part, which is dependent upon the operating condition and design requirement. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the apparatus Lee87 in view of Hector to set the buffer circuit in between the first and second power source wiring lines since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950).

Lee87 does not explicitly disclose each of the buffer circuit protected by one of the protection circuit. Ker discloses in figures 9 and 12 that buffer circuits (154, 156) connect to a high potential line (132 and 136) and a low potential line (134 and 138) and arrange from one end to the other end, wherein each of the buffer circuits are protected by ESD protection circuits (150 and 152). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the apparatus of Lee87 in view of Hector and utilize protection circuit, as taught by Ker, in order to protect each of the buffer circuit against ESD pulses.

27. **Regarding claim 10**, Lee87 discloses wiring line (450) including the buffer circuit, wherein the buffer circuit includes a first NOT circuit to which the electrical signal is input and a second NOT circuit electrically connected to the first NOT circuit in series; Ker discloses a third ESD protection circuit (140) arranged on the high potential line between a point of connection with the first NOT circuit (154) and a point of connection with the second NOT circuit (156) to protect the buffer circuit; and a fourth ESD protection circuit (142) arranged on the low potential line between a point of connection with the first NOT circuit and a point of connection with the second NOT circuit to protect the buffer circuit (col. 6, lines 11-34). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to further include additional ESD protection circuit, as taught by Ker, in order to protect the buffer against ESD pulses.

28. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee87 in view of Cooperman et al. (US 5,329,185, “Cooperman”).

Lee87 discloses the buffer circuit, connected on wiring line (540), including a first NOT circuit to which the electrically signal is input and a second NOT circuit electrically connected to the first NOT circuit in series. Lee87 does not explicitly disclose each of the first and second NOT circuits consisting of a complementary type transistor; and a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit. Cooperman discloses each of first and second NOT circuits consisting of a complementary type transistor (see fig. 1); and

channel width of transistor of the first transistor being larger than a channel width of the transistor of the second NOT circuit. Cooperman discloses that increasing the width of the channel transistor of the buffer will increase operating speed (abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee87 LCD and utilize speed control by increasing a channel width of the transistor, as taught by Cooperman, in order to increase speed operation (abstract).

29. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee87 in view of Ker.

Lee87 discloses the limitations as discussed above. Lee87 does not explicitly disclose ESD protection circuit connected to a power line to protect against ESD event. Ker discloses an ESD protection circuit (140) connected between a first power supply line (VDD) and a second power supply line (VDDA) to provide ESD protection between the two power supply lines; another ESD protection circuit (150) connected between the first power supply line (VDD) and a reference power supply line (VSS) to provide ESD protection between the first power supply line and the reference supply line. It is well known in the art that VDD line, VSS line and I/O pad are subjected to attack by ESD pulses. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee87 ESD protection circuit and utilize protection the power supply line, as taught by Ker, in order to protect VDD line because the VDD line is needed to be protected against ESD pulses.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is 571-270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Fureman can be reached on 571-272-2391. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tien Mai/
Examiner, Art Unit 2836
09/15/2010

/Stephen W Jackson/
Primary Examiner, Art Unit 2836

Notice of References Cited	Application/Control No. 12/436,335	Applicant(s)/Patent Under Reexamination KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,791,632	09-2004	Lee et al.	349/40
*	B	US-5,936,687	08-1999	Lee, Joo-Hyung	349/40
*	C	US-6,075,686	06-2000	Ker, Ming-Dou	361/56
*	D	US-2003/0030054	02-2003	Hector et al.	257/72
*	E	US-5,329,185	07-1994	Cooperman et al.	326/66
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2010								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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CONFIRMATION NO. 5191

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/436,335	05/06/2009 RULE	361	2836	122872.01

APPLICANTS
Yutaka Kobashi, Fujimichou, JAPAN;

**** CONTINUING DATA ***************************
This application is a CON of 11/101,450 04/08/2005 PAT 7,755,875

**** FOREIGN APPLICATIONS ***************************
JAPAN 2004-198040 07/05/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/18/2009

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☑ Yes ☐ No	/TIEN HUNG MAI/ Examiner's Signature	☐ Initials	JAPAN	6	16	2

ADDRESS

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UNITED STATES

TITLE

SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07)

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:37
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:39
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42

S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18
S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00

S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02
S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:39

S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52
S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB; USPAT	OR	ON	2009/02/05 09:28
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54

S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 13:03
S82	78	(6222710|6304305| 6445427|20050151194| 6175394|6515644| 2005311125| 20050237685| 20060077162|6587322| 6734504|11119256| 6690433|6989298| 6285535|20060208315| 6456474|20050078232| 20050241853| 20050243043| 20060139299|6858867| 20060231896| 20060082528| 20060002045|6495890| 6043512|6653750| 20060232539|6924687| 20060118787| 20060092591|7106402| 6740596|6088206| 20020060893| 20060176072|5657139| 20050168899|7095048| 20060057820|6355875| 6115017|6344958| 4481521|20060197166| 20040145551| 20010034093|6724025| 4602192|6469767| 20020085198|5892494| 5892493|5724057| 5448384|6759867| 20020125922|5900854| 20050105747| 20040080363| 20020149036|4472648| 5596474|6788355| 20040084672|6891196| 5373377|5736732| 5485019|5982004| 5985700|20030222705| 6812777|6731156| 9707544|6008684|	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 16:44

		6144217).pn.				
S83	35	S82 and (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 16:45
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04
S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12

S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19
S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over $1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50

S102	5	"11113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 11:23
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39

S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:40
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:47
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40

S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45
S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:46
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15

S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40
S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25

S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S138	8	capacit$4 near3 signal near line with capacit$4 near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:22
S139	1442	capacit$4 adj (protect$4 circuit) near3 signal near line with capacit$4 (protect$3 circuit) near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S140	2	capacit$4 near (protect $4 circuit) with signal near line same capacit$4 near (protect$3 circuit) with (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S141	0	capacit$4 near (first second) near protect$3 near circuit and capacit $4 near (third fourth) near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:30
S142	26	capacit$4 near protect$3 near circuit same (greater lower bigger larger) same capacit$4 near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:31

9/ 15/ 2010 5:27:46 PM
C:\ Documents and Settings\ tmai4\ My Documents\ EAST\ Workspaces\ 12436335.wsp

Receipt date: 05/06/2009

Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 122872.01	APPLICATION NO. New U.S. Continuation Patent Application 12/436335
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yutaka KOBASHI	
		FILING DATE May 6, 2009	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	1	2002/0057392 A1	05/16/2002	Ha
	2	6,795,143 B1	09/21/2004	Fukushima
	3	2003/0030054 A1	02/13/2003	Hector et al.
	4	2005/0151706 A1	07/14/2005	Lifka et al.
	5	2002/0068388 A1	06/06/2002	Murakami et al.
	6	5,786,616	07/28/1998	Fukumoto et al.
	7	5,610,427	03/11/1997	Shida
	8	6,175,394 B1	01/16/2001	Wu et al.
	9	6,623,990 B2	09/23/2003	Watanabe et al.
	10	2002/0009890 A1	01/24/2002	Hayase et al.
	11	6,791,632 B2	09/14/2004	Lee et al.
	12	6,028,465	02/22/2000	So
	13	6,157,361	12/05/2000	Kubota et al.
	14	6,329,694 B1	12/11/2001	Lee et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	15	JP-B2-3141511	03/05/2001	Japan		
	16	JP-B2-2884946	04/19/1999	Japan		
	17	WO 03/088199 A1	10/23/2003	WIPO		
	18	CN 1396656 A	02/12/2003	China		
	19	JP-A-2003-308050	10/31/2003	Japan		

OTHER DOCUMENTS

Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER /Tien Mai/	DATE CONSIDERED 09/15/2010

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.M./

Date: May 6, 2009

Form PTO-1449 (REV. 1/06) US Dept. of Commerce PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 122872.01	APPLICATION NO. New U.S. Continuation Patent Application 12/436335
	APPLICANT Yutaka KOBASHI	
	FILING DATE May 6, 2009	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	20	6,351,364 B1	02/26/2002	Chen et al.
	21	2004/0264080 A1	12/30/2004	Yang et al.
	22	5,719,647	02/17/1998	Fujikawa et al.
	23	2004/0085284 A1	05/06/2004	Chen et al.
	24	6,108,056	08/22/2000	Nakajima et al.
	25	4,654,865	03/31/1987	Sunazuka et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	26	JP-A-02-307258	12/20/1990	Japan		
	27	JP-A-2001-298157	10/26/2001	Japan		
	28	TW 441069B	06/16/2001	Taiwan		
	29	TW 441073B	06/16/2001	Taiwan		

OTHER DOCUMENTS

Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER /Tien Mai/	DATE CONSIDERED 09/15/2010

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.M./

Date: May 6, 2009

Interview Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

All participants (applicant, applicant's representative, PTO personnel):

(1) *TIEN MAI*. (3)*ANDY KIM*.

(2) *JARED FUREMAN*. (4)_____.

Date of Interview: *02 December 2010*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1,2 and 7-12*.

Identification of prior art discussed: *Lee et al. (US 6,791,632) and Lee (US 5,936,687).*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Proposed amendment overcomes the previous 112 2nd paragraph rejections and prior art rejections; however, amended claims raise new issues that would require further consideration and/or search. It was agreed that a formal response will be filed*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Jared J. Fureman/
Supervisory Patent Examiner, Art Unit 2836

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

JFW



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the September 24, 2010 Office Action and further in view of the personal held with the Examiners on December 2, 2010, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a semiconductor circuit;

a wiring line electrically connected to the semiconductor circuit;

an input terminal electrically connected to the wiring line to supply ~~an electrical signal;~~ power; and

a first protection circuit and a second protection circuit that are electrically connected to the wiring line to protect the semiconductor circuit;

the first protection circuit being electrically connected to the wiring line between (i) a connecting portion of the semiconductor circuit and the wiring line and (ii) the input terminal; and

the semiconductor circuit being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line.

2. (Currently Amended) The display device as set forth in claim 1, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being ~~arranged on~~ electrically connected to the wiring line between at least one set of connecting portions of two consecutive semiconductor circuits of the plurality of semiconductor circuits and the wiring line to protect the plurality of semiconductor circuits.

3. (Original) The display device as set forth in claim 1, the wiring line being at least one of a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the semiconductor circuit.

4. (Original) The display device as set forth in claim 1, the wiring line being a signal input wiring line that transmits a signal to the semiconductor circuit.

5. (Original) The display device as set forth in claim 1, further comprising:

a substrate;

the semiconductor circuit being arranged on the substrate;

the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7. (Currently Amended) A semiconductor device, comprising:

~~a~~ a first wiring line ~~over a~~ electrically connected to a first terminal portion to which ~~an electrical signal is supplied from outside and~~ a first power is supplied;

a second wiring line electrically connected to a second terminal portion to which ~~an electrical signal is not supplied from outside;~~ a second power is supplied;

a semiconductor circuit electrically connected to the first wiring ~~line;~~ line and the second wiring line;

a first protection circuit being ~~arranged on the~~ electrically connected to the first wiring line between (i) a connecting portion of the semiconductor circuit and the first wiring line and (ii) ~~and~~ the first terminal portion to protect the semiconductor circuit;

a second protection circuit being ~~arranged on the~~ electrically connected to the second wiring line between (i) a connecting portion of the semiconductor circuit and the second wiring line and (ii) ~~and~~ the second terminal portion to protect the semiconductor circuit; and

a buffer circuit being ~~arranged on the~~ electrically connected to the first wiring line between ~~the first terminal portion and the semiconductor circuit.~~ (i) a connecting portion of the semiconductor circuit and the first wiring line and (ii) the first terminal portion.

8. (Currently Amended) The semiconductor device as set forth in ~~claim 1,~~ claim 7, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being ~~arranged on the~~ electrically connected to the first wiring line between adjacent sets of connecting portions of the semiconductor circuits of the plurality of semiconductor circuits and the first wiring line to protect the plurality of semiconductor circuits.

9. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a first power source wiring line branched from a high potential power source wiring line;

a second power source wiring line branched from a low potential power source wiring line;

the buffer circuit being arranged between the first and second power source wiring lines;

a fourth protection ~~circuit that sandwiches the buffer circuit of the first power source wiring line being arranged opposite to a branching point from the high potential power source wiring line~~ circuit, the buffer circuit being electrically connected to the first power source wiring line between (i) a connecting portion of the fourth protection circuit and the first power source wiring line and (ii) a connecting portion of the first protection circuit and the first power source wiring line to protect the buffer circuit; and

a fifth protection ~~circuit that sandwiches the buffer circuit of the second power source wiring line being arranged opposite to a branching point from the low potential power source wiring line~~ circuit, the buffer circuit being electrically connected to the second power source wiring line between (i) a connecting portion of the fifth protection circuit and the second power source wiring line and (ii) a connecting portion of the second protection circuit and the second power source wiring line to protect the buffer circuit.

10. (Currently Amended) The semiconductor device as set forth in ~~claim 7,~~ claim 9, further comprising:

the buffer circuit including a first NOT circuit to which the ~~electrical signal~~first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

a sixth protection circuit being ~~arranged on~~ electrically connected to the first power source wiring line between (i) a connecting portion of ~~a point of connection with~~ the first NOT circuit and the first power source wiring line and ~~a point of connection with~~ (ii) a connecting portion of the second NOT circuit to protect the buffer ~~circuit;~~ circuit and the first power source wiring line; and

a seventh protection circuit being ~~arranged on~~ electrically connected to the second power source wiring line between (i) a connecting portion of ~~a point of connection with~~ the first NOT circuit and the second power source wiring line and ~~a point of connection with~~ (ii) a connecting portion of the second NOT circuit to protect the buffer ~~circuit.~~circuit and the second power source wiring line.

11. (Currently Amended) The semiconductor device as set forth in claim 7,

the buffer circuit including a first NOT circuit to which the ~~electrical signal~~first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

each of the first and second NOT circuits consisting of a complementary-type transistor; and

a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit.

12. (Currently Amended) The semiconductor device as set forth in claim 7,

the first wiring line comprising ~~a low potential power source wiring line or~~ a high potential power source wiring line supplying a power source potential to the semiconductor ~~circuit.~~circuit; and

the second wiring line comprising a low potential power source wiring line supplying a power source potential to the semiconductor.

13. (Original) The semiconductor device as set forth in claim 7,

the wiring line comprising a signal input wiring line that transmits a signal to the semiconductor circuit.

14. (Original) The semiconductor device as set forth in claim 7, further comprising:

a substrate on which the semiconductor circuit is arranged;

the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

15. (Original) A display device provided with the semiconductor device as set forth in claim 7.

16. (Currently Amended) An electronic device provided with the ~~display~~ semiconductor device as set forth in claim 7.

REMARKS

Claims 1-16 are pending in this application. By this Amendment, claims 1, 2, 7-12, and 16 are amended. The Amendment is supported by the specification at least at Figs. 2, 3, and 8. No new matter is added. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The courtesies extended to Applicant's representative by Examiner Mai and Supervisory Examiner Fureman at the personal interview held on December 2, 2010 are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below, which constitute Applicant's separate record of the substance of the interview. During the interview, it was indicated that the combination of proposed amendments, which are incorporated into this amendment, would overcome the 35 U.S.C. §112 rejections and also distinguish the claims over the prior art of record.

I. Objections to Claims

The Office Action objects to claims 2 and 8 as being a substantial duplicate. By this Amendment, claim 8 is amended to depend from claim 7 instead of claim 1 as to obviate the objection. Accordingly, withdrawal of the objection is respectfully requested.

II. Rejection of Claims Under 35 U.S.C. §112

The Office Action rejects claims 3, 7, 9, and 12 under 35 U.S.C. §112, second paragraph, as being indefinite.

The Office Action rejects claims 3 and 12 for reciting, "supplying a *power source potential*." Specifically, the Office Action asserts that the recitation of "supplying a *power source potential*" is indefinite in view of the base claims 1 and 7, which recite "supply an *electrical signal*" and "*electrical signal* is supplied," respectively. The Office Action states on pages 2 and 3 that the electrical signal and power source potential are two different species. By this Amendment, claim 1 and claim 7 are amended to replace "supply an

electrical signal" with "supply power," and "electrical signal is supplied" with "power is supplied" respectively for consistency. Claims 10 and 8 are also amended for consistency in this regard.

The Office Action also asserts that the term "over" recited in claim 7 is unclear. By this Amendment, claim 7 is amended to remove "over" and recite "a first wiring line electrically connected to a first terminal portion to which a first power is supplied" for further clarity.

The Office Action also asserts that the term "sandwiches" recited in claim 9 is indefinite. By this Amendment, claim 9 is amended to remove "sandwiches" and recite "a fourth protection circuit, the buffer circuit being electrically connected to the first power source wiring line between (i) a connecting portion of the fourth protection circuit and the first power source wiring line and (ii) a connecting portion of the first protection circuit and the first power source wiring line to protect the buffer circuit."

The Office Action also asserts that "the first power source wiring line" and "the second power source wiring line" recited in claim 10 have insufficient antecedent basis. By this Amendment, claim 10 is amended to depend from claim 9, instead of claim 7, to provide sufficient antecedent basis for "the first power source wiring line" and "the second power source wiring line."

Accordingly, withdrawal of the rejection of claims 3, 7, 9, and 12 under 35 U.S.C. §112 is respectfully requested.

III. The Claims Define Allowable Subject Matter

The Office Action rejects claims 1, 2, 4-6, and 8 under 35 U.S.C. §102(b) as being anticipated by Lee '32 (U.S. Patent No. 6,791,632); rejects claims 7 and 13-16 under 35 U.S.C. §102(b) as being anticipated by Lee '87 (U.S. Patent No. 5,936,687); rejects claim 3 under 35 U.S.C. §103(a) over Lee '32 in view of Ker (U.S. Patent No. 6,075,686);

rejects claims 9 and 10 under 35 U.S.C. §103(a) over Lee '87 in view of Hector (U.S. Patent Application Publication No. 2003/0030054) and Ker; rejects claim 11 under 35 U.S.C. §103(a) over Lee '87 in view of Cooperman (U.S. Patent No. 5,329,185); and rejects claim 12 under 35 U.S.C. §103(a) over Lee '87 in view of Ker. The rejections are respectfully traversed.

As discussed and agreed during the interview, in particular, Lee '32 does not disclose at least "a semiconductor circuit; an input terminal electrically connected to the wiring line to supply power; and the first protection circuit being electrically connected to the wiring line between (i) a connecting portion of the semiconductor circuit and the wiring line and (ii) the input terminal; the semiconductor circuit being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line," as recited in independent claim 1; and Lee '87 does not disclose at least "a first wiring line electrically connected to a first terminal portion to which a first power is supplied; a second wiring line electrically connected to a second terminal portion to which a second power is supplied," as recited in independent claim 7.

Regarding claim 1, the Office Action asserts that gate shortening line GSL, as shown in Fig. 4, corresponds to an input terminal electrically connected to the wiring line to *supply an electrical signal*. As stated in the Office Action on pages 2 and 3, in connection with the §112 rejection, electrical signal and power source potential are two different species, and thus supplying an electrical signal does not reasonably correspond to supplying power. Supplying an electrical signal, as allegedly disclosed in Fig. 4 of Lee '32, does not reasonably correspond to "an input terminal electrically connected to the wiring line to *supply power*," as recited in claim 1.

Further, Lee '32 does not disclose any semiconductor circuit in Fig. 4. The Office Action, on page 4, asserts that pixel positioned near crossing over data lines D1-D3072 and gate lines G1-G768 correspond to a semiconductor circuit. However, Fig. 4 of Lee '32 only shows empty space in each of grid lines formed by crossings of data lines D1-D3072 and gate lines G1-G768. Thus, Fig. 4 of Lee '32 fails to show any configuration of the alleged semiconductor circuit.

During the interview, the Examiners asserted that LCD panel including a pair of transistors and capacitors corresponds to a semiconductor circuit, as shown in Fig. 2 of Lee '32. The Examiners further asserted, in view of Fig. 2 of Lee '32, Fig. 4 implies presence of such a LCD panel, for example, at an intersection of data line D1 and gate line G1. Even if such assertion is true, which Applicant do not concede, a LCD panel at an intersection of a data line and a gate line would not have connected to any wiring line to which any input terminal is connected to supply power. Thus, the LCD panel of Lee '32 does not reasonably correspond to a semiconductor circuit to which a wiring line electrically is connected, wherein an input terminal electrically connected to the wiring line to supply power. Therefore, Lee '32 also fails to disclose a semiconductor circuit recited in claim 1.

In absence of the semiconductor circuit in Lee '32, the Office Action fails to show that "the first protection circuit being electrically connected to the wiring line between (i) *a connecting portion of the semiconductor circuit* and the wiring line and (ii) the input terminal" and "*the semiconductor circuit* being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line," as recited in claim 1.

Regarding claim 7, Fig. 11 of Lee '87 discloses a liquid crystal display including input 490 coupled to inverters, shortening lines 450-480, gate lines G1-G4, data lines Dl-D4, pixels a-d, and diodes d43 and d57. The Office Action, on page 5, asserts that input 490

corresponds to a first terminal portion and other end of the shortening lines 450-480 corresponds to a second terminal portion. However, Fig. 11 of Lee '87 does not show any object on the other end of shortening lines 450-480 other than diodes D57 and D58. Lee '87 does not show the diodes D57 (allegedly "a second protection circuit") being arranged on the wiring line between pixels a-d (allegedly "semiconductor circuit") and any second terminal portion. Further, Lee '87 does not disclose that shortening lines 450-480 (allegedly "a first wiring line" and "a second wiring line") electrically connected to any terminal portion to which first and second powers are supplied. Instead, in Lee '87, input 490 appears to provide input signals to drive data lines D1-D4. As discussed above, supplying *signal* does not reasonably correspond to supplying *power*.

Ker, Hector, and Cooperman also do not disclose the above-cited features. In view of the foregoing, Applicant respectfully submits that claims 1 and 7 are allowable. Claims 2-6 depend from claim 1; and claims 8-16 depend from claim 7, and are therefore also allowable by virtue of their dependencies, as well as for the additional features that they recite. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §102(b) and §103(a) are respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-16 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Andy N. Kim
Registration No. 61,050

JAO:ANK/rle

Date: December 22, 2010

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/436,335	05/06/2009	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/22/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DORIS m. BURNS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

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OLIFF & BERRIDGE, PLC
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EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
02/02/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response of 12/22/2010 has been entered and considered. Upon entering amendment, claims 1, 2, 7-12 and 16 have been amended; claim objection and claim rejection under 35 USC 112, second paragraph, have been withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 4 and 13, it is not understood what is meant by “the wiring line being a signal input wiring line that transmits a signal to the semiconductor circuit.” While claim 1 requires the wiring line supply power. The electrical signal and power potential source are two different species as stated in the instant application. For purpose of examination, the above limitations are interpreted as “the wiring line being the power input wiring line that transmits power potential.”

6. Claim 9 recites the limitations “the first and second power source wiring lines” in lines 7-8; “the first power source wiring line” in lines 12-14 and “the second power source wiring line" in lines 18-20. There is antecedent basis for this limitation in the claim. It is not clear which of the first/second power source wiring line Applicant refers to (see claim 7 and claim 9). For purpose of examination, "a first power source wiring line" and "a second power source wiring line" in lines 3 and 5 have been interpreted as "the first power source wiring line" and "the second power source wiring line”.

Claim Rejections - 35 USC § 102

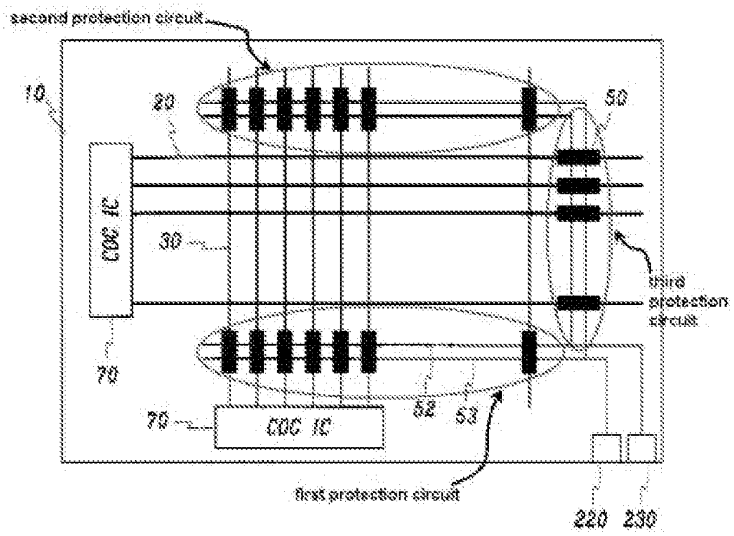
7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-8 and 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,936,687, “Lee”).

9. **Regarding claim 1**, Lee discloses liquid crystal display having an electrostatic discharge (ESD) protection circuit, the apparatus (figs. 5, 6 and also see reproduced figure below) comprising: a semiconductor circuit (pixels that are at corner between line 20 and line 30); a wiring line (20, 30, 52 and 53) electrically connected to the semiconductor circuit; an input terminal (220 and 230) electrically connected to the wiring line to supply power; and a first protection circuit and a second protection circuit that are electrically connected to the wiring line to protect the semiconductor circuit; the

first protection circuit being electrically connected to the wiring line between (i) a connecting portion of the semiconductor circuit and the wiring line and (ii) the input terminal; and the semiconductor circuit being electrically connected to the wiring line between (i) a connecting portion of the first protection circuit and the wiring line and (ii) a connecting portion of the second protection circuit and the wiring line.



10. **Regarding claim 2**, Lee discloses a plurality of semiconductor circuits (pixel) being electrically connected to the wiring line; and a third protection circuit being electrically connected to the wiring line between at least one set of connecting portions of two consecutive semiconductor circuits of the plurality of semiconductor circuits and the wiring line to protect the plurality of semiconductor circuits. Lee discloses in figure 5 that the third protection circuit protects lines 20 against ESD. Lee also discloses in figure 6 that each of the ESD protection circuit comprises two diodes to protect line 30. Lee further discloses in figure 10 that diode d59 connects between at least one set of

connecting portions of two consecutive semiconductor circuits (b and d) to protect the semiconductor circuits since both gates of semiconductor circuits (b and d) connect to cathode of diode d59.

11. **Regarding claim 3**, Lee discloses the wiring line being a low potential power source (GND) and a high potential power source (10V) for supplying a power source potential to the semiconductor circuit for protection purpose (see fig. 6).

12. **Regarding claim 4**, Lee discloses the wiring line being a power input wiring line that transmits power potential (see fig. 6).

13. **Regarding claim 5**, Lee discloses a substrate (glass substrate); the semiconductor circuit being arranged on the substrate (col. 1, line 14); the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate (at least portion of the wiring lines arrange on the right side of the substrate); the first protection circuit being arranged in the first corner portion of the substrate (at least one of the first protection circuits arranges on lower right corner); the second protection circuit being arranged in the second corner portion of the substrate (at least one of the second protection circuits arranges on upper right corner).

14. **Regarding claim 6**, Lee discloses that the display device is an electronic device.

15. **Regarding claim 7**, Lee discloses liquid crystal display having an electrostatic discharge (ESD) protection circuit, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a first wiring line (52) electrically connected to a first terminal portion (230) to which a first power is supplied; a second wiring line (53) electrically connected to a second terminal portion (220) to which a second power is supplied; a

semiconductor circuit (pixels that are at corner between line 20 and line 30) electrically connected to the first wiring line and the second wiring line; a first protection circuit being electrically connected to the first wiring line between (i) a connecting portion of the semiconductor circuit and the first wiring line and (ii) the first terminal portion to protect the semiconductor circuit; a second protection circuit being electrically connected to the second wiring line between (i) a connecting portion of the semiconductor circuit and (ii) the second terminal portion to protect the semiconductor circuit; and a buffer circuit (inverter in figure 11). The buffer circuit inherently electrically connects to the first wiring line between (i) a connecting portion of the semiconductor circuit and the first wiring line and (ii) the first terminal portion to fulfill its function, as evidenced by Hatzilambrou et al. (US 6,801,416). Hatzilambrou discloses a semiconductor structure level of an inverter circuit (510, 520) connected and an input, a high potential line (Vdd), and a low potential line (Vss), wherein the inverter circuit outputs high when it receives logic low and via versa (also see http://en.wikipedia.org/wiki/Inverter_(logic_gate)).

16. **Regarding claim 8**, Lee discloses a plurality of semiconductor circuits being electrically connected to the wiring line; and a third protection circuit being electrically connected to the first wiring line between adjacent sets of connecting portions of the semiconductor circuits of the plurality of semiconductor circuit and the first wiring line to protect the plurality of semiconductor circuits. Lee discloses in figure 5 that the third protection circuit protects lines 20 against ESD. Lee also discloses in figure 6 that each of the ESD protection circuit comprises two diodes to protect line 30. Lee further discloses in figure 10 that diode d59 connects between at least one set of connecting

portions of two adjacent set of semiconductor circuits (b and d) to protect the semiconductor circuits since both gates of semiconductor circuits (b and d) connect to cathode of diode d59.

17. **Regarding claim 12**, Lee discloses the first wiring line comprising high potential power source wiring line supplying a power source potential to the semiconductor circuit for protection purpose; and the second wiring line comprising a low potential power source wiring line supplying a power source potential to the semiconductor circuit also for protection purpose (see fig. 6).

18. **Regarding claim 13**, Lee discloses the wiring line being a power input wiring line that transmits power potential (see fig. 6).

19. **Regarding claim 14**, Lee discloses a substrate (col. 1, line 19) on which the semiconductor circuit is arranged; the wiring line being formed at first and second corner portions of the substrate so as to follow a periphery of the substrate; the first protection circuit being arranged in the first corner portion of the substrate (at least one of the first protection circuits arranges on lower right corner); the second protection circuit being arranged in the second corner portion of the substrate (at least one of the second protection circuits arranges on upper right corner).

20. **Regarding claim 15**, Lee discloses the apparatus is a display device (title).

21. **Regarding claim 16**, Lee discloses the apparatus comprising an electronic device (gate and data drive circuits).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Ker (US 6,075,686, "Ker").

24. Regarding claim 9, Lee discloses the first power source wiring line branched from a high potential power source wiring line(10V); the second power source wiring line branched from a low potential power source wiring line (GND); the buffer circuit being arranged between the first and second power source wiring lines (as discussed in claim 7); a fourth protection circuit (d41); a fifth protection circuit (d42), wherein the buffer circuit connect to the first power source wiring line between a connecting portion of the fourth protection circuit and the first power source wiring line and a connecting portion of the first protection circuit and first power source wiring line (for powering the buffer circuit), and wherein the buffer circuit connect to the second power source wiring line between a connecting portion of the fifth protection circuit and the second power source wiring line and a connecting portion of the second protection circuit and the second power source wiring line (for powering the buffer circuit). Lee does not explicitly disclose each of the buffer circuit protected by the fourth and fifth protection circuits. Ker discloses in figure 5 that buffer circuits (48 and 50) connect to a high potential line (38 and 42) and a low potential line (40 and 44) and arranged from one end to the other

end, wherein each of the buffer circuits are protected by ESD protection circuit (Dp1, Dn1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Lee and utilize protection circuits, as taught by Ker, in order to protect each of the buffer circuit against ESD pulses at the signal input.

25. **Regarding claim 10**, Lee discloses wiring line (450) including the buffer circuit, wherein the buffer circuit includes a first NOT circuit to which the first power is input and a second NOT circuit electrically connects to the first NOT circuit in series. Lee also discloses a sixth protection circuit (d45) and a seventh protection circuit (d46). Lee does not explicitly disclose the sixth protection circuit connected to the first power source wiring line between a connecting portion of the first NOT circuit and the first power source wiring line and a connecting portion of the second NOT circuit to protect the buffer circuit and the first power source wiring line; and the seventh protection circuit connected to the second power source wiring line between a connecting portion of the first NOT circuit and the second power source wiring line and a connecting portion of the second NOT circuit to protect the buffer circuit and the second power source wiring line. Ker discloses in figure 7 that sixth and second protection circuits (Mp4 and Mn4) connect between first and second buffer circuits (48 and 50) to protect the buffer circuits against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Lee and utilize protection circuits, as taught by Ker, in order to protect each of the buffer circuit against ESD pulses.

26. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Cooperman et al. (US 5,329,185, "Cooperman")

Lee discloses in figure 11 that the buffer circuit including a first NOT circuit to which the first power is input (power supply as discussed in claim 7) and a second NOT circuit electrically connected to the first NOT circuit in series. Lee does not explicitly disclose each of the first and second NOT circuits consisting of complementary type transistor; and a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit. Cooperman discloses each of first and second NOT circuits consisting of a complementary type transistor (see fig. 1); and channel width of transistor of the first transistor being larger than a channel width of the transistor of the second NOT circuit. Cooperman discloses that increasing the width of the channel transistor of the buffer will increase operating speed (abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee LCD and utilize speed control by increasing a channel width of the transistor, as taught by Cooperman, in order to increase speed operation (abstract).

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is 571-270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Fureman can be reached on 571-272-2391. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tien Mai/
Examiner, Art Unit 2836
01/25/2011

/Stephen W Jackson/
Primary Examiner, Art Unit 2836

Notice of References Cited	Application/Control No. 12/436,335	Applicant(s)/Patent Under Reexamination KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	http://en.wikipedia.org/wiki/Inverter_(logic_gate), 2005
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2010	01/25/2011							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:37
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:39
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42

S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18
S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00

S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02
S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:39

S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52
S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB; USPAT	OR	ON	2009/02/05 09:28
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54

S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 13:03
S82	78	(6222710|6304305| 6445427|20050151194| 6175394|6515644| 2005311125| 20050237685| 20060077162|6587322| 6734504|11119256| 6690433|6989298| 6285535|20060208315| 6456474|20050078232| 20050241853| 20050243043| 20060139299|6858867| 20060231896| 20060082528| 20060002045|6495890| 6043512|6653750| 20060232539|6924687| 20060118787| 20060092591|7106402| 6740596|6088206| 20020060893| 20060176072|5657139| 20050168899|7095048| 20060057820|6355875| 6115017|6344958| 4481521|20060197166| 20040145551| 20010034093|6724025| 4602192|6469767| 20020085198|5892494| 5892493|5724057| 5448384|6759867| 20020125922|5900854| 20050105747| 20040080363| 20020149036|4472648| 5596474|6788355| 20040084672|6891196| 5373377|5736732| 5485019|5982004| 5985700|20030222705| 6812777|6731156| 9707544|6008684|	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 16:44

		6144217).pn.				
S83	35	S82 and (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 16:45
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04
S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12

S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19
S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over $1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50

S102	5	"11113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 11:23
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39

S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:40
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:47
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40

S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45
S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:46
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl $3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15

S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40
S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25

S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S159	2	"20040141269"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/20 18:36
S160	36	"5936687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 13:10
S161	5	("5936687" | "5953191" | "5973901" | "6649944" | "6753836").PN. OR ("6985340").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 13:14
S165	13	"6801416"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 17:50
S166	2	inverter with via near versa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:02
S167	31856	inverter with high with low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S168	2484	inverter near2 high near2 low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S169	13	inverter near2 high near2 low near input near signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:33
S170	3	11/101450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:47
S171	3997	protect$3 near (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S172	168	protect$3 near (buffer inverter) and esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S173	14	("20030107424" | "20030214768" | "20050093069" | "4264941" | "4384287" | "4466120" | "5287241" | "5691557" | "6507469" | "6583972" | "6590264" | "6643109" | "6671146" | "7064942").PN. OR ("7663851").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 19:50

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S138	8	capacit$4 near3 signal near line with capacit$4 near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:22
S139	1442	capacit$4 adj (protect$4 circuit) near3 signal near line with capacit$4 (protect$3 circuit) near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S140	2	capacit$4 near (protect $4 circuit) with signal near line same capacit$4 near (protect$3 circuit) with (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S141	0	capacit$4 near (first second) near protect$3 near circuit and capacit $4 near (third fourth) near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:30
S142	26	capacit$4 near protect$3 near circuit same (greater lower bigger larger) same capacit$4 near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:31

1/25/2011 11:58:45 AM
C:\Documents and Settings\tmai4\My Documents\EAST\Workspaces\12436335.wsp

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Application No.: 12/436,335

Filed: May 6, 2009



Group Art Unit: 2836

Examiner: T. MAI

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant hereby requests continued examination.

☒ Applicant further requests entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 237801 in the amount of ☒ $810.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Ryan M. Crockett
Registration No. 62,945

JAO:RMC/plj

Date: June 2, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

06/03/2011 SHOHAMME 00000089 12436335
01 FC:1601 810.00 OP

PATENT APPLICATION

OLIFF & BERRIDGE, PLC
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

Attorney Docket No.: 122872.01

CUSTOMER NUMBER 25944



AMENDMENT TRANSMITTAL

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ Entitlement to small entity status is hereby asserted.

☐ Small entity status of this application has been established.

Any additional claim fees have been calculated as shown below:

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	*26 MINUS	**20	=6	x 26	$		x 52	$ 312
INDEP CLAIMS	*6 MINUS	***3	=3	x 110	$		x 220	$ 660
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+ 195	$	OR	+ 390	$
					$			$ 972

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

☒ Check No. 237799 in the amount of $972.00 is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Ryan M. Crockett
Registration No. 62,945

JAO:RMC/plj
Date: June 2, 2011

OPAP
JUN 02 2011
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the February 2, 2011 Office Action, the period for reply being extended by the attached Petition for Extension of Time, and in consideration of the attached Request for Continued Examination, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

06/03/2011 SMOHAMME 00000090 12436335
01 FC:1201 660.00 OP
02 FC:1202 312.00 OP

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a semiconductor circuit;

a wiring line electrically connected to the semiconductor circuit;

an input terminal electrically connected to the wiring line to supply power; and

a first protection circuit and a second protection circuit that are electrically connected to the wiring line to protect the semiconductor circuit;

the first protection circuit being electrically connected to the wiring line between (i) a first connecting portion ~~of the~~at which the semiconductor circuit and the wiring line are electrically connected and (ii) the input terminal; and

the semiconductor circuit being electrically connected to the wiring line between ~~(i) a~~ (iii) a second connecting portion ~~of the~~at which the first protection circuit and the wiring line are electrically connected and ~~(ii) a~~ (iv) a third connecting portion ~~of the~~ at which the second protection circuit and the wiring ~~line.~~line are electrically connected.

2. (Currently Amended) The display device as set forth in claim 1, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being electrically connected to the wiring line to protect the plurality of semiconductor circuits, the third protection circuit being connected to the wiring line between at least one set of connecting portions of two consecutive semiconductor circuits of the plurality of semiconductor circuits and the wiring ~~line to protect the plurality of semiconductor circuits.~~line.

3. (Original) The display device as set forth in claim 1, the wiring line being at least one of a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the semiconductor circuit.

4. (Canceled)

5. (Original) The display device as set forth in claim 1, further comprising:

a substrate;

the semiconductor circuit being arranged on the substrate;

the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7. (Currently Amended) A semiconductor device, comprising:

a first wiring line electrically connected to a first terminal portion to which a first power is supplied;

a second wiring line electrically connected to a second terminal portion to which a second power is supplied;

a semiconductor circuit electrically connected to the first wiring line and the second wiring line;

a first protection circuit being electrically connected to the first wiring line to protect the semiconductor circuit, the first protection circuit being electrically connected to the first wring line between (i) a first connecting portion ~~of the~~at which the semiconductor

circuit and the first wiring line are electrically connected and (ii) the first terminal ~~portion to protect the semiconductor circuit;~~portion;

a second protection circuit being electrically connected to the second wiring line to protect the semiconductor circuit, the second protection circuit being electrically connected to the second wiring line between ~~(i) a~~ (iii) a second connecting portion ~~of the~~ at which the semiconductor circuit and the second wiring line are electrically connected and ~~(ii) the~~ (iv) the second terminal ~~portion to protect the semiconductor circuit;~~portion; and

a buffer circuit being electrically connected to the first wiring line between ~~(i) a~~ (v) the first connecting portion ~~of the~~at which the semiconductor circuit and the first wiring line are electrically connected and ~~(ii) the~~ (vi) the first terminal portion.

8. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a plurality of semiconductor circuits being electrically connected to the wiring line; and

a third protection circuit being electrically connected to the first wiring line to protect the plurality of semiconductor circuits, the third protection circuit being electrically connected to the first wiring line between adjacent sets of connecting portions of the semiconductor circuits of the plurality of semiconductor circuits and the first wiring line to protect the plurality of semiconductor circuits.

9. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

~~a first power source wiring line branched from a high potential power source wiring line;~~

~~a second power source wiring line branched from a low potential power source wiring line;~~

the buffer circuit being arranged between the first and second ~~power source~~ wiring lines;

a fourth protection ~~circuit,~~circuit being electrically connected to the first wiring line to protect the semiconductor circuit and the buffer circuit;

a fifth protection circuit being electrically connected to the second wiring line to protect the semiconductor circuit and the buffer circuit;

the buffer circuit being electrically connected to the first ~~power source~~ wiring line between ~~(i) a~~ (vii) a fourth connecting portion ~~of the~~at which the fourth protection circuit and the first ~~power source~~ wiring line are electrically connected and ~~(ii) a~~ (viii) a fifth connecting portion ~~of the~~ at which the first protection circuit and the first ~~power source~~ wiring line ~~to protect the buffer circuit;~~are electrically connected; and

~~a fifth protection circuit,~~ the buffer circuit being electrically connected to the second ~~power source~~ wiring line between ~~(i) a~~(ix)a sixth connecting portion ~~of the~~at which the fifth protection circuit and the second ~~power source~~ wiring line are electrically connected and ~~(ii) a~~(x) a seventh connecting portion ~~of the~~at which the second protection circuit and the second ~~power source~~ wiring line ~~to protect the buffer circuit.~~are electrically connected.

10. (Currently Amended) The semiconductor device as set forth in claim 9, further comprising:

the buffer circuit including a first NOT circuit to which the first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

a sixth protection circuit being electrically connected to the first ~~power source~~ wiring line to protect the buffer circuit, the sixth protection circuit being electrically connected to the first wiring line between ~~(i) a~~(xi) an eighth connecting portion ~~of the~~at which the first NOT circuit and the first ~~power source~~ wiring line are electrically connected and ~~(ii)~~

~~a~~(xii) a ninth connecting portion ~~of the~~at which the second NOT circuit ~~to protect the buffer circuit~~ and the first ~~power source~~ wiring ~~line;~~line are electrically connected; and

a seventh protection circuit being electrically connected to the second ~~power source~~ wiring line to protect the buffer circuit, the seventh protection circuit being electrically connected to the second wiring line between ~~(i) a~~ (xiii) a tenth connecting portion ~~of the~~at which the first NOT circuit and the second ~~power source~~ wiring line are electrically connected and ~~(ii) a~~(xiv) an eleventh connecting portion ~~of the~~at which the second NOT circuit ~~to protect the buffer circuit~~ and the second ~~power source~~ wiring ~~line.~~line are electrically connected.

11. (Previously Presented) The semiconductor device as set forth in claim 7,

the buffer circuit including a first NOT circuit to which the first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

each of the first and second NOT circuits consisting of a complementary-type transistor; and

a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit.

12. (Previously Presented) The semiconductor device as set forth in claim 7,

the first wiring line comprising a high potential power source wiring line supplying a power source potential to the semiconductor circuit; and

the second wiring line comprising a low potential power source wiring line supplying a power source potential to the semiconductor.

13. (Canceled)

14. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a substrate on which the semiconductor circuit is arranged;

the wiring ~~line~~ lines being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

15. (Original) A display device provided with the semiconductor device as set forth in claim 7.

16. (Previously Presented) An electronic device provided with the semiconductor device as set forth in claim 7.

17. (New) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

a power source line that supplies a power source to the driving circuit; and

first and second protection circuits that are electrically connected to the power source line;

the driving circuit being electrically connected to the power source line between the first and second protection circuits.

18. (New) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

a power source line that supplies a power source to the driving circuit;

first and second protection circuits that are electrically connected to the power source line;

a first connecting point at which the first protection circuit is electrically connected to the power source line;

a second connecting point at which the second protection circuit is electrically connected to the power source line; and

a third connecting point at which the driving circuit is electrically connected to the power source line;

the third connecting point being positioned between the first and second connecting points.

19. (New) The display device as set forth in claim 17, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

20. (New) The display device as set forth in claim 18, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

21. (New) The display device as set forth in claim 18, further comprising:

an input terminal that is electrically connected to the power source line;

the first connecting point being positioned between the input terminal and the third connecting point.

22. (New) An electronic device provided with the display device as set forth in claim 18.

23. (New) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line;

first and second protection circuits that are electrically connected to the first power source line; and

third and fourth protection circuits that are electrically connected to the second power source line;

the driving circuit being electrically connected to the first power source line between the first and second protection circuits, and being electrically connected to the second power source line between the third and fourth protection circuits.

24. (New) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line;

first and second protection circuits that are electrically connected to the first power source line;

third and fourth protection circuits that are electrically connected to the second power source line;

a first connecting point at which the first protection circuit is electrically connected to the first power source line;

a second connecting point at which the second protection circuit is electrically connected to the first power source line;

a third connecting point at which the third protection circuit is electrically connected to the second power source line;

a fourth connecting point at which the fourth protection circuit is electrically connected to the second power source line;

a fifth connecting point at which the driving circuit is electrically connected to the first power source line; and

a sixth connecting point at which the driving circuit is electrically connected to the second power source line;

the fifth connecting point being positioned between the first and second connecting points, and the sixth connecting point being positioned between the third and fourth connecting points.

25. (New) The display device as set forth in claim 23, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

26. (New) The display device as set forth in claim 24, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

27. (New) The display device as set forth in claim 24, further comprising:

a first input terminal that is electrically connected to the first power source line; and

a second input terminal that is electrically connected to the second power source line;

the first connecting point being positioned between the first input terminal and the fifth connecting point, and the third connecting point being positioned between the second input terminal and the sixth connecting point.

28. (New) An electronic device provided with the display device as set forth in claim 24.

REMARKS

Claims 1-3, 5-12 and 14-28 are pending in this application. By this Amendment, claims 1, 2, 7-10 and 14 are amended, and claims 17-28 are added. Support for the amendments to the claims can be found, for example, in the original claims and in Figs. 1-3, 8 and 11. No new matter is added. Claims 4 and 13 are canceled without prejudice to, or disclaimer to, the subject matter recited in those claims. A Request for Continued Examination is attached. Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Rejection Under 35 U.S.C. §112

The Office Action rejects claims 4, 9 and 13 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. The rejection is respectfully traversed.

To expedite allowance of the application, by this Amendment, claims 4 and 13 are canceled. Thus, the rejection of claims 4 and 13 is moot.

With respect to the rejection of claim 9, claim 9 is amended to recite "the first wiring line" and "the second wiring line" to obviate the rejection.

Accordingly, withdrawal of the rejections under §112 is respectfully requested.

Rejection Under 35 U.S.C. §102

The Office Action rejects claims 1-8 and 12-16 under 35 U.S.C. §102(b) over U.S. Patent No. 5,936,687 to Lee. The rejection is respectfully traversed.

The Office Action alleges that the pixels formed at the corner between line 20 and line 30 illustrated in Fig. 5 of Lee correspond to the claimed semiconductor circuit. The Office Action also alleges that the lower bank of protection diodes 50 along lines 52 and 53 in Fig. 5 of Lee correspond to the claimed first protection circuit, and that the bank of protection diodes 50 along the upper portion of Fig. 5 correspond to the claimed second protection circuit. Applicant respectfully disagrees.

Specifically, the pixels of Lee cannot reasonably be considered to correspond to the claimed semiconductor circuit. For example, as described in the present specification, one possibility for the semiconductor circuit is the scanning line driving circuit 800 (see paragraph [0037]). One of ordinary skill in the art would recognize that the pixels of Lee do not correspond to the claimed semiconductor circuit.

Instead, the driving elements 70 of Lee more reasonably could be considered to correspond to the claimed semiconductor circuit. However, the driving elements 70 of Lee do not have the claimed first and second protection circuits arranged as recited in the claims.

Further, Lee discloses that gate lines 20 supply gate signals, and data lines 30 supply data signals from the driving elements 70. Thus, the alleged protection circuits of Lee protect pixels connected to gate lines and data lines (signal lines). However, independent claims 1 and 7 recite wiring lines to supply power. That is, the claimed wiring line is a power source line, not a signal line as disclosed in Lee.

Thus, Lee fails to disclose each of the features recited in independent claims 1 and 7, and independent claims 1 and 7 are patentable over Lee. Claims 2-6, 8 and 12-16 depend from independent claims 1 and 7 and are, therefore, also patentable over Lee at least for the dependence, as well as for the additional features these claims recite.

Accordingly, withdrawal of the rejection is respectfully requested.

Also, added claims 17-28 specifically recite a driving circuit. Lee clearly fails to disclose the claimed driving circuit, in combination with the other features recited in added claims 17-28.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 9 and 10 under 35 U.S.C. §103(a) over Lee in view of U.S. Patent No. 6,075,686 to Ker; and rejects claim 11 under 35 U.S.C. §103(a) over Lee

in view of U.S. Patent No. 5,329,185 to Cooperman et al. (Cooperman). These rejections are respectfully traversed.

Claims 9-11 depend from independent claim 7. Ker and Cooperman fail to overcome the deficiencies of Lee with respect to independent claim 7, as discussed above. Accordingly, independent claim 7 is also patentable over the combination of Lee, Ker and Cooperman, and claims 9-11 are patentable over the combination at least for their dependence from independent claim 7, as well as for the additional features these claims recite.

Accordingly, withdrawal of the rejections is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Ryan M. Crockett
Registration No. 62,945

JAO:RMC/hs

Attachments:
Petition for Extension of Time
Request for Continued Examination
Amendment Transmittal

Date: June 2, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
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RCE# / DWD

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date June 2, 2011



In re the Application of

Yutaka KOBASHI

Application No.: 12/436,335

Filed: May 6, 2009

Group Art Unit: 2836

Examiner: T. MAI

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

LARGE ENTITY PETITION FOR 1st - 3rd EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a) AND TRANSMITTAL OF FEE UNDER 37 C.F.R. §1.17

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a response to the outstanding Official Action in the above-identified patent application. The shortened statutory period having expired May 2, 2011, an extension of time for a period of ONE month is hereby requested. Attached hereto is our Check No. 237800 in the amount of $130.00 in payment for:

XX Extension fee for response within first month pursuant to §1.136(a) ($130.00)

____ Extension fee for response within second month pursuant to §1.136(a) ($490.00)

____ Extension fee for response within third or subsequent month pursuant to §1.136(a) ($1,110.00)

The Commissioner is hereby authorized to charge any additional fee or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Ryan M. Crockett
Registration No. 62,945

JAO:RMC/plj

06/03/2011 SMOHAMME 00000088 12436335
01 FC:1251 130.00 OP

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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/436,335	05/06/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 06/02/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 26	Minus	** 26	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DAVID SASFAI/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 07/06/2012
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
07/06/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-3,5-12 and 14-28* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-3,5-12 and 14-28* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/02/2011 has been entered. Upon entering amendment, claims 1, 2, 7-10 and 14 have been amended; claims 17-28 have been added. Claims 4 and 13 have been added.

Response to Arguments

2. Applicant's arguments filed 06/02/2011 have been fully considered but they are not persuasive for the reasons discussed below.

3. Applicant argues that one of ordinary skill in the art would recognize that the pixels of Lee do not correspond to the claimed semiconductor circuit. The Applicant does not provide any evidence or believes why the pixel of Lee cannot read on the semiconductor circuit. However, Lee explicitly discloses the pixel formed by semiconductor circuit which includes transistors and capacitors (see fig. 9).

4. Applicant also argues that the claimed wiring line is a power source line, not a signal line as disclosed in Lee. The Examiner takes a broadest reasonable interpretation therefore since the claim does not explicitly say the line only be the power

supply line it is reasonable that ordinary skill in the art understands the wiring line can be both power line and signal line.

Claim Rejections - 35 USC § 102

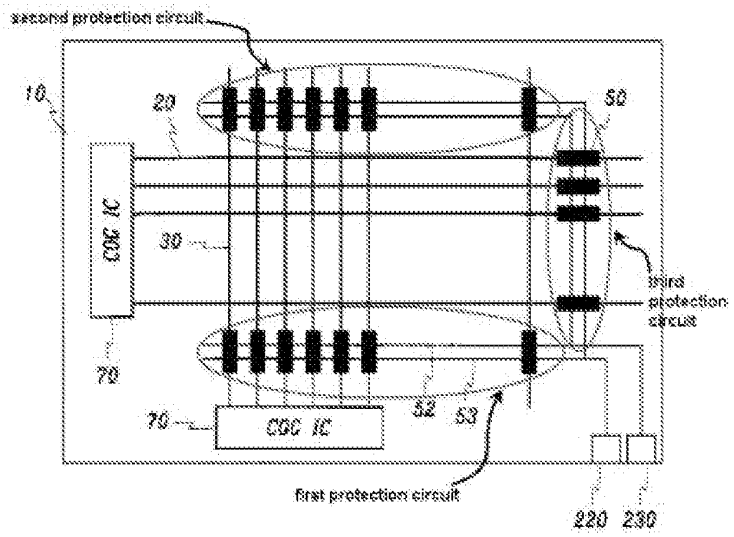
5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-8, 12 and 14-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,936,687, "Lee").

7. **Regarding claim 1**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure below) comprising: a semiconductor circuit (pixels that are at corner between line 20 and line 30); a wiring line (20, 30, 52 and 53) electrically connected to the semiconductor circuit; an input terminal (220 and 230) electrically connected to the wiring line to supply power; and a first protection circuit and a second protection circuit that are electrically connected to the wiring line to protect the semiconductor circuit; the first protection circuit being electrically connected to the wiring line between (i) a first connecting portion at which the semiconductor circuit and the wiring line are electrically connected and (ii) the input terminal; and the semiconductor circuit being electrically connected to the wiring line between (iii) a second connecting portion at which the first protection circuit and the wiring line are electrically connected and (iv) a third connecting

portion at which the second protection circuit and the wiring line are electrically connected.



8. **Regarding claim 2**, Lee discloses a plurality of semiconductor circuits being electrically connected to the wiring line; and a third protection circuit being electrically connected to the wiring line to protect the plurality of semiconductor circuits, the third protection circuit being connected to the wiring line between at least one set of connecting portions of two consecutive semiconductor circuits of the plurality of semiconductor circuit and the wiring line.

9. **Regarding claim 3**, Lee discloses the wiring line being at least one of a low potential power source wiring line (GND) or a high potential power source wiring line (10V) supplying a power source potential to the semiconductor circuit for protection purpose (see fig. 6).

10. **Regarding claim 5**, Lee discloses a substrate (glass substrate); the semiconductor circuit being arranged on the substrate (col. 1, line 14); the wiring line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate (at least portion of the wiring lines arrange on the right side of the substrate); the first protection circuit being arranged in the first corner portion of the substrate (at least one of the first protection circuits arranges on lower right corner); the second protection circuit being arranged in the second corner portion of the substrate (at least one of the second protection circuits arranges on upper right corner).

11. **Regarding claim 6**, Lee discloses that the display device is an electronic device.

12. **Regarding claim 7**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection circuit, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a first wiring line (52) electrically connected to a first terminal portion (230) to which a first power is supplied; a second wiring line (53) electrically connected to a second terminal portion (220) to which a second power is supplied; a semiconductor circuit (pixels that are at corner between line 20 and line 30) electrically connected to the first wiring line and the second wiring line; a first protection circuit being electrically connected to the first wiring line to protect the semiconductor circuit, the first protection circuit being electrically connected to the first wiring line between (i) a first connecting portion at which the semiconductor circuit and the first wiring line are electrically connected and (ii) the first terminal portion; a second protection circuit being electrically connected to the second wiring line to protect the semiconductor circuit, the second protection circuit being electrically connected to the second wiring line between

(iii) a second connecting portion at which the semiconductor circuit and the second wiring line are electrically connected and (iv) the second portion; and a buffer circuit (inverter in figure 11). The buffer circuit inherently electrically connects to the first wiring line between (v) the first connecting portion at which the semiconductor circuit and the first wiring line are electrically connected and (vi) the first terminal portion to fulfill its function, as evidenced by Hatzilambrou et al. (UC 6,801,416). Hatzilambrou discloses a semiconductor structure level of an inverter circuit (510 and 520) including output/input terminals and connected to a high potential line (Vdd), a low potential line (Vss), wherein the inverter circuit outputs high when it receives logic low and via versa (also see http://en.wikipedia.org/wiki/Inverter_(logic_gate)).

13. **Regarding claim 8**, Lee discloses a plurality of semiconductor circuits being electrically connected to the wiring line; and a third protection circuit being electrically connected to the first wiring line to protect the plurality of semiconductor circuits, the third protection circuit being electrically connected to the first wiring line between adjacent sets of connecting portions of the semiconductor circuits of the plurality of semiconductor circuits and the first wiring line. Lee discloses in figure 5 that the third protection circuit protects lines 20 against ESD. Lee also discloses in figure 6 that each of the ESD protection circuit comprises two diodes to protect line 30. Lee further discloses in figure 10 that diode d59 connects between at least one set of connecting portions of two adjacent set of semiconductor circuits (b and d) to protect the semiconductor circuits since both gates of semiconductor circuits (b and d) connect to cathode of diode d59.

14. **Regarding claim 12**, Lee discloses the first wiring line comprising high potential power source wiring line supplying a power source potential to the semiconductor circuit for protection purpose; and the second wiring line comprising a low potential power source wiring line supplying a power source potential to the semiconductor circuit also for protection purpose (see fig. 6).

15. **Regarding claim 14**, Lee discloses a substrate (col. 1, line 19) on which the semiconductor circuit is arranged; the wiring line being formed at first and second corner portions of the substrate so as to follow a periphery of the substrate; the first protection circuit being arranged in the first corner portion of the substrate (at least one of the first protection circuits arranges on lower right corner); the second protection circuit being arranged in the second corner portion of the substrate (at least one of the second protection circuits arranges on upper right corner).

16. **Regarding claim 15**, Lee discloses the apparatus is a display device (title).

17. **Regarding claim 16**, Lee discloses the apparatus comprising an electronic device (gate and data drive circuits).

18. **Regarding claim 17**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; a power source line (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit; and first and second

protection circuits that are electrically connected to the power source line; the driving circuit being electrically connected to the power source line between the first and second protection circuits.

19. **Regarding claim 18**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; a power source line (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit; and first and second protection circuits that are electrically connected to the power source line; a first connecting point at which the first protection circuit is electrically connected to the power source line; a second connecting point at which the second protection circuit is electrically connected to the power source line; and a third connecting point at which the driving circuit is electrically connected to the power source line; the third connecting point being positioned between the first and second connecting points.

20. **Regarding claims 19, 20, 25 and 26**, Lee discloses a region in which a plurality of the pixels arranged; the driving circuit being positioned outside of the region (see figure 5).

21. **Regarding claim 21**, Lee discloses an input terminal (220 and 230) electrically connected to the power source line; the first connecting point positioned between the input terminal and the third connecting point.

22. **Regarding claim 22**, Lee discloses the apparatus is a display device (title).

23. **Regarding claim 23**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; first and second power source lines (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit, a potential of the second power source line (220) being lower than that of the first power source line (230); first and second protection circuits (lower and upper) that are electrically connected to the first power source line; and third and fourth protection circuits (two upper and two lower further to the right in figure 5 that corresponds to the third and fourth protection circuits that are electrically connected to the second power source line; the driving circuit being electrically connected to the first power source line between the first and second protection circuits, and being electrically connected to the second power source line between the third and fourth protection circuits (see fig. 5).

24. **Regarding claim 24**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; first and second power source lines (52, 53 and other power lines that are not shown in the figure to supply

power to the driving circuit) that supplies a power source to the driving circuit, a potential of the second power source line (220) being lower than that of the first power source line (230); first and second protection circuits (lower and upper) that are electrically connected to the first power source line; third and fourth protection circuits (two upper and two lower further to the right in figure 5 that corresponds to the third and fourth protection circuits) that are electrically connected to the second power source line; a first connecting point at which the first protection circuit is electrically connected to the first power source line; a second connecting point at which the second protection circuit is electrically connected to the first power source line; a third connecting point at which the third protection circuit is electrically connected to the second power source line; a fourth connecting point at which the fourth protection circuit is electrically connected to the second power source line; a fifth connecting point at which the driving circuit is electrically connected to the first power source line; and a six connecting point at which the driving circuit is electrically connected to the second power source line; the fifth connecting point being positioned between the first and second connecting points, and the sixth connecting point being positioned between the third and fourth connecting points (see fig. 5).

25. **Regarding claim 27**, Lee discloses a first input terminal (230) electrically connected to the first power source line; and a second input terminal (220) electrically connected to the second power source line; the first connecting point being positioned between the first input terminal and the fifth connecting point, and the third connecting point being positioned between the second input terminal and the six connecting point.

26. **Regarding claim 28**, Lee discloses the apparatus is a display device (title).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Ker (US 6,075,686, “Ker”).

29. **Regarding claim 9**, Lee discloses the buffer circuit arranged between the first and second wiring lines (as discussed in claim 7); a fourth protection circuit (d41); a fifth protection circuit (d42); the buffer circuit electrically connected to the first wiring line between (vii) a fourth connecting portion at which the fourth protection circuit and the first wiring line are electrically connected and (viii) a fifth connecting portion at which the first protection circuit and the first wiring line are electrically connected (for powering the buffer); the buffer circuit electrically connected to the second wiring line between (ix) a sixth connecting portion at which the fifth protection circuit and the second wiring line are electrically connected and (x) a seventh connecting portion at which the second protection circuit and the second wiring line are electrically connected (for powering the buffer circuit). Lee does not explicitly disclose each of the buffer circuit protected by the fourth and fifth protection circuits. Ker discloses in figure 5 that buffer circuits (48 and 50) connect to a high potential line (38 and 42) and a low potential line (40 and 44) and

arranged from one end to the other end, wherein each of the buffer circuits are protected by ESD protection circuit (Dp1, Dn1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Lee and utilize protection circuits, as taught by Ker, in order to protect each of the buffer circuit against ESD pulses at the signal input.

30. **Regarding claim 10**, Lee discloses wring line (450) including the buffer circuit, wherein the buffer circuit includes a first NOT circuit to which the first power is input and a second NOT circuit electrically connects to the first NOT circuit in series. Lee also discloses a sixth protection circuit (d45) and a seventh protection circuit (d46). Lee does not explicitly disclose the sixth protection circuit connected to the first wiring line between a connecting portion of the first NOT circuit and the first wiring line and a connecting portion of the second NOT circuit and the first wiring line; and the seventh protection circuit connected to the second wiring line between a connecting portion of the first NOT circuit and the second wiring line and a connecting portion of the second NOT circuit and the second power source wiring line. Ker discloses in figure 7 that sixth and second protection circuits (Mp4 and Mn4) connect between first and second buffer circuits (48 and 50) to protect the buffer circuits against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Lee and utilize protection circuits, as taught by Ker, in order to protect each of the buffer circuit against ESD pulses.

31. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Cooperman et al. (US 5,329,185, "Cooperman").

32. Lee discloses in figure 11 that the buffer circuit including a first NOT circuit to which the first power is input (power supply as discussed in claim 7) and a second NOT circuit electrically connected to the first NOT circuit in series. Lee does not explicitly disclose each of the first and second NOT circuits consisting of complementary type transistor; and a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit. Cooperman discloses each of first and second NOT circuits consisting of a complementary type transistor (see fig. 1); and channel width of transistor of the first transistor being larger than a channel width of the transistor of the second NOT circuit. Cooperman discloses that increasing the width of the channel transistor of the buffer will increase operating speed (abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Lee LCD and utilize speed control by increasing a channel width of the transistor, as taught by Cooperman, in order to increase speed operation (abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can

be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tien Mai/
Examiner, Art Unit 2836
0/26/2012

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2836

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 11/13/2012

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
11/13/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

All participants (applicant, applicant's representative, PTO personnel):

(1) *TIEN MAI*.

(2) *David Zibelli*.

(3) *Rexford Barnie*.

(4)_____.

Date of Interview: *16 October 2012*.

Type: ☐ Telephonic ☐ Video Conference
☒ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1 and 17*.

Identification of prior art discussed: *Lee (US 5,936,687)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant presented amended claims and also argued that Lee does not disclose the limitations of claim 17; however, no agreement was reached.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

	/Rexford N BARNIE/ Supervisory Patent Examiner, Art Unit 2836

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI	Group Art Unit: 2836
Application No.: 12/436,335	Examiner: T. MAI
Filed: May 6, 2009	Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the July 6, 2012 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a ~~semiconductor~~ scanning line driving circuit;

a ~~wiring~~ power supply line electrically connected to the ~~semiconductor~~ scanning line driving circuit;

an input terminal electrically connected to the ~~wiring~~ power supply line to supply power; and

a first protection circuit and a second protection circuit that are electrically connected to the ~~wiring~~ power supply line to protect the ~~semiconductor~~ scanning line driving circuit;

the first protection circuit being electrically connected to the ~~wiring~~ power supply line between (i) a first connecting portion at which the ~~semiconductor~~ scanning line driving circuit and the ~~wiring~~ power supply line are electrically connected and (ii) the input terminal; and

the ~~semiconductor~~ scanning line driving circuit being electrically connected to the ~~wiring~~ power supply line between (iii) a second connecting portion at which the first protection circuit and the ~~wiring~~ power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the ~~wiring~~ power supply line are electrically connected.

2. (Currently Amended) The display device as set forth in claim 1, further comprising:

a plurality of ~~semiconductor~~ scanning line driving circuits being electrically connected to the ~~wiring~~ power supply line; and

a third protection circuit being electrically connected to the ~~wiring~~ power supply line to protect the plurality of ~~semiconductor~~ scanning line driving circuits, the third protection circuit being connected to the ~~wiring~~ power supply line between at least one set of connecting portions of two consecutive ~~semiconductor~~ scanning line driving circuits of the plurality of ~~semiconductor~~ scanning line driving circuits and the ~~wiring~~ power supply line.

3. (Currently Amended) The display device as set forth in claim 1, the ~~wiring~~ power supply line being at least one of a low potential power source wiring line or a high potential power source wiring line supplying a power source potential to the ~~semiconductor~~ scanning line driving circuit.

4. (Canceled)

5. (Currently Amended) The display device as set forth in claim 1, further comprising:

a substrate;

the ~~semiconductor~~ scanning line driving circuit being arranged on the substrate;

the ~~wiring~~ power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7. (Currently Amended) A semiconductor device, comprising:

a first ~~wiring~~ power supply line electrically connected to a first terminal portion to which a first power is supplied;

a second ~~wiring~~ power supply line electrically connected to a second terminal portion to which a second power is supplied;

a ~~semiconductor~~ scanning line driving circuit electrically connected to the first ~~wiring~~ power supply line and the second ~~wiring~~ power supply line;

a first protection circuit being electrically connected to the first ~~wiring~~ power supply line to protect the ~~semiconductor~~ scanning line driving circuit, the first protection circuit being electrically connected to the first ~~wring~~ power supply line between (i) a first connecting portion at which the ~~semiconductor~~ scanning line driving circuit and the first ~~wiring~~ power supply line are electrically connected and (ii) the first terminal portion;

a second protection circuit being electrically connected to the second ~~wiring~~ power supply line to protect the ~~semiconductor~~ scanning line driving circuit, the second protection circuit being electrically connected to the second ~~wiring~~ power supply line between (iii) a second connecting portion at which the ~~semiconductor~~ scanning line driving circuit and the second ~~wiring~~ power supply line are electrically connected and (iv) the second terminal portion; and

a buffer circuit being electrically connected to the first ~~wiring~~ power supply line between (v) the first connecting portion at which the ~~semiconductor~~ scanning line driving circuit and the first ~~wiring~~ power supply line are electrically connected and (vi) the first terminal portion.

8. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a plurality of ~~semiconductor~~ scanning line driving circuits being electrically connected to the ~~wiring~~ power supply line; and

a third protection circuit being electrically connected to the first ~~wiring~~ power supply line to protect the plurality of ~~semiconductor~~ scanning line driving circuits, the third protection circuit being electrically connected to the first ~~wiring~~ power supply line between adjacent sets of connecting portions of the ~~semiconductor~~ scanning line driving circuits of the plurality of ~~semiconductor~~ scanning line driving circuits and the first ~~wiring~~ power supply line to protect the plurality of ~~semiconductor~~ scanning line driving circuits.

9. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a second power ~~source wiring~~supply line branched from a low potential power source wiring;

the buffer circuit being arranged between the first and second ~~wiring~~ power supply lines;

a fourth protection circuit being electrically connected to the first ~~wiring~~ power supply line to protect the ~~semiconductor~~ scanning line driving circuit and the buffer circuit;

a fifth protection circuit being electrically connected to the second ~~wiring~~ power supply line to protect the ~~semiconductor~~ scanning line driving circuit and the buffer circuit;

the buffer circuit being electrically connected to the first ~~wiring~~ power supply line between (vii) a fourth connecting portion at which the fourth protection circuit and the first ~~wiring~~ power supply line are electrically connected and (viii) a fifth connecting portion at which the first protection circuit and the first ~~wiring~~ power supply line are electrically connected; and

the buffer circuit being electrically connected to the second ~~wiring~~ power supply line between (ix)a sixth connecting portion at which the fifth protection circuit and the

second ~~wiring~~ power supply line are electrically connected and (x) a seventh connecting portion at which the second protection circuit and the second ~~wiring~~ power supply line are electrically connected.

10. (Currently Amended) The semiconductor device as set forth in claim 9, further comprising:

the buffer circuit including a first NOT circuit to which the first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

a sixth protection circuit being electrically connected to the first ~~wiring~~ power supply line to protect the buffer circuit, the sixth protection circuit being electrically connected to the first ~~wiring~~ power supply line between (xi) an eighth connecting portion at which the first NOT circuit and the first ~~wiring~~ power supply line are electrically connected and (xii) a ninth connecting portion at which the second NOT circuit and the first ~~wiring~~ power supply line are electrically connected; and

a seventh protection circuit being electrically connected to the second ~~wiring~~ power supply line to protect the buffer circuit, the seventh protection circuit being electrically connected to the second ~~wiring~~ power supply line between (xiii) a tenth connecting portion at which the first NOT circuit and the second ~~wiring~~ power supply line are electrically connected and (xiv) an eleventh connecting portion at which the second NOT circuit and the second ~~wiring~~ power supply line are electrically connected.

11. (Previously Presented) The semiconductor device as set forth in claim 7,

the buffer circuit including a first NOT circuit to which the first power is input and a second NOT circuit electrically connected to the first NOT circuit in series;

each of the first and second NOT circuits consisting of a complementary-type transistor; and

a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit.

12. (Currently Amended) The semiconductor device as set forth in claim 7,

the first ~~wiring~~ power supply line comprising a high potential power source wiring line supplying a power source potential to the ~~semiconductor~~ scanning line driving circuit; and

the second ~~wiring~~ power supply line comprising a low potential power source wiring line supplying a power source potential to the ~~semiconductor~~scanning line driving circuit.

13. (Canceled)

14. (Currently Amended) The semiconductor device as set forth in claim 7, further comprising:

a substrate on which the ~~semiconductor~~ scanning line driving circuit is arranged;

the ~~wiring~~ power supply lines being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate;

the first protection circuit being arranged in the first corner portion of the substrate; and

the second protection circuit being arranged in the second corner portion of the substrate.

15. (Original) A display device provided with the semiconductor device as set forth in claim 7.

16. (Previously Presented) An electronic device provided with the semiconductor device as set forth in claim 7.

17. (Previously Presented) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

a power source line that supplies a power source to the driving circuit; and

first and second protection circuits that are electrically connected to the power source line;

the driving circuit being electrically connected to the power source line between the first and second protection circuits.

18. (Previously Presented) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

a power source line that supplies a power source to the driving circuit;

first and second protection circuits that are electrically connected to the power source line;

a first connecting point at which the first protection circuit is electrically connected to the power source line;

a second connecting point at which the second protection circuit is electrically connected to the power source line; and

a third connecting point at which the driving circuit is electrically connected to the power source line;

the third connecting point being positioned between the first and second connecting points.

19. (Previously Presented) The display device as set forth in claim 17, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

20. (Previously Presented) The display device as set forth in claim 18, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

21. (Previously Presented) The display device as set forth in claim 18, further comprising:

an input terminal that is electrically connected to the power source line;

the first connecting point being positioned between the input terminal and the third connecting point.

22. (Previously Presented) An electronic device provided with the display device as set forth in claim 18.

23. (Previously Presented) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line;

first and second protection circuits that are electrically connected to the first power source line; and

third and fourth protection circuits that are electrically connected to the second power source line;

the driving circuit being electrically connected to the first power source line between the first and second protection circuits, and being electrically connected to the second power source line between the third and fourth protection circuits.

24. (Previously Presented) A display device, comprising:

a scanning line;

a data line;

a pixel arranged corresponding to an intersection of the scanning line and the data line;

a driving circuit that outputs a driving signal to the pixel;

first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line;

first and second protection circuits that are electrically connected to the first power source line;

third and fourth protection circuits that are electrically connected to the second power source line;

a first connecting point at which the first protection circuit is electrically connected to the first power source line;

a second connecting point at which the second protection circuit is electrically connected to the first power source line;

a third connecting point at which the third protection circuit is electrically connected to the second power source line;

a fourth connecting point at which the fourth protection circuit is electrically connected to the second power source line;

a fifth connecting point at which the driving circuit is electrically connected to the first power source line; and

a sixth connecting point at which the driving circuit is electrically connected to the second power source line;

the fifth connecting point being positioned between the first and second connecting points, and the sixth connecting point being positioned between the third and fourth connecting points.

25. (Previously Presented) The display device as set forth in claim 23, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

26. (Previously Presented) The display device as set forth in claim 24, further comprising:

a region in which a plurality of the pixels are arranged;

the driving circuit being positioned outside of the region.

27. (Previously Presented) The display device as set forth in claim 24, further comprising:

a first input terminal that is electrically connected to the first power source line; and

a second input terminal that is electrically connected to the second power source line;

the first connecting point being positioned between the first input terminal and the fifth connecting point, and the third connecting point being positioned between the second input terminal and the sixth connecting point.

28. (Previously Presented) An electronic device provided with the display device as set forth in claim 24.

REMARKS

Claims 1-3, 5-12 and 14-28 are pending in this application. By this Amendment, 1-3, 5, 7-10, 12 and 14 are amended. No new matter is added. Reconsideration of the rejections is requested based on the amendments and the following remarks.

On October 16, 2012 a personal interview was conducted with Examiner Mai and Supervisory Patent Examiner Barnie. The Examiners are thanked for the courtesies extended to Applicant's representative. The substance of the interview is incorporated into the following remarks.

1. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claims 1-3, 5-8, 12 and 14-28 under 35 U.S.C. §102(b) over Lee (U.S. Pat. No. 5,936,687) and rejects claims 9 and 10 under 35 U.S.C. §103(a) over Lee in view of Ker (U.S. Pat. No. 6,075,686). These rejections are respectfully traversed.

Regarding independent claims 1 and 7, the Office Action asserts that Lee discloses all of the recited elements. Regarding claim 1, and as similarly recited in claim 7, Lee does not disclose "a first protection circuit and a second protection circuit that are electrically connected to the power supply line to protect the scanning line driving circuit; the first protection circuit being electrically connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal; and the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected" as recited in claim 1. Ker does not solve the deficiencies of Lee.

In particular, Lee does not disclose a first protection circuit and a second protection circuit that are electrically connected to the power supply line to protect the scanning line

driving circuit. In Lee, the element corresponding to the scanning line driving circuit is driving element 70. Lee does not have first and second protection circuits that protect the scanning line driving circuit. Further, Lee does not disclose the first protection circuit being electrically connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal; or the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected.

Lee does not disclose any power supply lines connected to the driving circuit 70 (the scanning line driving circuit) much less the first protection circuit being electrically connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal; the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected.

During the interview, Examiner Mai asserted that the driving element 70 of Lee would inherently have a power supply to receive power. The Examiner further asserted that the inherent power supply connected to the driving element 70 of Lee could be a common power supply supplying power to the pads 220, 230 and driving element 70 of Lee, and that such an interpretation could read on the claims of the present application. Applicant's representative first pointed out that even if the driving element 70 of Lee did have a power supply, there is no disclosure of any first and second protection circuits that protect the driving circuit, or the first protection circuit being electrically connected to the power supply

line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal; the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected, as recited in independent claim 1 and similarly recited in independent claim 7.

Applicant's representative further pointed out during the interview that lines 52 and 53 are not power supply lines, but are shorting lines connected to the diodes, which are used to dissipate the electrostatic charges. While the specification of Lee indicates that voltages of 0V and 10V may be applied to the pads 220 and 230, Lee indicates that such is done as a method for testing display quality of an LCD before assembling the substrate for an LCD. See col. 4, lines 19-24. Thus, once the LCD is assembled, the pads will not be supplied with power, as such would cause the shorting lines 52 and 53 to not function as shorting lines for the needed ESD protection. Thus, the shorting lines 52 and 53 are not power supply lines as asserted by the Examiner. That they may be incidentally disclosed as useful for testing the LCD by applying power prior to assembly to test for disconnection of the data line does not make 52 and 53 power supply lines.

Further, one or ordinary skill in the art would not have been motivated to modify Lee to use a common power supply to supply power to the driving element 70 and the shorting lines 52 and 53 as asserted by the Examiner. As pointed out above, the shorting lines 52 and 53 are used to dissipate electrostatic discharge from the pixels, and thus are shorted or grounded, and do not receive power. Accordingly, one of ordinary skill, if modifying Lee to connect a power supply to driving element 70, would not also connect the power supply to the pads 220, 230 and hence to the shorting lines, because applying power to the shorting

lines would cause them not to function for their intended purpose of shorting and dissipating the electrostatic charges.

Moreover, even if one of ordinary skill were to modify Lee as suggested by the Examiner during the interview to connect a power supply to the driving element 70 and the pads 220, 230 of Lee (which one of ordinary skill would not be motivated to do), such would still not result in structure to read on the claims of the present application. Regarding claims 1 and 7, even with the Examiner's suggested modification of Lee, Lee would still not disclose: 1) a first protection circuit and a second protection circuit that are electrically connected to the power supply line to protect the scanning line driving circuit; 2) the first protection circuit being electrically connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal; or 3) the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected, as recited in independent claim 1 and similarly recited in independent claim 7.

Regarding feature 1), Lee as modified by the Examiner's suggestion would not disclose this feature because the power supply as suggested by the Examiner would be connected directly to both the pads 220, 230 and to the driving element 70. The direct connection to the driving element 70 would not provide a "first protection circuit and a second protection circuit that are electrically connected to the power supply line to protect the scanning line driving circuit" but would instead provide protection circuits connected to the data lines 30 to protect the pixel circuits.

Regarding feature 2), Lee as modified by the Examiner's suggestion would not disclose this feature because the power supply would be connected directly to the driving element 70, and thus would not include "the first protection circuit being electrically connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal."

Regarding feature 3), Lee as modified by the Examiner's suggestion would not disclose this feature because the power supply would be directly connected to the driving element 70, and thus would not include "the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are electrically connected."

For at least the above reasons, independent claims 1 and 7, and all claims dependent therefrom, are not anticipated by Lee. Claims 9 and 10 would not have been obvious over Lee in view of Ker due to their dependence from claim 7, and because Ker does not solve the deficiencies of Lee.

Regarding independent claim 17, the applied references do not disclose at least "the driving circuit being electrically connected to the power source line between the first and second protection circuits." Even if Lee had a power supply connected to the driving circuit 70, Lee has no disclosure that it would be other than directly connected to the driving circuit 70, and does not disclose at least "the driving circuit being electrically connected to the power source line between the first and second protection circuits."

Regarding independent claim 18, the applied references do not disclose at least "a first connecting point at which the first protection circuit is electrically connected to the power

source line; a second connecting point at which the second protection circuit is electrically connected to the power source line; and a third connecting point at which the driving circuit is electrically connected to the power source line; the third connecting point being positioned between the first and second connecting points.

Regarding independent claim 23, the applied references do not disclose at least "first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line; first and second protection circuits that are electrically connected to the first power source line; and third and fourth protection circuits that are electrically connected to the second power source line; the driving circuit being electrically connected to the first power source line between the first and second protection circuits, and being electrically connected to the second power source line between the third and fourth protection circuits.

Regarding independent claim 24, the applied references do not disclose at least "a driving circuit that outputs a driving signal to the pixel; first and second power source lines that supply a power source to the driving circuit, a potential of the second power source line being lower than that of the first power source line; first and second protection circuits that are electrically connected to the first power source line; third and fourth protection circuits that are electrically connected to the second power source line; a first connecting point at which the first protection circuit is electrically connected to the first power source line; a second connecting point at which the second protection circuit is electrically connected to the first power source line; a third connecting point at which the third protection circuit is electrically connected to the second power source line; a fourth connecting point at which the fourth protection circuit is electrically connected to the second power source line; a fifth connecting point at which the driving circuit is electrically connected to the first power source line; and a sixth connecting point at which the driving circuit is electrically connected

to the second power source line; the fifth connecting point being positioned between the first and second connecting points, and the sixth connecting point being positioned between the third and fourth connecting points."

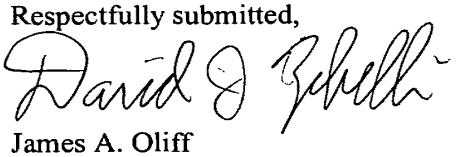
For at least the above reasons, independent claims 17, 18, 23 and 24, and all claims dependent therefrom, are not anticipated by Lee. Withdrawal of the rejection is requested.

2. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Attachment:
Petition for Extension of Time

Date: November 27, 2012

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

OPAP
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PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

LARGE ENTITY PETITION FOR 1st - 3rd EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a) AND TRANSMITTAL OF FEE UNDER 37 C.F.R. §1.17

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a response to the outstanding Official Action in the above-identified patent application. The shortened statutory period having expired October 6, 2012, an extension of time for a period of two months is hereby requested. Attached hereto is our Check No. 249147 in the amount of $570.00 in payment for:

_____ Extension fee for response within first month pursuant to §1.136(a) ($150.00)

XXX Extension fee for response within second month pursuant to §1.136(a) ($570.00)

_____ Extension fee for response within third or subsequent month pursuant to §1.136(a) ($1,290.00)

The Commissioner is hereby authorized to charge any additional fee or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

11/28/2012 CCHAU1 00000029 12436335
01 FC:1252 570.00 OP

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: November 27, 2012

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/436,335	05/06/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/27/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 26	Minus	** 26	= 0	X $ =		OR	X $62=	0
Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Tina J. Barden/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 02/20/2013
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
02/20/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-3,5-12 and 14-28* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-3,5-8,11,12 and 14-28* is/are rejected.

8)☒ Claim(s) *9 and 10* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response of 11/27/2012 has been entered and considered. Upon entering amendment, claims 1-3, 5, 7-10, 12 and 14 have been amended.

Drawings

2. Figure 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of 35 U.S.C. 112(b):

(B) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the

subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. It is not understood what is meant by “the second power supply line” in lines 5-6. It is not clear which second power supply line applicant prefers to since both claims 7 and 9 recites “a second power supply line”.

Response to Arguments

5. Applicant's arguments filed 11/27/2012 have been fully considered. Some of the arguments are now moot in view of new ground(s) rejection and the other arguments have been found non-convincing for reasons discussed below.

6. Applicant argues that Lee does not disclose the driving circuit being electrically connected to the power source line between the first and second protection circuits. The Examiner respectfully disagrees because

a. the driving circuit must connect to the power source to supply to internal circuit elements otherwise the driving circuit does not operate. Such connection can be found in Applicant Admitted Prior Art (fig. 11).

b. As shown in the below figure the driving circuit (70) is in between the first and second protection circuits

7. As to argument to claims 18, 23 and 24, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1, 3, 5 and 6 are rejected under 35 U.S.C. 102(a or b) as being anticipated by Applicant Admitted Prior Art (AAPA).

10. **Regarding claim 1**, AAPA discloses a semiconductor device, the apparatus (fig. 11) comprising: a scanning line driving circuit (801); a power supply line (750 and 751) electrically connected to the scanning line driving circuit; an input terminal (651) electrically connected to the power supply line to supply power; and a first protection circuit (ESD2) and a second protection circuit (ESD1) that are electrically connected to the power supply line to protect the scanning line driving circuit; the first protection circuit being electrically connected to the power line between (i) a first connecting portion (right side of the scanning line driving circuit) at which the scanning line driving circuit and the power supply line are electrically connected and (ii) the input terminal (651); and the scanning line driving circuit being electrically connected to the power supply line between (iii) a second connecting portion (right side of the scanning line driving circuit) at which the first protection circuit and the power supply line are electrically connected and (iv) a third connecting portion (left side of the scanning line

driving circuit) at which the second protection circuit and the power supply line are electrically connected.

11. **Regarding claim 3**, AAPA discloses the power supply line being low and high potential power sources supplying a power source potential to the scanning line driving circuit (see para. [0007]).

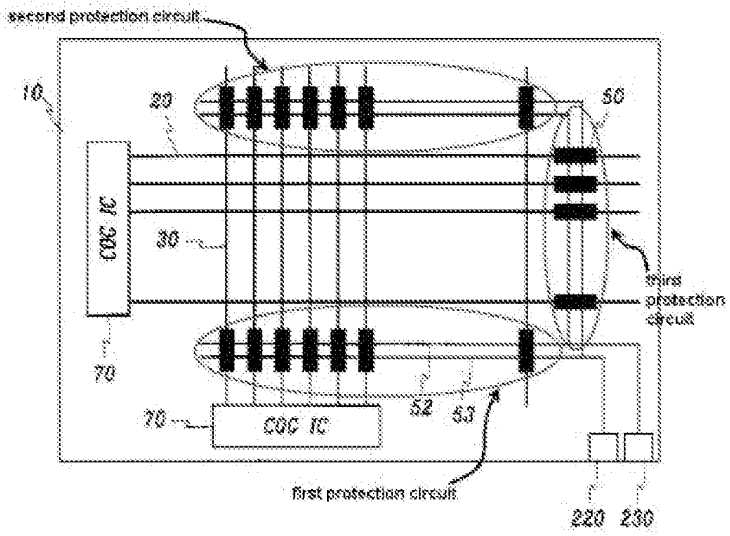
12. **Regarding claim 5**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate; the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate; the first protection circuit being arranged in the first corner portion of the substrate; and the second protection circuit being arranged in the second corner portion of the substrate (see fig. 11).

13. **Regarding claim 6**, AAPA discloses the semiconductor device being display device.

14. Claims 17-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,936,687, “Lee”).

15. **Regarding claim 17**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; a power source line (52, 53 and other power lines that are not shown in the figure to supply power to the driving

circuit) that supplies a power source to the driving circuit; and first and second protection circuits that are electrically connected to the power source line; the driving circuit being electrically connected to the power source line between the first and second protection circuits.



16. **Regarding claim 18**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; a power source line (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit; and first and second protection circuits that are electrically connected to the power source line; a first connecting point at which the first protection circuit is electrically connected to the power

source line; a second connecting point at which the second protection circuit is electrically connected to the power source line; and a third connecting point at which the driving circuit is electrically connected to the power source line; the third connecting point being positioned between the first and second connecting points.

17. **Regarding claims 19, 20, 25 and 26**, Lee discloses a region in which a plurality of the pixels arranged; the driving circuit being positioned outside of the region (see figure 5).

18. **Regarding claim 21**, Lee discloses an input terminal (220 and 230) electrically connected to the power source line; the first connecting point positioned between the input terminal and the third connecting point.

19. **Regarding claim 22**, Lee discloses the apparatus is a display device (title).

20. **Regarding claim 23**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; first and second power source lines (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit, a potential of the second power source line (220) being lower than that of the first power source line (230); first and second protection circuits (lower and upper) that are electrically connected to the first power source line; and third and fourth protection circuits (two upper and two lower further to the right in figure 5 that corresponds to the

third and fourth protection circuits that are electrically connected to the second power source line; the driving circuit being electrically connected to the first power source line between the first and second protection circuits, and being electrically connected to the second power source line between the third and fourth protection circuits (see fig. 5).

21. **Regarding claim 24**, Lee discloses a liquid crystal display having an electrostatic discharge (ESD) protection, the apparatus (figs. 5, 6 and also see reproduced figure above) comprising: a scanning line (20); a data line (30); a pixel arranged corresponding to an intersection of the scanning line and the data line; a driving circuit (70) that outputs a driving signal to the pixel; first and second power source lines (52, 53 and other power lines that are not shown in the figure to supply power to the driving circuit) that supplies a power source to the driving circuit, a potential of the second power source line (220) being lower than that of the first power source line (230); first and second protection circuits (lower and upper) that are electrically connected to the first power source line; third and fourth protection circuits (two upper and two lower further to the right in figure 5 that corresponds to the third and fourth protection circuits) that are electrically connected to the second power source line; a first connecting point at which the first protection circuit is electrically connected to the first power source line; a second connecting point at which the second protection circuit is electrically connected to the first power source line; a third connecting point at which the third protection circuit is electrically connected to the second power source line; a fourth connecting point at which the fourth protection circuit is electrically connected to the second power source line; a fifth connecting point at which the driving

circuit is electrically connected to the first power source line; and a six connecting point at which the driving circuit is electrically connected to the second power source line; the fifth connecting point being positioned between the first and second connecting points, and the sixth connecting point being positioned between the third and fourth connecting points (see fig. 5).

22. **Regarding claim 27**, Lee discloses a first input terminal (230) electrically connected to the first power source line; and a second input terminal (220) electrically connected to the second power source line; the first connecting point being positioned between the first input terminal and the fifth connecting point, and the third connecting point being positioned between the second input terminal and the six connecting point.

23. **Regarding claim 28**, Lee discloses the apparatus is a display device (title).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kitagawa (US 2004/0141269, "Kitagawa").

AAPA discloses a plurality of scanning line driving circuit (801-1 - 801-480) being electrically connected to the power supply line.

AAPA does not explicitly disclose a third protection circuit connected between at least one set of connection portion of two consecutive scanning line driving circuits. Kitagawa discloses a protection circuit (29 together with ESD protection circuits 311-315 and diodes 32, 34 and 35) being connected to power supply line (VDD1-VDD3 and GND1-GND3) to protect plurality of protected circuits (23-25), the protection circuit being connected to the power supply line between at least one set of connecting portions of two consecutive protected circuits and the power supply line. Kitagawa illustrates that the ESD surge voltage can occur in any line, i.e., I/O signal, high voltage supply line, or low voltage supply line. Kitagawa solution would bring the circuit of AAPA robust since the ESD surge voltage can occurs in any line and all the scanning line driving circuits should be protected against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Kitagawa because the ESD surge voltage can occurs in any line and all the scanning line driving circuits should be protected against ESD pulses.

26. Claims 7, 12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee.

27. **Regarding claim 7**, AAPA discloses semiconductor device, the apparatus (fig. 11) comprising: a first power supply line (751) electrically connected to a first terminal portion (651) to which a first power is supplied; a second power supply line (750) electrically connected to a second terminal portion (650) to which a second power is

supplied; a scanning line driving circuit (801-1 – 801-480) electrically connected to the first power supply line and the second power supply line; a first protection circuit (ESD2) being electrically connected to the first power supply line to protect the scanning line driving circuit, the first protection circuit being electrically connected to the first power supply line between (i) a first connecting portion at which the scanning line driving circuit and the first power supply line are electrically connected and (ii) the first terminal portion; and a second protection circuit (ESD1) being electrically connected to the second power supply line to protect the scanning line driving circuit, the second protection circuit being electrically connected to the second power supply line between (iii) a second connecting portion at which the scanning line driving circuit and the second power supply line are electrically connected and (iv) the second terminal portion.

AAPA does not explicitly disclose a buffer circuit. Lee discloses a buffer circuit connected to data signal to boost the signal (see fig. 11), the buffer circuit inherently electrically connected to a first power supply line to fulfill its function, as evidenced by Hatzilambrou et al. (US 6,801,416). Hatzilambrou discloses a semiconductor structure level of an inverter circuit (510 and 520) including output/input terminals and connected to a high potential line (Vdd), a low potential line (Vss), wherein the inverter circuit outputs high when it receives logic low and via versa (also see http://en.wikipedia.org/wiki/Inverter_(logic_gate)).

As to the buffer circuit connected between a first connecting portion at which the scanning line driving circuit and the first power supply line are electrically connected and

the first terminal portion, this is viewed to be chosen a location for electrical connection which is dependent upon convenient location and/or design requirements. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to connect the buffer circuit, as described above, because choosing a location for such connection is dependent upon convenient location and/or design requirements.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to connect the buffer circuit in order to boost the signal.

28. **Regarding claim 12**, AAPA discloses the first power supply line comprising a high potential power source wiring line supplying a power source potential to the scanning line driving circuit; and the second power supply line comprising a low potential power source wiring line supplying a power source potential to the scanning line driving circuit.

29. **Regarding claim 14**, AAPA discloses a substrate on which the scanning line driving circuit is arranged; the power supply lines being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate; the first protection circuit being arranged in the first corner portion of the substrate; and the second protection circuit being arranged in the second corner portion of the substrate.

30. **Regarding claim 15**, AAPA discloses the semiconductor device being a display device.

31. **Regarding claim 16**, AAPA discloses the semiconductor device being an electronic device.

32. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee and further in view of Kitagawa.

AAPA discloses a plurality of scanning line driving circuits (801-1 - 801-480) being electrically connected to the power supply line.

AAPA does not explicitly disclose a third protection circuit connected between at least one set of connection portion of two consecutive scanning line driving circuits. Kitagawa discloses a protection circuit (29 together with ESD protection circuits 311-315 and diodes 32, 34 and 35) being connected to power supply line (VDD1-VDD3 and GND1-GND3) to protect plurality of protected circuits (23-25), the protection circuit being connected to the power supply line between at least one set of connecting portions of two consecutive protected circuits and the power supply line. Kitagawa illustrates that the ESD surge voltage can occur in any line, i.e., I/O signal, high voltage supply line, or low voltage supply line. Kitagawa solution would bring the circuit of AAPA robust since the ESD surge voltage can occurs in any line and all the scanning line driving circuits should be protected against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Kitagawa because the ESD surge voltage can occurs in any line and all the scanning line driving circuits should be protected against ESD pulses.

33. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee, and further in view of Cooperman et al. (US 5,329,185, “Cooperman”).

Lee discloses in figure 11 that the buffer circuit including a first NOT circuit to which the first power is input (power supply as discussed in claim 7) and a second NOT circuit electrically connected to the first NOT circuit in series. Lee does not explicitly disclose each of the first and second NOT circuits consisting of complementary type transistor; and a channel width of the transistor of the second NOT circuit being larger than a channel width of the transistor of the first NOT circuit. Cooperman discloses each of first and second NOT circuits consisting of a complementary type transistor (see fig. 1); and channel width of transistor of the first transistor being larger than a channel width of the transistor of the second NOT circuit. Cooperman discloses that increasing the width of the channel transistor of the buffer will increase operating speed (abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of AAPA in view of Lee and utilize speed control by increasing a channel width of the transistor, as taught by Cooperman, in order to increase speed operation (abstract).

Allowable Subject Matter

34. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. Regarding claim 9, the prior art of record does not fairly suggest the combination of features set forth in the Applicant's claims. The references do not appear to suggest

the feature fourth and fifth protection circuits, and the buffer circuit, in combination with the other features of Applicant's independent claim.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can

be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tien Mai/
Examiner, Art Unit 2836
01/22/2013

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2836

Notice of References Cited	Application/Control No. 12/436,335	Applicant(s)/Patent Under Reexamination KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0141269	07-2004	Kitagawa, Nobutaka	361/056
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:37
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB;	OR	ON	2007/02/13 10:39

			USPAT			
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42
S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18
S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00
S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02

S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2008/04/14 12:39

			IBM_TDB			
S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52
S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB;	OR	ON	2009/02/05 09:28

			USPAT			
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54
S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 13:03
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04

S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19
S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over$1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50
S102	5	"11113120"	US-	OR	ON	2009/11/03

			PGPUB; USPAT; EPO; JPO; IBM_TDB			11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 11:23
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39
S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2009/11/03 12:40

			IBM_TDB			
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:47
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40
S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45
S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2010/02/26 14:46

			IBM_TDB			
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15
S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40
S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO;	OR	ON	2010/09/15 15:23

			IBM_TDB			
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S159	2	"20040141269"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/20 18:36
S160	36	"5936687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 13:10
S161	5	("5936687" | "5953191" | "5973901" | "6649944" | "6753836").PN. OR ("6985340").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 13:14
S165	13	"6801416"	US-	OR	OFF	2011/01/24

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO			17:50
S166	2	inverter with via near versa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:02
S167	31856	inverter with high with low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S168	2484	inverter near2 high near2 low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S169	13	inverter near2 high near2 low near input near signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:33
S170	3	11/101450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:47
S171	3997	protect$3 near (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S172	168	protect$3 near (buffer inverter) and esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S173	14	("20030107424" | "20030214768" | "20050093069" | "4264941" | "4384287" | "4466120" | "5287241" | "5691557" | "6507469" | "6583972" | "6590264" | "6643109" | "6671146" | "7064942").PN. OR ("7663851").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 19:50
S174	3	11/101450	US-PGPUB; USPAT	OR	ON	2013/01/15 10:07
S175	56	esd and plurality near internal near circuit	US-PGPUB; USPAT; USOCR;	OR	ON	2013/01/17 21:57

			EPO; JPO; IBM_TDB			
S176	7	("5679971" | "6014298" | "6624992" | "6762086" | "7692907" | "7827512" | "7869174").PN. OR ("8339757").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/17 21:57

1/28/2013 2:35:01 PM
C:\Users\tmai4\Documents\EAST\Workspaces\12436335.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM
see updated East search	01/22/2013	TM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

MAY 16 2013 IAP20 PATENT & TRADEMARK OFFICE

RCE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant(s) hereby request(s) continued examination (2nd or subsequent request).

☒ Applicant(s) further request(s) entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 252467 in the amount of $1,700.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

05/17/2013 EEKUBAY1 00000022 12436335
01 FC:1820 1700.00 OP

Date: May 16, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
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OPAP
MAY 16 2013
PATENT & TRADEMARK OFFICE
IAP20

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI	Group Art Unit: 2836
Application No.: 12/436,335	Examiner: T. MAI
Filed: May 6, 2009	Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the February 20, 2013 Office Action, and upon entry of the attached Request for Continued Examination, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Amendments to the Drawings include an attached replacement sheet;

Remarks.

Amendments to the Drawings:

The attached replacement drawing sheet makes changes to Fig.11.

Attachment: Replacement Sheet

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line ~~electrically~~ connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line;

an input terminal ~~electrically~~ connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are ~~electrically~~ connected to the power supply line, ~~to protect the scanning line driving circuit;~~

the first protection circuit being ~~electrically~~ connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are ~~electrically~~ connected and (ii) the input terminal; and

the scanning line driving circuit being ~~electrically~~ connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are ~~electrically~~ connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are ~~electrically~~ connected.

2. (Currently Amended) The display device as set forth in claim 1, further comprising:

a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving circuits being ~~electrically~~ connected to the power supply line; and

a third protection circuit ~~being electrically~~ connected to the power supply line ~~to protect the plurality of scanning line driving circuits, the third protection circuit being connected to the power supply line~~ between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. ~~at least one set of connecting portions of two consecutive scanning line driving circuits of the plurality of scanning line driving circuits and the power supply line.~~

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The display device as set forth in claim 1, further comprising:

a ~~substrate;~~substrate,

the scanning line driving circuit being arranged on the ~~substrate;~~ substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the ~~substrate;~~ substrate,

the first protection circuit being arranged in the first corner portion of the ~~substrate;~~ substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7-28. (Canceled)

REMARKS

Claims 1, 2, 5 and 6 are pending in this application. By this Amendment, claims 1, 2 and 5 are amended, Fig. 11 is amended, and claims 3, 4, 7-12 and 14-28 are cancelled. No new matter is added. Reconsideration of the rejections is requested based on the amendments and the following remarks.

The Office Action indicates that Fig. 11 should be designated by a legend such as -- Prior Art-- because only that which is old is illustrated. Fig. 11 has been amended to add a -- Related Art-- label. Approval is requested.

I. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claim 9 under 35 U.S.C. §112, second paragraph. This rejection is moot since claim 9 is canceled. Withdrawal of the rejection is respectfully requested.

The Office Action rejects claims 1, 3, 5 and 6 under 35 U.S.C. §102 (a or b) over Applicants Admitted Prior Art Fig. 11 (AAPA), rejects claims 17-28 under 35 U.S.C. §102(b) over Lee (U.S. Pat. No. 5,936,687), rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Kitagawa (U.S. Pat. Appl. Publ. No. 2004/0141269), rejects claims 7, 12 and 14-16 under 35 U.S.C. §103(a) over AAPA in view of Lee, rejects claim 8 under 35 U.S.C. §103(a) over AAPA in view of Lee and Kitagawa, and rejects claim 11 under 35 U.S.C. §103(a) over AAPA in view of Lee and Cooperman et al. (U.S. Pat. No. 5,329,185). These rejections are respectfully traversed regarding claims 1, 2, 5 and 6. The rejections are moot regarding claims 3, 7, 8, 11, 12 and 14-28 which have been cancelled and are being pursued in a divisional application.

AAPA does not disclose a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high

potential power supply line, as recited in claim 1 of the application. Elements 750 and 751 of AAPA are not "a power supply line being one of a low potential power supply line and a high potential power supply line" but instead 751 is a high potential power supply line and 751 is a low potential power supply line as indicated in [0007] of the specification. Further, 750 and 751 are not connected to each other, because they are different potentials. If they did connect to each other, they would cause a short circuit and could destroy the scanning line driving circuit.

For the above reasons, claim 1, and all claims dependent therefrom, are not anticipated by AAPA. Furthermore, claim 2 would not have been obvious over AAPA in view of Kitagawa due to its dependence from claim 1, and because Kitagawa does not solve the above-noted deficiency of AAPA. Withdrawal of the rejection is respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/hs

Attachments:
Request for Continued Examination
Replacement Sheet

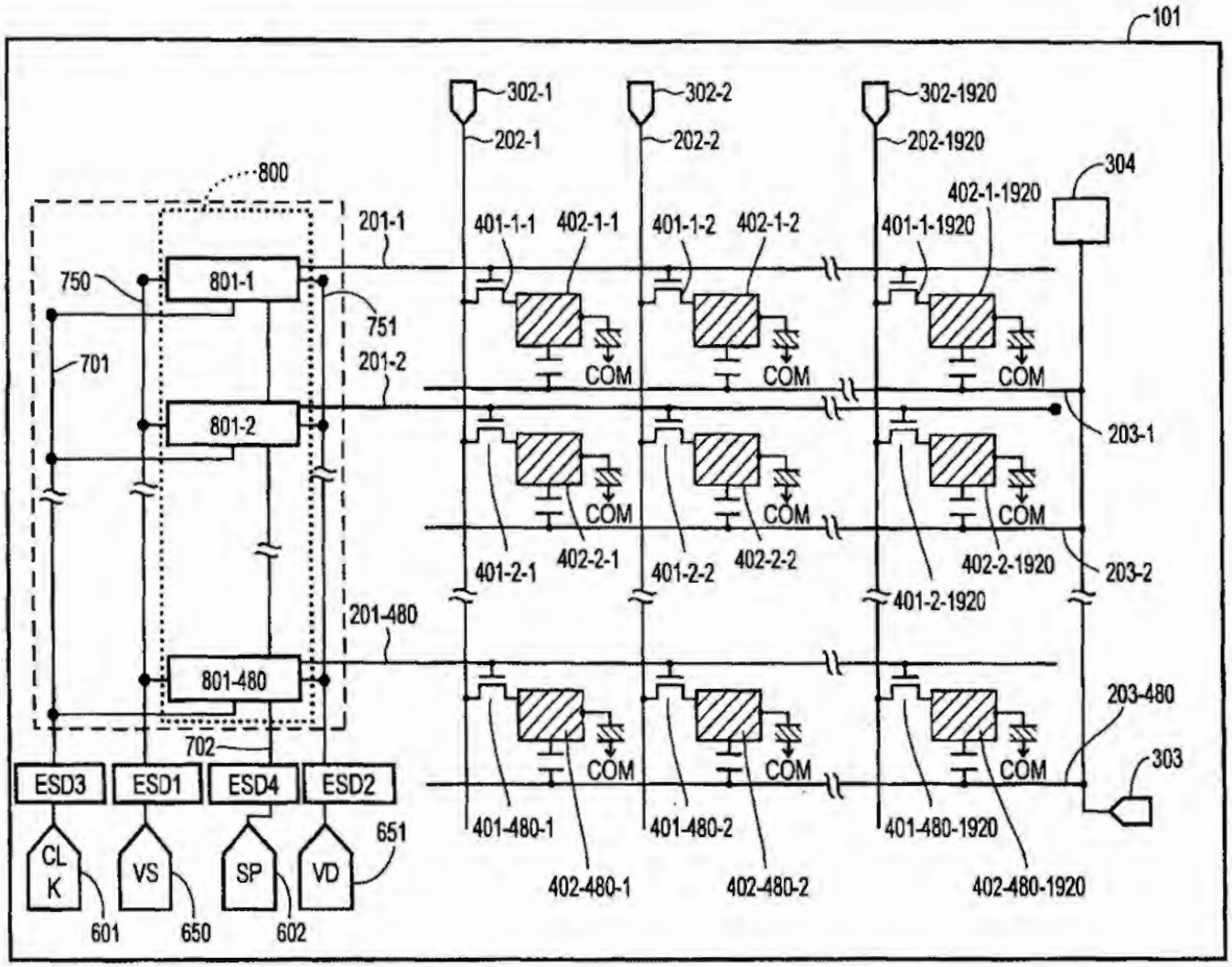
Date: May 16, 2013

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FIG. 11

Related Art



PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335	Filing Date 05/06/2009	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/16/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 4	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MONIQUE BRUNSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 06/20/2013
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
06/20/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,2,5 and 6* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5 and 6* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/16/2013 has been entered. Upon entering amendment, claims 1, 2 and 5 have been amended; claims 3, 4, 7-12 and 14-28 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 05/16/2013 have been fully considered but they are not persuasive for the reasons discussed below.

3. Applicant argues that AAPA does not disclose a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line. The Examiner respectfully disagrees because AAPA explicitly discloses the scanning line driving circuit connects to the power supply line such as lines 750 and 751. It is noted that the Applicant contradicted himself by stating that elements 750 and 751 of AAPA are not a power supply line being one of a low potential power supply line and a high potential power supply line but instead 751 is a high potential power supply line and 751 is a low potential power supply line.

4. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the low potential power supply line connects to the high potential power supply line) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. For the above reason, the rejections are maintained.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 5 and 6 are rejected under 35 U.S.C. 102(a or b) as being anticipated by Applicant Admitted Prior Art (AAPA).

8. **Regarding claim 1**, AAPA discloses a semiconductor device, the apparatus (fig. 11) comprising: a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential supply line (VS) and a high potential supply line (VD); an input terminal (651) connected to the power supply line to supply power; and a first protection circuit (ESD2)

and a second protection circuit (ESD1) that are connected to the power supply line, the first protection circuit being connected to the power supply line between (i) a first connecting portion (right side of the scanning line driving circuit) at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal; and the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion (right side of the scanning line driving circuit) at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion (left side of the scanning line driving circuit) at which the second protection circuit and the power supply line are connected.

9. **Regarding claim 5**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, the first protection circuit being arranged in the first corner portion of the substrate, and the second protection circuit being arranged in the second corner portion of the substrate (see fig. 11).

10. **Regarding claim 6**, AAPA discloses the semiconductor device being display device.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kitagawa (US 2004/0141269, "Kitagawa").

AAPA discloses a plurality of scanning line driving unit circuit (801-1 – 801-480) being included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line.

AAPA does not explicitly disclose a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. Kitagawa discloses a plurality of protection circuits (29 together with ESD protection circuits 311-315 and diodes 32, 34 and 35) being connected to power supply line (VDD1-VDD3 and GND1-GND3) to protect plurality of protected circuits (23-25), the protection circuit (311) connected between the first protected circuit (23) and the second protected circuit (25), the first protected circuit and the second protected circuit being adjacent to each other. Kitagawa illustrates that the ESD surge voltage can occur in any line, i.e., I/O signal, high voltage supply line, or low voltage supply line. Kitagawa solution would bring the circuit of AAPA robust since the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Kitagawa

because the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tien Mai/
Examiner, Art Unit 2836
06/12/2013

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2836

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 09/12/2013
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
09/12/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	12/436,335	KOBASHI, YUTAKA	
	Examiner	Art Unit	
	TIEN MAI	2836	

All participants (applicant, applicant's representative, PTO personnel):

(1) *TIEN MAI*. (3)_____.

(2) *David Zilbelli*. (4)_____.

Date of Interview: *27 August 2013*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Aplicant Admitted Prior Art, Kitagawa (US 2004/0141269)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

During a telephone interview no agreement was reached. Applicant would consider filing reconsideration after final.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

	/Rexford N BARNIE/ Supervisory Patent Examiner, Art Unit 2836

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

OPAP AKIMA-3
SEP 19 2013
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

PRE-APPEAL BRIEF REQUEST FOR REVIEW

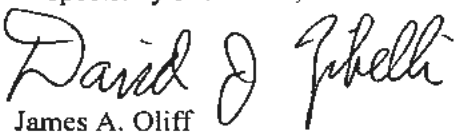
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This request is being filed with a Notice of Appeal. Review of the June 20, 2013 Final Rejection is requested for the reasons set forth in the attached five or fewer sheets.

Should any questions arise regarding this submission, or the Review Panel believe that anything further would be desirable in order to place this application in even better condition for allowance, the Review Panel is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/hs

Date: September 19, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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OPAP AKIMA-3 SEP 19 2013 PATENT & TRADEMARK OFFICE

REMARKS

Claims 1, 2, 5 and 6 are pending in this application. Reconsideration of the rejections is requested in accordance with the following remarks.

As discussed below, the AAPA does not disclose the following combination of features recited in claim 1: "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line; a first protection circuit and a second protection circuit that are connected to the power supply line." Therefore all of the rejections should be withdrawn.

The Pending Claims Define Patentable Subject Matter

The June 20, 2013 Final Rejection rejects claims 1, 5 and 6 under 35 U.S.C. §102(a or b) over Applicant's Admitted Prior Art Fig. 11 (AAPA), and rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Kitagawa (U.S. Pat. Appl. Publ. No. 2004/0141269). These rejections are respectfully traversed.

The AAPA Doesn't Disclose a First Protection Circuit and a Second Protection Circuit Connected to the Power Supply Line

Independent claim 1 of the application recites "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line" and "a first protection circuit and a second protection circuit that are connected to the power supply line." Thus, claim 1 requires that: 1) the power supply line is one of a low potential power supply line and a high potential power supply line (a low potential power supply line or a high potential power supply line); and 2) a first protection circuit and a second protection circuit that are connected to the power supply line (the power supply line being one of a low potential power supply line and a high potential power supply line).

The Final Rejection asserts that elements 750 and 751 of the AAPA are the power supply line, that element ESD2 of the AAPA is the first protection circuit, and that element ESD1 of the AAPA is the second protection circuit. These assertions are traversed for the reasons discussed below.

Element 750 of the AAPA is a low potential power supply line and element 751 is a high potential power supply line, as indicated in [0007] of the application. Thus, elements 750 and 751 of the AAPA are not "one of a low potential power supply line and a high potential power supply line" as recited in present claim 1. ESD1 and ESD2 are protection circuits that are connected to two different power supply lines, and are not two protection circuits that are connected to one of a low potential power supply line and a high potential power supply line.

During an August 27, 2013 telephone interview with Examiner Mai, Examiner Mai agreed with Applicant's representative that the recitation of "one of a low potential power supply line and a high potential power supply line" in claim 1 should be interpreted to require the power supply line to be a low potential power supply line or a high potential power supply line.

However, during the interview, Applicant's representative also asserted that the later recitation in claim 1 of "a first protection circuit and a second protection circuit that are connected to the power supply line" (emphasis added) required that the first and second protection circuits are connected to the power supply line, where the power supply line is "one of the a low potential power supply line and a high potential power supply line" as earlier recited in claim 1. Examiner Mai disagreed with this assertion at the interview and asserted that he was interpreting the recitation of "the power supply line" broadly to not require "the power supply line" to be the same power supply line as the earlier recited in

claim 1 "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line."

Examiner Mai thus took the position that the later in claim 1 recited "the power supply line" did not have to be "one of a low potential power supply line and a high potential power supply line" as earlier recited in claim 1. The Examiner asserted that therefore the recitation of "a first protection circuit and a second protection circuit that are connected to the power supply line" in claim 1 could read on the AAPA's low potential power supply line 750 connected to ESD2 and high potential power supply line 751 connected to ESD1, despite the fact that the low potential power supply line 750 and the high potential power supply line 751 are not "one of a low potential power supply line and a high potential power supply line." Applicant's representative strenuously disagreed with the Examiner's position during the interview.

It is respectfully asserted that the Examiner's position is legally erroneous, and that the Examiner is misconstruing the claim. Reasons for this position are further explained below.

The requirement of antecedent basis is a rule of patent claim drafting, administered during patent examination. As explained in Manual of Patent Examining Procedure (MPEP), a claim can be indefinite if it does not properly use the terms "a" or "an" when first introducing an element, and later in the claim or in a claim dependent therefrom, using the term "the" or "said" when referring to the same element, so that it is clear that the same element is being referenced. The MPEP uses as one example lack of clarity when a claim recites "said lever" or "the lever" and the claim contains no earlier recitation of "a lever" such that it would be unclear as to what element the limitation was making reference. See MPEP §2173.05(e).

The Examiner's position is disregarding the antecedent basis rule of claim construction and is therefore misconstruing the claim. In particular, claim 1 recites "a power

supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line" (emphasis added), and later recites "a first protection circuit and a second protection circuit that are connected to the power supply line" (emphasis added). The recitation of "the power supply line should be interpreted under antecedent basis rules to be the same power supply line as the earlier in claim 1 recited "a power supply line." Furthermore, because a power supply line is recited to be "one of a low potential power supply line and a high potential power supply line," the later recited "the power supply line" must also be interpreted to be "one of a low potential power supply line and a high potential power supply line."

When the claim is properly construed as discussed above, it is evident that the Examiner's interpretation of AAPA to read on claim 1 of the application is erroneous. In particular, claim 1 properly interpreted requires "a power supply line" to be one of a low potential power supply line and a high potential power supply line, and requires a first protection circuit and a second protection circuit be connected to "the power supply line" (being one of the a low potential power supply line and a high potential power supply line).

As can be seen in AAPA Fig. 11, the low potential power supply line 750 is connected to only one protection circuit ESD1. Likewise, the high potential power supply line 751 is only connected to one protection circuit ESD2. Thus neither the low potential power supply line 750 nor the high potential power supply line 751 are connected to first and second protection circuits as recited in claim 1 of the application.

In contrast, as may be seen with reference to Fig. 1 of the present application illustrating, *inter alia*, elements of the claimed invention, high potential power supply line 751 is connected to a first protection circuit ESD2 and is connected to a second protection circuit ESD12. Likewise, the low potential power supply line 750 is connected to a first protection circuit ESD1 and is connected to a second protection circuit ESD11.

As explained in the present specification, the AAPA of Fig. 1, by providing only one protection circuit connected to the high potential power supply line 751, and only one protection circuit connected to the low potential power supply line 750, insufficient ESD protection is provided to the TFTs constituting the scanning line unit driving circuits, as explained in [0012-13], for example.

In contrast, the present invention provides additional ESD protection by providing a first protection circuit ESD2 and a second protection circuit ESD12 connected to the high potential power supply line 751, and by providing a first protection circuit ESD1 and a second protection circuit ESD11 connected to the low potential power supply line 750, as illustrated in Fig. 1. As explained in [0039], for example, this structure provides additional ESD protection to the scanning line driving circuit 800 connected to the high potential power supply line 751 and connected to the low potential power supply line 750.

For at least the above reasons, claim 1, and dependent claims 5 and 6 are not anticipated by the AAPA. Dependent claim 2 would not have been obvious over the AAPA in view of Kitagawa because Kitagawa does not solve the above-noted deficiencies of claim 1, from which claim 2 depends. Therefore, the rejections should be withdrawn.

OPAP AKIMA-3
SEP 19 2013
PATENT & TRADEMARK OFFICE

DFW/AF

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE HONORABLE PATENT TRIAL AND APPEAL BOARD

In re the Application of

Yutaka KOBASHI

On Appeal from Group:2836

Application No.:12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached is the Brief on Appeal in the above-identified application.

Also attached is Check No. 254791, in the amount of $800.00 ($400.00 Small Entity), in payment of the fee due under 37 C.F.R. 41.20(b)(2).

In the event of any underpayment or overpayment, please debit or credit Deposit Account No. 15-0461 as needed in order to effect proper filing of this Brief.

Respectfully submitted,

David J. Zibelli

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: September 19, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
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27049 e 2013-10-09

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ALEXANDRIA, VA 22320-4850

Paper No.

Application No.:	**12/436,335**	**Date Mailed:**	**2013-10-09**
First Named Inventor:	Kobashi, Yutaka,	Examiner:	MAI, TIEN HUNG
Attorney Docket No.:	122872.01	Art Unit:	2836
Confirmation No.:	5191	Filing Date:	2009-05-06

Please find attached an Office communication concerning this application or proceeding.

Commissioner for Patents

PTO-90c (Rev.08-06)

Communication Re: Appeal	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA
	Examiner MAI, TIEN	Art Unit 2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The Notice of Appeal filed on *19 September, 2013* is not acceptable because:

   (a) ☒ it was not timely filed.

   (b) ☒ the statutory fee for filing the appeal was not submitted. See 37 CFR 41.20(b)(1).

   (c) ☐ the appeal fee received on _____ was not timely filed.

   (d) ☐ the submitted fee of $_____ is insufficient. The appeal fee required by 37 CFR 41.20(b)(1) is $_____.

   (e) ☐ the appeal is not in compliance with 37 CFR 41.31(a)(1) in that no claim has been twice rejected.

   (f) ☐ a Notice of Allowability, PTO-37, was mailed by the Office on _____.

2. ☐ The appeal brief filed on _____ is NOT acceptable for the reason(s) indicated below:

   (a) ☐ the brief and/or brief fee is untimely. See 37 CFR 41.37(a).

   (b) ☐ the statutory fee for filing the brief has not been submitted. See 37 CFR 41.20(b)(2).

   (c) ☐ the submitted brief fee of $_____ is insufficient. The brief fee required by 37 CFR 41.20(b)(2) is $_____.

The appeal in this application will be dismissed unless corrective action is taken to timely submit the brief and requisite fee. See 37 CFR 41.37(a)(1). Extensions of time may be obtained under 37 CFR 1.136(a). See 37 CFR 41.37(e).

3. ☐ The appeal in this application is DISMISSED because:

   (a) ☐ the statutory fee for filing the brief as required under 37 CFR 41.20(b)(2) was not timely submitted and the period for obtaining an extension of time to file the brief under 37 CFR 1.136(a) has expired.

   (b) ☐ the brief was not timely filed and the period for obtaining an extension of time to file the brief under 37 CFR 1.136(a) has expired.

   (c) ☐ a Request for Continued Examination (RCE) under 37 CFR 1.114 was filed on _____.

   (d) ☐ other: _____.

4. ☐ Because of the dismissal of the appeal, this application:

   (a) ☐ is abandoned because there are no allowed claims.

   (b) ☐ is before the examiner for final disposition because it contains allowed claims. Prosecution on the merits remains CLOSED.

   (c) ☐ is before the examiner for consideration.

/EVERETT WILLIAMS/

OPAP AKIMA-3
OCT 09 2013
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

PRE-APPEAL BRIEF REQUEST FOR REVIEW

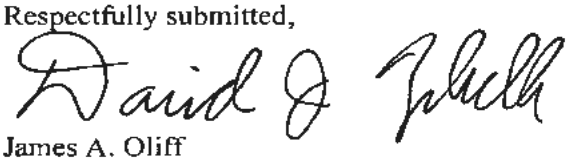
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This request is being filed with a Notice of Appeal. Review of the June 20, 2013 Final Rejection is requested for the reasons set forth in the attached five or fewer sheets.

Should any questions arise regarding this submission, or the Review Panel believe that anything further would be desirable in order to place this application in even better condition for allowance, the Review Panel is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/hs

Date: October 9, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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REMARKS

Claims 1, 2, 5 and 6 are pending in this application. Reconsideration of the rejections is requested in accordance with the following remarks.

As discussed below, the AAPA does not disclose the following combination of features recited in claim 1: "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line; a first protection circuit and a second protection circuit that are connected to the power supply line." Therefore all of the rejections should be withdrawn.

The Pending Claims Define Patentable Subject Matter

The June 20, 2013 Final Rejection rejects claims 1, 5 and 6 under 35 U.S.C. §102(a or b) over Applicant's Admitted Prior Art Fig. 11 (AAPA), and rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Kitagawa (U.S. Pat. Appl. Publ. No. 2004/0141269). These rejections are respectfully traversed.

The AAPA Doesn't Disclose a First Protection Circuit and a Second Protection Circuit Connected to the Power Supply Line

Independent claim 1 of the application recites "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line" and "a first protection circuit and a second protection circuit that are connected to the power supply line." Thus, claim 1 requires that: 1) the power supply line is one of a low potential power supply line and a high potential power supply line (a low potential power supply line or a high potential power supply line); and 2) a first protection circuit and a second protection circuit that are connected to the power supply line (the power supply line being one of a low potential power supply line and a high potential power supply line).

The Final Rejection asserts that elements 750 and 751 of the AAPA are the power supply line, that element ESD2 of the AAPA is the first protection circuit, and that element ESD1 of the AAPA is the second protection circuit. These assertions are traversed for the reasons discussed below.

Element 750 of the AAPA is a low potential power supply line and element 751 is a high potential power supply line, as indicated in [0007] of the application. Thus, elements 750 and 751 of the AAPA are not "one of a low potential power supply line and a high potential power supply line" as recited in present claim 1. ESD1 and ESD2 are protection circuits that are connected to two different power supply lines, and are not two protection circuits that are connected to one of a low potential power supply line and a high potential power supply line.

During an August 27, 2013 telephone interview with Examiner Mai, Examiner Mai agreed with Applicant's representative that the recitation of "one of a low potential power supply line and a high potential power supply line" in claim 1 should be interpreted to require the power supply line to be a low potential power supply line or a high potential power supply line.

However, during the interview, Applicant's representative also asserted that the later recitation in claim 1 of "a first protection circuit and a second protection circuit that are connected to the power supply line" (emphasis added) required that the first and second protection circuits are connected to the power supply line, where the power supply line is "one of the a low potential power supply line and a high potential power supply line" as earlier recited in claim 1. Examiner Mai disagreed with this assertion at the interview and asserted that he was interpreting the recitation of "the power supply line" broadly to not require "the power supply line" to be the same power supply line as the earlier recited in

claim 1 "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line."

Examiner Mai thus took the position that the later in claim 1 recited "the power supply line" did not have to be "one of a low potential power supply line and a high potential power supply line" as earlier recited in claim 1. The Examiner asserted that therefore the recitation of "a first protection circuit and a second protection circuit that are connected to the power supply line" in claim 1 could read on the AAPA's low potential power supply line 750 connected to ESD2 and high potential power supply line 751 connected to ESD1, despite the fact that the low potential power supply line 750 and the high potential power supply line 751 are not "one of a low potential power supply line and a high potential power supply line." Applicant's representative strenuously disagreed with the Examiner's position during the interview.

It is respectfully asserted that the Examiner's position is legally erroneous, and that the Examiner is misconstruing the claim. Reasons for this position are further explained below.

The requirement of antecedent basis is a rule of patent claim drafting, administered during patent examination. As explained in Manual of Patent Examining Procedure (MPEP), a claim can be indefinite if it does not properly use the terms "a" or "an" when first introducing an element, and later in the claim or in a claim dependent therefrom, using the term "the" or "said" when referring to the same element, so that it is clear that the same element is being referenced. The MPEP uses as one example lack of clarity when a claim recites "said lever" or "the lever" and the claim contains no earlier recitation of "a lever" such that it would be unclear as to what element the limitation was making reference. See MPEP §2173.05(e).

The Examiner's position is disregarding the antecedent basis rule of claim construction and is therefore misconstruing the claim. In particular, claim 1 recites "a power

supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line and a high potential power supply line" (emphasis added), and later recites "a first protection circuit and a second protection circuit that are connected to the power supply line" (emphasis added). The recitation of "the power supply line should be interpreted under antecedent basis rules to be the same power supply line as the earlier in claim 1 recited "a power supply line." Furthermore, because a power supply line is recited to be "one of a low potential power supply line and a high potential power supply line," the later recited "the power supply line" must also be interpreted to be "one of a low potential power supply line and a high potential power supply line."

When the claim is properly construed as discussed above, it is evident that the Examiner's interpretation of AAPA to read on claim 1 of the application is erroneous. In particular, claim 1 properly interpreted requires "a power supply line" to be one of a low potential power supply line and a high potential power supply line, and requires a first protection circuit and a second protection circuit be connected to "the power supply line" (being one of the a low potential power supply line and a high potential power supply line).

As can be seen in AAPA Fig. 11, the low potential power supply line 750 is connected to only one protection circuit ESD1. Likewise, the high potential power supply line 751 is only connected to one protection circuit ESD2. Thus neither the low potential power supply line 750 nor the high potential power supply line 751 are connected to first and second protection circuits as recited in claim 1 of the application.

In contrast, as may be seen with reference to Fig. 1 of the present application illustrating, *inter alia*, elements of the claimed invention, high potential power supply line 751 is connected to a first protection circuit ESD2 and is connected to a second protection circuit ESD12. Likewise, the low potential power supply line 750 is connected to a first protection circuit ESD1 and is connected to a second protection circuit ESD11.

As explained in the present specification, the AAPA of Fig. 1, by providing only one protection circuit connected to the high potential power supply line 751, and only one protection circuit connected to the low potential power supply line 750, insufficient ESD protection is provided to the TFTs constituting the scanning line unit driving circuits, as explained in [0012-13], for example.

In contrast, the present invention provides additional ESD protection by providing a first protection circuit ESD2 and a second protection circuit ESD12 connected to the high potential power supply line 751, and by providing a first protection circuit ESD1 and a second protection circuit ESD11 connected to the low potential power supply line 750, as illustrated in Fig. 1. As explained in [0039], for example, this structure provides additional ESD protection to the scanning line driving circuit 800 connected to the high potential power supply line 751 and connected to the low potential power supply line 750.

For at least the above reasons, claim 1, and dependent claims 5 and 6 are not anticipated by the AAPA. Dependent claim 2 would not have been obvious over the AAPA in view of Kitagawa because Kitagawa does not solve the above-noted deficiencies of claim 1, from which claim 2 depends. Therefore, the rejections should be withdrawn.

OPAP AKIMA3 OCT 09 2013 PATENT & TRADEMARK OFFICE

IFW/AF $

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

NOTICE OF APPEAL TO THE PATENT TRIAL AND APPEAL BOARD AND PETITION FOR EXTENSION OF TIME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant(s) hereby appeal(s) to the Patent Trial And Appeal Board from the Decision of the Primary Examiner dated June 20, 2013.

The $800.00 Appeal Fee ($400.00 Small Entity) is:

☒ Enclosed (Check No. 255194)

☐ Not required (fee paid in prior appeal in this application with no Board Decision on the merits).

The shortened statutory period having expired September 20, 2013, an extension of one month(s) is hereby requested. Included is check no. 255195 in the amount of $200 in payment of the fee for a one month extension of time for filing this Notice of Appeal.

In the event of any underpayment or overpayment, please debit or credit Deposit Account No. 15-0461 as needed in order to effect proper filing of this Notice of Appeal.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: October 9, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
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Telephone: (703) 836-6400

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10/10/2013 LNGUYEN1 00000009 12436335

01 FC:1401 800.00 OP
02 FC:1251 200.00 OP

UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 11/19/2013

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
11/19/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA
	Examiner TIEN MAI	Art Unit 2836

This is in response to the Pre-Appeal Brief Request for Review filed 09 October, 2013.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: *1,2,5 and 6*.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *TIEN MAI*.	(3) *DAVID MARTIN*.
(2) *REXFORD BARNIE*.	(4)_____.

/Tien Mai/ Examiner, Art Unit 2836	/David S. Martin/ Examiner, OPQA	/Rexford N BARNIE/ Supervisory Patent Examiner, Art Unit 2836

OPAP AKIMA-3 DEC 19 2013 PATENT & TRADEMARK OFFICE

IFW/RCE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the provisions of 37 C.F.R. §1.114, Applicant(s) hereby request(s) continued examination (2nd or subsequent request).

☒ Applicant(s) further request(s) entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 256624 in the amount of $1,700.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: December 19, 2013

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Telephone: (703) 836-6400

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12/20/2013 LNGUYEN1 00000046 12436335
01 FC:1820 1700.00 OP

OPAP
DEC 19 2013
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI		Group Art Unit:	2836
Application No.:	12/436,335	Examiner:	T. MAI
Filed:	May 6, 2009	Docket No.:	122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In reply to the July 6, 2013 Office Action, the due date being set by the September 19, 2013 Notice of Appeal and extended by the November 19, 2013 Notice of Panel Decision, and upon entry of the attached Request for Continued Examination, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line ~~and~~ or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

2. (Currently Amended) The display device as set forth in claim 1, further comprising:

a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and

a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a

second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The display device as set forth in claim 1, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7-28. (Canceled)

29. (New) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

30. (New) The display device as set forth in claim 29, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit.

31. (New) The display device as set forth in claim 29, further comprising:

a buffer circuit included in the scanning line driving circuit.

32. (New) The display device as set forth in claim 29, further comprising:

a transistor included in the scanning line driving circuit.

33. (New) The display device as set forth in claim 29, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

34. (New) An electronic device provided with the display device as set forth in claim 29.

35. (New) A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the circuit element,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

36. (New) The display device as set forth in claim 35, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.

37. (New) The display device as set forth in claim 35, further comprising:

a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.

38. (New) The display device as set forth in claim 35, further comprising:

a transistor included in the scanning line driving circuit, the transistor being the circuit element.

39. (New) The display device as set forth in claim 35, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

40. (New) An electronic device provided with the display device as set forth in claim 13.

REMARKS

Claims and 1, 2, 5, 6 and 29-40 are pending in this application. By this Amendment, and claims 1 and 2 are amended and claims 29-40 are added. No new matter is added. Reconsideration of the rejections is requested based on the amendments and the following remarks.

I. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 5 and 6 under 35 U.S.C. §102(a or b) over Applicant Admitted Prior Art (AAPA) and rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Kitagawa (U.S. Pat. Appl. No. 2004/014269). These rejections are respectfully traversed.

AAPA does not disclose a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line, a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line, as recited in claim 1. Instead, AAPA only discloses one protection circuit connected to the low potential power supply line or the high potential power supply line. Accordingly, claim 1 and dependent claims 5 and 6 are not anticipated by AAPA. Claim 2 would not have been obvious due to its dependence from claim 1, and because Kitagawa does not solve the above-noted deficiencies of Kitagawa.

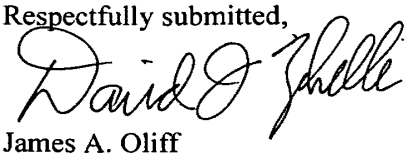
It is also believed that the new claims distinguish over the applied references.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/djz

Attachment:
Request for Continued Examination

Date: December 19, 2013

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PTO/SB/06 (09-11)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335	Filing Date 05/06/2009	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 12/19/2013

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MONIQUE BRUNSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

OPAP AKIMA-6
JAN 1 5 2014
PATENT & TRADEMARK OFFICE

IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits after the filing of a Request for Continued Examination under 37 CFR §1.114. No certification or fee is required.

☒ 2. An Office Action was issued in U.S. Application No. 13/905,924. A copy of the Office Action is submitted for the Examiner's consideration as Reference 1. The references cited therein have already been made of record in this application.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb
Date: January 15, 2014

OLIFF PLC
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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

Modified Form PTO-1449 (REV. 07/09) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 122872.01	APPLICATION NO. 12/436,335
	FIRST NAMED INVENTOR Yutaka KOBASHI	
	FILING DATE May 6, 2009	GROUP 2836

OPAP JAN 15 2014 PATENT & TRADEMARK OFFICE AKIMA-6

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	1	Office Action dated January 6, 2014 issued in U.S. Patent Application No. 13/905,924.

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 15, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 05/12/2014

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ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
05/12/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/19/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,2,5,6 and 29-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5,6 and 29-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *01/15/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/19/2013 has been entered. Upon entering amendment, claims 1 and 2 have been amended; claims 29-40 have been added.

Response to Arguments

2. Applicant's arguments with respect to claim 1 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6, 29, 30, 33, 34, 36, 39 and 40 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Lee et al. (US 6,791,632, "Lee").

5. **Regarding claim 1 and 29**, AAPA discloses a semiconductor device, the apparatus (fig. 11) comprising: a circuit element included in a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line (750) or a high potential power supply line (751); an input terminal (651) connected to the power supply line to supply power; and a first protection circuit (ESD2) that is connected to the power supply line to protect the power supply line (the ESD protecting the power supply line is the same as protecting the scanning line driving circuit or the circuit element since the power supply line provides voltage to the scanning line driving circuit and the scanning line driving circuit would damage if surge propagates in the power supply line), the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the power supply line is connected.

AAPA does not explicitly disclose a second protection circuit that is connected to the power supply line. Lee discloses protection circuit and method from electrostatic discharge of TFT-LCD, the apparatus (fig. 3) comprising: a first protection circuit

(IESD1) and a second protection circuit (IESD2) connected to a power line to protect the power line (col. 1, lines 59-62). It is well known in the art that connecting protection circuits on both ends of the power line to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Lee in order to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. Furthermore, adding additional ESD protection circuit onto existing device is viewed to be duplication of part, which is dependent upon the operation condition and design requirement for particular application. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to add additional ESD protection circuit since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. In re Harza, 274, F.2d 669, 124 USPQ 378 (CCPA 1960).

The Examiner suggests connecting the second ESD protection circuit to the power supply line either between circuit elements, i.e., scanning line driving unit circuits (801-1— 801-480) or the last node of the power supply line.

6. **Regarding claim 5**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, the first protection circuit being arranged in the first corner portion of the

substrate, and the second protection circuit being arranged in the second corner portion of the substrate (see fig. 11).

7. **Regarding claims 6, 34 and 40**, AAPA discloses the semiconductor device being display device.

8. **Regarding claim 30**, AAPA discloses a scanning line driving unit circuit (801-1 – 801-480) included in the scanning line driving circuit (see fig. 11).

9. **Regarding claims 33 and 39**, AAPA discloses a substrate (see para. [00063]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, and the first protection circuit being arranged in the first corner portion of the substrate. AAPA in view of Lee does not explicitly disclose the location of the second protection circuit. However, choosing a location for the second protection circuit, such as the second corner portion of the substrate, is dependent upon design requirement and available of the location. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to place the second protection circuit at the second corner portion of the substrate since it dependent upon design requirement and availability of the location and such location does not change perspective function of the second protection circuit.

10. **Regarding claim 36**, AAPA discloses a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element (see fig. 11).

11. Claim 2 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee, and further in view of Kitagawa (US 2004/0141269, "Kitagawa").

AAPA discloses a plurality of scanning line driving unit circuit (801-1 – 801-480) being included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line.

AAPA does not explicitly disclose a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. Kitagawa discloses a plurality of protection circuits (29 together with ESD protection circuits 311-315 and diodes 32, 34 and 35) being connected to power supply line (VDD1-VDD3 and GND1-GND3) to protect plurality of protected circuits (23-25), the protection circuit (311) connected between the first protected circuit (23) and the second protected circuit (25), the first protected circuit and the second protected circuit being adjacent to each other. Kitagawa illustrates that the ESD surge voltage can occur in any line, i.e., I/O signal, high voltage supply line, or low voltage supply line. Kitagawa solution would bring the circuit of AAPA robust since the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Kitagawa

because the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses.

12. Claims 31, 32, 37 and 38 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee, and further in view of Yamazaki et al. (US 2004/0075094, "Yamazaki").

13. **Regarding claims 31, 32, 37 and 38**, AAPA and Lee disclose the limitations as discussed above. AAPA does not explicitly disclose the scanning line driving circuit included a buffer circuit or transistor. Yamazaki discloses semiconductor display device comprising a scanning line driving circuit including buffer circuits (120-122) which form of transistor (see para [0239] and also see figure 19). The scanning line driving circuit including buffer circuit or transistor is well known in the art since the buffer would amplify the input signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement buffer in the scanning line driving circuit in order to amplify the input signal. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use transistor in the scanning line driving circuit since transistor provides fast switching.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/TIEN MAI/
Examiner, Art Unit 2836
04/16/2014

Notice of References Cited	Application/Control No. 12/436,335	Applicant(s)/Patent Under Reexamination KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,791,632	09-2004	Lee et al.	349/40
*	B	US-2004/0075094	04-2004	Yamazaki et al.	257/072
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 01/15/2014
OPAP
JAN 1 5 2014
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI	Group Art Unit: 2836
Application No.: 12/436,335	Examiner: T. MAI
Filed: May 6, 2009	Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

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☒ 2. An Office Action was issued in U.S. Application No. 13/905,924. A copy of the Office Action is submitted for the Examiner's consideration as Reference 1. The references cited therein have already been made of record in this application.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb
Date: January 15, 2014

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.M./

Modified Form PTO-1449 (REV. 07/09) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 122872.01	APPLICATION NO. 12/436,335
	FIRST NAMED INVENTOR Yutaka KOBASHI	
	FILING DATE May 6, 2009	GROUP 2836

OPAP JAN 15 2014 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	1	Office Action dated January 6, 2014 issued in U.S. Patent Application No. 13/905,924.

EXAMINER /Tien Mai/	DATE CONSIDERED 04/16/2014

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 15, 2014 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.M./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM
see updated East search	01/22/2013	TM
see updated East search	4/16/2014	TM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:37
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB;	OR	ON	2007/02/13 10:39

			USPAT			
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42
S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18
S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00
S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02

S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2008/04/14 12:39

			IBM_TDB			
S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52
S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB;	OR	ON	2009/02/05 09:28

			USPAT			
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54
S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 13:03
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04

S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19
S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over$1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50
S102	5	"11113120"	US-	OR	ON	2009/11/03

			PGPUB; USPAT; EPO; JPO; IBM_TDB			11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 11:23
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39
S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2009/11/03 12:40

			IBM_TDB			
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:47
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40
S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45
S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2010/02/26 14:46

			IBM_TDB			
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15
S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40
S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO;	OR	ON	2010/09/15 15:23

			IBM_TDB			
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S159	2	"20040141269"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/20 18:36
S160	36	"5936687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 13:10
S161	5	("5936687" | "5953191" | "5973901" | "6649944" | "6753836").PN. OR ("6985340").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 13:14
S165	13	"6801416"	US-	OR	OFF	2011/01/24

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO			17:50
S166	2	inverter with via near versa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:02
S167	31856	inverter with high with low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S168	2484	inverter near2 high near2 low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S169	13	inverter near2 high near2 low near input near signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:33
S170	3	11/101450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:47
S171	3997	protect$3 near (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S172	168	protect$3 near (buffer inverter) and esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S173	14	("20030107424" | "20030214768" | "20050093069" | "4264941" | "4384287" | "4466120" | "5287241" | "5691557" | "6507469" | "6583972" | "6590264" | "6643109" | "6671146" | "7064942").PN. OR ("7663851").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 19:50
S174	3	11/101450	US-PGPUB; USPAT	OR	ON	2013/01/15 10:07
S175	56	esd and plurality near internal near circuit	US-PGPUB; USPAT; USOCR;	OR	ON	2013/01/17 21:57

			EPO; JPO; IBM_TDB			
S176	7	("5679971" | "6014298" | "6624992" | "6762086" | "7692907" | "7827512" | "7869174").PN. OR ("8339757").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/17 21:57
S177	0	(11/766788).APP.	USPAT; USOCR	OR	ON	2014/04/16 11:54
S179	9	("6791632" | "5696928" | "20020105512" | "20030020845" | "20060001787" | "20050190168" | "20060001787" | "5619222" | "20060279667" | "5734722" | "6791632").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 11:55
S180	1	(10/180979).APP.	USPAT; USOCR	OR	ON	2014/04/16 12:11
S181	26	("5068748" | "5596342" | "5909035" | "5936687" | "6043971" | "6088073").PN. OR ("6791632").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 12:17
S182	1	13/115749	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:11
S183	1	"8456791"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:14
S184	14	tien near mai.xa. and rf	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:19
S185	117	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060146458" | "20070053130" | "20070139850" | "20090103226" | "20090109584" | "20090284888" | "20110080683" | "20110141646" | "20110159727" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4841253" | "4864250" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5278720" | "5321573" |	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:22

		"5353189" | "5442330" | "5537044" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" | "6502599" | "6527004" | "6721155" | "6754060" | "6757152" | "6785110" | "6789560" | "6814100" | "6968852" | "6975496" | "7082022" | "7104282" | "7106572" | "7130103" | "7159236" | "7215221" | "7221550" | "7250829" | "7430103" | "7623332" | "7808752").PN. OR ("8456791").URPN.				
S186	31	("20030072121" | "20030179533" | "20050259376" | "20070025043" | "4409637" | "4554608" | "5053910" | "5122921" | "5278720" | "5896265" | "6061223" | "6451773" | "6452773" | "6492894" | "6606232" | "6636407" | "6721155" | "7035073" | "7094104" | "7170728").PN. OR ("7623332").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:23
S187	133	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040042149" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060120005" | "20060139832" | "20060146458" | "20070053130" | "20070095400" | "20070097583" | "20070139850" | "20090103226" | "20090109584" | "20090296430" | "20110141646" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4356360" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5170151" | "5278720" | "5321573" | "5353189" | "5412526" | "5442330" | "5537044" | "5611224" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5798790" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6226166" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" |	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:24

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S189	24	"3956717"	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:34
S190	9196	buffer with (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:21
S191	1674	buffer near2 (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:22
S192	1196	buffer near2 (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:23
S193	416	buffer near (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:24
S194	2958	buffer with (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S195	738	buffer near3 (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S196	243	buffer near2 (scan$4 near line gat$3) near (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:26
S197	1	(10/667518).APP.	USPAT; USOCR	OR	ON	2014/04/16 22:34
S198	2550	(advantage benefit) near transistor	US-PGPUB; USPAT; USOCR;	OR	ON	2014/04/16 23:16

			EPO; JPO; IBM_TDB			

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S138	8	capacit$4 near3 signal near line with capacit$4 near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:22
S139	1442	capacit$4 adj (protect$4 circuit) near3 signal near line with capacit$4 (protect$3 circuit) near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S140	2	capacit$4 near (protect$4 circuit) with signal near line same capacit$4 near (protect$3 circuit) with (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S141	0	capacit$4 near (first second) near protect$3 near circuit and capacit$4 near (third fourth) near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:30
S142	26	capacit$4 near protect$3 near circuit same (greater lower bigger larger) same capacit$4 near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:31

4/ 16/ 2014 11:46:15 PM
C:\ Users\ tmai4\ Documents\ EAST\ Workspaces\ 12436335.wsp



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI	Group Art Unit: 2836
Application No.: 12/436,335	Examiner: T. MAI
Filed: May 6, 2009	Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In reply to the May 12, 2014 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the ~~power supply line~~scanning line driving circuit to protect the ~~power supply line~~ scanning line driving circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

2. (Previously Presented) The display device as set forth in claim 1, further comprising:

a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and

a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The display device as set forth in claim 1, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7-28. (Canceled)

29. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the ~~power supply line~~ scanning line driving circuit to protect the scanning line driving circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

30. (Previously Presented) The display device as set forth in claim 29, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit.

31. (Previously Presented) The display device as set forth in claim 29, further comprising:

a buffer circuit included in the scanning line driving circuit.

32. (Previously Presented) The display device as set forth in claim 29, further comprising:

a transistor included in the scanning line driving circuit.

33. (Previously Presented) The display device as set forth in claim 29, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

34. (Previously Presented) An electronic device provided with the display device as set forth in claim 29.

35. (Currently Amended) A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the ~~power supply line~~ scanning line driving circuit to protect the circuit element,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

36. (Previously Presented) The display device as set forth in claim 35, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.

37. (Previously Presented) The display device as set forth in claim 35, further comprising:

a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.

38. (Previously Presented) The display device as set forth in claim 35, further comprising:

a transistor included in the scanning line driving circuit, the transistor being the circuit element.

39. (Previously Presented) The display device as set forth in claim 35, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

40. (Currently Amended) An electronic device provided with the display device as set forth in ~~claim 13~~claim 35.

41. (New) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

42. (New) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply

line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

43. (New) A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect a part of the circuit element,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

REMARKS

Claims 1, 2, 5, 6 and 29-43 are pending in this application. By this Amendment, claims 1, 29, 35 and 40 are amended and new claims 41-43 are added. No new matter is added. Reconsideration of the rejections is requested based on the amendments and the following remarks.

I. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 5, 6, 29, 30, 33, 34, 36, 39 and 40 under 35 U.S.C. §103(a) over AAPA in view of Lee et al. (U.S. Pat. No. 6,791,632), rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Lee and Kitagawa et al. (U.S. 2004/0142269), and rejects claims 31, 32, 37 and 38 under 35 U.S.C. §103(a) over AAPA in view of Lee and Yamazaki et al. (U.S. 2004/0075094). These rejections are respectfully traversed.

Regarding independent claims 1, 29 and 35, the Office Action asserts that Lee discloses first and second protection circuits connected to a power line to protect the power line. However, claims 1 and 29 recite "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit." Independent claim 35 likewise recites a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element." Lee and the other applied references do not disclose first and second protection circuits connected to the scanning line driving circuit to protect the scanning line driving circuit.

Furthermore, the addition of the second protection circuit is not just a mere duplication of parts as asserted in the Office Action. Instead, the second protection circuit, as disclosed in the specification, provides additional ESD protection not provided by just the first protection circuit.

For the above reasons, claims 1, 29 and 35, and all claims dependent therefrom, would not have been obvious over the applied references. Withdrawal of the rejections is respectfully requested.

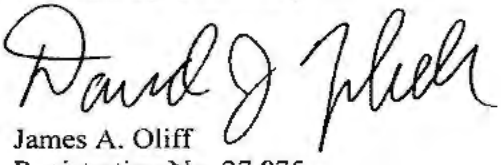
New independent claims 41-43 recite that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit. It is believed that these features are not disclosed in the applied references.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/djz

Date: August 12, 2014

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335	Filing Date 05/06/2009	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/12/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 6	Minus	***3	= 3	X $420 =	1260
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	1260

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ROCHELLE GETER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 09/10/2014

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ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	
ART UNIT	**PAPER NUMBER**
2836	

NOTIFICATION DATE	DELIVERY MODE
09/10/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/12/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,2,5,6 and 29-43* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5,6 and 29-43* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions. Applicant's response of 08/12/2014 has been entered and considered. Upon entering amendment, claims 1, 29, 35 and 40 have been amended; claims 41-43 have been added.

Double Patenting

2. Claims 29, 33 and 34 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 1, 5 and 6. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

3. Applicant's arguments filed 08/12/2014 have been fully considered but they are not persuasive for the reasons discussed below.

4. Applicant argues that the applied references do not disclose first and second protection circuits connected to the scanning line driving circuit to protect the scanning line driving circuit. The Examiner respectfully disagrees because AAPA explicitly discloses the protection circuit connected to the power supply line which provides the power to the scanning line driving circuit; the protection circuit protects the scanning line driving circuit from ESD event (see para. [0010]). The modification of AAPA and Lee

discloses the first and second protection circuits connected to the scanning line driving circuit to protect the scanning line driving circuit.

Claim Rejections - 35 USC § 103

5. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 5, 6, 29, 30, 33-36 and 39-43 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Lee et al. (US 6,791,632, “Lee”).

7. **Regarding claims 1, 29 and 35**, AAPA discloses a semiconductor device, the apparatus (fig. 11) comprising: a circuit element included in a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line (750) or a high potential power supply line (751); an input terminal (650 and 651) to supply power; and a first protection circuit (ESD1 and ESD2) connected to the scanning line driving circuit to protect the scanning line driving circuit or the circuit element (since the power supply line provide power to the scanning line driving circuit and the scanning line driving circuit would damage if surge propagate on the power supply line) (see para. [0010]); the first protection circuit being connected to the power supply line between (i) a

first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and the scanning line driving circuit connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the supply line are connected and (iv) a third connecting portion at which the power supply line is connected.

8. AAPA does not explicitly disclose a second protection circuit that is connected to the powers supply line. Lee discloses a protection circuit from electrostatic discharge of TFT-LCD, the apparatus (fig. 3) comprising: a first protection circuit (IESD1) and a second protection circuit (IESD2) connected to a power line to protect the power line (col. 1, lines 59-62). It is well known in the art that connecting protection circuits on both ends of the power line to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. Connecting the protection circuit to the power supply line would provide protection to any circuits that are connected to the power supply line since the protection circuits suppress transient on the power supply line before it gets to the protected circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Lee in order to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. Furthermore, adding additional ESD protection circuit onto existing device is viewed to be duplication of part, which is dependent upon the operation condition and design requirement for particular application. Therefore, it would have been obvious to

one of ordinary skill in the art at the time of the invention was made to add additional ESD protection circuit since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. In re Harza, 274, F.2d 669, 124 USPQ 378 (CCPA 1960).

9. The Examiner suggests connecting the second ESD protection circuit to the power supply line either between circuit elements, i.e., scanning line driving unit circuits (801-1 - 801-480) or the last node of the power supply line.

10. **Regarding claim 5**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, the first protection circuit being arranged in the first corner portion of the substrate, and the second protection circuit being arranged in the second corner portion of the substrate (see fig. 11).

11. **Regarding claims 6, 34 and 40**, AAPA discloses the semiconductor device being display device.

12. **Regarding claim 30**, AAPA discloses a scanning line driving unit circuit (801-1 – 801-480) included in the scanning line driving circuit (see fig. 11).

13. **Regarding claims 33 and 39**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, and the first protection circuit being arranged in the first corner portion of the substrate. AAPA in view of Lee does not explicitly disclose the

location of the second protection circuit. However, choosing a location for the second protection circuit, such as the second corner portion of the substrate, is dependent upon design requirement and available of the location. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to place the second protection circuit at the second corner portion of the substrate since it dependent upon design requirement and availability of the location and such location does not change perspective function of the second protection circuit.

14. **Regarding claim 36**, AAPA discloses a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element (see fig. 11).

15. **Regarding claims 41, 42 and 43**, AAPA discloses a semiconductor device, the apparatus (fig. 11) comprising: a circuit element included in a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line (750) or a high potential power supply line (751); an input terminal (651) connected to the power supply line to supply power; a first protection circuit (ESD2) that is connected to the power supply line to protect the power supply line/ the scanning line driving circuit/ part of the circuit element (the ESD protecting the power supply line is the same as protecting the scanning line driving circuit or the circuit element since the power supply line provides voltage to the scanning line driving circuit and the scanning line driving circuit would damage if surge propagates in the power supply line) (see para. [0010]), the first protection circuit being connected to the power supply line between (i) a first

connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the power supply line is connected.

16. AAPA does not explicitly disclose a second protection circuit that is connected to the power supply line. Lee discloses protection circuit and method from electrostatic discharge of TFT-LCD, the apparatus (fig. 3) comprising: a first protection circuit (IESD1) and a second protection circuit (IESD2) connected to a power line to protect the power line (col. 1, lines 59-62). It is well known in the art that connecting protection circuits on both ends of the power line to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Lee in order to ensure ESD event is suppressed when one of the ESD protection circuit fail, the other one still provides protection for the semiconductor device. Furthermore, adding additional ESD protection circuit onto existing device is viewed to be duplication of part, which is dependent upon the operation condition and design requirement for particular application. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to add additional

ESD protection circuit since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. In re Harza, 274, F.2d 669, 124 USPQ 378 (CCPA 1960).

17. AAPA in view of Lee does not explicitly disclose the location of the second protection circuit. However, choosing a location for the second protection circuit, such as the second side of the scanning line driving circuit, is dependent upon design requirement and available of the location. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to place the second protection circuit at the second corner portion of the scanning line driving circuit since it dependent upon design requirement and availability of the location and such location does not change perspective function of the second protection circuit.

18. Claim 2 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee, and further in view of Kitagawa (US 2004/0141269, "Kitagawa").

19. AAPA discloses a plurality of scanning line driving unit circuit (801-1 – 801-480) being included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line.

20. AAPA does not explicitly disclose a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. Kitagawa

discloses a plurality of protection circuits (29 together with ESD protection circuits 311-315 and diodes 32, 34 and 35) being connected to power supply line (VDD1-VDD3 and GND1-GND3) to protect plurality of protected circuits (23-25), the protection circuit (311) connected between the first protected circuit (23) and the second protected circuit (25), the first protected circuit and the second protected circuit being adjacent to each other. Kitagawa illustrates that the ESD surge voltage can occur in any line, i.e., I/O signal, high voltage supply line, or low voltage supply line. Kitagawa solution would bring the circuit of AAPA robust since the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the teaching of Kitagawa because the ESD surge voltage can occurs in any line and all the scanning line driving unit circuits should be protected against ESD pulses.

21. Claims 31, 32, 37 and 38 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lee, and further in view of Yamazaki et al. (US 2004/0075094, "Yamazaki").

22. **Regarding claims 31, 32, 37 and 38**, AAPA and Lee disclose the limitations as discussed above. AAPA does not explicitly disclose the scanning line driving circuit included a buffer circuit or transistor. Yamazaki discloses semiconductor display device comprising a scanning line driving circuit including buffer circuits (120-122) which form of transistor (see para [0239] and also see figure 19). The scanning line driving circuit

including buffer circuit or transistor is well known in the art since the buffer would amplify the input signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement buffer in the scanning line driving circuit in order to amplify the input signal. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use transistor in the scanning line driving circuit since transistor provides fast switching.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277.

The examiner can normally be reached on M-Th: 8:00-7:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/TIEN MAI/
Examiner, Art Unit 2836
09/02/2014

/REXFORD BARNIE/
Supervisory Patent Examiner, Art Unit 2836

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
122872.01	12/436,335	May 6, 2009
First Named Inventor:	**Title:**	
Yutaka KOBASHI	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
   - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
   - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
     - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
     - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
       - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
       - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/David J. Zibelli/for James A. Oliff	December 10, 2014
Name (Print/Typed) David J. Zibelli	**Practitioner Registration No.** 36,394

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☑ * Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2836

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI — Group Art Unit: 2836

Application No.: 12/436,335 — Examiner: T. MAI

Filed: May 6, 2009 — Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In reply to the September 10, 2014 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; ~~and~~

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line;

a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and

a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power

supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The display device as set forth in claim 1, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

6. (Original) An electronic device provided with the display device as set forth in claim 1.

7-28. (Canceled)

29. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

30. (Previously Presented) The display device as set forth in claim 29, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit.

31. (Previously Presented) The display device as set forth in claim 29, further comprising:

a buffer circuit included in the scanning line driving circuit.

32. (Previously Presented) The display device as set forth in claim 29, further comprising:

a transistor included in the scanning line driving circuit.

33. (Previously Presented) The display device as set forth in claim 29, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

34. (Previously Presented) An electronic device provided with the display device as set forth in claim 29.

35. (Currently Amended) A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element, the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

36. (Previously Presented) The display device as set forth in claim 35, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.

37. (Previously Presented) The display device as set forth in claim 35, further comprising:

a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.

38. (Previously Presented) The display device as set forth in claim 35, further comprising:

a transistor included in the scanning line driving circuit, the transistor being the circuit element.

39. (Previously Presented) The display device as set forth in claim 35, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

40. (Previously Presented) An electronic device provided with the display device as set forth in claim 35.

41. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

42. (Currently Amended) A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

43. (Currently Amended) A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect a part of the circuit element, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

REMARKS

Claims 1, 5, 6 and 29-43 are pending in this application. By this Amendment, claims 1, 29, 35, and 41-43 are amended and claim 2 is canceled. No new matter is added. Reconsideration of the rejections is requested based on the amendments and the following remarks. This Amendment is being filed with an AFCP 2.0 Request.

I. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claims 29, 33 and 34 as being a substantial duplicate of claims 1, 5 and 6. Claim 1 is amended to include the features of claim 2, so this rejection is moot. Withdrawal of the rejection is requested.

The Office Action rejects claims 1, 5, 6, 29, 30, 33, 34, 36, 39-43 under 35 U.S.C. §103(a) over AAPA in view of Lee et al. (U.S. Pat. No. 6,791,632), rejects claim 2 under 35 U.S.C. §103(a) over AAPA in view of Lee and Kitagawa et al. (U.S. 2004/0142269), and rejects claims 31, 32, 37 and 38 under 35 U.S.C. §103(a) over AAPA in view of Lee and Yamazaki et al. (U.S. 2004/0075094). These rejections are respectfully traversed.

Regarding independent claims 1, 29, 35, and 41-43, the Office Action asserts that Lee discloses first and second protection circuits connected to a power line to protect the power line. However, claims 1 and 29 recite "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit." Independent claim 35 likewise recites "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element." Lee and the other applied references do not disclose first and second protection circuits connected to the scanning line driving circuit to protect the scanning line driving circuit or to protect the circuit element.

In addition, the independent claims all recite that the first and second protection circuits are connected to the power supply line and that the first and second protection

circuits are connected to the scanning line drive circuit. These features require that the first and second protection circuits are connected to one power supply line ("the power supply line" as recited in the independent claims) and to the scanning line drive circuit. Lee and the AAPA do not disclose or suggest such first and second protection circuits are connected to one power supply line ("the power supply line") and to the scanning line drive circuit. The protection circuits of Lee are not connected to a scanning line drive circuit, but instead connect the data line ESD protection units DESD1 and DESD3072 to the ITO. See Lee at column 3, lines 8-12.

The Office Action improperly equates the "power line" of Lee to the claimed "power supply line connected to the scanning line driving circuit" when in fact the ITO line of Lee Fig. 3 is in fact a common electrode used to supply voltages to the TFTs in the matrix by use of the silver dots 114. See Lee col. 1, lines 35-62. Thus, Lee does not disclose or suggest applying ESD circuits to a power supply line connected to a scanning line drive circuit as recited in the present claims, but instead applies ESD protection circuits at various locations within a TFT matrix array.

Lee explains that static electricity can damage the TFT array, and Fig. 3 of Lee uses a variety of ESD protection units to protect the TFT array. See Lee at col. 2, line 36- col. 3, line 11 and Fig. 3. Lee thus utilizes ESD protection units to protect the TFT array, but provides no teaching or suggestion that such ESD protection circuits should be used to protect a scanning line driving circuit by using first and second protection circuits connected to the power supply line and connected to the scanning line drive circuit as recited in the present claims.

Additionally, it is noted that the LCD module shown in Lee includes not only the TFT array, but also a scanning line driver circuit 202, but Lee does not disclose using any of the ESD protection units in association with the scanning line driver circuit. Thus, Lee teaches to

use the protection units in the TFT array, but does not use any protection circuits in to protect a scanning line driving circuit, or a power supply line connected to the scanning line driving circuit as recited in the present claims. Lee therefore provides not motivation to utilize its ESD protection circuits with the power supply line and scanning line driving circuit of the AAPA.

Furthermore, the addition of the second protection circuit is not just a mere duplication of parts as asserted in the Office Action. Instead, the second protection circuit, as disclosed in the specification, provides additional ESD protection not provided by just the first protection circuit.

Independent claims 41-43 additionally recite that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit. The Office Action asserts that this feature is obvious without providing any reference teaching the features, but instead asserts that the location of the protection circuits is dependent upon design requirement and available location. However, as noted above, the protection circuits of Lee are arranged to protect the TFT array, and thus are presumably positioned near the TFT array and thus all on one side of the scanning line driving circuit. The AAPA does not remedy this deficiency of Lee.

For the above reasons, claims 1, 29, 35, and 41-43, and all claims dependent therefrom, would not have been obvious over the applied references. Withdrawal of the rejections is respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: December 10, 2014

Attachment:
AFCP 2.0 Request

OLIFF PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

Electronic Acknowledgement Receipt

EFS ID:	20919977
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Customer Number:	27049
Filer:	James Albert Oliff/Kristin Bennett
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	122872.01
Receipt Date:	10-DEC-2014
Filing Date:	06-MAY-2009
Time Stamp:	14:12:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	12287201_AFCP.pdf	159948 96bf28771a2c0889b100517626f1b89fb4fc24e2	no	2
Warnings:					
Information:					

2		12287201_AAFR.pdf	552608 0602845407314c444b319e2dbda6b40de717eb4d	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	13

Warnings:	
Information:	
Total Files Size (in bytes):	712556

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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FTO/SB/06 (09-11)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335	Filing Date 05/06/2009	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/10/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 26	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 6	Minus	*** 6	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MARCUS PRIDGEN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 01/05/2015

OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
01/05/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 12/436,335	**Applicant(s)** KOBASHI, YUTAKA	
	Examiner TIEN MAI	**Art Unit** 2836	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 10 December 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
(2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: .
Claim(s) objected to: .
Claim(s) rejected: .
Claim(s) withdrawn from consideration: .

/THIENVU TRAN/ Supervisory Patent Examiner, Art Unit 2836	/TIEN MAI/ Examiner, Art Unit 2836

Continuation of 3. NOTE:

The newly added limitation such as "a third protection circuit connected to the power supply line between a first scanning line driving circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other" in claim 1 requires further consideration and/or search.

Continuation of 12. NOTE:

Claims 29 and 35, the newly recitation, such as "the first protection circuit and the second protection circuit are connected to the power supply line", does not differentiate from the previous claims since the claims already recite the limitation (see last two clauses).

Claims 41, 42 and 43, the newly recitation, such as "the first protection circuit and the second protection circuit are connected to the scanning line drive circuit", does not differentiate from the previous claims, since the claims already recite the limitation (see last two clauses).

PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2836

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DO NOT ENTER: /T.M./

In reply to the September 10, 2014 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI

Group Art Unit: 2836

Application No.: 12/436,335

Examiner: T. MAI

Filed: May 6, 2009

Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the provisions of 37 C.F.R. §1.114, Applicant(s) hereby request(s) continued examination (2nd or subsequent request).

☒ Applicant(s) further request(s) entry and consideration of the submission filed **December 10, 2014**.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

The fees associated with this filing are being paid electronically with this filing. The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

/David J. Zibelli/

James A. Oliff
Registration No. 27,075

David J. Zibelli
Registration No. 36,394

JAO:DJZ/kjb

Date: January 27, 2015

OLIFF PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461

Electronic Patent Application Fee Transmittal	
Application Number:	12436335
Filing Date:	06-May-2009
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Filer:	James Albert Oliff/Kristin Bennett
Attorney Docket Number:	122872.01
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 2nd and Subsequent Request	1820	1	1700	1700
		Total in USD ($)		**1700**

Electronic Acknowledgement Receipt	
EFS ID:	21322386
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Customer Number:	27049
Filer:	James Albert Oliff/Kristin Bennett
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	122872.01
Receipt Date:	27-JAN-2015
Filing Date:	06-MAY-2009
Time Stamp:	16:07:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1700
RAM confirmation Number	2179
Deposit Account	150461
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	_201501271-27-15_RCE.pdf	19863 44a1c7d75de79c735091d91cffc7b40ddce66f76	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30742 95e6409548f24ae69c827c92452ae5007bcd5df6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	50605		

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New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/436,335	Filing Date 05/06/2009	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/27/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 26	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 6	Minus	*** 6	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/RENEE HAWKINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 04/23/2015

OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
04/23/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction27049@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/10/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,5,6 and 29-43* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,5,6 and 29-43* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/27/2015 has been entered. Upon entering amendment, claims 1, 29, 35 and 41-43 have been amended; claim 2 has been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 29, 35 and 41-43 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6 and 29-43 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Fujita (US 2005/0052384, "Fujita").

5. **Regarding claims 1, 6, 29, 30, 34-36 and 40**, AAPA discloses a display device or semiconductor device, the apparatus (fig. 11) comprising: a circuit element included in a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line (750) or a high potential power supply line (751); an input terminal (650 and 651) to supply power; a first protection circuit (ESD1 and ESD2) connected to the scanning line driving circuit to protect the scanning line driving circuit or the circuit element (since the power supply line provide power to the scanning line driving circuit and the scanning line driving circuit would damage if surge propagate on the power supply line) (see para. [0010]); and a plurality of scanning line driving circuits (801-1 to 801-480) included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line, the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and the scanning line driving circuit connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the supply line are connected and (iv) a third connecting portion at which the power supply line is connected.

6. AAPA does not explicitly disclose second and third protection circuits connected to the power supply line. Fujita discloses a display device, the apparatus (figs. 1, 2 and 5) comprising: a scanning line driving circuit (130); a power supply line (VDDY, VSSY, VHHY, VLLY, VDDX, VSSX, VHHX and VLLX) connected to the scanning line driving circuit, the supply line being one of the low potential power supply line or a high potential power supply line; an input terminal (not shown) connected to the power supply line to supply power, a plurality of scanning line driving circuits (132a(1) – 132a(m) and a portion of a shift register (131)) included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; a first protection circuit, a second protection circuit and a third protection circuit (represent by a block circuit 133; fig. 5 illustrates protective circuit has one input (512), one output (513), low power supply line (VSSY) and high power supply line (VDDY), each of the protective circuit protects input signals (DY, YCK and YCKB) from ESD) connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection and the second protection circuits are connected to the power supply line (see fig. 5), the third protection circuit connected to the power supply line (see fig. 5) between a first scanning line driving circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. Fujita's goal is to protect all the signal inputs and outputs of the scanning line driving circuit from electrostatic discharge by using a plurality protective circuits (simply into one block such

as 133, 134a and 134b). Each of the protective circuit has number of ESD protection circuit elements to protect each of the input signals or output signals (see para. [0079] and [0080]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the ESD protection circuit structure, as taught by Fujita, in order to protect both the scanning line driving circuit and each of the pixel in the image display area, since the ESD would be deteriorated or destroy these function circuits.

7. **Regarding claims 5, 33 and 39**, AAPA discloses a substrate (see para. [0006]), the scanning line driving circuit being arranged on the substrate, the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate, the first protect circuit being arranged in the first corner portion of the substrate. AAPA discloses in figure 11 that number of ESD protection circuits (ESD1 - ESD4) arrange between the first corner portion and a third corner portion. AAPA and Fujita does not explicitly disclose the second protection circuit being arranged in the second corner portion of the substrate. However, choosing a location for the ESD protection, such as the second corner portion of the substrate, is dependent upon available location, design requirement and/or operating condition. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further modify the system of AAPA in view of Fujita, and place the second protection circuit at second corner portion of the substrate, since choosing a location for the ESD protection, such as the second corner portion of the substrate, is dependent upon available location, design requirement and/or operating condition.

8. **Regarding claim 31 and 37**, Fujita discloses a buffer circuit (515 in the ESD protection circuit; un-number element in circuit 132a(1)-132a(m)) included in the scanning line driving circuit.

9. **Regarding claim 32**, Fujita discloses a transistor (in fig. 5) included in the scanning line driving circuit.

10. **Regarding claim 38**, the shift register of Fujita inherently has transistors.

11. **Regarding claims 41-43**, AAPA discloses a display device, the apparatus (fig. 11) comprising: a circuit element included in a scanning line driving circuit (801); a power supply line (750 and 751) connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line (750) or a high potential power supply line (751); an input terminal (651) connected to the power supply line to supply power; a first protection circuit (ESD2) that is connected to the power supply line to protect the power supply line/ the scanning line driving circuit/ part of the circuit element (the ESD protecting the power supply line is the same as protecting the scanning line driving circuit or the circuit element since the power supply line provides voltage to the scanning line driving circuit and the scanning line driving circuit would damage if surge propagates in the power supply line), the first protection circuit connected to the scanning line driving circuit (see para. [0010]), the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and the scanning line driving circuit being

connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the power supply line is connected.

12. AAPA does not explicitly disclose second protection circuit connected to the power supply line. Fujita discloses a display device, the apparatus (figs. 1, 2 and 5) comprising: a scanning line driving circuit (130); a power supply line (VDDY, VSSY, VHHY, VLLY, VDDX, VSSX, VHHX and VLLX) connected to the scanning line driving circuit, the supply line being one of the low potential power supply line or a high potential power supply line; an input terminal (not shown) connected to the power supply line to supply power, a plurality of scanning line driving circuits (132a(1) – 132a(m) and a portion of a shift register (131)) included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; a first protection circuit, a second protection circuit and a third protection circuit (represent by a block circuit 133; fig. 5 illustrates protective circuit has one input (512), one output (513), low power supply line (VSSY) and high power supply line (VDDY), each of the protective circuit protects input signals (DY, YCK and YCKB) from ESD) connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection and the second protection circuits are connected to the power supply line (see fig. 5), the third protection circuit connected to the power supply line (see fig. 5) between a first scanning line driving circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the

second scanning line driving unit circuit being adjacent to each other. Fujita's goal is to protect all the signal inputs and outputs of the scanning line driving circuit from electrostatic discharge by using a plurality protective circuits (simply into one block such as 133, 134a and 134b). Each of the protective circuit has number of ESD protection circuit elements to protect each of the input signals or output signals (see para. [0079] and [0080]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the semiconductor device of AAPA and utilize the ESD protection circuit structure, as taught by Fujita, in order to protect both the scanning line driving circuit and each of the pixel in the image display area, since the ESD would be deteriorated or destroy these function circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran ThienVu can be reached on 571-270-1276. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TIEN MAI/
Examiner, Art Unit 2836
04/18/2015

/THIENVU TRAN/
Supervisory Patent Examiner, Art Unit 2836

Notice of References Cited	Application/Control No. 12/436,335	Applicant(s)/Patent Under Reexamination KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0052384	03-2005	Fujita, Shin	345/087
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM
see updated East search	01/22/2013	TM
see updated East search	4/16/2014	TM
see updated East search	4/18/2015	TM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:37
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB;	OR	ON	2007/02/13 10:39

			USPAT			
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42
S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18
S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00
S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02

S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2008/04/14 12:39

			IBM_TDB			
S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52
S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB;	OR	ON	2009/02/05 09:28

			USPAT			
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54
S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 13:03
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04

S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19
S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over$1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50
S102	5	"11113120"	US-	OR	ON	2009/11/03

			PGPUB; USPAT; EPO; JPO; IBM_TDB			11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 11:23
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39
S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2009/11/03 12:40

			IBM_TDB			
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:47
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40
S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45
S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2010/02/26 14:46

			IBM_TDB			
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15
S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40
S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO;	OR	ON	2010/09/15 15:23

			IBM_TDB			
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S159	2	"20040141269"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/20 18:36
S160	36	"5936687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 13:10
S161	5	("5936687" | "5953191" | "5973901" | "6649944" | "6753836").PN. OR ("6985340").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 13:14
S165	13	"6801416"	US-	OR	OFF	2011/01/24

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO			17:50
S166	2	inverter with via near versa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:02
S167	31856	inverter with high with low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S168	2484	inverter near2 high near2 low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S169	13	inverter near2 high near2 low near input near signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:33
S170	3	11/101450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:47
S171	3997	protect$3 near (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S172	168	protect$3 near (buffer inverter) and esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S173	14	("20030107424" | "20030214768" | "20050093069" | "4264941" | "4384287" | "4466120" | "5287241" | "5691557" | "6507469" | "6583972" | "6590264" | "6643109" | "6671146" | "7064942").PN. OR ("7663851").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 19:50
S174	3	11/101450	US-PGPUB; USPAT	OR	ON	2013/01/15 10:07
S175	56	esd and plurality near internal near circuit	US-PGPUB; USPAT; USOCR;	OR	ON	2013/01/17 21:57

			EPO; JPO; IBM_TDB			
S176	7	("5679971" | "6014298" | "6624992" | "6762086" | "7692907" | "7827512" | "7869174").PN. OR ("8339757").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/17 21:57
S177	0	(11/766788).APP.	USPAT; USOCR	OR	ON	2014/04/16 11:54
S179	9	("6791632" | "5696928" | "20020105512" | "20030020845" | "20060001787" | "20050190168" | "20060001787" | "5619222" | "20060279667" | "5734722" | "6791632").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 11:55
S180	1	(10/180979).APP.	USPAT; USOCR	OR	ON	2014/04/16 12:11
S181	26	("5068748" | "5596342" | "5909035" | "5936687" | "6043971" | "6088073").PN. OR ("6791632").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 12:17
S182	1	13/115749	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:11
S183	1	"8456791"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:14
S184	14	tien near mai.xa. and rf	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:19
S185	117	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060146458" | "20070053130" | "20070139850" | "20090103226" | "20090109584" | "20090284888" | "20110080683" | "20110141646" | "20110159727" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4841253" | "4864250" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5278720" | "5321573" |	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:22

		"5353189" | "5442330" | "5537044" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" | "6502599" | "6527004" | "6721155" | "6754060" | "6757152" | "6785110" | "6789560" | "6814100" | "6968852" | "6975496" | "7082022" | "7104282" | "7106572" | "7130103" | "7159236" | "7215221" | "7221550" | "7250829" | "7430103" | "7623332" | "7808752").PN. OR ("8456791").URPN.				
S186	31	("20030072121" | "20030179533" | "20050259376" | "20070025043" | "4409637" | "4554608" | "5053910" | "5122921" | "5278720" | "5896265" | "6061223" | "6451773" | "6452773" | "6492894" | "6606232" | "6636407" | "6721155" | "7035073" | "7094104" | "7170728").PN. OR ("7623332").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:23
S187	133	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040042149" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060120005" | "20060139832" | "20060146458" | "20070053130" | "20070095400" | "20070097583" | "20070139850" | "20090103226" | "20090109584" | "20090296430" | "20110141646" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4356360" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5170151" | "5278720" | "5321573" | "5353189" | "5412526" | "5442330" | "5537044" | "5611224" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5798790" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6226166" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" |	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:24

		"6502599" | "6527004" | "6535369" | "6650203" | "6721155" | "6754060" | "6757152" | "6782329" | "6785110" | "6789560" | "6814100" | "6816348" | "6968852" | "6975496" | "7082022" | "7092230" | "7104282").PN. OR ("7106572" | "7130103" | "7159236" | "7221550" | "7250829" | "7338547" | "7371970" | "7453268" | "7471172" | "7507105" | "7623332" | "7808752" | "7817398").PN. OR ("8599528").URPN.				
S188	19	("20050243493" | "4571656" | "5390337" | "5978199" | "6529357").PN. OR ("7221550").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:26
S189	24	"3956717"	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:34
S190	9196	buffer with (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:21
S191	1674	buffer near2 (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:22
S192	1196	buffer near2 (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:23
S193	416	buffer near (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:24
S194	2958	buffer with (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S195	738	buffer near3 (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S196	243	buffer near2 (scan$4 near line gat$3) near (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:26
S197	1	(10/667518).APP.	USPAT; USOCR	OR	ON	2014/04/16 22:34
S198	2550	(advantage benefit) near transistor	US-PGPUB; USPAT; USOCR;	OR	ON	2014/04/16 23:16

			EPO; JPO; IBM_TDB			
S199	4	11/101450	US-PGPUB; USPAT	OR	ON	2014/08/29 11:30
S200	1	13/061267	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2014/09/02 09:26
S201	4	"12436335"	US-PGPUB; USPAT	OR	ON	2015/04/15 17:51
S202	4	scanning near driving near circuit same (esd electro$1static near discharg$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/04/18 00:42
S203	27	("20040264080" | "6791632" | "20040075094" | "20090149923" | "20020009890" | "6623990" | "20020068388" | "20030030054" | "4654865" | "5719647" | "20040085284" | "6795143" | "5329185" | "6572849" | "6157361" | "6329694" | "6075686" | "5786616" | "6028465" | "20050151706" | "6175394" | "20030030054" | "20020057392" | "5610427" | "6108056" | "6351364" | "5936687" | "6791632" | "20040141269").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/04/18 01:32

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S138	8	capacit$4 near3 signal near line with capacit$4 near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:22
S139	1442	capacit$4 adj (protect$4 circuit) near3 signal near line with capacit$4 (protect$3 circuit) near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S140	2	capacit$4 near (protect$4 circuit) with signal near line same capacit$4 near (protect$3 circuit) with (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S141	0	capacit$4 near (first second) near protect$3 near circuit and capacit$4 near (third fourth) near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:30
S142	26	capacit$4 near protect$3 near circuit same (greater lower bigger larger) same capacit$4 near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:31

4/ 18/ 2015 1:35:13 PM
C:\ Users\ tmai4\ Documents\ EAST\ Workspaces\ 12436335.wsp

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yutaka KOBASHI	Group Art Unit: 2836
Application No.: 12/436,335	Examiner: T. MAI
Filed: May 6, 2009	Docket No.: 122872.01

For: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In reply to the April 23, 2015 Office Action, reconsideration of the rejection is respectfully requested in light of the following remarks.

Remarks.

REMARKS

Claims 1, 5, 6 and 29-43 are pending in this application. Reconsideration of the rejection is requested based on the perfection of the priority date and the following remarks.

I. The Pending Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 5, 6 and 29-43 under 35 U.S.C. §103(a) over AAPA in view of newly applied Fujita (U.S. 2005/0052384). However, attached hereto is an English language translation of the priority document. A certified copy of the priority document was filed in the parent application. Accordingly, the July 5, 2004 priority date of the present application is perfected, and thus Fujita is not prior art against the application, because of Fujita's July 20, 2004 U.S. filing date. Withdrawal of the rejection is therefore requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

/David J. Zibelli/

James A. Oliff
Registration No. 27,075

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Registration No. 36,394

JAO:DJZ/kjb

Attachment:
Translation of Priority Document

Date: June 16, 2015

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DEPOSIT ACCOUNT USE AUTHORIZATION
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CERTIFICATE

I, Tae-dong KIM, residing at 405 Gureum Vill, 580-1, Gusan-Dong, Ilsanseo-Gu, Kyunggi, 411-801 Korea, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2004-198040 and certify that the following is a true translation to the best of my knowledge and belief.

Tae-Dong Kim May 29, 2015

Signature of Translator Date

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[Reference Number] J011113701
[Destination] Director General of the Patent Office, Esq.
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[Identification of Handling Fee]
[Payment in Advance Register Number] 013044
[Paid Amount] 16,000
[List of Submitted Documents]
[Document] Claims 1
[Document] Specification 1
[Document] Drawings 1
[Document] Abstract 1
[General Power of Attorney] 0109826

[Name of Document] CLAIMS

[Claim 1]

A semiconductor device comprising:

a plurality of semiconductor circuits arranged on a substrate;

wiring lines electrically connected to the semiconductor circuits;

input terminals electrically connected to the wiring lines to supply electrical signals; and

protective circuits connected to the wiring lines to protect the wiring lines or the semiconductor circuits from static electricity or noise,

wherein at least one semiconductor circuit among the semiconductor circuits is disposed between the input terminals and the protective circuits.

[Claim 2]

The semiconductor device according to Claim 1,

wherein the electrical resistance between a connection part connecting the at least one semiconductor circuit among the plurality of semiconductor circuits to the wiring lines and a connection part connecting the wiring lines to the input terminals, is lower than the electrical resistance between a connection part connecting the protective circuits to the wiring lines and a connection part connecting the wiring lines to the input terminals.

[Claim 3]

The semiconductor device according to Claim 1 or 2,

wherein a plurality of the protective circuits are arranged, and at least one semiconductor circuit among the semiconductor circuits is arranged between the protective circuits.

[Claim 4]

The semiconductor device according to Claim 3,

wherein the plurality of protective circuits are arranged with a predetermined gap therebetween.

[Claim 5]

The semiconductor device according to any one of Claims 1 to 4,

wherein the wiring lines include a low potential power line that supplies at least relatively low reference potential and a high potential power line that supplies relatively high reference potential, and at least one protective circuit is connected to both of the low potential power line and the high potential power line to form a power source protective circuit.

[Claim 6]

The semiconductor device according to Claim 5,

wherein the input line has a signal input line that transmits a signal which is not a fixed reference potential, and at least one protective circuit is a protective circuit

between signal power sources, in which either the low potential power line or the high potential power line is connected to the signal line.

[Claim 7]

The semiconductor device according to Claim 5 or 6,

wherein a capacitive element is provided at least between the low potential power line and the high potential power line, or between the signal line and the low potential power line, or between the signal line and the high potential power line, and the capacitance of the capacitive element is not less than $I \times t \times 0.1$ (F) when the maximum current flowing in the low potential power line or the high potential power line is I (A), and smaller one of tolerable times when a voltage drop in the low potential power line or in the high potential power line occurs is t (second).

[Claim 8]

The semiconductor device according to Claim 7,

wherein t is not more than 10^{-8} (second).

[Claim 9]

The semiconductor device according to any one of Claims 6 to 8,

wherein the capacitance between the signal input line and the low potential power line or the high potential power line is lower than the capacitance between the low potential power line and the high potential power line.

[Claim 10]

The semiconductor device according to any one of Claims 1 to 9,

wherein at least one of the power source protective circuit and the signal power source protective circuit includes a diode element, and one end of the diode element is connected to either the low potential power line or the high potential power line.

[Claim 11]

The semiconductor device according to any one of Claims 5 to 10,

wherein each of the plurality of semiconductor circuits includes a first transistor being an n-channel type field effect transistor and a second transistor being a p-channel type field effect transistor, and at least a part of the first transistor is connected to the low potential power line and at least a part of the second transistor is connected to the high potential power line.

[Claim 12]

The semiconductor device according to Claim 11,

wherein each of the first transistor and the second transistor has a polysilicon thin film serving as an active layer, and the substrate is an insulating substrate.

[Claim 13]

The semiconductor device according to any one of Claims

1 to 12,

wherein a plurality of active elements are formed in a matrix on the substrate, and at least a part of the plurality of semiconductor circuits constitutes a driving circuit for supplying a drive signal to the plurality of active elements.

[Claim 14]

The semiconductor device according to Claim 13,

wherein internal protective circuits are arranged at corners far from the input terminals among four corners of the plurality of active elements arranged in the matrix shape.

[Claim 15]

A display device including:

a first substrate having the semiconductor device according to any one of Claims 1 to 14 formed thereon,

a second substrate opposing the first substrate, and

a liquid crystal layer interposed between the first substrate and the second substrate.

[Claim 16]

A display device including the semiconductor device according to any one of Claims 1 to 14, on which an organic EL element is formed.

[Claim 17]

An electronic apparatus having the display device

according to Claim 15 or 16.

[Name of Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

[Technical Field]

[0001]

The present invention relates to a semiconductor device, display device and electronic apparatus, and more particularly, to a display device having a driving circuit provided on an active matrix substrate.

[Background Art]

[0002]

In a semiconductor device, it is important to take measure against the electro-static damages (ESD) when a high voltage caused by a static electricity or a various noise phenomenon is unintentionally applied to the inside of the device to damage an insulating film, thereby causing a fatal damage to the device. In order to prevent the problem, various protective circuits have been proposed. For example, in Patent Documents 1 and 2, it has been proposed that an abnormal voltage applied to lines is discharged to GND, etc. by proper combination of diodes. However, since general semiconductor devices are formed on a silicon wafer made of conductive material, there are little chances of being electrified within the semiconductor device, so that it is a key issue to prevent the damage when a static electricity

flows through input terminals. To solve such a problem, conventionally, protective circuits are formed between input terminals and the semiconductor device forming a circuit, i.e., immediately after the input terminals, so that it is prevented that the high voltage from the input terminals is transmitted to the device.

[0003]

On the other hand, in a display device using an active element such as a thin film transistor (TFT), which has been rapidly spread in recent years, a device is formed on an insulating substrate. As a result, there is a problem in that it is easy that the device is easily electrified by static electricity, and that the electro-static damage is generated during the manufacturing process. On this account, for example, an electro-static measure is taken by forming an antistatic line, called as a guide ring or a short ring, at the periphery of an active matrix circuit.

[0004]

In recent years, a display device having a built-in driving circuit has been widely spread, in which an improvement of a definition, a cost reduction and better reliability are realized by using a polysilicon TFT having polysilicon serving as an active layer. In such a device, as a measure against the static electricity of the driving circuit, a conventional method used in a semiconductor on a

silicon wafer is applied as it is, so that only protective circuits for preventing the static electricity from the input terminals are built in, and a conventional method of a display device not having the built-in driving circuit is used to protect the active matrix circuit from the static electricity. Hereinafter, the conventional art relating to the protection of the driving circuit will be described in detail with respect to FIG. 11.

[0005]

FIG. 11 is a view illustrating a configuration of an active matrix substrate of a VGA-LCD using polysilicon TFT by the conventional art. Reference numerals 201-1 to 201-480 indicate scanning lines of the active matrix circuit, driven by a scanning line driving circuit 800. Reference numerals 202-1 to 202-1920 indicate data lines, and pixel transistors 401 composed of n-type TFT and pixel electrodes 402 are formed at intersections of the scanning lines and the data lines, respectively, to drive a liquid crystal device.

[0006]

Reference numerals 801-1 to 801-480 indicate scanning line driving unit circuits composed of 480 stages, which form the scanning line driving circuit 800, and each of them is composed by a CMOS circuit. A specific configuration of the scanning line driving unit circuits 801-1 to 801-n is

shown in FIG. 5.

[0007]

Each of the scanning line driving unit circuits 801-1 to 801-480 is connected to a low potential power line 750 and a high potential power line 751, through which power is supplied. The low potential power line 750 is connected to a low potential power terminal 650, the high potential power line 751 is connected to a high potential power terminal 651. Also, the low potential power terminal 650 and the high potential power terminal 651 are connected to a power IC through a FPC, and they are supplied with reference potentials of a potential VS and a potential VD, respectively. Herein, VS is less than VD.

[0008]

Further, a signal (for example, a clock signal) required for the operation of each of the scanning line driving unit circuits 801-1 to 801-480 are supplied from an external IC through signal lines 701 and 702 and signal terminals 601 and 602.

[0009]

Here, in order to prevent TFTs constituting each of the scanning line driving unit circuits 801-1 to 801-480 from being damaged by the static electricity or noise current input through the low potential power terminal 650, the high potential power terminal 651 and the signal terminals 601

and 602, static electricity protection circuits ESD1 to ESD4 are provided between the input terminals 601, 650 and 651 and the scanning line driving unit circuits 801-1 to 801-480, respectively. A specific configuration of the static electricity protection circuit ESD1 to ESD4 is shown in Patent Document 1 and Patent Document 2.

[0010]

[Patent Document 1] Japanese Patent No. 2884946

[Patent Document 2] Japanese Patent No. 3141511

[Disclosure of the Invention]

[Problems to be Solved by the Invention]

[0011]

However, in the driving circuit on an insulating substrate, it is difficult for charges to escape as compared to the circuit on silicon wafer, and it is easy to be electrified. In addition, in the case that the driving circuit of the display device is formed on a glass substrate, the area of the circuit is larger as compared to the IC formed on a general silicon wafer. Therefore, in such a configuration, there is a problem in that a protection of the wiring lines far from the input terminals against the static electricity is not sufficient, especially during a manufacturing process. Specifically, since there is a possibility that the static electricity is electrified on a certain location on the substrate during the manufacturing

process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation. Such a problem is the same in a semiconductor device using a SOI substrate.

[0012]

Further, in a case of an insulating substrate, a large current may flow in the wiring lines by electrostatic induction when strong electrostatic discharge occurs in the outside of the substrate even in a finished product state after completion of the manufacturing process. Even in such a case, there is a possibility that a circuit located far from the terminal is damaged.

[0013]

Furthermore, the present invention provides a measure against the problem in that potentials on the wiring lines are instantaneously changed, when a large amount of current flows in the wiring lines through a circuit.

[Means for Solving the Problems]

[0014]

In order to solve the above problems, it is proposed that a semiconductor circuit be disposed between protective

circuits and input terminals. More specifically, it is proposed that an electrical resistance between a connection part connecting the semiconductor circuit to wiring lines and input terminals be lower than an electrical resistance between a connection part connecting the protective circuits to the wiring lines and the input terminals.

[0015]

Thus, there is an effect that the protection against the static electricity is sufficiently obtained even in a place far from the terminal, by providing internal protective circuits in an area which is not connected to the input terminals of the wiring lines as well as providing the protective circuits around the input terminals as in the conventional art.

[0016]

Further, it is proposed that a plurality of the protective circuits are arranged on the wiring lines and the semiconductor circuit is interposed between the protective circuits. Thereby, it is possible to prevent the static electricity or noise input from the input terminals, and to protect a semiconductor circuit far from the input terminals. In addition, it is preferable that the plurality of the protective circuits be arranged with a predetermined gap therebetween, thereby the entire part of the semiconductor circuit connected to the wiring lines can be protected.

[0017]

Furthermore, in the present invention, it is proposed that the wiring line include a low potential power line and a high potential power line, and the protective circuits between power sources connected to both of the low potential power line and the high potential power line is comprised. In this configuration, the protective circuit can be easily formed by a diode element, etc., and since all are power lines, it is difficult to be affected by the noise. Also, in general, the power line is remarkably lengthened within a circuit, so that it requires a static protection more than other lines. Therefore, the effect is remarkable. In addition to this, for a signal line, it is proposed that the protective circuits between signal power sources be formed between the power lines. Since it is easy to be affected by the noise between the signal lines, it is possible to reduce an adverse influence by providing the protective circuit between the power source and the signal line. Also, it is proposed that the capacitance of the protective circuits between signal power sources be lower than the capacitance of the protective circuits between the power sources. In this way, it is possible to minimize an influence on the power line by the signal.

[0018]

Further, in the present invention, the capacitive

component between the wiring lines in the protective circuits is not less than $I \times t \times 0.1$ (F) when the maximum current flowing in the low potential power line or the high potential power line is I (A) and the maximum tolerable time when a voltage drop in power line occurs is t (second). t is preferably below 10^{-8} (second) in consideration of general operation time in a polysilicon TFT. Thereby, when a large amount of current flows in the circuit and a supply from the outside is not sufficient to follow it to generate instantaneous voltage changes on the wiring lines, there is an effect that the voltage changes are reduced by the capacitive components within the protective circuits.

[0019]

Further, in the present invention, it is proposed that the protective circuit between power sources or the protective circuit between signal power sources include a diode element, and one end of the diode element is connected to the power line. In this configuration, the static electricity or the noise current is easily discharged, so that the protective performance is remarkably improved.

[0020]

Further, in the present invention, it is proposed that contents of the invention described above is applied to a so-called CMOS type semiconductor device, which is composed of an n-channel type field effect transistor and a p-channel

type field effect transistor. Because the CMOS type semiconductor device requires at least 2 types of reference power source, the number of power line is increased, so that the effect of this invention is remarkable. Particularly, in the CMOS type semiconductor device composed of the polysilicon thin film transistor, the substrate is an insulating substrate, and thus electrification easily occurs under a state in which there is no protective circuit, so that the effect of the present invention is more prominent. Further, when an active matrix used in a TFT-LCD or TFT-OLED and a driving circuit thereof are formed on the insulating substrate, the driving circuit is configured to surround the active matrix, so that it becomes larger and accordingly its line is also lengthened. As a result, the effect of the present invention is more remarkable.

[0021]

Further, in the present invention, it is proposed that, when the active matrix is applied to the present invention, internal protective circuits are arranged at corners far from the input terminals among four corners of the active matrix. By such a configuration, it is possible to arrange large-sized protective circuits without making the peripheral area large.

[0022]

Moreover, in a display device using the semiconductor

device of the present invention and an electronic apparatus having the display device, the electro-static damage is difficult to be generated during a manufacturing process, so that it is advantageous in terms of cost, and it is difficult that the voltage drop at the power source occurs, so that there is an effect that the display quality is improved.

[Best Mode for Carrying Out the Invention]

[0023]

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings.

[First Embodiment]

[0024]

FIG. 1 is a view illustrating a configuration of an active matrix substrate having a built-in scanning line driving circuit according to a first embodiment in which a liquid crystal display device using a scanning line driving circuit of the present invention is implemented. 480 Scanning lines 201-1 to 201-480 and 1920 data lines 202-1 to 202-1920 are provided orthogonally to each other on an active matrix substrate 101, and 480 capacitance lines 203-1 to 203-480 are alternately arranged in parallel to the scanning lines 201-1 to 201-480. The data lines 202-1 to 202-1920 are connected to data line input terminals 302-1 to 202-1920. The capacitance lines 203-1 to 203-480 are short-

circuited from one another to be connected to a common potential input terminal 303. An opposite conductive part 304 is also connected to the common potential input terminal 303.

[0025]

A pixel switching device 401-n-m composed of n-channel type field effect thin film transistor is formed at each intersection of the scanning line 201-n and the data line 202-m. Also, its gate electrode is connected to the scanning line 201-n, and its source and drain electrodes are connected to the data lines 202-m and pixel electrodes 402-n-m, respectively. The pixel electrode 402-n-m constitutes a capacitance line 203-n and an auxiliary capacitor, and forms a capacitor together with an opposing substrate electrode COM with a liquid crystal device therebetween when it is assembled as the liquid crystal display device.

[0026]

The scanning lines 201-1 to 201-480 are connected to the scanning line driving circuit 800, which is formed by integrating polysilicon thin film transistors on the active matrix substrate, thereby being supplied with a drive signal. Herein, the scanning line driving circuit is composed of 480 scanning line driving unit circuits 801-1 to 801-480 which are connected to each of the scanning lines. In the present invention, the semiconductor circuit in the scope of claims

is the scanning line driving circuit 800. Further, the wiring lines in the scope of claims represents a CLK signal line 701, a SP signal line 702, a high potential power line 751, and a low potential power line 750.

[0027]

The CLK signal line 701, the SP signal line 702, the high potential power line 751, and the low potential power line 750 are connected to the scanning line driving circuit 800, to which a clock pulse signal, a start pulse signal and respective power potentials are supplied. Herein, The CLK signal line 701, the SP signal line 702, the high potential power line 751 and the low potential power line 750 are connected to the CLK signal terminal 601, the high potential power terminal 651 and the lower potential power terminal 650, and the terminals is connected to an external IC through a FPC to receive a desired signal and a power potential.

[0028]

A first to a fourth protective circuits ESD1 to ESD4 are connected to a connecting line between CLK signal terminal 601 and a CLK signal line 701, a connecting line between a SP signal terminal 602 and a SP signal line 702, a connecting line between the high potential power terminal 651 and the high potential power line 751, and a connecting line between the low potential power terminal 650 and the

low potential power line 750, respectively, thereby preventing TFTs within the scanning line driving circuit 800 from being damaged when the static electricity or noise current is input from each of the terminals 601, 602, 651 and 650.

[0029]

In addition, a fifth to a seventh protective circuits ESD11 to ESD13 are disposed at far end of the opposite side, as seen from the CLK signal terminal 601 on CLK signal line 701, the high potential power terminal 651 on the high potential power line 751, and the low potential power terminal 650 on the low potential power line 750, with a scanning line driving circuit 800 therebetween. Thereby, it is possible to prevent that a unit, (for example, n = 1), located far from a terminal, among scanning line driving unit circuits 801-n, is damaged by the static electricity during manufacturing the active matrix substrate. Further, the fifth to seventh protective circuits ESD11 TO ESD13 can be arranged without making the substrate area larger, if arranged at the corner part of the active matrix substrate, more particularly, at the corner opposite to the input terminals.

[0030]

FIG. 4 is a view illustrating an example of a specific circuit configuration of protective circuits ESD1 to ESD13.

A source electrode and a gate electrode of a p-type transistor 504 are connected to a high potential power source VH, and its drain electrode is connected to a wiring line being protected. A source electrode and a gate electrode A of an n-type transistor 502 are connected to a low potential power VL, and its drain electrode is connected to a wiring line being protected. Here, a signal level given to the wiring line being protected has to be not more than VH and not less than VL. When the potential of the power source being protected is out of the range of VH to VL by the static electricity, the n-type transistor 502 or the p-type transistor 504 is on, thereby an abnormal current runs through a reference potential VH line or a reference potential VL line. Also, by a protective resistor 503, it is possible to prevent that the potentials of the wiring lines rapidly increase to damage the n-type transistor 502 or the p-type transistor 504. Here, as VH and VL, the highest power and the lowest power are used within the circuit, respectively, however, VH = VD, VL = VS may be possible.

[0031]

Further, the protective circuits ESD1 to ESD13 are the same configuration, however, it is possible that each of the protective circuits has a different circuit configuration according to its necessity. Particularly, compared to

internal protective circuits ESD11 TO ESD13, the protective circuits ESD1 to ESD4 of input part are required to have relatively high protective performance. On this account, for example, it is preferable that the first protective circuit ESD1 has a circuit configuration having protective performance higher than the fifth protective circuit ESD11, more specifically, it is preferable that the first protective circuit ESD1 is larger than the fifth protective circuit ESD11 with respect to channel widths of the n-type transistor 502 and the p-type transistor 504.

[0032]

FIG. 5 is a view illustrating an example of a configuration of scanning line driving unit circuits 801-1 to 801-480, which is composed of a NAND circuit, a NOT circuit, and a static type shift register using two clock inverters. Further, an OUT terminal of the scanning line driving unit circuit 801-n at the nth stage (n < 480) is connected to an IN terminal of the scanning line driving unit circuit 801-n-1 at the (n-1)th stage, and the IN terminal of the scanning line driving unit circuit 801-480 at the 480th stage is connected to a SP signal line 702.

[0033]

FIG. 6 is a perspective view (partial sectional view) illustrating a configuration of a transmission liquid crystal display device according to a first embodiment. The

active matrix substrate 101 shown in FIG. 1 is attached to an opposite substrate 901, in which common electrodes are formed by coating ITO on a color filter, by sealant 920, and nematic liquid crystal materials 910 are injected therebetween. Further, conductive materials are disposed in the opposite conductive part 304 provided on the active matrix substrate 101, and is short-circuited from the common electrodes of the opposite substrate 901.

[0034]

A data line input terminals 302-1 to 302-1920, a common potential input terminal 303, a CLK signal terminal 601, a SP signal terminal 602, a high potential power terminal 651, a lower potential power terminal 650 are connected to one or a plurality of external ICs 940 through a FPC 930 mounted on the terminals to be supplied with a required electrical signal and potential.

[0035]

Furthermore, an upper deflection plate 951 is disposed at the external side of the active matrix substrate, a lower deflection plate 952 is disposed at the external side of the opposite substrate, and they are disposed in such a way that polarizing directions thereof are linear. Also, a back light 960 is attached to the lower deflection plate 952, so that a liquid crystal display device is formed. The back light 960 may be a cold cathode tube to which a light

guiding plate or a dispersion plate is attached, or a unit where an entire surface emits light by an EL element. Although it is not shown, according to the necessity, the surrounding may be covered by an outer shell, or a protective glass or an acryl plate may be attached on the upper deflection plate.

[0036]

In the liquid crystal display device, as compared to the conventional art, it is difficult that the electrostatic damage caused by the static electricity is generated during the manufacturing process or after the completion thereof. Therefore, the yield is increased and the reliability is improved.

[Second Embodiment]

[0037]

FIG. 2 is a view illustrating a configuration of a driving circuit in a second embodiment implementing a liquid crystal display device using the scanning line driving circuit of the present invention. The figure is a diagram corresponding to the inside of the frame indicated by a broken line A of FIG. 1.

[0038]

In the present embodiment, not only the input part protective circuits ESD1 to ESD3 between terminals 601, 650 and 651 and the scanning line driving circuit 800 and the

internal protective circuits ESD11 to ESD13 located at the far end with the driving circuit 800 therebetween as seen from input terminals 601, 650 and 651, but also an eighth to a tenth protective circuits ESD21 to ESD23 are provided between the unit driving circuit 801-240 at the 240th stage, which is an intermediate stage of the driving circuit 800, and the unit driving circuit 801-241 at the 241st stage. Thereby, it is possible to prevent the damage caused by the static electricity in the vicinity of the intermediate stage (n = 240), which is far from both the vicinity and the far end of the terminal. In the present embodiment, the protective circuits are added only in the intermediate stage, but it is possible to increase the number of the protective circuit to be interposed in accordance with the size of the circuit. For example, in addition to the locations of the present embodiment, more preferably, the protective circuits are interposed between the 120th stage (801-120) and the 121st stage (801-121) and between the 360th stage (801-360) and the 361st stage (801-361), and most preferably the protective circuits are interposed between all stages if there is no problem in the circuit area. However, in any case, a distance when interposing the protective circuits should be approximately equal, otherwise, it is easy that the electro-static damage occurs only in a place where the distance is large.

[0039]

With respect to the configuration of the active matrix substrate and the details of the protective circuits or the driving circuit in a place other than the above specified place, the second embodiment is the same as the first embodiment. Also, for the liquid crystal display device using the active matrix substrate including the circuit shown in FIG. 2, the configuration is the same as in the first embodiment, so that the explanation is omitted.

[Third Embodiment]

[0040]

FIG. 3 is a view illustrating a configuration of an active matrix substrate having formed with a scanning line driving circuit in a first embodiment implementing a liquid crystal display device using the scanning line driving circuit of the present invention.

[0041]

In the present embodiment, differently from the first and second embodiments, a CLK signal and a SP signal applied to the scanning line driving circuit 800 are not directly input from a CLK signal terminal 601 and a SP signal terminal 602, but, after driving capability is amplified at buffer circuits 810-1 and 810-2, they are input to the scanning line driving circuit 800. By such a configuration, when the signal driving capability of the external IC is not

so high, it is possible to drive the signal without big delay even in a panel having a large area.

[0042]

FIG. 7 is a detailed view illustrating a configuration of the buffer circuits 810-1 and 810-2 in the third embodiment. A first NOT circuit 821 and a second NOT circuit 822 are connected in series by two stages, the transistor constituting the second NOT circuit 822 has a channel width wider than the transistor constituting the first NOT circuit 821. For example, the first NOT circuit 821 is set to be W = 250 μm, the second NOT circuit 822 is set to be W = 1000 μm. A power line 850 is a branch line rising from the low potential power line 750 of FIG. 3, and the power line 851 is a branch line rising from the high potential power line 751 of FIG. 3, wherein a white circle mark indicates a branching point direction, and a eleventh and a twelfth circuits ESD41 and ESD42 are disposed at the opposite side, i.e., at the end of the branch lines 850 and 851 with the buffer circuit 810-1 and 810-2 interposed therebetween.

[0043]

In such a configuration, the buffer circuits 810-1 and 810-2 are connected to a part between the first protective circuit ESD11 and the eleventh protective circuit ESD41 on the low potential power line 750 and the a part between the

second protective circuit ESD12 and the twelfth protective circuit ESD42 on the high potential power line 750, so that the protective performance when the static electricity is electrified within the buffer circuit 810-1 and 810-2 is remarkably improved as compared to the case in which there is only the first protective circuit ESD11.

[0044]

FIG. 8 is a detailed view illustrating another example of a configuration of the buffer circuits 810-1 and 810-2 in the third embodiment. As compared to the configuration of FIG. 7, a thirteenth protective circuit ESD51 and a fourteenth protective circuit ESD51 are added on the wiring line connecting a connection point of a first NOT circuit 821 with a connection point of a second NOT circuit 822 provided on the low potential power line 750 and the high potential power line 751. The other configuration is the same as in FIG. 7. As such, there are internal protective circuits in the intermediate points between circuits, and thus the protective performance is more improved.

[0045]

Further, in this embodiment, there is another effect that the voltage change in power source is prevented. Since the resistance of the power source is limited, when a large current is instantaneously consumed in a complementary circuit, the voltage is changed even though it is partial

and instantaneous. According to the present embodiment, the channel width of the second NOT circuit 822 is W = 1000 μm, which is so large, and so large current instantaneously flows to change the potential of the power source when the input signal is inverted (the time depends on the capacitance of the wiring line to which the output terminal of the second NOT circuit 822 is connected).

[0046]

FIG. 10 is a view illustrating a simulation result of potential change with respect to time in the buffer circuit of FIG. 7 and FIG. 8. Hereinafter, the present embodiment will be described in detail by referring to FIG. 10. Graph 880 shows a waveform of the signal which is output from the first NOT circuit 821 and input to the second NOT circuit 822, in which the potential is changed from VS to VD. At this time, the n-type transistor constituting the second NOT circuit 822 is turned on to apply the potential of the output terminal to VS. In this case, a large current flows in the low potential power line 850, so that a voltage gradient is generated. As a result, the potential is instantaneously risen a little. In order to prevent this, it is preferable to widen the line width of the low potential power line 850, but it may be limited due to a circuit area. The graph 881 shows the potential around the second NOT circuit 822 of the low potential power line 850,

when the low potential power line 850 is fixed as a predetermined line width, especially, when counter measures are not taken, and it can be seen that the voltage is instantaneously risen.

[0047]

When such a phenomenon occurs, the driving capability of the buffer circuit is deteriorated, and it is possible to have an adverse effect on other lines connected to the low potential power line 850. In other words, the voltage drop as in graph 881 is transmitted to another circuit through the low potential power line 850, thereby causing malfunction in the worst case. As a result, it affects the output precision in a case of an analog circuit. Such a problem is more remarkable in a TFT circuit on an insulating substrate, which has a circuit area larger than a circuit on a silicon wafer, and especially, in the display circuit of the display device.

[0048]

Next, the graph 882 shows a result of the case in which an appropriate capacitive element is added to the low potential power line. In this case, the current instantaneously flowing is supplied from the capacitive element to some degree, and thus the voltage drop is small. In other words, in order to reduce the voltage drop, the capacitive element is preferably added to the power line.

The larger the capacitance of the capacitive element is, the greater the effect of reducing the voltage drop is. However, according to the present invention, assuming that the maximum current flowing in the power line is I (A) and a tolerable time when a voltage drop occurs is t (second), the capacitive element having a capacitance not less than I x t x 0.1 (F) is effective on the voltage drop, on the other hand, the capacitive element having a capacitance not more than I x t x 0.1 (F) is not effective on the voltage drop. Here, the tolerable time t when the voltage drop is generated is determined by maximum operation speed of a logical circuit or sampling time of an analog circuit. Generally, in the TFT using a polysilicon, the operation speed is not so high and the limit of the maximum operation is only 10 MHz. In other words, the power voltage change not more than 10n second almost causes no problem. Further, the maximum current flowing in the power source is the same as the maximum instantaneous consumption current of the circuit.

[0049]

Accordingly, assuming that the maximum current consumed in the circuit is I (A) and the tolerable time when the voltage drop is generated is t (second), it is effective on reduction of the voltage drop to add a capacitance not less than I x t x 0.1 (F) to the power source. At that time, the

time is preferably $t \leq 10^{-8}$ (second). Further, it is preferable that another power line of which the potential is not changed is connected to the capacitance. However, when such a capacitance is provided, the circuit area increases. As such, when a plurality of protective circuits are disposed on the power line as in the embodiment, a capacitance is generated between the power line being protected and the reference potential power line VH and VL by the capacitive components on the protective circuits. In this case, since the circuit can be used as a protective circuit or as a measure against the power potential change, it is prominent and advantageous in terms of a circuit area.

[0050]

When a reduction of such a power potential drop change is expected, it is necessary to provide the protective circuits near the circuit of which a current consumption is large. Otherwise, a voltage change also occurs by the power line resistance between the circuit having a large current consumption and the protective circuits. Specifically, the distance (X) of the power line from the circuit having a large current consumption to the protective circuits should be smaller than the distance (Y) of the power line from the circuit having a large current consumption to the input terminals.

[0051]

The specific configurations of the first to second and the eleventh to fourteenth protective circuits ESD1 to ESD2, and ESD11 to ESD14 is preferably the same as in FIG. 4 or FIG. 9. The explanation on the circuit configuration of FIG. 4 is omitted since it is the same as in the first embodiment, but even in this configuration, the capacitance is added between the wiring line protected by the gate-drain capacitance component of the transistor and the high potential power source VH and the lower potential power source VL. In the configuration of FIG. 9, as compared to the configuration of FIG. 4, the first capacitance 505 and the second capacitance 506 are added, and thus, when a strong voltage is instantaneously applied, they are combined with the protective resistor 503 to operate as a CR circuit. Thereby, it is possible to prevent the n-type transistor 502 and the p-type transistor 504 from being damaged. Also, since the capacitances between the protective line and the high potential power source VH and between the protective line and the low potential power source VL can be controlled by a first capacitance 505 and the second capacitance 506, it is so effective configuration as a measure against the power voltage drop.

[0052]

Furthermore, in such a configuration, the capacitance of the protective circuits ESD1, ESD2, ESD11 and ESD12

connected to the low potential power line 750 and the high potential power line 751 should be smaller than the capacitance of the protective circuits ESD3, ESD4 and ESD13 connected to the signal lines 701 and 702. The reason is that the potential of the signal line is changed, so that, if the capacitance between the signal line and the protective circuit is too large, a cross-talk is generated between the protective circuit and the reference power line connected to the signal line. Specifically, if the configuration of the protective circuits is the same as in FIG. 9, the first capacitance 505 and the second capacitance 506 of the protective circuit connected to the low potential power line 750 and the high potential power line 751 is preferably set to be larger than the first capacitance 505 and the second capacitance 506 of the protective circuits ESD3, ESD4 and ESD13 connected to the signal lines 701 and 702.

[0053]

Even in a case of forming a complementary circuit other than the buffer circuit described in the present embodiment, such as a data line driving circuit, DAC circuit, power circuit, level shift circuit, memory circuit, etc. on the active matrix substrate, it is preferable to provide the protective circuits at the end or intermediate of a branched power line, and it is more preferable that all circuits are

located on the power line between protective circuits. Also, it is preferable in terms of reduction of the power noise that protective circuits having a capacitance not less than a predetermined value are provided at the front and rear ends of the circuit having high current consumption. Specifically, when the current consumption of the circuit is I and the tolerable time t when the voltage drop occurs (typically, $t \leq 10^{-8}$ (second)), it is preferable to have the capacitance not less than I x t x 0.1 (F)).

[0054]

With respect to the configuration of the active matrix substrate and the details of the protective circuits or the driving circuit in a place other than the above specified place, the third embodiment is the same as the first embodiment. Also, for the liquid crystal display device using the active matrix substrate shown in FIG. 3, the configuration is the same as in the first embodiment, so that the explanation is omitted.

[0055]

Further, in the first embodiment, only the protective circuit of FIG. 4 has been described, however, it is possible to obtain the same effect as in the third embodiment by providing the protective circuit of FIG. 9.

[Industrial Applicability]

[0056]

The present invention is not limited to the above-mentioned embodiments, but it can be also applicable to a liquid crystal display using an active matrix substrate formed with a data line driving circuit, a DAC, a power circuit, etc. In this case, the present invention may be applicable to each of the circuits, or it may be applied to some of the circuits if there is any problem in layout, and so on. In case of applying it to the scanning line driving circuit, various sequential selection circuits as well as the shift register circuit as in the embodiment are possible.

[0057]

Further, the protective circuits can have the same configuration as in the embodiment and foregoing examples, and any configurations which have been suggested so far can be used.

[0058]

Further, instead of a polysilicon transistor, an amorphous silicon thin film transistor may be used. Also, instead of a thin film transistor formed on the insulating substrate, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is formed on a crystal silicon wafer.

[0059]

Further, as a liquid crystal display device, it may be a reflective type or a transflective type instead of the

transmission type, and it may be a projection type light value instead of a direct viewing type light value. Also, a normally black mode can be used instead of a normally white mode as in the embodiment. Especially, in this case, a vertical alignment mode or a horizontal electric field switching mode may be possible as an alignment mode of the liquid crystal.

[Brief Description of the Drawings]

[0060]

[Fig. 1] Fig. 1 is a view illustrating a configuration of an active matrix substrate for explaining a first embodiment of the present invention;

[Fig. 2] FIG. 2 is a view illustrating a scanning line driving circuit for explaining a second embodiment of the present invention;

[Fig. 3] FIG. 3 is a view illustrating a configuration of an active matrix substrate for explaining a third embodiment of the present invention;

[Fig. 4] FIG. 4 is a view illustrating a protective circuit for explaining embodiments of the present invention;

[Fig. 5] FIG. 5 is a view illustrating a scanning line driving unit circuit for explaining embodiments of the present invention

[Fig. 6] FIG. 6 is a perspective view (partially sectional view) of a liquid crystal display device for

explaining the first embodiment of the present invention;

[Fig. 7] FIG. 7 is a view illustrating a buffer circuit for explaining the third embodiment of the present invention;

[Fig. 8] FIG. 8 is a view illustrating a buffer circuit for explaining another example of the third embodiment of the present invention;

[Fig. 9] FIG. 9 is a view illustrating a protective circuit for explaining the third embodiment of the present invention;

[Fig. 10] FIG. 10 is a graph illustrating a simulation result of a reference potential change for explaining the third embodiment of the present invention; and

[Fig. 11] FIG. 11 is a view illustrating a configuration of an active matrix substrate for explaining the conventional example.

[Reference Numerals]

[0061]

101: active matrix substrate

201-1 to 201-480: scanning lines 1 to 480

202-1 to 201-1920: data lines 1 to 1920

ESD1 to ESD4: first to fourth protective circuits

ESD11 to ESD13: fifth to seventh protective circuits

ESD21 to ESD23: eighth to tenth protective circuits

800: scanning line driving circuit

801-1 to 801-480: scanning line driving unit circuits

FIG. 1

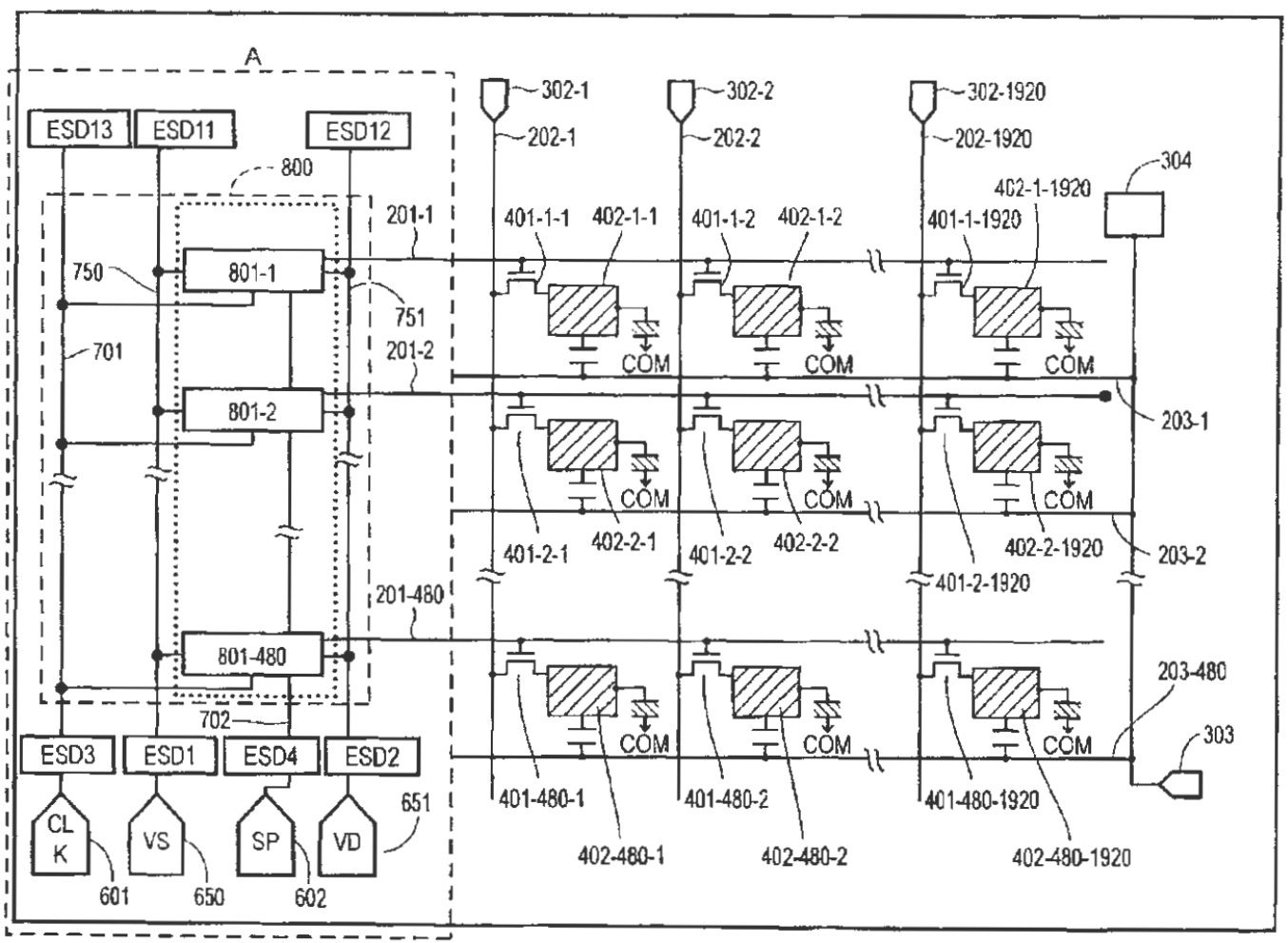

A
ESD13
ESD11
ESD12
800
201-1
750
801-1
751
701
201-2
801-2
201-480
801-480
702
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602
302-1
302-2
302-1920
202-1
202-2
202-1920
304
402-1-1920
401-1-1
402-1-1
401-1-2
402-1-2
401-1-1920
COM
203-1
401-2-1
402-2-1
401-2-2
402-2-2
402-2-1920
401-2-1920
203-2
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303
401-480-1
402-480-1
401-480-2
402-480-2
401-480-1920
402-480-1920

FIG.2

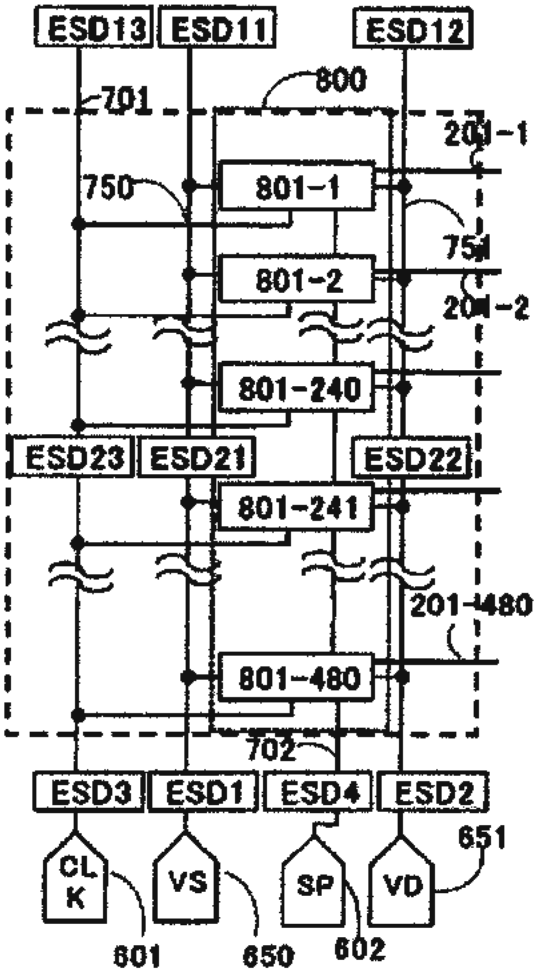

ESD13
ESD11
ESD12
701
800
750
801-1
801-2
801-240
ESD23
ESD21
ESD22
801-241
801-480
702
ESD3
ESD1
ESD4
ESD2
CL K
VS
SP
VD
601
650
602
651

FIG.3

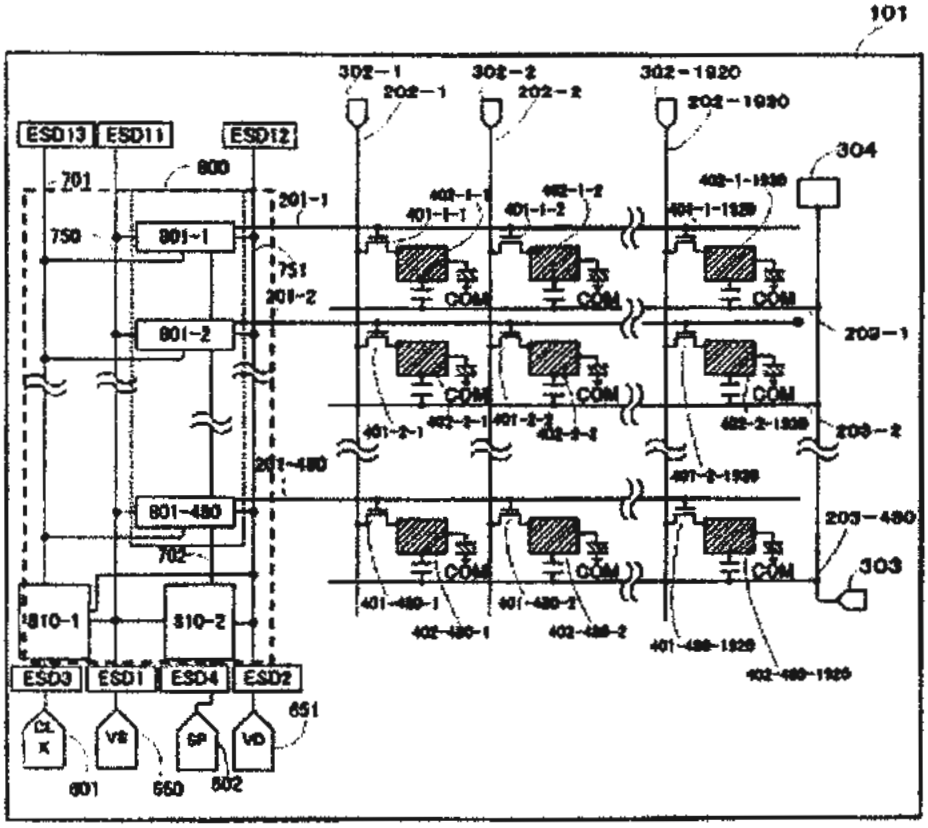

101
302-1
302-2
302-1920
202-1
202-2
202-1920
304
ESD13
ESD11
ESD12
700
701
750
801-1
751
201-1
201-2
801-2
203-1
203-2
801-480
201-480
702
203-480
303
810-1
810-2
ESD3
ESD1
ESD4
ESD2
651
601
660
502
COM

FIG.4

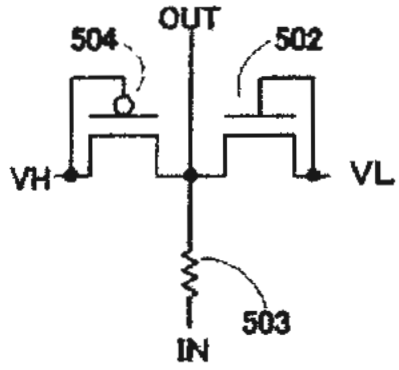

OUT
504
502
VH
VL
503
IN

FIG.5

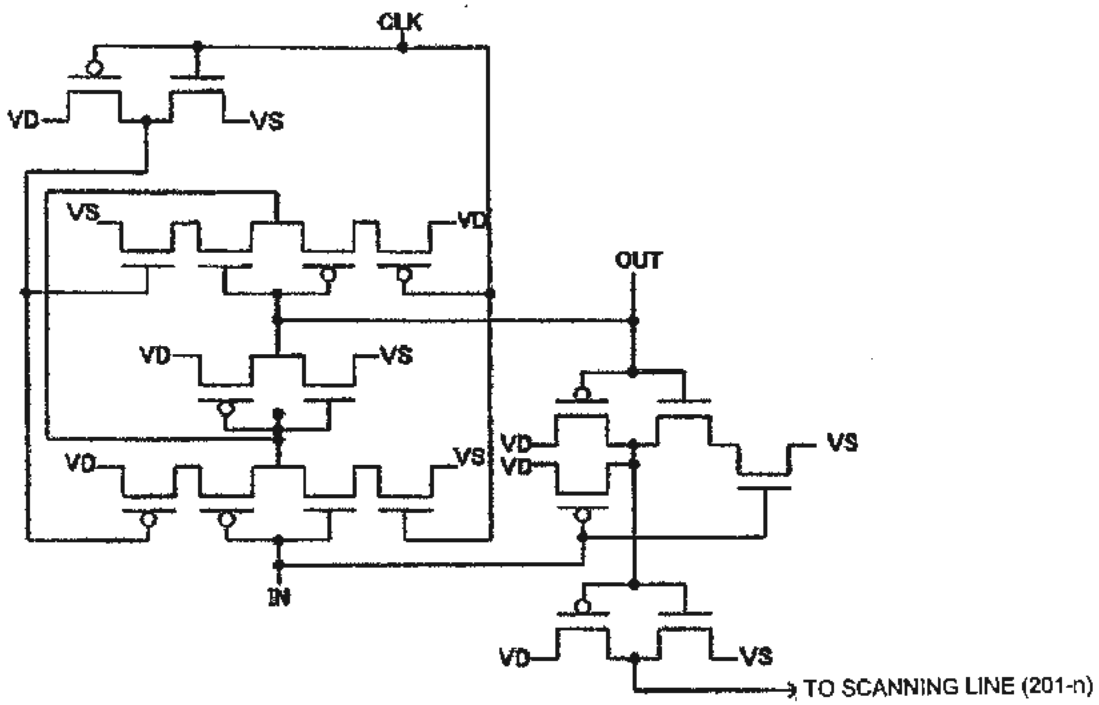

CLK
VD
VS
VS
VD
OUT
VD
VS
VD
VS
VD
VD
VS
IN
VD
VS
TO SCANNING LINE (201-n)

FIG.6

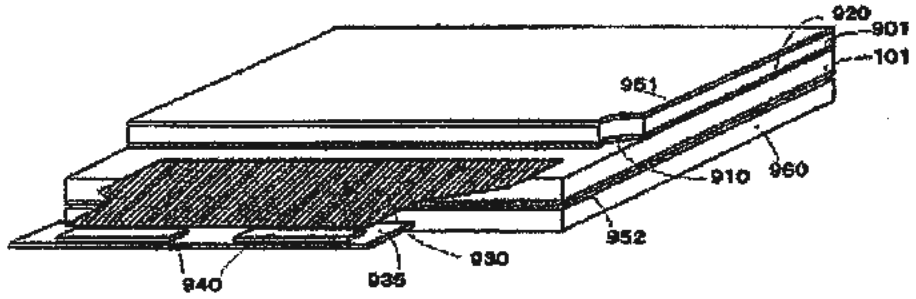

920
901
101
951
910
960
952
930
940
935

FIG.7

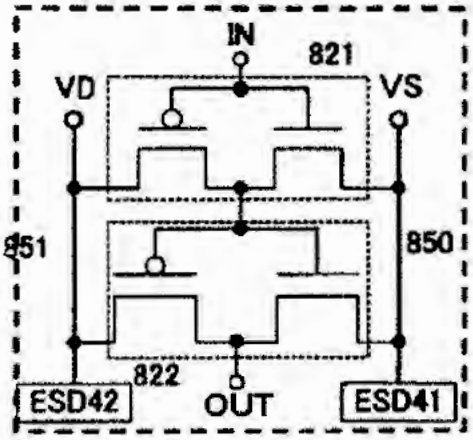


FIG.8

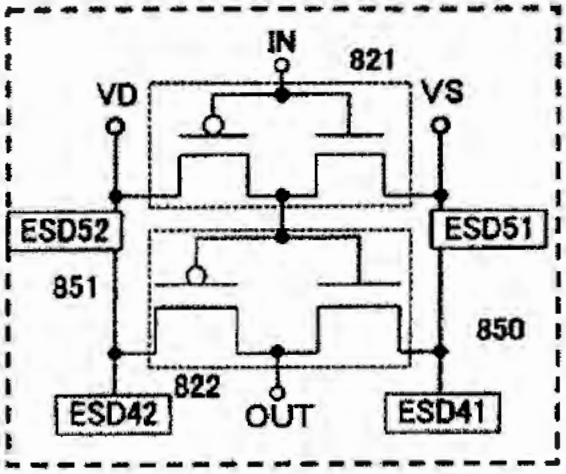


FIG.9

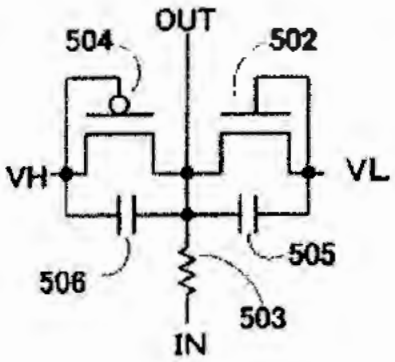


FIG.10

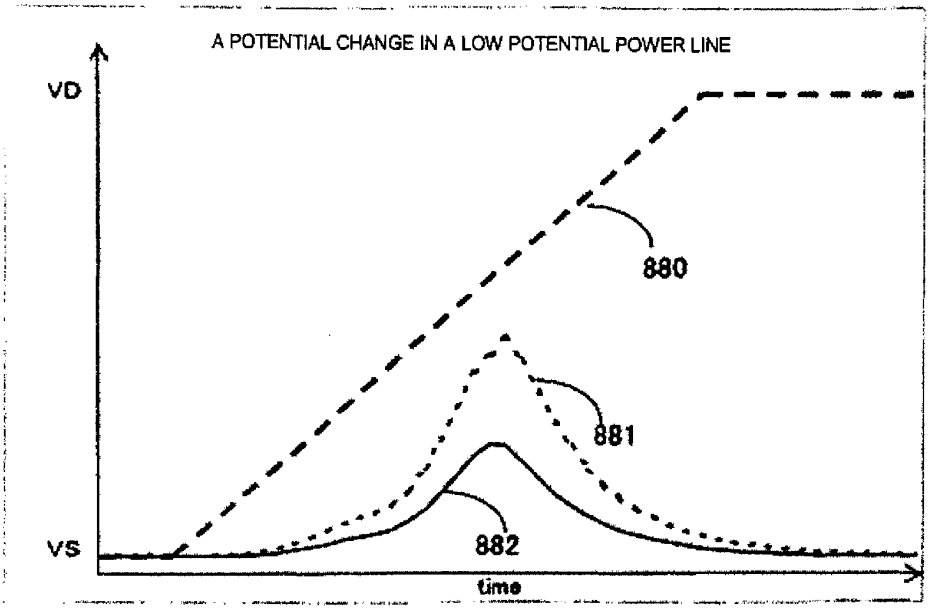
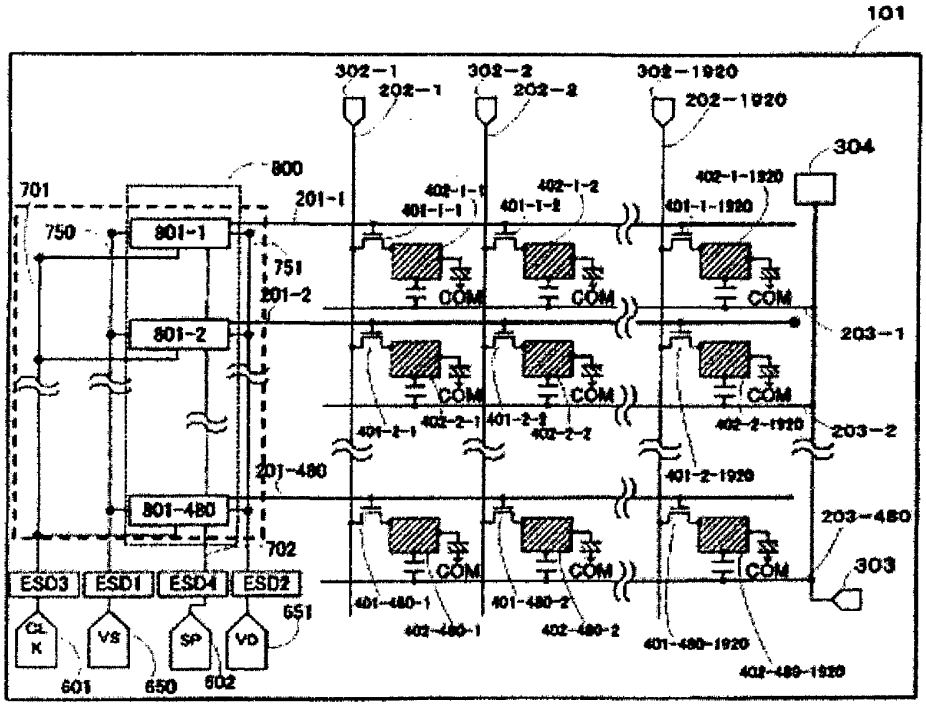

A POTENTIAL CHANGE IN A LOW POTENTIAL POWER LINE
VD
VS
880
881
882
time

FIG.11


101
302-1
202-1
302-2
202-2
302-1920
202-1920
304
800
701
201-1
750
801-1
751
201-2
801-2
203-1
203-2
201-480
801-480
203-480
303
702
ESD3
ESD1
ESD4
ESD2
651
CL K
VS
SP
VD
601
650
602
COM

[Name of Document] ABSTRACT

[Abstract]

[Object] To prevent an electrostatic damage on a display device formed with a driving circuit.

[Solving Means] Protective circuits are provided not only at input terminal parts, but also at intermediate parts of a circuit or at the ends of wiring lines. Otherwise, the protective circuits are provided at the ends of the wiring lines and at the places immediately before and after the input terminals, respectively, and then the circuit is interposed therebetween. Further, the protective circuits are provided around a circuit with a large current consumption.

[Selected Figure] Fig. 2

Electronic Acknowledgement Receipt	
EFS ID:	22648407
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Customer Number:	27049
Filer:	James Albert Oliff/Kristin Bennett
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	122872.01
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	2015061661615_RFR_02.pdf	22788 fb4fa3ba1bf902671bd3ca5aa0ef3c20430a9a9a	no	3
Warnings:					
Information:					

2	Translation of Foreign Priority Documents	20150616J0111137US02_2004-198040_02.pdf	1630235 6bf1971cdde977773f227ffe2b5a3f35839c4d13	no	47

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DATE MAILED: 07/10/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

TITLE OF INVENTION: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/13/2015

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II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27049 7590 07/10/2015

OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

TITLE OF INVENTION: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/13/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
MAI, TIEN HUNG	2836	361-056000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka Kobashi	122872.01	5191

27049 7590 07/10/2015

OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
MAI, TIEN HUNG	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 07/10/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (h)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/436,335	Applicant(s) KOBASHI, YUTAKA	
	Examiner TIEN MAI	Art Unit 2836	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/16/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,5,6 and 29-43*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *11/101450* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/TIEN MAI/ Examiner, Art Unit 2836	

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions. Applicant's response of 06/16/2015 has been entered and considered. Upon entering amendment, no claim has been amended. Claiming foreign priority is acknowledged.

Allowable Subject Matter

2. Claims 1, 5, 6 and 29-43 are allowed.

3. Regarding claim 1, 29, 35, 41, 42 and 43, the prior art of record does not fairly suggest the combination of features set forth in the Applicant's claims. The references do not appear to suggest the feature first and second protection circuits connect to the scanning line driving circuit to protect circuit are connected to the power supply line, in combination with the other features of Applicant's independent claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIEN MAI whose telephone number is (571)270-1277. The examiner can normally be reached on M-Th: 8:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran ThienVu can be reached on 571-270-1276. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TIEN MAI/
Examiner, Art Unit 2836
06/26/2015

/REXFORD BARNIE/
Supervisory Patent Examiner, Art Unit 2836

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20060002045"	US-PGPUB; USPAT	OR	ON	2007/02/14 14:58
S2	268531	semiconductor same substrate	US-PGPUB; USPAT	OR	ON	2007/02/08 12:41
S3	28062	protect$4 adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:42
S4	3404764	wiring adj line conductor cable line conduit	US-PGPUB; USPAT	OR	ON	2007/02/08 12:45
S5	1326	(electrical adj signal power adj supply vdd) near input adj terminal	US-PGPUB; USPAT	OR	ON	2007/02/08 12:56
S6	26	S2 and S3 and S4 and S5	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S7	208840	display adj device	US-PGPUB; USPAT	OR	ON	2007/02/08 13:09
S8	475	S2 and S3 and S7	US-PGPUB; USPAT	OR	ON	2007/02/08 13:10
S9	643	361/91.1.ccls.	US-PGPUB; USPAT	OR	ON	2007/02/12 12:59
S10	276	361/91.1.ccls. and semiconductor	US-PGPUB; USPAT	OR	ON	2007/02/12 13:29
S11	62	esd same display same pixel	US-PGPUB; USPAT	OR	ON	2007/02/12 13:30
S12	39	esd same display same pixel and resist$4	US-PGPUB; USPAT	OR	ON	2007/02/12 15:27
S13	6	esd same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:30
S14	193	display same pixel and protective adj circuit	US-PGPUB;	OR	ON	2007/02/12 15:37

			USPAT			
S15	36	input adj terminal same display same pixel and protective adj circuit	US-PGPUB; USPAT	OR	ON	2007/02/12 15:38
S16	16	(ozawa near2 norio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:39
S17	2	(isono near2 toshio).inv.	US-PGPUB; USPAT	OR	ON	2007/02/13 10:42
S18	2	protect$4 adj circuit$4 same n-type same p-type same high adj potential same low adj potential	US-PGPUB; USPAT	OR	ON	2007/02/13 10:55
S19	2	2002/0057392	US-PGPUB; USPAT	OR	ON	2007/02/13 10:57
S20	1	"10036386"	US-PGPUB; USPAT	OR	ON	2007/02/13 11:57
S22	29	signal adj line same display same capacitance same protect$4	USPAT	OR	OFF	2007/02/14 12:14
S23	39	signal adj line same display same capacitance same protect$4	USPAT	OR	ON	2007/02/13 11:58
S24	1	signal adj line same display same capacitance same organic same (led leds)	USPAT	OR	OFF	2007/02/13 11:59
S25	585	minimize adj capacitance	USPAT	OR	OFF	2007/02/13 12:12
S28	94	minimize adj capacitance and display	USPAT	OR	OFF	2007/02/13 13:36
S29	14	minimize adj capacitance and display same protect$4	USPAT	OR	OFF	2007/02/13 13:19
S32	2	minimize adj capacitance same respond	USPAT	OR	OFF	2007/02/13 13:37
S33	656	361/56.ccls. and esd	USPAT	OR	OFF	2007/02/14 12:15
S34	22	data adj line adj noise	USPAT	OR	OFF	2007/02/14 12:16
S35	1171	data adj line same noise	USPAT	OR	OFF	2007/02/14 12:16
S36	0	S33 and S35	USPAT	OR	OFF	2007/02/14 12:16
S37	325	S33 and capacitance	USPAT	OR	OFF	2007/02/14 12:16
S38	30	S37 and power adj line	USPAT	OR	OFF	2007/02/14 12:17
S39	865	power adj line same capacitance	USPAT	OR	OFF	2007/02/14 12:18
S40	9	S33 and S39	USPAT	OR	OFF	2007/02/14 12:18

S42	88160	n adj type same p adj type	US-PGPUB; USPAT	OR	ON	2007/02/14 15:00
S44	15133	low adj power same high adj power	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S45	1437326	LCD LED display screen	US-PGPUB; USPAT	OR	ON	2007/02/14 15:01
S46	275	S42 and S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:02
S47	11	S42 same S44 and S45	US-PGPUB; USPAT	OR	ON	2007/02/14 15:03
S48	2043	polysilicon adj thin adj film	US-PGPUB; USPAT	OR	ON	2007/02/14 17:39
S49	5	polysilicon adj thin adj film near active adj layer	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S51	39267	substrate near insulating	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S52	518	substrate near insulating and S48	US-PGPUB; USPAT	OR	ON	2007/02/14 17:43
S53	4	polysilicon adj thin adj film near active adj layer and substrate near4 insulati$3	US-PGPUB; USPAT	OR	ON	2007/02/14 17:44
S54	0	dirving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S55	817	driving adj circuit near structure	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:02
S56	215	S55 and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S57	0	S56 and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 11:03
S58	65	driving adj circuit and lcd and esd	US-	OR	ON	2008/04/11

			PGPUB; USPAT; EPO; JPO; IBM_TDB			11:04
S59	9	("5872561").URPN.	USPAT	OR	ON	2008/04/11 11:24
S60	2	2002/0057392	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S61	1	"20020057392"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/11 13:00
S62	595	diode near thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:39
S63	596	diode near thin near film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S64	22	S63 same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:40
S65	149	diode with thin near film same (electrostatic esd)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:58
S66	96	diode with thin near film same (electrostatic esd) same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S67	88	S66 not S64	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 12:59
S68	8	("6191455").URPN.	USPAT	OR	ON	2008/04/14 13:50
S69	9	("4803536" | "5220443" | "5313319" | "5371351" | "5373377" | "5497146" | "5504348" | "5668032" | "5909035").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/14 13:52

S70	1967549	buffer adj circuit with (mos transistor gate) same thin film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:40
S71	183	buffer adj circuit with (mos transistor gate) same thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S72	167	buffer adj circuit with (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S73	9	buffer adj circuit near (mos transistor gate) with thin adj film	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/04/14 14:41
S74	4	(6329694|6351364|20040264080|5719647).pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/10/23 16:29
S75	8	"4654865"	US-PGPUB; USPAT	OR	ON	2009/02/05 09:28
S76	1	S75 and clock near signal and electrostatic	US-PGPUB; USPAT	OR	ON	2009/02/05 09:30
S77	55	(electrostatic esd transient spike) with clock near signal same protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:45
S78	19	Chun$1ching near wei.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 09:54
S79	5	(electrostatic esd transient spike) with clock near (signal line) and lcd and scanning near (line signal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:02
S80	52	(electrostatic esd transient spike) with clock near (signal line) and lcd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 10:29
S81	1	"20030030054"	US-	OR	ON	2009/02/05

			PGPUB; USPAT; EPO; JPO; IBM_TDB			13:03
S84	29	"5,019,002"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/02/05 17:00
S85	598	clock near (signal line terminal wir$3) with (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S86	40	clock near (signal line terminal wir$3) near (electrostatic esd spike transient) and (data near (line signal) address near (line signal) scan$5 near (line signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/02/05 17:10
S87	259	clock near (signal line terminal wire) with (electrostatic esd spike surge transient) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S88	82	S87 and (pixel active near element)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 11:34
S89	4	"6791632"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:04
S90	5	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and LCD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:08
S91	13	protect$3 with (esd transient spike surge electrostatic) with clock near (signal line terminal wire) and display	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S92	8	S91 not S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:12
S93	9	("4066918" | "4078200" | "5574395" | "5640189" | "5774100" | "6078205").PN. OR ("6333661").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 12:19

S94	20	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 12:31
S95	215	349/40.ccls. and (esd transient electrostatic spike surge)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:18
S96	2	349/40.ccls. and (esd transient electrostatic spike surge) same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:27
S97	4388	(display pixel active near element tft lcd led) and clock same (esd electrostatic transient surge spike)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:36
S98	95	(display pixel active near element tft lcd led) and clock with (esd electrostatic transient surge spike over$1voltage over adj voltage) with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/02 13:37
S99	8	("4816815" | "5602567" | "5691741" | "5727191" | "5910806" | "5917468" | "5995089" | "6323828").PN. OR ("6625666").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/02 14:09
S100	28	"5936687"	US-PGPUB; USPAT	OR	ON	2009/11/03 10:27
S101	11	power near line near "750"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 10:50
S102	5	"11113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:20
S103	2	"11/113120"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:23
S104	6	("20030214042" | "7026754").PN. OR ("7126268").URPN.	US-PGPUB;	OR	ON	2009/11/03 11:23

			USPAT; USOCR			
S106	18	(tft display pixel) and clock with esd with protect$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 11:44
S110	346	(pixel tft) and clock with vdd with vss	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:22
S111	20	("20010015715" | "20020024508" | "4789857" | "4822142" | "4908710" | "5012228" | "5365284" | "5701167" | "5721601" | "5754155" | "5838400" | "5850216" | "5959709" | "6075505" | "6300928" | "6380919" | "6462723" | "6545653" | "6545655" | "6690347").PN. OR ("7522145").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/11/03 12:27
S113	126	(display pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:28
S114	9	(pixel active near element tft) and clock with (vdd vss) and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:29
S117	303	(pixel active near element tft) and esd same protect$3 with (input terminal)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:32
S118	154	(pixel active near element tft) and esd same protect$3 with (input terminal) and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:35
S120	283	(pixel active near element tft) and esd near2 protect$3 and clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:39
S122	47	(pixel active near element tft) and (esd transient electrostatic spike surge) near2 protect$3 same clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:40
S123	92	yutaka near kobashi.in.	US-PGPUB; USPAT;	OR	ON	2009/11/03 12:47

			EPO; JPO; IBM_TDB			
S125	128	(pixel active near element tft) and (esd transient electrostatic spike surge) with clock near signal	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/03 12:53
S126	8	"4654865"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2009/11/04 11:40
S127	5	(esd electrostatic) same capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:51
S128	15	(esd electrostatic) and capacitance with signal near line same capacitance with power near line	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 13:58
S129	2	"20060050451"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:18
S130	4	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (coupl$3 connect$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:23
S131	0	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage) near (vdd vss ground)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S132	30	(detect$3 monitor$3 sens$3) near (esd electrostatic) same (disconnect$3 disabl$3 terminat$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:26
S133	2	"11987222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:40
S134	1924	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:45

S135	410	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:46
S136	51	(detect$3 monitor$3 sens$3) near (esd electrostatic) and (connect$3 abl$3 coupl$3) with (capacit$4 storage) with (vdd vss ground power near line) same esd near event	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 14:47
S137	20	("5450267" | "5886862" | "5907464" | "5946177" | "6008970" | "6069782" | "6320735" | "6356427" | "6369998" | "6400540" | "6455902" | "6674622" | "6862161").PN. OR ("7102862").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/02/26 14:55
S143	3	fourth near protective near circuit and esd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2010/02/26 15:45
S144	21	("20020009890" | "20020057392" | "20020068388" | "20030030054" | "20040085284" | "20040264080" | "20040264080" | "20050151706" | "4654865" | "5610427" | "5719647" | "5786616" | "5936687" | "6028465" | "6108056" | "6157361" | "6175394" | "6329694" | "6351364" | "6623990" | "6791632" | "6795143").PN.	US-PGPUB; USPAT	OR	ON	2010/09/14 14:15
S145	1	12/436335	US-PGPUB; USPAT	OR	ON	2010/09/14 15:09
S146	20	"6075686"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/14 17:07
S147	3	"11101450"	US-PGPUB; USPAT	OR	ON	2010/09/15 10:29
S148	1	"7522145"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:31
S149	540	electrostatic near discharge same scr	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 12:40

S150	1303309	(buffer inverter)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S151	25566	S150 with larger	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:23
S152	1088	S151 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S153	2519	(buffer inverter) with larg$2 with channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S154	249	(buffer inverter) with larg$2 near channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S155	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:24
S156	572	(buffer inverter) with larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S157	140	(buffer inverter) near2 larg$2 near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/09/15 15:25
S158	66	(buffer inverter) near2 larger near2 channel	US-PGPUB; USPAT; USOCR; EPO; JPO;	OR	ON	2010/09/15 15:25

			IBM_TDB			
S159	2	"20040141269"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/20 18:36
S160	36	"5936687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 13:10
S161	5	("5936687" | "5953191" | "5973901" | "6649944" | "6753836").PN. OR ("6985340").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 13:14
S165	13	"6801416"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 17:50
S166	2	inverter with via near versa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:02
S167	31856	inverter with high with low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S168	2484	inverter near2 high near2 low	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:32
S169	13	inverter near2 high near2 low near input near signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:33
S170	3	11/101450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 18:47

S171	3997	protect$3 near (buffer inverter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S172	168	protect$3 near (buffer inverter) and esd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/01/24 19:48
S173	14	("20030107424" | "20030214768" | "20050093069" | "4264941" | "4384287" | "4466120" | "5287241" | "5691557" | "6507469" | "6583972" | "6590264" | "6643109" | "6671146" | "7064942").PN. OR ("7663851").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/24 19:50
S174	3	11/101450	US-PGPUB; USPAT	OR	ON	2013/01/15 10:07
S175	56	esd and plurality near internal near circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2013/01/17 21:57
S176	7	("5679971" | "6014298" | "6624992" | "6762086" | "7692907" | "7827512" | "7869174").PN. OR ("8339757").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/17 21:57
S177	0	(11/766788).APP.	USPAT; USOCR	OR	ON	2014/04/16 11:54
S179	9	("6791632" | "5696928" | "20020105512" | "20030020845" | "20060001787" | "20050190168" | "20060001787" | "5619222" | "20060279667" | "5734722" | "6791632").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 11:55
S180	1	(10/180979).APP.	USPAT; USOCR	OR	ON	2014/04/16 12:11
S181	26	("5068748" | "5596342" | "5909035" | "5936687" | "6043971" | "6088073").PN. OR ("6791632").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 12:17
S182	1	13/115749	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:11
S183	1	"8456791"	US-	OR	ON	2014/04/16

			PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB			17:14
S184	14	tien near mai.xa. and rf	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 17:19
S185	117	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060146458" | "20070053130" | "20070139850" | "20090103226" | "20090109584" | "20090284888" | "20110080683" | "20110141646" | "20110159727" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4841253" | "4864250" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5278720" | "5321573" | "5353189" | "5442330" | "5537044" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" | "6502599" | "6527004" | "6721155" | "6754060" | "6757152" | "6785110" | "6789560" | "6814100" | "6968852" | "6975496" | "7082022" | "7104282" | "7106572" | "7130103" | "7159236" | "7215221" | "7221550" | "7250829" | "7430103" | "7623332" | "7808752").PN. OR ("8456791").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:22
S186	31	("20030072121" | "20030179533" | "20050259376" | "20070025043" | "4409637"	US-PGPUB;	OR	ON	2014/04/16 17:23

		| "4554608" | "5053910" | "5122921" | "5278720" | "5896265" | "6061223" | "6451773" | "6452773" | "6492894" | "6606232" | "6636407" | "6721155" | "7035073" | "7094104" | "7170728").PN. OR ("7623332").URPN.	USPAT; USOCR			
S187	133	("20020167302" | "20020191360" | "20030072121" | "20030211782" | "20040042149" | "20040121648" | "20040145849" | "20040264087" | "20050036262" | "20050044858" | "20050176275" | "20050185354" | "20060120005" | "20060139832" | "20060146458" | "20070053130" | "20070095400" | "20070097583" | "20070139850" | "20090103226" | "20090109584" | "20090296430" | "20110141646" | "2030179" | "3167729" | "3323083" | "3619721" | "3663901" | "3731234" | "3750053" | "3783178" | "3831110" | "3845358" | "3944937" | "3980976" | "4046451" | "4047120" | "4112395" | "4262317" | "4356360" | "4359764" | "4384331" | "4409637" | "4481641" | "4554608" | "4563720" | "4586104" | "4689713" | "4698721" | "4727350" | "4952173" | "4984146" | "4985800" | "5053910" | "5057964" | "5102818" | "5122921" | "5124873" | "5142429" | "5166855" | "5170151" | "5278720" | "5321573" | "5353189" | "5412526" | "5442330" | "5537044" | "5611224" | "5617284" | "5625521" | "5667298" | "5721662" | "5781844" | "5790361" | "5798790" | "5844766" | "5854730" | "5953195" | "5966283" | "5982602" | "5986869" | "6054905" | "6060182" | "6061223" | "6086544" | "6115227" | "6137352" | "6141194" | "6177849" | "6226166" | "6236551" | "6243247" | "6252755" | "6281690" | "6292344" | "6342998" | "6381283" | "6385030" | "6394122" | "6421220" | "6502599" | "6527004" | "6535369" | "6650203" | "6721155" | "6754060" | "6757152" | "6782329" | "6785110" | "6789560" | "6814100" | "6816348" | "6968852" | "6975496" | "7082022" | "7092230" | "7104282").PN. OR ("7106572" | "7130103" | "7159236" | "7221550" | "7250829" | "7338547" | "7371970" | "7453268" | "7471172" | "7507105" | "7623332" | "7808752" | "7817398").PN. OR ("8599528").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:24
S188	19	("20050243493" | "4571656" | "5390337" |	US-	OR	ON	2014/04/16

		"5978199" | "6529357").PN. OR ("7221550").URPN.	PGPUB; USPAT; USOCR			17:26
S189	24	"3956717"	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/16 17:34
S190	9196	buffer with (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:21
S191	1674	buffer near2 (scan$4 near line gat$3) near2 (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:22
S192	1196	buffer near2 (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:23
S193	416	buffer near (scan$4 near line gat$3) near (driving circuit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:24
S194	2958	buffer with (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S195	738	buffer near3 (scan$4 near line gat$3) near2 (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:25
S196	243	buffer near2 (scan$4 near line gat$3) near (driving circuit) and display near (apparatus device module)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 21:26
S197	1	(10/667518).APP.	USPAT; USOCR	OR	ON	2014/04/16 22:34
S198	2550	(advantage benefit) near transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2014/04/16 23:16
S199	4	11/101450	US-PGPUB;	OR	ON	2014/08/29 11:30

			USPAT			
S200	1	13/061267	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2014/09/02 09:26
S201	4	"12436335"	US-PGPUB; USPAT	OR	ON	2015/04/15 17:51
S202	4	scanning near driving near circuit same (esd electro$1static near discharg$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/04/18 00:42
S203	27	("20040264080" | "6791632" | "20040075094" | "20090149923" | "20020009890" | "6623990" | "20020068388" | "20030030054" | "4654865" | "5719647" | "20040085284" | "6795143" | "5329185" | "6572849" | "6157361" | "6329694" | "6075686" | "5786616" | "6028465" | "20050151706" | "6175394" | "20030030054" | "20020057392" | "5610427" | "6108056" | "6351364" | "5936687" | "6791632" | "20040141269").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/04/18 01:32
S204	4	12/436335	US-PGPUB; USPAT	OR	ON	2015/06/26 19:39
S205	0	H02H9/00.cpc. and scanning near line near circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/06/26 19:41
S206	0	H02H9/00.cpc. and scanning near line	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/06/26 19:41
S207	68	H02H9/00.cpc.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2015/06/26 19:41
S208	1711	H01L27/0251.cpc.	US-PGPUB; USPAT	OR	ON	2015/06/26 19:51
S209	8	S208 and scanning near line near driving near circuit	US-PGPUB; USPAT	OR	ON	2015/06/26 19:51

S210	0	G02F1/13620.cpc.	US-PGPUB; USPAT	OR	ON	2015/06/26 19:52
S211	999	G02F1/136204.cpc.	US-PGPUB; USPAT	OR	ON	2015/06/26 19:53
S212	48	S211 and scanning near line near driving near circuit	US-PGPUB; USPAT	OR	ON	2015/06/26 19:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S138	8	capacit$4 near3 signal near line with capacit$4 near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:22
S139	1442	capacit$4 adj (protect$4 circuit) near3 signal near line with capacit$4 (protect$3 circuit) near (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S140	2	capacit$4 near (protect$4 circuit) with signal near line same capacit$4 near (protect$3 circuit) with (power near line)	USPAT; UPAD	OR	ON	2010/02/26 15:24
S141	0	capacit$4 near (first second) near protect$3 near circuit and capacit$4 near (third fourth) near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:30
S142	26	capacit$4 near protect$3 near circuit same (greater lower bigger larger) same capacit$4 near protect$3 near circuit	USPAT; UPAD	OR	ON	2010/02/26 15:31
S213	1	(scanning line driving circuit and (electro$1static near discharg$3 or esd or transient surge spike)).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/06/26 18:50
S214	1	(scanning line driving circuit and (electro$1static discharg$3 or esd or transient surge spike)).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/06/26 18:58
S215	4	(scanning line driving circuit and (electro$1static discharg$3 or esd or transient or surge or spike)).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/06/26 18:59

6/26/2015 8:02:52 PM
C:\Users\tmai4\Documents\EAST\Workspaces\12436335.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	**Art Unit**
	TIEN MAI	2836

CPC						
Symbol					**Type**	**Version**
H01L		27	/	0251	F	2013-01-01
H01L		27	/	12	A	2013-01-01
G02F		1	/	136204	I	2013-01-01
G09G		3	/	3208	I	2013-01-01
G09G		3	/	36	I	2013-01-01
G09G		2300	/	043	A	2013-01-01
G09G		2300	/	0819	A	2013-01-01
H01L		27	/	1214	I	2013-01-01
			/			
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

/TIEN MAI/ Examiner.Art Unit 2836	06/26/2015	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/REXFORD BARNIE/ Supervisory Patent Examiner Art Unit 2836	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	**Art Unit**
	TIEN MAI	2836

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
361	56	H	0	2	H	9/00 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
361	56	111			

/TIEN MAI/ Examiner.Art Unit 2836	06/26/2015	Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/REXFORD BARNIE/ Supervisory Patent Examiner.Art Unit 2836	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	**Art Unit**
	TIEN MAI	2836

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17	8	33										
	2		18	9	34										
	3		19	10	35										
	4		20	11	36										
2	5		21	12	37										
3	6		22	13	38										
	7		23	14	39										
	8		24	15	40										
	9		25	16	41										
	10		26	17	42										
	11		27	18	43										
	12		28												
	13	4	29												
	14	5	30												
	15	6	31												
	16	7	32												

/TIEN MAI/ Examiner.Art Unit 2836	06/26/2015	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/REXFORD BARNIE/ Supervisory Patent Examiner Art Unit 2836	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office Part of Paper No. 20150626

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12436335	KOBASHI, YUTAKA
	Examiner	Art Unit
	TIEN MAI	2836

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/0251	6/26/2015	TM
G02F 1/136204	6/26/2015	TM

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
361	56, 111	9/15/2010	TM

SEARCH NOTES		
Search Notes	Date	Examiner
see East search	9/15/2010	TM
see updated East search	1/25/2011	TM
see updated East search	01/22/2013	TM
see updated East search	4/16/2014	TM
see updated East search	4/18/2015	TM
see updated East search	6/26/2015	TM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
USPGPUB; USPAT; UPAD	see interference search	6/26/2015	TM

/TIEN MAI/ Examiner.Art Unit 2836	

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

OLIFF PLC
277 S Washington St.
Suite 500
Alexandria, Virginia 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	05/06/2009	Yutaka KOBASHI	122872.01	5191

TITLE OF INVENTION: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960.00			$960.00	10/10/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
MAI, TIEN HUNG	2836	361-056000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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2
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SEIKO EPSON CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /David J. Zibelli/ Date October 8, 2015

Typed or printed name David J. Zibelli Registration No. 36,394

Electronic Patent Application Fee Transmittal

Application Number:	12436335
Filing Date:	06-May-2009
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Filer:	William P. Berridge/Dana Moore-Galloway
Attorney Docket Number:	122872.01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	23732192
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Customer Number:	27049
Filer:	William P. Berridge/Dana Moore-Galloway
Filer Authorized By:	William P. Berridge
Attorney Docket Number:	122872.01
Receipt Date:	08-OCT-2015
Filing Date:	06-MAY-2009
Time Stamp:	15:11:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	1617
Deposit Account	150461
Authorized User	ZIBELLI, DAVID J
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20151008Issue_Fee_Transmittal.pdf	33069 c34e2eced4e3c6c33ff17073a70ab394bc51fbe5	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31150 dc26bce13b56b2ee3a71ad277f29b86839899a911	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64219		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/436,335	11/10/2015	9184157	122872.01	5191

27049 7590 10/21/2015

OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 207 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yutaka Kobashi, Fujimichou, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	12/436,335
Filing Date	05-06-2009
First Named Inventor	Yutaka Kobashi
Title	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
Art Unit	2836
Examiner Name	MAI, TIEN HUNG
Attorney Docket Number	122872.01

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael L. Bartholomew/	Date (Optional)	
Name	Michael L. Bartholomew	Registration Number	60225
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 36491

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

138 East LCD Advancements Limited

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Ciarán Dempsey	Date (Optional)	
Name	Ciarán Dempsey		
Title	Director, 138 East LCD Advancements Limited		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/AIA/14 (02-18)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fail under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yutaka		Kobashi	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Fujimichou	Country of Residence i	JP

Mailing Address of Inventor:

Address 1			
Address 2			
City	Fujimichou	State/Province	
Postal Code		Country i	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	~~25944~~ 38491		
Email Address	~~email@oliff.com~~ docket@ktslaw	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS		
Attorney Docket Number	122872.01	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	~~25944~~ 36491		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	11/101450	2005-04-08

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
2004-198040	JP	2004-07-05	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. **Priority Document Exchange (PDX)** - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. **Search Results from U.S. Application to EPO** - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

⊗ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	~~SEIKO EPSON CORPORATION~~ 138 EAST LCD ADVANCEMENTS LIMITED		
Mailing Address Information For Applicant:			
Address 1	~~4-1, Nishi-shinjuku 2-chome, Shinjuku-ku~~ FIRST FLOOR, BLACKTHORN EXCHANGE		
Address 2	BRACKEN ROAD, SANDYFORD		
City	~~Tokyo~~ DUBLIN	**State/Province**	
Country	~~JP~~ IRELAND	Postal Code	D18 P3Y9
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country[i]		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Michael L. Bartholomew/			Date (YYYY-MM-DD)	2021-05-19
First Name	Michael	Last Name	Bartholomew	Registration Number	60225

Additional Signature may be generated within this form by selecting the Add button.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	122872.01
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	42766931
Application Number:	12436335
International Application Number:	
Confirmation Number:	5191
Title of Invention:	SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Yutaka Kobashi
Customer Number:	27049
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	122872.01
Receipt Date:	19-MAY-2021
Filing Date:	06-MAY-2009
Time Stamp:	18:57:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	2021-05-19_Statement_under_37-CFR-3_73c.pdf	122194 f6118d7a9e07f875917d7afbc59a280c11b8eab3	no	3

Warnings:

Information:					
2	Power of Attorney	2021-05-19_3430_2_365US3_CombinedPOA.pdf	457177 e0713a9ec86dc186827823ca195c5ab3c99a0764	no	2
Warnings:					
Information:					
3	Application Data Sheet	2021-05-19_ADS.pdf	138802 0deb11d74c0d98f7f08db4046f0129bfb1a06f99	no	8
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
			Total Files Size (in bytes):	718173	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Yutaka Kobashi

Application No./Patent No.: 12436335 Filed/Issue Date: 2009-05-06

Titled: SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

138 EAST LCD ADVANCEMENTS LIMITED, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Yutaka Kobashi To: SEIKO EPSON CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 046153, Frame 0397, or for which a copy thereof is attached.

2. From: SEIKO EPSON CORPORATION To: 138 EAST LCD ADVANCEMENTS LIMITED

The document was recorded in the United States Patent and Trademark Office at
Reel 046153, Frame 0397, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Michael L. Bartholomew/	2021-05-19
Signature	Date
Michael L. Bartholomew	60225
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/436,335	05/06/2009	Yutaka Kobashi	122872.01

CONFIRMATION NO. 5191

POA ACCEPTANCE LETTER

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101



Date Mailed: 05/24/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/19/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/436,335	05/06/2009	Yutaka Kobashi	122872.01

CONFIRMATION NO. 5191

27049
OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

POWER OF ATTORNEY NOTICE



Date Mailed: 05/24/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/19/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/