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(54) Title of Invention

MANUFACTURING METHOD FOR ELEMENT-SUBSTRATE DEVICE AND
MANUFACTURING METHOD FOR ELECTRO-OPTICAL DEVICE, AND RETICLE

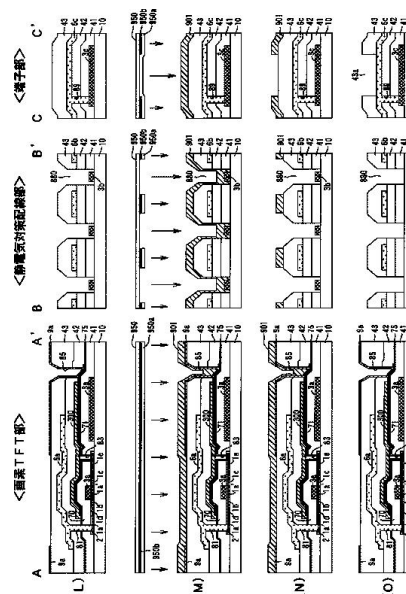
(57) Abstract

Problem

To make it possible to effectively carry out antistatic measures by forming short-circuit wiring and to effectively carry out the cutting thereof in the manufacturing of an element-substrate device.

Solution

A reticle (950), which has one light transmittance at a location opposing a cutting hole (880) formed in interlayer-insulating films (41-43) on a short-circuit wiring (3b) and has another light transmittance that is lower than the one light transmittance at a location not opposing the cutting hole, is used to cut the short-circuit wiring according to the present invention



CLAIMS

1. An element-substrate-device manufacturing method for manufacturing an element-substrate device that comprises: a plurality of pixel electrodes; a plurality of thin-film transistors connected to said plurality of pixel electrodes; and wirings connected to the plurality of transistors for driving said plurality of pixel electrodes; comprising:

a step of forming a short-circuit wiring that connects the wirings;

a step of forming an interlayer-insulating film on the short-circuit wiring;

a step of forming a cutting hole in the interlayer-insulating film, which is on the short-circuit wiring;

a step of applying a resist onto the interlayer-insulating film and onto the short-circuit wiring after the formation of the cutting hole;

a step of exposing the resist using a reticle, which has one light transmittance at a location opposing the cutting hole and has another light transmittance that is lower than the one light transmittance at a location not opposing said cutting hole and on which a light-shielding film of a prescribed pattern is formed in a region excluding the location opposing the cutting hole; and

a step of utilizing the cutting hole, after the resist has been removed, to cut the short-circuit wiring.

2. The element-substrate-device manufacturing method according to claim 1, wherein the wirings include a scan line.

3. The element-substrate-device manufacturing method according to claim 1 or 2, wherein the wirings include a data line.

4. The element-substrate-device manufacturing method according to claim 2 or 3, wherein the wirings include a signal wiring, which supplies a signal for driving at least one of a scan-line drive circuit connected to the scan line and a data-line drive circuit connected to the data line.

5. The element-substrate-device manufacturing method according to any one of claims 1–4, further comprising:

a step in which a plurality of the element-substrate devices is formed on a motherboard, the element-substrate device is formed by splitting the motherboard along a cutting line, and an inter-substrate-device short-circuit wiring, which is electrically connected to the short-circuit wiring, is formed along the cutting line that is on the motherboard; and

a step of splitting the inter-substrate-device short-circuit wiring between the element-substrate devices by carrying out the splitting along the cutting line.

6. The element-substrate-device manufacturing method according to any one of claims 1–5, further comprising: a step of forming a storage capacitor on the interlayer-insulating film after the step of forming the interlayer-insulating film and prior to the step of forming the cutting hole; and a step of forming another interlayer-insulating film on the storage capacitor.

7. The element-substrate-device manufacturing method according to any one of claims 1–6, wherein a thin film is formed at the location at which the reticle has the other light transmittance.

8. The element-substrate-device manufacturing method according to claim 7, wherein the thin film is formed on the light-shielding film on the reticle.

9. The element-substrate-device manufacturing method according to claim 7 or 8, wherein at least one portion of the thin film has the same refractive index as that of the reticle.

10. The element-substrate-device manufacturing method according to any one of claims 7–9, wherein the at least one portion of the thin film has a layered structure constituted by a plurality of different materials.

11. The element-substrate-device manufacturing method according to any one of claims 1–10, further comprising: a drive circuit, which comprises a stripe-shaped electrode instead of a pixel electrode, in which the wirings are directly connected to the stripe-shaped electrode, and which includes another thin-film transistor that is connected to the wirings and is for driving the stripe-shaped electrode.

12. An electro-optical-device manufacturing method, comprising:

a step of manufacturing the element-substrate device in accordance with the element-substrate-device manufacturing method according to any one of claims 1–11;

a step of mutually bonding the element-substrate device and an opposing substrate so that the opposing substrate opposes the element-substrate device; and

a step of sealing an electro-optical substance between the element-substrate device and the opposing substrate.

13. A reticle for use in a semiconductor process, wherein:

the reticle has one light transmittance at at least one location thereof and has another light transmittance that is greater than the one light transmittance at another location;

a light-shielding film of a prescribed pattern is formed in at least one portion of the other location; and

the light-shielding film is not formed in at least one portion of the one location.

14. The reticle according to claim 13, wherein a thin film is formed at the location having the other transmittance.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD PERTAINING TO THE INVENTION

The present invention pertains to the technical field of a manufacturing method for an element-substrate device, such as an active-matrix-substrate device, on which is formed a plurality of circuit elements and wirings and the like, and a manufacturing method for an electro-optical device, which employs said element-substrate device, as well as the technical field of a reticle that can be generally employed in a semiconductor process.

[0002]

BACKGROUND ART

An electro-optical device is known that comprises pixel electrodes arrayed in a matrix shape, and thin-film transistors (thin-film transistors, referred to as "TFTs" as appropriate below) connected respectively to said electrodes, and scan lines provided in parallel in a row (or column) direction and data lines provided in a

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row (or column) direction connected respectively to said TFTs, wherein the driving of the scan lines and the driving of the data lines are performed by a scan-line drive circuit and by a data-line drive circuit respectively, thereby enabling so-called active-matrix drive. The wirings, such as the scan lines or the data lines described above, which connect other circuit elements, such as the TFTs described above, or connect between said circuit elements, are formed by applying a semiconductor process in this kind of electro-optical device.

[0003]

Incidentally, an insulating material, such as glass, is sometimes employed for a substrate on which other circuit elements, such as the TFTs described above, are installed in this kind of electro-optical device, especially in, for example, a liquid-crystal device or the like. Meanwhile, for example, a sputtering process, a dry-etching process, or the like can be considered as the above-mentioned semiconductor processes. From these points, because "charged" particles are collided with/are deposited onto an "insulating" substrate during a sputtering process, for example, an electrostatic charge may accumulate on said substrate. If this kind of electrostatic charge accumulates, then defects arising therefrom increase the possibility of, for example, the electrostatic breakdown of other circuit elements, such as the TFTs described above.

[0004]

Accordingly, a process in which the scan lines or the data lines are formed is conventionally performed in combination with forming short-circuit wirings, which electrically connect the scan lines or the data lines, respectively. If this short-circuit wiring is formed, then the electric charge or the static electricity that has accumulated on the surface of the insulating substrate is diffused toward an outer perimeter of the substrate via said short-circuit wiring, and therefore sudden excessive electric current no longer flows through the other circuit elements or the like, such as the TFTs, via the scan lines or the data lines, and an electrostatic breakdown of said circuit elements or the like can be prevented before it happens.

[0005]

However, because the short-circuit wiring described above must be cut prior to completing the manufacturing process for the electro-optical device to allow normal operation of aforesaid electro-optical device, the applicant of the present application proposes a method of forming cutting holes on the short-circuit wiring in combination with an intermediate process thereof, and cutting prescribed locations of the short-circuit wiring via these cutting holes to separate the short-circuit wiring and the scan lines or the data lines (see Japanese Laid-open Examined Patent Publication H8-14667).

[0006]

In addition, the applicant of the present application proposes adopting, in roughly the same manner, the technique for dealing with static electricity with respect to the data-line drive circuits, the scan-line drive circuits, or the like described above by forming/cutting of the short-circuit wiring (see Japanese Laid-open Examined Patent Publication H11-95257).

[0007]

PROBLEMS TO BE SOLVED BY THE INVENTION

Nevertheless, the following kinds of problems are found in the forming and cutting of the short-circuit wiring described above. That is, in recent years, to meet the general demand, that is, to achieve increased definition, increased fineness, and a high numerical aperture for electro-optical devices, there is a trend toward a structure in which wirings and various circuit elements

and the like constituting said electro-optical device are layered on a substrate in a vertical direction via various interlayer-insulating films or the like; as a result, these various circuit elements, wirings, and the like become "highly multi-layered" so to speak. In other words, the "height" of the electro-optical device is taller compared to previously. Furthermore, as this kind of high multi-layering advances, a problem arises in which the cutting process cannot be successfully performed in the forming and cutting of the short-circuit wiring described above.

[0008]

It is assumed that the forming of the short-circuit wiring, which is in combination with the scan-line forming process, is performed at a relatively initial stage of the manufacturing process for the electro-optical device, and that the cutting of the short-circuit wiring is performed at a relatively later stage of aforesaid process, and therefore, for example, this cutting must be performed premised on the various types of interlayer-insulating films or the like that are "highly multi-layered." Here, considering furthermore that said cutting can be carried out using a photolithography method, this means that first, along with forming the cutting hole described above with respect to various types of interlayer-insulating films or the like that are highly multi-layered, a resist is applied to a bottom portion of said hole and on the uppermost layer of the interlayer-insulating films or the like, and etching is performed after exposure/development is carried out; however, as described above, if the cutting hole is formed on the interlayer-insulating films or the like that are highly multi-layered, then the depth thereof adversely becomes large, and therefore the resist existing at the bottom portion of said hole can no longer be effectively exposed. Accordingly, the resist remains at the bottom portion of said hole and, as a result, a defect arises in which the cutting of the short-circuit wiring cannot be sufficiently performed.

[0009]

To deal with this, for example, increasing the luminous exposure with respect to the resist can be considered. That is, by increasing the luminous exposure, the resist at the bottom portion can be sufficiently exposed such that sufficient light arrives as far as the bottom portion of the cutting hole. Nevertheless, such a technique adversely leads to excess luminous exposure of the resist that exists on the interlayer-insulating film or the like, and a problem such as halation or the like inevitably occurs. Here, "halation" means that the light used in the exposure is reflected or the like in unanticipated directions by a surface such as a metal layer, for example. If this kind of halation occurs, then even portions that naturally should not be exposed are exposed, and thereby this may result in, for example, a newly created problem in which control, such as control of aperture dimensions or the like of a groove, can no longer be performed accurately.

[0010]

The present invention was conceived considering the above-mentioned problems, and an object of the present invention is to provide a manufacturing method for an element-substrate device, a manufacturing method for an electro-optical device, and a reticle in which it is possible to effectively carry out antistatic measures by forming a short-circuit wiring, and to reliably carry out the cutting thereof.

[0011]

MEANS FOR SOLVING THE PROBLEMS

To solve the above-mentioned problems, an element-substrate-device manufacturing method of the present invention is an element-substrate-device manufacturing method for manufacturing an element-substrate device that comprises: a plurality of pixel electrodes; a plurality of thin-film transistors connected to said plurality of pixel electrodes respectively; and

wirings connected to the plurality of transistors for driving said plurality of pixel electrodes; comprising: a step of forming a short-circuit wiring that connects the wirings; a step of forming an interlayer-insulating film on the short-circuit wiring; a step of forming a cutting hole in the interlayer-insulating film which is on the short-circuit wiring; a step of applying a resist onto the interlayer-insulating film and onto the short-circuit wiring after the formation of the cutting hole; a step of exposing the resist using a reticle, which has one light transmittance at a location opposing the cutting hole and has another light transmittance that is lower than the one light transmittance at a location not opposing said cutting hole and on which a thin film of a prescribed pattern is formed in a region excluding the location opposing the cutting hole; and a step of utilizing the cutting hole, after the resist has been removed, to cut the short-circuit wiring.

[0012]

According to the element-substrate-device manufacturing method of the present invention, first, a short-circuit wiring is formed to create a connection between the wirings connected to the thin-film transistors, which are connected to the pixel electrodes to drive them. Here, specifically the scan lines or the data lines, for example, correspond to the wirings. Owing to the existence of this short-circuit wiring, even if there is a situation in which, for example, static electricity is generated during subsequent manufacturing processes, that static electricity can be diffused through the wirings and that short-circuit wiring; alternatively, in addition, even if an electric potential were to fluctuate at the short-circuit wiring due to the occurrence of static electricity, almost no electric potential differential would be generated among the gate, the source, and the drain that are mutually shorted in the thin-film transistor; therefore, it becomes possible, starting with the thin-film transistor described above, for example, to prevent electrostatic breakdown of other circuit elements that are provided on the substrate as necessary.

[0013]

Next, an interlayer-insulating film is then formed on this short-circuit wiring. Owing to this interlayer-insulating film, it becomes possible to ensure that no short circuit occurs among the various structural elements—such as the semiconductor layer constituting the thin-film transistor; the scan line, which includes the gate electrode that similarly constitutes the thin-film transistor; the data line, which is connected to that thin-film transistor; or electrodes constituting a storage capacitor connected to that thin-film transistor—all of which are layered and formed on the substrate, and it becomes possible to so-to-speak "multi-layer" the various above-described structural elements in a vertical direction with respect to the substrate surface. That is, according to the present invention, it is possible to support increasing the fineness and definition of the electro-optical device.

[0014]

Furthermore, next, after forming cutting holes in the short-circuit wiring and the just-mentioned interlayer-insulating film, a resist is applied on the interlayer-insulating film and on the short-circuit wiring. Here, it goes without saying that the application of the resist onto the short-circuit wiring is performed using the cutting hole. Accordingly, the application of the resist according to the present invention is performed on surfaces having a difference in the height direction so as to be applied to the bottom portion of the cutting hole, that is, on the short-circuit wiring and on

the interlayer-insulating film. Especially in the present invention, given that multi-layering is possible as described above, the depth of the cutting hole is generally deep and, accordingly, it is assumed that the above-mentioned "surfaces having a difference in the height direction" refers to surfaces that are spaced apart by distances to a substantial extent.

[0015]

Here, in particular, in the present invention, a reticle, which has one light transmittance in a location opposing the cutting hole and has another light transmittance that is lower than the one light transmittance at a location not opposing said cutting hole, is employed to expose the resist. In other words, if this kind of reticle is employed, then the luminous exposure at the location where the cutting hole exists becomes large, even if a single exposure light source having a uniform intensity is employed (that is because the exposure light is passing through the location having the one light transmittance), and the luminous exposure becomes small at the location where said hole does not exist (that is because the exposure light is passing through the location having the other light transmittance that is lower than the one light transmittance). Accordingly, according to the present invention, it becomes possible to increase the possibility that the resist at the bottom portion of the cutting hole, i.e., on the short-circuit wiring, will be sufficiently exposed, and to decrease the possibility of the occurrence of halation or the like without excessive exposure happening of the resist existing on the interlayer-insulating film. Accordingly, according to the present invention, removal of the resist can be reliably performed at the bottom portion of the cutting hole, and as a result, the cutting of the short-circuit wiring can be reliably carried out.

[0016]

Furthermore, in addition, the reticle according to the present invention has a light shielding film of a prescribed pattern formed thereon within an area that excludes the location opposing the cutting hole. This means that the existence of said light-shielding film almost completely blocks the progress of the exposure light; from a different view point, that is, said from the viewpoint of a location at which the light-shielding film exists and a location at which the light-shielding film does not exist, this has no meaning other than that normal patterning can be carried out in accordance with the reticle of the present invention. In other words, an embodiment is generally conceivable in which a location at which a light-shielding film of a prescribed pattern exists has an even lower light transmittance than the other light transmittance.

[0017]

In short, according to the present invention, at the same time that the short-circuit wiring is exposed to intense light so that the resist residue at the bottom portion of the cutting hole can be reduced, among the exposure light of normal patterning, that is, the exposure light blocked due to the light-shielding film and the exposure light passing through a location at which no light-shielding film exists and which has the other light transmittance, the luminous exposure of the latter is properly curtailed, and thereby halation prevention or the like can be achieved; as a result, high accuracy patterning can be performed.

[0018]

Note that specific values for the one light transmittance and the other light transmittance described above can change, as appropriate, in accordance with what degree of thickness the above-mentioned interlayer-insulating film may have, to what degree there is a difference in the height of the bottom portion of the cutting hole and aforesaid interlayer-insulating film, or specific circumstances such as the properties of the resist applied, the properties of the exposure light source, the performance of a stepper that utilizes aforesaid reticle to perform exposure, or the like.

[0019]

However, even if there is only a little difference between these transmittances, it becomes possible to relatively increase the luminous exposure with respect to the resist at the bottom portion of the cutting hole while relatively reducing the luminous exposure with respect to the resist existing on the interlayer-insulating film.

[0020]

In one aspect of the element-substrate device of the present invention, the wirings include a scan line.

[0021]

According to this aspect, given that the wirings include scan lines, electrically connecting by way of the short-circuit wiring includes at least said scan lines. Accordingly, according to the present aspect, it becomes possible to prevent electrostatic breakdown of the thin-film transistor due to the static electricity that passes through the scan lines.

[0022]

In another aspect of the element-substrate device of the present invention, the wirings include a data line.

[0023]

According to this aspect, given that the wirings include data lines, electrically connecting by way of the short-circuit wiring includes at least said data lines. Accordingly, according to the present aspect, it becomes possible to prevent electrostatic breakdown of the thin-film transistor due to the static electricity that passes through the data lines.

[0024]

Especially in such an aspect in which the wirings include the scan lines or the data lines, in particular, the wirings may include signal wirings that supply a signal for driving at least one of a scan-line drive circuit connected to the scan lines and a data-line drive circuit connected to the data line.

[0025]

According to this kind of configuration, the signal wirings, which supply the signals for driving the scan-line drive circuits or the data-line drive circuit, which generally include the thin-film transistor, such as a CMOS type, other circuit elements, are electrically connected by the short-circuit wiring. Accordingly, according to the present aspect, the possibility of a defect arising, such as an electrostatic breakdown, can be reduced in said scan-line drive circuits and said data-line drive circuit as well, and thereby an even more reliable element-substrate device can be manufactured.

[0026]

Another aspect of the element-substrate-device manufacturing method of the present invention further comprises: a step in which a plurality of the element-substrate devices is formed on a motherboard, the element-substrate device is formed by splitting the motherboard along a cutting line, and an inter-substrate-device short-circuit wiring, which is electrically connected to the short-circuit wiring, is formed along the cutting line that is on the motherboard; and a step of splitting the inter-substrate-device short-circuit wiring between the element-substrate devices by carrying out the splitting along the cutting line.

[0027]

According to this aspect, an inter-substrate-device short-circuit wiring, which is electrically connected to the short-circuit wiring, is formed in a state in which a plurality of aforesaid element-substrate devices is formed on a motherboard. Consequently, each element-substrate device is shorted on the motherboard, and the static electricity generated on the substrate

travels toward the inter-substrate-device short-circuit wiring through the wirings, such as the scan lines, the data lines, and the signal wiring, or the short-circuit wirings, and said static electricity is caused to be diffused to the outer perimeter of the substrate. Accordingly, according to the present aspect, in addition to what is described above, the risk of electrostatic breakdown arising in each of the various circuit elements that constitute said device is reduced.

[0028]

Furthermore, with regard to the present aspect, realizing a division at aforesaid element-substrate device for the inter-substrate-device short-circuit wiring based on carrying out division along the sectioning-plane line thereby forms individual element-substrate devices. Accordingly, there is no hindrance to an operation at each electro-optical device that will be manufactured thereafter, due to the inter-substrate-device short-circuit wiring.

[0029]

Another aspect of the element-substrate-device manufacturing method of the present invention further comprises: a step of forming a storage capacitor on the interlayer-insulating film after the step of forming the interlayer-insulating film and prior to the step of forming the cutting hole; and a step of forming another interlayer-insulating film on the storage capacitor.

[0030]

According to this aspect, other than the interlayer-insulating film, a storage capacitor and other interlayer-insulating films are separately formed on the short-circuit wiring, and therefore the depth of the cutting hole becomes deeper. Accordingly, according to the present aspect, it becomes possible to more markedly exhibit the effects of the invention, i.e., it is possible to provide sufficient exposure with respect to the resist on the short-circuit wiring while performing no excessive exposure with respect to the resist existing on other interlayer-insulating films.

[0031]

In another aspect of the element-substrate-device manufacturing method of the present invention, a thin film is formed at the location at which the reticle has the other light transmittance.

[0032]

According to this aspect, for example, because a thin film possessing light absorbency or light reflectiveness is formed at a location at which the reticle has the other light transmittance (that is, a location not opposing the cutting hole), it becomes possible to relatively easily effect manufacture at the location having the other light transmittance that is lower than the one light transmittance.

[0033]

Note that the material for the thin film can be, for example, indium tin oxide (ITO), silicon nitride (SiN_x), or the like.

[0034]

In the aspect in which a thin film is formed at the location having the other light transmittance, the thin film in particular may be formed on the light-shielding film on the reticle.

[0035]

According to this configuration, there is no need to have any special consideration with regard to the formation of the thin film (that is, for example, to form the thin film while avoiding a light-shielding-film forming location), and thereby it is possible to easily manufacture the reticle according to the present invention.

[0036]

Note that it is also possible to adopt a configuration in which the thin film is formed on the reticle, and the light-shielding film is formed on top of that.

[0037]

In the aspect where a thin film is formed on the reticle described above, or a configuration in which the thin film is formed on the light-shielding film in particular, at least one portion of the

thin film may have the same refractive index as that of the reticle.

[0038]

According to this configuration, the thin film has the same refractive index as the reticle, and thereby there is no longer a situation in which, for example, the light transmitted through the location having the one light transmittance and the light passing through the location having the other light transmittance each have a different optical path. In other words, the light advances along the same optical path in the aforesaid thin film and the reticle main body. Accordingly, the kind of situation in which exposure is performed outside of desired locations does not occur, and it is possible to manufacture the element-substrate device with high accuracy.

[0039]

Note that, for example, SiO₂ or the like can be given as an example of a material that satisfies the requirements of the present configuration.

[0040]

In addition, in the present configuration, "at least one portion of the thin film" means at least one portion of the entire surface of the thin film formed at the location having the other light transmittance. That is, more specifically, it is possible to hypothesize an embodiment wherein, at one region at a location having the other light transmittance, a thin film of the same refractive index is formed, and at another region a thin film not having that is formed, and the like. In any circumstance, it remains that even that kind of embodiment or the like is within the scope of the present invention.

[0041]

Furthermore, other than both refractive indices of the reticle and the thin film being completely the same, the "same refractive index" mentioned in the present invention means that both refractive indices are the same to the degree that the optical reflection caused by the difference between both refractive indices does not hinder, in practice, the process of exposing the resist in aforesaid manufacturing method; that degree can be determined dependent on the specifications or manufacturing conditions of the manufacturing apparatus. Furthermore, this degree of similarity may be specifically and separately defined through experimentation, experience, theory, or through simulation in accordance with the manufacturing apparatus and the manufacturing conditions that will be used in actuality.

[0042]

In addition, with regard to the aspect in which the thin film is formed on the reticle described above, the configuration in which the thin film is formed on the light-shielding film, or the configuration such that at least one portion of the thin film has the same refractive index as that of the reticle, the at least one portion of the thin film in particular may be such that it has a layered structure constituted by a plurality of different materials.

[0043]

According to this kind of configuration, it is possible to more finely establish the light transmittance on the reticle by having a layered structure in which the thin film is constituted by a plurality of different materials, thereby contributing to carrying out an accurate exposing process. Assuming a situation where the layered structure described above is at one location of said thin film, and a non-layered structure, i.e., a monolayer structure is at another location, according to the present configuration, it becomes possible, for example, for the weakest exposure to happen at aforesaid one location, an intermediate exposure to happen at aforesaid other location, and the strongest exposure to happen at the location having the one light transmittance, i.e., at the location where no thin film is formed, or the like. Of course, naturally, a situation where the thin film is a layered structure of three or more layers is also included in the scope of the present invention.

[0044]

Note that the significance of the "at least one portion" according to the present configuration is similar to what is

described above.

[0045]

In addition, the location having the other light transmittance may be composed of a film that is the same as or different from the location having the one light transmittance, and may be thickly formed.

[0046]

Another aspect of the substrate-device manufacturing method of the present invention further comprises: a drive circuit, which comprises a stripe-shaped electrode instead of a pixel electrode, in which the wirings are directly connected to the stripe-shaped electrode, and which includes another thin-film transistor that is connected to the wirings and is for driving the stripe-shaped electrode.

[0047]

According to this aspect, it is possible, for example, to prevent electrostatic breakdown of the other thin-film transistor that is included in the drive-circuit portion for the purpose of driving a stripe-shaped electrode in an element-substrate device capable of so-called passive-matrix drive.

[0048]

To solve the above-mentioned problems, an electro-optical-substance manufacturing method of the present invention comprises: a step of manufacturing the element-substrate device in accordance with the element-substrate-device manufacturing method described above (provided that the various aspects are included); a step of mutually bonding the element-substrate device and an opposing substrate so that the element-substrate device opposes the element-substrate device; and a step of sealing an electro-optical substance between the element-substrate device and the opposing substrate.

[0049]

According to the electro-optical-substance manufacturing method of the present invention, a suitable electro-optical device can be manufactured that does not include a thin-film transistor or the like that has suffered electrostatic breakdown.

[0050]

To solve the above-mentioned problems, a reticle of the present invention is a reticle for use in a semiconductor process and has one light transmittance at at least one location thereof and has another light transmittance that is greater than the one light transmittance at another location; a light-shielding film of a prescribed pattern is formed in at least one portion of the other location; and the light-shielding film is not formed in at least one portion of the one location.

[0051]

The reticle of the present invention can be suitably utilized in the element-substrate-device manufacturing method of the present invention, or in the electro-optical-device manufacturing method of the present invention, as is made clear from what is described above.

[0052]

Note that the "semiconductor process" mentioned in the present invention can be thought of, for example, with the photolithographic technique in mind.

[0053]

In one aspect of the reticle of the present invention, a thin film is formed at the location having the other transmittance.

[0054]

According to the present aspect, for example, a thin film possessing light absorbency or light reflectiveness may be formed at a location at which the reticle has the other light transmittance, and therefore it is possible to relatively easily effect manufacture at the location having the other light transmittance that is lower than the one light transmittance.

[0055]

This kind of effect and other benefits of the present invention are made clear from the embodiments, which are explained below.

[0056]

EMBODIMENTS OF THE INVENTION

Embodiments of the present invention are explained below with reference to the drawings.

[0057]

(Overall Configuration of Active-Matrix Substrate)

First, an active-matrix substrate for a liquid-crystal device is given as an embodiment of an element-substrate device of the present invention and is explained with reference to FIG. 1 to FIG. 4. Here, FIG. 1 is a block diagram schematically illustrating the configuration of a drive-circuit-integrated-type active-matrix substrate that is employed in a liquid-crystal display panel. In addition, FIG. 2 is a plan view illustrating aperture portions formed in interlayer-insulating films so as to correspond to terminals 800, 801, 802, ... illustrated in FIG. 1, and contact holes formed in the interlayer-insulating films for the purpose of achieving electrical connection between the terminals 800, 801, 802, ... and short-circuit wirings illustrated in FIG. 1; FIG. 3 is a block diagram illustrating a detailed configuration of electrostatic-protection circuits 150 and 151, which are illustrated in FIG. 1; and FIG. 4 is a plan view illustrating the details of signal wirings 72 and 73, which are illustrated in FIG. 1, and the layout mode with a first short-circuit wiring 91, which is described later in detail.

[0058]

As shown in FIG. 1, with regard to a drive-circuit-integrated-type active-matrix substrate AM, which is employed in a liquid-crystal display panel of the present embodiment, pixel electrodes 9a are configured in a matrix shape by a plurality of scan lines 3a and a plurality of data lines 6a, made to mutually intersect on a TFT-array substrate 10 constituted by an insulating material such as glass, for example, a quartz glass. Here, the scan lines 3a and the data lines 6a correspond to one example of the "wiring" of the present invention. The scan lines 3a are constituted by a doped-silicon film, and the data lines 6a are constituted by a metal film, such as an aluminum film, or an alloy film. In addition, an image-display region 10a is defined based on the entire area on which the pixel electrodes 9a are formed in the matrix shape.

[0059]

A data-line drive circuit 101, which supplies image signals to the plurality of data lines 6a respectively, is configured in an outer area (peripheral portion) of the image-display region 10a on the TFT-array substrate 10. In addition, a scan-line drive circuit 104, which supplies pixel selection scan signals to each of the scan lines 3a, is configured at both end portions of the scan lines 3a.

[0060]

The data-line drive circuit 101 comprises an X-side shift-register circuit, a sample-and-hold circuit S/H, which comprises TFTs that serve as analog switches that operate on the basis of signals output from the X-side shift-register circuit, and six image-signal lines video, and the like corresponding to, for example, image signals VID1-VID6, which are expanded to six phases. With regard to the present embodiment, the data-line drive circuit 101 is constituted by four phases of the X-side shift-register circuit, and a start signal DX, clock signals CLX1-CLX4, and inverted-clock signals CLX1 bar to CLX4 bar are supplied to the X-side shift-register circuit from the outside via terminals, and the data-line drive circuit 101 is driven in accordance with these signals. Accordingly, in the sample-and-hold circuit S/H, by having each TFT operate on the basis of a signal output from the X-side

shift-register circuit, the image signals VID1-VID6 supplied via the image-signal line video can be taken into the data lines 6a at a prescribed timing, and the same can be supplied to each pixel electrode 9a.

[0061]

Meanwhile, a start signal DY, a clock signal CLY, and an inverted-clock signal CLY bar are supplied to the scan-line drive circuits 104 from the outside via terminals, and the scan-line drive circuits 104 are driven in accordance with these signals.

[0062]

Note that while FIG. 1 illustrates a mode in which there are two scan-line drive circuits 104, which appear on the left and on the right in the drawing, and one data-line drive circuit 101 provided at the bottom in the drawing, so long as there is no problem of a delay in the scan signal supplied to the scan lines 3a, the mode may be such that there is only one scan-line drive circuit 104 provided on the left or the right in the drawing; alternatively, the mode may naturally be such that the data-line drive circuits 101 are arrayed along both sides of the image-display region 10a.

[0063]

With regard to the active-matrix substrate AM of the present embodiment, the numerous terminals 800, 801, 802, ...—which are composed of a metal film such as an aluminum film, a metal-silicide film, or a conductive film such as an ITO film and into which are input constant power supplies VDDX, VSSX, VDDY, VSSY, modulated image signals (the image signals VID1-VID6), various drive signals, etc.—are configured at a side portion, among the side portions of the TFT-array substrate 10, on the side where the data-line drive circuit 101 is configured.

[0064]

These terminal 800, 801, 802, ... are formed on a later-described second interlayer-insulating film 42, which is formed on the TFT-array substrate 10 and, nonetheless, are formed in a way in which the same are exposed to the outside by aperture portions 43a that are provided on a later-described third interlayer-insulating film 43. By utilizing these kinds of terminals 800, 801, 802, ..., i.e., pads, it is possible to connect the active-matrix substrate AM according to the present embodiment and an external terminal. Furthermore, to form later-described first to third short-circuit wirings 91-93 at the same time as the scan lines 3a as a lower layer of a first interlayer-insulating film 41, an electrical connection between a terminal-undersheet film 94, which is one portion of the first to third short-circuit wirings 91-93, and the terminals 800, 801, 802, ... is made through a contact hole 89 formed at the later-described first and second interlayer-insulating films 41 and 42, as shown in FIG. 2.

[0065]

In addition, returning to FIG. 1, the plurality of signal wirings 72 and 73, which are composed of a low-resistance metal film such as aluminum film, or a metal-silicide film, for driving the scan-line drive circuits 104 and the data-line drive circuit 101 are routed from these terminals 800, 801, 802, ..., respectively. Here, in addition to the scan lines 3a and the data lines 6a described above, the signal wirings 72 and 73 correspond to one example of the "wiring" of the present invention.

[0066]

The electrostatic-protection circuits 150 and 151 are

formed at intermediate locations of the signal wirings 72 and 73. Here, various kinds of circuits may be utilized for the electrostatic-protection circuits 150 and 151; however, the circuit illustrated in FIG. 3, for example, utilizes protection resistors 66, and P-channel TFTs 67 and N-channel TFTs 68, which are in a push-pull layout and constitute diodes between positive power supplies VDD and negative power supplies VSS, respectively. Here, and particularly in the present embodiment, what connects the first short-circuit wiring 91 to the signal wiring 72 (or 73) is between the terminal 800 (or 801, 802) and the protection resistor 66; thereby, static electricity entering from the terminal 800 (or 801, 802) or the first short-circuit wiring 91 does not reach the data-line drive circuit 101 and the scan-line drive circuit 104 unless it passes through the protection resistor 66 and the electrostatic-protection circuit 150 (or 151). With this kind of configuration, static electricity is reliably absorbed by the electrostatic-protection circuit 150 (or 151), and the data-line drive circuit 101 and the scan-line drive circuit 104 can be reliably protected.

[0067]

Returning to FIG. 1, note that the active-matrix substrate AM and the opposing substrate, which is not shown in FIG. 1, are such that counter-electrode potential LCCOM entering from outside is supplied to the opposing substrate by way of an up-down conductive material (see FIG. 12 and FIG. 13 with regard to the opposing substrate and the conductive material).

[0068]

Here, in particular with regard to the present embodiment, as illustrated in FIG. 1, the first to third short-circuit wirings 91–93 are each formed at a prescribed location. Here, the first short-circuit wiring 91 is electrically connected to all the signal wirings 72 and 73, the second short-circuit wiring 92 is electrically connected to all the scan lines 3a, and the third short-circuit wiring 93 is electrically connected to all the data lines 6a. In the present embodiment, these first to third short-circuit wirings 91–93 are all formed at the same time as the process for forming the scan lines 3a and the gate electrodes of the TFTs 30, i.e., in combination with said process (described in detail in a subsequent manufacturing method). In addition, that material is constituted by material including for example a polysilicon film, or the like.

[0069]

However, of what is mentioned above, the first and third short-circuit wirings 91 and 93 in the present embodiment have a configuration as set out below. That is, these first and third short-circuit wirings 91 and 93 are formed at the same time as the scan lines 3a and the like as described just now, and thereby the first short-circuit wiring 91 does not end up existing in the same layer as the signal wirings 72 and 73 on the TFT-array substrate 10, and the third short-circuit wiring 93 similarly does not exist in the same layer as the data lines 6a (refer to FIG. 6 which is referenced later, or the explanation regarding the later-described manufacturing method). Accordingly, in the present embodiment as shown in FIG. 4, between the first short-circuit wiring 91 and the signal wirings 72 and 73, a contact hole 403 is provided that passes through the later-described first and second interlayer-insulating films 41 and 42, are interposed in aforesaid interlayer. In addition, though not shown,

contact holes are similarly provided also between the third short-circuit wirings 93 and the data lines 6a. In so doing, both electrical connections are made for each of the combinations respectively.

[0070]

In addition, after the end of the manufacturing process for the active-matrix substrate AM (that is, at shipping at the latest) the existence of these first to third short-circuit wirings 91–93 is, on the contrary, harmful to the normal operation of the device, and therefore they are cut at the locations marked with 'x' in FIG. 1 at an appropriate stage in said manufacturing process. As is described in a subsequent manufacturing method, this cutting can be achieved through techniques such as forming a cutting hole 880 in, for example, the first, second, and third interlayer-insulating films 41, 42 and 43 on the above-mentioned first to third short-circuit wirings 91–93 and then utilizing the cutting hole 880 to etch the first to third short-circuit wirings 91–93. Furthermore, in the present embodiment, and in particular when cutting the short-circuit wiring by etching using this cutting hole 880, a distinguishing feature is that a reticle is utilized that has, respectively, a location having one light transmittance and a location having another light transmittance lower than the same; a more detailed description thereof will be made in a later-described manufacturing method.

[0071]

Next, a more detailed explanation is given, with reference to FIG. 5 and FIG. 6, of a more detailed configuration around the above-mentioned pixel electrodes 9a and of the layered structure formed on the TFT-array substrate 10, which includes the pixel electrodes 9a, the TFTs, and the like. Here, FIG. 5 is a plan view illustrating a plurality of mutually adjacent pixel groups of the TFT-array substrate, on which are formed the data lines, the scan lines, the pixel electrodes, and the like; and FIG. 6 is a cross-sectional view taken along line A-A' in FIG. 5. Note that in FIG. 6, the various layers and members are scaled differently to sizes that enable the layers and members to be recognizable.

[0072]

In FIG. 5, as already described, the plurality of transparent pixel electrodes 9a (the outlines thereof indicated by dotted-line portions 9a') is provided in a matrix shape on the TFT-array substrate of the electro-optical device, and the data lines 6a and the scan lines 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a.

[0073]

Of these, as previously described, the data lines 6a may be constituted by, for example, a metal film, such as an aluminum film, or an alloy film; however, in the present embodiment, the signal wirings 72 and 73 described above are formed at the same time as those data lines 6a in the forming process for those data lines 6a.

[0074]

In addition, the scan lines 3a are disposed so as to oppose a channel region 1a', which is indicated by an upwardly right hatched area in FIG. 5, in a semiconductor layer 1a, and the scan lines 3a function as gate electrodes. That is, at each location where the scan lines 3a and the data lines 6a intersect, a pixel-switching TFT 30 is provided opposingly disposed at the channel region 1a', where the main-line portion of the scan line 3a serves as

a gate electrode.

[0075]

The TFT 30 has a lightly doped drain (LDD) structure as shown in FIG. 6, and the structural elements therefor comprise: the scan line 3a, which functions as a gate electrode as described above; the channel region 1a' of the semiconductor layer 1a, which is composed of a polysilicon film, for example, and in which a channel is formed by an electric field from the scan line 3a; an insulating film 2, which includes a gate-insulating film that insulates the scan line 3a and the semiconductor layer 1a; and a low-density source region 1b and a low-density drain region 1c, as well as a high-density source region 1d and a high-density drain region 1e, in the semiconductor layer 1a.

[0076]

Incidentally, the above-mentioned first to third short-circuit wirings 91–93 are formed at the same time as the scan lines 3a, which include the above-mentioned gate electrodes, are formed in the forming process for the scan lines 3a, as explained in detail in a subsequent manufacturing method.

[0077]

Note that while it is preferable to have the LDD structure shown in FIG. 6, the TFT 30 may have an offset structure in which impurities are not implanted in the low-density source region 1b and the low-density drain region 1c, or may be a self-aligned type TFT in which impurities are implanted at high density, with the gate electrode, which is constituted by one portion of the scan line 3a, as a mask, to form a high-density source region and a high-density drain region in a self-aligned manner. In addition, while in the present embodiment the gate electrode of the pixel switching TFT 30 is a single gate structure in which only one gate electrode is disposed between the high-density source region 1d and the high-density drain region 1e, two or more gate electrodes may be disposed therebetween. If the TFT is configured from this kind of dual gate, or triple or more gate, then leakage current can be prevented at a junction between the channel and the source region and between the channel and the drain region, and thereby can reduce the electric current at an OFF time.

[0078]

Meanwhile, as shown in FIG. 5 and FIG. 6, a relay layer 71, which serves as a pixel-potential-side capacitor electrode that is connected to the high-density drain region 1e and the pixel electrode 9a of the TFT 30, and one portion of the capacitor line 300, which serves as a fixed-potential-side capacitor electrode, are oppositely disposed, with a dielectric film 75 interposed therebetween, to form a storage capacitor 70. This storage capacitor 70 thereby makes it possible to markedly increase the electric-potential holding characteristic in the pixel electrode 9a.

[0079]

The relay layer 71 functions as a pixel-potential-side capacitor electrode and is composed of, for example, a conductive polysilicon film. However, the relay layer 71 may be configured from a single layer film or a multilayer film that includes a metal or an alloy similarly to the later-described capacitor line 300. Other than functioning as the pixel-potential-side capacitor electrode, the relay layer 71 also has the function of relaying the connection between the pixel electrode 9a and the high-density drain region 1e of the TFT 30 via contact holes 83 and 85.

[0080]

Other than functioning as the pixel-potential-side capacitor electrode, the relay layer 71 also fulfills the function of relaying the connection between the high-density drain region 1e within the semiconductor layer 1a of the TFT 30 and the pixel

electrode 9a via the contact holes 83 and 85.

[0081]

If utilized in this manner, the relay layer 71 having an interlayer distance of at longest approximately 2,000 nm, for example, avoids the technical difficulties of connecting both with a single contact hole, while also making it possible to satisfactorily connect both with two or more contact holes that are of relatively small diameter and in series, and thereby it becomes possible to increase the pixel aperture ratio. In addition, this is also helpful in preventing penetration of the etching when forming the contact holes.

[0082]

The capacitor line 300 functions as a fixed-potential-side capacitor electrode that is constituted by a conductive film that includes, for example, a metal or an alloy. As shown in FIG. 5, this capacitor line 300 is formed overlapping with the formation area of the scan lines 3a when viewed in a plane. More specifically, the capacitor line 300 comprises: protruding portions that protrude respectively upward in the drawing along the data lines 6a from each location at which the main-line portion, which extend along the scan lines 3a, and the data lines 6a intersect; and neck portions that are slightly bent at locations corresponding to the contact holes 85. Among these, the protruding portions contribute to increasing the formation area for the storage capacitor 70 by utilizing the regions on the scan lines 3a and the regions below the data lines 6a.

[0083]

This kind of capacitor line 300 is preferably composed of a conductive, light-shielding film that contains a high-melting-point metal, and other than functioning as the fixed-potential-side capacitor electrode of the storage capacitor 70, also functions as a light-shielding layer that shields the TFT 30 from incident light at the upper side of the TFT 30.

[0084]

In addition, the capacitor line 300 preferably extends from the pixel-display area 10a, in which the pixel electrodes 9a are disposed, to therearound, is electrically connected to the constant-potential source, and is taken as a fixed potential. The constant-potential sources of the positive power supply and the negative power supply supplied to the data-line drive circuit 101 may serve as such a constant-potential source, and it is no problem for it to be the constant potential that is supplied to the counter electrode of the opposing substrate.

[0085]

The dielectric film 75 is composed of: a silicon-oxide film, such as a high-temperature oxide (HTO) film or a low-temperature oxide (LTO) film; a silicon-nitride film; or the like that is relatively thin, for example, having a film thickness of approximately 5–200 nm. From the viewpoint of enlarging the storage capacitor 70, the thinner the dielectric film 75, the better, as long as sufficient reliability of the film is obtained.

[0086]

Other than what is mentioned above, in FIG. 5 and FIG. 6, a lower-side, light-shielding film 11a is provided at the lower side of the TFT 30. The lower-side, light-shielding film 11a is patterned into a lattice shape and thereby defines the aperture region of each pixel. In addition, the aperture region is also defined by the data lines 6a extending in the vertical direction in FIG. 5, and the capacitor lines 300 extending in the horizontal direction in FIG. 5, which are formed intersecting each other.

[0087]

Note that similar to the situation with the capacitor line 300 previously described, the lower-side, light-shielding film 11a as well may be extended from the pixel-display region and therearound and be connected to the constant-potential source to avoid the potential fluctuation thereof bringing about adverse effects in the TFT 30.

[0088]

In addition, a base-insulating film 12 is provided under the TFT 30. Other than functioning as an interlayer insulating the TFT 30 from the lower-side, light-shielding film 11a, the base-insulating film 12 is formed on the entire surface of the TFT-array substrate 10, and thereby has the function of preventing changes in the characteristics of the pixel-switching TFT 30, such as contamination remaining after roughening at the time of surface polishing, or rinsing the TFT-array substrate 10.

[0089]

The first interlayer-insulating film 41, in which are formed the contact hole 81 that leads to the high-density source region 1d and the contact hole 83 that leads to the high-density drain region 1e, is formed on the scan lines 3a.

[0090]

The relay layer 71 and the capacitor line 300 are formed on the first interlayer-insulating film 41, and on these are formed a second interlayer-insulating film 42, in which are formed the contact hole 81 that leads to the high-density source region 1d and the contact hole 85 that leads to the relay layer 71.

[0091]

Incidentally, in the present embodiment, in addition to the contact holes 81, 83 and 85 just described, the contact hole 403, which is for achieving electrical connection between the first short-circuit wiring 91 and the signal wirings 72 and 73 described above, or a contact hole, which is for achieving electrical connection between the third short-circuit wiring 93 and the data lines 6a, is formed (not shown in FIG. 6) in the first and second interlayer-insulating films 41 and 42.

[0092]

Note that in the present embodiment, sintering may be performed on the first interlayer-insulating film 41 at approximately 1,000°C to activate the ions injected into the polysilicon film, which constitutes the semiconductor layer 1a or the scan lines 3a. Whereas, not performing this kind of sintering on the second interlayer-insulating film 42 may mitigate stress that could arise in the vicinity of the interface of the capacitor line 300.

[0093]

The data lines 6a are formed on the second interlayer-insulating film 42, and thereupon the third interlayer-insulating film 43 is formed, in which the contact hole 85 leading to the relay layer 71 is formed.

[0094]

The surface of the third interlayer-insulating film 43 is flattened by a chemical-mechanical polishing (CMP) process or the like to reduce alignment defects in a liquid-crystal layer 50 that may arise from differences in height due to the various wirings and elements existing therebelow. However, instead of or in addition to performing this kind of flattening process on the third interlayer-insulating film 43, the flattening process may be performed by digging a groove in at least one of the TFT-array substrate 10, the base-insulating film 12, the first interlayer-insulating film 41, and the second interlayer-insulating film 42 to embed wirings, such as the data lines 6a, the TFTs 30, or the like.

[0095]

Incidentally, in the present embodiment, in addition to the contact holes 81, 83, 85, and 403 described above, the cutting hole 880 for cutting the first to third short-circuit wirings 91–93 described above is formed in the above-mentioned first, second, and third interlayer-insulating films 41, 42, and 43; more details are

given with regard to this point in a subsequent manufacturing method.

[0096]

Moreover, other than what is mentioned above, the pixel electrodes 9a are provided on the TFT-array substrate 10 as shown in FIG. 6, and on the upper side thereof, an alignment film 16 is also provided, for which a prescribed alignment process, such as a rubbing process, is performed. The pixel electrodes 9a are composed of a transparent conductive film, such as ITO, for example. In addition, the alignment film 16 is composed of an organic film, such as a polyimide film, for example.

[0097]

In the present embodiment, as described above, the semiconductor layer 1a constituting the TFT 30, the insulating film 2, and the scan line 3a, which includes the gate electrode constituting that TFT 30; additionally, the relay layer 71, the capacitor line 300, and the dielectric film 75 constituting the storage capacitor 70; furthermore, the various interlayer-insulating films 41, 42, and 43; and the like are formed by being layered on the TFT-array substrate 10—in other words, they are "highly multi-layered" so to speak. From this, according to the electro-optical device as in the present embodiment, it becomes possible to support a reduced size and an increased definition thereof. Nevertheless, on the other hand, the distance in the vertical direction in the drawing is relatively long from the upper surface, in the drawing, of the third interlayer-insulating film 43, to which the pixel electrodes 9a are provided, to the layer in which the scan lines 3a are located.

[0098]

Next, the configuration of a motherboard provided with a plurality of the active-matrix devices AM of the type described above is described with reference to FIG. 7 and FIG. 8. Here, FIG. 7 is a plan view illustrating the appearance of laying out and forming the active-matrix substrate illustrated in FIG. 1 on the motherboard; and FIG. 8 is an enlarged plan view illustrating an area A on the motherboard illustrated in FIG. 7.

[0099]

In FIG. 7 and FIG. 8, an inter-substrate-device short-circuit wiring 99, which is electrically connected to and between the above-mentioned first to third short-circuit wirings 91–93 provided on the outer-perimeter side of each active-matrix substrate AM, is provided on a motherboard MM along a cutting line on said motherboard MM (indicated as a dotted line in the drawing). The existence of this inter-substrate-device short-circuit wiring 99 makes it possible for the electric charge of the static electricity—which, after flowing through the signal wirings 72 and 73, the scan lines 3a, the data lines 6a, or the like, further flows through the first to third short-circuit wirings 91–93—to be diffused to the outer perimeter of the substrate. In addition, in the present embodiment, the inter-substrate-device short-circuit wiring 99 in particular, which is electrically connected with the first to third short-circuit wirings 91–93, is configured such that adjacent active-matrix substrates AM are connected to each other until the final process and, at the time of cutting the motherboard MM, the active-matrix substrates AM are cut and separated from each other. If such a configuration is adopted, then it ensures a state in which the inter-substrate-device short-circuit wiring 99 is in a state of being dispersed over a wide area; therefore, the effects of the present invention, i.e., that concentration of the electric charge can be prevented and that the danger of electrostatic breakdown of other circuit elements, such as the TFT 30 formed on the substrate, can be avoided, can be even more reliably exhibited.

[0100]

(Manufacturing Method of Active-Matrix Substrate)

A description is given below with regard to a manufacturing method for the kind of active-matrix substrate AM described above, with reference to FIG. 9 to FIG. 11. Here, FIG. 9 to FIG. 11 are process cross-sectional views illustrating a manufacturing method of the active-matrix substrate; in each of the drawings, the left portion is a cross section taken along line A-A' in FIG. 5 (the cross section including the TFT 30), the center portion is a cross section taken along line B-B' in FIG. 4 (the cross section including the location marked with "x" indicated in FIG. 1 where the cutting of the short-circuit wiring is performed), and the right portion is a cross section taken along line C-C' in FIG. 2 (the cross section of a terminal portion in which the terminals 800, 801, 802, ... are formed). Note that below, the portions in FIG. 9 to FIG. 11 corresponding to the left portion, the center portion, and the right portion are called, respectively, the pixel TFT portion, the antistatic-wiring portion, and the terminal portion.

[0101]

First, as shown in FIG. 9(A), a semiconductor film 1 composed of a polysilicon film of thickness approximately 20 nm to approximately 200 nm, and preferably approximately 100 nm is formed by a low-pressure CVD method or the like either directly on the surface of the transparent TFT-array substrate 10—which is composed of a glass substrate, e.g., an alkali-free glass, quartz, or the like—on the entire surface of a base-insulating film formed on the surface of the TFT-array substrate 10, and thereafter, as shown in FIG. 9(B), patterning that by using a photolithographic technique to form the island-shaped semiconductor layer 1a (active layer) on the side with the pixel TFT portion. At this time, the semiconductor film 1 is completely removed from the side with the antistatic-wiring portion and the terminal portion. With regard to the aforementioned formation of the semiconductor film, a method may be employed in which: after an amorphous silicon film is deposited, a polysilicon film is formed by performing a heat treatment for 1 hr to 72 hrs and preferably for 4 hrs to 6 hrs at a temperature of 500°C–700°C; after depositing a polysilicon film, silicon is implanted; and, after making it amorphous, recrystallization is performed by a heat treatment to form the polysilicon film. Note that the cross-sectional views in FIG. 9 to FIG. 11 are different from the cross-sectional view shown in FIG. 6, and a lower-side, light-shielding film 11 and the base-insulating film 12 are not shown, in order to provide a simplified description.

[0102]

Next, as shown in FIG. 9(C), a gate oxide film 2 composed of a silicon-oxide film of a thickness of approximately 50 nm to approximately 150 nm is formed on the surface of the semiconductor layer 1a by a thermal-oxidizing method or the like. Alternatively, after forming a thermally oxidized film of approximately 5 nm to approximately 100 nm, and preferably of 30 nm, a silicon-oxide film of approximately 10 nm to approximately 100 nm, and preferably of 50 nm may be deposited over the entire surface by a CVD method or the like, thereby forming the gate insulating film 2. In addition, a silicon-nitride film may be employed to further increase the withstand voltage of the gate-insulating film 2.

[0103]

Next, as shown in FIG. 9(D), after the polysilicon film 3, which is for forming the gate electrodes and the like, is formed on the entire surface of the TFT-array substrate 10, phosphorus is thermally diffused therein to make the polysilicon film 3 conductive. In addition, a doped-silicon film, into which the phosphorus was introduced at the same time as the polysilicon film 3 was formed, may be employed. Next, a photolithographic technique may be employed for patterning the polysilicon film 3 as

shown in FIG. 9(E), to form the scan lines 3a, which include the gate electrodes, on the side with the pixel TFT portion. At the time of this patterning, the polysilicon film is left on the side with the antistatic-wiring portion and the terminal portion to serve as a short-circuit wiring 3b (corresponding to the first to third short-circuit wirings 91–93 described above) and a terminal-undersheet film 3c (corresponding to the terminal-undersheet film 94 described above). That is, in the present embodiment, the first to third short-circuit wirings 91–93 are formed at the same time as the process for forming the scan lines 3a, which include the gate electrode of the TFT 30, i.e., it is formed in combination with that process.

[0104]

Next, as shown in FIG. 9(F), low-density impurity ions 979 (phosphorus ions) are implanted at a dose of approximately $0.1 \times 10^{13}/\text{cm}^2$ to approximately $10 \times 10^{13}/\text{cm}^2$ on the side with the pixel TFT portion and the N-channel TFT portion of the drive circuit, using the gate electrode 3a as a mask, and a low-density source region 1b, and a low-density drain region 1c are formed in a self-aligned manner with respect to the gate electrode 3a on the side with the pixel TFT portion. Here, a portion where the impurity ions 979 are not introduced because it is located directly beneath the gate electrode 3a remains as the semiconductor layer 1a to become a channel region. In this manner, at the time of performing the ion implantation, impurities are introduced also into the polysilicon film formed to serve as the gate electrode 3a, the short-circuit wiring 3b, and the terminal-undersheet film 3c, and therefore these parts are made more conductive.

[0105]

Next, as shown in FIG. 10(G), with regard to the pixel TFT portion, a resist mask 959 of a width wider than the gate electrode 3a is formed, and high density impurity ions 980 (phosphorus ions) are implanted at a dose of approximately $0.1 \times 10^{15}/\text{cm}^2$ to approximately $10 \times 10^{15}/\text{cm}^2$ to form the high-density source region 1d and the high-density drain region 1e.

[0106]

Instead of these impurity-introducing processes, in the state in which the resist mask 959 of a wider width than the gate electrode 3a has been formed without implanting the low-density impurities, the high-density impurities (phosphorus ions) may be implanted to form a source region and a drain region of an offset structure. In addition, of course, high-density impurities (phosphorus ions) may be implanted on the gate electrode 3a to form a source region and a drain region of a self-aligned structure.

[0107]

In addition, while omitted from the drawings, to form the P-channel TFT portion of a peripheral-drive circuit, the aforementioned pixel portion and the N-channel TFT portion may be protected by being covered by a resist, and boron ions may be implanted at a dose of approximately $0.1 \times 10^{15}/\text{cm}^2$ to approximately $10 \times 10^{15}/\text{cm}^2$, using the gate electrode as a mask, to form the source and drain regions of the P-channel in a self-aligned manner. Note that, after low-density impurities (boron ions) are introduced at a dose of approximately $0.1 \times 10^{13}/\text{cm}^2$ to approximately $10 \times 10^{13}/\text{cm}^2$, using the gate electrode as a mask, to form a low-density region in the polysilicon film, a mask with a wider width than the gate electrode may be formed and high-density impurities (boron ions) may be implanted at a dose of approximately $0.1 \times 10^{15}/\text{cm}^2$ to approximately $10 \times 10^{15}/\text{cm}^2$ to form

the source region and the drain region of a lightly doped drain structure (LDD structure) similarly to when the N-channel TFT portion is formed. In addition, in the state in which a mask having a wider width than the gate electrode has been formed without implanting the low-density impurities, the high-density impurities (phosphorus ions) may be implanted to form a source region and a drain region of an offset structure. These ion-implanting processes make it possible to make it a CMOS, and it becomes possible to integrate the peripheral-drive circuits with the same substrate.

[0108]

Next, as shown in FIG. 10(H), the first interlayer-insulating film 41—which is composed of: a silicate-glass film made of non-silicate glass (NSG), phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), or the like; a silicon-nitride film; or a silicon-oxide film—is formed on the surface side of the gate electrode 3a, the short-circuit wiring 3b, and the terminal-undersheet film 3c by a normal pressure or low-pressure CVD method, or the like that employs, for example, a tetraethyl orthosilicate (TEOS) gas, a tetraethylborate (TEB) gas, or a tetramethyl oxyphosphate (TMOP) gas, or the like. The thickness thereof is on the order of approximately 500 nm to approximately 1,500 nm, for example.

[0109]

Next, as shown in FIG. 10(I), after forming the contact hole 83 so it reaches the high-density drain region 1e of the TFT 30 by dry etching, such as reactive-ion etching or reactive-ion-beam etching, a metal film made of Pt or the like is formed, on the first interlayer-insulating film 41, with a film thickness of approximately 100–500 nm by sputtering. Furthermore, the relay layer 71 having a prescribed pattern is formed by photolithography and etching. Then, the dielectric film 75 composed of a TaOx film or the like is formed on the relay layer 71 by a plasma CVD method or the like. This dielectric film 75 may be configured from either a monolayer film or a multilayer film, similarly to the situation with the insulating film 2, and generally can be formed by various well-known techniques used in the formation of gate-insulating films of TFTs. Furthermore, the thinner the dielectric film 75, the larger the storage capacitor 70, and therefore, ultimately, it is advantageous to form the same as a very thin insulating film of film thickness 50 nm or less under the condition that no defects arise such as film cracking or the like. Then, a metal film, made of Al or the like, having a film thickness on the order of approximately 100–500 nm is formed on the dielectric film 75 by sputtering. Furthermore, the capacitor line 300 having a prescribed pattern is formed by photolithography and etching. With this capacitor line 300, and the relay layer 71 and the dielectric film 75 previously described, the storage capacitor 70 is thereby completed. Note that, at this time, at the antistatic-wiring portion and the terminal portion, the relay layer 71 and the capacitor line 300 described above are removed by photolithography and etching from above the first interlayer-insulating film 41 when patterning to a prescribed pattern.

[0110]

Next, as shown in FIG. 10(J), the second interlayer-

insulating film 42 composed of a silicate-glass film, made of NSG, PSG, BSG, BPSG, or the like, a silicon-nitride film, a silicon-oxide film, or the like is formed on the first interlayer-insulating film 41 and the capacitor line 300 described above by, for example, a normal-pressure or a low-pressure CVD method that employs TEOS gas or the like. The film thickness thereof is, for example, on the order of approximately 500–1,500 nm. Then, the contact holes 81 and 89 are formed at a portion corresponding to the source region 1d of the first interlayer-insulating film 41 on the side with the pixel TFT portion, and at a portion corresponding to the terminal-undersheet film 3c of the first and second interlayer-insulating films 41 and 42 on the side with the terminal portion, respectively, by employing a photolithographic technique. Then, for example, an aluminum film is formed by a sputtering method or the like to configure the source electrode on the surface side of the second interlayer-insulating film 42. In addition to a metal film made of aluminum or the like, a metal-silicide film or a metal-alloy film may also be employed. Thereafter, a photolithographic technique is employed in patterning the aluminum film, and a source electrode is formed as one portion of the data line 6a in the pixel TFT portion. In all, a signal wiring 6b (corresponding to the signal wirings 72 and 73 described above) is formed on the antistatic-wiring portion, and a terminal 6c (corresponding to the terminals 800, 801, 802, ... described above) is formed on the side with the terminal portion.

[0111]

By utilizing these processes in FIG. 10(J), a wiring connection is made between the first and third short-circuit wirings 91, 93, described with reference to FIG. 4, and the signal wirings 72, 73 and the data lines 6a.

[0112]

Next, as shown in FIG. 10(K), the third interlayer-insulating film 43 composed of a silicate-glass film made of NSG, PSG, BSG, BPSG, or the like, a silicon-nitride film, a silicon-oxide film, or the like is formed on the surface side of the source electrode 6a, the signal wiring 6b, and the terminal 6c by, for example, a normal-pressure or a low-pressure CVD method that employs TEOS gas or the like. The film thickness thereof is, for example, on the order of approximately 500–1,500 nm. Then, on the side with the pixel TFT portion, the contact hole 85 is formed, such that it reaches the aforementioned relay layer 71 within the third interlayer-insulating film 43 and the second interlayer-insulating film 42, by employing a photolithographic technique and a dry-etching method and the like. In all, the cutting hole 880 is formed on the short-circuit wiring 3b (corresponding to the first to third short-circuit wirings 91–93 described above) on the side with the antistatic-wiring portion. Furthermore, in the present embodiment, as can be understood from viewing FIG. 10(K), given that this cutting hole 880 in particular is formed after the formation of the storage capacitor 70—which is composed of at least three layers, i.e., the relay layer 71, the dielectric film 75, and the capacitor line 300—the third interlayer-insulating film 43, and the like, it can be understood that the distance (i.e., the depth of that cutting hole 880) from that aperture portion to the short-circuit wiring 3b becomes large.

[0113]

Next, as shown in FIG. 11(L), after forming an ITO film with a thickness of approximately 40 nm to approximately 200 nm on the surface side of the third interlayer-insulating film 43 by a sputtering method, the ITO film is patterned using a photolithographic technique to form the pixel electrode 9a in the pixel TFT portion. This pixel electrode 9a is, as shown in the

drawing, connected to the high-density drain region 1e of the TFT 30 via the contact hole 85, the relay layer 71, and the contact hole 83. In addition, when forming this pixel electrode 9a, the ITO film is completely removed from the antistatic-wiring portion and the terminal portion. Here, the pixel electrode 9a is not limited to an ITO film, and it is possible to also use a transparent electrode material composed of a high-melting-point metal oxide or the like, such as an SnOx film or a ZnOx film; if these materials are used, then, in practice, step coverage within the contact hole can be tolerated.

[0114]

Next, as shown in FIG. 11(M), a resist 901 is applied to the surface side of the third interlayer-insulating film 43. Generally, this resist 901 is formed thickly on the third interlayer-insulating film 43 and on the short-circuit wiring 3b, that is, at the bottom portion of the cutting hole 880, and is formed thinly at the sidewalls of said cutting hole 880 as appears, for example, in the drawings illustrating the antistatic-wiring portion in FIG. 11(M).

[0115]

Furthermore, as also shown in FIG. 11(M), in the present embodiment in particular, a reticle 950 is employed, which has one light transmittance at a location opposing the cutting hole 880 and has another light transmittance that is lower than the one light transmittance at a location not opposing said cutting hole 880, to expose the resist 901. That is, in the present embodiment, this exposure is performed so that, for example, while a single exposure light source having a uniform intensity is employed, the luminous exposure at the location where the cutting hole 880 exists becomes large and the luminous exposure where that does not exist becomes small.

[0116]

In the present embodiment, to achieve the reticle 950, which has the different light transmittances such as mentioned above, more specifically, a thin film 950a is formed on one portion of said reticle 950, for example, as shown in FIG. 11(M). This thin film 950a is assumed to be one composed of ITO, silicon nitride (SiNx), or the like used as the material for the above-mentioned pixel electrodes 9a, for example, or SiO₂ or the like, for example, whose refractive index is substantially the same as that of the reticle 950. In addition, the thickness thereof may be approximately 100 nm, for example. The existence of this kind of thin film 950a reduces the light transmittance at the location in which said thin film 950a is formed compared with the location in which said thin film 950a is not formed, and accordingly the luminous exposure can be made small. By utilizing the thin film 950a, whose refractive index is the same as that of the main body of the reticle 950 in particular, there is no longer the situation where the light transmitted through the location having the one light transmittance and the light transmitted through the location having the other light transmittance each have a different optical path. That is, the light advances taking the same optical path in said thin film 950a and the main body of the reticle 950. Accordingly, the kind of situation where exposure happens outside of desired locations does not occur, and therefore it is possible to perform highly accurate manufacturing of the element-substrate device.

[0117]

Meanwhile, as shown in FIG. 11(M), a generally seen light-shielding portion should be configured on the reticle 950, and

a light-shielding film 950b constituted of Cr or the like, for example, is formed on the reticle 950 of the present embodiment. That is, the present embodiment has a structure in which the thin film 950a and the light-shielding film 950b are layered at a prescribed location on the reticle 950.

[0118]

From this, assuming the layered structure of the above-mentioned thin film 950a and the light-shielding film 950b at the location of the resist 901 where no window opening is needed, and assuming, as shown in the right part of FIG. 11(M), a mode in which, to form the aperture portion 43a (see FIG. 2) to be exposed as the terminal 6c, only the thin film 950a is formed and the light-shielding film 950b is not formed at the location at which window opening of the resist 901 is required, and the like, a suitable exposing process can be carried out. In short, if done in this manner, the light transmittance can be more finely established, contributing to carrying out a more accurate exposing process.

[0119]

In addition, in addition to such a configuration, the thin film 950a itself may also be one that has a layered structure constituted from a plurality of differing materials. It goes without saying that, in this situation, the light transmittance can be even more finely controlled.

[0120]

Note that, as more specific exposure conditions, for example, an i-line or the like of an optical wavelength of 365 nm should be used for the light emitted from the exposure light source, and, in the reticle 950 according to the present embodiment, the portion where the thin film 950a is not formed should have a light transmittance of approximately 100%, and the portion where only the thin film 950a is formed should have a light transmittance of, in general, approximately 50%–85%. In this situation, even more specifically, if the energy of the light emitted from the exposure light source is taken as approximately 2,200 J/m², then, at the location directly below where the thin film 950a is not formed, an exposure should be performed with an energy of approximately 2,200 J/m², and at the location directly below where only the thin film 950a is formed, an exposure should be performed with an energy of approximately 1,600 J/m².

[0121]

Thus, according to the present embodiment, utilizing the reticle 950 configured as described above, by carrying out the exposing process for the resist 901, it becomes possible to sufficiently expose the resist 901 on the bottom portion of the cutting hole 880, i.e., on the short-circuit wiring 3b, and to decrease the possibility of the occurrence of halation or the like without excessive exposure of the resist 901 existing on the third interlayer-insulating film 43. As a result, as shown in FIG. 11(N), the development and removal of the resist 901 at the bottom portion of the cutting hole 880 are performed substantially completely, and the mode in which the resist 901 remains on the third interlayer-insulating film 43 suitably emerges. Additionally, creating an area on the reticle 950 on which only the thin film 950a exists makes it possible to more reliably perform window opening of the reticle 901 or the like related to the formation of the aperture portion 43a for exposing the terminal 6c.

[0122]

Note that, in the description above, with regard to the exposure of the resist 901 at the antistatic-wiring portion, i.e., when carrying out window opening at a location where the cutting hole 880 exists, in the end, aforesaid window-opening portion is preferably made larger than the aperture portion of the cutting hole 880. In addition, in relation to this, with regard to the cutting hole 880, it is preferable that the same is formed in advance so that the dimension of the upper-end aperture thereof is made wider than the lower-end dimension (refer to FIG. 11(N) with regard to either of these). A wet-etching-based method is one of the most suitable methods for satisfying the requirement of the latter.

[0123]

Having gone through the above kinds of processes, etching is performed through the resist 901, and, as shown in FIG. 11(O), the terminal 6c is exposed from the aperture portion 43a at the terminal portion. In all, the short-circuit wiring 3b is cut at the side with the antistatic-wiring portion, and each wiring is separated by this cutting part 19.

[0124]

Thus, the short-circuit wiring 3b is cut in the final process of the manufacturing process, and therefore it becomes possible to prevent the static electricity, which would occur in many of the processes prior to that, from imparting adverse effects to the various circuit elements formed on the substrate.

[0125]

Thus, the manufacturing of the active-matrix substrate AM is generally complete; however, it is possible for said substrates AM to be formed all at once or for a plurality to be formed at the same time on the motherboard MM, as shown in FIG. 7 and FIG. 8. In such a situation, a state is created in which the first to third short-circuit wirings 91–93 and the inter-substrate-device short-circuit wiring 99 described above are electrically connected. Specifically, when forming each of the short-circuit wirings 91–93 (i.e., when forming the scan lines 3a), the electrical connection should be made at the same time by forming the inter-substrate-device short-circuit wiring 99, or, depending on the situation, by separately forming a contact hole that connects both of them.

[0126]

With the existence of this inter-substrate-device short-circuit wiring 99, the electric charge or the like generated on the substrate is thereby guided to the outer perimeter of said substrate, and therefore, the risk of electrostatic breakdown of the TFT other circuit elements on the substrate is much further reduced.

[0127]

As explained above, according to the present embodiment, first, regarding the scan lines 3a, the data lines 6a, and the signal wirings 72 and 73 connected to the data-line drive circuit 101 and the scan-line drive circuit 104, respectively, given that most of the processes related to manufacturing the active-matrix substrate are performed in a state in which the first to third short-circuit wirings 91–93 exist, even if static electricity is generated, or an electric charge accumulates on the substrate surface, it is possible for such an electric charge to be diffused via the first to third short-circuit wirings 91–93. Accordingly, an excessive electric current no longer suddenly flows in the scan lines 3a, the data lines 6a, and the data-line drive circuit 101 and the data-line drive circuit 104; for this reason, the TFT 30 and

other various circuit elements formed on the active-matrix substrate AM according to the present embodiment can effectively prevent electrostatic breakdown and the like.

[0128]

Especially in the present embodiment, the reticle 950, which has one light transmittance at the location opposing the cutting hole 880 formed for cutting the above-mentioned first to third short-circuit wirings 91–93 and has another light transmittance that is lower than the one light transmittance at a location not opposing said cutting hole 880, is employed to expose the resist 901, and thereby it becomes possible to effectively develop and remove the resist 901 applied to the bottom portion of the cutting hole 880 having a relatively deep depth, and special mention can be made that the resist on the third interlayer-insulating film 43 is not excessively exposed. That is, using this kind of reticle 950 and carrying out exposure that employs said reticle 950 makes it possible to reliably perform the cutting of the first to third short-circuit wirings 91–93, and for the most part stops a situation that would lead to a needless short-circuit fault thereafter.

[0129]

In addition, in the present embodiment, during the forming process for the TFT 30, the forming process for the various wirings, the forming process for each of the terminals 800, 801, 802, ..., or the like, the formation of the first to third short-circuit wirings 91–93, and the formation of the cutting hole 880, as well as the process related to cutting each of the short-circuit wirings 91–93, which utilizes said hole 880, can be carried out at the same time, and therefore it is possible to reduce the manufacturing cost commensurately.

[0130]

(Electro-Optical Device and Manufacturing Method for Electro-Optical Device)

The electro-optical device and the manufacturing method therefor are described below for a situation in which the active-matrix substrate AM manufactured as described above is employed as one of the substrates in a pair that constitutes aforesaid electro-optical device.

[0131]

First, the manufacturing of the electro-optical device is described with reference to FIG. 12 and FIG. 13. Note that FIG. 12 is a plan view of a TFT-array substrate and each structural element formed thereon, viewed from the opposing substrate 20 side; and FIG. 13 is a cross-sectional view taken along line H-H' in FIG. 12.

[0132]

In FIG. 12 and FIG. 13, the TFT-array substrate 10 and the opposing substrate 20 are opposingly disposed in the electro-optical device according to the present embodiment, and the liquid-crystal layer 50 is sealed between these substrates 10 and 20, and both of the substrates 10 and 20 are mutually bonded by a sealing material 52 provided in a seal region located around the image-display region 10a. Note that the sealing material 52 may be composed of, for example, an ultraviolet-light setting resin, a thermosetting resin, or the like and set by ultraviolet rays, heating, or the like to paste both of the substrates together.

[0133]

In addition, if the liquid-crystal device according to the present embodiment is for use as a projector and is a liquid-crystal device of a small form factor for providing an enlarged display, then a gap material (spacer), such as glass fiber or glass beads, is distributed within this sealing material 52 to make the distance between both of the substrates (the inter-substrate gap) a prescribed value. Alternatively, if aforesaid liquid-crystal display is a liquid-crystal display of a large form factor for unity-magnification

display, as with a liquid-crystal display or a liquid-crystal television, then such a gap material should be included in the liquid-crystal layer 50.

[0134]

Furthermore, a light-shielding film 53, which acts as a picture frame defining the periphery of the image-display region 10a, is provided on the TFT-array substrate 10 on the opposing substrate 20 side, side-by-side on the inner side of the aforementioned sealing material 52. However, one portion or the entire portion of the picture-frame light-shielding film 53 may be provided as an internal light-shielding film on the TFT-array substrate 10 side.

[0135]

In the region on the outer side of the sealing material 52, as already mentioned in the description that referenced FIG. 1, the data-line drive circuit 101, which drives the data lines 6a by supplying said data lines 6a with image signals at prescribed timings, and an external-circuit connection terminal 102 are provided along one side of the TFT-array substrate 10; and the scan-line drive circuits 104, which drive the scan lines 3a by supplying scan signals to the scan lines 3a at prescribed timings, are provided along two sides adjacent to the one side. Moreover, on the remaining one side of the TFT-array substrate 10, a plurality of wirings 105 is provided for connection between the scan-line drive circuits 104 provided on both sides of the image-display region 10a. In addition, a conductive material 106 for electrical conduction between the TFT-array substrate 10 and the opposing substrate 20 is provided in at least one location of the corner portions of the opposing substrate 20.

[0136]

On one hand, in FIG. 13, on the TFT-array substrate 10, an alignment layer is formed on the pixel electrode 9a after the pixel switching TFT and the wirings, such as the scan lines and the data lines, have been formed. On the other hand, on the opposing substrate 20, in addition to a counter electrode 21, an alignment layer is formed on the uppermost layer. In addition, the liquid-crystal layer 50 is composed of, for example, liquid crystal in which one type or multiple types of nematic liquid crystal have been mixed together, and there is a prescribed alignment state between this pair of alignment layers.

[0137]

Note that, in addition to the data-line drive circuit 101, the scan-line drive circuits 104, and the like, a precharging circuit, which is for supplying a precharging signal of a prescribed voltage level respectively to the plurality of data lines 6a ahead of the image signals, and a testing circuit, which is for testing the quality of and for testing for defects in aforesaid electro-optical device partway through manufacturing or at shipping, may be formed on the TFT-array substrate 10.

[0138]

This kind of electro-optical device can be manufactured by going through the kind of processes shown, for example, in the flow chart in FIG. 14. Note that the explanation here is based on a mode in which a plurality of the above-mentioned active-matrix substrates is formed on the motherboard MM as described above.

[0139]

First, undergoing each process described with reference to FIG. 9 to FIG. 11, the manufacturing of the individual active-matrix substrates AM on the motherboard MM is completed (step S11). Note that, though not mentioned in the manufacturing method described above, after applying a coating liquid for the polyimide alignment layer, the alignment film 16 is formed on the pixel electrodes 9a by performing a rubbing process or the like in a

prescribed direction so as to have a prescribed pretilt angle (see FIG. 6).

[0140]

Meanwhile, a plurality of opposing substrates is formed on a separate motherboard in parallel with the manufacturing of the above-mentioned active-matrix substrate AM. Specifically, first, a glass substrate or the like is prepared as the motherboard (step S51), and the light-shielding film serving as the picture frame is formed by passing through photolithography and etching after sputtering, for example, metal chrome (step S52). Note that these light-shielding films do not need to be conductive and, in addition to metal materials such as Cr, Ni, and Al, may be formed from a material such as resin black, in which carbon or Ti is dispersed in a photoresist. Thereafter, the counter electrode is formed by depositing a transparent conductive film, such as ITO, by a sputtering process or the like over the entire surface of the opposing substrate to a thickness of approximately 50–200 nm (step S53). Furthermore, after applying a coating liquid of a polyimide alignment layer over the entire surface of the counter electrode, an alignment layer 22 is formed by performing a rubbing process or the like in a prescribed direction so as to have a prescribed pretilt angle (step S54).

[0141]

Thus, once the plurality of active-matrix substrates AM is formed on the motherboard MM and the plurality of opposing substrates is formed on a separate motherboard, next, these are pasted together via the sealing material (step S81). Then, an electro-optical substance, such as a liquid crystal in which, for example, a plurality of types of nematic liquid crystal are mixed, is sealed by vacuum suction or the like in the space sandwiched between the active-matrix substrates AM and the opposing substrate (step S82). Lastly, in the state in which both motherboards are pasted together, the motherboards are separated along the cutting line (step S83), and thereby the electro-optical devices are completed.

[0142]

Note that this separating process thereby results in the above-mentioned inter-substrate-device short-circuit wiring 99 being separated at the same time, and therefore operation of the electro-optical device manufactured as described above has no risk of being hindered by the inter-substrate-device short-circuit wiring 99.

[0143]

The present invention is not limited to the embodiments described above and can be appropriately modified within a range that does not depart from the gist or idea of the invention that can be read from the claims and the entire specification, and a method of manufacturing an element-substrate device, the method of manufacturing the electro-optical device, as well as the reticle that accompany such modifications are also included within the technical scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram schematically illustrating an overall configuration of an active-matrix substrate according to an embodiment of the present invention.

FIG. 2 is a plan view illustrating: terminals shown in FIG. 1; aperture portions formed in interlayer-insulating films to correspond to the terminals; and contact holes formed in interlayer-insulating films to achieve electrical connection between said terminals and short-circuit wirings, which are illustrated in FIG. 1.

FIG. 3 is a block diagram illustrating a detailed

configuration of an electrostatic-protection circuit, which is illustrated in FIG. 1.

FIG. 4 is a plan view illustrating details of a layout mode between a signal wiring, which is illustrated in FIG. 1, and a first short-circuit wiring.

FIG. 5 is a plan view of a plurality of mutually adjacent pixel groups of a TFT-array substrate on which is formed data lines, scan lines, pixel electrodes, and the like.

FIG. 6 is a cross-sectional view taken along line A-A' in FIG. 5.

FIG. 7 is a plan view illustrating an aspect in which the active-matrix substrates, which is illustrated in FIG. 1, have been formed and arranged on a motherboard.

FIG. 8 is an enlarged plan view of an area A on the motherboard which is illustrated in FIG. 1.

FIG. 9 is a process cross-sectional view (part 1) illustrating a manufacturing method for the active-matrix substrate illustrated in FIG. 1.

FIG. 10 is a process cross-sectional view (part 2) illustrating a manufacturing method for the active-matrix substrate illustrated in FIG. 1.

FIG. 11 is a process cross-sectional view (part 3) illustrating a manufacturing method for the active-matrix substrate illustrated in FIG. 1.

FIG. 12 is a plan view of a TFT-array substrate and each structural element formed thereon, viewed from the opposing substrate side.

FIG. 13 is a cross-sectional view taken along line H-H' in FIG. 12.

FIG. 14 is a flow chart illustrating a manufacturing method for an electro-optical device following the order of the processes.

EXPLANATION OF THE REFERENCE NUMBERS

3a Scan line

6a	Data line
10	TFT-array substrate
20	Opposing substrate
30	TFT
41, 42, 43	Interlayer-insulating films
50	Liquid-crystal layer
70	Storage capacitor
72, 73	Signal wirings
81, 82, 83, 85, 89, 403	Contact holes
91, 92, 93, 3b	First to third short-circuit wirings
99	Inter-substrate-device short-circuit wiring
101	Data-line drive circuit
102	External-circuit connection terminal
104	Scan-line drive circuit
800, 801, 802	Terminals
880	Cutting hole
901	Resist
950	Reticle
950a	Thin film
950b	Light-shielding film
AM	Active-matrix substrate
MM	Motherboard

FIG. 1

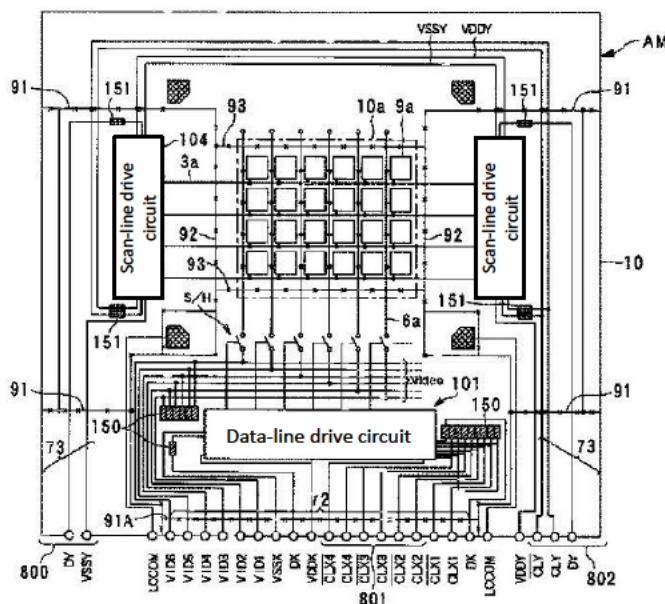


FIG. 2

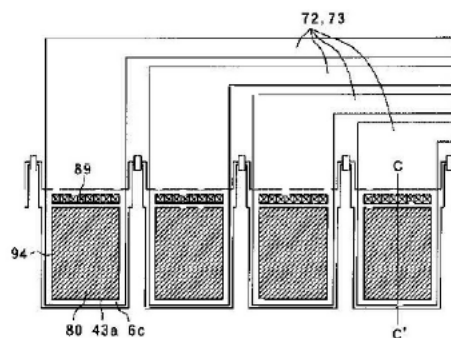


FIG. 13

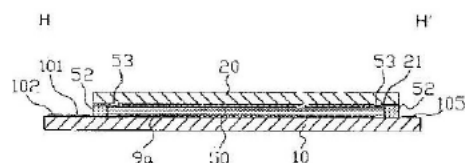


FIG. 3

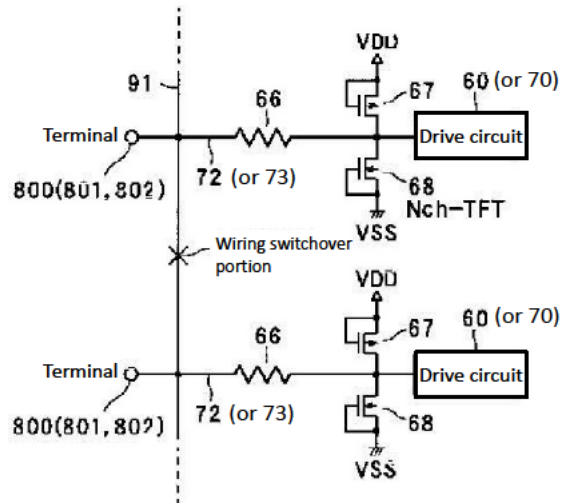


FIG. 4

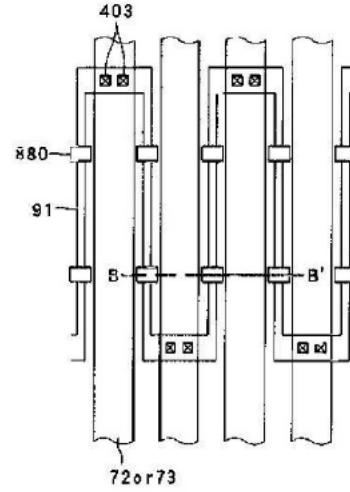


FIG. 5

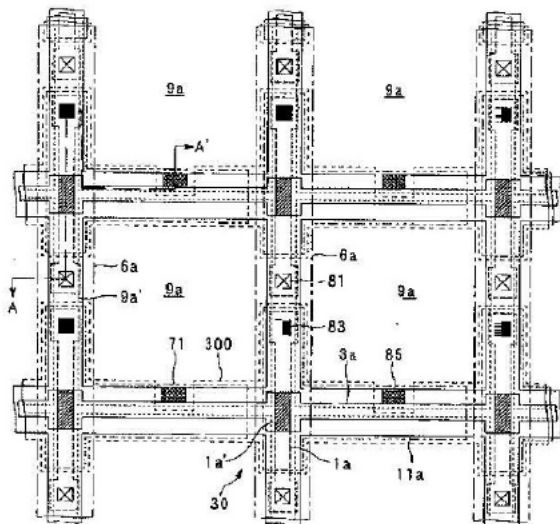


FIG. 7

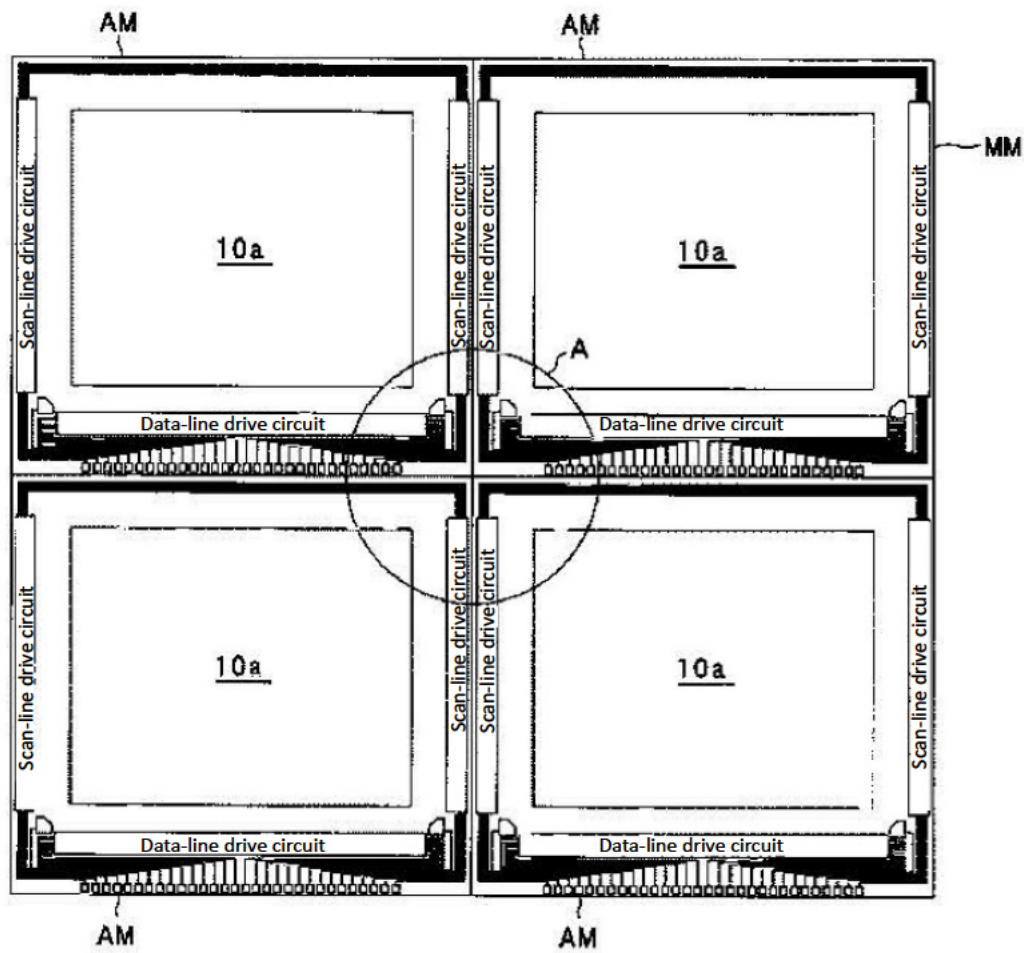


FIG. 6

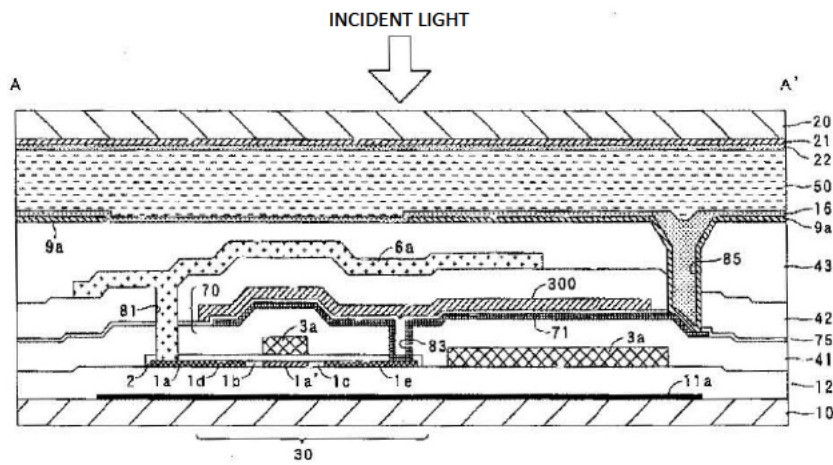


FIG. 8

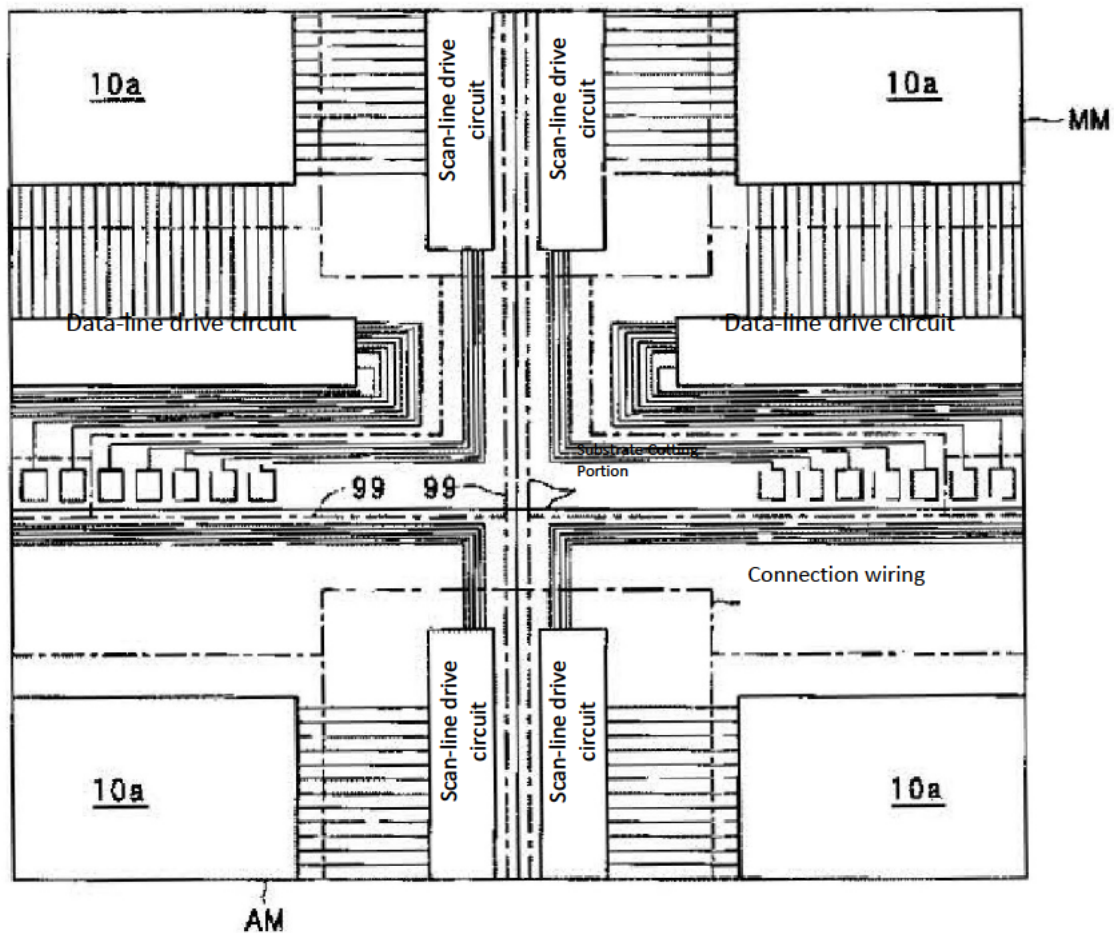


FIG. 14

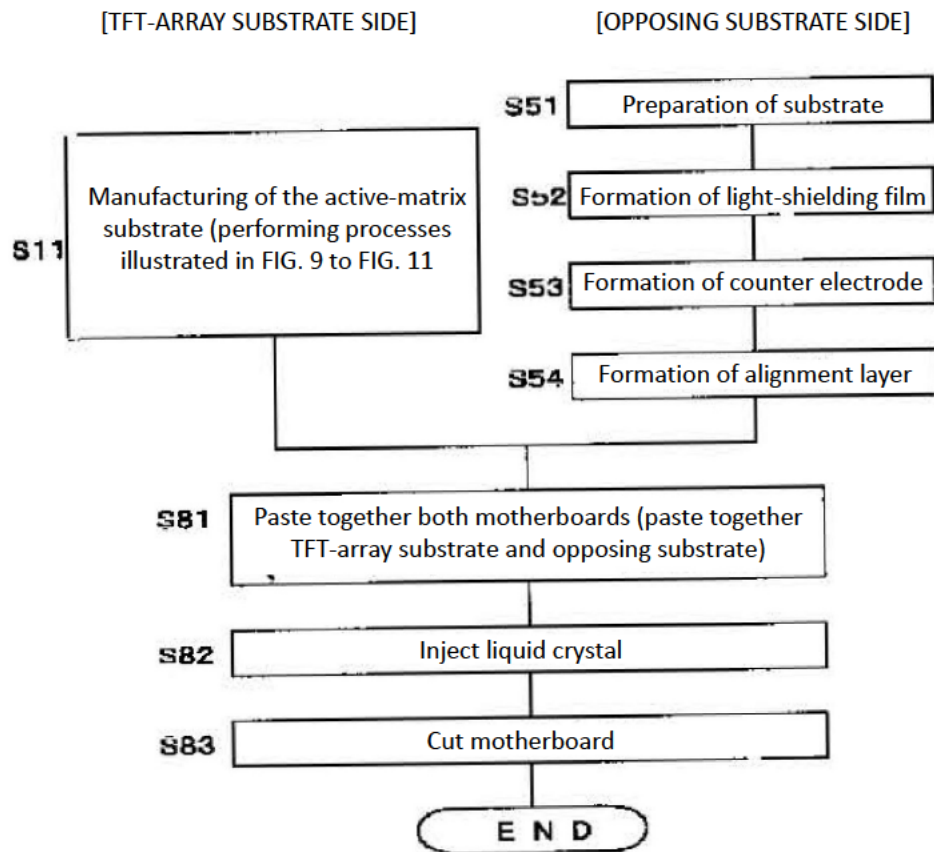


FIG. 9

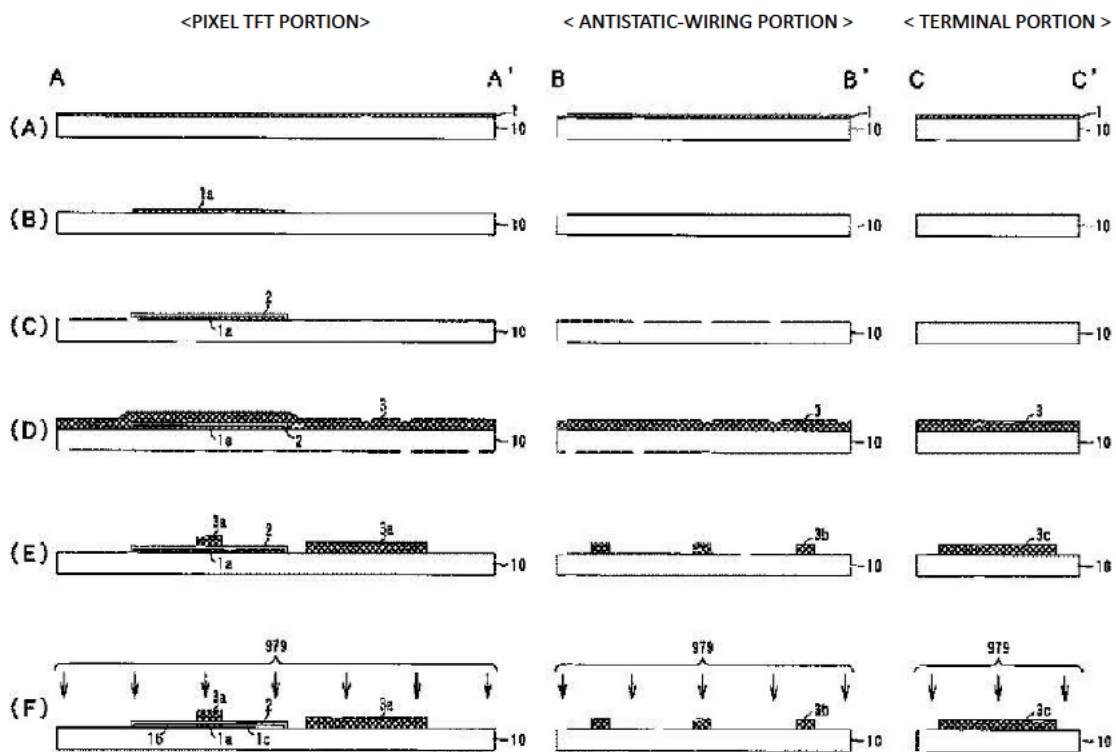


FIG. 10

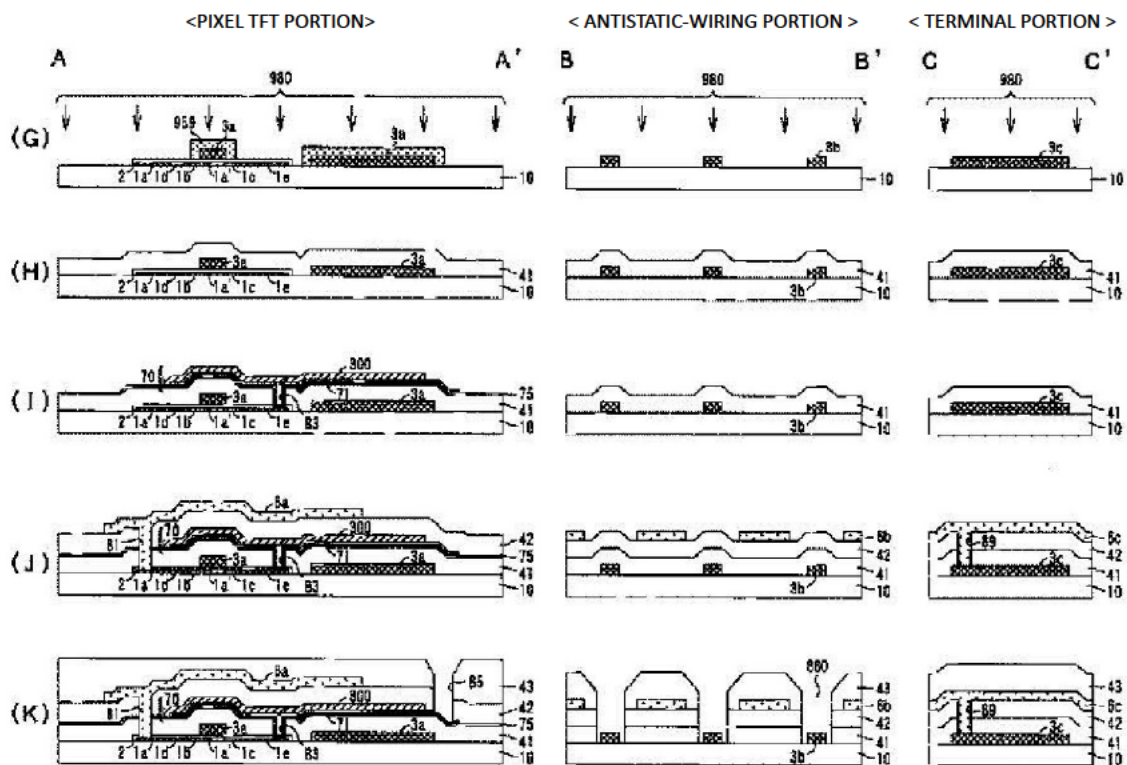


FIG. 11

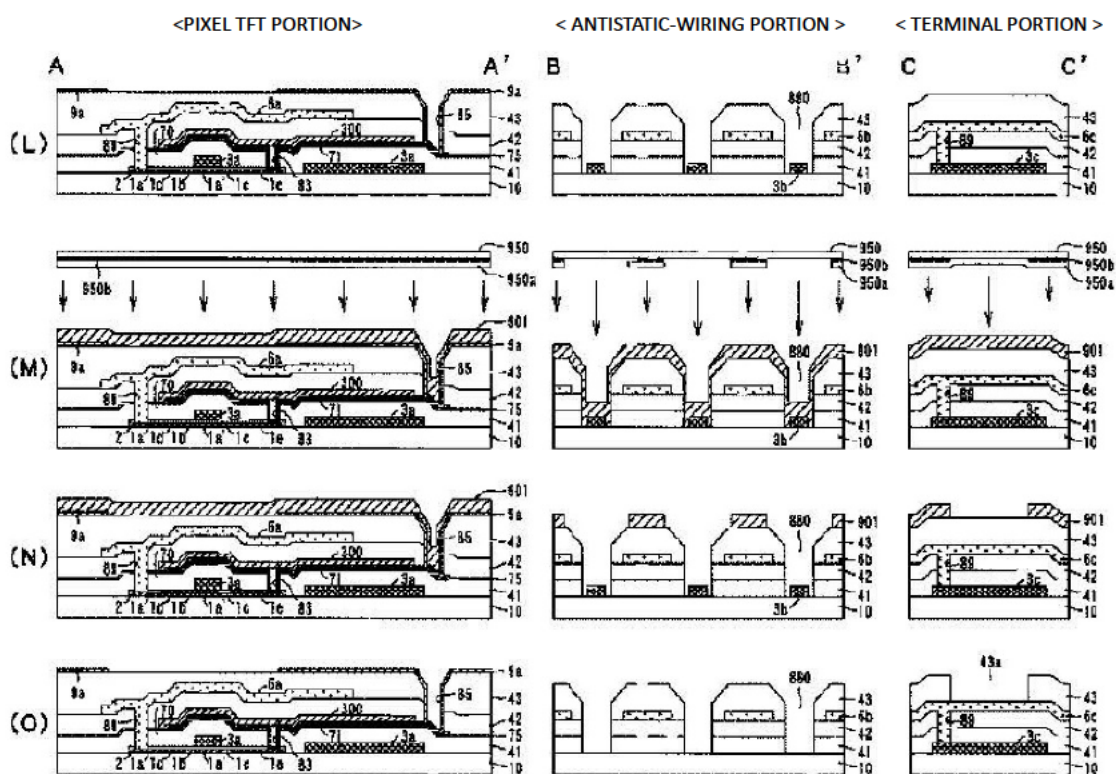
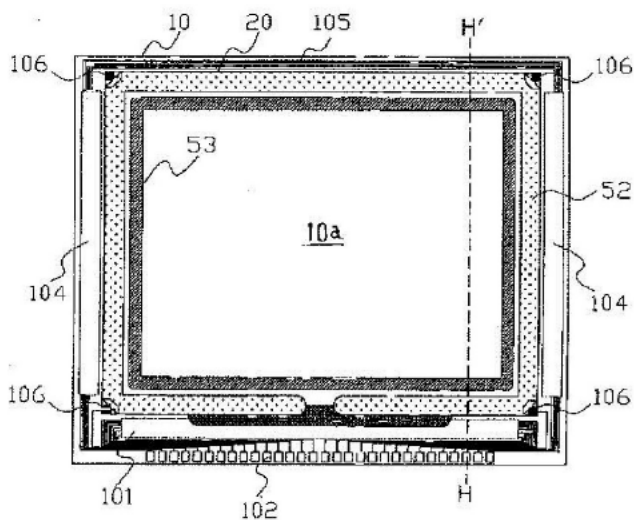


FIG. 12



Continuation of front page

(51) Int. Cl. ⁷	ID	FI	(Reference)
G09F	9/00 338	G09F	9/00 338
	9/30 338		9/30 338
H01L	21/027	H01L	29/78 612C
	29/786		623A
			21/30 502R

F-Term (Reference)	2H088	FA00	FA24	FA28	HA01	HA02
		HA05	HA06	HA08	MA03	MA20
2H092	GA14	GA64	HA11	JA24	JB22	
	JB31	JB79	MA13	MA17	NA14	
	PA01	PA06				
2H095	BA12	BB02	BC04	BC24		
2H097	GB00	LA10				
5C094	AA42	AA43	AA46	AA48	BA03	
	BA43	CA19	DA09	DA13	DA15	
	DB01	DB04	DB10	EA04	EA05	
	EB02	FA01	FA02	FB01	FB12	
	FB15	GB10				
5F110	AA22	BB02	BB04	CC02	DD02	
	DD03	EE09	EE28	EE37	FF02	
	FF03	FF09	FF23	FF29	GG02	
	GG13	GG25	GG47	HJ01	HJ04	
	HJ13	HJ23	HL02	HL03	HL05	
	HL06	HL23	HM14	HM15	NN03	
	NN04	NN22	NN23	NN24	NN35	
	NN72	NN73	PP01	PP10	PP33	
	QQ11					
5G435	AA17	BB12	CC09	EE37	HH12	
	HH14	KK05	KK10			