

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case IPR2024-00973
U.S. Patent No. 9,184,157

**DECLARATION OF PATRICK MURPHY, PH.D., P.E.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,184,157**

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I. INTRODUCTION

1. I, Dr. Patrick Murphy, submit this declaration to state my opinions on the matter described below. I am over the age of 21 and am competent to make this declaration.

2. I have been retained by counsel for BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”), as an independent expert in this proceeding before the United States Patent and Trademark Office (“USPTO”). I am a salaried employee of Exponent. Exponent charges \$550 per hour for my time plus expenses for work performed in connection with this project, and I am being paid my regular salary for time spent on this project. I have received no additional compensation for work in this case. My compensation does not depend upon the contents of this declaration, any testimony I may provide, or the ultimate outcome of the case. I have no other interest in this proceeding.

3. I understand that this proceeding involves U.S. Patent No. 9,184,157, (“the ’157 patent”) (Ex. 1001). I have been asked to provide my opinions as to the patentability of claims 1-18 of the ’157 patent. I understand that the application for the ’157 patent was filed on May 6, 2009, and claims priority to an earlier U.S. patent application filed on April 8, 2005, as well as a Japanese priority document filed on July 5, 2004.

4. I have been asked to consider the validity of claims 1-18 of the '157 patent based on certain prior art references. I have also been asked to consider the state of the art and prior art available as of July 5, 2004.

5. As discussed in this declaration, it is my opinion that claims 1-18 of the '157 patent would have been obvious based on *Reiner* (Ex. 1005) (Ground 1) or alternatively the combination of *Reiner* and *Takahara* (Ex. 1006 (original document), Ex. 1007 (English translation)) (Ground 2).

II. EXPERIENCE AND QUALIFICATIONS

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my educational and work experience, and specifically, flat panel display devices, including liquid crystal displays ("LCDs"), and electrostatic damage ("ESD") protection for such devices.

7. A summary of my experience, qualifications, and current employment are included in my CV attached as Exhibit 1004. This CV includes a list of all publications I have authored within the preceding ten years. I have also provided a list of cases in which I have testified as an expert at trial or by deposition within the preceding four years, attached as part of Exhibit 1004. The following is a brief summary of my relevant qualifications and professional experience.

8. I received my B.S. degree in Electrical Engineering (magna cum laude) in 2002 from Boston University; my M.A. degree in Electrical Engineering in 2004 from Princeton University; and my Ph.D. degree in Electrical Engineering, also from Princeton University in 2009. This education included advanced coursework, project work, and laboratory work in design and manufacturing of electronic circuits, integrated circuits, and optoelectronic devices, including LCDs and ESD protection. Specifically, my undergraduate and Master's coursework included study of the optics of liquid crystal materials used in LCDs, the effects of electrical overstress and electrostatic discharge on CMOS devices and circuits, techniques such as surge limiting devices for protecting against electrostatic discharge when designing electronic circuits and systems, and fabrication techniques for manufacturing integrated circuits including thin-film transistors for LCD backplanes.

9. My training and research for my academic degrees at Princeton was generally in the area of semiconductor integrated circuit design and fabrication technologies, including liquid crystal optoelectronic devices. I taught university-level topics in electronic devices, integrated circuit fabrication, and optics. I am author of several publications in these areas, including on liquid crystal-based

optoelectronic devices as well as on electronic and optoelectronic devices for displays and other applications.

10. I am licensed as a professional engineer in the State of New York and licensed as a professional engineer in electrical engineering in the State of California. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE). I have over 20 years of experience in electrical engineering including over 20 years of experience in the areas of design and manufacturing of electronic circuits and optoelectronic devices.

11. I am currently a Principal Engineer in Exponent's Electrical Engineering and Computer Science Practice and I am based in Exponent's New York office. Exponent is an engineering and science consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025.

12. Since joining Exponent in 2009, my duties and responsibilities have included leading investigations into the performance, design, and condition, of electrical and electronic systems and devices, including projects relating to the design, structure, function, and failures of electronic circuits and optoelectronic devices, such as LCDs and ESD protection devices.

13. As part of my work at Exponent, I have analyzed the materials, manufacturing processes, components, designs, and applications of LCD panels. I

also have experience with the technology of connectors, flat panel displays, TFTs and backplanes for displays, as well as design, layout, and manufacturing of electronic circuits on printed circuit boards, signal routing on semiconductor devices, and ESD protection of semiconductor devices, such as LCDs.

14. As part of my work at Exponent, I have evaluated failed integrated circuits and semiconductor devices for ESD and electrical overstress (EOS) related failure by way of analysis of circuit and device designs, as well as testing of circuits and devices for compliance with ESD and EOS industry standards.

15. As part of my work at Exponent, I have analyzed the design and manufacturing and performance of such semiconductor devices and integrated circuits as microprocessors, flash memory, 3D integrated circuits, bipolar power transistors, insulated-gate bipolar transistors, photodetectors, photovoltaic cells, light-emitting diodes, and thin-film transistors for displays.

III. MATERIALS CONSIDERED

16. In forming my opinions, I have reviewed the '157 Patent, along with its prosecution history and references cited by the examiner during prosecution. I also reviewed the materials listed below and any other materials cited throughout my declaration.

Declaration of Patrick Murphy, Ph.D., P.E.
U.S. Patent No. 9,184,157

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,184,157 to Kobashi (“the ’157 patent”)
Ex. 1002	File History for U.S. Patent No. 9,184,157
Ex. 1005	International Publication No. WO 03/019657 A2 to Reiner et al. (“ <i>Reiner</i> ”)
Ex. 1006	Japanese Patent Application Publication No. JP2003-121875 to Takahara
Ex. 1007	Certified English Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara (“ <i>Takahara</i> ”)
Ex. 1008	Certificate of Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara to English
Ex. 1009	Japanese Patent Application Publication No. JP2001-166334 to Murai
Ex. 1010	Certified English Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai (“ <i>Murai</i> ”)
Ex. 1011	Certificate of Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai to English
Ex. 1012	James E. Vinson & Juin J. Liou, “Electrostatic Discharge in Semiconductor Devices: An Overview,” Proceedings of the IEEE, Vol. 86, No. 2, pp. 399-418 (Feb. 1998)
Ex. 1013	Toshio Murakami et al., “Electrostatic problems and ionization solutions in TFT-LCD Production,” Solid State Technology, Vol. 40, No. 1, pp. 99-102 (Jan. 1997)

IV. LEGAL STANDARDS

17. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

18. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

19. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

20. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-18 of the '157 patent from the perspective

of a person of ordinary skill in the art at the '157 patent's earliest claimed priority date in 2004, as described in more detail below.

21. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means "more likely than not."

22. In forming my opinions and considering the subject matter of the '157 patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

23. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims.

24. I understand that a claimed invention is only patentable when it is new, useful, and non-obvious in light of the "prior art." That is, the invention, as defined by the claims of the patent, must not be anticipated by or rendered obvious by the prior art.

A. Level of Ordinary Skill in the Art

25. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

26. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Claim Construction

27. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of one of ordinary skill in the art at the time of the alleged invention.

28. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I

understand, however, that claim terms are generally not limited by the embodiments described in the specification.

29. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

C. Prior Art

30. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

D. Anticipation

31. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

E. Obviousness

32. I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

33. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;

- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

34. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the July 5, 2004. My opinions would not change if I assumed a later date of invention.

35. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

36. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve

the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

37. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have had a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

38. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of

ordinary skill in the art would have had a good reason to pursue those known options.

39. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

40. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to

combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

41. I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '157 patent.

42. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. BACKGROUND OF THE TECHNOLOGY

43. Electronic devices are susceptible to damage from the discharge of static electricity. The everyday experience of receiving a shock when touching a door handle is an example of a typical static discharge event. While startling, but generally not harmful, to humans, static electricity discharge can damage or destroy electronics. Referred to in the field as “electrostatic discharge,” or ESD, steps are taken to prevent potentially damaging ESD events from taking place and

to provide electronic devices with circuit-level protections for when these events do occur. ESD is a subset of a larger area of study known as “electrical overstress,” or EOS, which aims to document the mechanisms by which electronic devices can break or degrade as a result of exposure to overly large voltages or currents. Ex. 1012, Vinson & Liou, “Electrostatic Discharge in Semiconductor Devices: An Overview,” 1998, p. 1.¹

44. ESD concerns itself with the specific phenomenon of rapid charge transfer between differentially charged objects when they are brought into contact. A well-known method of accumulating charge on an object is by rubbing it, a process formally referred to as ‘triboelectric charging.’ Another method is electrostatic induction, whereby external electric fields can induce charges on an object. These electric fields may emanate from another nearby electrostatically charged object or energized electrical equipment. Lastly, an object may become charged by coming into contact with another charged object, where the charge will then equilibrate between the two objects, leaving both of them charged relative to the Earth even if they are later separated. Ex. 1012, Vinson & Liou, pp. 1, 4.

¹ My citations to pages refer to exhibit page number, rather than original page numbers.

45. Of critical concern in the manufacturing of electronic devices is the generation of static charge on sensitive components during the manufacturing process. Many process steps are abrasive, and often involve high temperatures, thus presenting a significant risk of charge buildup, which can lead to ESD events. Further, packaging and testing steps can expose these devices to damaging ESD events, which can cause damage and reduce process yield. Although environmental precautions can be put into place in controlled facilities to reduce the risk of static charge buildup, they may not be fully effective. Moreover, electronics in the hands of end-users are at risk of damage from ESD events because they cannot rely on any environmental ESD protections and may be exposed conditions that are electrostatically hostile. A user walking over a thick rug on a low-humidity day may become charged to thousands of volts, which can discharge through the circuitry of the device. Circuit-level ESD protections are designed into electronic devices in order to protect against these types of events during manufacturing or use. Ex. 1012, Vinson & Liou, p. 2.

46. The goal of ESD protection circuits is to provide a conduction pathway that routes ESD current around the circuits to be protected. Ex. 1012, Vinson & Liou, p. 9-10. Commonly used circuitry for diverting ESD current to ground or supply rails include reverse-biased diodes and the parasitic bipolar

junction transistors that accompany MOSFETs. Resistors may also be used in the signal path to slow the rate of ESD charge transfer, thereby reducing the ESD current driven into the electronic device. Examples of each of these basic protection elements are shown in the figures below.

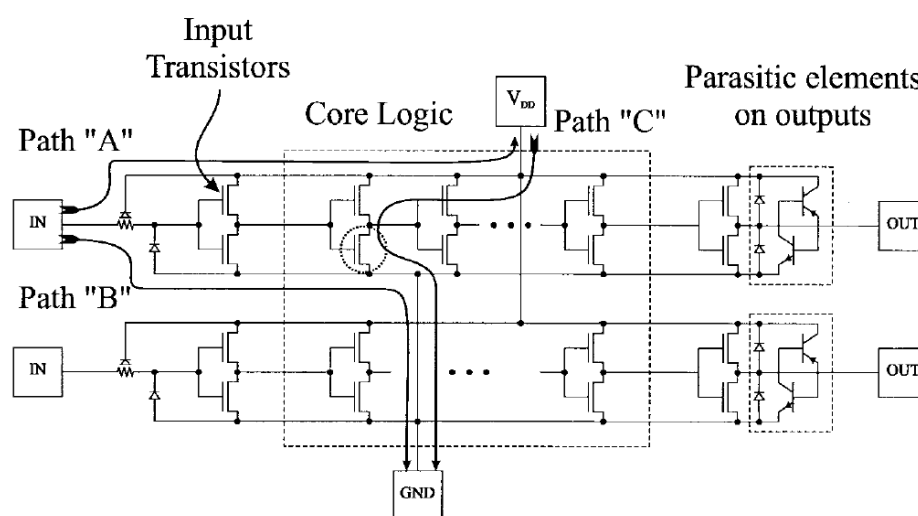


Fig. 11. Digital circuit schematic as seen by an ESD event.

Ex. 1012, Vinson & Liou, p. 11, Fig. 11.

47. One consideration in designing ESD protection circuits is that these circuits should be suppressive to ESD events, but not overly affect the signals intended to be driven into the circuit. Ex. 1012, Vinson & Liou, p. 9. Several standard models of common ESD sources have been developed to quantify the level of protection that any given circuit provides. These include the Human Body Model (HBM), which models the effect of a charged human touching an electronic

device; the Machine Model (MM), which models an electronic device coming into contact with other charged equipment during the automated fabrication process; and the Charged Device Model (CDM) which models charged elements within the electronic device itself discharging into an externally contacted object. Ex. 1012, Vinson & Liou, pp. 4, 6-7.

48. Most integrated electronics are implemented in silicon, and large investments are made in protecting these devices from ESD. Certain applications, however, may use different substrate materials. Electronic device displays, for example, LCDs, can be implemented on glass substrates and, because glass is insulative, can have increased ESD risks. As an insulator, glass is capable of accumulating electrostatic charge easily and retaining it for long periods. Thus, in the production of electronic displays, special attention is devoted to ESD mitigation. Ex. 1013, Murakami et al., “Electrostatic problems and ionization solutions in TFT-LCD Production,” 1997. Regardless of the substrate type, however, the same fundamental principles apply in the design of ESD protection circuits. And a POSITA would routinely look to ESD protection circuits for silicon substrates when designing ESD protection circuits for devices based on glass substrates.

VI. STATE OF THE ART AND ADMITTED CONVENTIONAL ESD PROTECTION

49. The '157 patent acknowledges that, in the prior art, “it is important to take measure[s] against the electro-static damages (ESD) when a high voltage caused by static electricity or a various noise phenomenon is unintentionally applied to the inside of the device to damage an insulating film, thereby causing a fatal damage to the device.” Ex. 1001, 1:14-19. The use of “it is a key issue to prevent the damage when static electricity flows through the input terminals.” Ex. 1001, 1:23-28. “Conventionally” this problem was solved with “protective circuits ... formed between [the] input terminals and the semiconductor device.” Ex. 1001, 1:28-32. “[C]onventional method[s]” also included a “silicon wafer” in the driving circuit having “protective circuits for preventing the static electricity from the input terminals.” Ex. 1001, 1:47-56. This “conventional art” is described in FIG. 11. Ex. 1001, 1:54-56.

50. FIG. 11 of the '157 patent shows this “the conventional art” having a “scanning lines” 201-1 to 201-480, “driven by a scanning line driving circuit 800.” Ex. 1001, 1:57-61. Scanning line driving unit 800 includes “scanning line driving unit circuits composed of 480 stages” 801-1 to 801-480.” Ex. 1001, 1:66-2:2. Each scanning line driving unit circuit “is connected to a **low potential power line 750 [VS]** and a **high potential power line 751 [VD]**, through which power is supplied.”

Ex. 1001, 2:5-15. The “low potential power line 750 is connected to low potential power terminal 650” and the “high potential power line 751 is connected to a high potential power terminal 651.” Ex. 1001, 2:8-10. To “prevent TFTs [thin film transistors] constituting each of the scanning line driving unit circuits 801-1 to 801-480 from being damaged by static electricity ... through the low potential power terminal 650[] [or] the high potential power terminal 651,” “static electricity protection circuits” ESD1 and ESD2 “are provided between the input terminals” 650, 651 “and the scanning line driving unit circuits 801-1 to 801-480,” as shown in FIG. 11. Ex. 1001, 2:20-28. ESD3 and ESD4 similarly protect CLK signal line 701 and SP signal line 702, as shown below.



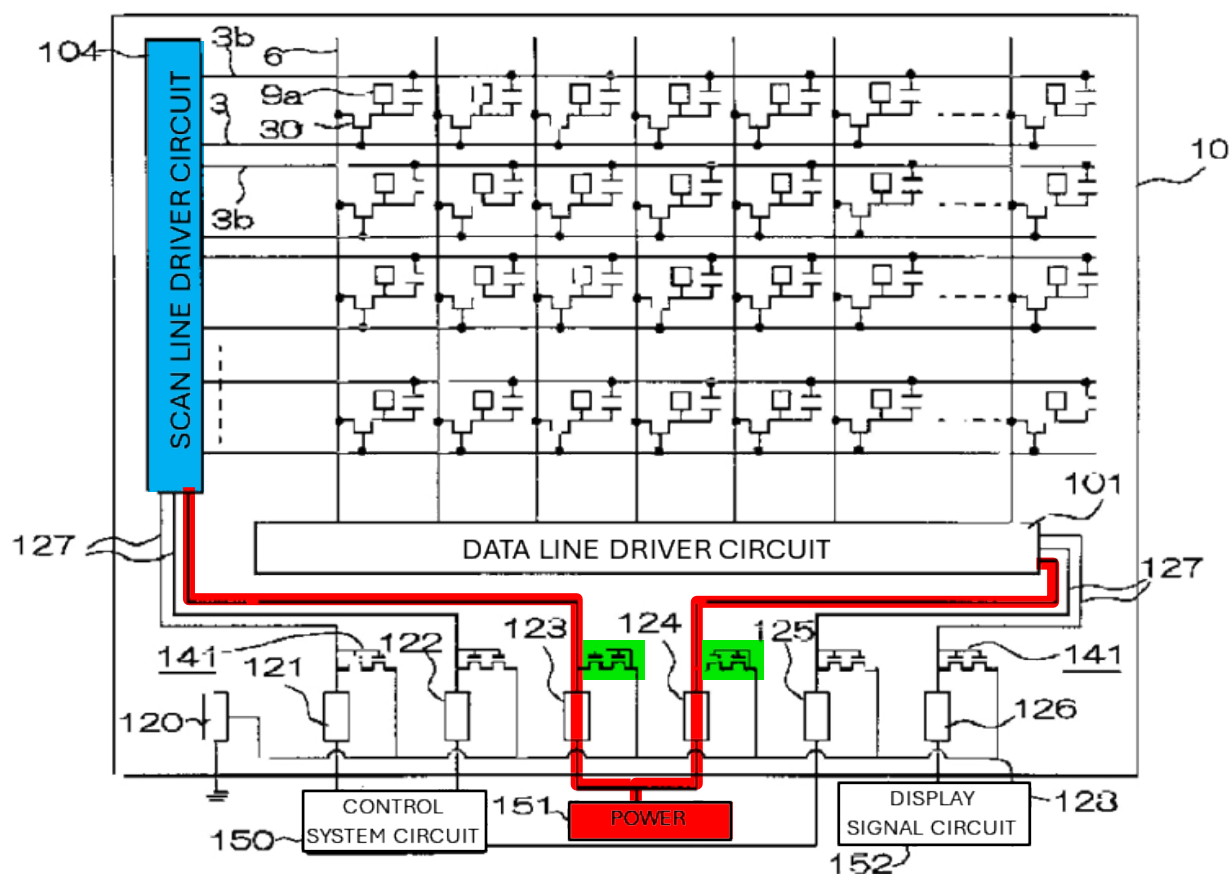
² All colors and colored annotations have been added to figures unless otherwise noted.

driving circuits or data line driving circuits, against ESD events and potential damage.

52. For example, *Murai* discloses providing ESD protection at many locations in an LCD device. *Murai*'s FIG. 1 shows "external-circuit connection terminal portions 123, 124" that are connected to "power circuit [151]." *Murai*, [0021].³ This power is supplied to "scan line driver circuit 104" and "data line driver circuit 101." *Murai*, [0021]-[0022]. *Murai* explains that, to "prevent[] ... electrostatic breakdown of the driver circuit caused by static electricity," an "electrostatic-breakdown-preventing circuit" 141 is provided "partway along a wire connecting the external-circuit connection terminal portion and the driver circuit." *Murai*, [0003], [0021], FIG. 1. Control system circuit 150 and display signal circuit 152 are similarly protected by electrostatic breakdown protection circuits 141. *Murai*, [0021], FIG. 1.

³ My citations to *Murai* are made to the English translation (Ex. 1010).

FIG. 1

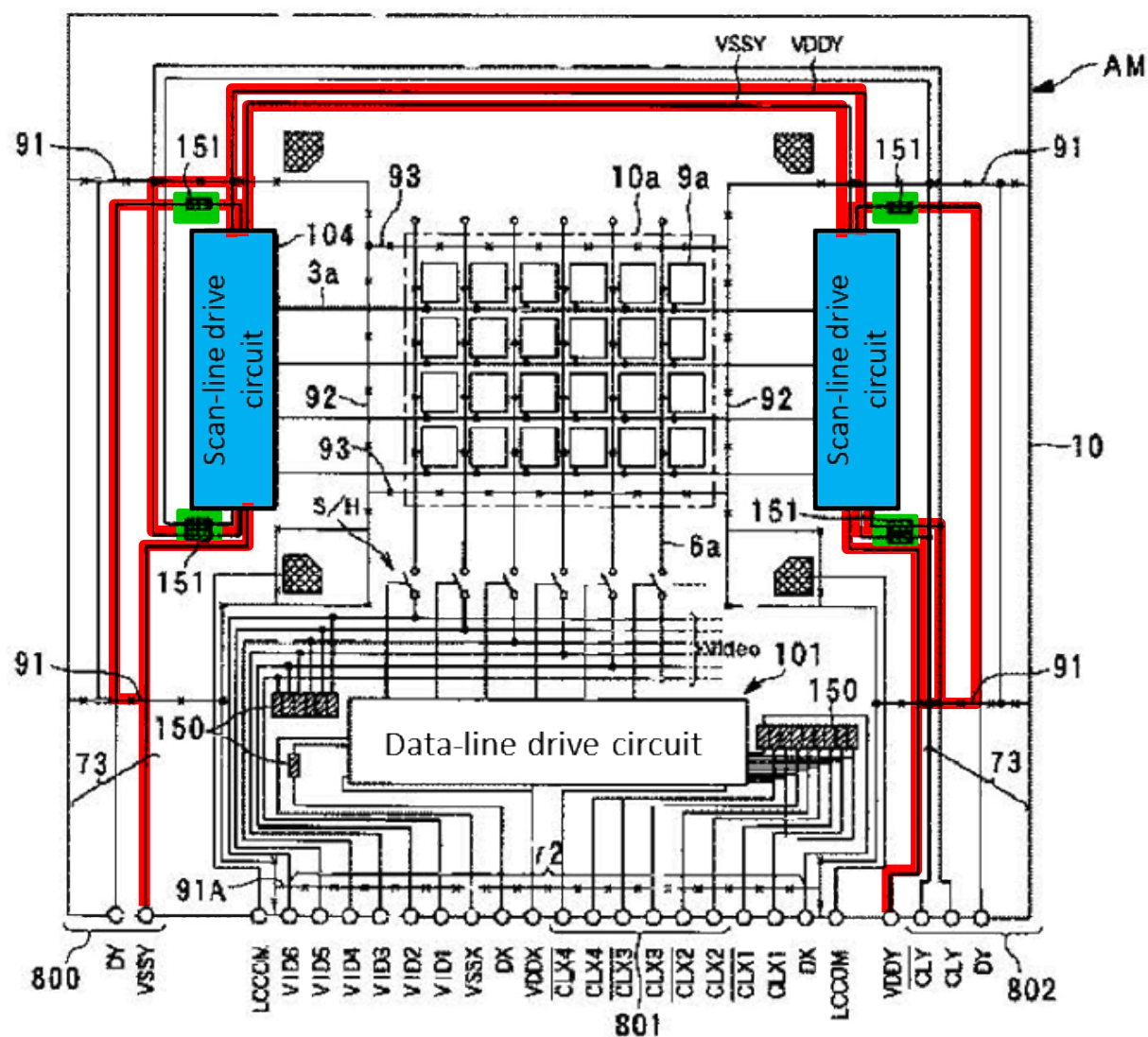


Murai, FIG. 1.

53. *Takahara* similarly teaches ESD protection using multiple protection circuits. *Takahara* teaches that “[e]lectrostatic-protection circuits 150 and 151 are formed at intermediate locations of the signal wirings 72 and 73” so that “static electricity is reliably absorbed” and “scan-line drive circuit 104 can be reliably protected.” *Takahara*, [0066], FIG. 1. Power lines VDDY and VSSY are shorted to

ESD protection circuits 150 and 151 using shorting wiring lines 91 (marked with an “x”) to protect both ends of the scan-line drive circuit 104. Takahara, [0070].

FIG. 1



Takahara, FIG. 1.

54. *Reiner* likewise teaches “integrated circuit devices with ESD protection.” *Reiner*, 2:2-3.⁴ *Reiner* explains that a “typical example” of a protected integrated circuit device is “an integrated circuit display driver 61 or 63 that is designed to drive many lines of an LCD display 60.” *Reiner*, 9:11-14. One such example is “gate driver 63” ([scanning line driving circuit](#)) that “drives one whole gate line 68” shown in *Reiner*’s FIG. 4. *Reiner*, 9:27-28, FIG. 4.

⁴ My citations to *Reiner* are in page:line format. I have been instructed to cite to the exhibit page numbers, not original page numbers. The exhibit page numbers are one number greater than the original page numbers because the original cover page is not numbered.

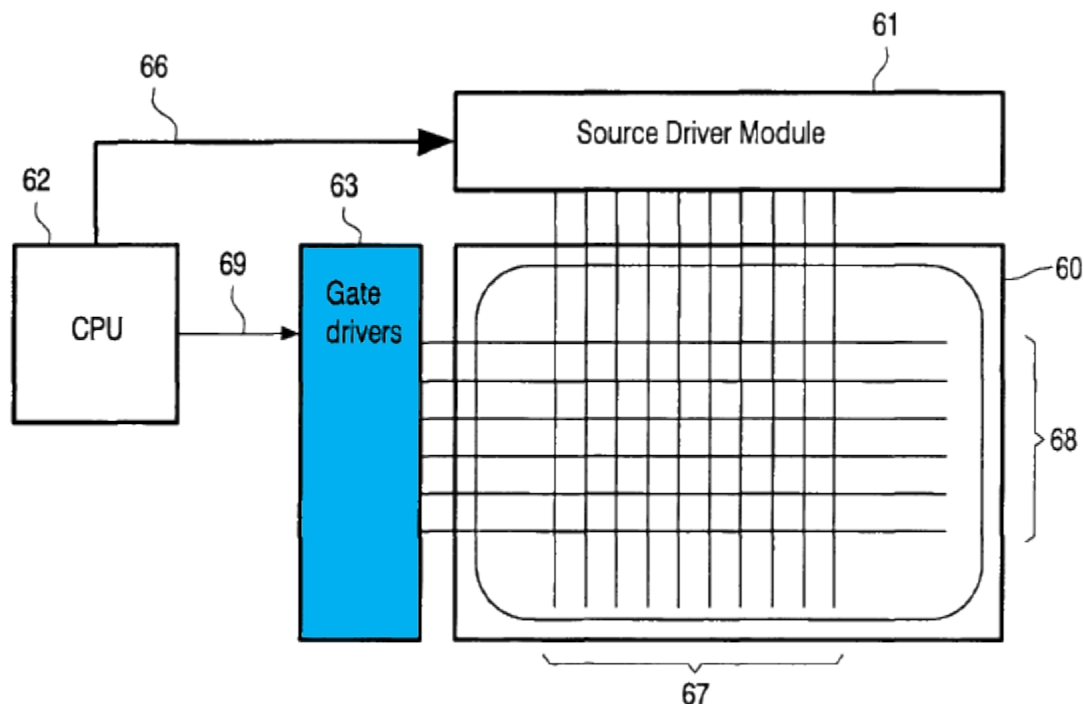


FIG. 4

Reiner, FIG. 4.

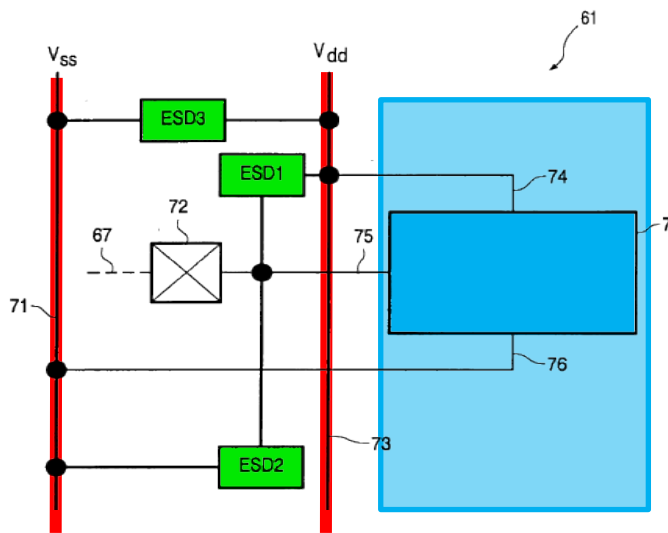
55. *Reiner* explains that, “[q]uite often,” these “integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when subjected to a discharge event.” *Reiner*, 2:28-3:1. *Reiner*’s teachings are “well suited for use in integrated circuit devices ... that comprise electrostatic discharge device (ESD) protection” and describe an advantage to “provide a scheme that allows to add an ESD protection network to densely packed integrated circuits.” *Reiner*, 5:15-16, 8:8-10. *Reiner* discloses an ESD protection network for the exemplary source

driver module 61 in FIG. 5, by providing “three ESD devices ESD1, ESD2, and ESD3 ... for each output device 70, in order to protect the circuitry inside the devices 70.” *Reiner*, 10:10-12. For at least the reasons explained below, it is my opinion that a POSITA would have understood that the ESD protection network of *Reiner* applies to both integrated circuits 61 (source/data line driver) and 63 (gate driver/scanning line driver).

56. An example ESD protection network is shown in FIG. 5, where the ESD protection network is connected to two power supply lines—“supply voltage Vdd” and “supply voltage Vss”—and connected to the “output devices 70” of the integrated circuit device 61. *Reiner*, 10:1-15. *Reiner*’s disclosure teaches providing an “ESD protection network” that is “connect[ed] ... with the inputs and/or outputs of the integrated circuit device to be protected” at “each output device.” *Reiner*, 3:4-8, 4:15-16, 8:11-15, 10:1-15 (emphasis added). In particular, because the “three ESD devices” are provided “for each output device 70,” *Reiner* teaches replicating the ESD protection network at each of the “many output devices of the integrated circuits 61 or [63]”⁵ and “easily integrated into” such output driver

⁵ *Reiner*’s reference to 62 is a clear typographical error. Gate driver 63 is the only other integrated circuit device listed in *Reiner*, whereas item 62 is the CPU.

devices. *Reiner*, 9:10-14, 9:18-22, 10:1-15, FIG. 5. *Reiner*'s FIG. 5 shows one of the protection networks having ESD1-ESD3 for an output device 70. Composite FIG. F, below, shows an example of how *Reiner*'s teaching that each of the **output devices** in the integrated circuit 61, 63 includes the **three-ESD protection network** would have been understood by a POSITA.



Reiner, FIG. 5

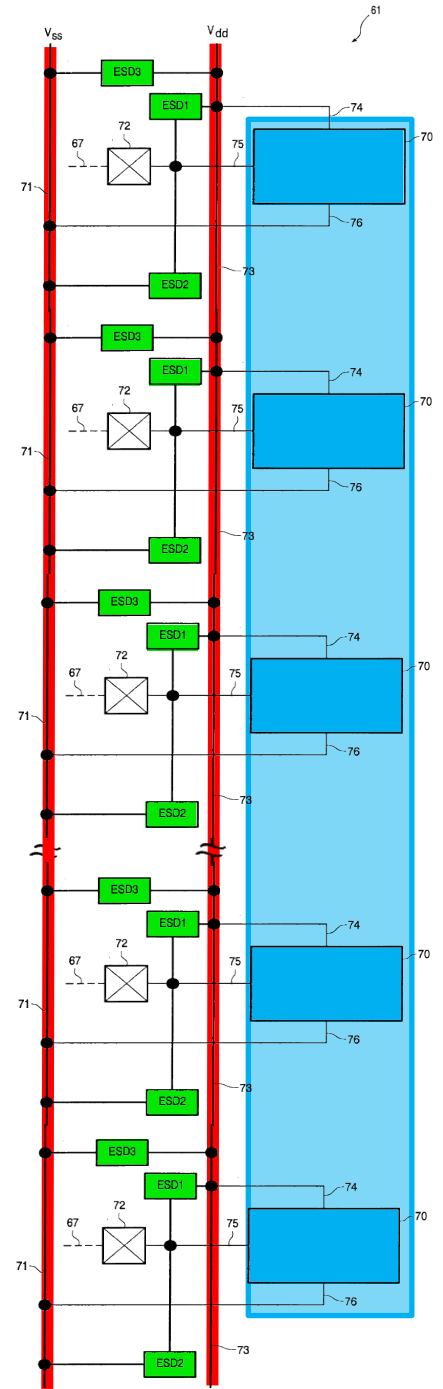


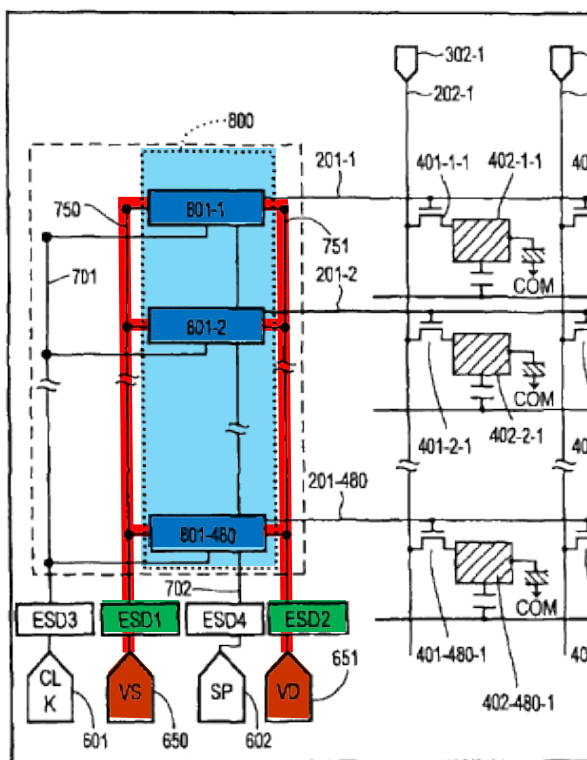
FIG. F

VII. THE '157 PATENT

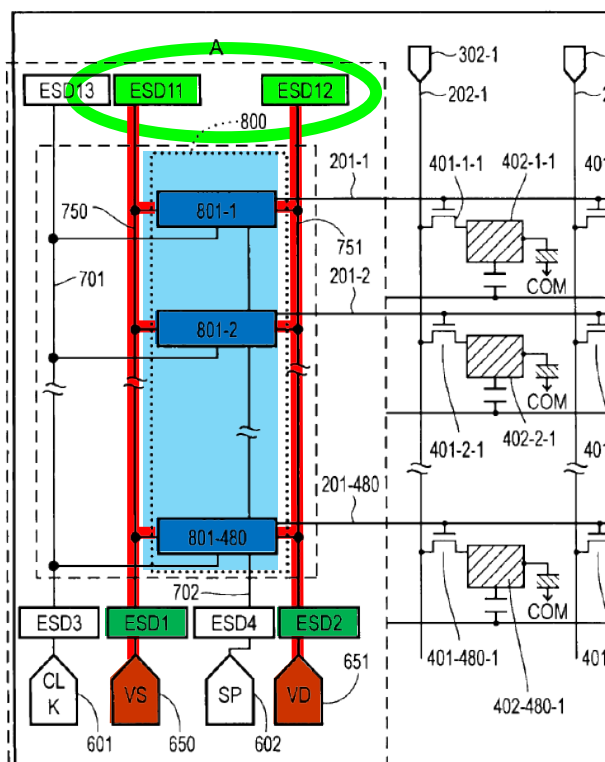
A. Alleged Invention of the '157 Patent

57. The '157 patent “relates to a semiconductor device, display device and electronic apparatus, and more particularly, to a display device having a driving circuit provided on an active matrix substrate.” Ex. 1001, 1:10-13.

58. The '157 patent purports to improve the admitted conventional prior art of FIG. 11 by adding additional ESD protection circuits in various configurations. Ex. 1001, FIGS. 1, 2, 3. For example, in one embodiment in FIG. 1, the '157 patent shows **second ESD circuits ESD11 and ESD12** added to **power lines 750, 751** of FIG. 11, but no other differences, as highlighted in the excerpted comparison of FIGS. 1 and 11, below.



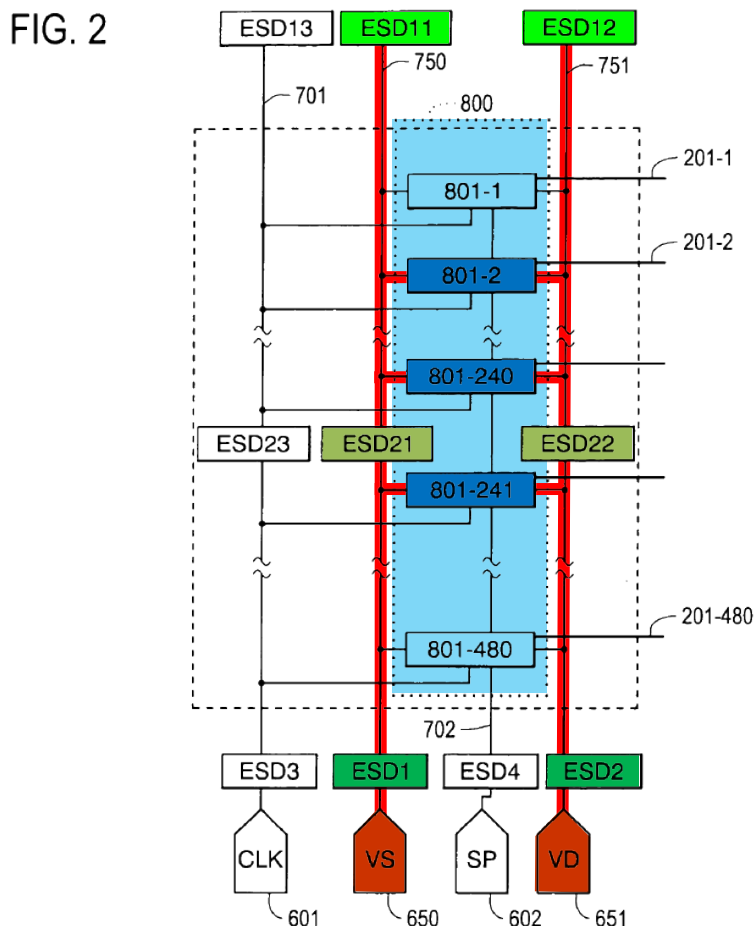
Ex. 1001, FIG. 11 (excerpted)



Ex. 1001, FIG. 1 (excerpted)

(admitted prior art)

59. Although FIG. 1 shows the additional ESD circuits ESD11/ESD12 at the end of the scanning line driving circuit 800, the '157 patent also describes adding additional ESD protection circuits ESD21 and ESD22. For example, ESD protection circuits ESD21 and ESD22 may be “provided between the unit driving circuit 801-240 at the 240th stage ... and the unit driving circuit 801-241 at the 241st stage” of the scanning line driving circuit 800, as shown in FIG. 2. Ex. 1001, 7:25-34.



Ex. 1001, FIG. 2.

60. The '157 patent continues that, “in addition to the locations of [FIG. 2], more preferably, the protective circuits are [also] interposed between the 120th stage (801-120) and the 121st stage (801-121), and between the 360th stage (801-360) and the 361st stage (801-361),” which would be every quarter of the scanning line driving circuit 800. Ex. 1001, 7:41-46. However, the '157 patent explains that, “[m]ost preferably, the protective circuits are interposed between all

stages [801-n] if there is no problem in the circuit area.” Ex. 1001, 7:46-51

(emphasis added).

61. For at least the reasons explained above in Section VI and below in Section X, the prior art already described protecting the scanning line driving circuits and circuit elements by interposing ESD protection circuits between each of the scanning line driver unit stages.

B. Prosecution History of the '157 Patent

62. The '157 patent was filed May 6, 2009, as U.S. Patent Application No. 12/436,335 and claims priority to U.S. Patent Application No. 11/101,450, filed April 8, 2005, and Japanese Patent Application No. JP2004-198040, filed July 5, 2004. Ex. 1001, cover (items (22), (63), (30)); Ex. 1002, 2.⁶

63. Prosecution of the '157 patent lasted more than 6 years, with the patent issuing November 10, 2015. Ex. 1001, cover (item (45)); Ex. 1002, 503 (Issue Notification).

64. The Examiner issued a first non-final office action on September 24, 2010. Ex. 1002, 94. In that office action, the Examiner rejected all of pending

⁶ Citations to the '157 patent's prosecution history (Ex. 1002) are made to exhibit page numbers.

claims 1-16. Ex. 1002, 95. First, the Examiner rejected claims 3, 7, 9, and 12 as being indefinite because several of the claim terms were unclear and could not be understood by the Examiner. Ex. 1002, 96-97. The Examiner then rejected claims 1, 2, 4-5, and 8 as being anticipated by U.S. Patent No. 6,791,632 (“Lee32”) and claims 7 and 13-16 as being anticipated by U.S. Patent No. 5,936,687 (“Lee87”). Ex. 1002, 98-100. The Examiner rejected claim 3 as being obvious of Lee32 and U.S. Patent No. 6,075,686 (“Ker”) and claims 9-12 as being obvious over Lee87 and other prior art references. Ex. 1002, 101-104.

65. In response to the first non-final office action, the Applicant filed an Amendment amending various claims, including to change “electrical signal” to “power” in claims 1 and 11 and to clarify certain connections between components in claims 2, 7, 8, 9, and 10, among other changes. Ex. 1002, 126-132. The Applicant argued that the amendments overcame the Examiner’s indefiniteness rejections and overcame the prior art rejections. Ex. 1002, 133-138. In attempting to distinguish the Lee32 reference, the Applicant argued that “[s]upplying an electrical signal, as allegedly disclosed in Fig. 4 of [Lee32], does not reasonably correspond to ‘an input terminal electrically connected to the wiring line to *supply power*,’ as recited in claim 1.” Ex. 1002, 135. The Applicant also argued that “[Lee32] does not disclose any semiconductor circuit in Fig. 4” because “Fig. 4 of

[Lee32] only shows empty space in each of grid lines formed by crossings of data lines D1-D3072 and gate lines G1-G768. Thus, Fig. 4 of [Lee32] fails to show any configuration of the alleged semiconductor circuit.” Ex. 1002, 136. The Applicant also argued that “a LCD panel at an intersection of a data line and a gate line would not have connected to any wiring line to which any input terminal is connected to supply power. Thus, the LCD panel of [Lee32] does not reasonably correspond to a semiconductor circuit to which a wiring line electrically is connected, wherein an input terminal electrically connected to the wiring line to supply power.” Ex. 1002, 136. The Applicant attempted to distinguish Lee87 because “Fig. 11 of [Lee87] does not show any object on the other end of shortening lines 450-480 other than diodes D57 and D58. [Lee87] does not show the diodes D57 (allegedly ‘a second protection circuit’) being arranged on the wiring line between pixels a-d (allegedly ‘semiconductor circuit’) and any second terminal portion” and because “supplying *signal* does not reasonably correspond to supplying *power*.” Ex. 1002, 136-137.

66. In response to the Applicant’s amendments, the Examiner issued a final office action, again rejecting each of claims 1-16. Ex. 1002, 140-141. The Examiner again rejected claims 4, 9, and 13 as being indefinite. Ex. 1002, 142-143. The Examiner also rejected claims 1-8 and 12-16 as being anticipated by Lee87

(which the final office action refers to as “Lee”). Ex. 1002, 143-147. The Examiner rejected claims 9 and 10 as being obvious over Lee87 and Ker and rejected claim 11 as being obvious over Lee87 and U.S. Patent No. 5,329,185 (“Cooperman”). Ex. 1002, 148-150.

67. In response, the Applicant again amended some claims and canceled claims 4 and 13, but also added new claims 17-28. Ex. 1002, 170-180. The amendments to claims 1, 7, 9, and 10 attempted to specify various “connecting portions” being “electrically connected” to each other. Ex. 1002, 170-175. In response to the Examiner’s obviousness rejections, the Applicant argued that “the pixels of Lee cannot reasonably be considered to correspond to the claimed semiconductor circuit” and that “[o]ne of ordinary skill in the art would recognize that the pixels of Lee do not correspond to the claimed semiconductor circuit.” Ex. 1002, 182. The Applicant explained that, “[i]nstead, the driving elements 70 of Lee more reasonably could be considered to correspond to the claimed semiconductor circuit,” but “the driving elements 70 of Lee do not have the claimed first and second protection circuits arranged as recited in the claims.” Ex. 1002, 182. Because of this, the Applicant argued that “the alleged protection circuits of Lee protect pixels connected to gate lines and data lines (signal lines),” but “independent claims 1 and 7 recite wiring lines to supply power. That is, the

claimed wiring line is a power source line, not a signal line as disclosed in Lee.”

Ex. 1002, 182. The Applicant argued that the other claims were not anticipated or rendered obvious based on their dependence from claims 1 and 7. Ex. 1002, 182-183.

68. The Examiner then issued a second non-final office action on July 6, 2012, which rejected all pending claims 1-3, 5-12, and 14-18. Ex. 1002, 187. In response to the Applicant’s arguments, the Examiner stated that the “Applicant does not provide any evidence or believes [*sic*] why the pixel of Lee cannot read on the semiconductor circuit” and “Lee explicitly discloses the pixel formed by a semiconductor circuit that includes transistors and capacitors (see fig. 9).” Ex. 1002, 189. The Examiner then rejected claims 1-3, 5-8, 12, and 14-28 as being anticipated by Lee87 (which the Examiner again refers to as “Lee”). Ex. 1002, 190-198. The Examiner rejected claims 9 and 10 as being obvious over Lee87 and Ker and claim 11 as being obvious over Lee87 and Cooperman. Ex. 1002, 199-200.

69. The Applicant, in response, further amended the claims to generally replace “semiconductor circuit” with “scanning line driving circuit” and replace “wiring” line with “power supply” line. Ex. 1002, 206-217. The Applicant then attempted to distinguish Lee87 because “there is no disclosure of any first and

second protection circuits that protect the driving circuit, or the first protection circuit being electrically connected to the power supply line” between various connections along the power supply line. Ex. 1002, 219-220. The Applicant also argued that Lee87’s “lines 52 and 53 are not power supply lines, but are shorting lines connected to the diodes, which are used to dissipate the electrostatic charges” and that “shorting line 52 and 53 are not power supply lines.” Ex. 1002, 220. The Applicant also argued that Lee87 did not disclose the order of connections for the first and second protection circuits and the scanning line driving circuit. Ex. 1002, 222-224.

70. The Examiner then issued a second final office action rejecting all of the pending claims, except claims 9 and 10, as anticipated by “applicant admitted prior art” (“AAPA”) in the ’157 patent’s background or AAPA and other prior art. Ex. 1002, 228-243. The Examiner indicated that claims 9 and 10 would be allowable if rewritten in independent form. Ex. 1002, 241. The Examiner rejected the Applicant’s arguments that the driving circuit would not be connected to a power supply line and also rejected the argument that there were not two protection circuits connected to the scanning line driving circuit because both were shown in the AAPA.

71. In response to the second final office action, the Applicant amended claims 1, 2, and 5, and canceled claims 3 and 7-12, and 14-28 (claims 4 and 13 were previously canceled, as explained above). Ex. 1002, 259-262. The amendment to claim 1 recited that the “power supply line” is “one of a low power supply line and a high power supply line” and deleted that the “first protection and ... second protection circuit” “protect the scanning line driving circuit.” Claim 2 was amended to recite that the scanning line driving circuit includes a plurality of “scanning line driving unit circuits” and that a “third protection circuit” is connected to the power supply line between a first and second of the scanning line driving unit circuits, which are “adjacent to each other.” Ex. 1002, 261-262. The Applicant then attempted to distinguish the AAPA, arguing that the “AAPA does not disclose a power supply line connected to the scanning line driving circuit” because “[e]lements 750 and 751 of the AAPA are not ‘a power supply line being one of a low potential power supply line and a high potential power supply line’ but instead 751 is a high potential power supply line and 751 [*sic*: 750] is a low potential power supply line” and “750 and 751 are not connected to each other because they are different potentials.” Ex. 1002, 263-264.

72. The Examiner again rejected the claims based on AAPA. Ex. 1002, 269-275. The Examiner would then issue subsequent office actions rejecting the

Applicant's amendments based on AAPA and other prior art. Ex. 1002, 309-317, 350-361. The Applicant would continue to amend the claims and add new claims, with the thrust of the arguments reciting that the protection circuits protect the scanning line driving circuit (Ex. 1002, 298-303, 337-344) and then incorporating the limitations of claim 2 into claim 1 while the other independent claims were amended to recite that "the first protection circuit and the second protection circuit are connected to the power supply line" (Ex. 1002, 364-372). In each of these amendments and office actions, the dispute between the Examiner and Applicant focused around whether the prior art discloses the "first and second protection circuits connected to the scanning line driving circuit to protect the scanning line driving circuit or to protect the circuit element" and whether "first and second protection circuits are connected to one power supply line ('the power supply line') and to the scanning line drive circuit." *E.g.*, Ex. 1002, 373. For example, the Applicant explained that, in the AAPA, "the low potential power supply line 750 is connected to only one protection circuit ESD1" and "the high potential power supply line 751 is only connected to one protection circuit ESD2" and therefore "neither the low potential power supply line 750 nor the high potential power supply line 751 are connected to first and second protection circuits as recited in claim 1 of the application." Ex. 1002, 283; *see also* Ex. 1002, 304. The Applicant

also responded to the Examiner's obviousness rejection by stating that "the addition of the second protection circuit is not just a mere duplication of parts as asserted in the Office Action. Instead, the second protection circuit, as disclosed in the specification, provides additional ESD protection not provided by just the first protection circuit." Ex. 1002, 345; *see also* Ex. 1002, 375.

73. On April 23, 2015, the Examiner again issued a non-final office action rejecting the claims based on AAPA and U.S. Patent Application Publication No. 2005/0052384 ("Fujita"). Ex. 1002, 390-399. The Applicant argued that Fujita was not prior art because Fujita was filed in the United States on July 20, 2004, whereas the Applicant's application had a foreign priority date of July 5, 2004. Ex. 1002, 418.

74. The Examiner then issued a Notice of Allowance. Ex. 1002, 469-475. The '157 patent issued on November 11, 2015. Ex. 1002, 503.

C. Person of Ordinary Skill in the Art

75. I have been informed that patentability must be analyzed from the perspective of "one of ordinary skill in the art" ("POSITA") in the same field as the '157 patent at the time of the invention. I am also informed that several factors are considered in assessing the level of ordinary skill in the art, including (1) the types of problems encountered in the art; (2) the prior art solutions to those

problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the field.

76. In my opinion, a person of ordinary skill in the art (“POSITA”) pertinent to the ’157 patent as of its earliest priority date would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional relevant work experience can compensate for less education, and *vice versa*. For example, a master’s degree in electrical engineering, computer science, physics, or a similar field can be a substitute for two years of experience designing semiconductor display devices.

77. At the earliest priority date of the ’157 patent, I qualified as a POSITA. My analysis and opinions regarding the ’157 patent have been based on the perspective of the POSITA.

VIII. CLAIM CONSTRUCTION OF TERMS OF THE ’157 PATENT

78. As I discussed above, I have been informed that for purposes of *inter-partes* reviews, the standard for claim construction of terms within the claims of the patent is the same as that applied in federal district court litigation.

79. I have been asked to assume that the claim terms generally have their plain and ordinary meaning to a person skilled in the art in light of the specification

and the prosecution history. If the Patent Owner proposes or the Patent Board adopts a different construction, I will respond to those constructions at the appropriate time.

IX. SUMMARY OF OPINIONS ON UNPATENTABILITY

80. In my opinion, claims 1-18 of the '157 patent are unpatentable based on combinations of prior art.

A. Prior Art References

1. *Reiner*

81. International Publication No. WO03/019657 to Reiner et al. ("*Reiner*") (Ex. 1005), published March 6, 2003. I have been informed that *Reiner* is prior art to the '157 patent.

82. *Reiner* is analogous art to the '157 patent because it is directed to the same field of endeavor, in particular, semiconductor devices and display devices, and protecting semiconductor devices (e.g., driving circuits) with ESD protection circuits. Compare, e.g., *Reiner*, 2:1-3, 2:28-3:1, 4:15-16, 8:8-15, 9:12-14, 10:1-15, 12:23-25, FIG. 5, with Ex. 1001, Abstract, 1:10-13, FIG. 1. *Reiner* is also directed to at least one of the same problems as the '157 patent, for example, "integrated circuit devices with ESD protection" to prevent damage from ESD to the circuits.

Compare, e.g., Reiner, 2:1-3, 2:28-3:1, 4:15-16, 8:8-15, 9:12-14, 10:1-15, 12:23-25, FIG. 5, *with* Ex. 1001, Abstract, 1:10-13, FIG. 1.

2. *Takahara*

83. Japanese Patent Application Publication No. JP2003-121875 to Takahara (“*Takahara*”) (Ex. 1006; Ex. 1007 (translation)⁷), published April 23, 2003. I have been informed that *Takahara* is prior art to the ’157.

84. *Takahara* is analogous art to the ’157 patent because it is directed to the same field of endeavor, in particular, semiconductor devices and display devices, and protecting semiconductor devices (e.g., driving circuits) with ESD protection circuits. *Compare, e.g., Takahara*, [0003], [0057], [0066], FIG. 1, *with* Ex. 1001, Abstract, 1:10-13, FIG. 1. *Takahara* is also directed to at least one of the same problems as the ’157 patent, for example, “reliably protect[ing]” a driver circuit from “static electricity” damage. *Compare, e.g., Takahara*, [0003], [0057], [0066], FIGS. 1, 3, *with* Ex. 1001, Abstract, 1:10-13, FIG. 1.

⁷ My citations to *Takahara* are made to the English translation in Exhibit 1007.

B. Basis for Unpatentability Opinions

85. In my analysis that follows, I identify the following combinations of prior art that, in my opinion, would have rendered the claims obvious to a POSITA:

Ground	Claims	Bases
1	1-18	Obviousness based on <i>Reiner</i> (Ex. 1005)
2	1-18	Obviousness based on <i>Reiner</i> in view of <i>Takahara</i> (Ex. 1006 (original document), Ex. 1007 (translation))

X. CLAIMS 1-18 WOULD HAVE BEEN OBVIOUS TO A PERSON OF ORDINARY SKILL IN THE ART

A. Ground 1: Claims 1-18 Are Rendered Obvious by *Reiner*

86. In my opinion, *Reiner* renders obvious claims 1-18.

87. I have been requested to present my opinions related to claims 4-18 before claims 1-3. I agree with this presentation because claims 1-3 generally include similar elements to claims 4-18, but add a third protection circuit between two adjacent intermediate scanning line driving unit circuits. Therefore, discussing claims 4-18 first helps identify the distinctions between the claims by beginning with the claim with the fewest elements and then discussing the additional claim elements of claims 1-3.

1. Independent Claim 4

88. In my opinion, *Reiner* renders obvious independent claim 4.

a. [4pre]: “A display device, comprising:”

89. I have been asked to assume for purposes of this declaration that the preamble is limiting and that I should provide my opinion with respect to the preamble as well as the claim elements.⁸ In my opinion, *Reiner* discloses a display device. FIG. 4 shows a “block diagram of an LCD [liquid crystal display] display with control circuitry,” including an “LCD screen 60,” a gate driver (scanning line driver circuit) 63, source driver (data line driver circuit) 61, gate lines (scanning lines) 68, and source lines (data lines) 67. *Reiner*, 6:7, 8:12-14, 9:24-26.

⁸ I take no position on whether the preambles would be considered limiting. I do not need to do so because *Reiner* discloses the preambles of each of the claims.

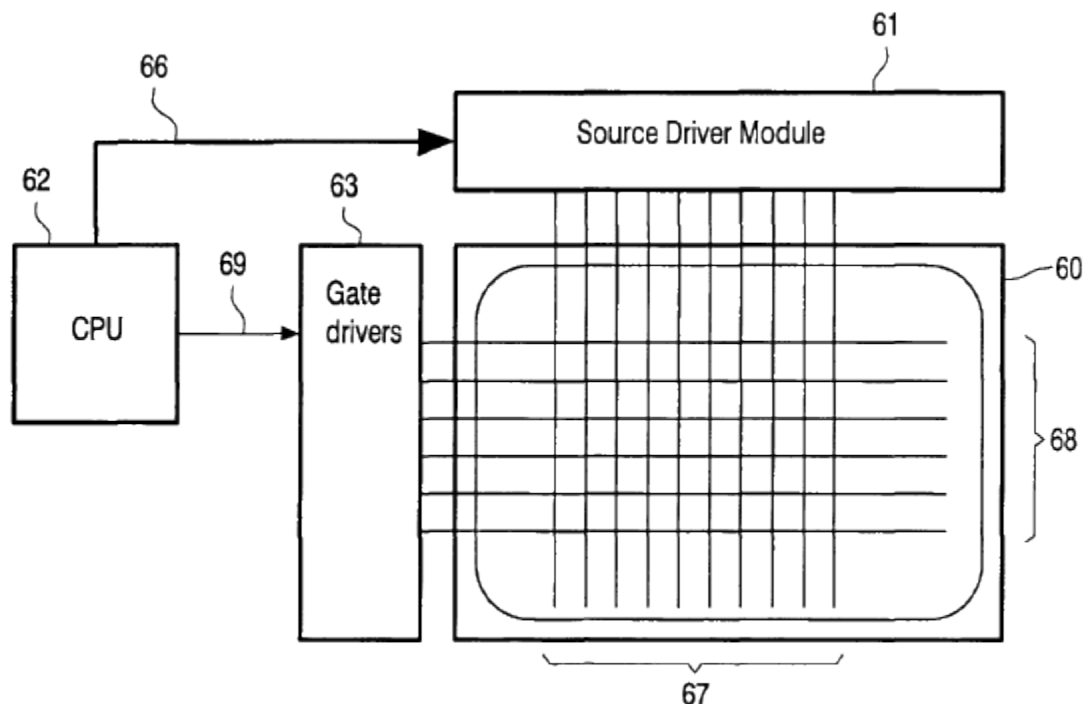


FIG. 4

Reiner, FIG. 4.⁹

b. [4a]: “a scanning line driving circuit;”

90. In my opinion, *Reiner* discloses that the LCD device includes a scanning line driving circuit. *Reiner*, 9:12-14, 9:25-31.

91. For example, *Reiner* discloses [gate driver 63](#) ([scanning line driving circuit](#)) “designed to drive many lines of an LCD display 60, as illustrated in Fig. 4.” *Reiner*, 9:11-14, 9:25-26.

⁹ All colors and colored annotations added to figures unless otherwise noted.

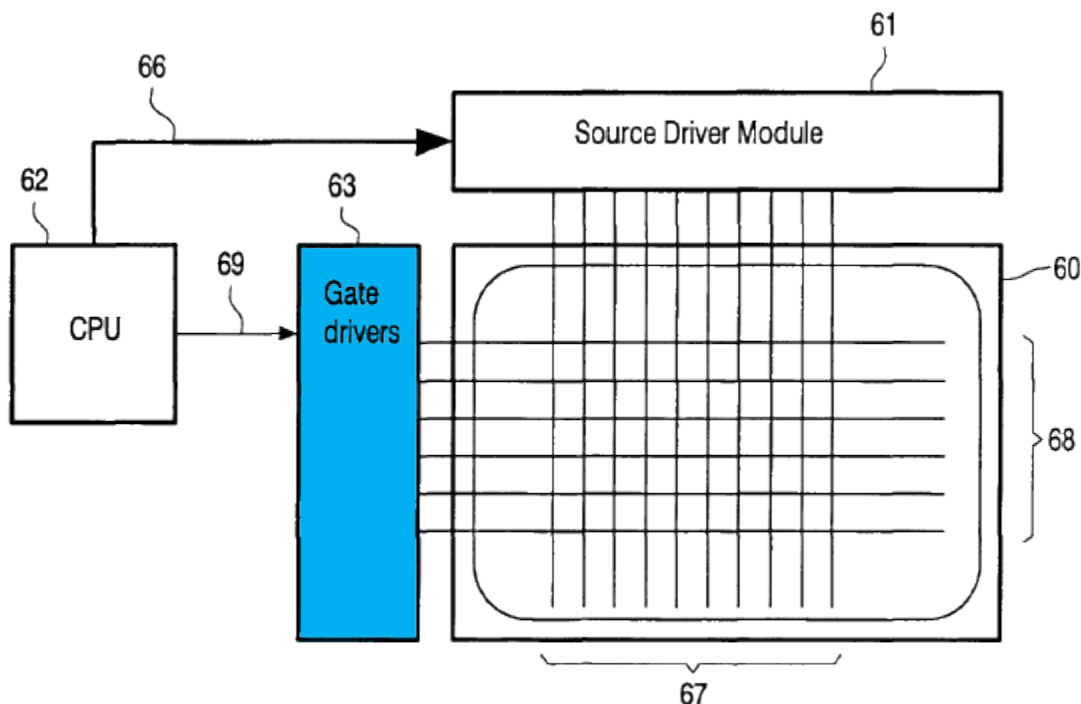


FIG. 4

Reiner, FIG. 4.

92. *Reiner*'s "LCD display comprises an LCD screen 60 with a plurality of source lines 67 and a plurality of gate lines 68." *Reiner*, 9:25-26. Gate driver 63 "usually drives one whole gate line 68" using "row timing signals (control signals)" sent "to the gate driver 63" by CPU 62 *Reiner*, 9:25-31. A POSITA, in my opinion, would have recognized that **gate driver 63** describes a scanning line driving circuit because it scans each of the horizontal lines of the LCD display using the "row timing signals." *Reiner*, 9:25-31.

- c. [4b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”

93. In my opinion, *Reiner* discloses a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line.

94. For example, *Reiner*’s teachings are “well suited for integrated circuit devices operating with two or more supply voltages (e.g., Vdd, Vee and Vss)” (power supply lines). *Reiner*, 12:4-5. A “typical example” of these “integrated circuit devices” is “an integrated circuit display driver 61 or 63” of “LCD display 60.” *Reiner*, 9:12-14. *Reiner* teaches that “many output devices of the integrated circuit device 61 or 62 [sic: 63¹⁰] ... cross the power supply lines which provide supply voltage (e.g., Vdd) to the output devices” of integrated circuits 61 and 63. *Reiner*, 9:18-22 (emphasis added). FIG. 5 shows power supply line Vdd is

¹⁰ *Reiner*’s reference to 62 is a clear typographical error because in the other instances, it refers to the gate driver as item 63. Compare *Reiner*, 9:28-31, FIG. 4, with *Reiner* 9:11-14. Similarly, *Reiner* consistently refers to the CPU as item 63. This a POSITA would have recognized that this is a clerical error and should refer to drivers 61 and 63.

connected to driver unit 70 through connection 74 and power supply line Vss is connected to driver unit 70 through connection 76, as shown below. Although *Reiner*'s FIG. 5 is an example of the source driver circuit 61, a POSITA would have recognized that it also describes gate driver 63 based on *Reiner*'s description that power supply lines Vdd and Vss are connected to source driver 61 and gate driver 63 to supply power to the individual driver output units of each of the drivers. *Reiner*, 9:18-22. Thus, *Reiner* discloses that supply lines Vdd and Vss supply power to the integrated circuit, gate driver 63's, individual driving units and thus powers each the scanning line driving unit (gate driver 63) in the same way as source driver 61.

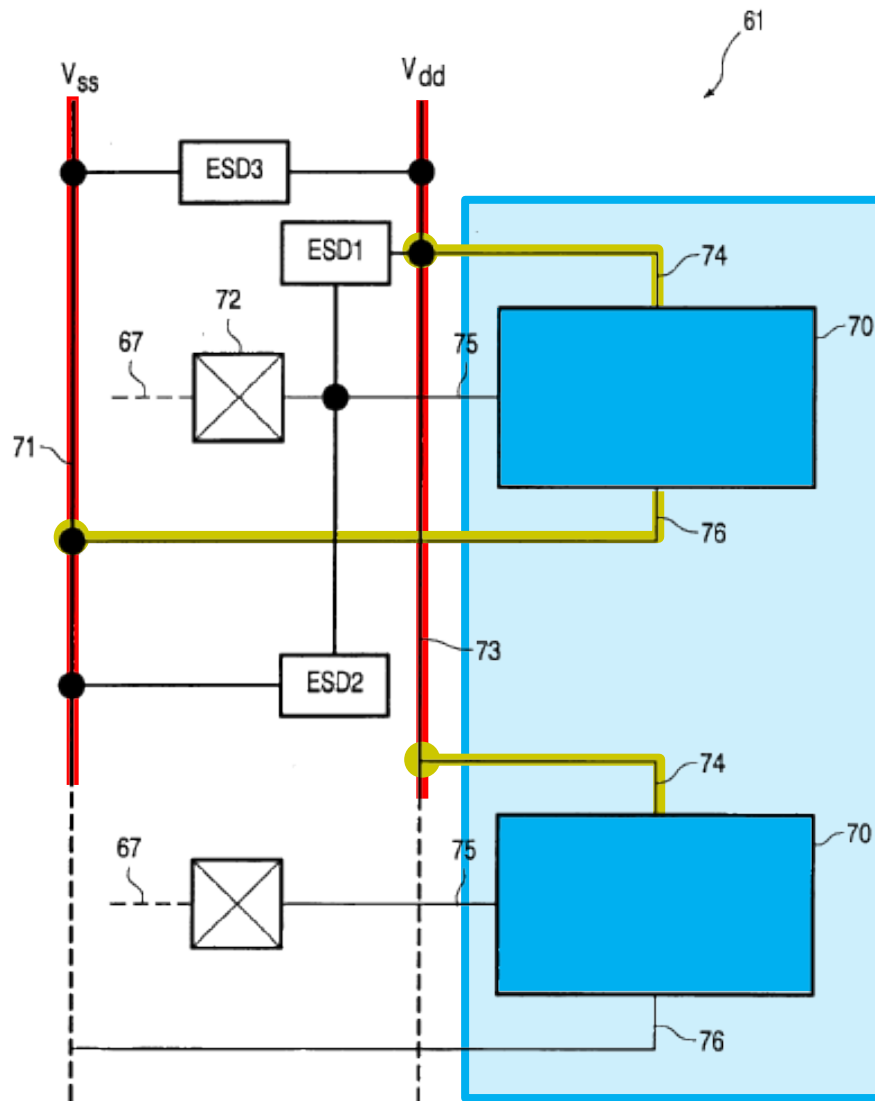


FIG. 5

Reiner, FIG. 5.

95. In my opinion, a POSITA would have recognized that Vdd and Vss are the high potential power supply line and the low potential power supply line,

respectively, because these are well-known, widely adopted, and long-used acronyms in the field.

d. [4c]: “an input terminal connected to the power supply line to supply power; and”

96. In my opinion, *Reiner* suggests or renders obvious an input terminal connected to the power supply line to supply power.

97. For at least the reasons explained for [4b], *Reiner* discloses **power supply lines** for **Vdd** and **Vss** that supply power to the integrated circuits 61 (source driver) and 63 (**gate driver** or **scanning line driver circuit**). For example, “**power supply line 73**” “*provides the supply voltage Vdd* through connection 74 to the output devices 70” of source driver 61, and a POSITA would have understood that this is exemplary and that the disclosure also applies to **gate driver 63** (**scanning line driving circuit**). *Reiner*, 10:7-8 (emphasis added). Similarly, a “second power supply line 71” “*provides the supply voltage Vss* through connection 76 to the output devices 70.” *Reiner*, 10:8-9 (emphasis added). In my opinion, a POSITA would have also understood that this description is exemplary and also applies to gate driver 63 (scanning line driving circuit), for at least the reasons explained for [4a] and [4b]. *Reiner*, 10:8-9 (emphasis added). A POSITA also would have recognized that power supply lines are needed to provide power input to the driver circuitry, which is admitted by the ’157 patent as “conventional”

in the art. *See* Ex. 1001, 1:54-56, 2:5-15, FIG. 11. *Reiner* explains that the driver units making up the gate driver 63 and the source driver 61 can be MOS transistors, such as CMOS devices, like the admitted “conventional” prior art scanning line driving circuit described in FIG. 11 of the ’157 patent. *Compare Reiner*, 2:28-3:3, 6:12-17, *with* Ex. 1001, 1:66-2:4. As such, a POSITA would have recognized that input terminals would have been connected to the power supply lines based on the conventionality in the prior art to use such terminals to power both types of driving circuits, which would not be able to function to control the display matrix without the power lines being powered.

98. In my opinion, a POSITA would have understood that the **power supply lines 73 (Vdd)** and **71 (Vss)** would require input terminals to drive the output devices 70 that form the integrated circuit 20 (which include **gate driver 63** and source driver 61) so that power can be provided from the power source to the driver units to drive the LCD display 60.

99. I have also been asked to consider the situation in which Patent Owner argues that *Reiner* does not disclose input terminals connected to the power supply line. In that case, in my opinion, a POSITA would have found it obvious to provide input terminals to supply power to power supply lines 71, 73 because it was conventional to do so and because there would need to be an input terminal to

create a connection between the power lines Vss and Vdd of the scanning line driving circuit and the power source for the LCD display.

100. For example, the '157 patent admits that FIG. 11 is “conventional art relating to the protection of the driving circuit.” Ex. 1001, 1:54-56. FIG. 11 of the '157 patent shows that the “low potential power line 750” (VS) is connected to a “low potential power terminal 650” and the “high potential power line 751” (VD) is connected to a “high potential power terminal 651.” Ex. 1001, 2:8-10. The '157 patent describes “the low potential power terminal 650 and the high potential power terminal 651 [being] connected to a power IC” and being “supplied with reference potentials of a potential VS and a potential VD.” Ex. 1001, 2:10-14. VS and VD respectively describe *Reiner's* Vss and Vdd power supply lines. Ex. 1001, 2:8-14. In my opinion, a POSITA would have found it obvious, indeed would have understood that it was “conventional” as admitted by the '157 patent and therefore found it obvious to provide input terminals to supply the voltages Vss and Vdd to *Reiner's* power supply lines of the gate driver 63. A POSITA would have generally recognized that the configuration in FIG. 5 would have had the input terminals above the first ESD3, as I show below in the figures in [4d]-[4f], and was conventional in the prior art, as I explain above in Section VI.

i. Motivation

101. A POSITA would, in my opinion, have been motivated to provide respective input terminals connected to each of *Reiner*'s power supply lines 71 (Vss) and 73 (Vdd) because the terminals would be needed to transfer power from a wiring line from the power source to the lines of the gate driver 63 to "drive [the] many lines of ... LCD display 60" to display images on the LCD display. *Reiner*, 9:12-14. A POSITA would have recognized that *Reiner*'s integrated circuits, such as gate driver 63, can be fabricated and then attached to a substrate by being "flipped onto the substrate 16[] according to the well-known flip-chip technology" and therefore there would need to be input terminal power connections to the substrate because the wiring lines for the display 60 often run along the substrate, such as shown in FIG. 1 of *Takahara*. *Reiner*, 7:23-25; *Takahara*, [0063], [0066], FIG. 1 (power supply lines VSSY, VDDY have input terminals 800, 802 for driving scan-line drive circuit 104); *see also* Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751) (acknowledging that "conventional art" related to protecting driving circuits used input terminals to supply power via power lines). A POSITA would have been motivated to provide input terminals connected to the power supply lines to supply power to *Reiner*'s gate driver 63 to ensure proper electrical connections with the power supply and to facilitate manufacturing to

connect the power supply lines supplying the gate driver 63 with the corresponding power source or with the power supply lines of the substrate on which the LCD display is arranged.

ii. Expectation of Success

102. In my opinion, a POSITA would have reasonably expected to succeed in providing input terminals connected to *Reiner*'s power supply lines Vss 61 and Vdd 63 to supply power to the gate driver 63 (scanning line driving circuit). The use of input terminals connected to *Reiner*'s power supply lines for scanning line driving circuits was admittedly part of the "conventional art" to provide ESD protection for driving circuits of LCD displays that both *Reiner* and the '157 patent describe. *Reiner*, 9:18-20; Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751) (acknowledging that "conventional art" related to protecting driving circuits used input terminals to supply power via power lines); *see also Takahara*, [0063], [0066], FIG. 1 (power supply lines VSSY, VDDY having input terminals 800, 802 for driving scan-line drive circuit 104). Implementing this would have required only the application of ordinary skill in the art because every LCD device would have required a connection to get power to the power supply lines of the scanning line driving circuit so that the individual driver units (e.g., output devices 70) that make up the scanning line driver circuit can drive each of the gate/scan lines and

the display pixels can then be illuminated. Using input terminals connected to respective power supply lines, such as *Reiner*'s Vss 71 and Vdd 73, to supply power to the power supply lines would have been merely the straightforward application of known, conventional techniques applied to *Reiner*'s already-disclosed power supply lines Vss 71, Vdd 73 used according to their known functions to yield predictable results (providing a connection through which power flows to the power supply lines to power the gate driver 63 so that it can scan and drive gate lines 68). *See Reiner*, 9:12-13, 9:18-20, 9:27-29, 10:6-10, 12:4-5.

- e. **[4d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,”**

103. In my opinion, *Reiner* discloses or renders obvious a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line.

104. As I explain in [4b], *Reiner* “relates to *integrated circuit devices* with ESD protection.” *Reiner*, 2:2-3, 4:15-16 (“It is an object of the present invention to provide a scheme that allows to add an ESD protection network to densely packed integrated circuit devices.”) (emphasis added). A “typical example is an [integrated](#)

circuit display driver 61 or 63” in *Reiner*. *Reiner*, 9:12-14, 12:4-5 (emphasis added). *Reiner* generally discloses that its teachings are “well suited for integrated circuit devices operating with two or more supply voltages (e.g., Vdd, Vee and Vss)” (power supply lines). *Reiner*, 12:4-5. *Reiner* also explains that its disclosure has “advantages” of being “well suited for conducting currents occurring during ESD events” and “avoid[ing] thermal damage caused by high current during an ESD event.” *Reiner*, 12:23-25, *see also Reiner*, 8:8-15 (“The present invention is well suited for use in integrated circuit devices, such as CMOS devices for example, that comprise an electrostatic discharge device (ESD) protection.”). *Reiner* continues that, “[q]uite often *integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection* in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1 (emphases added).

105. *Reiner*’s FIG. 5 shows a “schematic block diagram of a display driver 61” where “ESD protection means can easily be integrated into such a display driver 61.” *Reiner*, 9:20-22. This statement in *Reiner* ends a paragraph that more generally discusses “integrated circuit display driver 61 or 63” and “display driver 61, 63,” thus confirming that both the source driver 61 and the gate driver 63 are “display drivers” to be protected from ESD events. *Reiner*, 9:11-22 (emphases

added). Indeed, a POSITA would have understood that *Reiner* generally describes the protection of “integrated circuits,” which *Reiner* makes clear can be either gate driver 63 or source driver 61. As such, a POSITA would have understood that FIG. 5 describes source driver 61 as exemplary and that FIG. 5’s teachings apply equally to **gate driver 63 (scanning line driving circuit)** because gate driver 63 is also a “driver display circuit.” Indeed, *Reiner*’s explanation that “[q]uite often, integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event” does not differentiate between the source driver 61 and the gate driver 63, thus teaching, or at least suggesting, that both integrated driver circuits would be protected in a similar manner. *Reiner*, 2:28-3:1.

106. In *Reiner*’s FIG. 5, “three ESD devices ESD1, ESD2, and ESD3 are provided for each output device 70, *in order to protect the circuitry inside the devices 70.*” *Reiner*, 10:10-12 (emphasis added). More specifically, because “three ESD devices” are “provided for *each* output device 70,” a POSITA would have understood that each line driver unit would have its own ESD protection, as shown

in the composite FIGS. A1-C1¹¹ below. *Reiner* also explains that the other end of the ESD can be connected to “a ground terminal” to protect against “a voltage peak” on a power line or output line. *Reiner*, 10:15-17.

¹¹ To avoid confusion with *Reiner*’s original figures, figures created for this declaration showing *Reiner*’s teaching are identified by letter rather than number. For example, FIGS. A1-C1 (and similar figures below) show portions of a gate driver 63 with the ESD protection networks “for each output device 70, in order to protect the circuitry inside the devices 70.” *Reiner*, 10:10-12. I discuss three scenarios for the challenged claims. However, because each output device 70 has three corresponding ESD devices, there would be hundreds of ESD devices in *Reiner*’s driver circuits and therefore many ways to read them on the limitations of the claims. I present only three of these many alternatives. The first mapping is identified as Ax throughout this declaration, the second as Bx, and the third as Cx, so that they can be consistently compared. Where I include general discussions not specifically identifying one of the alternatives Ax, Bx, or Cx, then the discussion applies to all three alternatives, such as when I discuss why the claims would have been obvious to a POSITA.

107. FIGS. A1-C1 show three alternative mappings of [4d]. FIGS. A1-C1 show the first three and last two gate driver line-driving units 70,¹² omitting the other intermediate driver units for scan lines 68. But a POSITA would have recognized that there would be as many gate driver line-driving units 70 as there are scanning lines 68 in LCD display 60.

108. As shown in FIG. A1, the first ESD1 protection circuit at the first driver unit of gate driver 63 (closest to the input terminals) and the second ESD1 protection circuit at the last gate driver unit (farthest from the input terminals) are connected to the line driving units 70 of the gate driver 63 through output line 75 “in order to protect the circuitry inside the devices” and also connected to the power supply line Vdd. See *Reiner*, 10:1-15.

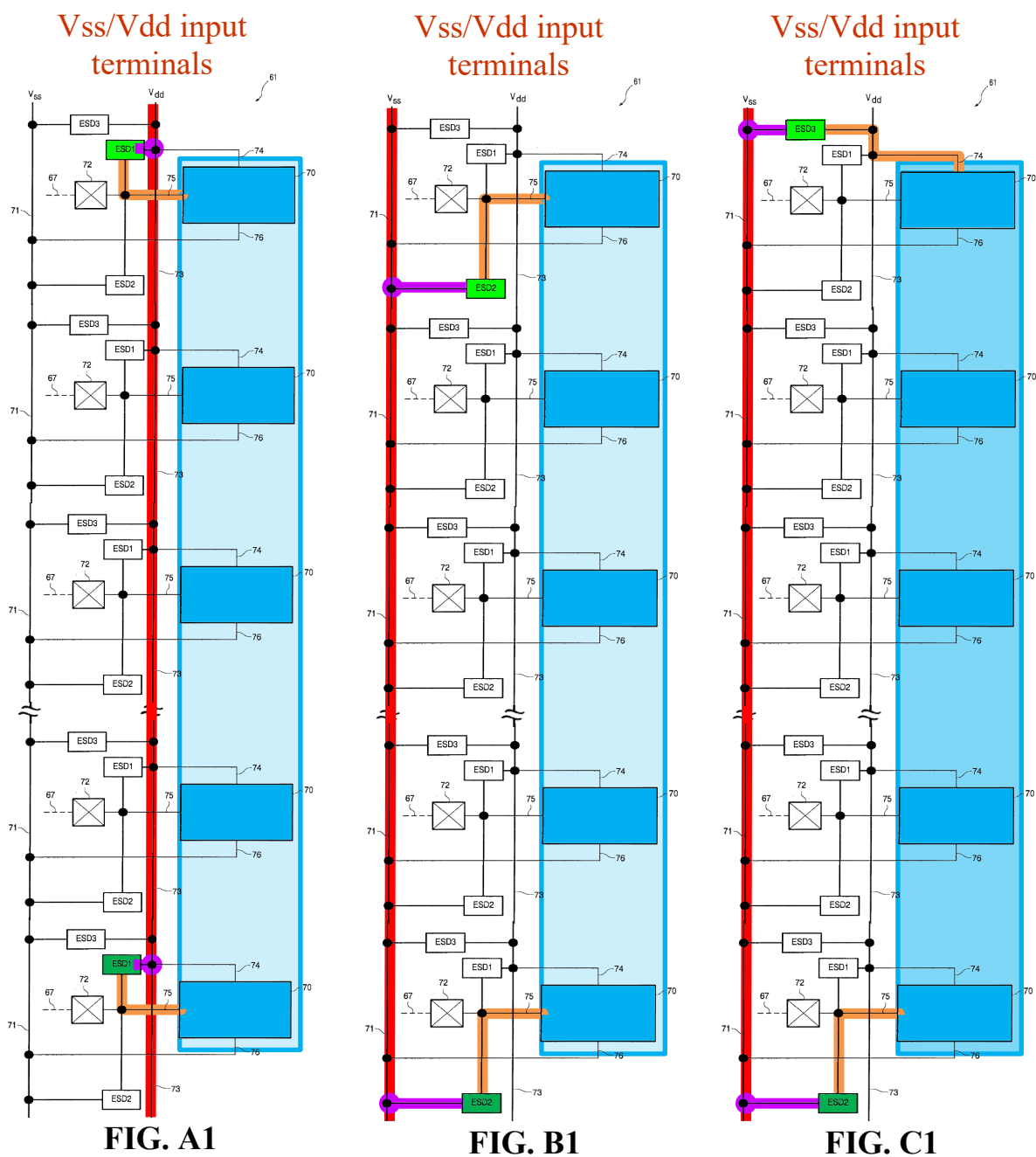
109. As shown in FIG. B1, the first ESD2 protection circuit at the first driver unit of gate driver 63 (closest to the input terminals) and the second ESD2 protection circuit at the last gate driver unit (farthest from the input terminals) are

¹² For ease of reference, because output device 70 is shown as a generic box and would have been understood to represent the gate driving circuitry when circuit element 20 is a gate driver 63, my references to the output devices of the gate driver 63 retains the same numbering as FIG. 5.

connected to the line driving units of the gate driver 63 through output line 75 “in order to protect the circuitry inside the devices” and also connected to the power supply line Vss. See *Reiner*, 10:1-15.

110. I have also been asked to consider the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines.¹³ As shown in FIG. C1, the first protection circuit ESD3 before the first driver unit of the gate driver 63 (closest to the input terminals) and the second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) are connected to the line driving units of the gate driver 63 “to protect the circuitry inside the devices” and also connected to the power supply line Vss on either side of the gate driver 63. See *Reiner*, 10:1-15.

¹³ I express no opinion on the correctness of this.



111. Thus, *Reiner* explains that ESD1, ESD2, and ESD3 protect the drive circuitry at each line driver unit 70, which together form the gate driver 63 and thus the gate driver 63 is protected. *Reiner*, 10:10-15. In FIG. 5, as shown below,

driver “output devices 70” are shown as ‘black box’ elements. These boxes 70 do not show the internal circuitry, and a POSITA would have recognized that the ESD protection network protects any driver circuitry in that box and that the protection provided applies equally to both source driver 61 and the gate driver 63, especially in light of *Reiner*’s discussions that both drivers are “integrated circuits” that *Reiner* discloses need protecting from electrostatic damage because they contain “very sensitive circuits” that are easily damaged. *See Reiner*, 2:28-3:1, 4:15-16, 9:11-22. As such, a POSITA would have understood that *Reiner*’s description of ESD protection in FIG. 5 also applies to gate driver 63 and that the ESD protection shown in FIG. 5 would have protected [gate driver 63](#), where each of output devices 70 (together the gate driver 63) comprises the line-driving circuitry for driving each scan line 68.

112. I have also been asked to consider the situation in which Patent Owner argues that *Reiner* does not disclose [4d]. In that case, in my opinion, *Reiner* would have rendered it obvious to a POSITA. For at least the reasons explained above, *Reiner* “relates to *integrated circuit devices* with ESD protection” and generally “provide[s] a scheme that allows to *add an ESD protection network* to densely packed *integrated circuit devices*.” *Reiner*, 2:2-3, 4:15-16 (emphases added). Thus, *Reiner* describes protecting integrated circuits generally using ESD protection

devices. Because *Reiner* teaches that a “typical example” of a protected integrated circuit “is an **integrated circuit display driver 61 or 63**,” a POSITA would have found it obvious to protect the **gate driver 63 (scanning line driving circuit)** with the same ESD protection network as the source driver 61 described in the example of FIG. 5. *Reiner*, 9:12-14, 12:4-5 (emphasis added). *Reiner* generally describes protecting integrated circuits and both gate drivers (scanning line driving circuits) and source drivers (data line driving circuits) are types of integrated circuits that are usually comprised of various circuit elements, such as transistors, that receive power and other signals, such as clock or data signals.

113. As explained by *Reiner*, the transistors in these driving circuits can be MOS (metal oxide semiconductor) transistors or other types of transistors that are used to provide the driving signal for each of the gate lines (scan lines) or source lines (data lines). That is, each of the lines being driven will have its own semiconductor units (e.g., *Reiner*’s output devices 70) to drive that particular line. The collection of each of the line drivers for the scan lines or data lines forms the entire driving circuit for either the gate driver 62 or the source driver 61, respectively. In my opinion, a POSITA would have recognized that the similarities in the driving circuits, such as both having transistor elements in the line driving units, and *Reiner*’s warning that both driver circuits contain “very sensitive

circuits” that can be “destroyed” by ESD, would have lent itself to protecting both the source driver 61 and the gate driver 63. A POSITA also would have been cognizant that *Reiner*’s ESD protection network of FIG. 5 has several benefits, including being effective for “densely packed” driver circuits, protecting against both electrical and thermal ESD damage, and being compatible with manufacturing methods that have only a single metal layer (which could lower the cost of producing the driver circuits). Given these benefits (although the same motivation would apply for either or both benefit) and the similarities of the gate and source drivers themselves, a POSITA would have found it obvious to protect *Reiner*’s gate driver 63 using the same type of ESD protection network described for the source driver 61 in FIG. 5.

114. In my opinion, a POSITA would have found this obvious because it would have also protected the gate driver 63 from being damaged by ESD events that could “destroy[]” the “very sensitive circuits” of the gate driver, which could render the display unacceptable. Such damage can be either thermal or electrical and *Reiner* explains that its ESD protection would have protected against both types of damage. *Reiner*, 2:28-3:1, 12:24-25. As such, a POSITA would have been further motivated to implement *Reiner*’s ESD protection network in gate driver 63 to prevent damage to any part of the circuit.

i. Motivation

115. A POSITA would, in my opinion, have been motivated to provide a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit from ESD events and damage and also connected to the power supply line Vss and/or Vdd that can be subject to ESD events, such as when a chip's pins are touched. *Reiner*, 3:2-3; *see also* Ex. 1001, 1:14-19 (confirming the importance of protecting against ESD events was conventional in the prior art). A POSITA would have recognized that *Reiner*'s integrated circuits, whether source driver 61 or gate driver 63, are at risk of ESD damage because the metal lines can conduct static electricity that “destroy[s]” the “very sensitive circuits” in the driver modules. *Reiner*, 2:28-3:1. For example, *Reiner* recognizes, as was conventional in the art, that driver circuits, whether a source driver 61 or a gate driver 63, contain transistors and other circuit elements that can be damaged by ESD events. *Reiner*, 6:12-17, 8:30-31 (“The transistor 31 is in the present embodiment part of an outputs stage [output device 70] of the integrated circuit device 30.”). A POSITA would have been motivated, as explained by *Reiner*, to “protect the circuitry” of each of the output devices of the gate driver 63 in the same way as source driver 61 to prevent the sensitive circuits from being damaged by ESD events occurring on either of the voltage lines

V_{SS} and V_{DD} or on the output line from the gate driver (the equivalent of output line 75 of the source driver 61). *Reiner*, 10:10-12. For example, a POSITA would have been motivated to provide ESD protection circuits for the gate driver 63 because a POSITA would have wanted to protect both driver circuits because an LCD display can be rendered unacceptably or irreparably damaged if either the gate driver (scanning line driving circuit) or the source driver (data line driving circuit) is damaged by ESD because damage to either driver prevents impairing activating parts of the screen, such as pixel rows or columns of the LCD screen.

116. In my opinion, a POSITA would have also been motivated to protect *Reiner*'s gate driver 63 with ESD protection like that shown in FIG. 5 because it "allows ... add[ing] an ESD protection network to densely packed integrated circuit devices." *Reiner*, 4:15-16. A POSITA would have recognized that the risk of ESD damage (both electric and thermal) is heightened for densely packed integrated circuits, such as *Reiner*'s gate driver 63, because they contain "very sensitive" circuit elements that would be close together and thus more of the individual driver units making up the gate driver 63 would be susceptible to ESD damage. *Reiner*, 2:28-3:1, 4:15-16.

117. A POSITA would have also recognized that implementing the "ESD protection network" of *Reiner*'s FIG. 5 in gate driver 63 protect "each output

device” of the gate driver 63 (the driver unit equivalent to output device 70 for each scan line) because it represents merely implementing the known prior art ESD protection network of *Reiner* in *Reiner*’s gate driver 63 to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s]” of gate driver 63. *Reiner*, 4:15-16, 10:10-12. Similarly, a POSITA would have been motivated to implement *Reiner*’s known ESD protection network to improve the similar gate driver 63 in the same way as the example shown in FIG. 5 because the ESD protection network protects the output circuit in box 70, which could be either a source driver or gate driver because they have similar configurations and both need protection from ESD events. *See Reiner*, 2:28-3:1. At a minimum, in my opinion, a POSITA would have found it obvious to try implementing *Reiner*’s ESD protection network shown in FIG. 5 to protect the scan line driver units (output device) of gate driver 63 and thereby protect the gate driver 63, given *Reiner*’s teaching that both source driver 61 and gate driver 63 are “integrated circuits” and contain “very sensitive circuits” that can be “destroyed when ... subjected to [an ESD] discharge event” and, therefore, need protecting. *Reiner*, 2:28-3:1, 9:12-14.

118. A POSITA also would have been motivated to implement a first and second ESD protection circuit connected to *Reiner*’s gate driver 63 to protect the gate driver 63 from electrical and thermal ESD damage, and also connected to the

power supply line, such as Vss and/or Vdd, because the configuration described in *Reiner* would have protected the “densely packed integrated circuits” within the gate driver 63. A POSITA also would have been motivated to implement *Reiner*’s ESD protection network because the configuration would also reduce fabrication costs because it could use a single metal layer and would have made the integrated circuit chip less bulky. *Reiner*, 4:10-12, 4:15-19, 9:16-22, 10:15-17, 12:15-18, claim 11 (describing using ESD protection on an “integrated circuit device (20)” generically).

119. A POSITA would also have been motivated to implement the ESD protection network to protect gate driver 63 to prevent damage to the sensitive line driver circuitry and “realize more densely packed integrated circuit devices” and thereby reduce the risk of damage from ESD events, and reduce fabrication costs. *Reiner*, 4:15-19, 12:16-18. A POSITA also would have recognized that because *Reiner*’s gate driver 63 and source driver 61 include contact pads 72 for bonding the driver to a substrate, that static charge could also enter the circuits through the contact pads 72, and that ESD2 and ESD3 would protect the circuitry inside of the drivers (e.g., would protect each of the driver output devices 70) from static charges, in addition to protecting the drivers from static charges accumulating on the power lines Vdd and Vss.

ii. Expectation of Success

120. In my opinion, a POSITA would have reasonably expected to succeed in implementing the ESD protection network of *Reiner*'s FIG. 5 to protect gate driver 63 (scanning line driving circuit), which would have connected the first and second protection circuits to the scanning line driving unit to protect the scanning line driving unit and the power supply line(s). The use of ESD circuits to protect *Reiner*'s scanning line driving circuit was admittedly part of the "conventional art" for preventing ESD damage. *Reiner*, 7:23-25; Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751) (acknowledging that "conventional art" related to protecting driving circuits); *see also Takahara*, [0066], FIG. 1 (describing using electrostatic protective circuits 150, 151 to protect the scanning line driving circuit from static electricity). Using a first protection circuit and a second protection circuit connected to the gate driver 63 (scanning line driving circuit) to protect the scanning line driving circuit, and also connected to the power supply line (either Vss 71, Vdd 73), such as in the configuration of *Reiner*'s FIG. 5, would have been merely the straightforward application of known, conventional techniques using *Reiner*'s already-disclosed ESD protection network to protect the driver units of gate driver 63 (which are similar to driver units 70) according to their known functions to yield predictable results (protecting the line driver units of gate driver

63 and thereby protecting gate driver 63). *See Reiner*, 2:28-3:1, 3:4-8, 3:15-16, 8:8-15, 8:18-20, 8:30-33, 9:12-22, 10:1:17, 12:22-25.

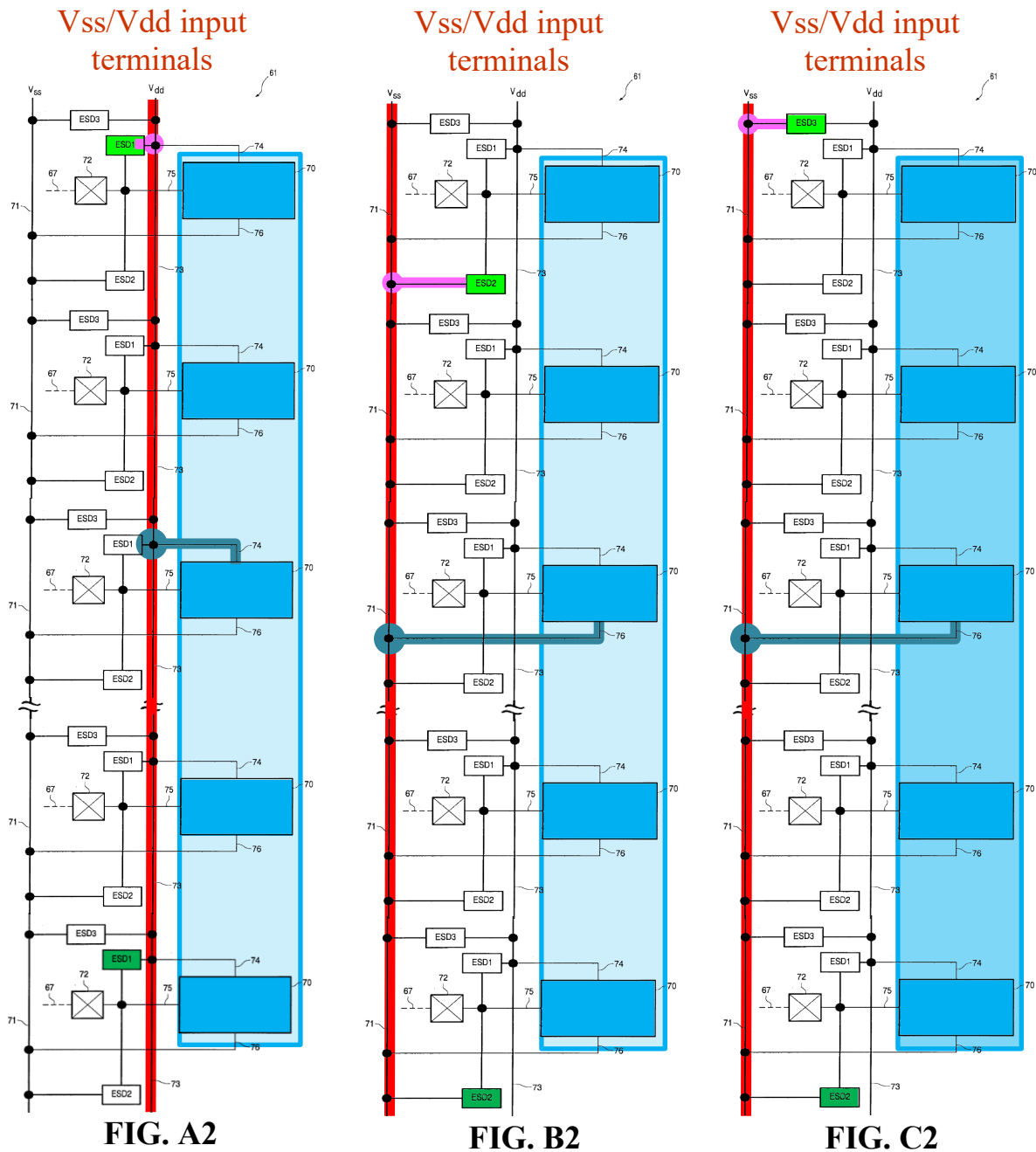
- f. [4e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and”

121. In my opinion, *Reiner* discloses or renders obvious the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal. This is shown in each of the alternative mappings Ax, Bx, and Cx discussed in this declaration.

122. As I explain in [4d], *Reiner* discloses or a POSITA would have found it obvious to implement *Reiner*’s ESD protection network providing ESD1-ESD3 “for each output device” driving each scan line, such as shown in FIG. 5, “to protect the circuitry inside the [output] devices” of gate driver 63 (scanning line driving circuit). *Reiner*, 10:10-12; *supra* § X.A.1.e (FIGS. A1-C1).

123. When protecting the gate driver 63 in this way, the first protection circuit is connected to the power supply line (e.g., Vdd, Vss) between (i) a first connecting portion at which the gate driver 63 and the power supply line are connected and (ii) the input terminal supplying power to the power supply line, for

example, as described below and shown in FIGS. A2-C2. The '157 patent does not use the term “connecting portion,” except in the claims. A POSITA, however, would recognize that a scanning line driving circuit, such as *Reiner*'s gate driver 63 or the '157 patent's scanning line driving circuit 800, is connected to **power supply lines Vdd and Vss** at each driver unit, such as *Reiner*'s units 70 or the '157 patent's units 801-n, at each of the connections 74 or 76. This is confirmed by the '157 patent, which explains that, “[m]ost preferably, the protective circuits are interposed between all stages if there is no problem in the circuit area.” Ex. 1001, 7:46-47. As such, I identify one connecting portion between the gate driver 63 and the power line below, but there are others at the other driver units 70 that could be identified instead. As I explain elsewhere in this declaration, claim 4 does not recite which of the ESD protection circuits in this embodiment would constitute the first and second protection circuits, any of them could, so long as they have the appropriate relative positions along the power line recited in elements [4d]-[4f]. This is true for all three of my examples in FIGS. Ax, Bx, and Cx. Indeed, this “most preferabl[e]” example from the '157 patent is practically the same as *Reiner*'s ESD protection network that is “provided for each output device 70.” *Reiner*, 10:10-15.



124. As shown above in FIG. A2, for example, the first protection circuit ESD1 at the first gate driver unit of gate driver 63 closest to the input terminals is

connected to the power supply line Vdd between (i) a first connecting portion at which the gate driver 63 and the power supply line Vdd are connected at line 74 and (ii) the input terminal supplying power to the power supply line Vdd.

125. Similarly, as shown above in FIG. B2, for example, the first protection circuit ESD2 at the first gate driver unit of gate driver 63 closest to the input terminals is connected to the power supply line Vss between (i) a first connecting portion at which the gate driver 63 and the power supply line Vss are connected at line 76 and (ii) the input terminal supplying power to the power supply line Vss.

126. And, when considering the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines, as shown above in FIG. C2, for example, the first protection circuit ESD3 before the first driver unit of the gate driver 63 closest to the input terminals is connected to the power supply line Vss between (i) a first connecting portion where the gate driver 63 and the power supply line Vss are connected at line 76 and (ii) the input terminal supplying power to the power supply line Vss. *Reiner*, 10:1-15.

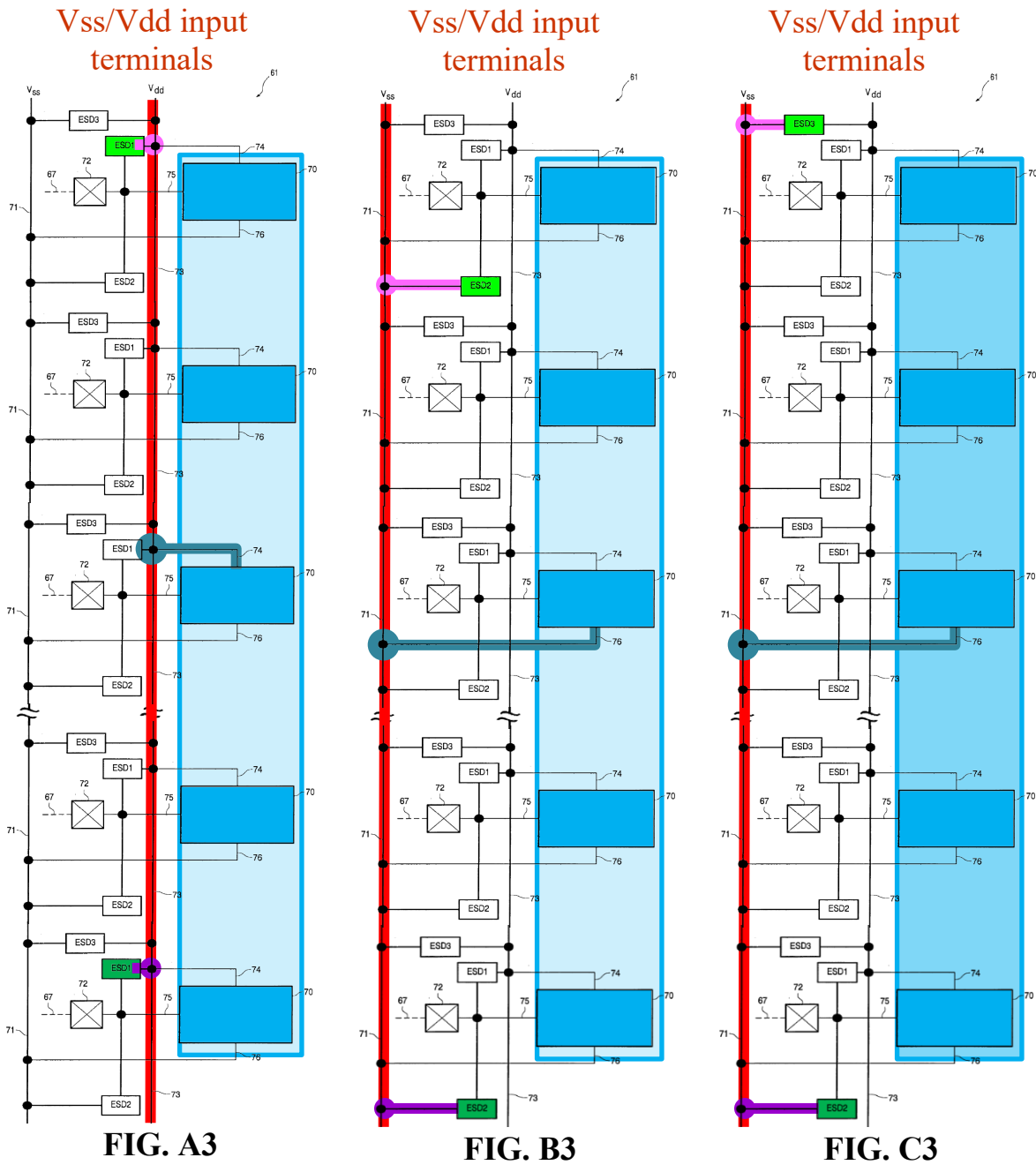
- g. [4f]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

127. In my opinion, *Reiner* discloses or renders obvious the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected. This is shown in each of the alternative mappings Ax, Bx, and Cx discussed in this declaration.

128. As I explain in [4d], *Reiner* discloses or a POSITA would have found it obvious to implement *Reiner*'s ESD protection network, such as shown in FIG. 5, to protect the gate driver 63 (scanning line driving circuit), including providing ESD1-ESD3 “for each output device” driving each scan line “to protect the circuitry inside the [output] devices.” *Reiner*, 10:10-12; *supra* § X.A.1.e (FIGS. A1-C1). As also explained in [4e], this protection configuration would have included the first protection circuit being connected to the power supply line (e.g., Vdd or Vss) between (i) a first connecting portion at which the gate driver 63 and

the power supply line are connected and (ii) the input terminal supplying power to the power supply line. *Supra* § X.A.1.f.

129. *Reiner* provides an ESD protection network with “three ESD devices ESD1, ESD2, and ESD3 ... for each output device 70, in order to protect the circuitry inside the devices 70,” which, when applied to the gate driver 63 (scanning line driving circuit), would have included the gate driver 63 (scanning line driving circuit) being connected to the power supply line (e.g., Vdd, Vss) (such as described in [4e]) between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected (also described in [4e]) and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected, for example, as described below and shown in FIGS. A3-C3. Furthermore, as I explain above in [4e], in the three alternative mappings that I discuss in this declaration, although I show one particular connecting portion between the gate driver 63 and a power line in FIGS. A3-C3, the gate driver 63 is connected to the power lines Vdd or Vss at each of the connections at lines 74 or 76, and thus the mapping below (or in [4e]) could be adjusted to identify any one of such connections.



130. As shown above in FIG. A3, for example, the gate driver 63 (scanning line driving circuit) is connected to the power supply line Vdd (such as described in [4e], FIG. A2) between (iii) a second connecting portion at which the first

protection circuit ESD1 at the first gate driver unit of gate driver 63 (closest to the input terminals) and the power supply line Vdd are connected (also described in [4e], FIG. A2) and (iv) a third connecting portion at which the second protection circuit ESD1 at the last gate driver unit of gate driver 63 (farthest from the input terminals) and the power supply line Vdd are connected. See Reiner, 10:1-15.

131. Similarly, as shown above in FIG. B3, for example, the gate driver 63 (scanning line driving circuit) is connected to the power supply line Vss (such as described in [4e], FIG. B2) between (iii) a second connecting portion at which the first protection circuit ESD2 at the first gate driver unit of gate driver 63 (closest to the input terminals) and the power supply line Vss are connected (also described in [4e], FIG. B2) and (iv) a third connecting portion at which the second protection circuit ESD2 at the last gate driver unit of gate driver 63 (farthest from the input terminals) and the power supply line Vss are connected. See Reiner, 10:1-15.

132. And, when considering the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines, as shown above in FIG. C3, for example, the gate driver 63 is connected to power supply line Vss (see [4e], FIG. C2) between (iii) a second connecting portion where the first protection circuit ESD3 before the first gate driver unit (on the side closest to the input terminals) and the power supply line Vss are connected (see [4e],

FIG. C2) and (iv) a **third connecting portion** where the **second protection circuit ESD2** at the **last gate driver unit** (farthest from the **input terminals**) and **power supply line Vss** are connected on the side of the **gate driver 63** farthest from the input terminals. *See Reiner*, 10:1-15. That is, in each of FIGS. A3-C3, a connection between the scanning line driving circuit and the power supply line is between the connections between the protection circuits and the power supply line.

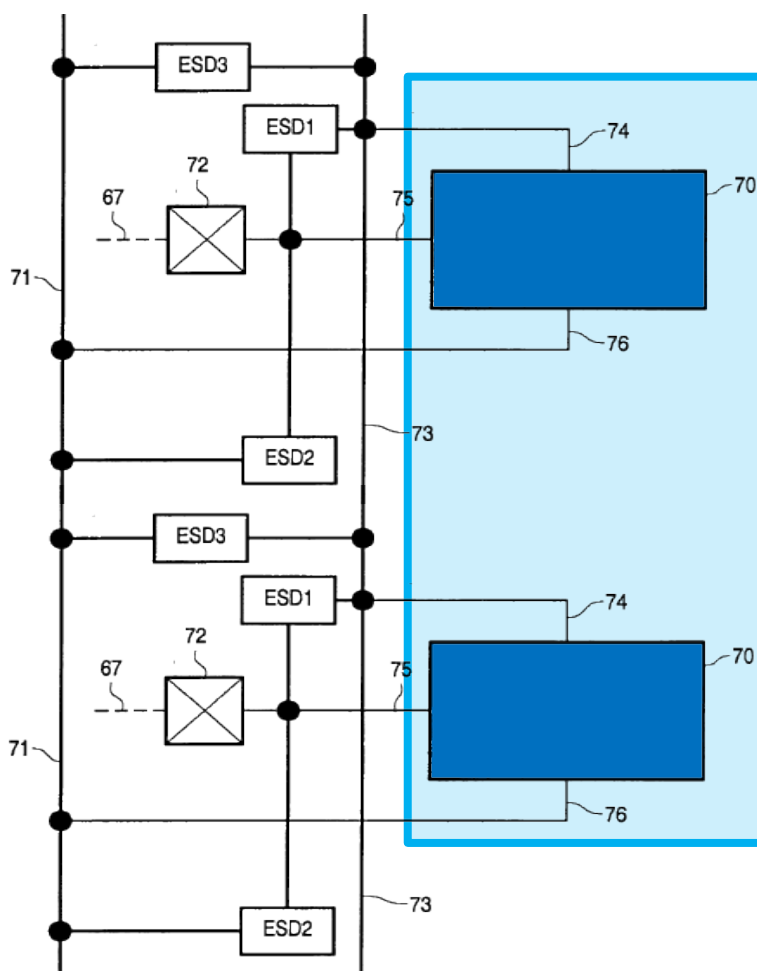
133. In my opinion, for at least the reasons explained above, *Reiner* thus renders obvious claim 4.

2. Claim 5

- a. **“The display device as set forth in claim 4, further comprising: a scanning line driving unit circuit included in the scanning line driving circuit.”**

134. In my opinion, *Reiner* discloses or renders obvious a scanning line driving unit circuit included in the scanning line driving circuit.

135. As I explain in [4d], *Reiner* teaches individual **gate-line driving units 70** (**scanning line driving unit circuits**) being included in **gate driver 63** (**scanning line driving circuit**) for driving each gate line 68, like that shown in FIG. 5.



Reiner, FIG. 5.

136. For example, *Reiner* discloses that the “integrated circuits,” such as gate driver 63, may comprise “a plurality of integrated devices [22],” such as transistors. *Reiner*, 6:12-17, 6:18-21 (“an integrated circuit device 20” comprises “at least one integrated device 22 (e.g., a transistor)”), 8:18-20 (“integrated circuit device 30 ... comprises a plurality of integrated devices”). *Reiner* explains that “integrated circuit display driver 61 or 63 ... is designed to drive many lines of an

LCD display 60” and each of “display driver 61, 63 typically has a large number of parallel outputs” and “many output devices” connected to the lines being driven.

Reiner, 9:11-22. And, *Reiner*’s teachings “allow [the] many output devices of” gate driver 63 to supply power to the output devices to drive the gate or scan lines.

Reiner, 9:18-20.

137. I have also been asked to consider the situation in which Patent Owner argues that *Reiner* does not expressly disclose the gate driver 63 having driver output devices 70. In my opinion, a POSITA would have found this obvious, at least for the reasons discussed above in claim 4, because *Reiner* discloses that the gate driver 63 includes “an integrated circuit display driver ... 63 that is designed to drive many lines of an LCD display 60,” and that the driver 63 has “a large number of parallel outputs” that include “output devices” that receive power from the power lines. *Reiner*, 9:11-15; *supra* § X.A.1.

3. Claim 6

- a. “The display device as set forth in claim 4, further comprising: a buffer circuit included in the scanning line driving circuit.”**

138. In my opinion, *Reiner* discloses or renders obvious a buffer circuit included in the scanning line driving circuit.

139. For example, *Reiner* discloses that “[e]ach output device 70 of a source driver module 61, for example, may comprise a digital-to-analog (D/A) converter, a buffer as well as other devices. The buffers drive the source lines 67 with the voltages needed by each pixel of the LCD screen 60.” *Reiner*, 10:1-3. For at least the reasons explained above for claim 4, a POSITA would have understood, or at least found it obvious, that the driver circuitry for [gate driver 63](#) to drive gate line 68 would have included similar circuit elements to source driver 61 that drive source lines 67. *Supra* §§ X.A.1.b-X.A.1.e ([4a]-[4d]).

4. Claim 7

- a. **“The display device as set forth in claim 4, further comprising: a transistor included in the scanning line driving circuit.”**

140. In my opinion, *Reiner* discloses a transistor included in the scanning line driving circuit.

141. For example, *Reiner* discloses that the “integrated circuit device compris[es]” a “MOS transistor” or other type of transistor. *Reiner*, 6:12-17. As shown in FIG. 2, integrated “circuit device 20” includes “integrated device 22 (e.g., a [transistor](#)) having contacts 23.1 and 23.2.” *Reiner*, 6:18-21.

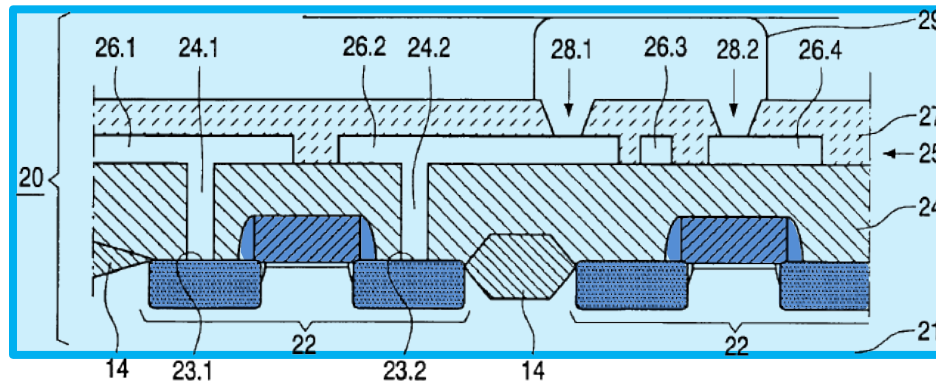
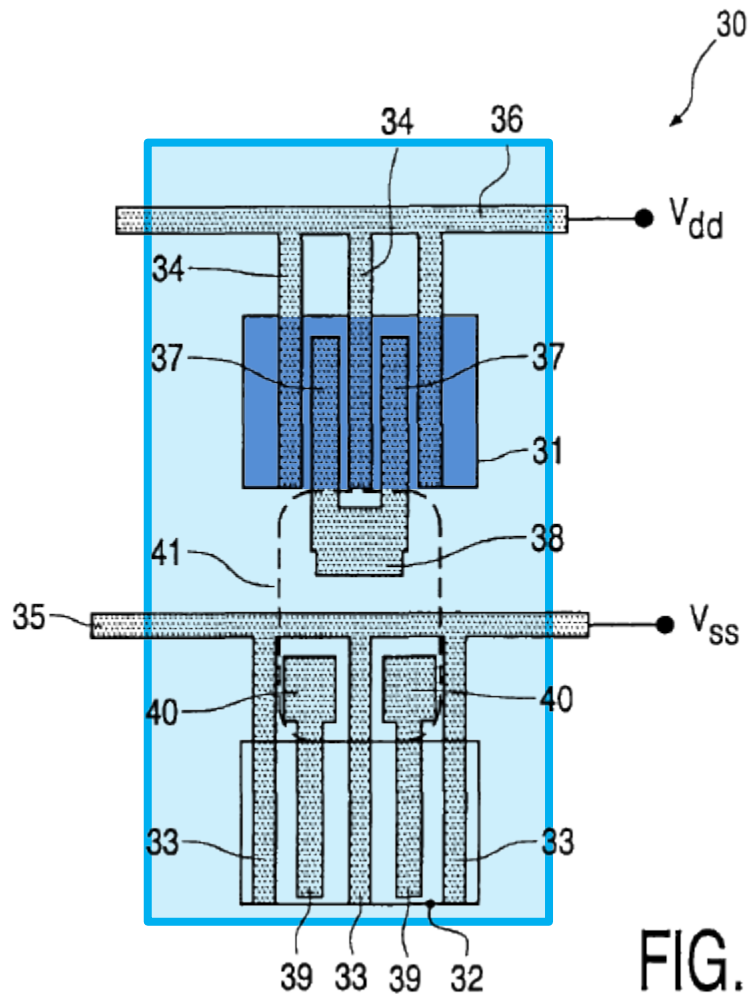


FIG. 2

Reiner, FIG. 2.

142. Similarly, FIG. 3 shows an integrated circuit device 30, which can be source driver 61 or gate driver 63, and includes “integrated devices 31 and 32,” both of which may include a “CMOS transistor[].” *Reiner*, 8:18-31. Transistor 31 is “an output stage of the integrated circuit device 30” (e.g., gate driver 63). *Reiner*, 8:21-31. An output stage corresponds to at least a portion of the output devices 70 of the integrated circuits of the gate driver 63 or source driver 61.



Reiner, FIG. 3.

5. Claim 8

143. In my opinion, *Reiner* renders obvious the additional limitations of claim 8.

a. [8a] “The display device as set forth in claim 4,
further comprising: a substrate,”

144. In my opinion, *Reiner* discloses the display device further comprising a substrate.

145. For example, *Reiner* discloses that FIG. 2 shows integrated circuit 20 (e.g., source driver 61, gate driver 63), including transistors 22, arranged on substrate 21. *Reiner*, 6:18-24. Similarly, the bump bridge(s) of integrated circuit device 20 (e.g., gate drivers 61, 63) allows the integrated circuit device to be arranged on substrate 16 via an interconnection on substrate 16 (not shown). *Reiner*, 7:22-26.

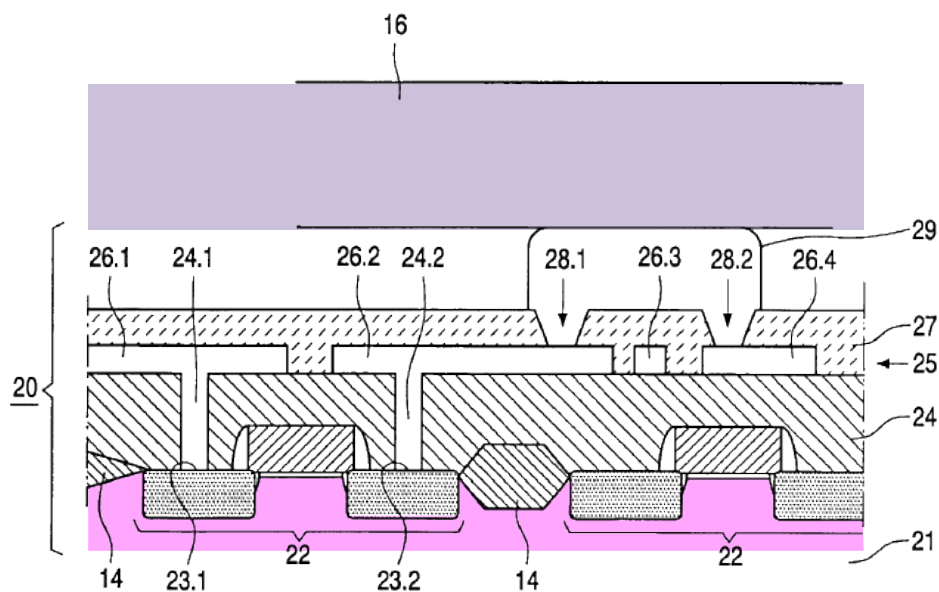


FIG. 2

Reiner, FIG. 2.

146. In my opinion, a POSITA would have recognized that substrates 21 or 16 may include, for example, the substrate on which the LCD display 60's scan/gate lines 68, source/data lines 67, and pixels are formed, such as shown in the general schematic of FIG. 4. *Reiner* explains that the driver output devices can be "connected (e.g. by means of bonding)" to their respective display lines via contact pads 72 to drive the lines, which could be patterned on the display's substrate, as shown in *Reiner*'s FIG. 4. *Reiner*, 10:1-6. Thus, *Reiner*'s gate driver 63 is arranged on a substrate to create the LCD display device described in *Reiner*, which the prior art confirms was conventional. *Takahara*, [0001], [0064], FIG. 1; *Murai*, [0001], [0017], FIG. 1; Ex. 1001, 1:57-59 ("FIG. 11 is a view illustrating a configuration of an active matrix substrate of a VGA-LCD using polysilicon TFT by the conventional art."). This known conventionality confirms the POSITA's reading of *Reiner* that the gate driver 63 would be arranged on a substrate when it is bonded at contact pad 72 to the scan lines because the scan lines, as shown in FIG. 4 and conventional in the art, are arranged on the display substrate and so the bonding together also arranges the gate driver 63 on the display substrate.

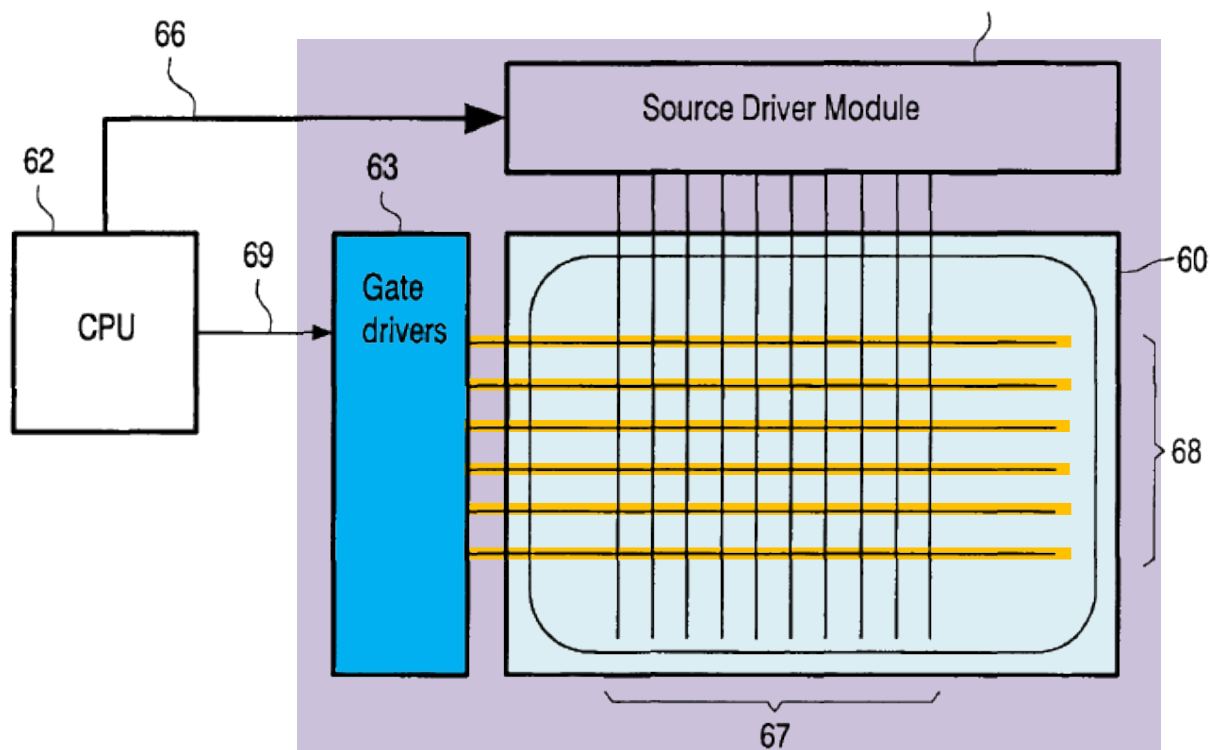


FIG. 4

Reiner, FIG. 4.

147. I have also been asked to consider the situation in which Patent Owner argues that *Reiner* discloses such connections only for the source driver 61. In my opinion, a POSITA would have found it obvious to include the same connections to interconnect gate driver 63 to the substrate, as I explain in claim 4.

b. [8b]: “the scanning line driving circuit being arranged on the substrate,”

148. For the reasons discussed in [8a], *Reiner* discloses or renders obvious the scanning line driving circuit being arranged on the substrate on which the LCD display 60’s scan lines are formed. *Supra*, § X.A.5.a.

c. [8c]: “the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”

149. In my opinion, *Reiner* discloses or renders obvious the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate.

150. For example, *Reiner* explains that the “power supply lines 71 [Vss] and 73 [Vdd] run perpendicular to the output lines 75 of the output devices 70” to supply power to each of the output devices of the driver unit, such as shown in FIG. 5. *Reiner*, 10:7-10, FIG. 5. A POSITA would have understood that *Reiner*’s discussion of the layout of FIG. 5 applies equally to both the source driver 61 and the gate driver 63 (scanning line driving unit), or at least would have found it obvious to use a similar layout, for at least the reasons I explained for claim 4. *Supra* § X.A.1.

151. Although *Reiner*’s FIG. 4 shows a display having six scan/gate lines 68 and ten data/source lines 67, a POSITA would have understood that an actual

LCD display would have had well over a hundred, and possibly over a thousand, such lines. Therefore, a POSITA would have known that the area in which the source driver 61 and gate driver 63 are positioned with their respective power lines would have been a very small portion of the overall substrate's area, with the majority of the area being devoted to the LCD screen 60. As shown in FIG. D below, even for an LCD display having 60 scan/gate lines and 120 source/data lines. Even with this example showing only a fraction of the size of an actual display, it is apparent that the power supply lines Vdd and Vss are formed over first corner portion and second corner portion of the substrate¹⁴ and follow the periphery of the substrate because they are perpendicular to the scan lines 68 at gate driver 63, as shown in Reiner's FIG. 5, outside (towards the substrate's outer edge) of contact portion 72, where gate driver 63 is connected to gate/scan line 68. See Reiner, 10:1-10, FIGS. 4, 5 (FIG. D). When Reiner's FIGS. 4 and 5 are taken in context, and accounting for the general size of the display and underlying

¹⁴ The first and second corner portions are not identified in claim 8 by any other positioning other than being "corner portions." The claim also does not recite the input terminal location and the same argument applies regardless of which side of the gate driver 63 they are on.

substrate, FIG. D below shows the **gate driver 63** (scanning line driving circuit) on the left side of the substrate and how the **power supply lines** (**Vdd**, **Vss**) run perpendicular to the scan lines 68. Because the **gate driver 63** and **power supply lines** are outside of the LCD screen 60, they are formed on the periphery of the substrate and are formed over the **first corner portion** and **second corner portion** that include the ends of **gate driver 63**. FIG. D below shows the input terminals at the “top” corner of the substrate, a POSITA would have recognized that they could also be located at the “bottom” corner and would still run perpendicular to the scanning lines of *Reiner*’s display device and would therefore still follow the periphery of the substrate to provide power to the gate driver 63.

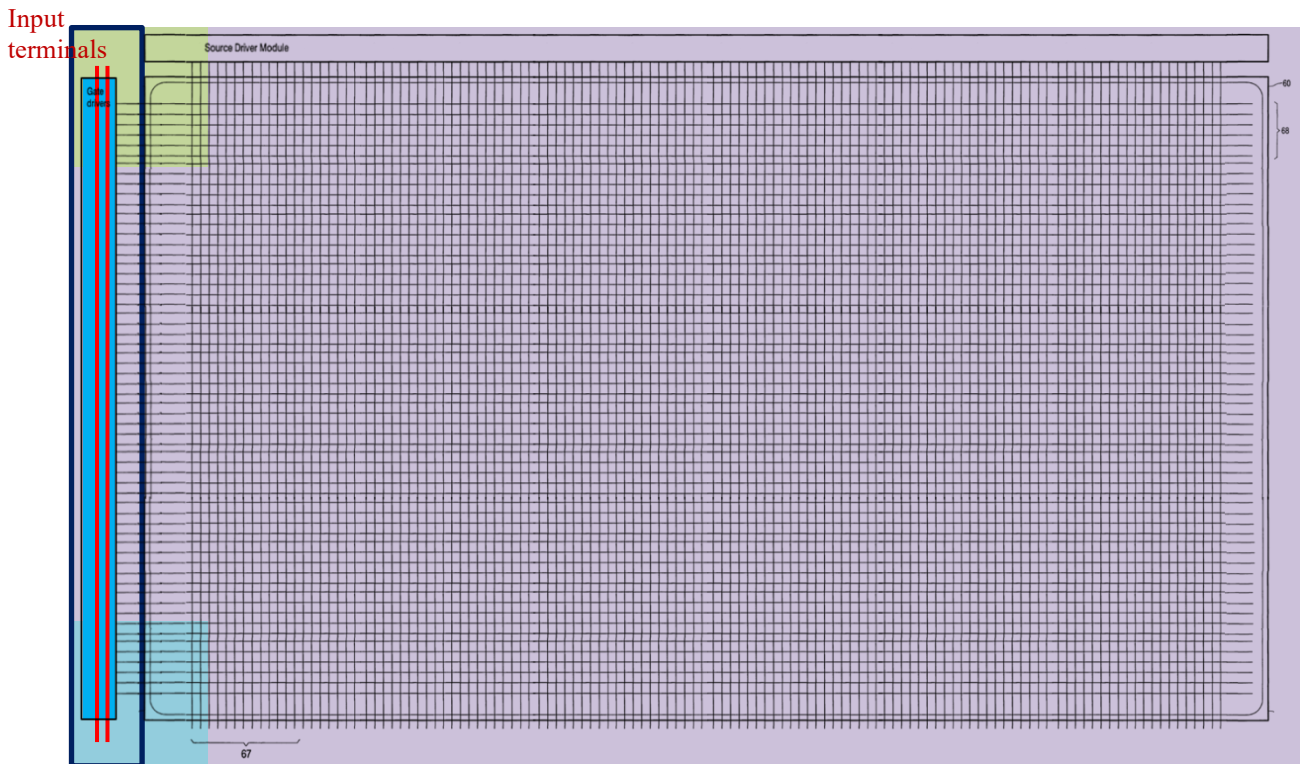


FIG. D

- d. [8d]: “the first protection circuit being arranged in the first corner portion of the substrate, and”

152. For at least the reasons explained above in [4d]-[4f], the first protection circuit can correspond to the ESD protection circuit ESD1, ESD2, or ESD3 at the first gate driver unit of gate driver 63 closest to the input terminals, at the first scan line 68, and is thus in the first corner portion of the substrate, as shown in [8c].

- e. **[8e]: “the second protection circuit being arranged in the second corner portion of the substrate.”**

153. For at least the reasons explained above in [4d]-[4f], the **second protection circuit** can correspond to the ESD protection circuit ESD1 or ESD2 at the **last gate driver unit** of **gate driver 63** farthest from the **input terminals**, at the last scan line 68, and is thus in the **second corner portion** of the **substrate**, as shown in [8c].

6. Claim 9

- a. **“An electronic device provided with the display device as set forth in claim 4.”**

154. In my opinion, *Reiner* discloses or renders obvious an electronic device provided with the display device of claim 4.

155. For example, for at least the reasons explained for claim 4, *Reiner* discloses an “LCD display” having an “LCD screen 60” that is powered by power supply lines Vss and Vdd, which a POSITA would understand describes an electronic device. *Reiner*, 9:23-26.

156. I have also been asked to consider the situation in which Patent Owner argues that *Reiner* is found to not disclose that the LCD screen 60 is provided in an electronic device. In that case, in my opinion, a POSITA would have found it obvious to have an electronic device provided with the display device of claim 4.

Reiner describes a display device having a CPU for controlling an LCD display 60 by providing video signals to the drivers 61 and 63, and a POSITA would have found it obvious to use the LCD display for its intended function as a display on an electronic device (powering the power lines Vss, Vdd), such as a television, computer monitor, personal digital assistant (PDA), cellular phone, laptop computer, or other device needing a display screen.

i. Motivation

157. In my opinion, a POSITA would have been motivated to use *Reiner*'s LCD display of claim 4 in an electronic device because the intended purpose of LCD displays is to provide a display screen for electronic devices, such as laptops, personal computers (PCs), PDAs, televisions, and other devices having display screens. LCDs were known to consume less power than other screen types, such as CRT displays, but could be subject to ESD damage, such as during manufacturing. A POSITA would have been motivated to implement *Reiner*'s LCD display of claim 4 as the display for an electronic device to reduce power consumption of the screen and implement an ESD protection network described to prevent ESD damage and thermal damage (for example, during manufacturing) that could render the display unacceptable for use. *Reiner*, 3:30-31, 12:22-25. A POSITA also would have been motivated to implement *Reiner*'s LCD display of claim 4 as the display

for an electronic device because it allows the designer “to realize more densely packed integrated circuits” for the display, which allows for the formation of smaller pixel rows leading to a sharper, less pixelated image on the screen. *Reiner*, 4:15-16, 12:18. The density of the integrated circuits would have also allowed for higher resolution screens, especially for smaller screens, thereby improving the user’s experience with the electronic device, and providing a further motivation for their use.

ii. Expectation of Success

158. A POSITA would have reasonably expected to succeed in implementing an electronic device provided with the display screen of claim 4. The use of LCD display screens in electronic devices was conventional in the prior art and for POSITAs. Implementing the display screen of claim 4 into an electronic device, such as a laptop computer, monitor, television, PDA, or cellular phone, would have been merely the straightforward application of known, conventional manufacturing techniques to fabricate the display with the device or attach the display to the device during manufacturing, used according to their known functions to yield predictable results (implementing an LCD display in device).

7. Independent Claim 10

a. [10pre]: “A display device, comprising:”

159. [10pre] is substantively the same as [4pre] and *Reiner* discloses [10pre] for the reasons discussed above in [4pre]. *Supra* § X.A.1.a.

b. [10a]: “a circuit element included in a scanning line driving circuit;”

160. [10a] is substantively similar to [4a], except that it recites a “circuit element” included in the scanning line driving circuit, rather than the entire circuit. *Compare* Ex. 1001, 12:27, *with id.*, 13:6. As I explain in [4d]-[4f] and claim 5, *Reiner* discloses or renders obvious the gate driver 63 (scanning line driving circuit) including the line driver output devices 70 (circuit elements), which may comprise a transistor and/or a buffer, and therefore discloses or renders obvious [10a] for the reasons discussed above in [4a], [4d]-[4f], and claim 5. *Supra* §§ X.A.1.b, X.A.1.e-X.A.2.

c. [10b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”

161. [10b] is substantively the same as [4b] and *Reiner* discloses or suggests [10b] for the reasons discussed above in [4b]. *Supra* § X.A.1.c.

d. [10c]: “an input terminal connected to the power supply line to supply power; and”

162. [10c] is substantively the same as [4c] and *Reiner* discloses or renders obvious [10c] for the reasons discussed in [4c]. *Supra* § X.A.1.d.

e. [10d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element, the first protection circuit and the second protection circuit are connected to the power supply line,”

163. [10d] is substantively similar to [4d], except that it recites the first and second protection circuits being connected to the scanning line driving circuit “to protect the circuit element” instead of “to protect the scanning line driving circuit.” *Compare* Ex. 1001, 12:33-37, *with id.*, 13:13-17. As I explain in [4d]-[4f] and claim 5, *Reiner* discloses or renders obvious the first and second protection circuits being connected to the gate driver 63 (scanning line driving circuit) “to protect the circuitry inside the [output] devices 70” (circuit elements) for each of the scanning lines, and therefore discloses or renders obvious [10d] for the reasons discussed above in [4d]-[4f] and claim 5. *Reiner*, 10:10-12; *supra* §§ X.A.1.e-X.A.2.

- f. **[10e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and”**

164. [10e] is substantively similar to [4e], except that it recites the “circuit element,” instead of the “scanning line driving circuit,” being connected to the power supply line in (i). *Compare* Ex. 1001, 12:38-41, *with id.*, 13:18-21. As I explain in [4e], *Reiner* discloses or renders obvious the first protection circuit being connected to the power supply line Vdd/Vss between (i) the first connecting portion where an intermediate gate driver output device 70 of gate driver 63 (circuit element) is connected to the power supply line, and (ii) the input terminals, and therefore discloses or renders obvious [10e] for the reasons discussed above in [4e]. *Supra* § X.A.1.f.

- g. **[10f]: “the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”**

165. [10f] is substantively similar to [4f], except that it recites the “circuit element,” instead of the “scanning line driving circuit,” being connected to the power supply line between the second connecting portion in (iii) and the third connecting portion in (iv). *Compare* Ex. 1001, 12:38-41, *with id.*, 13:18-21. As I

explain in [4f], *Reiner* discloses or renders obvious an intermediate output device 70 of gate driver 63 (circuit element) being connected to the power supply line Vdd/Vss between the second connecting portion connecting the first protection circuit to the power supply line and the third connecting portion connecting the second protection circuit to the power supply line, and therefore discloses or renders obvious [10f] for the reasons discussed above in [4f]. *Supra* § X.A.1.g.

8. Claim 11

- a. **“The display device as set forth in claim 10, further comprising: a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.”**

166. The additional limitations of claim 11 are substantively the same as those in claim 5, and are disclosed by *Reiner* for the reasons discussed for claim 5. *Supra* § X.A.2. The scanning line driving unit circuit includes a buffer or transistor element, as discussed in [10a]. *Supra* § X.A.7.b.

9. Claim 12

- a. **“The display device as set forth in claim 10, further comprising: a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.”**

167. The additional limitations of claim 12 are substantively the same as those in claim 6, and are disclosed or renders obvious by *Reiner* for the reasons

discussed for claim 6. *Supra* § X.A.3. The scanning line driving unit circuit includes a buffer that may comprise the circuit element, as discussed in [10a].

Supra § X.A.7.b.

10. Claim 13

- a. **“The display device as set forth in claim 10, further comprising: a transistor included in the scanning line driving circuit, the transistor being the circuit element.”**

168. The additional limitations of claim 13 are substantively the same as those in claim 7, and are disclosed by *Reiner* for the reasons discussed for claim 7.

Supra § X.A.4.

11. Claim 14

- a. **[14a]: “The display device as set forth in claim 10, further comprising: a substrate,”**

169. The additional limitations of [14a] are substantively the same as those in [8a], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8a]. *Supra* § X.A.5.a.

- b. **[14b]: “the scanning line driving circuit being arranged on the substrate,”**

170. The additional limitations of [14b] are substantively the same as those in [8b], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8b]. *Supra* § X.A.5.b.

- c. **[14c]: “the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”**

171. The additional limitations of [14c] are substantively the same as those in [8c], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8c]. *Supra* § X.A.5.c.

- d. **[14d]: “the first protection circuit being arranged in the first corner portion of the substrate, and”**

172. The additional limitations of [14d] are substantively the same as those in [8d], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8d]. *Supra* § X.A.5.d.

- e. **[14e]: “the second protection circuit being arranged in the second corner portion of the substrate.”**

173. The additional limitations of [14e] are substantively the same as those in [8e], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8e]. *Supra* § X.A.5.e.

12. Claim 15

- a. **“An electronic device provided with the display device as set forth in claim 10.”**

174. The additional limitations of claim 15 are substantively the same as those in claim 9, and are disclosed or rendered obvious by *Reiner* for the reasons discussed for claim 9. *Supra* § X.A.6.

13. Independent Claim 16

a. [16pre]: “A display device, comprising:”

175. [16pre] is substantively the same as [4pre] and *Reiner* discloses [16pre] for the reasons discussed above in [4pre]. *Supra* § X.A.1.a.

b. [16a]: “a scanning line driving circuit;”

176. [16a] is substantively the same as [4a] and *Reiner* discloses [16a] for the reasons discussed above in [4a]. *Supra* § X.A.1.b.

c. [16b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”

177. [16b] is substantively the same as [4b] and *Reiner* discloses or suggests [16b] for the reasons discussed above in [4b]. *Supra* § X.A.1.c.

d. [16c]: “an input terminal connected to the power supply line to supply power; and”

178. [16c] is substantively the same as [4c] and *Reiner* discloses or renders obvious [16c] for the reasons discussed above in [4c]. *Supra* § X.A.1.d.

- e. **[16d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”**

179. [16d] is substantively similar to [4d], except that it recites the first and second protection circuits being “connected to power supply line” to “protect the power supply line,” instead of being “connected to the scanning line driving circuit” to “protect the scanning line driving circuit.” *Compare* Ex. 1001, 12:33-37, *with id.*, 13:63-67.

180. As I explain in [4d]-[4f], *Reiner* discloses or renders obvious the first and second protection circuits being connected to power supply line Vdd or Vss. *Supra* §§ X.A.1.e-X.A.1.g.

181. For at least the reasons explained below, [16e]-[16h] recite the same connections between the first protection circuit, the second protection circuit, and the scanning line driving circuit as [4e] and [4f], and the first and second protection circuits being on a first and second side of the scanning line driving circuit, like the first and second corner portions of claim 8. Given the structural similarities, this configuration also protects the power supply line between the first and second protective circuits, as well as the scanning line driving circuit (and individual

driver elements of the scanning line driving circuit).¹⁵ *Reiner*'s ESD protection network, such as ESD1, ESD2, and ESD3, protect the power line because they are configured to "provide a low-ohmic path" to a "ground terminal" (not shown in FIG. 5) "in case of a voltage peak," which is an ESD event. *Reiner*, 10:15-17. In *Reiner*, the power supply line is protected because static electricity generated on power supply lines Vss or Vdd would be a "voltage peak" (electrostatic discharge) that gets shunted to a "ground terminal" by the "diodes" or "transistors" in ESD1, ESD2, or ESD3. *Reiner*, 10:1-17. For at least the reasons explained in *Reiner*, the ESD protection circuits ESD1, ESD2, and ESD3, also protect against thermal damage, which can occur when an electrostatic discharge occurs on a metal line because the high charge of the ESD event and the thinness of the metal lines, especially in *Reiner*'s "densely packed" driver circuits, can cause thermal damage by heating up the metal lines to the point that the heat damages the metal line, such

¹⁵ The specification of the '157 patent does not recite protecting the power supply line with protective circuits ESD1-ESD4 or ESD11-ESD13. A POSITA would have understood that the same configuration protecting the scanning line driving circuit would have been understood to protect the power supply line or the claim would not be described in the '157 patent.

as the power line, or a surrounding component, such as a transistor of the output unit. Thus, as Reiner explains, the electrostatic protection circuits ESD1, ESD2, and ESD3 each “protect the circuitry inside the [output] devices 70” and also protect the power lines. *Reiner*, 10:1-15, 12:24-25. *Reiner* discloses or renders obvious [16d] for the reasons discussed in [4d]-[4f] and the “corner portions” of claim 8. *Supra* §§ X.A.1.e-X.A.1.g, X.A.5.

- f. [16e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal”

182. [16e] is substantively the same as [4e] and *Reiner* discloses or renders obvious [16e] for the reasons discussed above in [4e]. *Supra* § X.A.1.f.

- g. [16f] “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”

183. [16f] is substantively broader than [8d] and *Reiner* discloses or renders obvious [16f] for the reasons discussed for [8d] because the first protection circuit is disposed at the first gate driver unit of gate driver 63 closest to the input terminals, thereby being at a position that is on a first side of the scanning line driving circuit closest to the input terminals near the first scan line.

Supra § X.A.5.d.

- h. **[16g]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”**

184. [16g] is substantively the same as [4f] and *Reiner* discloses or renders obvious [16g] for the reasons discussed above in [4f]. *Supra* § X.A.1.g

- i. **[16h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”**

185. [16h] is substantively broader than [8e] and *Reiner* discloses or renders obvious [16h] for the reasons discussed for [8e] because the second protection circuit is disposed at the **last gate driver unit** of **gate driver 63** farthest from the **input terminals**, thereby being at a position that is on a second side of the scanning line driving circuit farthest from the input terminals near the last scan line. *Supra* § X.A.5.d.

14. Independent Claim 17

- a. **[17pre]: “A display device, comprising:”**

186. [17pre] is substantively the same as [4pre] and *Reiner* discloses [17pre] for the reasons discussed above in [4pre]. *Supra* § X.A.1.a.

b. [17a]: “a scanning line driving circuit;”

187. [17a] is substantively the same as [4a] and *Reiner* discloses [17a] for the reasons discussed above in [4a]. *Supra* § X.A.1.b.

c. [17b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”

188. [17b] is substantively the same as [4b] and *Reiner* discloses or suggests [17b] for the reasons discussed above in [4b]. *Supra* § X.A.1.c.

d. [17c]: “an input terminal connected to the power supply line to supply power; and”

189. [17c] is substantively the same as [4c] and *Reiner* discloses or renders obvious [17c] for the reasons discussed above in [4c]. *Supra* § X.A.1.d.

e. [17d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”

190. [17d] is substantively the same as [4d], except that [17d] recites the first and second protective circuits being “connected to the power supply line,” like [16d]. For at least the reasons explained for [4e], [4f], [16d], [16e], and [16g], *Reiner* discloses or renders obvious the first and second protection circuits being

connected to the power supply line “to protect the circuitry inside the devices 70” and thereby protect scanning line driving circuit. *Supra* §§ X.A.1.f, X.A.1.g, X.A.13.e, X.A.13.f, X.A.13.h.

- f. **[17e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal”**

191. [17e] is substantively the same as [4e] and *Reiner* discloses or renders obvious [17e] for the reasons discussed above in [4e]. *Supra* § X.A.1.f.

- g. **[17f]: “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”**

192. [17f] is substantively the same as [16f] and *Reiner* discloses or renders obvious [17f] for the reasons discussed above in [16f] and [8d]. *Supra* §§ X.A.13.g, X.A.5.d.

- h. **[17g]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”**

193. [17g] is substantively the same as [4f] and *Reiner* discloses or renders obvious [17g] for the reasons discussed above in [4f]. *Supra* § X.A.1.g

- i. **[17h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”**

194. [17h] is substantively the same as [16h] and *Reiner* discloses or renders obvious [17h] for the reasons discussed above in [16h] and [8e]. *Supra* §§ X.A.13.i, X.A.5.e.

15. Independent Claim 18

- a. **[18pre]: “A display device, comprising:”**

195. [18pre] is substantively the same as [4pre] and *Reiner* discloses [18pre] for the reasons discussed above in [4pre]. *Supra* § X.A.1.a.

- b. **[18a]: “a circuit element included in a scanning line driving circuit;”**

196. [18a] is substantively the same as [10a] and *Reiner* discloses or renders obvious [18a] for the reasons discussed above in [4a] and [10a]. *Supra* §§ X.A.1.b, X.A.7.b.

- c. **[18b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”**

197. [18b] is substantively the same as [4b] and *Reiner* discloses or suggests [18b] for the reasons discussed above in [4b]. *Supra* § X.A.1.c.

- d. **[18c]: “an input terminal connected to the power supply line to supply power; and”**

198. [18c] is substantively the same as [4c] and *Reiner* discloses or renders obvious [18c] for the reasons discussed above in [4c]. *Supra* § X.A.1.d.

- e. **[18d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect a part of the circuit element, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”**

199. [18d] is substantively the same as [4d] and [10d], except that [18d] recites the first and second protective circuits being “connected to the power supply line,” like [16d], and to protect “a part of the circuit element,” like [10d]. For at least the reasons explained for [4e], [4f], [10d]-[10f], [16d], [16e], and [16g], *Reiner* discloses or renders obvious the first and second protection circuits being connected to the power supply line “to protect the circuitry inside the devices 70,” such as a buffer or transistor therein (which is part of the circuit element). *Supra* §§ X.A.1.f, X.A.1.g, X.A.7.e-X.A.7.g, X.A.13.e, X.A.13.f, X.A.13.h.

- f. **[18e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal”**

200. [18e] is substantively the same as [4e] and [10e] and *Reiner* discloses or renders obvious [17e] for the reasons discussed above in [4e] and [10e]. *Supra* §§ X.A.1.f, X.A.7.f.

- g. **[18f]: “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”**

201. [18f] is substantively the same as [16f] and *Reiner* discloses or renders obvious [18f] for the reasons discussed above in [16f] and [8d]. *Supra* §§ X.A.13.g, X.A.5.d.

- h. **[18g]: “the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”**

202. [18g] is substantively the same as [4f] and [10f] and *Reiner* discloses or renders obvious [118g] for the reasons discussed above in [4f] and [10f]. *Supra* §§ X.A.1.d, X.A.7.g.

- i. **[18h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”**

203. [18h] is substantively the same as [16h] and *Reiner* discloses or renders obvious [18h] for the reasons discussed above in [16h] and [8e]. *Supra* §§ X.A.13.i, X.A.5.e.

16. Independent Claim 1

- a. **[1pre]: “A display device, comprising:”**

204. [1pre] is substantively the same as [4pre] and *Reiner* discloses [1pre] for the reasons discussed above in [4pre]. *Supra* § X.A.1.a.

- b. **[1a]: “a scanning line driving circuit;”**

205. [1a] is substantively the same as [4a] and *Reiner* discloses [1a] for the reasons discussed above in [4a]. *Supra* § X.A.1.b.

- c. **[1b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”**

206. [1b] is substantively the same as [4b] and *Reiner* discloses or suggests [1b] for the reasons discussed above in [4b]. *Supra* § X.A.1.c.

d. [1c]: “an input terminal connected to the power supply line to supply power;”

207. [1c] is substantively the same as [4c] and *Reiner* discloses or renders obvious [1c] for the reasons discussed above in [4c]. *Supra* § X.A.1.d.

e. [1d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line;”

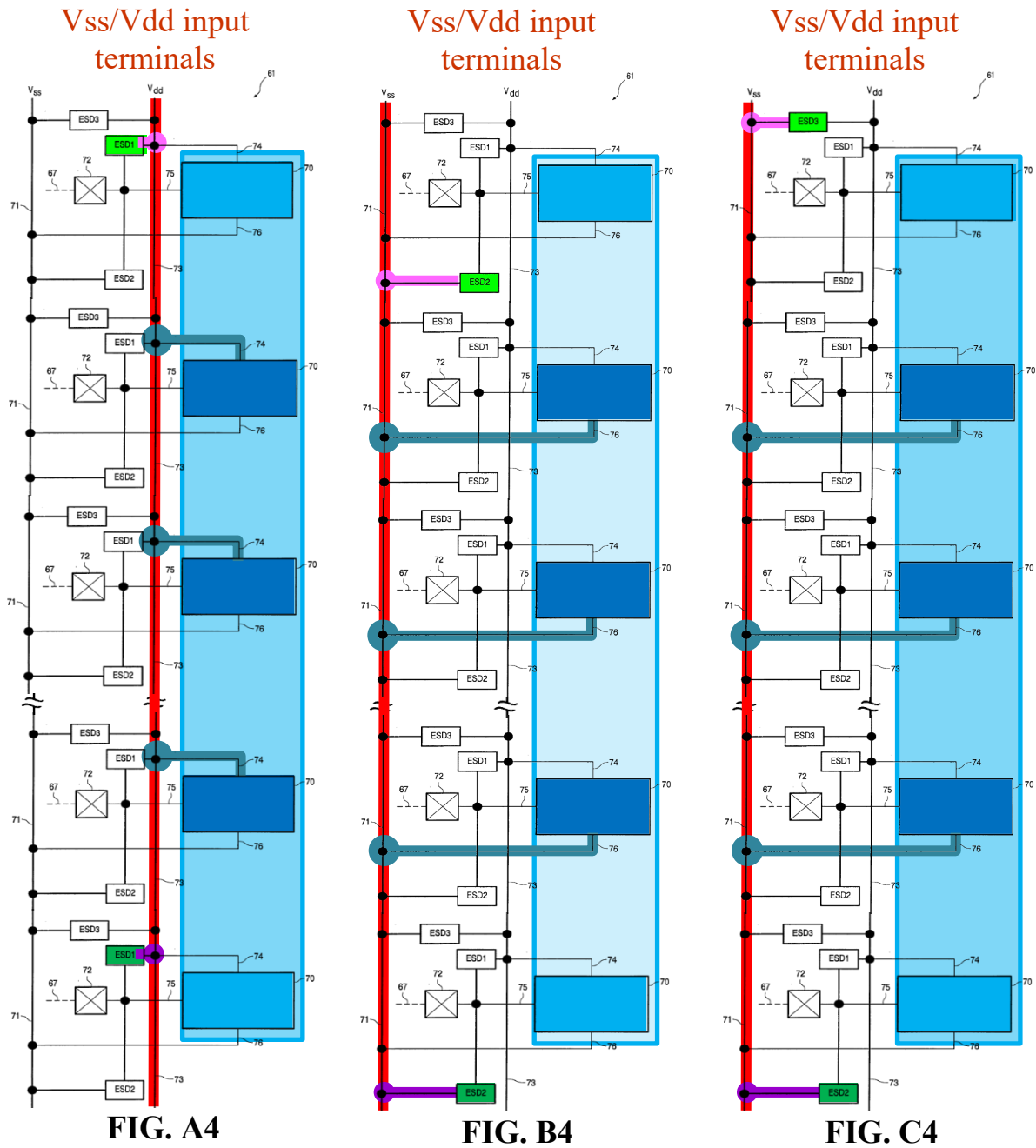
208. [1d] is substantively the same as [4d] and *Reiner* discloses or renders obvious [1d] for the reasons discussed above in [4d]. *Supra* § X.A.1.e.

f. [1e]: “a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and”

209. *Reiner* discloses a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line. This is shown in each of the alternative mappings Ax, Bx, and Cx discussed in this declaration.

210. For example, *Reiner* discloses that the “display driver ... 63 typically has a large number of parallel outputs” and is “designed to drive many lines of an LCD display 60,” such as shown in FIG. 4. *Reiner*, 9:11-15. *Reiner* explains that its “bump bridges allow many output devices of the integrated circuit device 61 or

62 [*sic*: 63] to cross the power supply lines which provide supply voltage (e.g., Vdd) to the output devices” of integrated circuits 61, 63 *Reiner*, 9:18-20. In other words, *Reiner* discloses that the gate driver 63 (scanning line driving circuit) includes “many output devices” (e.g., output devices 70) (scanning line driving unit circuits) to drive each of the gate lines and that these output devices receive power through their connections to power supply line Vdd or Vss to drive the gate lines, as shown in FIGS. A4, B4, and C4, below. *Reiner*, 9:11-20. The connections to the power supply lines are annotated for two output devices but are present for all of the output devices.



211. *Reiner* therefore discloses [1e].

- g. [1f]: “a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other,”

212. *Reiner* discloses or renders obvious a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other. This is shown in each of the alternative mappings Ax, Bx, and Cx discussed in this declaration.

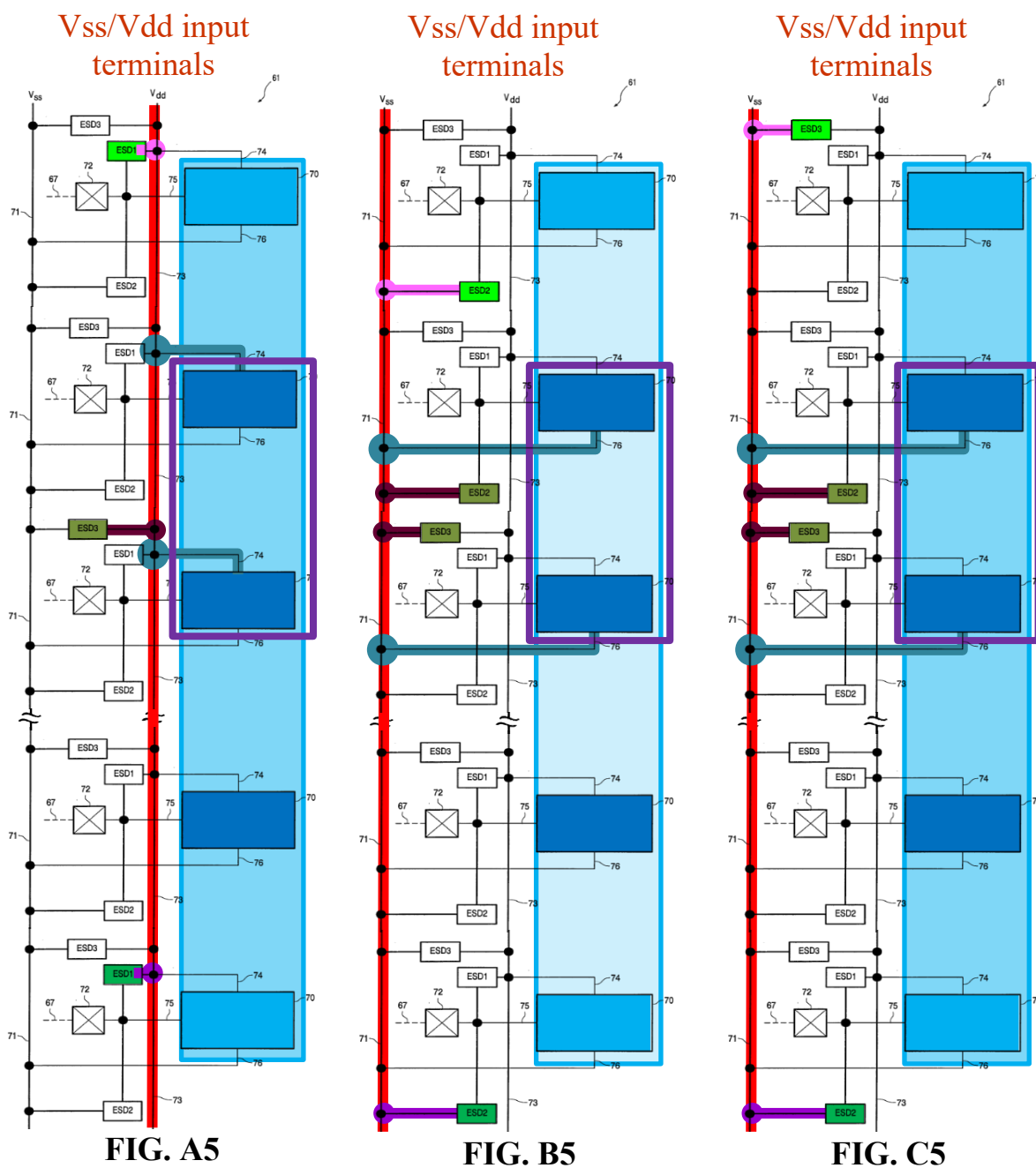
213. For example, *Reiner* explains that “three ESD devices ESD 1, ESD2, and ESD3 are provided *for each output device 70*, in order to protect the circuitry inside the devices 70.” *Reiner*, 10:10-12 (emphasis added). For at least the reasons explained for claim 4, this describes or renders obvious each of the [output devices 70](#) of [gate driver 63](#) having an “ESD protection network” comprising protection circuits ESD1, ESD2, and ESD3, such as shown in FIG. 5. *Supra*

§§ X.A.1.e-X.A.1.g. As I explain in claim 4, if it is argued that *Reiner* does not disclose applying the ESD protection networks to gate driver 63’s output devices,

in my opinion, a POSITA would have found it obvious to do so. *Supra*

§§ X.A.1.e-X.A.1.g.

214. As shown in FIGS. A5-C5, *Reiner* discloses or renders obvious a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of gate driver scanning line driving unit circuits of the gate driver 63 and a second scanning line driving unit circuit of the plurality of gate driver scanning line driving unit circuits of the gate driver 63, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other.



215. As shown above in FIG. A5, for example, a **third protection circuit** **ESD3** is **connected to the power supply line Vdd** between the **second output device 70** from the top (**first scanning line driving unit circuit**) of the “many output

devices” 70 for driving the scan lines (plurality of scanning line driving unit circuits) and the **third output device 70** from the top (**second scanning line driving unit circuit**) of the “many output devices” 70 for driving the scan lines (plurality of scanning line driving unit circuits), with the **second and third output devices 70** (first scanning line driving unit circuit and the second scanning line driving unit circuit) **being adjacent to each other** in the **gate driver 63**. *Reiner*, 9:12-22.

216. As shown above in FIG. B5, for example, a **third protection circuit ESD2 or ESD3** is **connected to the power supply line Vss** between the **second output device 70** from the top (**first scanning line driving unit circuit**) of the “many output devices” 70 for driving the scan lines (plurality of scanning line driving unit circuits) and the **third output device 70** from the top (**second scanning line driving unit circuit**) of the “many output devices” for driving the scan lines (plurality of scanning line driving unit circuits), with the **second and third output devices 70** (the first scanning line driving unit circuit and the second scanning line driving unit circuit) **being adjacent to each other** as the second and third output devices 70 in the **gate driver 63**. *Reiner*, 9:12-22.

217. And, when considering the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines, as shown above in FIG. C5, for example, a **third protection circuit ESD2 or ESD3** is

connected to the power supply line V_{ss} between the second output device 70 from the top (first scanning line driving unit circuit) of the “many output devices” 70 and the third output device 70 from the top (second scanning line driving unit circuit), with the second and third output devices 70 being adjacent to each other in gate driver 63. *Reiner*, 9:12-22.

218. Although the second and third output devices 70 are emphasized in FIGS. A5, B5, and C5, in my opinion, a POSITA would have known that the same analysis applies to any two adjacent output devices 70 (e.g., third and fourth, twentieth and twenty-first, etc.) of gate driver 63 because *Reiner* explains that, in the “ESD protection network,” “three ESD devices ESD1, ESD2, and ESD3 are provided for each output device 70, in order to protect the circuitry inside the [output] devices 70.” *Reiner*, 3:4-8, 10:10-12 (emphasis added).

219. *Reiner* therefore discloses or renders obvious [1f].

- h. [1g]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and”

220. [1g] is substantively the same as [4e] and *Reiner* discloses or renders obvious [1g] for the reasons discussed above in [4e]. *Supra* § X.A.1.f.

- i. **[1h]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”**

221. [1h] is substantively the same as [4f] and *Reiner* discloses or renders obvious [1h] for the reasons discussed above in [4f]. *Supra* § X.A.1.g

17. Claim 2

- a. **[2a]: “The display device as set forth in claim 1, further comprising: a substrate,”**

222. The additional limitations of [2a] are substantively the same as those in [8a], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8a]. *Supra* § X.A.5.a.

- b. **[2b]: “the scanning line driving circuit being arranged on the substrate,”**

223. The additional limitations of [2b] are substantively the same as those in [8b], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8b]. *Supra* § X.A.5.b.

- c. **[2c]: “the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”**

224. The additional limitations of [2c] are substantively the same as those in [8c], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8c]. *Supra* § X.A.5.c.

- d. **[2d]: “the first protection circuit being arranged in the first corner portion of the substrate, and”**

225. The additional limitations of [2d] are substantively the same as those in [8d], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8d]. *Supra* § X.A.5.d.

- e. **[2e]: “the second protection circuit being arranged in the second corner portion of the substrate.”**

226. The additional limitations of [2e] are substantively the same as those in [8e], and are disclosed or rendered obvious by *Reiner* for the reasons discussed for [8e]. *Supra* § X.A.5.e.

18. Claim 3

- a. **“An electronic device provided with the display device as set forth in claim 1.”**

227. The additional limitations of claim 3 are substantively the same as those in claim 9, and are disclosed or rendered obvious by *Reiner* for the reasons discussed for claim 9. *Supra* § X.A.6.

B. Ground 2: Claims 1-18 Are Rendered Obvious by *Reiner* and *Takahara*

1. Independent Claim 4

228. As an alternative opinion, I have been asked to consider the scenario in which *Reiner* is found not to disclose or render obvious the input terminals of [4c] or that it would have been obvious to protect the gate driver 63 (scanning line driver circuit) with ESD protection of [4d]-[4f]. In this situation, in my opinion, *Reiner* in view of *Takahara* would have rendered these limitations obvious to a POSITA.

a. [4c]: “an input terminal connected to the power supply line to supply power; and”

229. *Takahara* discloses that “terminals 800, 801, 802” (input terminals) provide power to power supply lines VDDY and VSSY “for driving the scan-line drive circuit 104.” *Takahara*, [0063], [0065]; see also *Takahara* [0025].

i. Motivation

231. A POSITA would have been motivated to provide a respective input terminal connected to each of *Reiner*'s power supply lines 71 (Vss) and 73 (Vdd), such as *Takahara*'s input terminals for the VDDY and VSSY power supply lines to supply power to the scanning line driving circuit because the terminals would have provided a power connection from a power source to the gate driver 63 to "drive [the] many lines of ... LCD display 60" to display images on the LCD screen. *Reiner*, 9:12-14; *Takahara*, [0063]. A POSITA would have recognized that *Reiner*'s gate driver 63 is arranged on a substrate, similar to *Takahara*'s active matrix substrate 10, to connect the gate driver 63's power supply lines with other components, such as power supply lines VDDY and VSSY on the substrate, and would have needed input terminal power connections 800, 801, 802 to power the Vdd (VDDY) and Vss (VSSY) wiring lines for the display 60 that drive the scanning line driving circuit, such as shown in FIG. 1 of *Takahara*. *Reiner*, 7:23-25; *Takahara*, [0063], [0066], FIG. 1; *see also* Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751) (acknowledging that "conventional art" related to protecting driving circuits includes input terminals to supply power via power lines). For example, in one option, the gate driver 63 could be bonded to the active matrix substrate at the "contact pads 72" to connect it to the gate lines that are

being driven and also other points of connection, such as the power lines running along the active matrix substrate to the location of the scanning line driving unit, such as shown in *Takahara's* FIG. 1. Alternatively, a POSITA would have been motivated to form the gate driver 63 on *Takahara's* glass substrate with the scan lines, power lines, and pixel units. Moreover, forming driver circuits, gate lines, and scan lines on the glass substrate was a well known, conventional structure and manufacturing practice, and applying *Reiner's* teachings could achieve benefits, such as a narrower border and larger area devoted to pixels. As I explain in the background section above (*supra* § V), using glass substrates can have risks of ESD events and ESD damage because of the insulative properties. Although the risk of ESD is heightened, the benefits of forming the driver units directly on the substrate can offset the risk when sufficiently protected. A POSITA therefore would have been motivated to include *Reiner's* protection circuits ESD1, ESD2, ESD3 to protect the gate driver 63 from ESD damage, in particular from both ESD events occurring on the power lines VDDY/VSSY and/or localized ESD occurring on the substrate itself. A POSITA would have recognized the benefits of providing ESD protection “to protect the circuitry inside” each of the output devices 70, as taught by *Reiner*, to better protect against localized ESD event and ESD events on the metal lines. *See Reiner*, 10:1-15. A POSITA also would have been motivated to

form *Reiner*'s gate driver 63 and protective circuits on the glass substrate of *Takahara* to take advantage of the "densely packed" circuit configuration of *Reiner* to provide a narrower border region, which has additional aesthetic appeal to customers. In both cases, the arrangement of the gate driver 63 (scanning line driving circuit) on the substrate would be connected to the input terminals as taught by *Takahara* to provide power to the scanning line driving circuit.

232. A POSITA would have been motivated to provide input terminals connected to *Reiner*'s power supply lines Vdd (VDDY) and Vss (VSSY), as taught by *Takahara*, to supply power to *Reiner*'s gate driver 63 so that the scanning lines (gate lines 68) can be driven and an image can be displayed on LCD display 60.

ii. Expectation of Success

233. A POSITA would have reasonably expected to succeed in providing input terminals connected to *Reiner*'s power supply lines Vss 61 and Vdd 63 to supply power to the gate driver 63 (scanning line driving circuit), as taught by *Takahara*. The use of input terminals to supply power to power supply lines was admittedly "conventional art" for LCD displays that *Reiner*, *Takahara*, and the '157 patent each describe. *Reiner*, 7:23-25; Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751); *Takahara*, [0063], [0066], FIG. 1 (power supply lines VSSY, VDDY having input terminals 800, 802 for driving scanning line driving

circuit 104). Incorporating input terminals connected to *Reiner*'s respective power supply lines Vdd (VDDY) and Vss (VSSY), as taught by *Takahara*, to provide power would have been merely the straightforward application of known, conventional techniques applied to *Reiner*'s power supply lines Vss 71, Vdd 73 used according to their known functions to yield predictable results (providing a connection through which power flows to the power supply lines to power the gate driver 63). *See Reiner*, 9:12-13, 9:18-20, 9:27-29, 10:6-10, 12:4-5; *Takahara*, [0063], [0066], FIG. 1.

- b. **[4d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,”**
[4e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and”
[4f]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

234. In the situation that *Reiner* is determined not to disclose or render obvious providing ESD protection to protect a scanning line driving circuit as

explained in Ground 1 above, then in my opinion, *Reiner* and *Takahara* would have rendered it obvious to a POSITA.

235. *Takahara* discloses that “[e]lectrostatic [ESD] protection circuits 150 and 151 are formed at intermediate positions of the signal lines ... 73,” which include power lines VDDY and VSSY, so that “static electricity is reliably absorbed” and “scan-line drive circuit 104 can be reliably protected.” *Takahara*, [0066], FIG. 1. Power lines VDDY and VSSY are shorted to the lines containing ESD protection circuits 150 and 151 that protect both ends of the scanning line driving circuit 104 by shorting lines 91. *Takahara*, [0070].

subjected to a discharge event.” *Reiner*, 2:28-3:1; *Takahara*, [0066] (“the scanning line driving circuit can be reliably protected”).

i. Motivation

237. A POSITA would have been motivated to provide a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the “very sensitive circuits” inside the gate driver 63 (scanning line driving circuit) from ESD events and damage and also connected to the power supply lines that can be lines that are subject to ESD events, for at least the reasons explained in Ground 1, claim 4. *Reiner*, 2:28-3:1; *see Takahara*, [0066], FIGS. 1, 3. A POSITA would have recognized that *Reiner*’s “very sensitive circuits” of gate driver 63 are at risk from ESD damage and can be “destroyed when ... subjected to a discharge event,” for at least the reasons explained in Ground 1, claim 4. *Reiner*, 2:28-3:1. A POSITA would have been motivated to “reliably protect[]” the gate driver from ESD damage and prevent the output devices of the gate driver 63 (and thereby protect the gate driver 63) from being damaged by ESD events. For example, *Takahara* discloses that using ESD protection circuits on signal or power lines connected to the scanning line driving unit can “reliably protect[]” the scanning line driving circuit from ESD damage. *Takahara*, [0066], FIGS. 1, 3 (items 150, 151). Moreover, the ’157 patent admits

that it was “conventional art” to protect scanning line driving circuits using ESD protection circuits, and *Reiner* and *Takahara* also recognize the need to do so. *Reiner*, 2:28-3:1, 6:12-17, 8:30-31; *Takahara*, [0063], [0066], FIG. 1; Ex. 1001, 1:25-2:30.

238. A POSITA would have been motivated to “protect the circuitry” of the output devices of *Reiner*’s gate driver 63 in the same way as source driver 61 to prevent them from being damaged by ESD events because *Takahara* confirms that scanning line drivers can be “reliably protected” by ESD protection circuits in the same way as data line drivers. *Reiner*, 10:10-12; *Takahara*, [0066]. A POSITA also would have been motivated to protect the gate driver 63 and its internal circuits because damage from ESD events could require costly repairs or additional complex manufacturing repair processes or render the display unfit for use. *Reiner*, 10:10-12; *Takahara*, [0066]. A POSITA would have been motivated to provide ESD protection circuits to protect *Reiner*’s gate driver 63 because a POSITA would have wanted to protect both driver circuits, as taught by *Takahara*, from ESD damage that can “destroy[]” the “very sensitive circuits” inside of the drivers, which could render the LCD display unacceptably or irreparably damaged and unfit for use by ESD events at either the gate driver (scanning line driving circuit) or the source driver (data line driving circuit). *Reiner*, 2:28-3:1; *Takahara*, [0066].

239. A POSITA would have been motivated to “add an ESD protection network to [the] densely packed integrated circuit devices” of *Reiner*’s gate driver 63, such as shown in *Reiner*’s FIG. 5, because *Takahara* teaches that ESD protection circuits “reliably protect[]” both gate and scanning line drivers. *Reiner*, 4:15-16; *Takahara*, [0066]. A POSITA would have recognized that *Reiner*’s “densely packed” gate driver 63 with includes “very sensitive” internal circuit elements would have benefitted from ESD protection to prevent them from being “destroyed” and therefore been motivated to protect them from ESD events and damage. *Reiner*, 2:28-3:1, 4:15-16.

240. A POSITA would have also recognized that using the “ESD protection network” of *Reiner*’s FIG. 5 to protect “each output device” of the gate driver 63 (the driver unit equivalent to output device 70 for each scan line) merely implements *Reiner*’s known prior-art ESD protection network to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s]” of gate driver 63, which *Takahara* confirms can be protected by ESD protection circuits and was “conventional art” as admitted by the ’157 patent. *Reiner*, 4:15-16, 10:10-12; *Takahara*, [0066], FIGS. 1, 3; Ex. 1001, 1:25-2:30. Similarly, a POSITA would have been motivated to implement *Reiner*’s known ESD protection technique to protect gate driver 63 in the same way as the example in FIG. 5, and

Takahara confirms that such protection is beneficial and was conventional in the prior art. *See Reiner*, 2:28-3:1. At a minimum, a POSITA would have found it obvious to try implementing *Reiner*'s ESD protection network shown in FIG. 5 to protect gate driver 63 and its many output devices, given *Reiner*'s suggestion that both source driver 61 and gate driver 63 are "integrated circuits" and contain "very sensitive circuits" can be "destroyed" by electrical or thermal ESD damage when ... subjected to [an ESD] discharge event." *Reiner*, 2:28-3:1, 9:12-14; *see also Takahara*, [0066], FIG. 1 (confirming that both scanning line driving circuits and data line driving circuits can be protected by ESD protection circuits).

241. A POSITA also would have been motivated to implement a first and second ESD protection circuit connected to *Reiner*'s gate driver 63, in the configurations described above in Ground 1, claim 4, to protect *Reiner*'s gate driver 63 from ESD events both electrically and thermally, and also connected to the power supply line, such as Vss and/or Vdd, for the reasons set forth in Ground 1, claim 4. *Reiner*, 4:10-12, 9:16-22, 4:15-19, 12:15-18, claim 11.

ii. Expectation of Success

242. A POSITA would have had a reasonable expectation of success in implementing first and second ESD protection circuits to protect *Reiner*'s gate

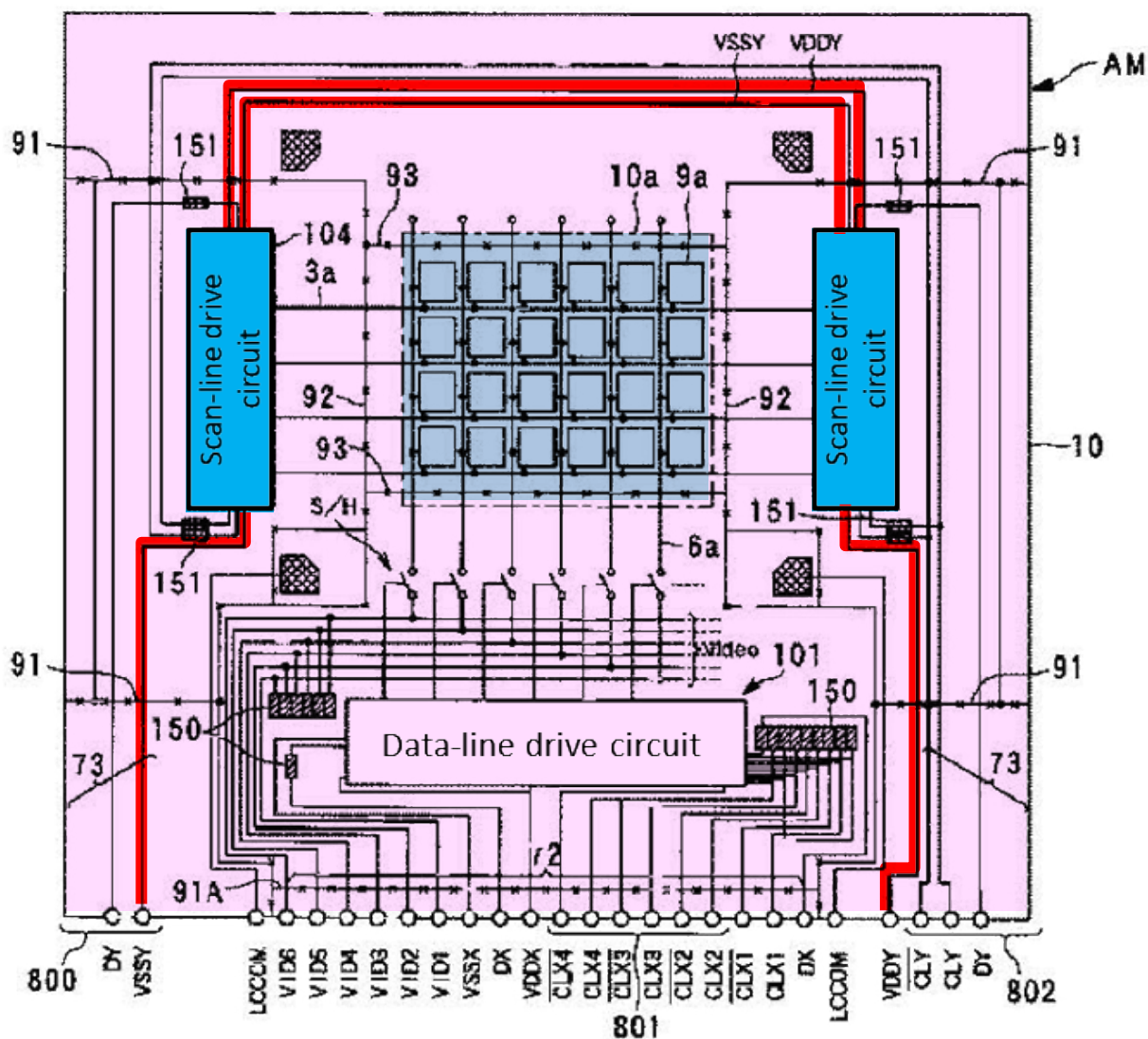
driver 63 and its output units as recited in claim 4 for the reasons I discussed above for Ground 1, claim 4. *Supra* §§ X.A.1.e-X.A.1.g.

2. Claim 8

243. As an alternative opinion, in the situation that *Reiner* is found not to disclose or render obvious the additional limitations of claim 8, then in my opinion, *Reiner* and *Takahara* would have rendered them obvious to a POSITA.

244. *Takahara* discloses that a scan-line drive circuit 104 is arranged on a substrate 10 that also includes the active matrix for the LCD display. *Takahara*, [0064], FIG. 1. The scanning lines 3a and data lines 6a are formed on the substrate 10 and intersect at the active matrix pixel locations, and the scan-line drive circuit 104 and power supply lines VDDY/VSSY are located on the periphery of the substrate 10. *Takahara*, [0062], FIG. 1.

FIG. 1



Takahara, FIG. 1.

245. A POSITA would have recognized that the display of *Reiner's* FIG. 4 would also have included a similar configuration to be placed on a substrate to

support the gate/scan lines 68, the source/data lines 67, pixels, and driver circuits 61, 63. This was well known in the art. *See Murai* [0017]-[0019], [0035], FIG. 1; Ex. 1001, FIG. 11.

246. Although *Takahara*'s FIG. 1 shows an active matrix of 4x6 pixels, as I explain in Ground 1, claim 8, a POSITA would have recognized that the active matrix typically has several hundred to a thousand or more scan and data lines, rendering the peripheral area a small fraction of the overall substrate and display and that the ends of the scanning line drive circuits would have included the first and second protection circuits, and at least the first few and last few scan lines of the driver circuit, in the corner portions of the substrate, as shown below in FIG. E.

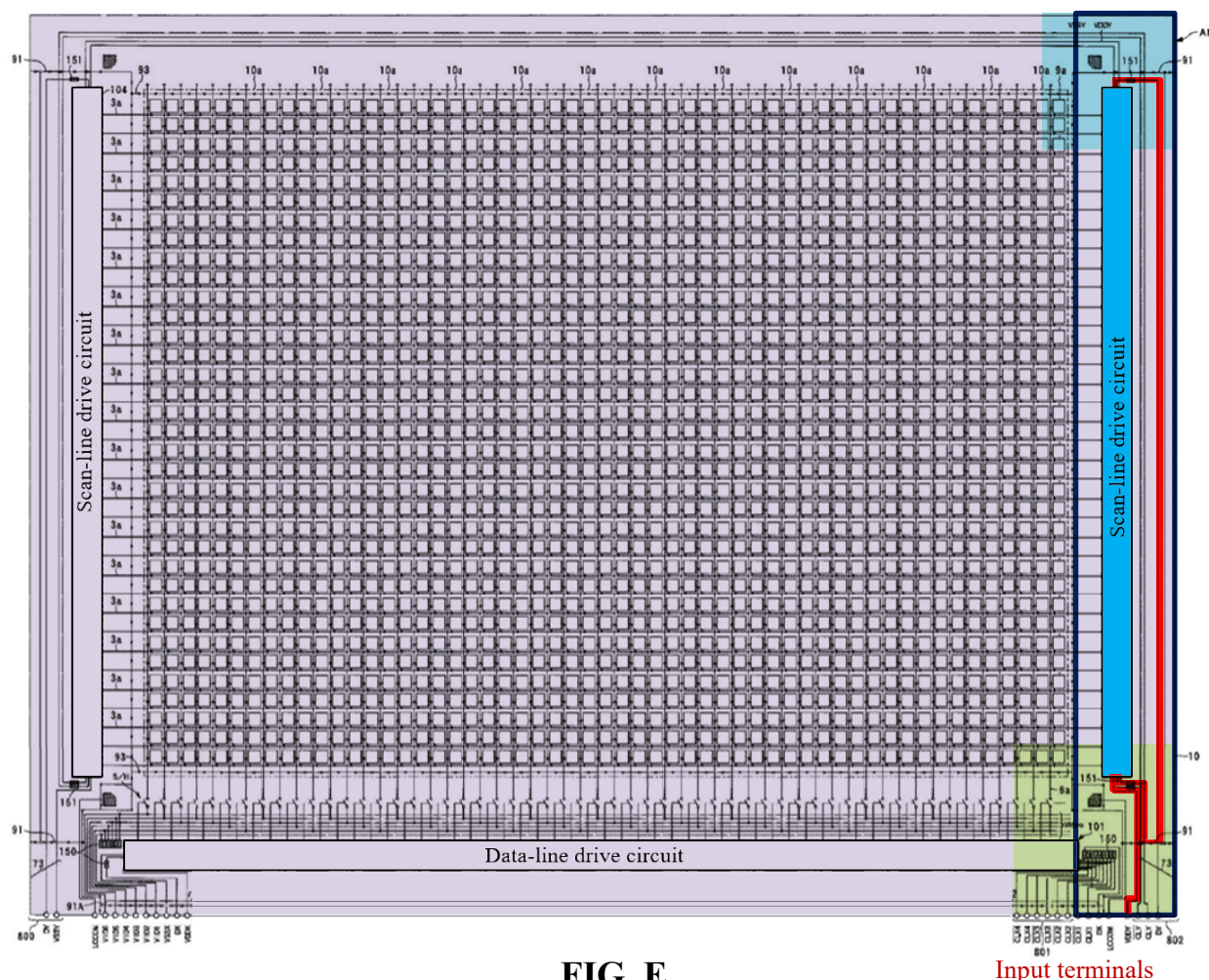
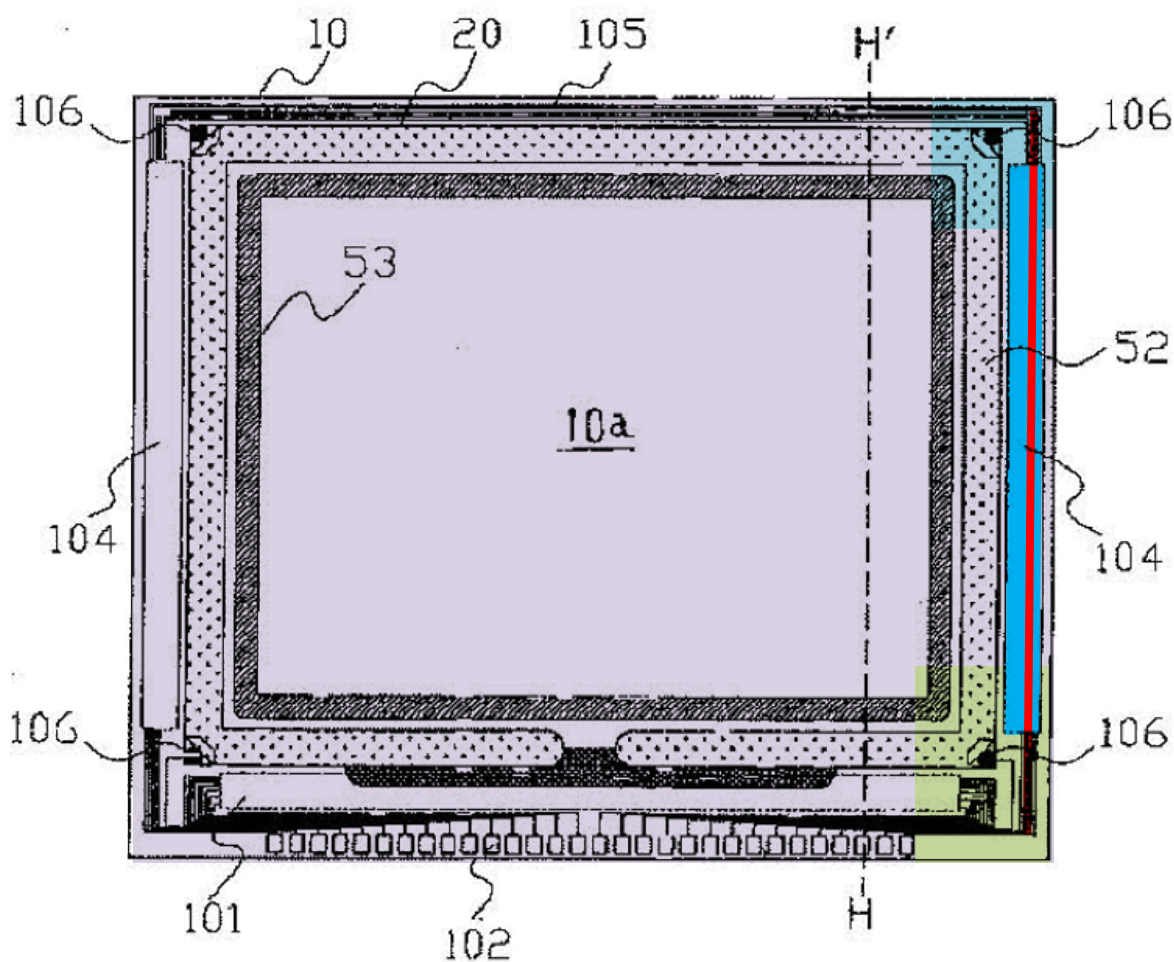


FIG. E

Input terminals

247. The disclosure is confirmed by *Takahara*'s FIG. 12, which shows “a plan view of a TFT-array substrate and each structural element formed thereon.” *Takahara*, [0131]. As shown in FIG. 12, the scan-line drive circuit 104 is on the periphery of the substrate with the power supply lines running into the scan-line drive circuit on both sides at the first corner portion and second corner portion of the substrate and therefore following the periphery of the substrate as they pass from one corner portion to the other through the scan-line drive circuit 104.

FIG. 12



Takahara, FIG. 12.

i. Motivation

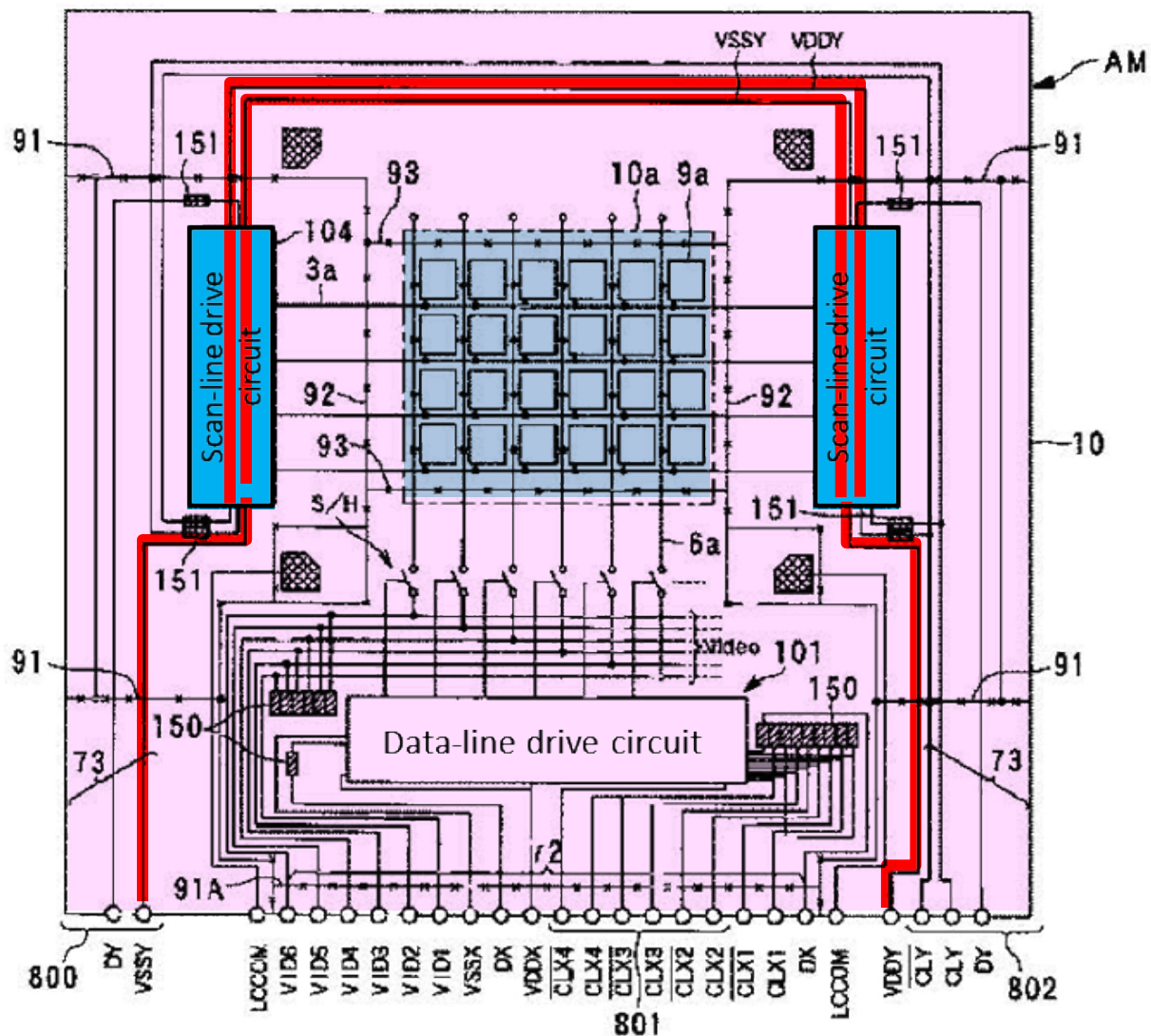
248. A POSITA would have been motivated to arrange *Reiner*'s source driver 63 on a substrate to support the LCD display device of *Reiner*'s FIG. 4 and provide locations for wiring and circuitry, as disclosed by *Takahara* and well known and conventional in the art. *Reiner*, for example, discloses the driver unit

having a silicon substrate 21 and being bonded to the driven lines (e.g., source line or gate line) at contact pad 72. *Reiner*, 6:18-24, 10:1-6, FIGS. 4, 5. A POSITA would have been motivated to arrange *Reiner*'s gate driver 63 and active matrix on a substrate and to connect the gate driver to the scan lines being drive on the substrate to provide an integrated display unit (e.g., *Reiner* FIG. 4) that can be incorporated into electronic devices as a display for a laptop computer, PDA, television, computer monitor, cellular phone screen, or other device. *Takahara*, [0064]. A POSITA also would have been motivated to arrange the gate driver on a substrate to provide external terminals to power the active matrix and the driver circuits, such as to connect to the CPU and power sources, such as an external power supply or battery of the electronic device. *Takahara*, [0064].

249. A POSITA would have been motivated to provide for the power supply lines for feeding into and supplying power to *Reiner*'s gate driver 63 (scanning line driving unit) to be formed on the substrate, as shown in *Takahara*'s FIG. 1, because *Reiner* teaches that the power supply lines run "perpendicular to" the output lines (scan lines) of the driver unit output devices of the driver circuits. *Reiner*, 10:7-10. A POSITA would have recognized that the most efficient way to run the power supply lines for gate driver 63 (whose outputs are *Reiner*'s scan lines 68; *Takahara*'s scan lines 3a) would be perpendicularly along the substrate's

periphery, as shown in *Takahara's* FIG. 1. As a result, a POSITA would have found it obvious to locate the first and second protection circuits in the first and second corner portions of the substrate, as I explain above for the combination here in claim 8 and in claim 4, and also as I explain in Ground 1, claim 8.

FIG. 1



Takahara, FIG. 1.

250. As I explain above for Ground 2, claim 4, a POSITA also would have been motivated to form *Reiner*'s gate driver 63, including the protection circuits, directly on *Takahara*'s glass substrate to provide better ESD protection against static electricity and the electrical and thermal damage it can cause to the sensitive circuits. *Supra* § X.B.1.b. A POSITA also would have been motivated to form *Reiner*'s gate driver 63, including the protection circuits, directly on *Takahara*'s glass substrate with the scanning lines and power lines to eliminate the need to attach it via contact pads and to simplify the manufacturing of the overall display.

ii. Expectation of Success

251. A POSITA would have reasonably expected to succeed in arranging *Reiner*'s gate driver 63 on a substrate with power supply lines Vss 61 and Vdd 63 following the periphery of the substrate from a first corner portion to a second corner portion, such that the first and second protection circuits are placed in the first and second corners portions, respectively, as taught by *Takahara*. Arranging scanning line driving circuits on substrates was "conventional art" of LCD displays that *Reiner*, *Takahara*, and the '157 patent each describe. *Reiner*, 7:23-25; Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751); *Takahara*, [0063], [0066], FIG. 1; *see also Murai*, FIG. 1.

252. Arranging *Reiner's* gate driver, scan lines, and power lines, such as shown in FIG. 4, on a substrate to facilitate manufacturing of the LCD display with the power lines running perpendicular to the scan lines, as taught by *Reiner* and *Takahara*, to provide power to the gate driver 63 would have been merely the straightforward application of known, conventional techniques applied to *Reiner's* gate driver 63 and patterning of power supply lines Vss 71, Vdd 73 on a substrate in the layout of *Takahara*. This is confirmed by *Murai*, as explained above.

Furthermore, arranging the gate driver 63 and the power lines perpendicularly on the substrate, as claimed, would have used only conventional techniques to either manufacture the supply lines and driver circuit on the substrate or to fabricate the driver circuit and then attach it via contact points, such as contact pads 72, to the power lines and scan lines, as taught by *Reiner*, according to their known functions to yield predictable results. *See Reiner*, 9:12-13, 9:18-20, 9:27-29, 10:6-10, 12:4-5.

Alternatively, as I explain above, forming *Reiner's* gate driver 63 directly on the substrate would have eliminated the need for contact pads 72 and also simplified manufacturing using well-known techniques for forming integrated circuits on glass substrates.

3. Independent Claims 1, 10, 16, 17, and 18

253. *Reiner* and *Takahara* render obvious the “input terminal,” connection, and protecting the scanning line driving circuit/power line/circuit element limitations of claims 1, 10, 16, 17, and 18 for the reasons discussed in Ground 2, claim 4, and also discussed in claims 1, 10, 16, 17, and 18 in Ground 1.

254. As an alternative opinion, I have been asked to consider the situation if *Reiner* is found not to disclose or render obvious the first protection circuit and the second protection circuit being at a first end and a second end of the scanning line driving circuit, as recited in claims 16-18. In this case, in my opinion, *Reiner* and *Takahara* would have rendered these limitations obvious to a POSITA for the reasons discussed for Ground 2, claim 8.

4. Claims 2 and 14

255. Claims 2 and 14 are substantively similar to claim 8. In my opinion, *Reiner* and *Takahara* would have rendered obvious claims 2 and 14 to a POSITA for the reasons discussed above for Ground 2, claim 8.

5. Claims 3, 5, 6, 7, 9, 11, 12, 13, and 15

256. *Reiner* discloses or renders obvious the additional limitations of claims 3, 5, 6, 7, 9, 11, 12, 13, and 15 for the reasons discussed above in Ground 1.

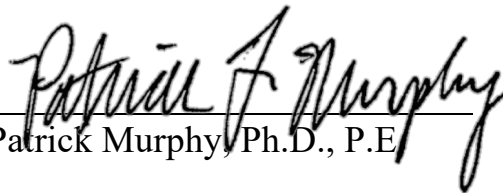
XI. CONCLUSION

257. For the reasons set forth above, it is my opinion that claims 1-18 of the '157 patent would have been obvious to a POSITA.

Declaration of Patrick Murphy, Ph.D., P.E.
U.S. Patent No. 9,184,157

I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 3, 2024

By: 
Patrick Murphy, Ph.D., P.E.