

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case IPR2024-00973
Patent No. 9,184,157

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,184,157 to Kobashi (“the ’157 patent”)
Ex. 1002	File History for U.S. Patent No. 9,184,157
Ex. 1003	Declaration of Dr. Patrick Murphy, Ph.D., P.E. (“Murphy”)
Ex. 1004	Curriculum Vitae of Dr. Patrick Murphy, Ph.D., P.E.
Ex. 1005	International Publication No. WO03/019657 A2 to Reiner et al. (“ <i>Reiner</i> ”)
Ex. 1006	Japanese Patent Application Publication No. JP2003-121875 to Takahara
Ex. 1007	Certified English Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara (“ <i>Takahara</i> ”)
Ex. 1008	Certificate of Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara to English
Ex. 1009	Japanese Patent Application Publication No. JP2001-166334 to Murai
Ex. 1010	Certified English Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai (“ <i>Murai</i> ”)
Ex. 1011	Certificate of Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai to English
Ex. 1012	James E. Vinson & Juin J. Liou, “Electrostatic Discharge in Semiconductor Devices: An Overview,” Proceedings of the IEEE, Vol. 86, No. 2, pp. 399-418 (Feb. 1998)
Ex. 1013	Toshio Murakami et al., “Electrostatic problems and ionization solutions in TFT-LCD Production,” Solid State Technology, Vol. 40, No. 1, pp. 99-102 (Jan. 1997)

Exhibit	Description
Ex. 1014	Complaint for Patent Infringement filed in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP, Dkt. 1 (E.D. Tex.) (Nov. 8, 2023)
Ex. 1015	Docket Control Order in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP, Dkt. 37 (E.D. Tex.) (Apr. 9, 2024)
Ex. 1016	Plaintiff's Infringement Contentions in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP (E.D. Tex.) (Mar. 11, 2024)
Ex. 1017	Excerpt from Federal Court Management Statistics—Profiles (Dec. 31, 2023), <i>available at</i> https://www.uscourts.gov/sites/default/files/fcms_na_distprofile1231.2023_0.pdf (last accessed May 26, 2024)

I. PRELIMINARY STATEMENT

Petitioner BOE Technology Group Co., Ltd., requests *inter partes* review of U.S. Patent No. 9,184,157, assigned to Patent Owner 138 East LCD Advancements Limited, and cancellation of claims 1-18. The challenged claims are directed to semiconductor devices and display devices and protecting such devices from electrostatic damage (“ESD”). The ’157 patent admits that the conventional prior art used an ESD protection circuit connected to a power line to protect a scanning line driving circuit from ESD. The ’157 patent purports to improve on the prior art by adding an additional protection circuit to protect the scanning line driving circuit. But the prior art already taught the same purported advancement, including in International Publication No. WO03/019657 (“*Reiner*”) and Japanese Patent Application Publication No. JP2003--121875 (“*Takahara*”).

As explained below, claims 1-18 would have been obvious based on *Reiner* or, alternatively, the combination of *Reiner* and *Takahara*. The Examiner did not consider *Reiner* or *Takahara* during examination. The Board should thus institute review and cancel all challenged claims.

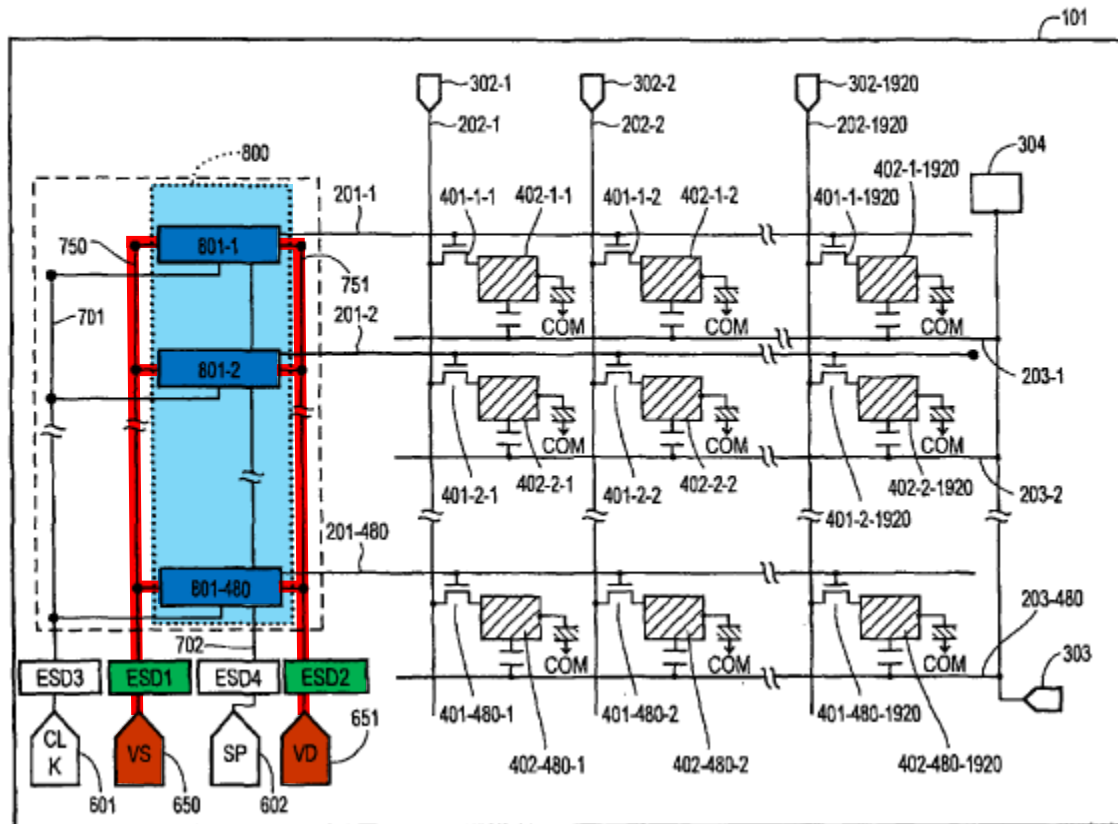
II. STATE OF THE ART AND ADMITTED CONVENTIONAL ESD PROTECTION

As was known before the ’157 patent, “it is important to take measure[s] against the electro-static damages (ESD) when a high voltage caused by static

electricity ... is unintentionally applied to the inside of the device to damage an insulating film, thereby causing a fatal damage to the device.” Ex. 1001, 1:14-19, 1:23-28. “[C]onventionally,” ESD protection was provided by “protective circuits ... formed between [the] input terminals and the semiconductor device.” *Id.*, 1:28-32, 1:47-56.

Figure 11 shows this “conventional art” having “scanning line driving unit 800” that includes “scanning line driving unit circuits” (801-1 to 801-480) to drive “scanning lines” (201-1 to 201-480). *Id.*, 1:57-2:2. Each scanning line driving unit circuit “is connected to a low potential power line 750 [VS] and a high potential power line 751 [VD], through which power is supplied” from terminals 650, 651. *Id.*, 2:5-15. To “prevent TFTs [thin film transistors]” in each scanning line driving unit circuit 801-n from “being damaged by static electricity,” “static electricity protection circuits [ESD1, ESD2]” are “provided between the input terminals” 650, 651 and “scanning line driving unit circuits 801-1 to 801-480.” *Id.*, 2:20-28.

FIG. 11
Related Art



Id., FIG. 11.¹

The state of the art confirms that ESD protection circuits were conventionally used to protect scanning line driving circuits from ESD. *See* Ex. 1003, Murphy Decl. (“Murphy”), §§ V-VI.

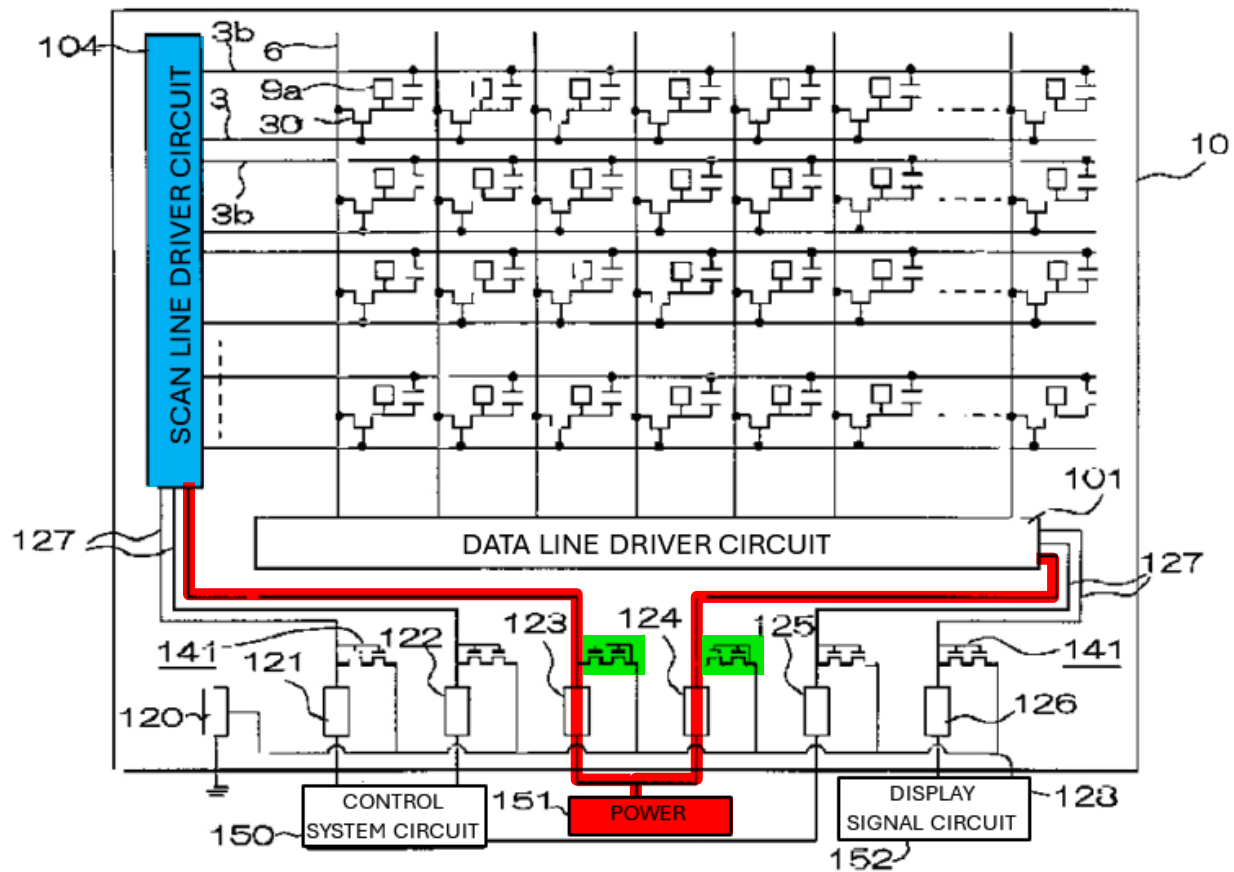
For example, *Murai* describes protecting many locations in an LCD device from ESD. *Murai*’s FIG. 1 shows “external-circuit connection terminal portions

¹ All colors and colored annotations added to figures unless otherwise noted.

123, 124” that are connected to “power circuit [151]” to power “scan line driver circuit 104” and “data line driver circuit 101.” *Murai*, [0021]-[0022].² To “prevent[] ... electrostatic breakdown of the driver circuit caused by static electricity,” an “electrostatic-breakdown-preventing circuit” 141 is provided “partway along a wire connecting the external-circuit connection terminal portion and the driver circuit.” *Murai*, [0003], [0021], FIG. 1.

² Citations to *Murai* are to the English translation (Ex. 1010).

FIG. 1



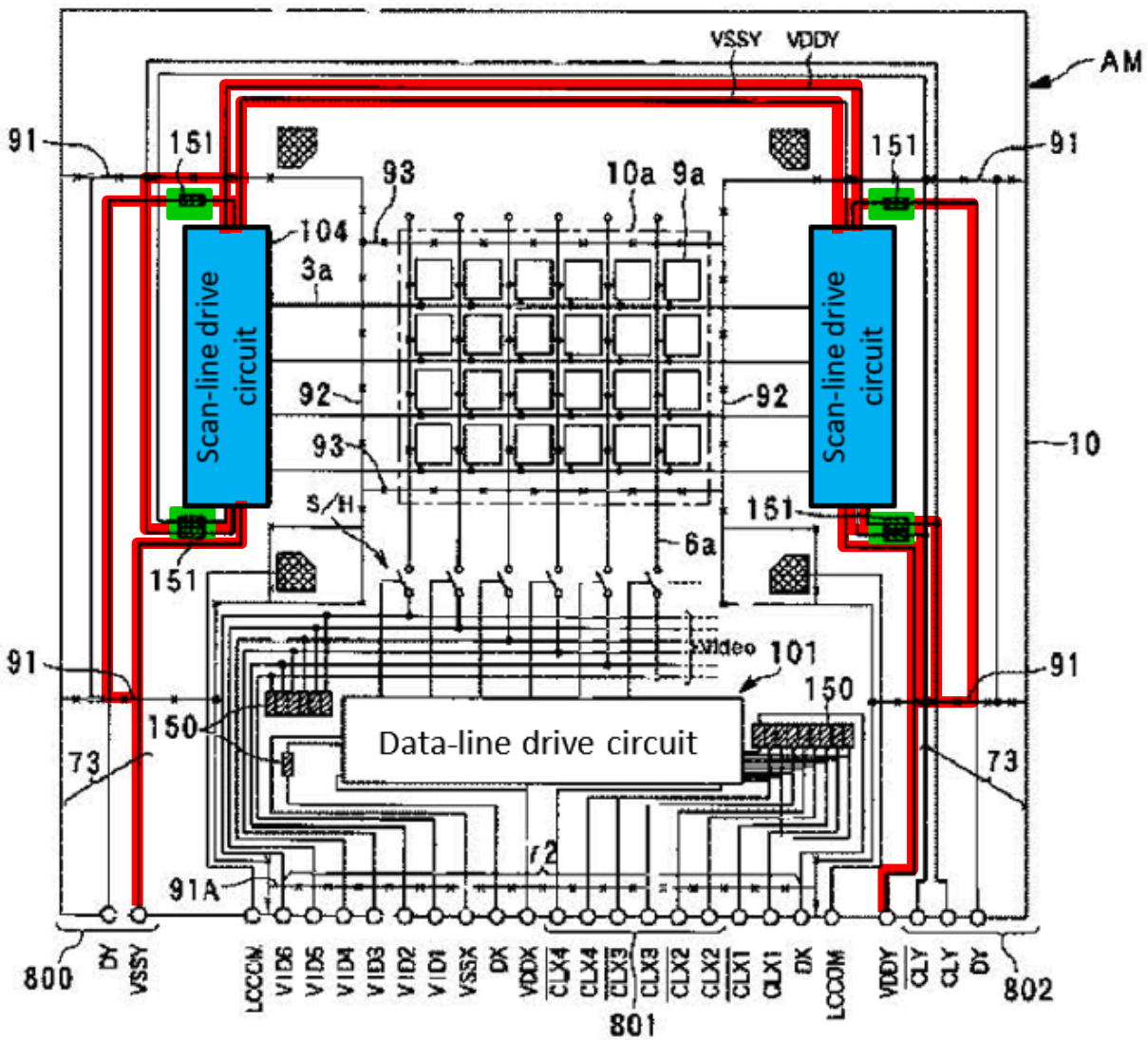
Murai, FIG. 1.

Takahara similarly teaches using multiple protection circuits, including “[e]lectrostatic-protection circuits 150 and 151 [that] are formed at intermediate locations” of “signal wirings” 73 so that “static electricity is reliably absorbed” and “scan-line drive circuit 104 can be reliably protected.” *Takahara*, [0066], FIG. 1. Power lines VDDY, VSSY are shorted to ESD protection circuits 150, 151 by

shorting wiring lines 91 to protect both ends of scan-line drive circuit 104.

Takahara, [0070].

FIG. 1



Takahara, FIG. 1.

Reiner likewise teaches “integrated circuit devices with ESD protection.”

Reiner, 2:2-3.³ A “typical example” of a protected integrated circuit device is “integrated circuit display driver 61 or 63,” such as “gate driver 63” ([scanning line driving circuit](#)) that drives gate (scan) lines 68 of LCD display 60 in FIG. 4.

Reiner, 9:11-14, 9:27-28.

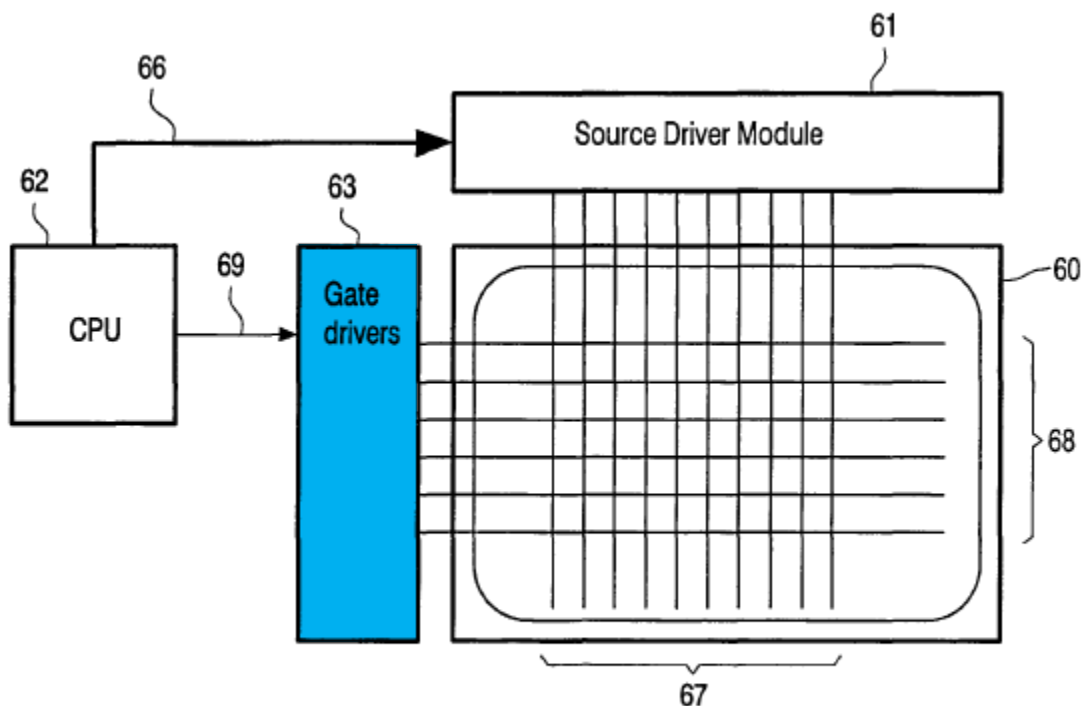


FIG. 4

Reiner, FIG. 4.

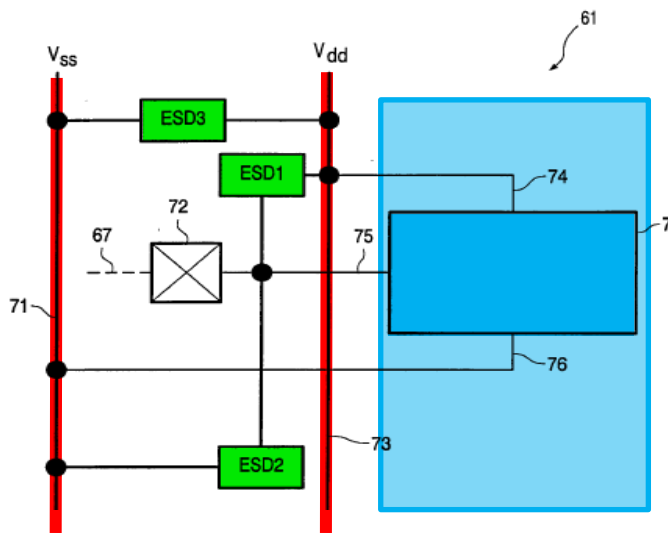
³ *Reiner* citations are in page:line format. Page numbers refer to exhibit page numbers, not original page numbers.

Reiner explains that, “[q]uite often,” integrated circuit devices “comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when subjected to a discharge event.” *Reiner*, 2:28-3:1. *Reiner* explains that it is advantageous “to add an ESD protection network to densely packed integrated circuits” and that its teachings are “well suited” for such circuits. *Reiner*, 4:15-16, 8:8-10. *Reiner* describes an “ESD protection network” having “three ESD devices ESD1, ESD2, and ESD3 ... for each output device 70, in order to protect the circuitry inside the devices 70.” *Reiner*, 10:10-12. As explained below, a POSITA would have understood that *Reiner*’s ESD protection network applies to both source/data line driver 61 and gate/scanning line driver 63.

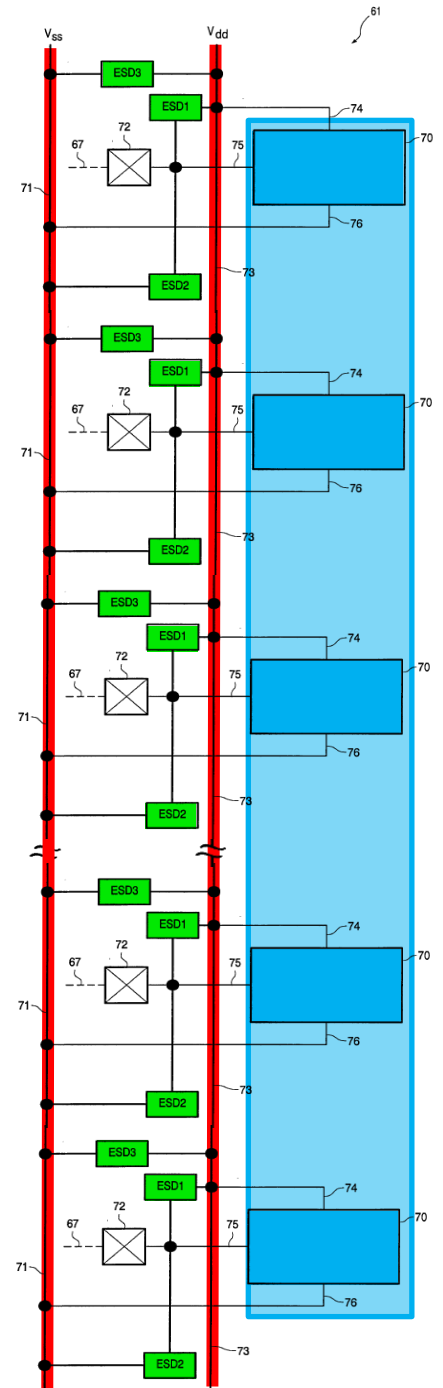
Reiner’s FIG. 5 shows an ESD protection network connected to supply voltage power lines Vdd, Vss and “connect[ed] ... with the inputs and/or outputs of the integrated circuit device [e.g., source driver 61, gate driver 63] to be protected” at “each output device [70].” *Reiner*, 3:4-8, 4:15-16, 8:11-15, 10:1-15. “[T]hree ESD devices” are provided “for each output device 70” and therefore replicated at each “output device[] of the integrated circuits 61 or [63].”⁴ *Reiner*,

⁴ *Reiner*’s reference to 62 is a clear typographical error and should refer to gate driver 63. Ex. 1003 (“Murphy”) ¶56, n.5.

9:10-14, 9:18-22, 10:1-15, FIG. 5. Figure 5 shows one such protection network and composite FIG. F from Petitioner's expert, Dr. Murphy, shows *Reiner's* teaching that each output device in the integrated circuit 61, 63 includes the three-ESD protection network.



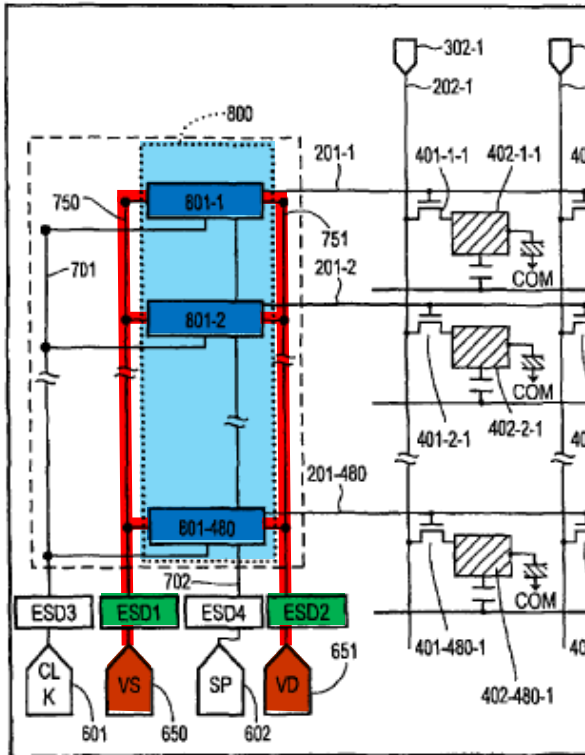
Reiner, FIG. 5



Ex. 1003 (“Murphy”), FIG. F

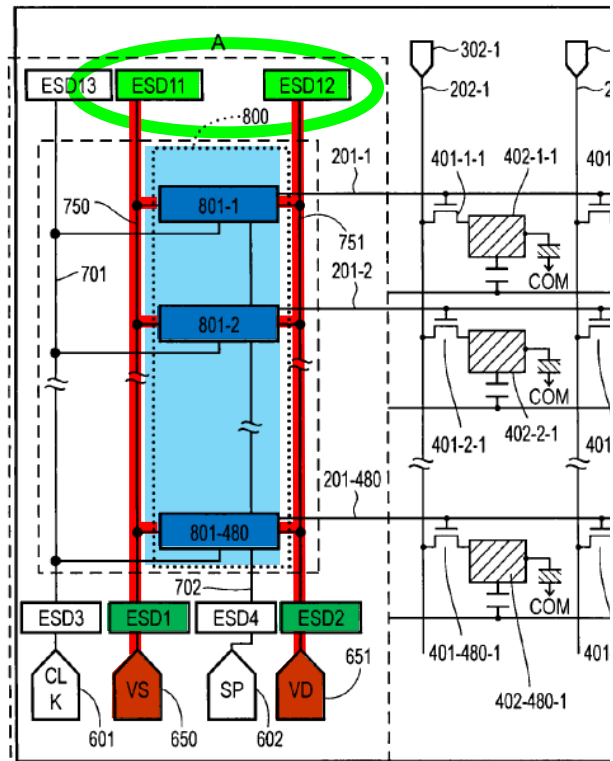
III. THE '157 PATENT

The '157 patent purports to improve the admitted conventional prior art of FIG. 11 by adding additional ESD protection circuits. Ex. 1001, FIGS. 1-3. The embodiment in FIG. 1 shows **second ESD circuits ESD11/ESD12** added to **power lines 750, 751**, highlighted in the excerpted figure comparison below, but no other differences from FIG. 11.



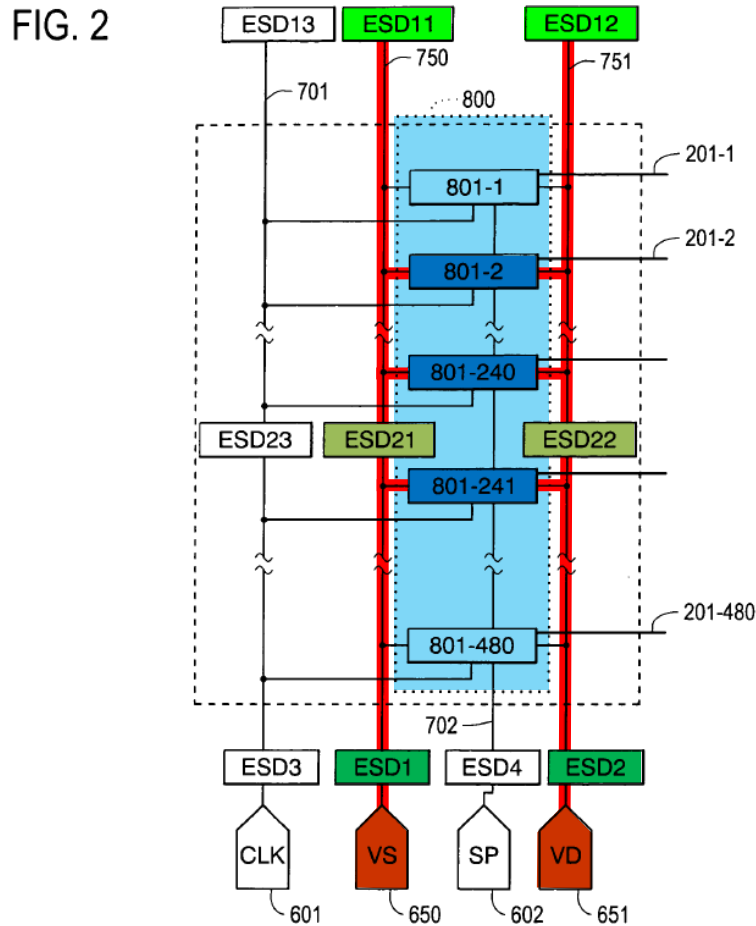
Id., FIG. 11 (excerpted)

(admitted prior art)



Id., FIG. 1 (excerpted)

The '157 patent also describes adding additional ESD protection circuits ESD21 and ESD22 “between the unit driving circuit 801-240 ... and the unit driving circuit 801-241,” as shown in FIG. 2. *Id.*, 7:25-34.



Id., FIG. 2.

In another embodiment, “[m]ost preferably, the protective circuits are interposed between *all stages* [801-n]” *Id.*, 7:46-51 (emphasis added).

But the prior art taught protecting the scanning line driving circuits and circuit elements by interposing ESD protection circuits between each scanning line driver unit stages. *See* §§ II, VII.

IV. CLAIM CONSTRUCTION

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Claims are construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.

V. STATEMENT OF PRECISE RELIEF REQUESTED

A. Prior Art

International Publication No. WO03/019657 (“*Reiner*”; Ex. 1005), published March 6, 2003, is prior art to the ’157 patent under pre-AIA 35 U.S.C. § 102(a)-(b). *Reiner* is analogous art because it is directed to the same field of endeavor as the ’157 patent—semiconductor devices and display devices, and protecting semiconductor devices (driving circuits) with ESD protection circuits. *Reiner*, 2:1-3, 2:28-3:1, 4:15-16, 8:8-15, 9:12-14, 10:1-15, 12:23-25, FIG. 5; Ex. 1001, Abstract, 1:10-13, FIG. 1. *Reiner* is also directed to the same problem as the ’157 patent, for example, “integrated circuit devices with ESD protection” to prevent damage from ESD to the circuits. *Reiner*, 2:1-3, 2:28-3:1, 4:15-16, 8:8-15, 9:12-14, 10:1-15, 12:23-25, FIG. 5; Ex. 1001, Abstract, 1:10-13, FIG. 1; Murphy ¶82.

Japanese Application Publication No. JP2003-121875 (“*Takahara*”;⁵ Ex. 1006; Ex. 1007 (translation)), published April 23, 2003, is prior art to the ’157 patent under pre-AIA 35 U.S.C. § 102(a)-(b). *Takahara* is analogous art because it is directed to the same field of endeavor as the ’157 patent—semiconductor devices and display devices, and protecting semiconductor devices (driving circuits) with ESD protection circuits. *Takahara*, [0003], [0057], [0066], FIG. 1; Ex. 1001, Abstract, 1:10-13, FIG. 1. *Takahara* is also directed to the same problem as the ’157 patent, for example, “reliably protect[ing]” a driver circuit from “static electricity” damage. *Takahara*, [0003], [0057], [0066], FIGS. 1, 3; Ex. 1001, Abstract, 1:10-13, FIG. 1; Murphy ¶84.

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1-18	§ 103	<i>Reiner</i>
2	1-18	§ 103	<i>Reiner</i> and <i>Takahara</i>

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar

⁵ Citations to *Takahara* are to the English translation.

field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional relevant work experience can compensate for less education, and *vice versa*. For example, a master's degree in electrical engineering, computer science, physics, or a similar field can substitute for two years of experience designing semiconductor display devices. Murphy ¶76.

VII. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

A. Ground 1: Claims 1-18 Are Rendered Obvious by *Reiner*

Reiner renders obvious claims 1-18. Murphy ¶¶86-227.

The Grounds present claims 4-18 before claims 1-3, because claims 1-3 generally include similar elements to claims 4-18, but add a third protection circuit between two adjacent scanning line driving unit circuits.

1. Independent Claim 4

a. [4pre]: “A display device, comprising:”

To the extent the preamble is limiting,⁶ *Reiner* discloses [4pre]. Murphy ¶89. FIG. 4 shows a “block diagram of an LCD [liquid crystal display] display with control circuitry,” including “LCD screen 60,” gate/scanning line driving circuit

⁶ Petitioner reserves the right to dispute whether the preambles are limiting. The Board need not resolve the issue.

63, source/data line driving circuit 61, gate/scanning lines 68, and source/data lines 67. *Reiner*, 6:7, 9:24-26. Murphy ¶89.

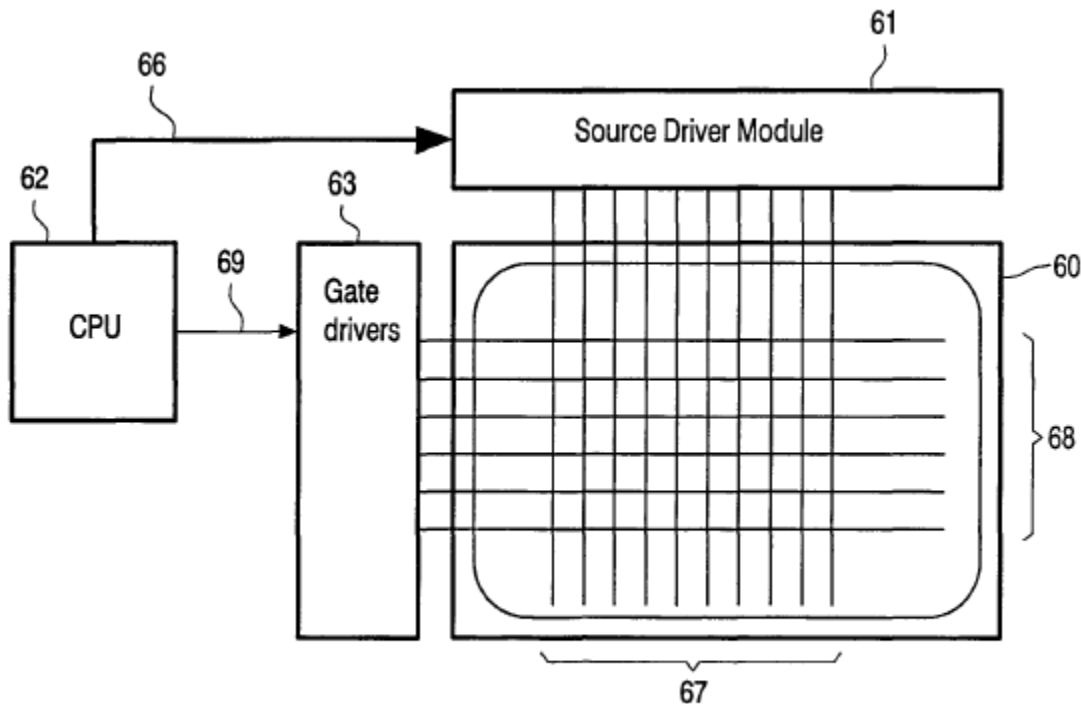


FIG. 4

Reiner, FIG. 4.⁷

b. [4a]: “a scanning line driving circuit;”

Reiner discloses the limitations of [4a]. Murphy ¶¶90-92.

Reiner discloses the LCD device 60 including a scanning line driving circuit.

Reiner, 9:12-14, 9:25-31. For example, *Reiner* discloses gate driver 63 (scanning

⁷ All colors and colored annotations added to figures unless otherwise noted.

line driving circuit) “designed to drive many lines of an LCD display 60,” such as “gate lines 68,” as shown in FIG. 4. *Reiner*, 9:11-14, 9:25-26.

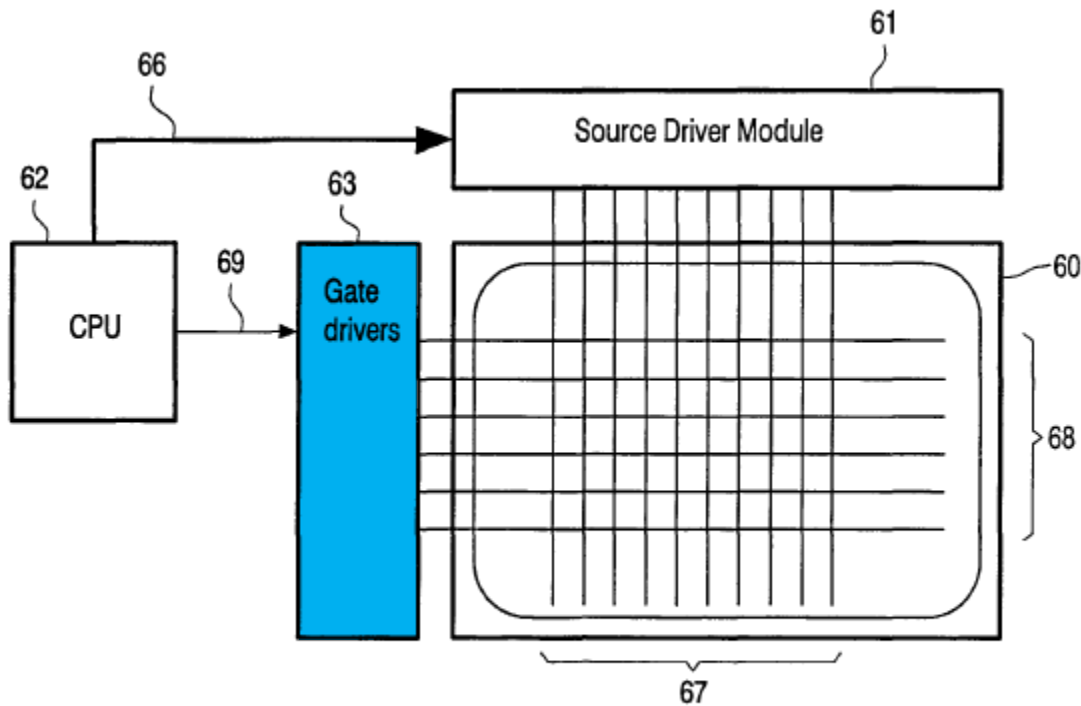


FIG. 4

Reiner, FIG. 4.

Gate driver 63 “usually drives one whole gate line 68” using “row timing signals” sent by CPU 62 *Reiner*, 9:25-31. A POSITA would have recognized that gate driver 63 describes a scanning line driving circuit because it scans each of the horizontal gate lines 68 of the LCD display using the row timing signals. *Reiner*, 9:25-31. Murphy ¶92.

- c. [4b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”

Reiner discloses the limitations of [4b]. Murphy ¶¶93-95.

Reiner’s teachings are “well suited for integrated circuit devices operating with two or more **supply voltages** (e.g., **Vdd**, Vee and **Vss**)” (**power supply lines**). *Reiner*, 12:4-5. A “typical example” of an integrated circuit device is “**integrated circuit display driver** 61 or **63**” of “LCD display 60.” *Reiner*, 9:12-14. *Reiner* teaches “many output devices of the **integrated circuit device** 61 or **62** [*sic*: 63] ... cross the **power supply lines** *which provide supply voltage* (e.g., **Vdd**) to the **output devices**” of integrated circuits 61 and 63. *Reiner*, 9:18-22 (emphasis added). FIG. 5 shows **power supply line Vdd** **connected to driver unit 70 through connection 74** and **power supply line Vss** **connected to driver unit 70 through connection 76**. Although FIG. 5 shows an exemplary source driver circuit 61, a POSITA would have recognized that it also describes gate driver 63 based on *Reiner*’s description that **power supply lines Vdd/Vss** are connected to source driver 61 and **gate driver 63 to supply power** to the individual **driver output units** of the driver. *Reiner*, 9:18-22; Murphy ¶¶94.

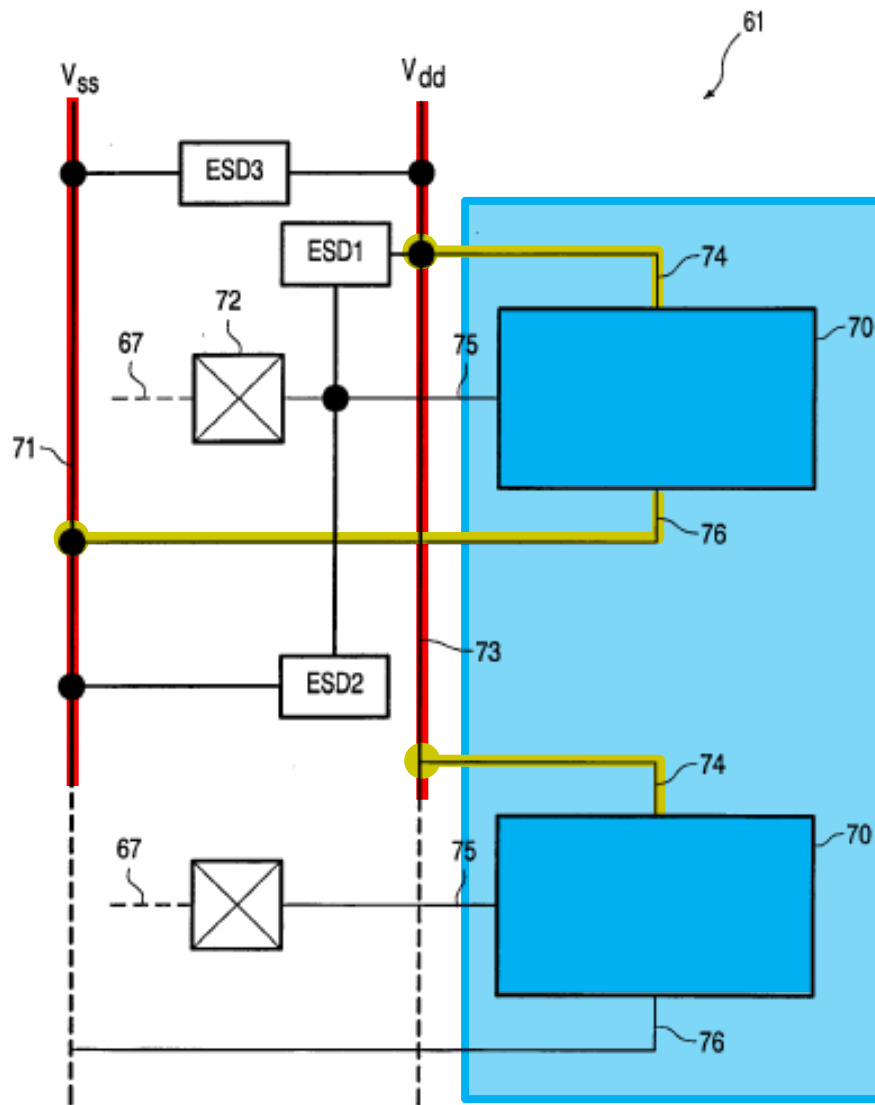


FIG. 5

Reiner, FIG. 5.

A POSITA would have recognized that V_{dd} and V_{ss} are nomenclatures for a high potential power supply line and low potential power supply line, respectively.

Murphy ¶95.

d. [4c]: “an input terminal connected to the power supply line to supply power; and”

Reiner suggests or renders obvious the limitations of [4c]. Murphy ¶¶96-102.

As explained for [4b], *Reiner* discloses power supply lines Vdd/Vss that supply power to gate driver 63 (scanning line driver circuit). “[P]ower supply line 73” “provides the supply voltage Vdd through connection 74” and “second power supply line 71” “provides the supply voltage Vss through connection 76” to “the output devices 70” of source driver 61. *Reiner*, 10:7-9. A POSITA would have understood that this description is exemplary and also applies to gate driver 63 (scanning line driving circuit), as explained for [4a] and [4b]. Murphy ¶97.

A POSITA would have understood that power supply lines 71, 73 would require input terminals to drive output devices 70 of gate driver 63 or source driver 61 (each an integrated circuit 20) so that power can be provided from the power source to the driver units to drive the LCD display 60. Murphy ¶98.

If Patent Owner argues or the Board finds that *Reiner* does not disclose [4c], a POSITA would have found it obvious to provide input terminals to supply power to power supply lines 71, 73 because it was conventional to do so and because there would need to be an input terminal to create a connection between the power

lines Vdd/Vss of the scanning line driving circuit and the power source for the LCD display. Murphy, ¶99.

The '157 patent admits that the “conventional art” shown in FIG. 11 shows a “low potential power line 750” (VS) and “high potential power line 751” (VD) being “connected to a low potential power terminal 650” and “high potential power terminal 651,” respectively. Ex. 1001, 1:54-56. These terminals are “supplied with reference potentials” VS and VD, which correspond to *Reiner*’s Vss and Vdd power supply lines. Ex. 1001, 2:8-14. A POSITA would have found it obvious, and indeed “conventional,” as the '157 patent admits, to provide input terminals to supply the voltages Vss/Vdd to *Reiner*’s power supply lines of the gate driver 63. Murphy ¶100. A POSITA would have recognized that the input terminals would have been above the first ESD3 in FIG. 5, as shown in Dr. Murphy’s composite figures in [4d]-[4f], below, which was conventional in the prior art. Murphy ¶100, *supra* § II.

i. Motivation

A POSITA would have been motivated to provide respective input terminals connected to *Reiner*’s power supply lines 71/73 (Vss/Vdd) because the terminals would be needed to transfer power from a power source to the lines of the gate driver 63 to “drive many lines” of “LCD display 60” to display images. *Reiner*, 9:12-14. A POSITA would have recognized that *Reiner*’s integrated circuits, such

as gate driver 63, can be fabricated and then attached to a substrate by being “flipped onto the substrate 16[]” and would therefore need input terminal power connections to the substrate because the wiring lines for display 60 often run along the substrate, such as shown in FIG. 1 of *Takahara. Reiner*, 7:23-25; *Takahara*, [0063], [0066], FIG. 1 (power supply lines VSSY, VDDY have input terminals 800, 802 for driving scan-line drive circuit 104); *see* Ex. 1001, 1:54-56, 2:5-14, FIG. 11. A POSITA would have been motivated to provide input terminals connected to *Reiner*’s power supply lines to supply power to gate driver 63 to facilitate manufacturing and to connect the power supply lines with the corresponding power source or with the power supply lines of the substrate on which the LCD display is arranged. Murphy ¶101.

ii. Expectation of Success

A POSITA would have reasonably expected to succeed in providing input terminals connected to *Reiner*’s power supply lines Vss and Vdd to supply power to the gate driver 63. Connecting input terminals to power supply lines for scanning line driving circuits was admittedly “conventional art” and therefore would have required only ordinary skill. *Reiner*, 9:18-20; Ex. 1001, 1:54-56, 2:5-14, FIG. 11; *Takahara*, [0063], [0066], FIG. 1. Using input terminals connected to respective power supply lines, such as *Reiner*’s Vss 71 and Vdd 73, to supply power would have been merely the straightforward application of known,

conventional techniques applied to *Reiner*'s power supply lines used according to their known functions to yield predictable results (providing a connection to the power supply lines to power gate driver 63 so that it can scan and drive gate lines 68). Murphy ¶102; *Reiner*, 9:12-13, 9:18-20, 9:27-29, 10:6-10, 12:4-5; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); *Slot Speaker Techs., Inc. v. Apple Inc.*, 680 F. App'x 932, 943-44 (Fed. Cir. 2017).

- e. [4d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,”

Reiner discloses or renders obvious the limitations of [4d]. Murphy ¶¶103-120.

As explained in [4b], *Reiner* “relates to integrated circuit devices with ESD protection.” *Reiner*, 2:2-3, 4:15-16. A “typical example is an integrated circuit display driver 61 or 63” in *Reiner*. *Reiner*, 9:12-14, 12:4-5 (emphasis added).

Reiner's teachings are “well suited for integrated circuit devices operating with two or more supply voltages (e.g., Vdd, Vee and Vss)” (power supply lines).

Reiner, 12:4-5. *Reiner*'s disclosure is “well suited for conducting currents occurring during ESD events” and “avoid[ing] thermal damage caused by high current during an ESD event.” *Reiner*, 12:23-25, 8:8-15; Murphy ¶104. *Reiner*

explains that “[q]uite often *integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection* in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1 (emphasis added).

Reiner’s FIG. 5 shows a “schematic block diagram of a display driver 61” where “ESD protection means can easily be integrated” into the driver circuit. *Reiner*, 9:20-22. This paragraph, however, generally discusses “integrated circuit display driver 61 *or* 63” and “display driver 61, 63,” confirming that both the source driver 61 and the gate driver 63 are “display drivers” to be protected. *Reiner*, 9:11-22 (emphases added). A POSITA would have understood that source driver 61 in FIG. 5 is exemplary and that it applies equally to [gate driver 63](#) ([scanning line driving circuit](#)) because gate driver 63 is also a “driver display circuit.” Murphy ¶105. Indeed, *Reiner* explains that generally “integrated circuit devices” comprise “electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits” from being damaged or destroyed by an ESD discharge event, which does not differentiate between the driver type, thus teaching, or at least suggesting, that both drivers would be protected in similar fashion. *Reiner*, 2:28-3:1; Murphy ¶105.

Reiner teaches “three ESD devices ESD1, ESD2, and ESD3 are provided for each output device 70, in order to protect the circuitry inside the devices 70.”

Reiner, 10:10-12, FIG. 5. Because “three ESD devices” are “provided for *each* output device 70,” a POSITA would have understood that each line driver unit would have its own ESD protection, as shown in the composite FIGS. A1-C1.⁸ The ESD devices are also connected to “a ground terminal” to protect against “a voltage peak” on a power line or output line. *Reiner*, 10:15-17; Murphy ¶106.

FIGS. A1-C1 show only the first three and last two gate driver line-driving units 70,⁹ omitting the other intermediate driver units for scan lines 68. But a POSITA would have understood that there would be as many gate driver line-driving units 70 as there are scanning lines in LCD display 60. Murphy ¶107.

⁸ Because each output device has three corresponding ESD devices, there would be hundreds of ESD devices for the driver circuit and many ways to read on the limitations of the claims. Petitioner presents only three alternatives, with figures prepared by Dr. Murphy. The first mapping is identified as Ax, the second as Bx, and the third as Cx, respectively. These alternatives are introduced by “Mapping A,” etc. Discussions not identified as a specific mapping apply to all three mappings. Murphy ¶106, n.11.

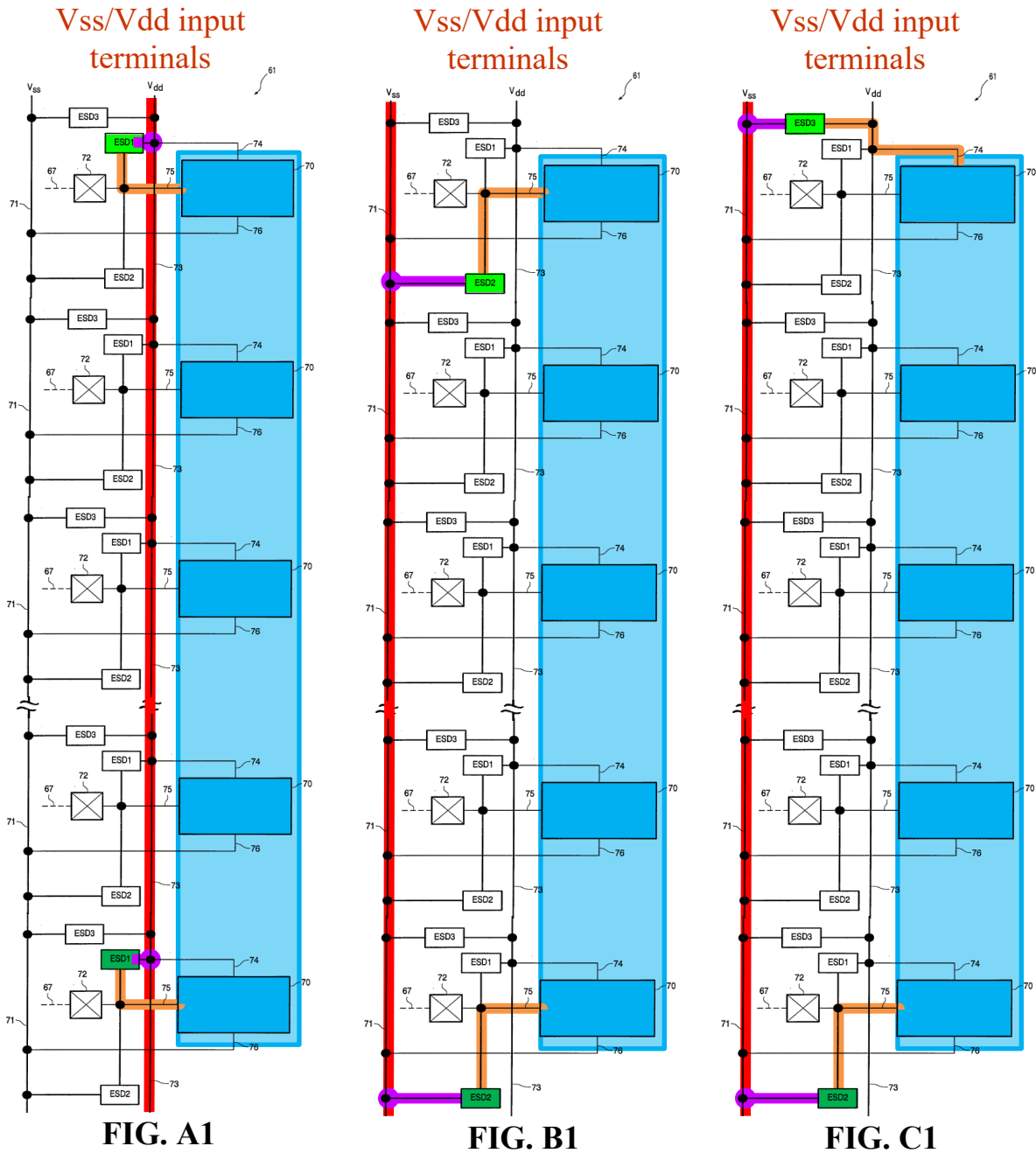
⁹ For ease of reference, because output device 70 is shown as a generic box and would have been understood to represent the gate driving circuitry when circuit element 20 is a gate driver 63, this Petition retains this numbering of FIG. 5.

Mapping A: FIG. A1 shows a first protection circuit ESD1 at the first driver unit of gate driver 63 (closest to the input terminals) and second protection circuit ESD1 at the last gate driver unit (farthest from the input terminals) being connected to the line driving units 70 of gate driver 63 through output line 75 “to protect the circuitry inside the devices” and also connected to power supply line Vdd. *Reiner*, 10:1-15; Murphy ¶108.

Mapping B: FIG. B1 shows a first protection circuit ESD2 at the first driver unit of gate driver 63 (closest to the input terminals) and second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) being connected to the line driving units of gate driver 63 through output line 75 “to protect the circuitry inside the devices” and also connected to power supply line Vss. *Reiner*, 10:1-15; Murphy ¶109.

Mapping C: In the district court, the Patent Owner appears to take the liberal view that any two circuits connected to the same powerline are connected to each other. Ex. 1014, ¶¶136-144. Petitioner disagrees. But assuming Patent Owner’s view, as shown in FIG. C1, a first protection circuit ESD3 before the first driver unit of gate driver 63 (closest to the input terminals) and second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) are connected to line driving units of gate driver 63 “to protect the circuitry inside the

devices” and also connected to power supply line V_{ss} on either side of the gate driver 63. Reiner, 10:1-15; Murphy ¶110.



Murphy ¶110.

Reiner explains that ESD1-ESD3 protect the drive circuitry of each line driving unit 70. *Reiner*, 9:18-22. In FIG. 5, driver “output devices 70” are shown as ‘black box’ elements that do not show the internal circuitry, but a POSITA would have recognized the ESD protection protects any driver circuitry in that box and applies equally to both source driver 61 and gate driver 63, especially in light of *Reiner*’s discussions that both drivers are “integrated circuits” to be protected from ESD damage. *Reiner*, 4:15-16, 9:11-22. As such, a POSITA would have understood that the ESD protection shown in FIG. 5 would have protected [gate driver 63](#), where each of output devices 70 comprises the line-driving circuitry for each scan line 68. Murphy ¶111.

If Patent Owner argues or the Board finds that *Reiner* does not disclose [4d], *Reiner* renders it obvious. As explained above, *Reiner* “relates to *integrated circuit devices* with ESD protection” and generally “provide[s] a scheme that allows to *add an ESD protection network* to densely packed *integrated circuit devices*.” *Reiner*, 2:2-3, 4:15-16 (emphases added). Because a “typical example” of protected integrated circuits “is an [integrated circuit display driver 61 or 63](#),” a POSITA would have found it obvious to protect the [gate driver 63](#) ([scanning line driving circuit](#)) with the same ESD protection network as the source driver 61 example of FIG. 5. *Reiner*, 9:12-14, 12:4-5 (emphasis added). A POSITA would have found this obvious because it would have also protected the gate driver 63 from ESD

events that could damage the “very sensitive circuits” of the gate driver, which could render the display unacceptable. *Reiner*, 2:28-3:1; Murphy ¶¶112-114.

i. Motivation

A POSITA would have been motivated to provide a first and second protection circuit connected to the scanning line driving circuit to protect the scanning line driving circuit from ESD damage and also connected to the power supply line Vss, Vdd that can be subject to ESD events. Murphy ¶115; *Reiner*, 3:2-3; Ex. 1001, 1:14-19.

A POSITA would have recognized that source driver 61 and gate driver 63 are at risk of ESD damage because the metal lines can conduct static electricity that “destroy[s]” the “very sensitive circuits” in the driver modules. *Reiner*, 2:28-3:1. *Reiner* recognizes, as was conventional in the art, that driver circuits (61 or 63) contain transistors and other circuit elements. *Reiner*, 6:12-17, 8:30-31 (“The transistor 31 is in the present embodiment part of an outputs stage [output device 70] of the integrated circuit device 30.”). A POSITA would have been motivated to “protect the circuitry” of each output device 70 of the gate driver 63 in the same way as source driver 61 to prevent the sensitive circuits from being damaged by ESD events occurring on either a voltage line (Vdd or Vss) or the output line (equivalent of output line 75). *Reiner*, 10:10-12; Murphy ¶115. A POSITA would have been motivated to provide ESD protection circuits for the gate driver 63 to

protect both driver circuits of an LCD display, which can be rendered unacceptably or irreparably damaged if either the gate (scanning line) driver or source (data line) driver is damaged because this impairs activating pixel rows or columns of the LCD screen. Murphy ¶115.

A POSITA would have been motivated to protect *Reiner*'s gate driver 63 with ESD protection like that shown in FIG. 5 to “add an ESD protection network to densely packed integrated circuit devices.” *Reiner*, 4:15-16. A POSITA would have recognized that the risk of ESD damage (both electric and thermal) is heightened for densely packed circuits (e.g., *Reiner*'s gate driver 63) that contain “very sensitive” elements close together and thus would be susceptible to ESD damage. *Reiner*, 2:28-3:1, 4:15-16; Murphy ¶116.

A POSITA would have also recognized that the “ESD protection network” of *Reiner*'s FIG. 5 implemented in gate driver 63 would have protected “each output device” (equivalent to output device 70 for each scan line) because it represents merely implementing *Reiner*'s known prior art ESD protection network in gate driver 63 to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s].” *Reiner*, 4:15-16, 10:10-12. Similarly, a POSITA would have been motivated to implement *Reiner*'s ESD protection network to improve gate driver 63 in the same way as shown in FIG. 5 to protect the output circuit in box 70, which could be a source driver or gate driver because they have similar

configurations and both need protection from ESD events. Murphy ¶117; *Reiner*, 2:28-3:1. At a minimum, a POSITA would have found it obvious to try implementing *Reiner*'s ESD protection network to protect the output devices of gate driver 63, given *Reiner*'s suggestion that both source driver 61 and gate driver 63 are "integrated circuits" and contain "very sensitive circuits" that can be "destroyed" by an ESD "discharge event." *Reiner*, 2:28-3:1, 9:12-14; Murphy ¶117.

A POSITA also would have been motivated to implement a first and second ESD protection circuit connected to *Reiner*'s gate driver 63 to protect the gate driver 63 from electrical and thermal ESD damage, and also connected to the power supply line Vss, Vdd because the configuration would have protected the circuits and using a single metal layer would have reduced the cost of fabricating gate driver 63 and made the chip less bulky. *Reiner*, 4:10-12, 4:15-19, 9:16-22, 10:15-17, 12:15-18, claim 11; Murphy ¶118.

A POSITA would have been motivated to implement *Reiner*'s ESD protection network for gate driver 63 to prevent damage to "realize more densely packed integrated circuit devices" while reducing the risk of damage from ESD events. *Reiner*, 4:15-19, 12:16-18; Murphy ¶119.

ii. Expectation of Success

A POSITA would have reasonably expected to succeed in implementing *Reiner*'s ESD protection network to protect gate driver 63 (scanning line driving circuit) and the power supply line(s). Murphy ¶120. Protecting a scanning line driving circuit was admittedly "conventional art" for preventing ESD damage. *Reiner*, 7:23-25; Ex. 1001, 1:54-56, 2:5-14, FIG. 11; *Takahara*, [0066], FIG. 1 (using electrostatic protective circuits 150, 151 to protect scan-line drive circuit 104 from static electricity). Using a first protection circuit and second protection circuit connected to the gate driver 63 (scanning line driving circuit) to protect the gate driver, and also connected to the power supply line (Vss 71, Vdd 73), such as in *Reiner*, would have been merely the straightforward application of known, conventional techniques using *Reiner*'s ESD protection network to protect the driver units of gate driver 63 (which are similar to driver units 70) according to their known functions to yield predictable results (protecting gate driver 63 and its driver units 70). Murphy ¶120; *Reiner*, 2:28-3:1, 3:4-8, 3:15-16, 8:8-15, 8:18-20, 8:30-33, 9:12-22, 10:1-17, 12:22-25; *KSR*, 550 U.S. at 416; *Slot Speaker*, 680 F. App'x at 943-44.

- f. [4e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and”

Reiner discloses or renders obvious the limitations of [4e], as shown by each proposed mapping A-C. Murphy ¶¶121-126.

As explained in [4d], *Reiner* discloses or a POSITA would have found it obvious to implement *Reiner*’s ESD protection network providing ESD1-ESD3 “for each output device” on each scan line “to protect the circuitry inside the [output] devices” of gate driver 63 (scanning line driving circuit). *Reiner*, 10:10-12; *supra* § VII.A.1.e; Murphy ¶¶103-120, ¶122, FIGS. A1-C1.

Reiner teaches the first protection circuit is connected to the power supply line (Vdd, Vss) between (i) a first connecting portion at which the gate driver 63 and the power supply line are connected and (ii) the input terminal supplying power to the power supply line, for example, as described below and shown in FIGS. A2-C2. Murphy ¶123. As Dr. Murphy explains, gate driver 63 is connected to power supply lines Vdd, Vss at each driver unit 801-n. Murphy ¶123; Ex. 1001, 7:46-47, FIGS. 1-3, 11. One first connecting portion is shown in FIGS. A2-C2, but there are other connecting portions between the output units 70 and the power line that could be mapped to the first connecting portion. Murphy ¶123.



FIG. A2



FIG. B2



FIG. C2

Murphy ¶123.

Mapping A: FIG. A2 shows first protection circuit ESD1 at the first driver unit of gate driver 63 (closest to the input terminals) being connected to power supply line Vdd between (i) a first connecting portion where gate driver 63 and the power supply line are connected at line 74 and (ii) the input terminal supplying power to power supply line Vdd. Murphy ¶124, FIG. A2.

Mapping B: FIG. B2 shows first protection circuit ESD2 at the first driver unit of gate driver 63 (closest to the input terminals) being connected to the power supply line Vss between (i) a first connecting portion where gate driver 63 and the power supply line are connected at line 76 and (ii) the input terminal supplying power to power supply line Vss. Murphy ¶125, FIG. B2.

Mapping C: And, if Patent Owner's view is adopted, FIG. C2 shows first protection circuit ESD3 before the first driver unit of gate driver 63 (closest to the input terminals) being connected to the power supply line Vss between (i) a first connecting portion where gate driver 63 and the power supply line are connected at line 76 and (ii) the input terminal supplying power to power supply line Vss. Murphy ¶126, FIG. C2.

- g. [4f]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

Reiner discloses or renders obvious the limitations of [4f], as shown by each proposed mapping A-C. Murphy ¶¶127-133.

As explained in [4d] and [4e], *Reiner* discloses or a POSITA would have found it obvious to implement *Reiner*’s ESD protection network to protect gate driver 63 and this protection would have included the configuration described in [4d]-[4e]. *Supra* §§ VII.A.1.e-VII.A.1.f; Murphy ¶¶103-126, ¶128, FIGS. A1-C1, A2-C2; *Reiner*, 10:10-15.

Reiner’s ESD protection network includes “three ESD devices ... for each output device 70,” that, when applied to gate driver 63 (scanning line driving circuit), would have included gate driver 63 being connected to the power supply line (Vdd, Vss) (see [4e]) between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected (see [4e]) and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected, for example, as described below and shown in FIGS. A3-C3. Murphy ¶129.

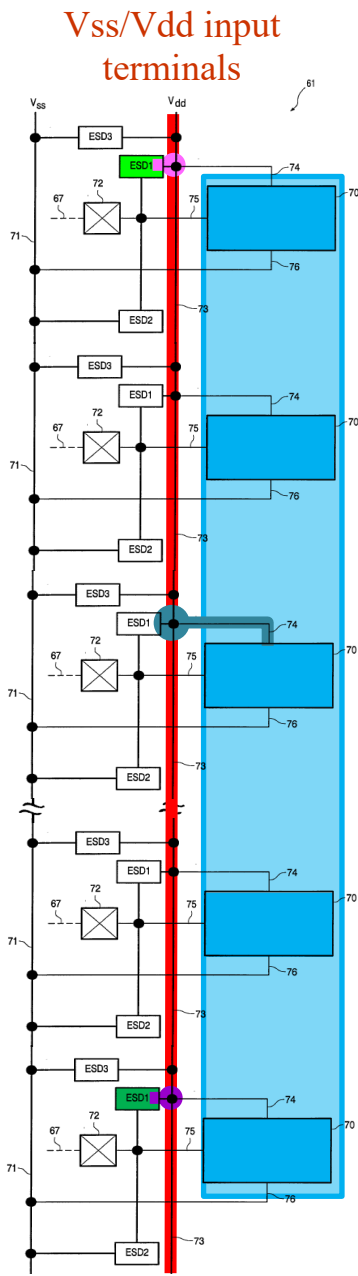


FIG. A3

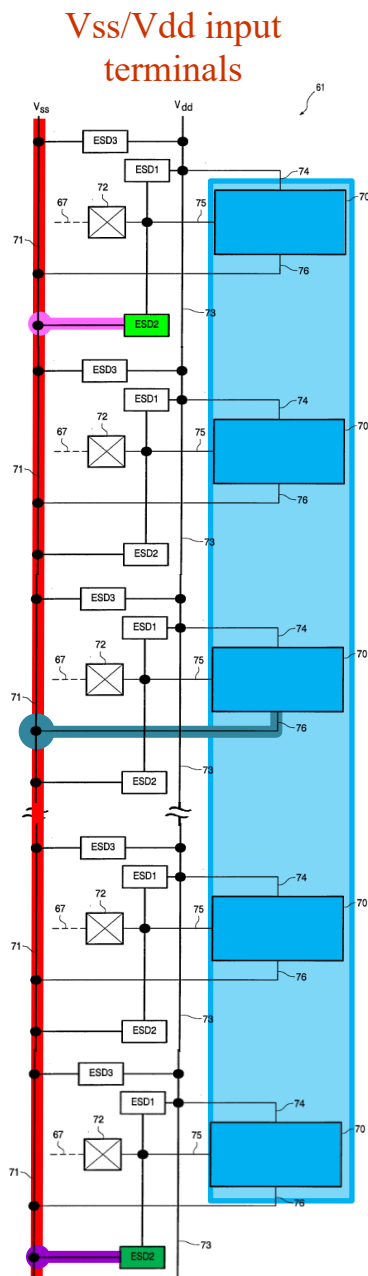


FIG. B3

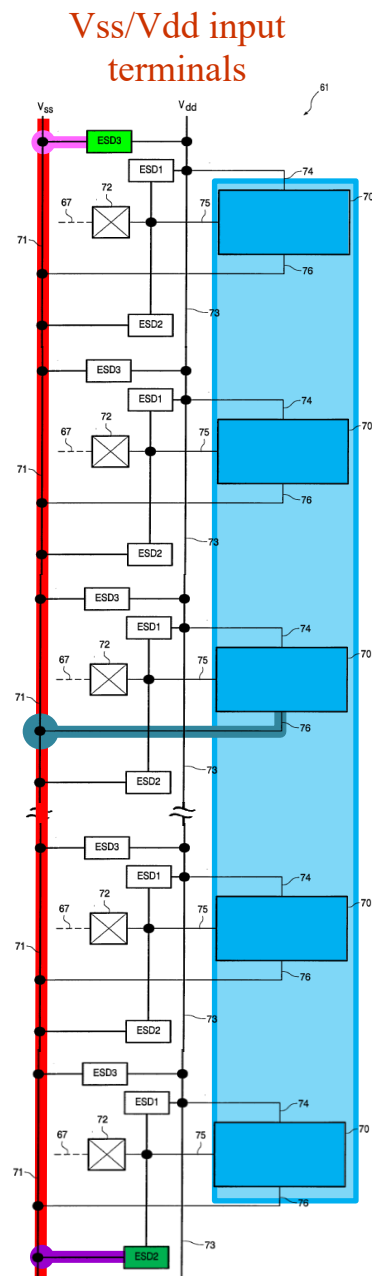


FIG. C3

Murphy ¶129.

Mapping A: FIG. A3 shows gate driver 63 being connected to power supply line Vdd (see [4e], FIG. A2) between (iii) a second connecting portion where the first protection circuit ESD1 at the first gate driver unit (closest to the input terminals) and the power supply line Vdd are connected (see [4e], FIG. A2) and (iv) a third connecting portion where the second protection circuit ESD1 at the last gate driver unit (farthest from the input terminals) and power supply line Vdd are connected. Murphy ¶130, FIG. A3.

Mapping B: FIG. B3 shows gate driver 63 being connected to power supply line Vss (see [4e], FIG. B2) between (iii) a second connecting portion where the first protection circuit ESD2 at the first gate driver unit (closest to the input terminals) and the power supply line Vss are connected (see [4e], FIG. B2) and (iv) a third connecting portion where the second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) and power supply line Vss are connected. Murphy ¶131, FIG. B3.

Mapping C: And, if Patent Owner's view is adopted, FIG. C3 shows gate driver 63 being connected to power supply line Vss (see [4e], FIG. C2) between (iii) a second connecting portion where the first protection circuit ESD3 before the first gate driver unit (closest to the input terminals) and the power supply line Vss are connected (see [4e], FIG. C2) and (iv) a third connecting portion where the second protection circuit ESD2 at the last gate driver unit (farthest from the input

terminals) and power supply line V_{ss} are connected on the side of the gate driver

63. Murphy ¶132, FIG. C3.

Reiner thus renders obvious claim 4.

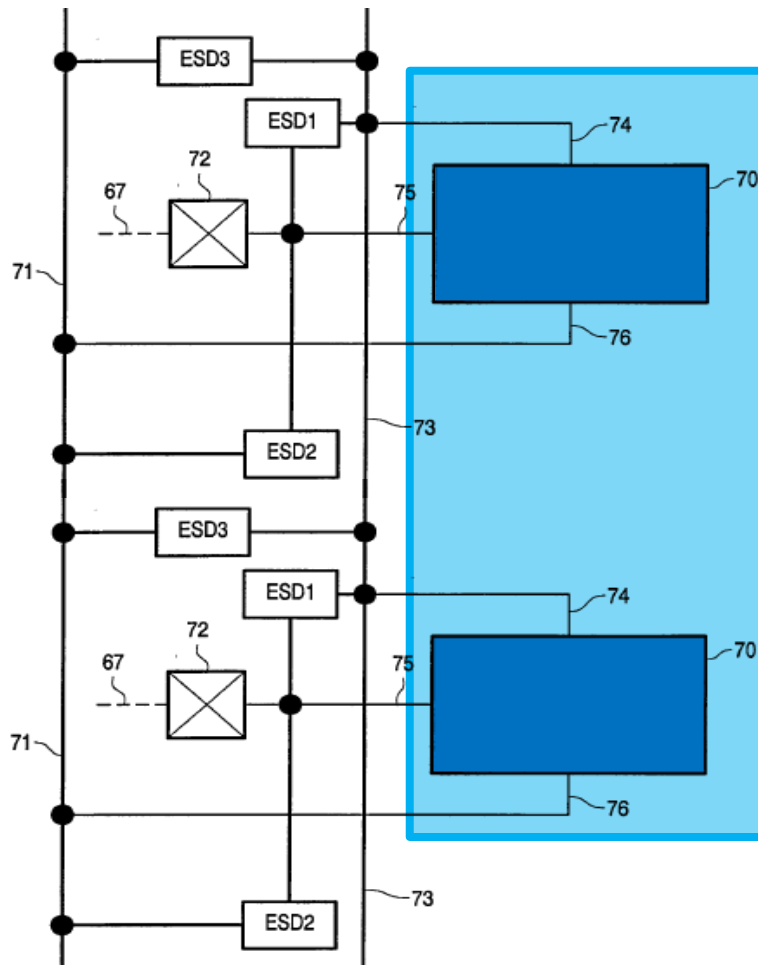
2. Claim 5

- a. “The display device as set forth in claim 4, further comprising: a scanning line driving unit circuit included in the scanning line driving circuit.”**

Reiner discloses or renders obvious the additional limitations of claim 5.

Murphy ¶¶134-137.

As explained in [4d], *Reiner* teaches individual gate-line driving units 70 (scanning line driving unit circuits) are included in gate driver 63 (scanning line driving circuit) for driving each gate line 68. Murphy ¶135; *Reiner*, FIG. 5.



Reiner, FIG. 5.

Reiner's "integrated circuits," such as gate driver 63, comprise "a plurality of integrated devices [22]," such as transistors. *Reiner*, 6:12-17, 6:18-21, 8:18-20. "[I]ntegrated circuit display driver ... 63" is "designed to drive many lines of an LCD display 60" and "typically has a large number of parallel outputs" and "many output devices" that receive power to drive the scan lines. *Reiner*, 9:11-22, FIG. 4; Murphy ¶136.

If Patent Owner argues or the Board finds that *Reiner* does not expressly disclose gate driver 63 having driver output units 70, a POSITA would have found it obvious for the reasons discussed in claim 4. *Supra* § VII.A.1; Murphy ¶137.

3. Claim 6

- a. “The display device as set forth in claim 4, further comprising: a buffer circuit included in the scanning line driving circuit.”**

Reiner discloses or renders obvious the additional limitations of claim 6. Murphy ¶¶138-139.

Reiner discloses that “[e]ach output device 70 ... may comprise ... a buffer” that “drive[s] the source lines 67 with the voltages needed by each pixel of the LCD screen 60.” *Reiner*, 10:1-3. As explained for claim 4, a POSITA would have understood, or at least found it obvious, that the driver circuitry for [gate driver 63](#) to drive gate line 68 would have included similar circuit elements to source driver 61 that drive source lines 67. *Supra* §§ VII.A.1.b-VII.A.1.e ([4a]-[4d]); Murphy ¶139.

4. Claim 7

- a. “The display device as set forth in claim 4, further comprising: a transistor included in the scanning line driving circuit.”**

Reiner discloses the additional limitations of claim 7. Murphy ¶¶140-142.

Reiner discloses that the “integrated circuit device compris[es]” a “MOS transistor” or other type of transistor. *Reiner*, 6:12-17; Murphy ¶141. As shown in FIG. 2, integrated “circuit device 20” includes “integrated device 22 (e.g., a transistor).” *Reiner*, 6:18-21.

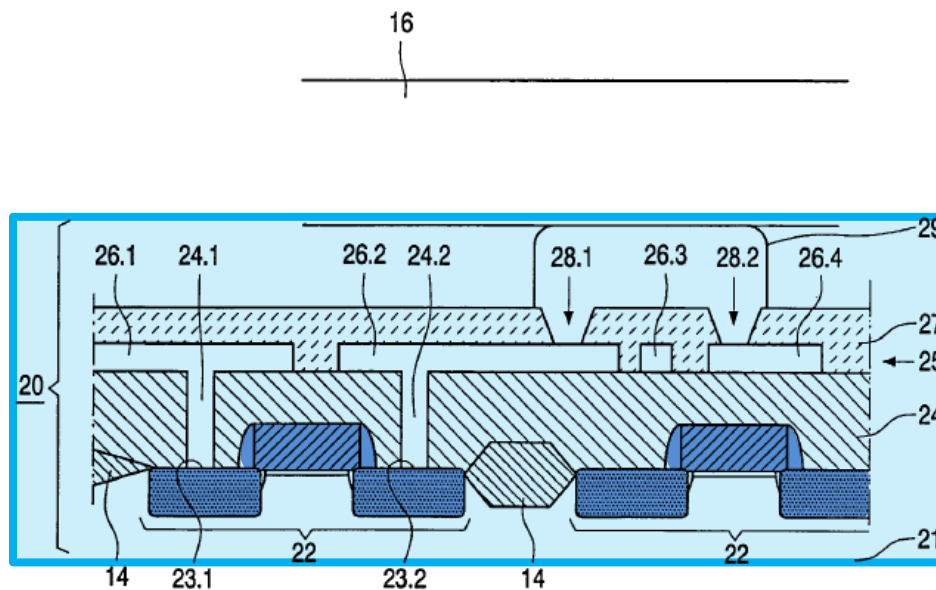


FIG. 2

Reiner, FIG. 2.

Similarly, FIG. 3 shows “integrated device[] 31,” which is “an output stage [output device 70] of the integrated circuit device 30” (e.g., gate driver 63), may include a “CMOS transistor[].” *Reiner*, 8:18-31; Murphy ¶142.

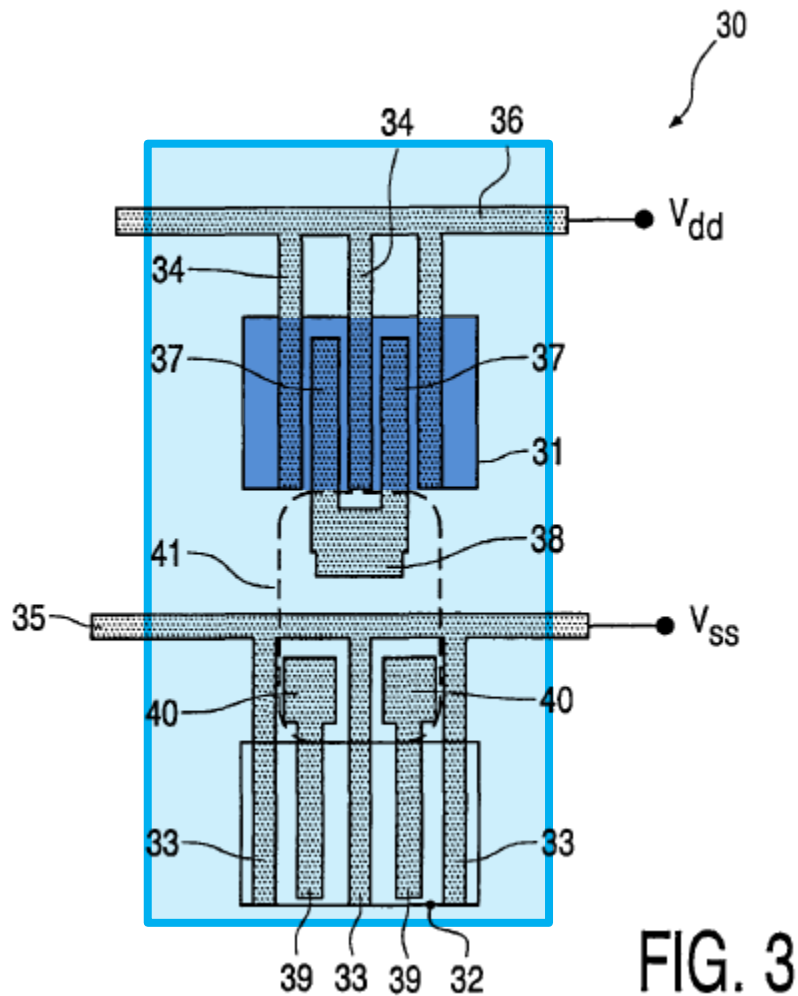


FIG. 3

Reiner, FIG. 3.

5. Claim 8

Reiner renders obvious the additional limitations of claim 8. Murphy ¶¶144-153.

- a. [8a] “The display device as set forth in claim 4, further comprising: a substrate,”

Reiner discloses the display device further comprising a substrate. Murphy ¶¶144-147.

Reiner FIG. 2 shows integrated circuit 20 (e.g., gate driver 63), including transistors 22, arranged on **substrate 21**. *Reiner*, 6:18-24. Similarly, the bump bridge(s) of integrated circuit device 20 allows the circuit device to be arranged on **substrate 16** via an interconnection (not shown). *Reiner*, 7:22-26; *Murphy* ¶145.

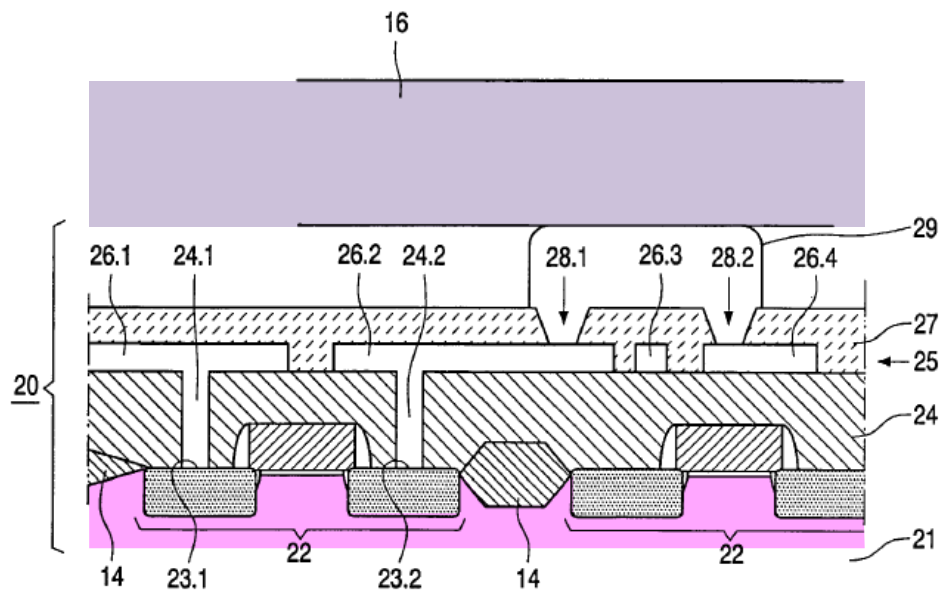


FIG. 2

Reiner, FIG. 2.

A POSITA would have recognized that substrates 21 or 16 may include, for example, the substrate on which LCD display 60's scan/gate lines 68, source/data lines 67, and pixels are formed, such as shown in FIG. 4. *Reiner's* driver output devices can be "connected (e.g. by means of bonding)" to their respective display lines via contact pads 72 to drive the lines, which could be patterned on the display substrate, as shown in *Reiner's* FIG. 4. *Reiner*, 10:1-6. Thus, gate driver 63 is

arranged on the substrate to create the LCD display device described in *Reiner*, which was conventional. Murphy ¶146; *Takahara*, [0001], [0064], FIG. 1; *Murai*, [0001], [0017], FIG. 1; Ex. 1001, 1:57-59 (FIG. 11 is “conventional art.”).

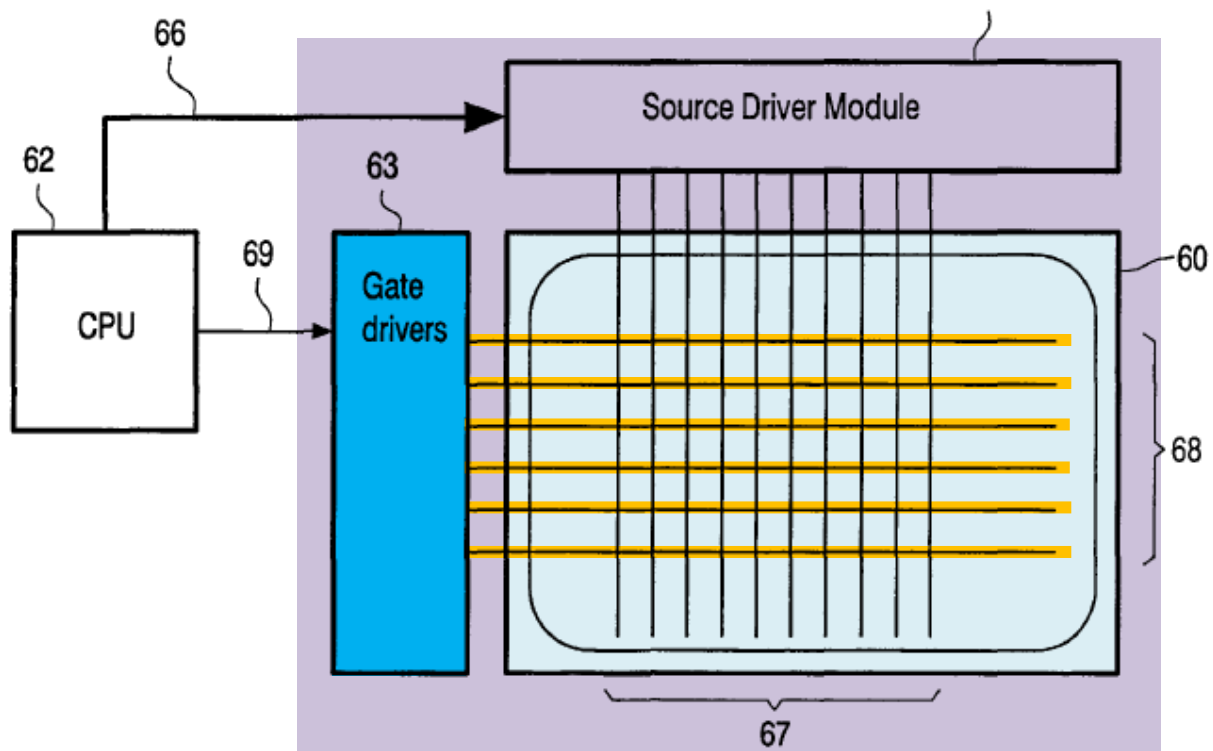


FIG. 4

Reiner, FIG. 4.

If Patent Owner argues or the Board finds that *Reiner* discloses such connections only for source driver 61, a POSITA would have found it obvious to include the same connections to interconnect gate driver 63 to the substrate, as explained in claim 4. Murphy ¶147.

b. [8b]: “the scanning line driving circuit being arranged on the substrate,”

As discussed in [8a], *Reiner* discloses or renders obvious the scanning line driving circuit being arranged on the substrate with LCD display 60’s scan lines.

Murphy ¶148; *supra*, § VII.A.5.a.

c. [8c]: “the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”

Reiner discloses or renders obvious the additional limitations of [8c].

Murphy ¶¶149-151.

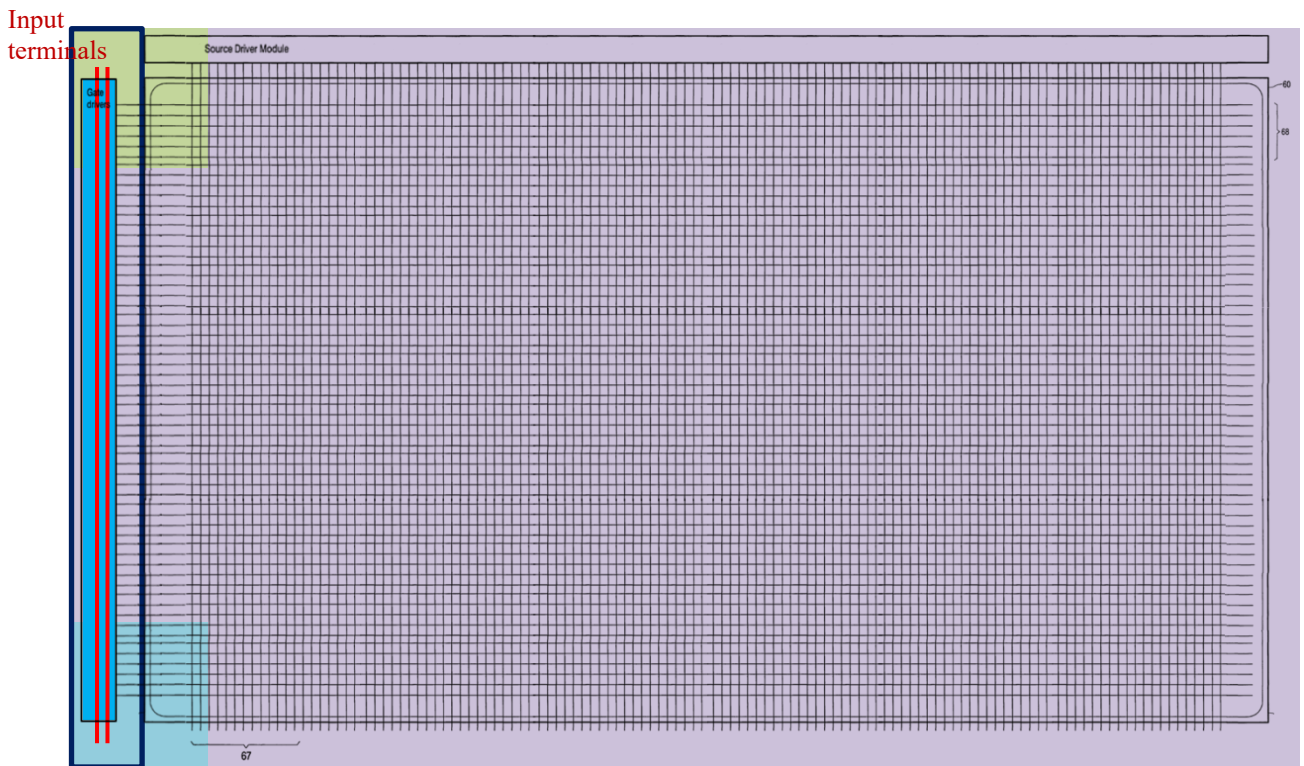
Reiner explains that “power supply lines 71 and 73” run perpendicular to output lines 75 and supply power to each output device 70 of the driver unit.

Reiner, 10:7-10, FIG. 5. A POSITA would have understood that the layout of FIG. 5 applies equally to source driver 61 and gate driver 63, or at least found it obvious to use a similar layout, as explained for claim 4. Murphy ¶150; *supra* § VII.A.1.

Although FIG. 4 shows a display having six scan/gate lines 68 and ten data/source lines 67, a POSITA would have understood that an LCD display would have had hundreds of such lines. Murphy ¶151. Therefore, a POSITA would have known that the area comprising source driver 61 and gate driver 63 with their respective power lines would have been a very small portion of the substrate’s

area. FIG. D shows an LCD display having 60 scan/gate lines 68 and 120 source/data lines 67. Murphy ¶¶50-51, ¶151. This is a fraction an actual display's size, but it is apparent that power supply lines Vdd and Vss are formed over first corner portion and second corner portion of the substrate¹⁰ and follow the periphery of the substrate because they are perpendicular to the scan lines 68 at gate driver 63, outside (towards the substrate's outer edge) contact portion 72, where gate driver 63 is connected to gate/scan line 68. *Reiner*, 10:1-10, FIGS. 4, 5; Murphy ¶151, FIG. D.

¹⁰ The claim does not recite the input terminal location and the same argument applies regardless of which side of the gate driver 63 they are on. Murphy ¶151, n.14.



Murphy ¶151 (FIG. D).

- d. [8d]: “the first protection circuit being arranged in the first corner portion of the substrate, and”

As explained in [4d]-[4f], the first protection circuit can correspond to ESD protection circuit ESD1, ESD2, or ESD3 at the first gate driver unit (closest to the input terminals), at the first scan line 68, and is thus in the first corner portion of the substrate, as shown in [8c]. Murphy ¶152.

- e. [8e]: “the second protection circuit being arranged in the second corner portion of the substrate.”

As explained in [4d]-[4f], the second protection circuit can correspond to ESD protection circuit ESD1 or ESD2 at the last gate driver unit (farthest from the

input terminals), at the last scan line 68, and is thus in the second corner portion of the substrate, as shown in [8c]. Murphy ¶153.

6. Claim 9

a. “An electronic device provided with the display device as set forth in claim 4.”

Reiner discloses or renders obvious the additional limitations of claim 9. Murphy ¶¶154-158.

As explained for claim 4, *Reiner* discloses “LCD display” having “LCD screen 60,” which a POSITA would understand describes an electronic device. *Reiner*, 9:23-26; Murphy ¶155.

If Patent Owner argues or the Board finds that *Reiner* does not disclose that the LCD display is provided in an electronic device, a POSITA would have found it obvious to have an electronic device provided with the display device of claim 4. *Reiner* describes a display device having a CPU for driving an LCD display 60, and a POSITA would have found it obvious to use the LCD display for its intended function as a display on an electronic device (powering the power lines Vss, Vdd), such as a television, computer monitor, personal digital assistant (PDA), cellular phone, laptop computer, or other device needing a display screen. Murphy ¶156.

i. Motivation

A POSITA would have been motivated to provide *Reiner*'s LCD display of claim 4 in an electronic device because the purpose of LCD displays is to provide a display screen for laptops, personal computers (PCs), PDAs, televisions, and other electronic devices. LCDs were known to consume less power than other screen types, but could be subject to ESD damage. Murphy ¶157. A POSITA would have been motivated to implement *Reiner*'s LCD display of claim 4 as an electronic device display to reduce power consumption and prevent ESD damage and thermal damage because of the ESD protection network. *Reiner*, 3:30-31, 12:22-25. A POSITA also would have been motivated to implement *Reiner*'s LCD display of claim 4 in an electronic device “to realize more densely packed integrated circuits,” which permits the formation of smaller pixel rows leading to a sharper, less pixelated display screen or a higher resolution display screen that improves the user's visual experience. *Reiner*, 4:15-16, 12:18; Murphy ¶157.

ii. Expectation of Success

A POSITA would have reasonably expected to succeed in implementing an electronic device provided with the display screen of claim 4. Murphy ¶158. Using LCD display screens in electronic devices was conventional for POSITAs and implementing the display screen of claim 4 into a laptop computer, monitor, television, PDA, cellular phone, etc., would have been merely the straightforward

application of known, conventional manufacturing techniques to fabricate the display with the device or attach the display to the device, used according to their known functions to yield predictable results (implementing an LCD display in device). Murphy ¶158; *KSR*, 550 U.S. at 416; *Slot Speaker*, 680 F. App'x at 943-44.

7. Independent Claim 10

a. [10pre]: “A display device, comprising:”

[10pre] is substantively the same as [4pre]. *Reiner* discloses [10pre] as discussed in [4pre]. *Supra* § VII.A.1.a; Murphy ¶¶159-164.

b. [10a]: “a circuit element included in a scanning line driving circuit;”

[10a] is substantively similar to [4a], but recites a “circuit element” included in the scanning line driving circuit. *Compare* Ex. 1001, 12:27, *with id.*, 13:6. *Reiner* discloses or renders obvious gate driver 63 (scanning line driving circuit) including line driver output devices 70 (circuit elements), which may comprise a transistor and/or buffer, and discloses or renders obvious [10a] as discussed in [4a], [4d]-[4f], and claim 5. *Supra* §§ VII.A.1.b, VII.A.1.e-VII.A.2; Murphy ¶160.

- a. **[10b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”**
[10c]: “an input terminal connected to the power supply line to supply power; and”

[10b] and [10c] are substantively the same as [4b] and [4c]. *Reiner* discloses or renders obvious [10b] and [10c] as discussed in [4b] and [4c]. *Supra* §§ VII.A.1.c-VII.A.1.d; Murphy ¶¶161-162.

- b. **[10d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element, the first protection circuit and the second protection circuit are connected to the power supply line,”**

[10d] is substantively similar to [4d], but recites the first and second protection circuits being connected to the scanning line driving circuit “to protect the circuit element” instead of “the scanning line driving circuit.” *Compare* Ex. 1001, 12:33-37, *with id.*, 13:13-17. *Reiner* discloses or renders obvious the first and second protection circuits being connected to gate driver 63 (scanning line driving circuit) “to protect the circuitry inside the [output] devices 70” (circuit elements), and thus discloses or renders obvious [10d] as discussed in [4d]-[4f] and claim 5. *Reiner*, 10:10-12; *supra* §§ VII.A.1.e-VII.A.2; Murphy ¶163.

- c. **[10e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and”**

[10e] is substantively similar to [4e], but recites the “circuit element” being connected to the power supply line in (i). *Compare* Ex. 1001, 12:38-41, *with id.*, 13:18-21. *Reiner* discloses or renders obvious the first protection circuit being connected to power supply line Vdd/Vss between (i) the first connecting portion where an intermediate gate driver output device 70 (circuit element) is connected to the power supply line, and (ii) the input terminals, and discloses or renders obvious [10e] as discussed in [4e]. *Supra* § VII.A.1.f; Murphy ¶164.

- d. **[10f]: “the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”**

[10f] is substantively similar to [4f], but recites the “circuit element” being connected to the power supply line between the second connecting portion in (iii) and the third connecting portion in (iv). *Compare* Ex. 1001, 12:38-41, *with id.*, 13:18-21. *Reiner* discloses or renders obvious an intermediate gate driver output device 70 (circuit element) being connected to power supply line Vdd/Vss between the second connecting portion connecting the first protection circuit to the power

supply line and the third connecting portion connecting the second protection circuit to the power supply line, and discloses or renders obvious [10f] as discussed in [4f]. *Supra* § VII.A.1.g; Murphy ¶165.

8. Claim 11

- a. “The display device as set forth in claim 10, further comprising: a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.”**

The additional limitations of claim 11 are substantively the same as those in claim 5, which *Reiner* discloses as discussed for claim 5. *Supra* § VII.A.2; Murphy ¶166. The scanning line driving unit circuit includes a buffer or transistor element, as discussed in [10a]. *Supra* § VII.A.7.b.

9. Claim 12

- a. “The display device as set forth in claim 10, further comprising: a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.”**

The additional limitations of claim 12 are substantively the same as those in claim 6, which *Reiner* discloses or renders obvious as discussed for claim 6. *Supra* § VII.A.3; Murphy ¶167. The scanning line driving unit circuit includes a buffer that may comprise the circuit element, as discussed in [10a]. *Supra* § VII.A.7.b.

10. Claim 13

- a. **“The display device as set forth in claim 10, further comprising: a transistor included in the scanning line driving circuit, the transistor being the circuit element.”**

The additional limitations of claim 13 are substantively the same as those in claim 7, which *Reiner* discloses as discussed for claim 7. *Supra* § VII.A.4; Murphy ¶168.

11. Claim 14

- a. [14a]: **“The display device as set forth in claim 10, further comprising: a substrate,”**
[14b]: **“the scanning line driving circuit being arranged on the substrate,”**
[14c]: **“the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”**
[14d]: **“the first protection circuit being arranged in the first corner portion of the substrate, and”**
[14e]: **“the second protection circuit being arranged in the second corner portion of the substrate.”**

The additional limitations of [14a]-[14e] are substantively the same as those in [8a]-[8e], which *Reiner* discloses or renders obvious as discussed for [8a]-[8e]. *Supra* §§ VII.A.5; Murphy ¶¶169-173.

12. Claim 15

- a. “An electronic device provided with the display device as set forth in claim 10.”**

The additional limitations of claim 15 are substantively the same as those in claim 9, which *Reiner* discloses or renders obvious as discussed for claim 9. *Supra* § VII.A.6; Murphy ¶174.

13. Independent Claim 16

- a. [16pre]: “A display device, comprising:”
[16a]: “a scanning line driving circuit;”
[16b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”
[16c]: “an input terminal connected to the power supply line to supply power; and”**

[16pre]-[16c] are substantively the same as [4pre]-4c]. *Reiner* discloses or renders obvious [16pre]-[16c] as discussed in [4pre]-[4c]. *Supra* §§ VII.A.1.a-VII.A.1.d; Murphy ¶¶175-178.

- b. [16d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”**

[16d] is substantively similar to [4d], but recites the first and second protection circuits being “connected to power supply line” to “protect the power

supply line,” instead of the scanning line driving circuit *Compare* Ex. 1001, 12:33-37, *with id.*, 13:63-67. Murphy ¶179.

As explained in [4d]-[4f], *Reiner* discloses or renders obvious the first and second protection circuits being connected to power supply line Vdd or Vss. *Supra* §§ VII.A.1.e-VII.A.1.g; Murphy ¶180.

As explained below, [16e]-[16h] recite the same connections between the first protection circuit, second protection circuit, and scanning line driving circuit as [4e]-[4f] and the first and second protection circuits being on a first and second side of the scanning line driving circuit, like the first and second corner portions of claim 8. *Reiner*’s ESD protection network, such as ESD1, ESD2, and ESD3, protect the power line because they are configured to “provide a low-ohmic path” to a “ground terminal” (not shown in FIG. 5) “in case of a voltage peak,” which is an ESD event. *Reiner*, 10:15-17. This configuration protects the power supply line between the first and second protective circuits, as well as the scanning line driving circuit (and individual driver elements).¹¹ The power supply line is protected

¹¹ The ’157 patent’s specification does not recite protecting the power supply line with protective circuits ESD1-ESD4 or ESD11-ESD13. The same configuration protecting the scanning line driving circuit would have been understood to protect the power supply line or the claim lacks written description. Murphy ¶181, n.15.

because static electricity generated on power supply lines Vss or Vdd would be a “voltage peak” (electrostatic discharge) that gets shunted to the “ground terminal” by the “diodes” or “transistors” in ESD1, ESD2, or ESD3. *Reiner*, 10:1-17. This prevents the static discharge from continuing further down the lines where it could cause potential damage. *Reiner* discloses or renders obvious [16d] as discussed in [4d]-[4f] and claim 8. *Supra* §§ VII.A.1.e-VII.A.1.g, VII.A.5; Murphy ¶181.

- c. **[16e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal”**

[16e] is substantively the same as [4e]. *Reiner* discloses or renders obvious [16e] as discussed in [4e]. *Supra* § VII.A.1.f; Murphy ¶182.

- d. **[16f] “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”**

[16f] is substantively broader than [8d]. *Reiner* discloses or renders obvious [16f] as discussed for [8d] because the first protection circuit is disposed at the **first gate driver unit** (closest to the **input terminals**), thereby being at a position on a first side of the scanning line driving circuit closest to the input terminals. *Supra* § VII.A.5.d; Murphy ¶183.

- e. **[16g]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”**

[16g] is substantively the same as [4f]. *Reiner* discloses or renders obvious [16g] as discussed in [4f]. *Supra* § VII.A.1.g Murphy ¶184.

- f. **[16h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”**

[16h] is substantively broader than [8e]. *Reiner* discloses or renders obvious [16h] as discussed for [8e] because the second protection circuit is disposed at the **last gate driver unit** (farthest from the **input terminals**), thereby being at a position on a second side of the scanning line driving circuit farthest from the input terminals. *Supra* § VII.A.5.e; Murphy ¶185.

14. Independent Claim 17

- a. [17pre]: “A display device, comprising:”
[17a]: “a scanning line driving circuit;”
[17b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”
[17c]: “an input terminal connected to the power supply line to supply power; and”

[17pre]-[17c] are substantively the same as [4pre]-[4c]. *Reiner* discloses or renders obvious [17pre]-[17c] as discussed in [4pre]-[4c]. *Supra* §§ VII.A.1.a-VII.A.1.d; Murphy ¶¶186-189.

- b. [17d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”

[17d] is substantively the same as [4d], but recites the first and second protective circuits being “connected to the power supply line,” like [16d]. As explained for [4e], [4f], [16d], [16e], and [16g], *Reiner* discloses or renders obvious the first and second protection circuits being connected to the power supply line to protect scanning line driving circuit. *Supra* §§ VII.A.1.f-VII.A.1.g, VII.A.13.b-VII.A.13.c, VII.A.13.e; Murphy ¶190.

- c. [17e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal”
 [17f]: “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”
 [17g]: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”
 [17h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”

[17e]-[17h] are substantively the same as [4e], [16f], [4f], and [16h], respectively, as explained in claim 16. *Reiner* discloses or renders obvious [17e]-[17h] as discussed in [4e], [4f], [8d], [8e], [16f], and [16h]. *Supra* §§ VII.A.1.f-VII.A.1.g, VII.A.5.d-VII.A.5.e, VII.A.13.d, VII.A.13.f; Murphy ¶¶191-194.

15. Independent Claim 18

- a. [18pre]: “A display device, comprising:”
[18a]: “a circuit element included in a scanning line driving circuit;”
[18b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”
[18c]: “an input terminal connected to the power supply line to supply power; and”

[18pre]-[18c] are substantively the same as [4pre]-[4c]. *Reiner* discloses or renders obvious [18pre]-[18c] as discussed in [4pre]-[4c]. *Supra*

§§ VII.A.1.a-VII.A.1.d; Murphy ¶¶195-198.

- b. [18d]: “a first protection circuit and a second protection circuit that are connected to the power supply line to protect a part of the circuit element, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,”

[18d] is substantively the same as [4d] and [10d], but recites the first and second protective circuits being “connected to the power supply line,” like [16d] to protect “a part of the circuit element,” like [10d]. As explained for [4e], [4f], [10d]-[10f], [16d], [16e], and [16g], *Reiner* discloses or renders obvious the first and second protection circuits being connected to the power supply line “to protect the circuitry inside the devices 70,” such as a buffer or transistor therein (part of the

circuit element). *Supra* §§ VII.A.1.f-VII.A.1.g, VII.A.7.b-VII.A.7.d, VII.A.13.b-VII.A.13.c, VII.A.13.e; Murphy ¶199.

- c. [18e]: “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal”
[18f]: “so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and”
[18g]: “the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected”
[18h]: “so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.”

[18e]-[18h] are substantively the same as [4e] and [10e], [16f], [4f] and [10f], and [16h]. *Reiner* discloses or renders obvious [18e]-[18h] as discussed in [4e], [4f], [8d], [8e], [10e], [10f], [16f], and [16h]. *Supra* §§ VII.A.1.f-VII.A.1.g, VII.A.5.d-VII.A.5.e, VII.A.7.c-VII.A.7.d, VII.A.13.d, VII.A.13.f; Murphy ¶¶200-203.

16. Independent Claim 1

- a. [1pre]: “A display device, comprising:”
[1a]: “a scanning line driving circuit;”
[1b]: “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;”
[1c]: “an input terminal connected to the power supply line to supply power;”
[1d]: “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line;”

[1pre]-[1d] are substantively the same as [4pre]-[4d]. *Reiner* discloses or renders obvious [1pre]-[1d] as discussed in [4pre]-[4d]. *Supra*

§§ VII.A.1.a-VII.A.1.e; Murphy ¶¶204-208.

- b. [1e]: “a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and”

Reiner discloses [1e], as shown by each proposed mapping A-C. Murphy ¶¶209-211.

Reiner’s display driver 63 “typically has a large number of parallel outputs” that “drive many lines” of LCD display 60. *Reiner*, 9:11-15, FIG. 4. *Reiner*’s power supply lines “provide supply voltage (e.g., Vdd) to the output devices [70]” (scanning line driving unit circuits) that make up gate driver 63 (scanning line

driving circuit) and source driver 61 through their connections to power supply lines Vdd/Vss, as shown in FIGS. A4-C4. *Reiner*, 9:11-20; Murphy ¶210.

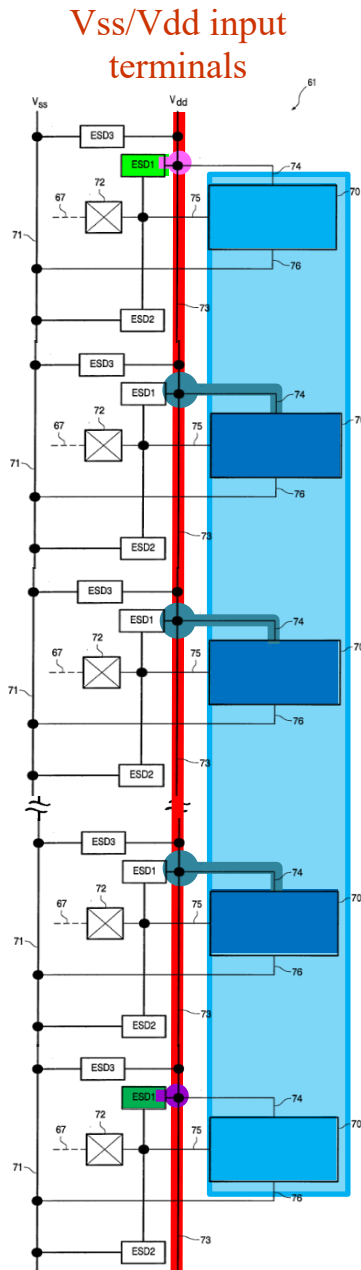


FIG. A4

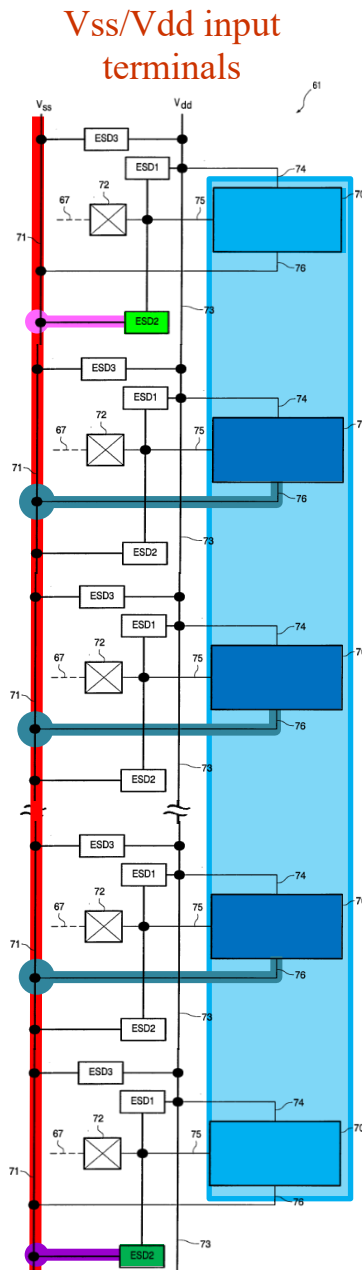


FIG. B4

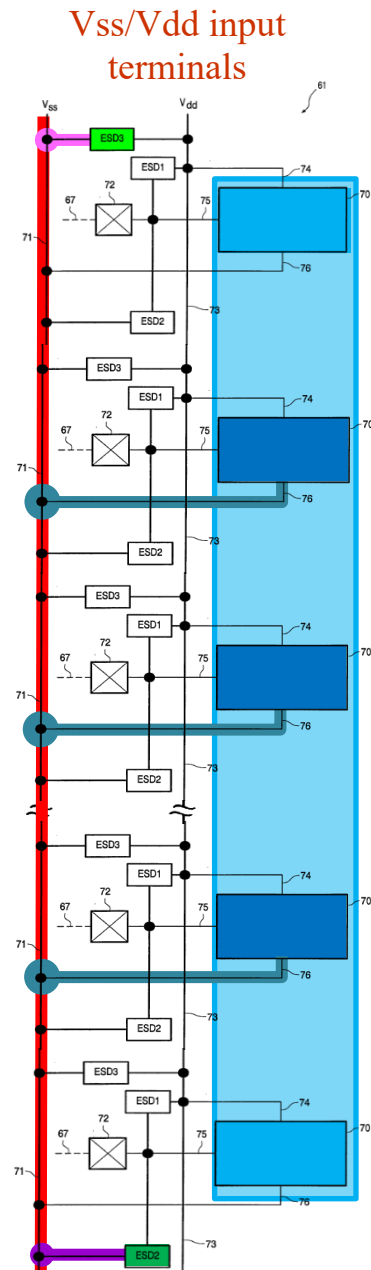


FIG. C4

Murphy ¶210.

Reiner discloses [1e].

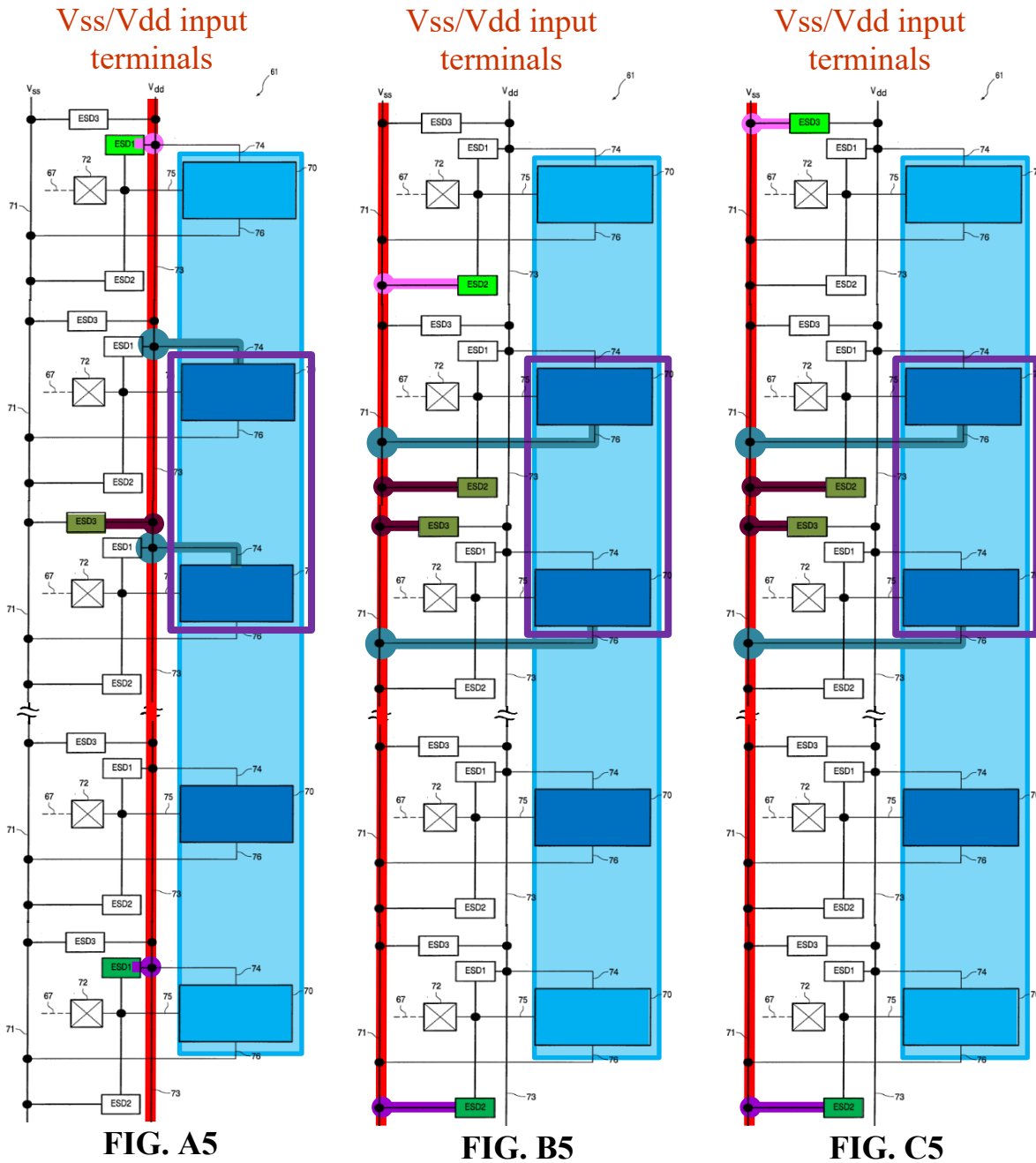
- c. [1f]: “a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other,”

Reiner discloses or renders obvious [1f], as shown by each proposed mapping A-C. Murphy ¶¶212-219.

In *Reiner*, “three ESD devices ESD 1, ESD2, and ESD3 are provided for each output device 70, in order to protect the circuitry inside the devices 70,” which describes or renders obvious each output device 70 of gate driver 63 having an “ESD protection network” comprising protection circuits ESD1-ESD3, as shown in FIG. 5. *Reiner*, 10:10-12; *supra* §§ VII.A.1.e-VII.A.1.g. As explained in claim 4, if *Reiner* is found not to disclose applying the ESD protection networks to gate driver 63’s output devices, a POSITA would have found it obvious to do so. *Supra* §§ VII.A.1.e-VII.A.1.g; Murphy ¶213..

As shown in FIGS. A5-C5, *Reiner* discloses or renders obvious a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of gate driver 63 and a second scanning line driving unit circuit

of gate driver 63, the first and second scanning line driving unit circuits being adjacent to each other. Murphy ¶214.



Murphy ¶214.

Mapping A: FIG. A5 shows a **third protection circuit ESD3** being connected to **power supply line Vdd** between the **second output device 70** from the top (**first scanning line driving unit circuit**) of the “many output devices” 70 for driving the scan lines (plurality of scanning line driving unit circuits) and the **third output device 70** from the top (**second scanning line driving unit circuit**) of the “many output devices” 70, the **second and third output devices 70** being adjacent to each other in **gate driver 63**. Murphy ¶215, FIG. A5; *Reiner*, 9:12-22.

Mapping B: FIG. B5 shows a **third protection circuit ESD2 or ESD3** being connected to **power supply line Vss** between the **second output device 70** from the top (**first scanning line driving unit circuit**) of the “many output devices” 70 and the **third output device 70** from the top (**second scanning line driving unit circuit**), the **second and third output devices 70** being adjacent to each other in **gate driver 63**. Murphy ¶216, FIG. B5; *Reiner*, 9:12-22.

Mapping C: If Patent Owner’s view is adopted, FIG. C5 shows a **third protection circuit ESD2 or ESD3** being connected to **power supply line Vss** between the **second output device 70** from the top (**first scanning line driving unit circuit**) of the “many output devices” 70 and the **third output device 70** from the top (**second scanning line driving unit circuit**), the **second and third output devices 70** being adjacent to each other in **gate driver 63**. Murphy ¶217, FIG. C5; *Reiner*, 9:12-22.

Although the second and third output devices 70 are emphasized in FIGS. A5-C5, the same analysis applies to any two adjacent output devices 70 (e.g., third and fourth, twentieth and twenty-first, etc.) of gate driver 63 because *Reiner*'s "ESD protection network" provides "three ESD devices ESD1, ESD2, and ESD3 ... for each output device 70." *Reiner*, 3:4-8, 10:10-12; Murphy ¶218.

- a. **[1g]: "the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and"**
[1h]: "the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected."

[1g]-[1h] are substantively the same as [4e]-[4f]. *Reiner* discloses or renders obvious [1g]-[1h] as discussed in [4e]-[4f]. *Supra* §§ VII.A.1.f-VII.A.1.g; Murphy ¶¶220-221.

17. Claim 2

- a. [2a]: “The display device as set forth in claim 1, further comprising: a substrate,”
[2b]: “the scanning line driving circuit being arranged on the substrate,”
[2c]: “the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,”
[2d]: “the first protection circuit being arranged in the first corner portion of the substrate, and”
[2e]: “the second protection circuit being arranged in the second corner portion of the substrate.”

The additional limitations of [2a]-[2e] are substantively the same as those in [8a]-[8e], which *Reiner* discloses or renders obvious as discussed for [8a]-[8e].

Supra §§ VII.A.5.a-VII.A.5.e; Murphy ¶¶222-226.

18. Claim 3

- a. “An electronic device provided with the display device as set forth in claim 1.”

The additional limitations of claim 3 are substantively the same as those in claim 9, which *Reiner* discloses or renders obvious as discussed for claim 9. *Supra* § VII.A.6; Murphy ¶227.

B. Ground 2: Claims 1-18 Are Rendered Obvious by *Reiner* and *Takahara*

1. Independent Claim 4

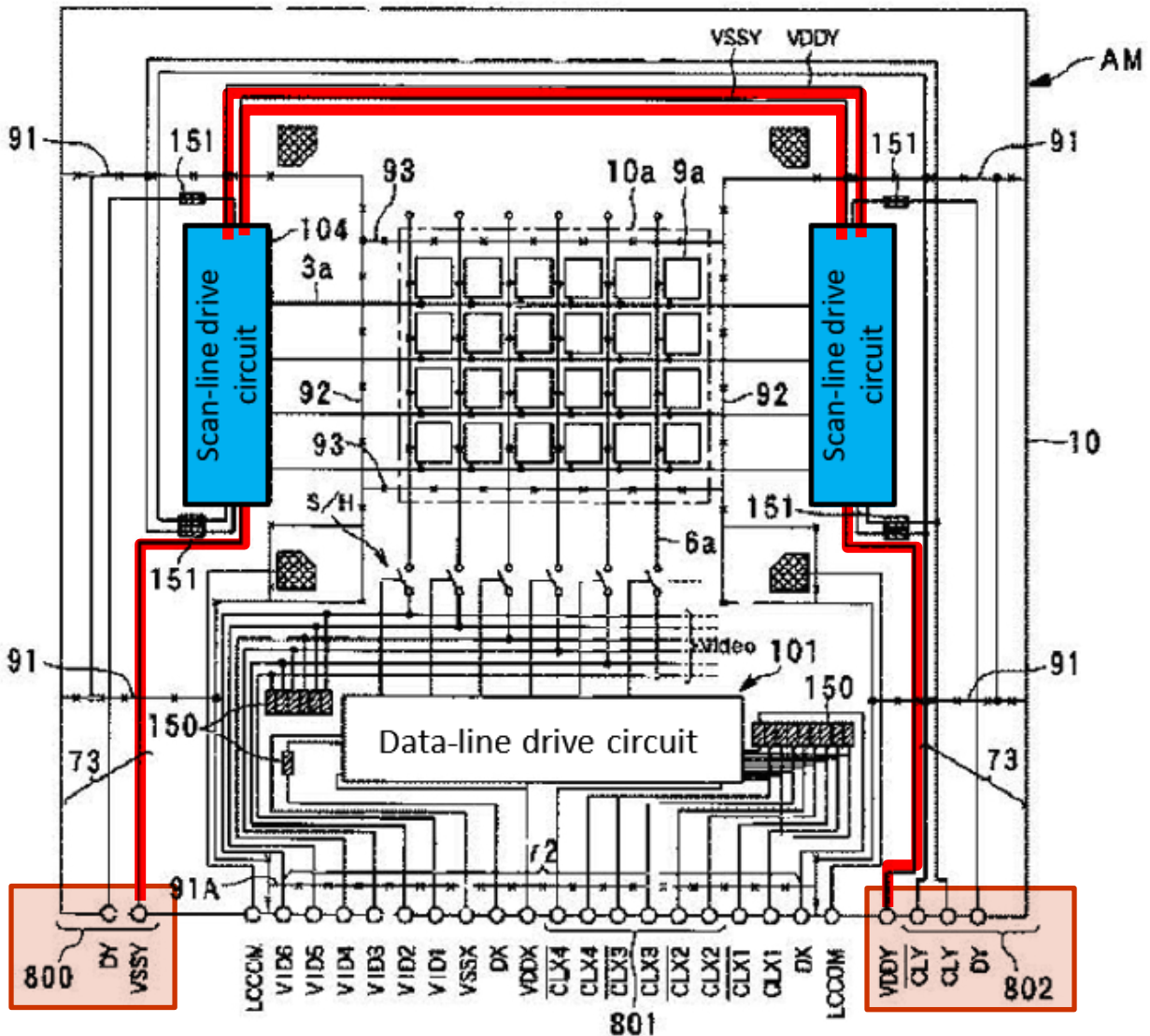
If Patent Owner argues or the Board finds that *Reiner* does not disclose or render obvious the input terminals of [4c] or that it would have been obvious to

protect the gate driver 63 (scanning line driver circuit) with ESD protection of [4d]-[4f], *Reiner* in view of *Takahara* would have rendered these obvious. Murphy ¶¶228-242.

a. [4c]

Takahara discloses that “terminals 800, 801, 802” (input terminals) provide power to power supply lines VDDY and VSSY “for driving the scan-line drive circuit 104.” *Takahara*, [0063], [0065]; Murphy ¶229.

FIG. 1



Takahara, FIG. 1.

A POSITA would have found it obvious to provide input terminals on *Reiner's* power supply lines Vdd, Vss of gate driver 63, which are equivalent to VDDY and VSSY of *Takahara*. Murphy ¶230.

i. Motivation

A POSITA would have been motivated to provide input terminals connected to *Reiner*'s power supply lines 71 (Vss), 73 (Vdd), such as *Takahara*'s input terminals for VDDY and VSSY, to supply power because the terminals would have provided a power connection from a power source to gate driver 63 to "drive the many lines of ... LCD display 60" to display images on the LCD screen. *Reiner*, 9:12-14; *Takahara*, [0063]. A POSITA would have recognized that *Reiner*'s gate driver 63 is arranged on a substrate, similar to *Takahara*'s active matrix substrate 10, to connect the gate driver 63's power supply lines with other components, such as power supply lines VDDY and VSSY on the substrate, and would have needed input terminal power connections 800, 801, 802 to power the Vdd (VDDY) and Vss (VSSY) power lines that drive the scanning line driving circuit, such as shown in *Takahara* FIG. 1. *Reiner*, 7:23-25; *Takahara*, [0063], [0066], FIG. 1; *see* Ex. 1001, 1:54-56, 2:5-14, FIG. 11 ("conventional art" includes input terminals to supply power via power lines). For example, the gate driver 63 could be bonded to the active matrix substrate at "contact pads 72" or other points of connection, such as the power lines running along the active matrix substrate to the scanning line driving unit. Moreover, a POSITA also would have found it obvious to form *Reiner*'s gate driver 63 directly on the glass substrate of *Takahara*, thereby eliminating the need for contact pads 72. As explained by Dr. Murphy,

glass substrates could exacerbate risks of ESD that could damage the gate driver 63 and therefore would have benefitted from ESD protection provided by *Reiner*'s protection circuits. Murphy ¶231.

A POSITA would have been motivated to provide input terminals connected to *Reiner*'s power lines Vdd (VDDY) and Vss (VSSY), as taught by *Takahara*, to supply power to gate driver 63 to drive gate lines 68 and so that LCD display 60 can display an image. Murphy ¶232.

ii. Expectation of Success

A POSITA would have reasonably expected to succeed in providing input terminals connected to *Reiner*'s power supply lines Vss, Vdd to supply power to gate driver 63, as taught by *Takahara*. Murphy ¶233. Using input terminals to supply power was admittedly “conventional art” for LCD displays that *Reiner*, *Takahara*, and the '157 patent each describe. *Reiner*, 7:23-25; Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751); *Takahara*, [0063], [0066], FIG. 1. Connecting *Reiner*'s power supply lines Vdd (VDDY), Vss (VSSY) to input terminals to provide power would have been merely the straightforward application of known, conventional techniques applied to *Reiner*'s power supply lines Vss, Vdd used according to their known functions to yield predictable results (providing a connection through which power flows to the power supply lines to power the gate driver 63). Murphy ¶233; *Reiner*, 9:12-13, 9:18-20, 9:27-29,

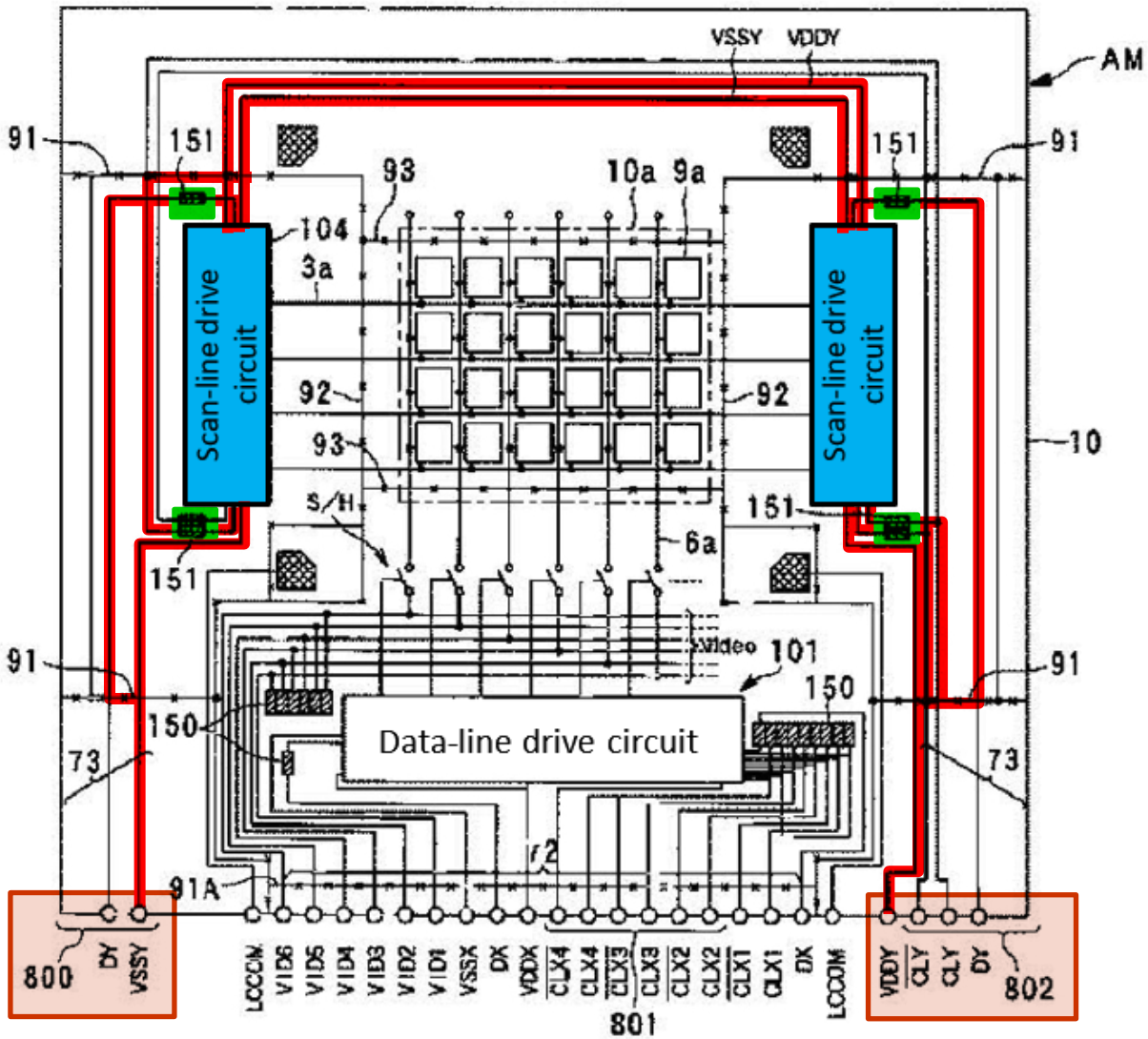
10:6-10, 12:4-5; *Takahara*, [0063], [0066], FIG. 1; *KSR*, 550 U.S. at 416; *Slot Speaker*, 680 F. App’x at 943-44.

b. [4d]-[4f]

If Patent Owner argues or the Board finds that *Reiner* does not disclose or render obvious providing ESD protection to protect a scanning line driving circuit, *Reiner* and *Takahara* render it obvious. Murphy ¶¶234-242.

Takahara discloses that “[e]lectrostatic [ESD] protection circuits 150 and 151 are formed at intermediate positions of the signal lines” 73, which include power lines VDDY, VSSY, so that “static electricity is reliably absorbed” and “scan-line drive circuit 104 can be reliably protected.” *Takahara*, [0066], FIG. 1. Power lines VDDY, VSSY are shorted to the ESD protection circuits 150 and 151 that protect both ends of scanning line driving circuit 104, as shown by the “x” on lines 91 between the wiring lines. *Takahara*, [0070]; Murphy ¶235.

FIG. 1



Takahara, FIG. 1.

A POSITA would have found it obvious to protect *Reiner*'s gate driver 63 using ESD protection, which *Takahara* confirms, to “reliably protect[]” the “very

sensitive circuits” of the driver “from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1; *Takahara*, [0066]; Murphy ¶236.

i. Motivation

A POSITA would have been motivated to provide a first and second protection circuit connected to the gate driver 63 to protect against ESD events and damage and also connected to the power supply lines that can be lines that are subject to ESD events, as explained in Ground 1, claim 4. *Reiner*, 2:28-3:1; *Takahara*, [0066], FIGS. 1, 3. A POSITA would have recognized that the “very sensitive circuits” of gate driver 63 are at risk from ESD damage, as explained in Ground 1, claim 4. *Reiner*, 2:28-3:1. A POSITA would have been motivated to “reliably protect[]” the gate driver from ESD damage and prevent the circuits of output devices of gate driver 63 from being damaged by ESD events. *Takahara*, [0066], FIGS. 1, 3 (items 150, 151). The ’157 patent admits it was “conventional art” to protect scanning line driving circuits using ESD protection circuits and *Reiner* and *Takahara* recognize the need to do so. *Reiner*, 2:28-3:1, 6:12-17, 8:30-31; *Takahara*, [0063], [0066], FIG. 1; Ex. 1001, 1:25-2:30; Murphy ¶237.

A POSITA would have been motivated to “protect the circuitry” of the output devices of *Reiner*’s gate driver 63 from being damaged by ESD events in the same way as source driver 61 to “reliably protect[]” gate driver 63 and its internal circuits because damage from ESD events could require costly repairs or

additional complex manufacturing repair processes or render the display unfit for use. *Reiner*, 10:10-12; *Takahara*, [0066]. A POSITA would have been motivated to provide ESD protection circuits to *Reiner*'s gate driver 63 because damage to either the gate driver or source driver by ESD events could render the LCD display unacceptably or irreparably damaged and unfit for use. *Reiner*, 2:28-3:1; *Takahara*, [0066]; Murphy ¶238.

A POSITA would have been motivated to “add an ESD protection network to [the] densely packed integrated circuit devices” of *Reiner*'s gate driver 63 because *Takahara* teaches that ESD protection circuits “reliably protect[]” both gate and scanning line drivers. *Reiner*, 4:15-16; *Takahara*, [0066]. A POSITA would have recognized that *Reiner*'s “densely packed” and “very sensitive” internal circuit elements would have benefitted from ESD protection to prevent them from being “destroyed” and therefore been motivated to protect them. *Reiner*, 2:28-3:1, 4:15-16; Murphy ¶239.

A POSITA would have also recognized that using *Reiner*'s “ESD protection network” of FIG. 5 to protect “each output device” of gate driver 63 (equivalent to output device 70) merely implements *Reiner*'s known prior-art ESD protection network to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s],” which *Takahara* confirms can be protected and was “conventional art.” *Reiner*, 4:15-16, 10:10-12; *Takahara*, [0066], FIGS. 1, 3;

Ex. 1001, 1:25-2:30. At a minimum, a POSITA would have found it obvious to try implementing *Reiner*'s ESD protection network to protect gate driver 63 and its many output devices, given *Reiner*'s suggestion that both source driver 61 and gate driver 63 contain "very sensitive circuits" can be "destroyed" by electrical or thermal ESD damage and *Takahara* confirms that both drivers can be protected by ESD protection circuits. *Reiner*, 2:28-3:1, 9:12-14; *Takahara*, [0066], FIG. 1; Murphy ¶240.

A POSITA also would have been motivated to implement a first and second ESD protection circuit connected to *Reiner*'s gate driver 63, in the configurations described in Ground 1, claim 4, to thermally and/or electrically protect *Reiner*'s gate driver 63 from ESD events as explained in Ground 1, claim 4. *Reiner*, 4:10-12, 9:16-22, 4:15-19, 12:15-18, claim 11; Murphy ¶241.

ii. Expectation of Success

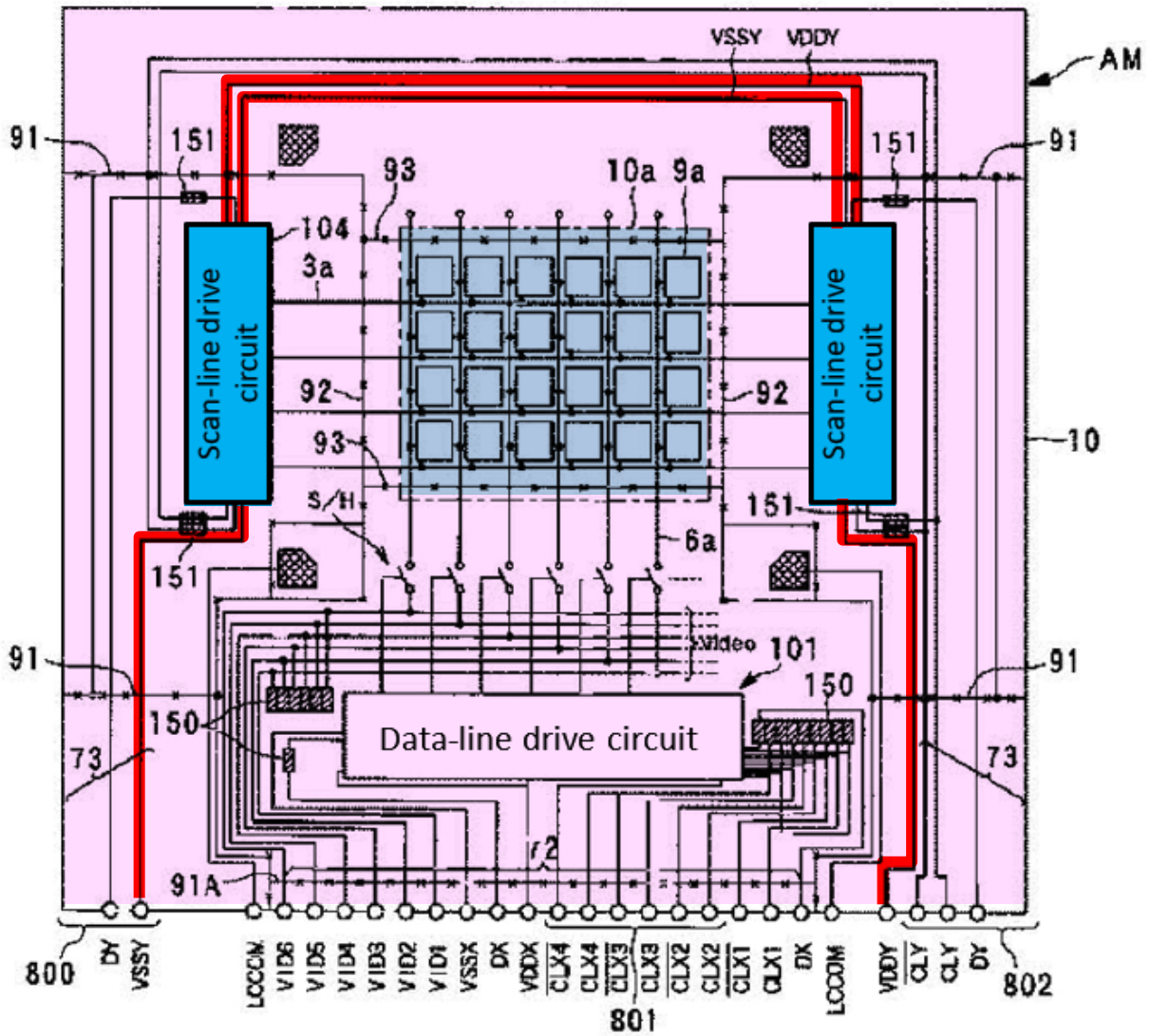
A POSITA would have had a reasonable expectation of success in implementing first and second ESD protection circuits to protect *Reiner*'s gate driver 63 and its output units as recited in claim 4 as discussed for Ground 1, claim 4. *Supra* §§ VII.A.1.e-VII.A.1.g; Murphy ¶242.

2. Claim 8

If Patent Owner argues or the Board finds that *Reiner* does not disclose or render obvious the additional limitations of claim 8, *Reiner* and *Takahara* render them obvious. Murphy ¶¶243-252.

Takahara discloses that a scan-line drive circuit 104 is arranged on substrate 10 that includes the active matrix for the LCD display. *Takahara*, [0064], FIG. 1. Scanning lines 3a and data lines 6a are formed on substrate 10 and intersect at active matrix pixel locations, and scan-line drive circuit 104 and power supply lines VDDY/VSSY are located on the periphery of substrate 10. *Takahara*, [0062], FIG. 1. Murphy ¶244.

FIG. 1



Takahara, FIG. 1.

A POSITA would have recognized that the display of *Reiner*'s FIG. 4 would have included a similar configuration to be placed on a substrate to support the

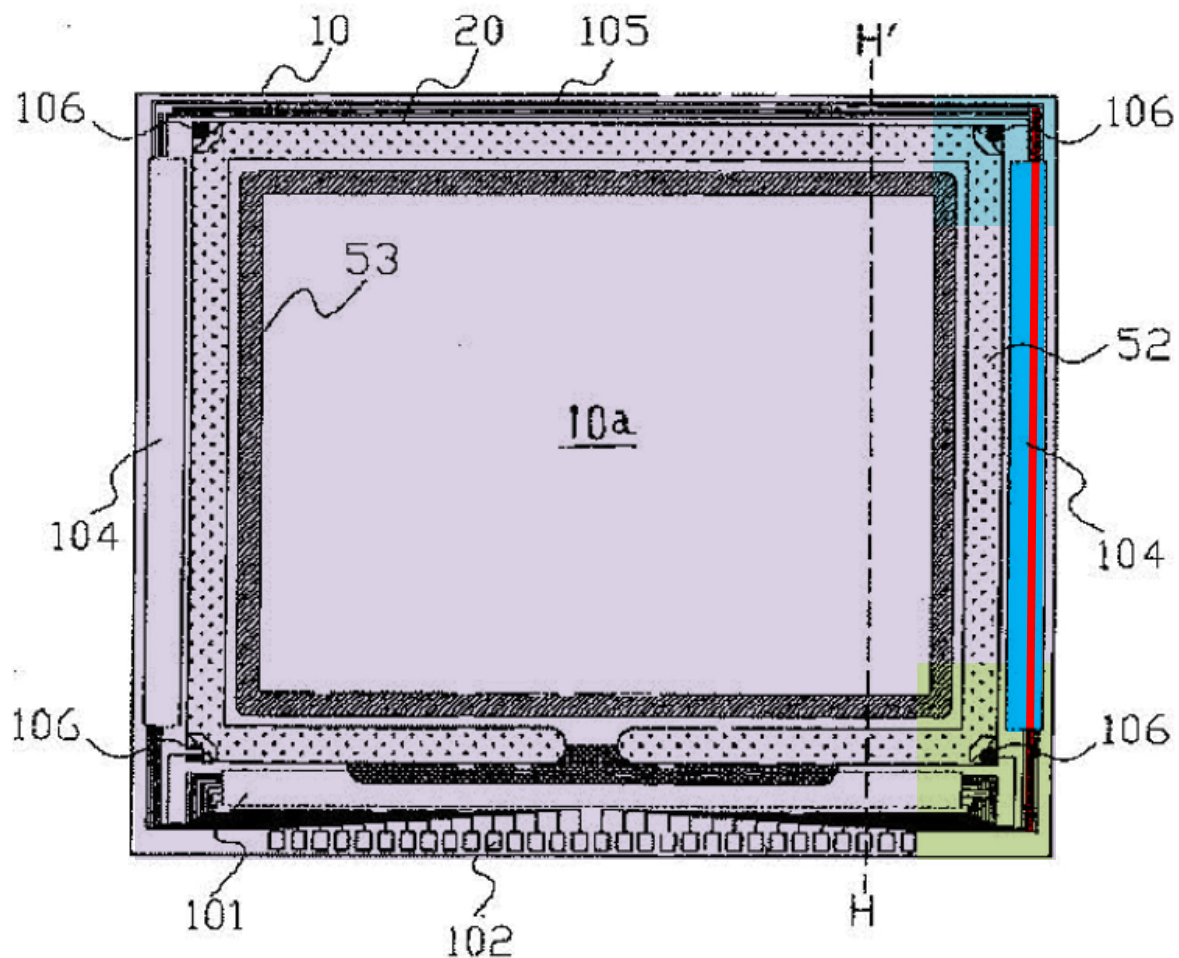
gate/scan lines 68, the source/data lines 67, pixels, and driver circuits 61, 63. This was well known in the art. *See Murai* [0017]-[0019], [0035], FIG. 1; Murphy ¶245.

Although *Takahara*'s FIG. 1 shows an active matrix of 4x6 pixels, a POSITA would have recognized that the active matrix typically has several hundred or more scan and data lines, rendering the peripheral area a small fraction of the overall substrate and that the ends of the scanning line drive circuits would have included the first and second protection circuits in corner portions of the substrate, as explained in Ground 1, claim 8, and shown in Dr. Murphy's FIG. E and *Takahara*'s FIG. 12. Murphy ¶¶246-247.



Murphy ¶246 (FIG. E).

FIG. 12



Takahara, FIG. 12.

i. Motivation

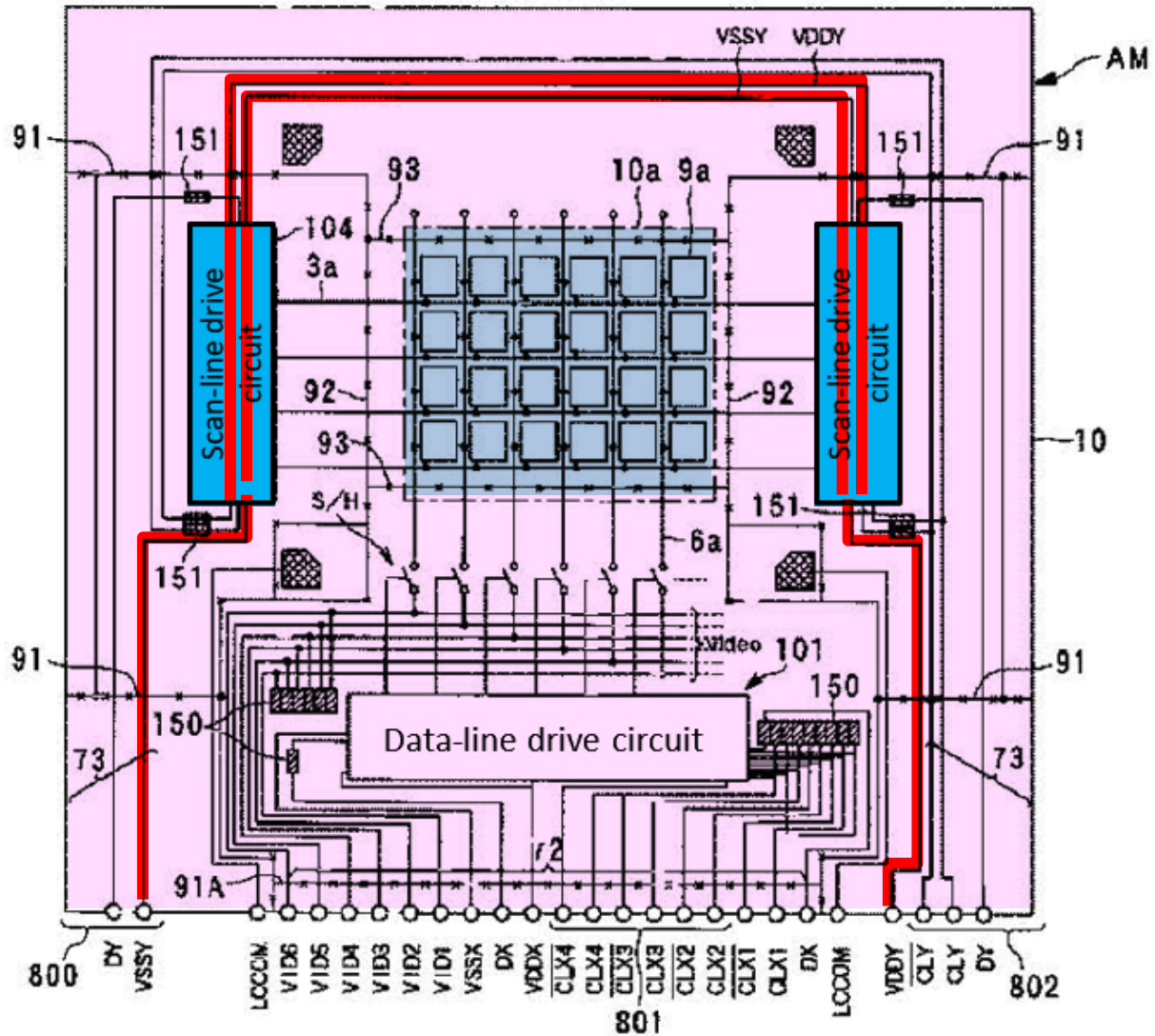
A POSITA would have been motivated to arrange *Reiner*'s source driver 63 on a substrate to support *Reiner*'s LCD display device and provide locations for wiring and circuitry, as taught by *Takahara* and conventional in the art. Murphy ¶248. *Reiner* discloses the driver unit having a silicon substrate 21 and being

bonded to the driven lines (source or gate lines) at contact pad 72. *Reiner*, 6:18-24, 10:1-6, FIGS. 4, 5. A POSITA would have been motivated to arrange *Reiner*'s gate driver 63 on a substrate to connect the gate driver to the scan lines being drive on the substrate and provide an integrated display unit that can be incorporated into electronic devices (e.g., laptop computer, PDA, television, computer monitor, cellular phone screen). *Takahara*, [0064]. A POSITA also would have been motivated to arrange the gate driver on a substrate to provide external terminals to power the active matrix and driver circuits and to connect to the CPU and power sources, such as an external power supply or battery. *Takahara*, [0064]; Murphy ¶249.

A POSITA would have been motivated to provide for the power supply lines feeding into *Reiner*'s gate driver 63 to be formed on the substrate, as shown in *Takahara*'s FIG. 1, because *Reiner* teaches that the power supply lines run “perpendicular to” the output lines (scan lines) of the driver circuits. *Reiner*, 10:7-10. A POSITA would have recognized that the most efficient way to run the power supply lines for gate driver 63 (whose outputs are *Reiner*'s scan lines 68; *Takahara*'s scan lines 3a) would be perpendicularly along the substrate's periphery, as shown in *Takahara*'s FIG. 1. As a result, a POSITA would have found it obvious to locate the first and second protection circuits in the first and

second corner portions of the substrate, as explained above for this Ground, claims 4 and 8, and also in Ground 1, claim 8. Murphy ¶249.

FIG. 1



Takahara, FIG. 1.

As also explained above in Ground 2, claim 4, a POSITA would have been motivated to form *Reiner*'s circuits directly on *Takahara*'s glass substrate to take advantage of additional protection from ESD events and also improve manufacturing. Murphy ¶250.

ii. Expectation of Success

A POSITA would have reasonably expected to succeed in arranging *Reiner*'s gate driver 63 on a substrate with power supply lines Vss, Vdd following the periphery of the substrate from a first corner portion to a second corner portion, such that the first and second protection circuits are placed in the first and second corners portions, as taught by *Takahara*. Arranging scanning line driving circuits on substrates was “conventional art” that *Reiner*, *Takahara*, and the '157 patent describe. *Reiner*, 7:23-25; *Takahara*, [0063], [0066], FIG. 1; Ex. 1001, 1:54-56, 2:5-14, FIG. 11; *Murai*, FIG. 1; Murphy ¶251.

Arranging *Reiner*'s gate driver, scan lines, and power lines on a substrate to facilitate manufacturing of the LCD display with the power lines running perpendicular to the scan lines, as taught by *Reiner* and *Takahara*, to provide power to gate driver 63 would have been merely the straightforward application of known, conventional techniques of patterning of power supply lines Vss, Vdd on a substrate, such as in the layout of *Takahara*, and arranging gate driver 63 on the substrate, using conventional techniques to either fabricate the driver circuit and

then attach it to the power lines and scan lines, as taught by *Reiner*, or to manufacture the driver directly on the glass substrate, according to their known functions to yield predictable results. Murphy ¶252; *Reiner*, 9:12-13, 9:18-20, 9:27-29, 10:6-10, 12:4-5; *KSR*, 550 U.S. at 416; *Slot Speaker*, 680 F. App'x at 943-44.

3. Independent Claims 1, 10, 16, 17, and 18

Reiner and *Takahara* render obvious the “input terminal,” connection, and protecting the scanning line driving circuit/power line/circuit element limitations of claims 1, 10, 16, 17, and 18 as discussed in Ground 2, claim 4, and in Ground 1, claims 1, 10, 16, 17, and 18. Murphy ¶¶253-254.

If Patent Owner argues or the Board finds that *Reiner* does not disclose the first and second protection circuits being at a first and second end of the scanning line driving circuit, as recited in claims 16-18, *Reiner* and *Takahara* render these limitations obvious as discussed for Ground 2, claim 8. Murphy ¶254.

4. Claims 2 and 14

Claims 2 and 14 are substantively similar to claim 8. *Reiner* and *Takahara* render obvious claims 2 and 14 as discussed for Ground 2, claim 8. Murphy ¶255.

5. Claims 3, 5, 6, 7, 9, 11, 12, 13, and 15

Reiner discloses or renders obvious the additional limitations of claims 3, 5, 6, 7, 9, 11, 12, 13, and 15 as discussed in Ground 1. Murphy ¶256.

VIII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office’s interim guidelines dated June 21, 2022 (“Interim Procedures”) require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 6 requires institution because this Petition’s merits are strong. The Petition relies upon materially different and non-cumulative references not applied during prosecution and teach the features the applicant argued are novel and lacking from the prior art.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions on March 11, 2024, less than three months ago. Ex. 1016. *See Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11 at 11 (March 20, 2020) (precedential); *CoolIT Sys., Inc. v. Asetek Danmark A/S*, IPR2021-01195, Paper 10 at 11, 14 (Dec. 28, 2021). Fact discovery opened only last month, and the claim construction hearing will not take place until January 2025; therefore, the district court’s investment by institution will be nominal. Ex. 1015.

Factor 4 favors institution because this petition challenges non-asserted claims 1-3, 6, and 12.

Regarding Factors 1, 2, and 5, Patent Owner filed its Complaint against Petitioner on November 8, 2023. Ex. 1014. No stay has been requested, trial is currently scheduled for June 2025, and the current median time-to-trial in the Eastern District of Texas is 21.4 months (Ex. 1017), so trial is projected to occur in August 2025 at the earliest. Ex. 1017. A FWD is anticipated by November 2025. *Fintiv* holistically considers all factors and the litigation trial date is not determinative, but weighed with the other relevant factors, and the Board has instituted under similar time frames. *NetNut Ltd., v. Bright Data Ltd.*, IPR2021-01492, Paper 12 at 9-16 (Mar. 21, 2022) (trial date six months before final written decision deadline; no stipulation regarding district court arguments made); *CoolIT*, IPR2021-01195, Paper 10 at 11, 14 (same by five months; *Sand II* stipulation); *Micron Tech., Inc., v. Vervain, LLC*, IPR2021-01550, Paper 11 at 9-13 (Apr. 11, 2022) (same).

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under § 325(d)

No other proceedings involving the '157 patent are currently pending or have been brought before the Office. Additionally, neither *Reiner* nor *Takahara* was before the Examiner during prosecution. Thus, the same or substantially the same prior art or arguments have not been previously presented to the Patent Office and denial of institution is not warranted under § 325(d).

IX. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in-interest is BOE Technology Group Co., Ltd.

B. Related Matters

Longitude Licensing asserted the '157 patent in the following litigation:

Longitude Licensing Ltd. v. BOE Technology Group Co., Ltd., Case No. 2:23-cv-00515-JRG (E.D. Tex.).

The '157 patent is a continuation of U.S. Patent No. 7,755,875 (U.S. Patent Application No. 11/101,450) and claims priority to Japanese Patent Application JP2004-198040. The following patents and patent application claim priority to the '157 patent: issued U.S. Patent Nos. 8,861,152; 10,181,462; 10,937,779; 11,362,071; and 11,955,473; and U.S. Patent Application No. 18/629,852, which is pending.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the addresses above.

Petitioner consents to electronic service by email at the above email addresses.

X. GROUNDS FOR STANDING

Petitioner certifies that the '157 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

XI. CONCLUSION

For the reasons set forth above, Petitioner has established a reasonable likelihood that the challenged claims are unpatentable. Petitioner requests institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: June 5, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under § 42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,994.

Dated: June 5, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), the **Petition for *Inter Partes* Review, the associated power of attorney, and Exhibits 1001-1017** were served via overnight courier on June 5, 2024, on the correspondence address of record below indicated in the Patent Office's Patent Center for U.S. Patent No. 9,184,157:

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Dated: June 5, 2024

By: /Lauren K. Young/
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Litigation Legal Assistant
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