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(54) Title of Invention ELECTRO-OPTICAL DEVICE

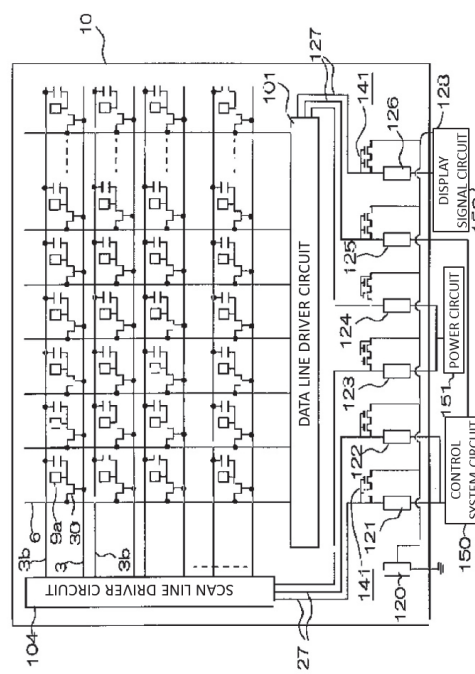
(57) Abstract

Problem

An electro-optical device comprising an electrostatic-breakdown-preventing circuit, wherein an electrostatic-breakdown-preventing circuit having higher electrostatic breakdown prevention effects is obtained.

Solution

Dual-gate TFTs 141, 142 that have been grounded as electrostatic-breakdown-preventing circuits are electrically connected to external-circuit connection terminal portions 121–126 used to input external signals to a scan line driver circuit 104 and a data line driver circuit 101. As a result, even if static electricity occurs, the current escapes to the ground as a result of the dual-gate TFTs turning on; thus, it is possible to prevent static-electricity-induced breakdown of, for example, TFTs disposed on the scan line driver circuit 104 and the data line driver circuit 101, and an electro-optical device having good display characteristics can be obtained.



CLAIMS

1. An electro-optical device having a switching element region in which a switching element is disposed on a substrate, comprising:
a wire for electrically connecting the switching element disposed on the substrate in the switching element region and a terminal; and

a dual-gate thin-film transistor that is electrically connected to the wire and grounded.

2. The electro-optical device according to claim 1, wherein the switching element region is constituted by: a plurality of data lines and a plurality of scan lines formed in a matrix shape; an image display region constituted by a pixel electrode and a pixel transistor disposed in correspondence with intersections of the data lines and the scan lines; and a driver circuit region constituted by a driver circuit for supplying a signal to at least one of the data lines and the scan lines.

3. The electro-optical device according to claim 1 or 2, further comprising:

a grounded semiconductor pattern extending from the switching element region;

wherein the dual-gate thin-film transistor is electrically connected to the semiconductor pattern.

4. The electro-optical device according to any one of claims 1-3, wherein:

the switching element comprises a first semiconductor layer and a first gate electrode disposed on the first semiconductor layer with a gate-insulating film interposed therebetween; and

the dual-gate thin-film transistor comprises a second semiconductor layer, which is constituted by the same layer as the first semiconductor layer, and a second gate electrode, which is disposed on the second semiconductor layer with the gate-insulating film interposed therebetween and is constituted by the same layer as the first gate electrode.

5. The electro-optical device according to claim 1 or 2, wherein:

the dual-gate thin-film transistor, which is electrically connected to a wire comprising the terminal portion to which is inputted a control system signal or a display signal, comprises:

a semiconductor layer having two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and

two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions;

a grounded ground wire is electrically connected to the drain region; and

the gate electrodes and the source region are electrically connected to the wire.

6. The electro-optical device according to claim 1 or 2, wherein:

the dual-gate thin-film transistor, which is connected to a wire comprising the terminal portion to which a power system signal is inputted, comprises:

a semiconductor layer having two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and

two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions;
the wire is electrically connected to the drain region; and
a grounded ground wire is electrically connected to the gate electrodes and the source region.

7. The electro-optical device according to claim 1 or 2, wherein:

the dual-gate thin-film transistor, which is electrically connected to a wire comprising the terminal portion to which is inputted a control system signal or a display signal, comprises:

a semiconductor layer having two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and

two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions; and

a grounded ground wire is electrically connected to the drain region and the drain-side gate electrode; and

the source-side gate electrode and the source region are electrically connected to the wire.

8. An electro-optical device comprising:

a plurality of scan lines and a plurality of data lines disposed on a substrate;

an image display region constituted by a pixel electrode and a pixel switching element disposed in correspondence with intersections of the scan lines and the data lines; and

a peripheral driver circuit including at least one of a scan line driver circuit for supplying a signal to the scan lines and a data line driver circuit for supplying a signal to the data lines;

wherein:

a signal from a terminal portion is supplied to the peripheral driver circuit via a wire; and

a dual-gate transistor is electrically connected to the wire.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD PERTAINING TO THE INVENTION

The present invention pertains to manufacturing methods for electro-optical devices, and particularly pertains to the technical field of electrostatic-breakdown-preventing circuits used in driver-circuit-integrated electro-optical devices in which an image display region and a driver circuit are formed on the same substrate.

[0002]

RELATED ART

Generally, in an active-matrix-type liquid-crystal device comprising a thin-film transistor (hereinafter referred to as a TFT) as a switching element, an electro-optical substance such as a liquid-crystal layer is sandwiched between a TFT array substrate and an opposing substrate.

[0003]

An image display region and a driver circuit for controlling display in this image display region are disposed on said TFT array substrate. An external-circuit connection terminal portion electrically connected to the driver circuit is disposed on the TFT array substrate, and control system signals, such as clock signals, and display signals are externally inputted to the external-circuit connection terminal portion. Moreover, a single-gate thin-film transistor is disposed on the TFT array substrate partway along a wire connecting the external-circuit connection terminal portion and the driver circuit as an electrostatic-breakdown-preventing circuit for preventing, for

example, electrostatic breakdown of the driver circuit caused by static electricity generated during the assembly of the liquid-crystal device.

[0004]

PROBLEMS TO BE SOLVED BY THE INVENTION

However, there have been instances in which the electrostatic-breakdown-preventing circuit described above has insufficient pressure resistance, and the electrostatic-breakdown-preventing circuit itself breaks down due to the generation of static electricity of high voltage such as 1,000V. When the electrostatic breakdown circuit breaks down, static electricity may cause breakdown of the switching element disposed on the image display region and the driver circuit, and there is the problem of pronounced degradation of the display characteristics of the electro-optical device.

[0005]

The present invention was created in view of the problem described above, and has an object of providing an electro-optical device structure having sufficient electrostatic breakdown prevention effects.

[0006]

MEANS FOR SOLVING THE PROBLEMS

In order to solve the problem described above, the electro-optical device according to the present invention is an electro-optical device having a switching element region in which a switching element is disposed on a substrate, the device comprising: a wire for electrically connecting the switching element disposed on the substrate in the switching element region and a terminal; and a dual-gate thin-film transistor that is electrically connected to the wire and grounded.

[0007]

In accordance with this configuration of the present invention, the dual-gate thin-film transistor is turned ON when a high current enters from the terminal portion due to the generation of static electricity or the like, and the high current is shunted to ground via the dual-gate thin-film transistor; thus, there is the effect of preventing electrostatic breakdown of the switching element. In addition, as a result of using a dual-gate thin-film transistor as the electrostatic-breakdown-preventing circuit, it is possible to improve the pressure resistance of the electrostatic-breakdown-preventing circuit compared to instances in which a single-gate thin-film transistor is used. As a result, it is possible to reduce the incidence of electrostatic breakdown of the switching element and obtain an electro-optical device having excellent display characteristics. In addition, there is better responsiveness compared to instances in which a thin-film transistor having an LDD structure is used as an electrostatic-breakdown-preventing circuit; thus, even if static electricity is generated, the thin-film transistor acting as the electrostatic-breakdown-preventing circuit is promptly turned ON.

[0008]

The present invention is also characterized in that the switching element region is constituted by: a plurality of data lines and a plurality of scan lines formed in a matrix shape; an image display region constituted by a pixel electrode and a pixel transistor disposed in correspondence with intersections of the data lines and the scan lines; and a driver circuit region constituted by a driver circuit for supplying a signal to at least one of the data lines and the scan lines. As a result of this configuration, it is possible to obtain a driver-circuit-integrated electro-optical device in which the image display region and the driver circuit region are formed on the same substrate, wherein static-electricity-induced switching element breakdown can be prevented and an electro-optical device of superior display characteristics can be obtained.

[0009]

The present invention is also characterized in that the switching element comprises a first semiconductor layer and a first gate electrode disposed on said first semiconductor layer with a gate-insulating film interposed therebetween; and the dual-gate thin-film transistor comprises a second semiconductor layer that is constituted by the same layer as the first semiconductor layer, and a second gate electrode that is disposed on the second semiconductor layer with the gate-insulating film interposed therebetween and is constituted by the same layer as the first gate electrode. As a result of this configuration, the switching element in the switching element region and the dual-gate thin-film transistor can be formed in the same step; thus, the dual-gate thin-film transistor can be manufactured without increasing manufacturing steps.

[0010]

In addition, [the present invention] is also characterized by further comprising a grounded semiconductor pattern extending from the switching element region, and the dual-gate thin-film transistor being electrically connected to the semiconductor pattern. As a result of this configuration, the semiconductor pattern, which is formed in a different layer than the wire, can be disposed over a wide range on the substrate, thus making it possible to obtain a wide grounded area. As a result, there is the effect that, even if high current is generated, the current can be efficiently shunted to the semiconductor pattern, and it is possible to obtain an electrostatic-breakdown-preventing circuit having higher electrostatic breakdown effects.

[0011]

The present invention is also characterized in that the dual-gate thin-film transistor, which is connected to a wire comprising the terminal portion to which is inputted a control system signal or a display signal, comprises: a semiconductor layer comprising two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions; wherein a grounded ground wire is electrically connected to the drain region; and the gate electrode and the source region are electrically connected to the wire. The dual-gate thin-film transistor thus configured is constantly in an ON state during normal operation of the electro-optical device, and can be used as an electrostatic-breakdown-preventing circuit when control system signals (such as clock signals), display signals, and the like are periodically inputted.

[0012]

In addition, [the present invention] is also characterized in that the dual-gate thin-film transistor, which is electrically connected to a wire comprising the terminal portion to which is inputted a control system signal or a display signal, comprises: a semiconductor layer comprising two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions; wherein a grounded ground wire is electrically connected to the drain region and the drain-side gate electrode; and the drain-side gate electrode and the source region are electrically connected to the wire. The dual-gate thin-film transistor thus configured is constantly in an ON state during normal operation of the electro-optical device, and can be used as an electrostatic-breakdown-preventing circuit when control system signals (such as clock signals),

display signals, and the like are periodically inputted.

[0013]

The present invention is also characterized in that the dual-gate thin-film transistor, which is connected to a wire comprising the terminal portion to which is inputted a power system signal, comprises: a semiconductor layer comprising two channel regions, and a source region and a drain region disposed with the two channel regions therebetween; and two gate electrodes disposed over the semiconductor layer with a gate-insulating film interposed therebetween and in correspondence with the channel regions; wherein the wire is electrically connected to the drain region; and a grounded ground wire is electrically connected to the gate electrodes and the source region. As a result of this configuration, the gate electrodes are grounded, and the dual-gate thin-film transistor is in an OFF state during normal operation of the electro-optical device and thus can be used as an electrostatic-breakdown-preventing circuit when a constant potential, such as a power system signal, is applied.

[0014]

The present invention is characterized by comprising: a plurality of scan lines and a plurality of data lines disposed on a substrate; an image display region constituted by a pixel electrode and a pixel switching element disposed in correspondence with intersections of the scan lines and the data lines; and a peripheral driver circuit including at least one of a scan line driver circuit for supplying a signal to the scan lines and a data line driver circuit for supplying a signal to the data lines; wherein a signal from a terminal portion is supplied to the peripheral driver circuit via a wire, and a dual-gate transistor is electrically connected to the wire.

[0015]

According to this configuration of the present invention, when high current enters from the terminal portion due to the generation of static electricity or the like, the dual-gate thin-film transistor is turned ON, and the high current is shunted to ground via the dual-gate thin-film transistor; thus, there is the effect of preventing electrostatic breakdown of the switching element. In addition, as a result of using a dual-gate thin-film transistor as the electrostatic-breakdown-preventing circuit, it is possible to improve the pressure resistance of the electrostatic-breakdown-preventing circuit compared to instances in which a single-gate thin-film transistor is used. As a result, it is possible to reduce the incidence of electrostatic breakdown of the switching element and obtain an electro-optical device having excellent display characteristics. In addition, there is better responsiveness compared to instances in which a thin-film transistor having an LDD structure is used as an electrostatic-breakdown-preventing circuit; thus, even if static electricity is generated, the thin-film transistor acting as the electrostatic-breakdown-preventing circuit is promptly turned ON.

[0016]

MODES FOR CARRYING OUT THE INVENTION

(First Embodiment)

Hereinafter, a first embodiment of the present invention will be described, on the basis of the drawings, using an example of application to a liquid-crystal device as the electro-optical device.

[0017]

The configuration of the liquid-crystal device according to the present invention will be described with reference to FIG. 1 through FIG. 4. FIG. 1 is a diagram illustrating an equivalent circuit of various elements, wires, and the like in a plurality of pixels formed in a matrix shape constituting an image display region of the liquid-crystal device, and an equivalent circuit of an electrostatic-breakdown-preventing circuit. FIG. 2 is a plan view of a plurality of pixel groups in a pixel image display region of a TFT array substrate on which data

lines, scan lines, pixel electrodes, and the like are formed. FIG. 3 is a partial, enlarged view of a TFT array substrate for explaining the electrostatic-breakdown-preventing circuit. FIG. 4 is a longitudinal cross-sectional view along each of A-A', B-B', and C-C' in FIG. 3. In the drawings, the various layers and various members are differently scaled to sizes such that the various layers and various members are discernible in the drawings.

[0018]

The liquid-crystal device is constituted by a liquid-crystal cell in which a liquid-crystal layer is sandwiched between a TFT array substrate and an opposing substrate, and an externally connected external control circuit substrate on which is disposed a driver circuit for inputting various types of signals and which is connected to an external-circuit connection terminal portion disposed on the TFT array substrate. A counter electrode is disposed on the opposing substrate, a pixel electrode is disposed on the TFT array substrate, and the optical characteristics of the liquid crystal are altered by the difference in potential between the counter electrode and the pixel electrode to create a display on the liquid-crystal device.

[0019]

As shown in FIG. 1, a TFT array substrate 10 is constituted by a switching element region in which a switching element is disposed, and, beyond this switching element region, a terminal portion region in which the external-circuit connection terminal portion is disposed.

[0020]

The switching element region comprises an image display region and a peripheral driver circuit region disposed adjacent to the image display region. Capacitor lines 3b and scan lines 3 disposed in parallel, data lines 6 disposed intersecting the scan lines 3, pixel electrodes 9a disposed in a matrix shape in correspondence with the intersections of the scan lines 3 and the data lines 6, and thin-film transistors (hereinafter referred to as TFTs) 30 serving as switching elements for controlling the pixel electrodes 9a are disposed in the image display region. Sources of the TFTs 30 are electrically connected to the data lines 6, to which an image signal is supplied, and gates of the TFTs 30 are electrically connected to the scan lines 3, to which a scan signal is supplied. A scan line driver circuit 104 and a data line driver circuit 101 are disposed in the peripheral driver circuit region, the scan line driver circuit 104 supplies the scan line signal to the scan lines 3, and the data line driver circuit 101 supplies the image signal to the data lines 6.

[0021]

Meanwhile, external-circuit connection terminal portions 121–126 and a ground terminal 120 that are electrically connected to the scan line driver circuit 104 and the data line driver circuit 101, respectively, by wires 127 are disposed in the terminal portion region. Various types of signals are inputted to the external-circuit connection terminal portions 121–126 from a control system circuit 150, a power circuit 151, and a display signal circuit 152 disposed on an externally connected external control circuit substrate (not shown in the drawings). Dual-gate TFTs—specifically, TFTs 141, 142 in which two transistors are connected in series—are electrically connected to the external-circuit connection terminal portions 121–126 as electrostatic-breakdown-preventing circuits. Drain regions of semiconductor layers of the dual-gate TFTs 141, 142 are electrically connected to the ground terminal 120 via a ground wire 128, and the ground terminal is grounded. The dual-gate TFTs 141, 142 have different structures

depending on the types of signals to be input to the electrically connected external-circuit connection terminal portions. While the specific structures will be discussed later, the connection structures of the gate electrodes differ between the dual-gate TFT 141, which connects to the external-circuit connection terminal portions 121, 122, 125, 126, into which are applied control system signals and image signals, which periodically apply potentials, and the dual-gate TFT 142, which connects to the external-circuit connection terminal portions 123, 124, into which are inputted a power system signal, which constantly applies a potential.

[0022]

The scan line driver circuit 104 of the peripheral driver circuit line-sequentially applies a pulsed scan signal to the scan lines 3 at a prescribed timing according to power supplied from the power circuit, which is an external control circuit, and a reference clock, an inverted clock, and the like supplied from the control system circuit, which is an external control circuit.

[0023]

In addition, the data line driver circuit 101 of the peripheral driver circuit is constituted by a sampling circuit and a pre-charging circuit. In the data line driver circuit 101, a sampling circuit driver signal for each of the data lines 6 is supplied to the sampling circuit at a prescribed timing, in keeping with the timing at which the scan line driver circuit 104 applies the scan signal, according to the power supplied from the power circuit and the reference clock CLX, inverted clock, and the like supplied from the control system circuit. A pre-charging circuit driver signal is supplied to the pre-charging circuit from the external control circuit so that a pre-charging signal for each of the data lines 6 is written at a timing preceding the supply of the image signal. When the image signals supplied from the image signal circuit 152 are inputted, the sampling circuit samples them. In other words, when the sampling circuit driver signal is inputted, image signals are sequentially applied to the data lines 6.

[0024]

Next, the structure of the wires, pixel electrodes, etc., in the image display region of the TFT array substrate will be described using FIG. 2.

[0025]

As shown in FIG. 2, the plurality of transparent pixel electrodes 9a is provided in a matrix shape on the TFT array substrate of the liquid-crystal device, and the data lines 6, the scan lines 3 (dotted lines), and the capacitor lines 3b (dotted lines) are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a. The data lines 6 are formed with shapes that are elongated in the vertical direction, the data lines 6 are electrically connected via contact holes 5a to source regions, to be described later, of semiconductor layers 1 (diagonal line portions) constituted by polysilicon films, and the data lines 6 are formed so as to be wider in width in the vicinities of regions connected to the source regions. Conductive layers 6b formed from the same layer as the data lines 6 are electrically connected to drain regions, to be described later, of the semiconductor layers 1 via contact holes 5b, and the conductive layers 6b are further electrically connected to the pixel electrodes 9a via contact holes 8. In addition, the scan lines 3 are disposed so as to oppose channel regions of the semiconductor layers 1, the scan lines 3 function as gate electrodes, and, in the present embodiment, there are two locations where the semiconductor layers 1 and scan lines 3

overlap, creating a double-gate structure. Note that, in the drawings, the portions in which the scan lines 3 and the semiconductor layers 1 overlap in plan view, i.e., the semiconductor layers at the locations corresponding to the gate electrodes, are hidden by the scan lines and thus not shown in the drawings. The capacitor lines 3b extend substantially linearly along the scan lines 3 and have protruding portions protruding along the data lines 6 from the locations where they intersect the data lines 6; and portions of the semiconductor layers are disposed substantially in correspondence with the protruding portions. The capacitor lines 3b overlap portions of the pixel electrodes 9a in plan view, form capacitors in these regions, and further form capacitors with the pixel electrodes 9a. The semiconductor layers 1 extend below the data lines 6 and the scan lines 3, and are similarly disposed opposing the portions of the capacitor lines 3b that extend along the data lines 6 and the scan lines 3, with insulating films 2 interposed therebetween, to form capacitors.

[0026]

Also, although not shown in the drawings, a complementary-structure TFT serving as a switching element is disposed in the peripheral driver circuit; this complementary-structure TFT is constituted by a p-channel TFT and an n-channel TFT and is formed in the same step as the TFTs in the display region.

[0027]

Next, the structure of the terminal portion region will be described using FIG. 3 and FIG. 4. FIG. 3 is a partial, enlarged plan view of the vicinity of the terminal portion region in which the ground terminal 120 and the external-circuit connection terminal portions 121–126 in FIG. 1 are disposed, and FIG. 4 is a longitudinal cross-sectional view along lines A-A', B-B', and C-C' in FIG. 3.

[0028]

As shown in FIG. 3, the external-circuit connection terminal portions 121–126 are electrically connected to the scan line driver circuit or the data line driver circuit via the wires 127. Furthermore, the wires 127 are electrically connected to the dual-gate TFTs 141, 142, the dual-gate TFTs 141, 142 are connected to the ground terminal 120 via the ground wire 128, and the ground terminal 120 is grounded.

[0029]

The wires 127 comprise branching portions 127a and, in the wires connected to the external-circuit connection terminal portions 121, 122, 125, 126, further comprise rebranching portions 127b that further branch from the branching portions. The branching portions 127a are electrically connected via contact holes 130, 132 to source regions 135c, 136c of semiconductor layers 135, 136 of the corresponding dual-gate TFTs 141, 142. In addition, drain regions 135b, 136b of the semiconductor layers 135, 136 of the respective dual-type TFTs 141, 142 are electrically connected to the ground wire 128 via the contact holes 130, 132.

[0030]

The dual-gate thin film transistor 141, which is connected to the external-circuit connection terminal portions 121, 122, 125, 126 to which, among the external-circuit connection terminal portions, the control system signal and the display signal are inputted, is disposed on a glass substrate 60 on which a base film 12 is formed, as shown in FIG. 4 (longitudinal cross-sectional views A-A' and B-B'), and is constituted by: a semiconductor layer comprising two channel regions 135a, as well as a source region

135b and a drain region 135c disposed with the two channel regions 135a sandwiched therebetween; and two gate electrodes 131 disposed, in correspondence with the channel regions 135a, over the semiconductor layer with a gate-insulating film 2 interposed therebetween. Furthermore, as shown in the drawings, an interlayer insulating film 4 is disposed covering the gate electrodes 131, and the branching portions 127a of the wires 127, which are electrically connected to the source region 135b of the semiconductor layer 135, and the ground wire 128, which is electrically connected to the drain region 135c, are disposed on the interlayer insulating film 4. The gate electrodes 131 are electrically connected to the rebranching portions 127b via contact holes 133. Furthermore, an interlayer insulating film 7 is disposed covering the TFT 141.

[0031]

In addition, the dual-gate thin film transistor 142, which is connected to the external-circuit connection terminal portions 123, 124 to which, among the external-circuit connection terminal portions, the power system signal is inputted, is disposed on the glass substrate 60 on which the base film 12 is formed, as shown in FIG. 4 (longitudinal cross-sectional view C-C'), and is constituted by: a semiconductor layer 136 comprising two channel regions 136a, as well as a source region 136b and a drain region 136c that are disposed with the two channel regions 136a sandwiched therebetween; and two gate electrodes 134 disposed over the semiconductor layer 136 in correspondence with the channel regions 136a with the gate-insulating film 2. Furthermore, as shown in the drawings, the interlayer insulating film 4 is disposed covering the gate electrodes 134; and the branching portions 127a of the wires electrically connected to the source region 136b of the semiconductor layer 136, and a branching portion 128a of the ground wire electrically connected to the drain region 136c, are disposed on the interlayer insulating film 4. The gate electrodes 134 are electrically connected to the ground wire 128. Furthermore, the interlayer insulating film 7 is disposed covering the TFT 141.

[0032]

Next, a manufacturing method for the TFT array substrate will be described using FIG. 5 to FIG. 13. Note that FIG. 5 to FIG. 13 show longitudinal cross-sectional views of the switching element region, which comprises a peripheral circuit region and the image display region, and longitudinal cross-sectional views of the terminal portion region. Note that the longitudinal cross-sectional views in the image display region are longitudinal cross-sectional views along line E-E' in FIG. 2, and the longitudinal cross-sectional views in the terminal portion region correspond to FIG. 4.

[0033]

First, as shown in FIG. 5(a), an SiO₂ film serving as the base film 12 is formed on the glass substrate 60 via PE (plasma-enhanced) CVD or ECR (electron cyclotron resonance) CVD to a thickness of approximately 200–500 nm. This base film has a function of preventing contamination on the surface of the glass substrate 60 or of preventing impurities contained in the glass substrate from causing degradation of the characteristics of the TFT 30.

[0034]

Next, as shown in FIG. 5(b), an a-Si film 401a is laid over the base film to a thickness of approximately 30–100 nm via PECVD or LP (low-pressure) CVD.

[0035]

Next, as shown in FIG. 5(c), the a-Si film is crystallized by

irradiating the a-Si film with an excimer laser beam such as KrF or XeCl at 300–600 mJ/cm² to obtain a p-Si film 401b. The irradiation intensity, irradiation time, etc., of the excimer laser light are adjusted, as appropriate, according to the film thickness, film quality, etc., of the a-Si film. In the present embodiment, a polysilicon layer can be obtained at a lower temperature via laser annealing; thus, a glass substrate, which is less expensive than a silicon substrate, can be used as the substrate.

[0036]

Next, as shown in FIG. 5(d), a photoresist film 402 is formed in a shape corresponding to the semiconductor layers of the TFT in the image display region and the peripheral driver circuit region, respectively, and in a shape corresponding to the semiconductor layer of the dual-gate TFT disposed in the terminal portion region.

[0037]

Next, as shown in FIG. 6(a), the p-Si film 401b is etched via RIE (reactive ion etching) using a chlorine-based gas, and with the photoresist film 402 serving as a mask, to form a p-Si layer 1 and the semiconductor layers 135, 136 of the dual-gate TFT. Note that, apart from dry etching such as RIE, wet etching using a chemical solution, such as etching using a mixture of hydrofluoric acid and nitric acid, can also be used.

[0038]

Next, as shown in FIG. 6(b), the photoresist film 402 is stripped, after which, as shown in FIG. 6(c), the gate insulating film 2, which has a film thickness of 50–120 nm, is formed via PECVD using a mixed gas of TEOS (tetraethyl orthosilicate) and oxygen gas as a feedstock gas. SiH₄ and oxygen gas may be used as feedstock gases.

[0039]

Next, as shown in FIG. 6(d), a photoresist film 403 is formed in the shape of the semiconductor layer 1 of the image display region from which a portion corresponding to the region functioning as a capacitor is removed. Then, using the photoresist film 403 as a mask, phosphorus ions are implanted into the semiconductor layer 1 as an impurity via ion implantation at a dosage of 5×10^{14} to 10^{16} /cm² to form a capacitor electrode 1f. After implantation, the photoresist film 403 is stripped.

[0040]

Next, as shown in FIG. 7(a), a two-layer film 405 constituted by an aluminum film and a titanium nitride film having a film thickness of 200–600 nm—in this instance, 400 nm—is formed on the gate-insulating film 2 via PVD (physical vapor deposition).

[0041]

Next, as shown in FIG. 7(b), a photoresist film 404 is formed that has a shape corresponding to the scan lines, gate electrodes, and capacitor lines in the switching element region and has a shape corresponding to the gate electrodes of the dual-gate TFT connected to the external-circuit connection terminal portion to which the control system signal, the electrical system signal, and the image signal are inputted in the terminal portion region. Using this as a mask, the two-layer film 405 constituted by an aluminum film and a titanium nitride film is etched via RIE using a fluorine-based or chlorine-based gas, as shown in

FIG. 7(c). As shown in FIG. 8(a), after etching, the photoresist film 404 is stripped to obtain, in the switching element region, the scan lines, gate electrodes 3a, 103, and the capacitor lines 3b that have a multilayer structure constituted by an aluminum lower layer and a titanium nitride upper layer; and to obtain, in the terminal portion region, the gate electrodes 131 and 134 of the dual-gate TFT connected to the external-circuit connection terminal portions to which the control system signal, electrical system signal, and image signal are inputted.

[0042]

Next, as shown in FIG. 8(b), a photoresist film 405 is formed in a shape in which the location corresponding to the semiconductor layer 1 constituting a p-channel TFT 140b in the peripheral circuit region has been removed. Subsequently, using the photoresist film 405 and the gate electrode 103 corresponding to the p-channel TFT as a mask, 5×10^{14} to $10^{16}/\text{cm}^2$ boron ions are implanted into the semiconductor film 1 via ion implantation to obtain the semiconductor layer 1 having a channel region 1a, a source region 1g, and a drain region 1h that are self-aligned with respect to the gate electrode 103.

[0043]

Next, the photoresist film 405 is stripped as shown in FIG. 8(c), after which a photoresist film 406 is formed that has a shape corresponding to the semiconductor layer 1 constituting the p-channel TFT 140b in the peripheral circuit region, as shown in FIG. 8(d). The semiconductor layers 1, 135, 136 are implanted with 5×10^{12} to $2 \times 10^{14}/\text{cm}^2$ phosphorus ions via ion implantation using, as masks, the photoresist film 406, the gate electrode 3a, the gate electrode 103 corresponding to the N-channel TFT, capacitor lines 3b, and the gate electrodes 131 and 134 corresponding to the dual-gate TFTs connected to the external-circuit connection terminal portions to which the control system signal, electrical system signal, and image signal are inputted. As a result, the semiconductor layer 1 corresponding to an N-channel TFT comprising the channel region 1a, which is self-aligned with respect to the gate electrode 103, as well as a low-density source region 1b and a low-density drain region 1c having a lower impurity density than a high-density source region and a high-density drain region that are subsequently formed, are obtained in the peripheral circuit region. In addition, the semiconductor 1 comprising the channel regions 1a at two locations (only one of which is shown in the drawings) and the low-density source region 1b and the low-density drain region 1c, which are formed sandwiching the channel regions at these two locations and have lower impurity densities than a high-density source region and a high-density drain region that are subsequently formed, is obtained in the image display region. In addition, the semiconductor layer 135 corresponding to the dual-gate TFT connected to the external-circuit connection terminal portions to which the control system signal and the image signal are inputted comprises two channel regions 135a and source regions 135b, 135c disposed sandwiching the two channel regions, and has a self-aligned structure. The semiconductor layer 136 corresponding to the dual-gate TFT connected to the external-circuit connection terminal portions to which the power system signal is inputted comprises two channel regions 136a and source regions 136b, 136c disposed sandwiching the two channel regions, and has a self-aligned structure.

[0044]

Next, as shown in FIG. 9(a), a photoresist film 407 is formed that has a pattern shape that covers the semiconductor layer of the P-channel TFT 140b, has a shape that covers the peripheral portions of the gate electrode 103 of an N-channel TFT 140a and the gate electrode 3a of the TFT in the image display region, and has a shape corresponding to the portion constituting the channel regions of the semiconductor layer of the dual-gate TFT. Using this as a mask, 5×10^{14} to $10^{16}/\text{cm}^2$ phosphorus ions are implanted into the semiconductor layers 1, 135, 136 via ion implantation. Subsequently, the photoresist film 407 is stripped using a stripper solution. As a result, it is possible to obtain a semiconductor layer with an LDD structure having a high-density source region 1d and a high-density drain region 1e having a higher impurity concentration than the low-density source region 1b and the low-density drain region 1c, as shown in FIG. 9(b). Accordingly, the TFT in the pixel image display region and the N-channel TFT in the peripheral driver circuit region have semiconductor layers that have LDD structures.

[0045]

Next, as shown in FIG. 9(c), a 1,500 nm-thick interlayer insulating film 4 composed of SiO_2 is formed on the entire surface of the substrate via PECVD using TEOS and ozone gas as feedstock gases so as to cover the gate electrodes 103, 3a, 131, 134, and the capacitor lines 3b. Subsequently, an activating thermal treatment (activating annealing treatment) is performed at temperature conditions of 400°C in order to activate the impurity ions.

[0046]

Next, as shown in FIG. 9(d), a patterned photoresist film 409 is formed in a shape corresponding to contact holes for connecting the source and drain regions of the TFTs in the peripheral circuit region to data lines and conductive layers to be subsequently formed, contact holes for connecting the source regions of the TFTs in the image display region to data lines to be subsequently formed, contact holes for connecting the drain regions of the TFTs in the image display region to conductive layers to be subsequently formed, contact holes for connecting the source region 135b of the dual-gate TFT to the branching portions 127a to be subsequently formed, a contact hole for connecting the drain region 135c to the ground wire 128 to be subsequently formed, contact holes for connecting the gate electrodes 131 to the rebranching portions 127b to be subsequently formed, contact holes for connecting the source region 136b to the branching portions 127a to be subsequently formed, and a contact hole for connecting the drain region 136c to the branching portion 128a, to be subsequently formed, of the ground wire.

[0047]

As shown in FIG. 10(a), the interlayer insulating film 4 is etched using the photoresist film 409 as a mask to form contact holes 5, 5a, 5b, 130, 132, 133. Subsequently, the photoresist film 409 is stripped to obtain the structure in FIG. 10(b).

[0048]

Next, as shown in FIG. 10(c), an aluminum-titanium multilayer film 410 having a film thickness of 300–1,000 nm is formed via PVD on the interlayer insulating film 4. Furthermore, as

shown in FIG. 10(d), a photoresist film 411 is formed on the aluminum-titanium multilayer film 410 in a shape in which the locations corresponding to the data lines and conductive layers in the switching element region, as well as the wires, ground wire, and external-circuit connection terminal portions in the terminal portion region, have been removed.

[0049]

Next, as shown in FIG. 11(a), the aluminum-titanium film 410 is etched via RIE using a chlorine-based gas and with the photoresist film 411 as a mask, after which the photoresist film 411 is stripped.

[0050]

As a result, data lines 106a, 107a and conductive layers 106b, 107b electrically connected to the source regions 1d, 1g and the drain regions 1e, 1h, respectively, of the semiconductor layers of the N-channel TFT and the P-channel TFT are obtained in the peripheral circuit region, as shown in FIG. 11 (b). In the image display region, the data lines 6 and the conductive layers 6b electrically connected to the source region 1d and the drain region 1e, respectively, of the semiconductor layer are obtained. In the terminal portion region, the ground wire 128 electrically connected to the drain regions 135c of the semiconductor layer of the dual-gate TFT, the branching portions 127a of the wires 127 electrically connected to the source region 135b, the rebranching portions 127b of the wires 127 electrically connected to the gate electrodes 131, the branching portion 128a of the ground wire 128 electrically connected to the drain region 136c, the branching portions 127a of the wires 127 electrically connected to the source region 136b, and the external-circuit connection terminal portions external-circuit connection terminal portions (not shown in the drawings) are obtained.

[0051]

Next, as shown in FIG. 11(c), the interlayer insulating film 7 is formed via PECVD using a mixed gas of TEOS and oxygen gas as a feedstock gas to cover the conductive layers 6b, the data lines 6, the wires 127, and the ground wire 128. Atmospheric-pressure CVD may be used as the film-forming method for the interlayer insulating film 7, and a mixed gas of TEOS and ozone gas or a mixed gas of SiH₄ and oxygen gas may be used as the feedstock gas. In addition, not only an inorganic film, but also an organic film, such as an acrylic film, may be used; in such instances, it is easier to obtain a film having a thick film thickness compared to an inorganic film, and use as a planarization film is thus also possible.

[0052]

Next, as shown in FIG. 12(a), a photoresist film 413 is formed on the interlayer insulating film 7 such that the resist at the locations corresponding to the contact holes connecting the conductive layers 6b and the subsequently formed pixel electrodes is removed. Subsequently, the interlayer insulating film 7 is etched via RIE or wet etching using the photoresist film 413 as a mask, as shown in FIG. 12(b), and the photoresist film 413 is stripped to obtain the interlayer insulating film 7 having the contact holes 8, as shown in FIG. 12(c).

[0053]

Next, as shown in FIG. 13(a), an ITO film 414 having a thickness of approximately 50–200 nm is formed on the interlayer insulating film 7 via sputtering. Subsequently, as shown in FIG. 13(b), a photoresist film 415 corresponding to the pixel electrode shape is

formed on the ITO film 414, and this is used as a mask to perform wet etching of the ITO film 414 using aqua regia or HBr or to perform dry etching via RIE using a gas such as CH₄ or HI, thereby obtaining the pixel electrodes 9a as shown in FIG. 13(c).

[0054]

The TFT array substrate manufactured as described above and the separately formed opposing substrate are oppositely disposed, and liquid crystal is injected between the two substrates to form a liquid-crystal cell. Subsequently, the external-circuit connection terminal portions of the liquid-crystal cell and the external control circuit are connected to obtain a liquid-crystal device. In the present invention, even if static electricity is generated during the liquid-crystal cell formation step and the external control circuit mounting step, the dual-gate TFTs are turned ON, and the current is shunted through the drains of the semiconductor layers; thus, electrostatic breakdown of the switching element disposed in the switching element region can be prevented. In addition, by using a dual-gate structure for the electrostatic-breakdown-preventing circuit, withstand voltage can be increased compared to a single-gate TFT, and breakdown of the electrostatic-breakdown-preventing circuit itself can be prevented.

[0055]

The liquid-crystal device obtained as described above has no electrostatic breakdown of switching elements, and thus has excellent display characteristics.

[0056]

(Second Embodiment)

A second embodiment of the present invention will be described using FIG. 14 and FIG. 15. The present embodiment has a configuration similar to that of the first embodiment, and only the differences therefrom will be described in detail.

[0057]

In the first embodiment, the drain regions of the semiconductor layers of the dual-gate TFTs are collectively connected to a single ground terminal portion via the ground wire, and the ground terminal portion is grounded. In contrast, the structure in the second embodiment differs in that a semiconductor pattern 137 is disposed in the terminal portion region, the drain regions of the semiconductor layers of the dual-gate TFTs 141, 142 are electrically connected to the semiconductor pattern 137 via a ground wire 139, and the semiconductor pattern 137 is grounded. Note that FIG. 15 is a longitudinal cross-sectional view along line D-D' in FIG. 14 and shows the connection structure between the semiconductor pattern 137 and the ground wire 139. The structure will be described in detail below, with descriptions of structures and manufacturing methods identical to those in the first embodiment being omitted.

[0058]

As shown in FIG. 14, the semiconductor pattern 137 in the present embodiment is disposed surrounding the mounting terminals 121–126 and the dual-gate-structure TFTs 141, 142. The semiconductor pattern 137 is formed in the same layer as the semiconductor layers of the dual-gate-structure TFTs 141, 142, and ion implantation is performed upon the semiconductor pattern 137 at the same time as the ion implantation step performed in the steps shown in FIG. 8(d) and FIG. 9(a) of the first embodiment described above. The drain regions of the semiconductor layers of the dual-gate TFTs 141, 142 are electrically connected to the

semiconductor pattern 137 via the ground wire 139. As shown in FIG. 15, the connection structure between the semiconductor pattern 137 and the ground wire 139 is a structure in which the semiconductor pattern 137 is disposed on the glass substrate 60 comprising the base film 12, the gate-insulating film 2 and the interlayer insulating film 4 are disposed on the semiconductor pattern 137, and the semiconductor pattern 137 and the ground wire 139 are electrically connected by a contact hole 138 formed in the gate-insulating film 2 and the interlayer insulating film 4. The ground wire 139 is formed in the same layer as the data lines in the image display region.

[0059]

In the present embodiment, the formation region of the semiconductor pattern can be made as large as possible; thus, the grounded area is wider and, even if high current is generated, the current can be efficiently shunted to the semiconductor pattern, thus making it possible to obtain an electrostatic-breakdown-preventing circuit having higher electrostatic breakdown effects.

[0060]

Note that the dual-gate TFT of the present invention is not limited to the structures described in the embodiments described above. Although the dual-gate TFTs described above are located between the external-circuit connection terminal portions and the peripheral circuit, a structure in which a dual-gate TFT into which signals from the control system circuit and the image signal circuit are inputted is directly connected to the external-circuit connection terminal portion 121, as shown, for example, in FIG. 16, is also acceptable. In FIG. 16, the dual-gate TFT is constituted by a semiconductor layer 142, a gate-insulating film (not shown in the drawing) formed covering the same, and the two gate electrodes 141 disposed on the gate-insulating film. A branching portion 140 branched from the mounting terminal 121 is electrically connected to a source region of the semiconductor layer 142, and the branching portion 140 is further electrically connected to the gate electrodes 141. In addition, a ground wire 143 is electrically connected to a drain region of the semiconductor layer 142. Electrostatic breakdown prevention effects similar to those of the embodiment described above can be obtained with such a structure as well.

[0061]

Although the present embodiments have been described using liquid-crystal devices as the electro-optical device, this is non-limiting, and application to various types of electro-optical devices, such as electroluminescent or plasma displays, is also possible.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an equivalent circuit diagram of TFT elements, wires, and the like provided in a plurality of pixels in a matrix shape constituting an image display region of a liquid-crystal device according to a first embodiment, and an equivalent circuit of an electrostatic-breakdown-preventing circuit.

FIG. 2 is an enlarged plan view of TFT elements, wires, and the like in an image display region of a TFT array substrate in the liquid-crystal device according to the first embodiment.

FIG. 3 is a partial, enlarged plan view of an electrostatic-breakdown-preventing circuit of the TFT array substrate in the liquid-crystal device according to the first embodiment.

FIG. 4 is a longitudinal cross-sectional view along lines A-A', B-B', and C-C' in FIG. 3.

FIG. 5 is a process diagram (part 1) showing a

manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 6 is a process diagram (part 2) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 7 is a process diagram (part 3) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 8 is a process diagram (part 4) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 9 is a process diagram (part 5) showing a manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 10 is a process diagram (part 6) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 11 is a process diagram (part 7) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 12 is a process diagram (part 8) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 13 is a process diagram (part 9) showing the manufacturing process, step-by-step, for the TFT array substrate in the liquid-crystal device of the first embodiment.

FIG. 14 is a partial, enlarged plan view of an electrostatic-breakdown-preventing circuit of a TFT array substrate in a liquid-crystal device according to a second embodiment.

FIG. 15 is a longitudinal cross-sectional view along line D-D' in FIG. 14.

FIG. 16 is a partial, enlarged plan view showing the structure of another electrostatic-breakdown-preventing circuit.

EXPLANATION OF THE REFERENCE NUMBERS

1, 135, 136, 142:	Semiconductor layers
2:	Gate-insulating film
3a, 103, 131, 134:	Gate electrodes
30, 140a, 140b:	TFTs
60:	Substrate
120:	Ground terminal
121, 122, 123, 124, 125, 126:	External-circuit connection terminal portions
127:	Wire
128:	Ground wire
135a, 136a:	Channel regions
135b, 136b:	Source regions
135c, 136b:	Drain regions
137:	Semiconductor pattern
141:	Dual-gate TFT serving as an electrostatic-breakdown-preventing circuit for control system signals or display signals
142:	Dual-gate TFT serving as an electrostatic-breakdown-preventing circuit for power system signals

150: Control system circuit

151: Power circuit

152: Display signal circuit

FIG. 1

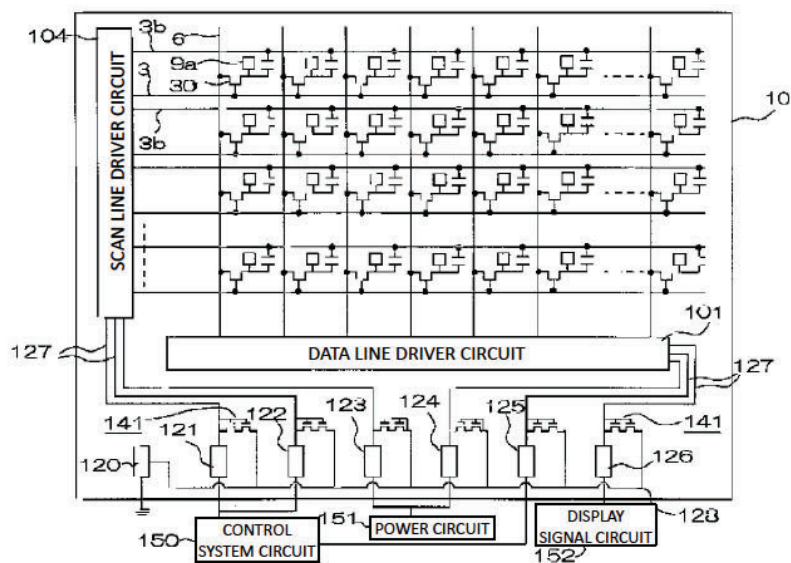


FIG. 16

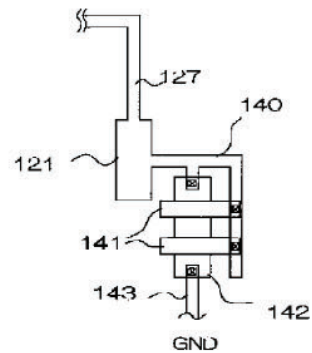


FIG. 2

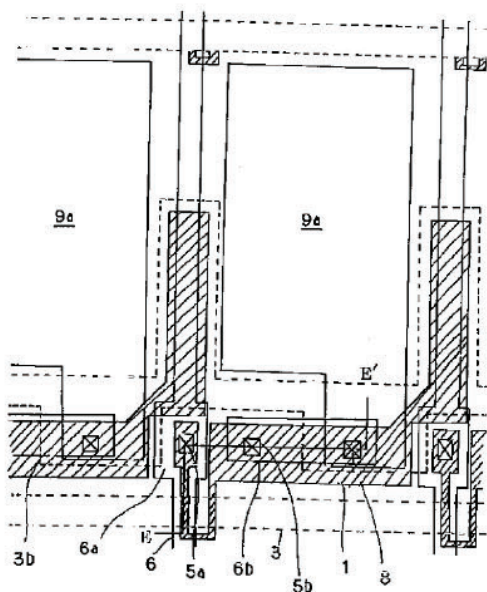


FIG. 4

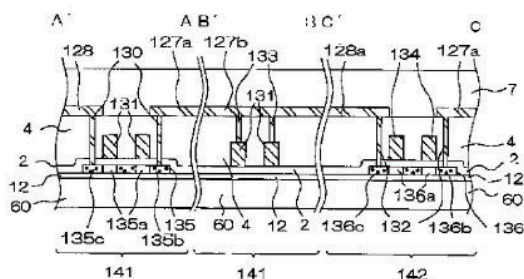


FIG. 15

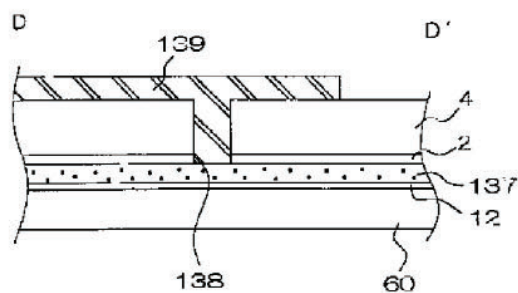


FIG. 3

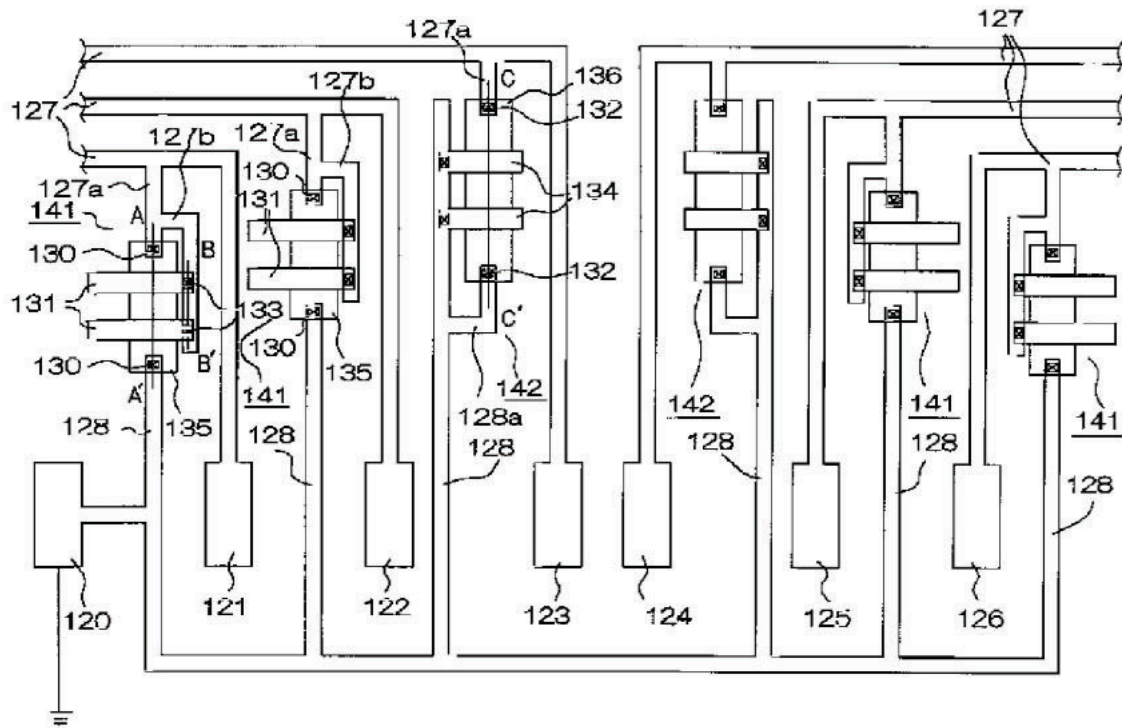


FIG. 5

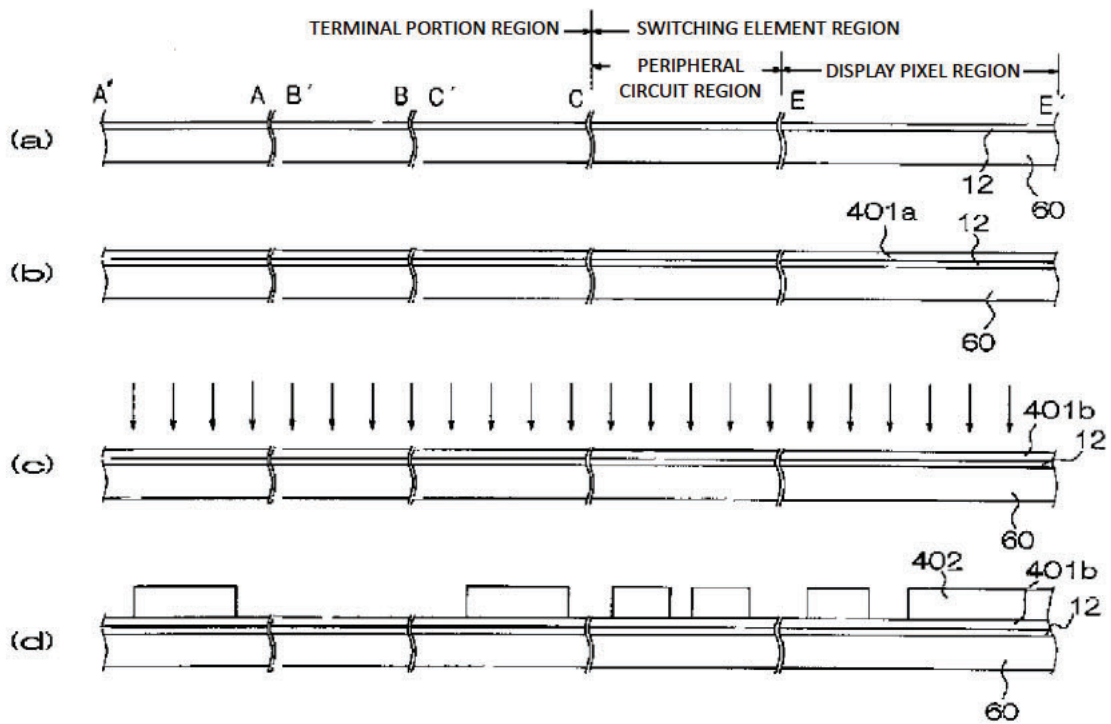


FIG. 6

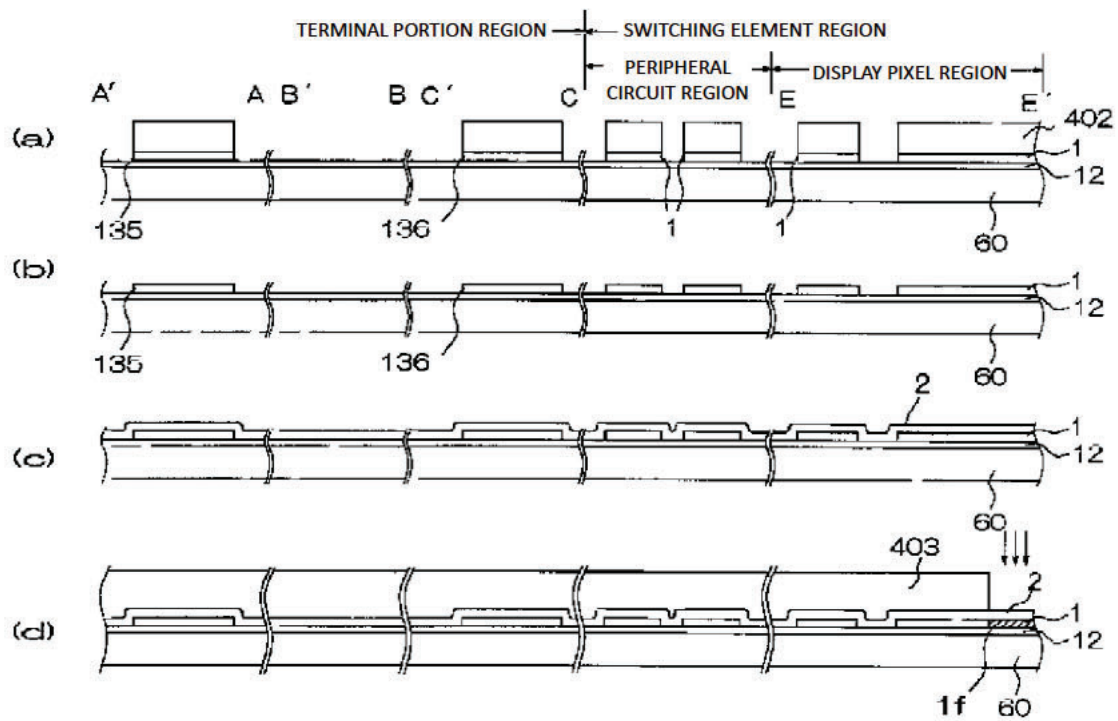


FIG. 7

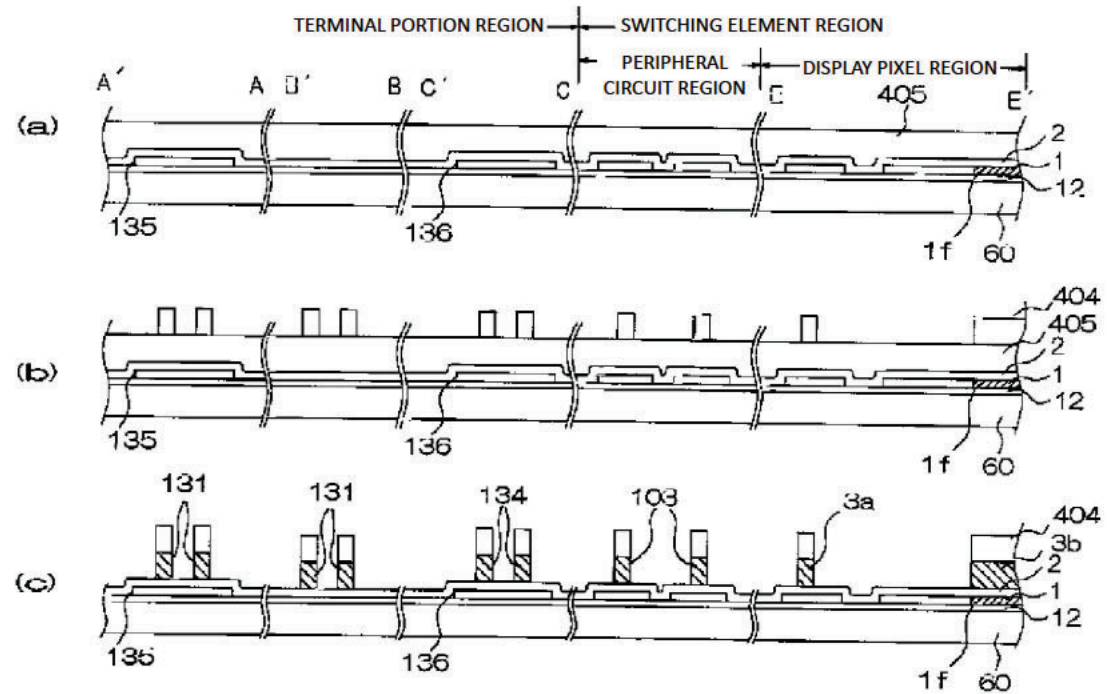


FIG. 8

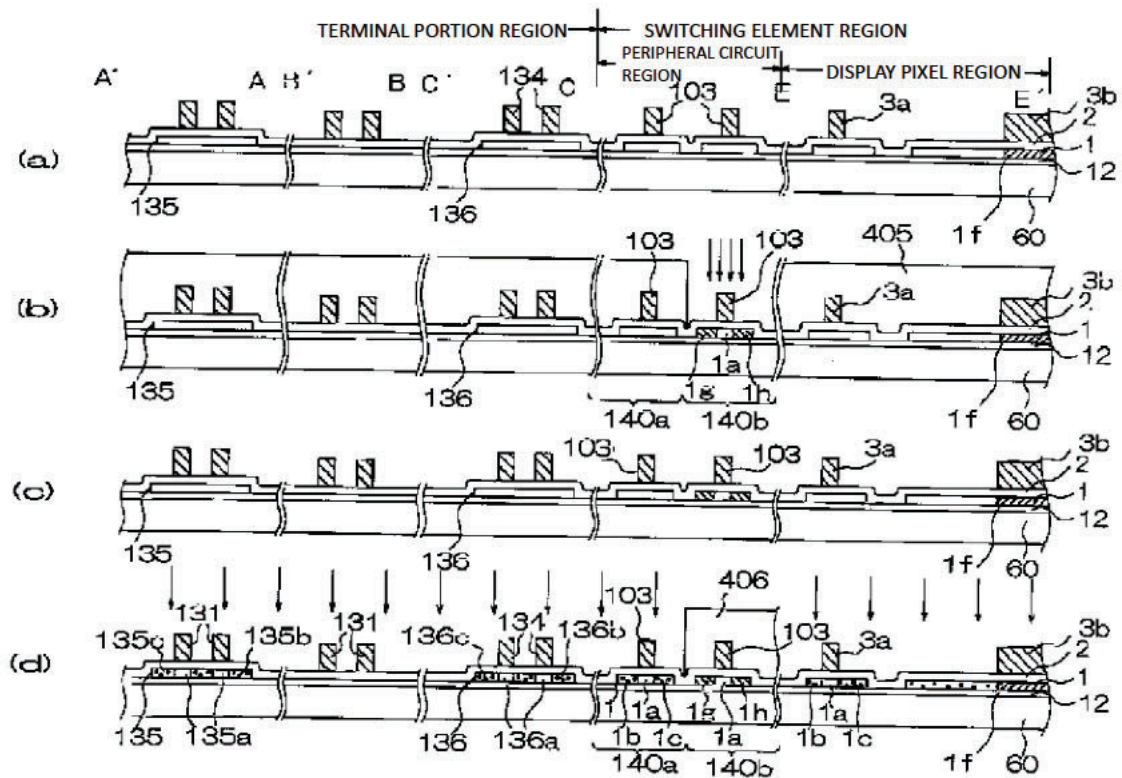


FIG. 9

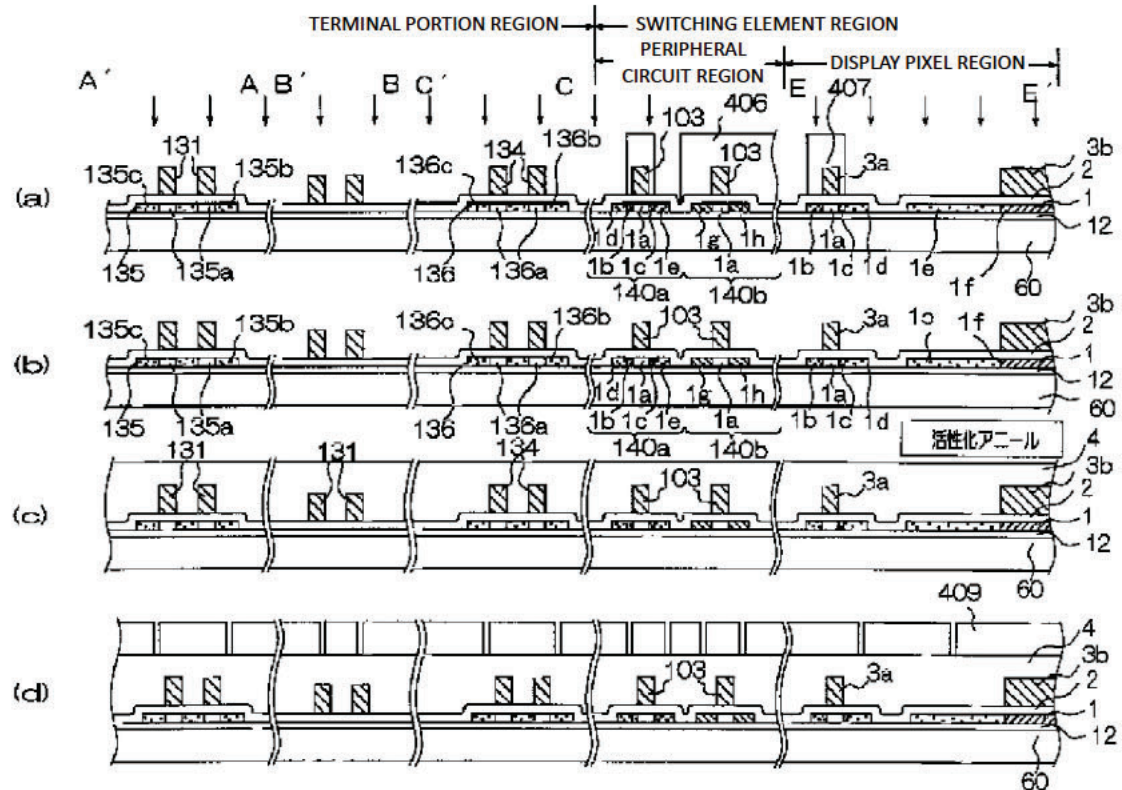


FIG. 10

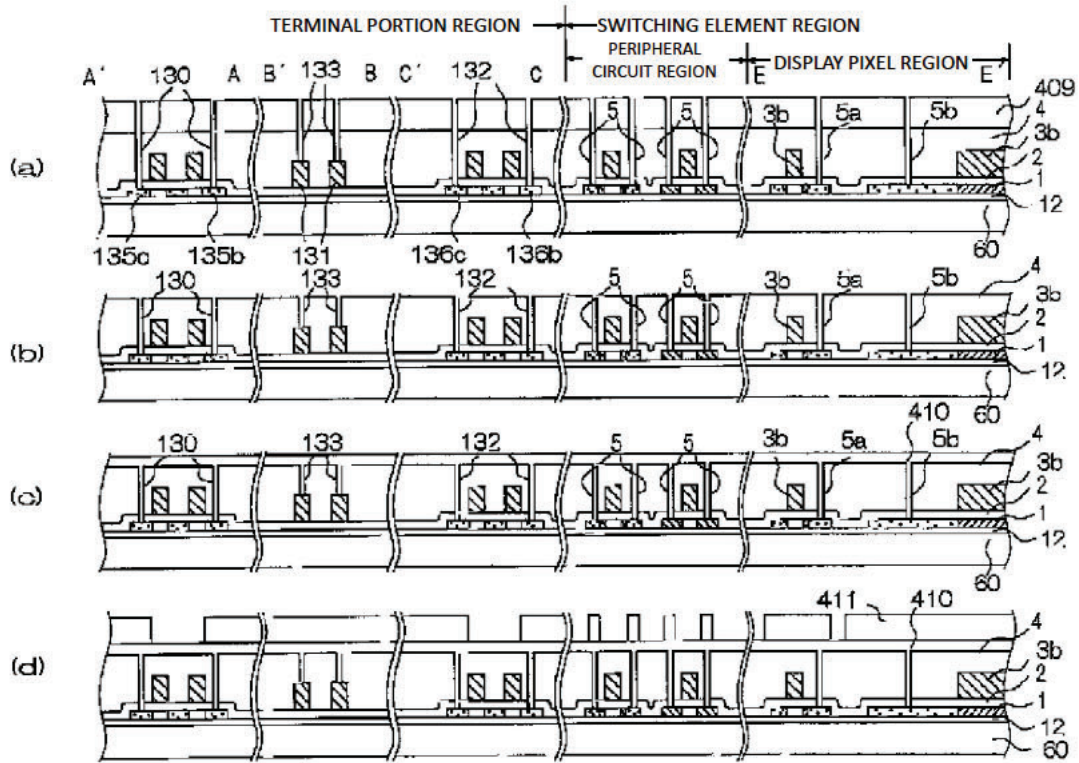


FIG. 11

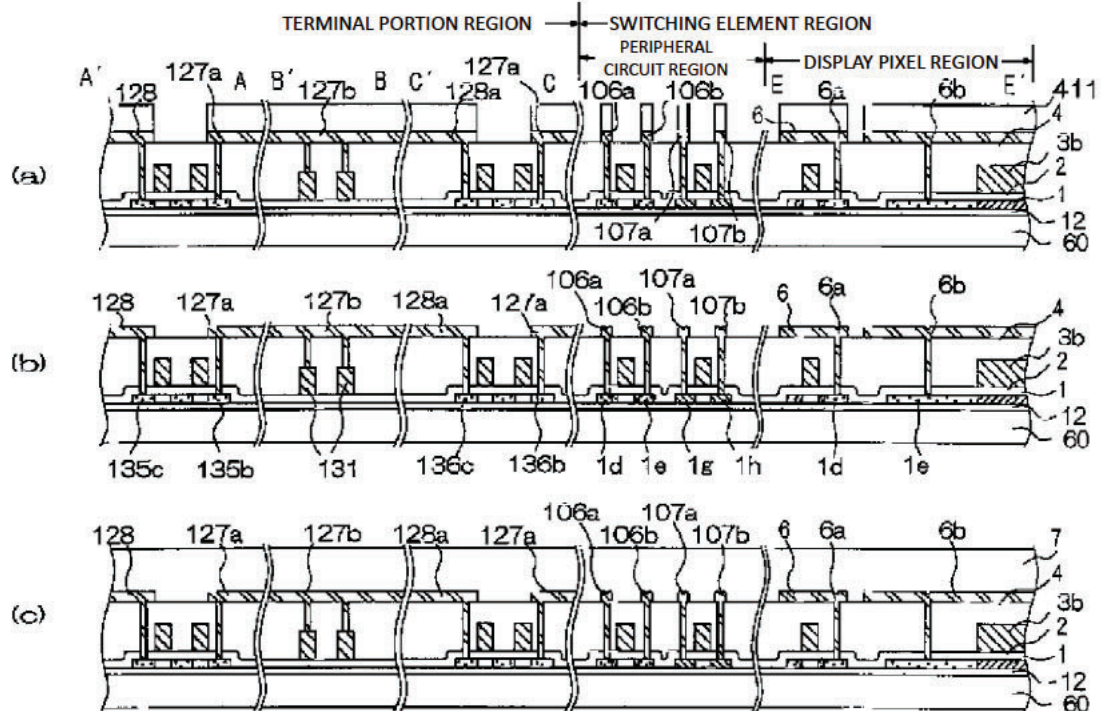


FIG. 12

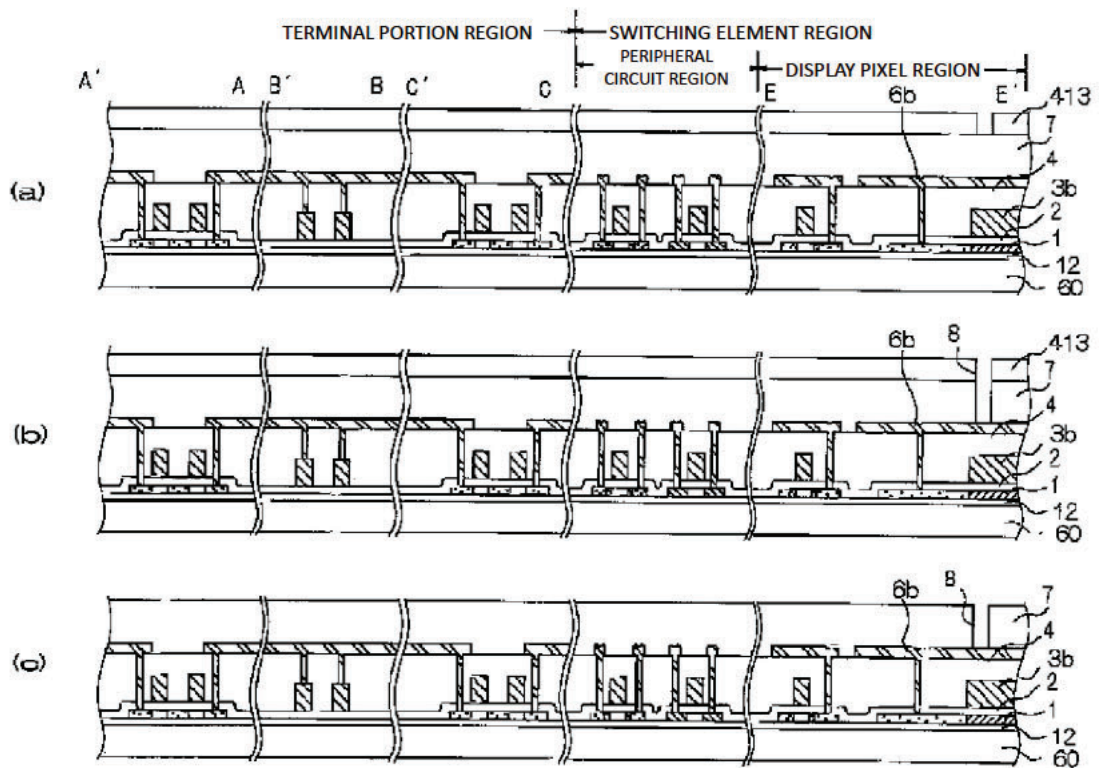


FIG. 13

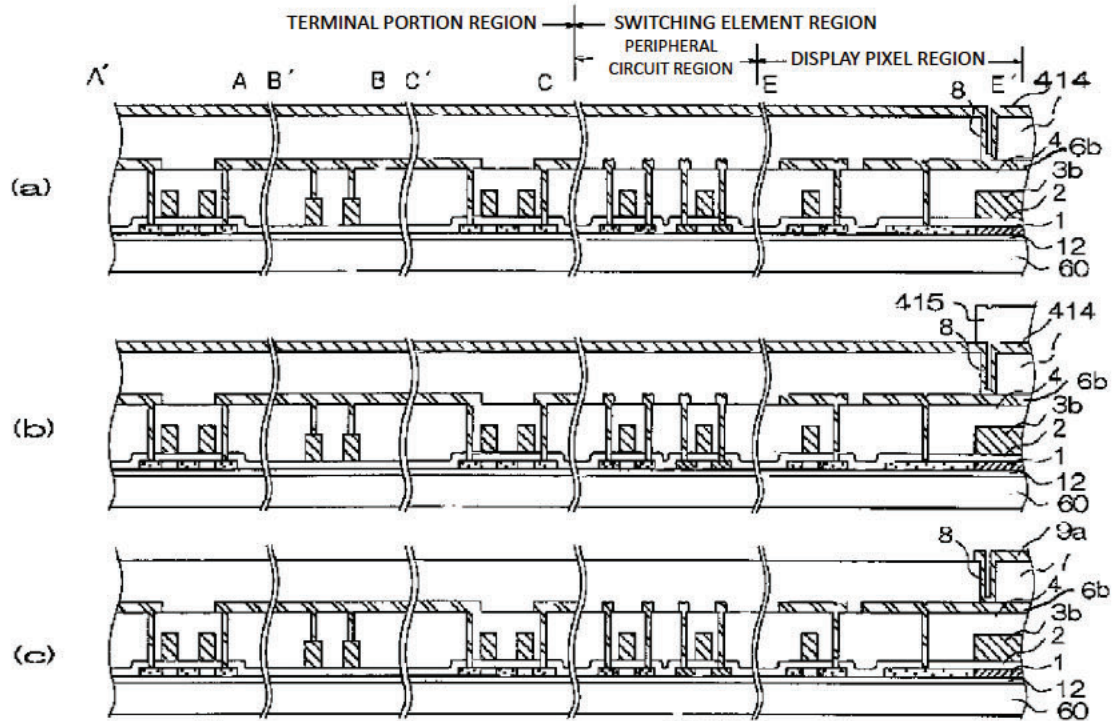
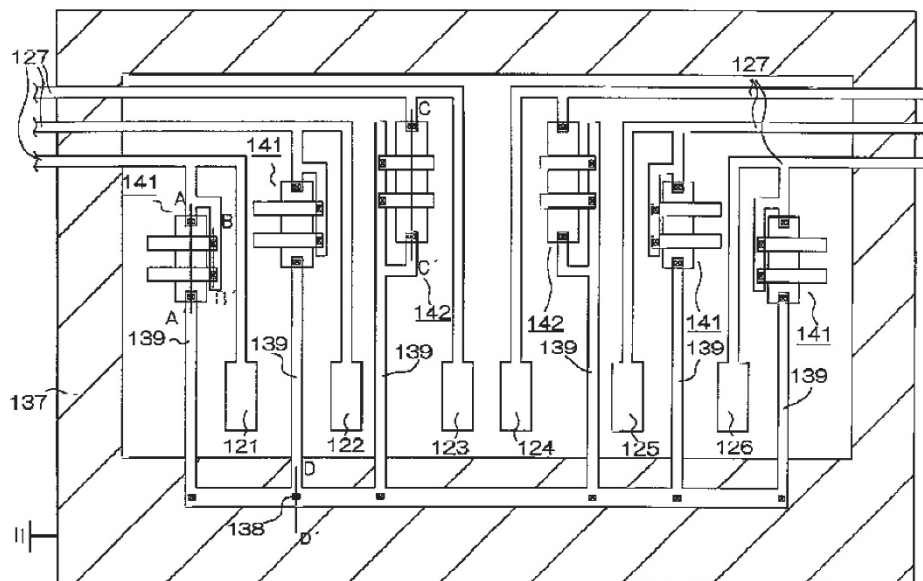


FIG. 14



Continuation of front page

F-term(s) (reference): 2H092 GA59 JA25 JA29 JA38 JA42
JA44 JB13 JB23 JB32 JB33
JB38 JB41 JB58 JB79 KA04
KA07 KA12 MA03 MA08 MA15
MA18 MA19 MA20 MA27 MA30
MA35 MA37 NA14 NA25 NA30
PA06
5C094 AA42 AA43 AA48 BA03 BA43
CA19 DA09 DA13 DB02 DB04
FA01 FA02 FB12 FB14 FB15
GB10
5F110 AA22 BB01 BB02 BB04 CC02
DD02 DD13 EE01 EE03 EE14
EE28 FF02 FF30 GG02 GG13
GG25 GG45 GG47 HJ01 HJ04
HJ13 HL03 HL04 HL11 HM15
NN02 NN04 NN23 NN27 NN35
NN72 PP03 QQ04 QQ05 QQ11