

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2024-00973
U.S. Patent No. 9,184,157

PATENT OWNER'S PRELIMINARY RESPONSE

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IPR2024-00973

U.S. Patent No. 9,184,157

TABLE OF EXHIBITS

Number	Description
2001	Declaration of E. Fred Schubert

I. PRELIMINARY STATEMENT

Pursuant to 37 C.F.R. § 42.107, Patent Owner 138 East LCD Advancements Limited (“138 East” or “Patent Owner”) submits its Preliminary Response to the Petition for *Inter Partes* Review of U.S. Patent No. 9,184,157 (“the ’157 patent”). Paper 1 (“Petition” or “Pet.”). Petitioner BOE Technology Group Co., Ltd., challenges the validity of claims 1-18 of the ’157 patent.

The Petition does not establish a reasonable likelihood that the asserted references render any of claims 1-18 unpatentable. The asserted references, alone or in combination as presented in the Grounds, do not disclose all limitations of any challenged claim. In particular, the Petition fails to show (1) that *Reiner* discloses or renders obvious electrostatic damage (“ESD”) protection circuits connected to a scanning line driving circuit to protect the scanning line driving circuit (Ground 1), and (2) that *Reiner* in view of *Takahara* renders obvious ESD protection circuits connected to a power supply line and a scanning line driving circuit to protect the scanning line driving circuit, or that *Takahara* would motivate a POSITA to modify *Reiner*’s ESD protection network to satisfy the ’157 claim limitations (Ground 2). *Reiner* and *Takahara* provide protection circuit arrangements distinct from those claimed in the ’157 patent: *Reiner* discloses an ESD protection network for a source (data line) driver integrated circuit—not a scanning line driving circuit—and *Takahara* does not disclose protection circuits

connected to power supply lines. The Board therefore should deny institution for failure to present a likelihood that the Petitioner will prevail on any Ground.

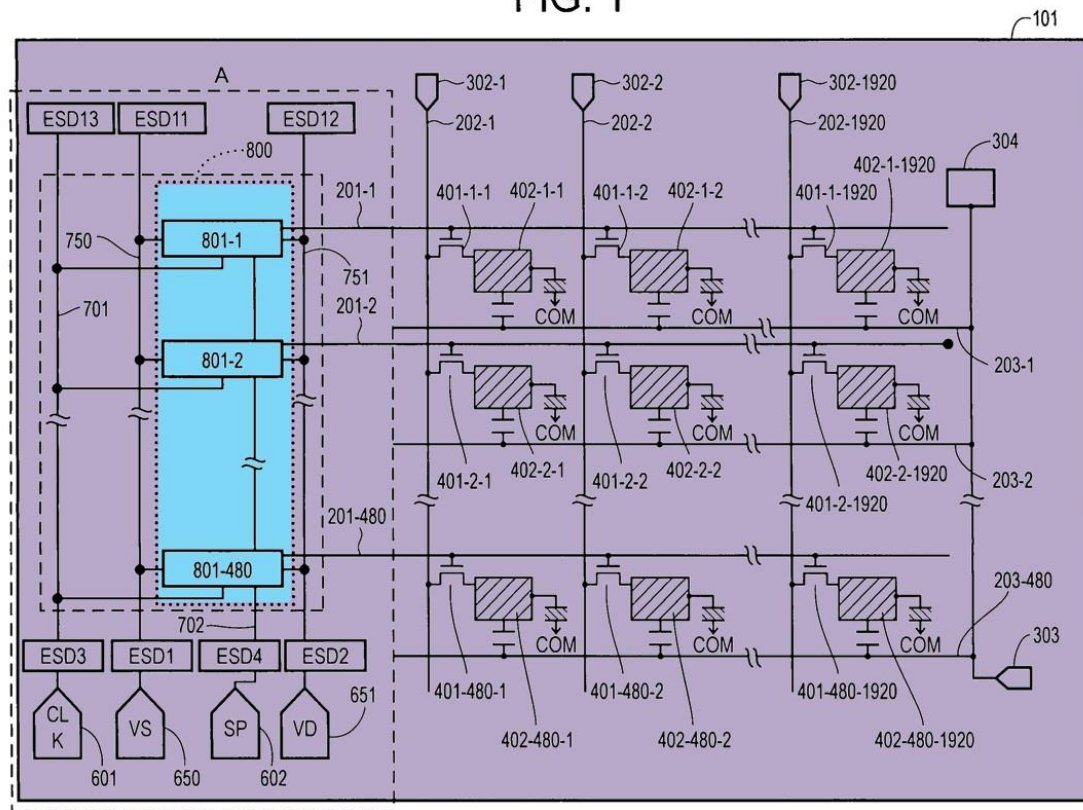
II. THE '157 PATENT

The '157 patent, titled “Semiconductor Device, Display Device, and Electronic Apparatus,” describes a “semiconductor device, display device and electronic apparatus” with improved measures to protect display circuitry from electrostatic damage when a high voltage caused by static electricity or “various noise phenomena” is “unintentionally applied to the inside of the device.” Ex. 1001, 1:10-16.

The '157 patent's improved ESD protection measures are specifically directed to “a display device having a driving circuit provided on an active matrix substrate.” *Id.*, 1:10-13. The driving circuit “in the scope of the claims” is a scanning line driving circuit that is “formed by integrating polysilicon thin film transistors [TFTs] on the active matrix substrate.” *Id.*, 5:20-28. A display device where the driving circuit is formed directly on the active matrix display substrate (“TFT driving circuit”) is different than a display device where the driving circuit is a “general semiconductor device” formed on a silicon wafer. Ex. 2001 ¶34. In a display device with a TFT driving circuit, the driving circuit is formed as part of the active matrix substrate in which the TFTs that control each pixel of, for example, an LCD display are formed.

For example, Figure 1 shows a **scanning line driving circuit 800** formed on the **active matrix substrate 101**, which supplies driving signals to scan lines 201, which are connected to pixel switching elements 401:

FIG. 1

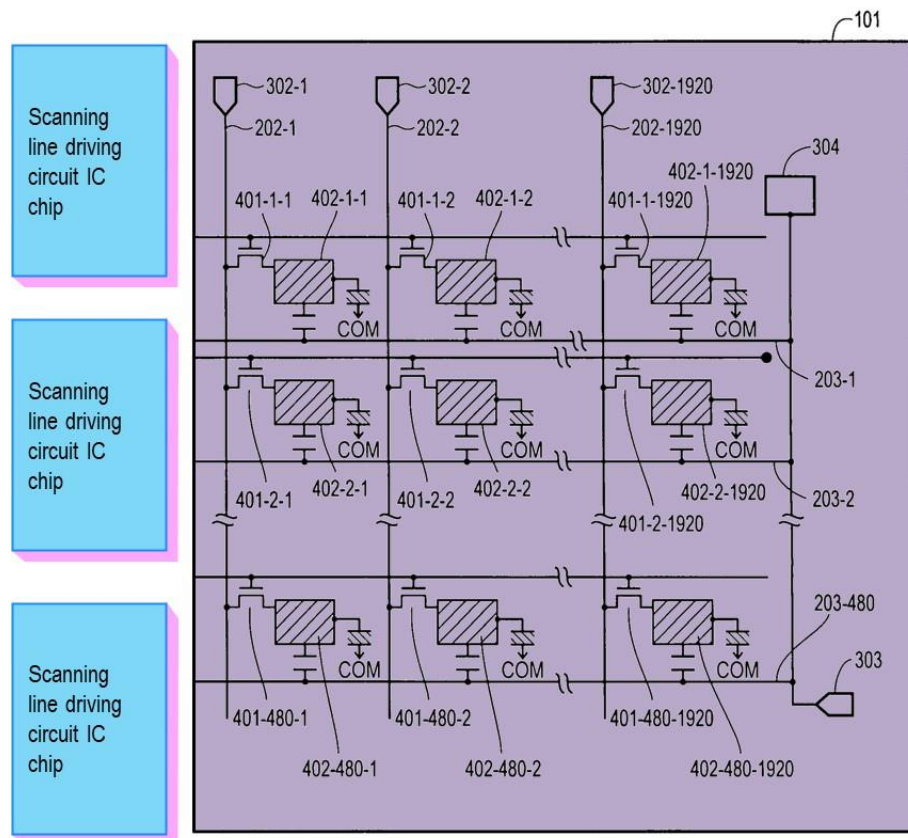


Id., Fig. 1.¹

In a display device where the scanning line driving circuit is not a TFT driving circuit, the scanning line driving circuitry exists in a discrete integrated circuit chip (“IC chip”), or multiple IC chips, and the driving circuitry of each IC chip is formed on a silicon substrate. Ex. 2001 ¶35. In this type of display device,

¹ All colors and colored annotations added to Figures unless otherwise noted.

the silicon substrate of the driving circuit IC chips is different than the display substrate, typically a glass substrate, on which the pixel electrodes and associated transistors (TFTs), and the data and scan lines, are formed. *Id.* The following modified figure based on Figure 1 of the '157 patent shows an example of such a display device with three **scanning line driving circuit IC chips** that are formed on **silicon substrates** separate from the **display substrate** (typically a glass substrate) on which the pixel electrodes and transistors (TFTs), scan and data lines, etc., are formed.



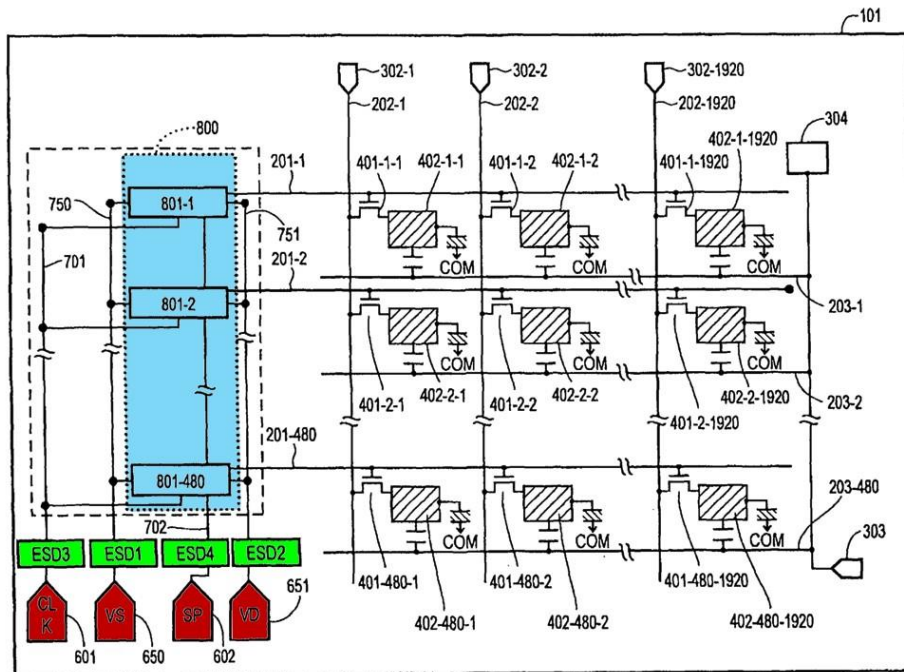
Ex. 2001 ¶35.

Regarding ESD protection, the '157 patent explains that for “general semiconductor devices” formed on a silicon wafer there is “little chance[]” of an ESD event occurring within the IC chip semiconductor device because the silicon wafer is conductive. Ex. 1001, 1:23-28. The “key issue to prevent” ESD events in an IC chip semiconductor device formed on a silicon wafer is therefore to prevent high voltage from entering the device via its input terminals. *Id.* The conventional solution to prevent high voltage from entering the semiconductor device and thus ESD damage inside the device is to place protective circuits between the input terminals and the semiconductor device. *Id.*, 1:28-32.

By contrast, the '157 patent explains that a display device where the active matrix circuitry (e.g., a scanning line TFT driving circuit) is formed directly on the display substrate (typically glass) is subject to different ESD problems because, unlike semiconductor devices formed on silicon (IC chips), the driving circuits are formed on an insulating substrate. *Id.*, 1:33-39. Due to the insulating substrate, ESD damage to the internal circuitry is more likely because static electricity can easily occur during the manufacturing process, and it is more difficult for such charges to escape as compared to a semiconductor device formed on a silicon substrate. *Id.*, 1:33-39, 2:33-35.

The '157 patent explains that existing layouts for protecting display devices with, for example, a scanning line TFT driving circuit, from ESD damage use the

same method used to protect IC chips: “only protective circuits for preventing the static electricity from [entering via] the input terminals are built in” to protect the driving circuit from ESD damage. *Id.*, 1:47-54, 2:20-30. Figure 11 shows the conventional art for protecting a **scanning line driving circuit 800**, comprising **protection circuits ESD1 to ESD4** placed between the **input terminals 601, 602, 650, and 651** and the **scanning line driving circuit 800** to protect the scanning line driving circuit from static charges entering via the input terminals:



Id., Fig. 11.

The '157 patent explains that because the driving circuit is formed on an insulating substrate, “it is difficult for charges to escape as compared to the circuit on [a] silicon wafer, and it is easy to be electrified.” *Id.*, 2:33-50. Furthermore,

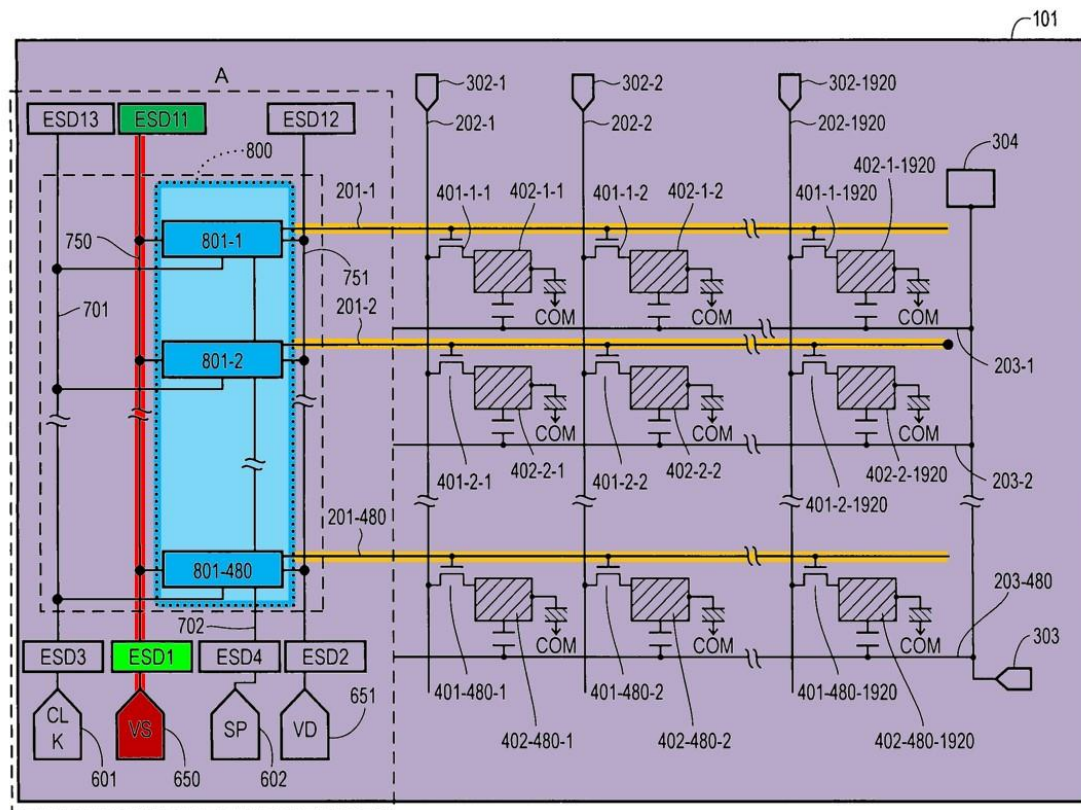
because “the area of [a TFT driving circuit] is larger as compared to the IC formed on a general silicon wafer,” the ESD protection circuits located after the input terminals are insufficient to protect the driving circuitry located far from the input terminals from ESD events, particularly during the manufacturing process. *Id.*

Specifically, “since there is a possibility that the static electricity is electrified on a certain location on the substrate during the manufacturing process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation.” *Id.*; *see also id.*, 3:67-4:13 (“when an active matrix used in a TFT-LCD or TFT-OLED and a driving circuit thereof are formed on the insulating substrate, the driving circuit is configured to surround the active matrix, so that it becomes larger and accordingly its line is also lengthened”).

To address these problems, the ’157 patent discloses and claims placing ESD protection circuits on both ends of the scanning line driving circuit. ESD protection circuits ESD1 to ESD4 are disposed between input terminals and the scanning line driving circuit, to protect the scanning line driving circuit from charges entering via the input terminals. And ESD protection circuits ESD11 to

ESD13 are disposed at the far end of the opposite side of the scanning line driving circuit relative to the input terminals. *Id.*, 5:44-6:2.

For example, as shown below for protecting the scanning line driving circuit 800 from charges entering via the low potential power source line 750, the **scanning line driving circuit 800** composed of **driving unit circuits 801** is formed on the **active matrix substrate 101** and the **driving unit circuits 801** are connected to **scan lines 201** to supply a driving signal. The pixel switching elements 401 are connected to the **scan lines 201** and data lines 202. The **low potential power source line 750** is connected to the **scanning line driving circuit 800** and the **low potential power source terminal 650**. A **first protection circuit ESD1** is connected between the **low potential power source terminal 650** and the **low potential power source line 750**, and a **second protection circuit ESD11** connected to the **low potential power source line 750** is “disposed at the far end of the opposite side” from the **input terminal 650** “with the **scanning line driving circuit 800** therebetween”:



Id., Fig. 1; 4:60-5:65.

The '157 patent explains that ESD1 prevents the scanning line driving circuit 800 from being damaged when excess charges are input from the low potential power supply terminal 650. *Id.*, 5:51-54. And ESD11 prevents static charges generated “during the manufacturing [of] the active matrix substrate” from entering the scanning line driving circuit 800 via the opposite end of the low potential power supply line 750 with respect to its supply terminal 650 and damaging portions of the scanning line driving circuit “located far from a terminal.” *Id.*, 5:61-65.

Independent claims 4 and 17, for example, recite this improved ESD protection scheme:

4. A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Id., 12:25-47.

17. A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

Id., 14:16-43.

The '157 patent explains that placing the scanning line driving circuit between protection circuits in this manner confers an additional benefit because the protective circuits on either side of the scanning line driving circuit may be

“arranged at corners far from the input terminals among four corners of the active matrix” which makes it “possible to arrange large-sized protective circuits without making the peripheral area [of the active matrix substrate—i.e., the portion of the substrate that does not include pixels] large.” *Id.*, 4:14-19. In particular, arranging the second set of protective circuits “at the corner part of the active matrix substrate, particularly at the corner opposite to the input terminals” enables the scanning line driving circuit to be protected without “making the substrate area larger.” *Id.*, 5:65-6:2.

Dependent claim 8, for example, recites this improved ESD protection scheme:

8. The display device as set forth in claim 4, further comprising:
a substrate,
the scanning line driving circuit being arranged on the
substrate,
the power supply line being formed over first and second
corner portions of the substrate so as to follow a
periphery of the substrate,
the first protection circuit being arranged in the first corner
portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

Id., 12:58-13:2.

III. CLAIM CONSTRUCTION

For purposes of this Preliminary Response, Patent Owner contends that the claims should be given their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art. 37 C.F.R. § 100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

IV. LEGAL STANDARD

The Board may not institute an *inter partes* review unless the Petition demonstrates a reasonable likelihood that the petition would prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

V. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Preliminary Response only, Patent Owner does not dispute the level of skill for a person of ordinary skill in the art (“POSITA”), set forth in the Petition. Pet., 15-16. The level of skill in the art does not affect whether to deny institution, because the Petition and Petitioner’s expert do not address certain claim limitations of the ’157 patent and disclosures from the asserted prior art references. Patent Owner does not waive, however, any argument regarding the proper level of skill and reserves the right to later advance additional arguments.

**VI. THE PETITION DOES NOT ESTABLISH A REASONABLE
LIKELIHOOD THAT THE ASSERTED REFERENCES RENDER
UNPATENTABLE ANY CHALLENGED CLAIM.**

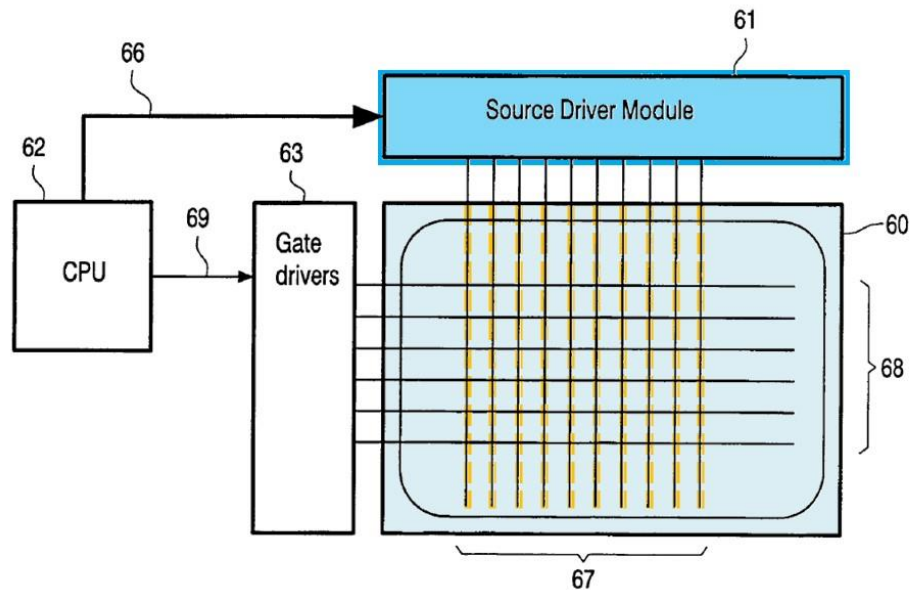
**A. The Petition does not establish a reasonable likelihood that *Reiner*
renders obvious claims 1-18 (Ground 1).**

1. *Reiner*: Overview

Reiner relates to “integrated circuit devices” and, in particular, forming “bump bridges” that provide low-ohmic interconnections within an integrated circuit device. Ex. 1005, 2:1-3. *Reiner* addresses a different problem than the ’157 patent.

Relevant here, *Reiner* discloses an “integrated circuit display driver” to “drive many lines of an LCD display.” *Id.*, 9:11-22. *Reiner* Figure 4 shows a schematic block diagram including an LCD display 60 and external integrated circuit display drivers: LCD screen 60, a source driver 61 to drive a plurality of source (i.e., data) lines 67, gate drivers 63 to drive a plurality of gate (i.e., scan) lines 68, and CPU 62 that provides video signals to the source driver 61 via bus 66 and row timing signals to gate driver 63 via bus 69:²

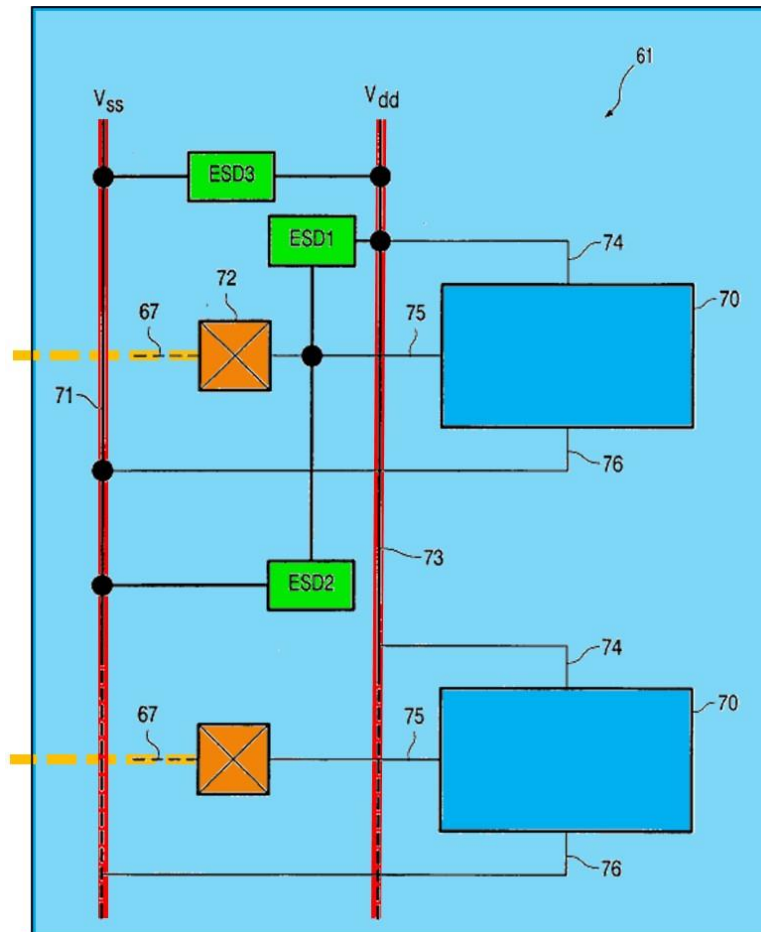
² A POSITA would understand that “source” lines and “data” lines refer to the same lines, and “gate” lines and “scan” lines refer to the same lines. The respective terms are interchangeable. Ex. 2001 ¶48, n. 2.



Id., Fig. 4, 9:23-35.

Reiner describes, and Figure 5 shows, “ESD protection means” “integrated into” source driver 61. *Id.*, 9:21-22. *Reiner*’s **source driver 61** includes “an array of parallel **output devices 70**,” which “drive the **source lines 67** with the voltages needed by each pixel of the LCD screen 60.” *Id.*, 10:1-24. Each output device 70 includes an output 75, which is connected to a **source line 67** via a **contact pad 72**. *Id.* (source lines 67 connected to contact pad “by means of bonding”). A **power supply line 73** provides the supply voltage V_{dd} to the **output devices 70** via connection 74, and a second **power supply line 71** provides the supply voltage V_{ss} to the **output devices 70** via connection 76. *Id.* Three ESD devices, **ESD1**, **ESD2**, and **ESD3**, “are provided for each **output device 70** . . . to protect the circuitry inside the **devices 70**.” *Id.* **ESD1** is connected between the output line 75 and the

power supply line 73 (V_{dd}), **ESD2** is connected between the output line 75 and the **power supply line 71** (V_{ss}), and **ESD3** is situated between the two **power supply lines 71** and **73**. *Id.*



Id., Fig. 5.

Reiner therefore discloses “ESD protection means” inside a source driver integrated circuit, to protect the circuitry within output devices 70. *Id.*, 10:10-12. Specifically, the ESD devices protect against electrical charges that may enter the output device via contact pads 72. *Reiner* explains that IC chips, like source driver

61, often comprise ESD protection “in order to prevent the very sensitive circuits on the chip from being destroyed when it is subject to a discharge event. This might happen for example when somebody induces a voltage peak in the circuitry by touching the pins of the chip.” *Id.*, 3:2-3. *Reiner* further explains that ESD protection networks within IC chips, like source driver 61, “comprise[] protection diodes and/or transistors and metal interconnection lines for connecting these diodes and/or transistors with **inputs and/or outputs of the integrated circuit device to be protected.**” *Id.*, 3:4-8 (emphasis added). In short, *Reiner* describes an ESD protection network inside an integrated circuit for protecting the IC chip’s internal circuits from electrical charges that could enter the IC chip through its input and/or output terminals.

In *Reiner*’s source driver 61, the ESD protection network protects the individual outputs 70 from electrical charges that could enter the IC chip through its contact pads or pins. *Reiner* does not disclose input pins on the source driver 61 IC chip. *Id.*, 9:11-10:23. *Reiner* discloses only contact pads 72, for connecting the source driver’s outputs 75 to the source lines on the LCD display 60. *Id.*, 10:4. Figure 5 shows no other inputs/outputs. *Id.*; see also Ex. 2001 ¶51.

2. The Petition fails to show that *Reiner* discloses or renders obvious all limitations of any challenged claim.

a. Claim 4³

i. The Petition does not show that *Reiner* discloses or renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed (claims 4[d], 4[e] and 4[f]).

The Petition fails to show that *Reiner* discloses “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged as claimed. Ex. 1001, claim 4[d-f]. The Petition cites no evidence that shows that *Reiner* discloses protection circuits connected to a scanning line driving circuit. *Reiner* discloses, and the Petition cites, only an ESD protection network within a source (data line) driver IC chip. And the Petition fails to show that *Reiner* discloses or renders obvious applying *Reiner*’s source driver ESD protection network to a gate driver. See claim 4[d-f]. Because claim 4 recites a particular protection circuit layout, and because the Petition relies on *Reiner*’s precise source driver ESD protection network, it is not enough to argue that *Reiner* renders obvious providing general ESD protection for a gate driver. The Petition has not met its burden.

³ Claims 4-18 are addressed before claims 1-3 to follow the order in which the Petition presents Ground 1.

Reiner discloses a particular ESD protection network for only a source driver. *Reiner* discloses no ESD protection circuits for a scanning line driving circuit. *Reiner* discloses “[a] source driver module 61” that drives “the individual source lines 67” of an LCD display 60 and “[a] gate driver 63 . . . that usually drives one whole gate line 68.” Ex. 1005, 9:23-34. *Reiner*’s Figure 5 shows a “schematic block diagram of a display driver 61” including “details of display driver 61 in accordance with” *Reiner*’s invention, including ESD devices. *Id.*, 9:23, 10:1-24 (describing the configuration and operation of source driver 61 shown in Figure 5). But unlike source driver 61, *Reiner* does not disclose a gate driver including an ESD protection network. In fact, *Reiner* discloses few gate driver details, except that a gate driver “usually drives one whole gate line” and that CPU 62 provides “row timing signals (control signals) via a bus 69 to the gate driver 63.” *Id.*, 9:27-31. *Reiner* does not disclose protection circuits connected to a gate (scan line) driver.

And the Petition cites no evidence to support its argument that a “POSITA would have understood that source driver 61 in Figure 5 is exemplary and that it applies equally to gate driver 63 (scanning line driving circuit) because gate driver 63 is also a ‘driver display circuit.’” Pet., 25. Instead, the Petition quotes *Reiner* out of context. *Reiner* suggests that its bump bridge teachings are “well suited” for integrated circuits generally, but the Petition mischaracterizes those teachings to

suggest that *Reiner* teaches ESD protection “well suited” for all integrated circuits.

That teaching simply does not exist. See Pet., 24; Ex. 1005, 8:1-11, 12:23-25.

Nothing in *Reiner* suggests that its gate drivers 63 include an ESD protection network. More to the point, no evidence shows that the gate driver would include an ESD protection network identical to the source driver’s network and include the same number of ESD devices connected in the same way. The Petition offers no evidence that *Reiner* teaches that Figure 5’s ESD protection network applies to a gate line driver.

The Petition does not show that *Reiner* renders obvious protection circuits connected to a scanning line driving circuit and arranged as claimed, either. The Petition argues only that a gate driver would benefit from ESD protection *in general* and that a POSITA would have been motivated to protect “gate driver 63 in the same way as source driver 61 to prevent the sensitive circuits from being damaged by ESD events.” Pet., 30. The Petition argues that a POSITA would want to protect “each output device 70,” but the Petition does not cite evidence showing that (1) the gate drivers comprise output devices 70, or (2) the gate driver is arranged like the source driver, to accommodate the same ESD layout. Indeed, the Petition ignores *Reiner*’s disclosure that the gate driver integrated circuit comprises individual gate drivers, not output devices 70. Ex. 1005, 9:20-9:31. And the

Petition's argument that the gate driver integrated circuit and the source driver integrated circuit would "have similar configurations" is conclusory. Pet., 31-32.

To the contrary, a POSITA would expect to see differences between the gate driver arrangement and the source driver arrangement. Ex. 2001 ¶58. For example, a POSITA would understand that individual gate/scan line drivers are coupled to one another, to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time. This coupling between individual gate/scan unit drivers is not, however, required for source/data unit drivers because each individual source/data driver transmits image data signals simultaneously to each vertical column of a display. Ex. 2001, ¶58.

In short, *Reiner* does not disclose or suggest that source driver 61's internal ESD layout would, or even could, apply to a gate driver. Indeed, a POSITA would understand that a source driver and a gate driver would have different layouts. Ex. 2001 ¶58-59.

Thus, the Petition fails to show that *Reiner* discloses or renders obvious "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit" and arranged with respect to the scanning line driving circuit and power supply line as claimed in 4[e] and 4[f].

- ii. **The Petition does not show that *Reiner* discloses or renders obvious "an input terminal connected to the power supply line" and**

protection circuits and a scanning line driving circuit arranged relative to that input terminal, as claimed (claims 4[c], 4[e], 4[f]).

The Petition fails to show that *Reiner* discloses or renders obvious a display device including “an input terminal connected to the power supply line,” and, thus, it does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal. Ex. 1001, claim 4[c], 4[e-f].

The Petition concedes that *Reiner* is silent regarding input terminals for power lines 71 (Vss) and 73 (Vdd) of source driver 61 generally, and regarding where input terminals for a display device would be located. Pet., 21; Ex. 1005, 9:11-10:23 (disclosing only output contact pads 72 for connecting source driver 61’s outputs 75 to the source lines on the LCD display 60), Figs. 4-5. But the Petition cites no evidence to support its conclusion that a POSITA would have recognized that the input terminals would have been placed in a specific location, namely, “above the first ESD3” in *Reiner* Figure 5. Pet., 22; Ex. 2001 ¶62.

The Petition’s assertion that merely providing input terminals for power supply lines would have been obvious in view of conventional art described in the ’157 patent is irrelevant. *Id.* The relevant question, for which the Petition cites no evidence, is whether *Reiner* discloses or renders obvious a particular location for input terminals of the display device. It does not. Thus, the Petition fails to offer evidence to show that *Reiner* discloses or renders obvious protection circuits and a

scanning line driving circuit arranged relative to that input terminal. Ex. 1001, claim 4[c], 4[e-f]; Ex. 2001 ¶63. Accordingly, the Petition fails to show that *Reiner* suggests or renders obvious “an input terminal connected to the power supply line to supply power,” and, thus, it does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal. *Id.*

b. Claim 5

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 4 and, thus, fails to show that *Reiner* renders obvious claim 5.

c. Claim 6

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 4 and, thus, fails to show that *Reiner* renders obvious claim 6.

d. Claim 7

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 4 and, thus, fails to show that *Reiner* renders obvious claim 7.

e. Claim 8

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 4 and, thus, fails to show that *Reiner* renders obvious the additional limitations of claim 8.

f. Claim 9

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 4 and, thus, fails to show that *Reiner* renders obvious claim 9.

g. Claim 10

The Petition fails to show that *Reiner* discloses or renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged as claimed. See §VI.A.2.a.i, *supra*; claim 10[d-f]. And the Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line,” and therefore does not disclose or render obvious protection circuits and a circuit element arranged relative to that input terminal as claimed. See §VI.A.2.a.ii, *supra*; claim 10[c], [e-f]. Therefore, the Petition fails to show that *Reiner* renders obvious claim 10.

h. Claim 11

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 10 and, thus, fails to show that *Reiner* renders obvious claim 11.

i. Claim 12

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 10 and, thus, fails to show that *Reiner* renders obvious claim 12.

j. Claim 13

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 10 and, thus, fails to show that *Reiner* renders obvious claim 13.

k. Claim 14

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 10 and, thus, fails to show that *Reiner* renders obvious claim 14.

l. Claim 15

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 10 and, thus, fails to show that *Reiner* renders obvious claim 15.

m. Claim 16

The Petition fails to show that *Reiner* discloses or renders obvious “the first protection circuit and a second protection circuit are connected to the scanning line driving circuit” and arranged as claimed. *See* §VI.A.2.a.i, *supra*; claim 16[d-f]. And the Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line,” and therefore does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal as claimed. *See* §VI.A.2.a.ii, *supra*; claim 16[c], [e-f]. Therefore, the Petition fails to show that *Reiner* renders obvious claim 16.

n. Claim 17

The Petition fails to show that *Reiner* discloses or renders obvious “the first protection circuit and a second protection circuit are connected to the scanning line driving circuit” and arranged as claimed. See §VI.A.2.a.i, *supra*; claim 17[d-f].

And the Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line,” and therefore does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal as claimed. See §VI.A.2.a.ii, *supra*; claim 17[c], [e-f]. Therefore, the Petition fails to show that *Reiner* renders obvious claim 17.

o. Claim 18

The Petition fails to show that *Reiner* discloses or renders obvious “the first protection circuit and a second protection circuit are connected to the scanning line driving circuit” and arranged as claimed. See §VI.A.2.a.i, *supra*; claim 18[d-f].

And the Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line,” and therefore does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal as claimed. See §VI.A.2.a.ii, *supra*; claim 18[c], [e-f]. Therefore, the Petition fails to show that *Reiner* renders obvious claim 18.

p. Claim 1

The Petition fails to show that *Reiner* discloses or renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged as claimed. See §VI.A.2.a.i, *supra*; claim 1[d], [g-h]. And the Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line,” and therefore does not disclose or render obvious protection circuits and a scanning line driving circuit arranged relative to that input terminal as claimed. See §VI.A.2.a.ii, *supra*; claim 1[c], [g-h]. Therefore, the Petition fails to show that *Reiner* renders obvious claim 1.

q. Claim 2

The Petition fails to show that *Reiner* renders obvious the display device as set forth in 1 and, thus, fails to show that *Reiner* renders obvious claim 2.

r. Claim 3

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 1 and, thus, fails to show that *Reiner* renders obvious claim 3.

B. The Petition does not establish a reasonable likelihood that *Reiner* in view of *Takahara* renders obvious claims 1-18 (Ground 2).

The Petition does not show that *Reiner* renders obvious claims 1-18. *Reiner* discloses a source (data line) driver integrated circuit including an internal ESD protection network, separate from an LCD display. Thus, the Petition does not show that *Reiner* renders obvious a display device that includes a scanning line

driving circuit and first and second protection circuits connected to that scanning line driving circuit.

Takahara does disclose a display device that includes a scanning line driving circuit. But the Petition does not show that either reference, or the combination that the Petition proposes, discloses or renders obvious a scanning line driving circuit connected to protection circuits, which are also connected to a power supply line. Though *Takahara*'s protection circuits protect the scanning line driving circuit, they are not connected to a power supply line. The Petition ignores *Takahara*'s express disclosures directed to *signal* lines, not *power* lines. The arrangements remain distinct from the claimed inventions.

1. *Takahara*: Overview

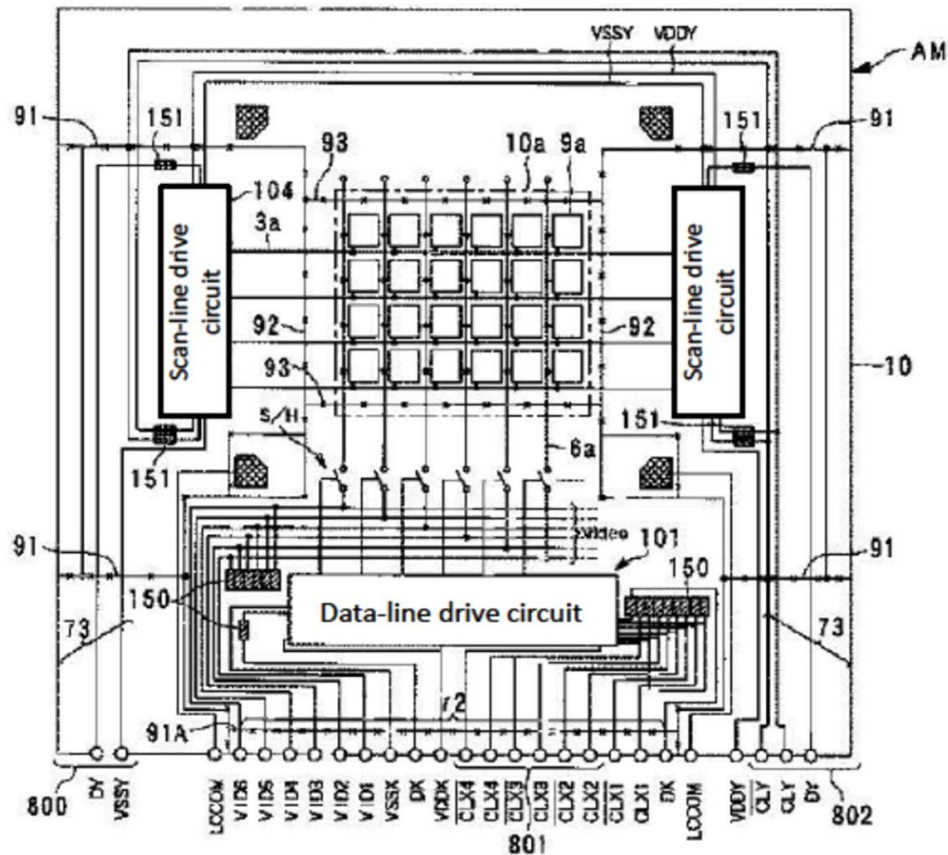
Takahara relates to methods for manufacturing an electro-optical device, such as an LCD device, that employs an “element-substrate device, such as an active-matrix-substrate device” that is formed on an insulating material such as glass. Ex. 1007, [0001], [0003].

Takahara addresses a different problem than the '157 patent. *Takahara* is directed to methods to form and cut short-circuit wirings to help diffuse static charges that build up on the substrate during manufacturing to the outer perimeter of the substrate, to protect the electro-optical device. *Id.*, [0003]-[0004], [0007]-[0011], [0015]. The short-circuit wirings are formed at an early stage of

manufacturing—when the scan lines and gate electrodes are formed on the insulating substrate—before the device is operational, and then cut prior to completing the manufacturing process to allow normal operation of the electro-optical device. *Id.*, [0004]-[0005], [0008], [0068], [0070]. The short-circuit wirings electrically connect (1) the scan line wirings, (2) the data line wirings, and (3) the signal wirings that supply a signal for driving scan line and data line driving circuits. *Id.*, [0004], [0012], [0020]-[0021] (describing connecting scan lines to short-circuit wiring), [0022]-[0023] (describing connecting data lines to short-circuit wiring), [0024] (describing connecting signal lines to short-circuit wiring). The short-circuit wirings prevent electrostatic breakdown of the thin-film transistors to which the scan and data lines are connected, and the thin-film transistors in the scan and data line driving circuits. *Id.*, [0012], [0020]-[0025].

Relevant here, *Takahara* discloses an active matrix substrate for an LCD device that includes data and scan line driving circuits. *Id.*, [0059]. *Takahara* discloses scan line driving circuits 104 that are arranged along both sides of the image display region 10a and driven by signal wirings DY (start signal), CLY (clock signal), and CLY bar (inverted clock signal), and connected to power supply lines VDDY and VSSY. *Id.*, [0062]-[0065]. *Takahara* discloses electrostatic protection circuits 150 and 151 that are formed at intermediate locations of the signal wirings (in Fig. 1, on lines CLY, DY, CLX, DX, and VID) to prevent static

electricity from entering the scan line driving circuits via the signal wirings. *Id.*, [0066].



Id., Fig. 1.

Important, *Takahara* does not disclose protection circuits connected to the power supply lines VDDY and VSSY. *Id.*, [0061]-[0066].

2. The Petition fails to show that *Reiner* in view of *Takahara* renders obvious claims 1-18.

a. Claim 4

- i. The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit . . . to**

protect the scanning line driving circuit . . . and the first protection circuit and the second protection circuit are connected to the power supply line” (claim 4[d]).

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit,” where the protection circuits are connected to a power supply line. Ex. 1001, claim 4[d].

As discussed, the Petition fails to show that *Reiner* discloses or renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit.” See §VI.A.2.a.i, *supra*. The Petition fails to show that *Takahara* fills *Reiner*’s gaps: *Takahara* does not disclose or render obvious “a first protection circuit and a second protection circuit . . . and the first protection circuit and the second protection circuit are connected to the power supply line.”

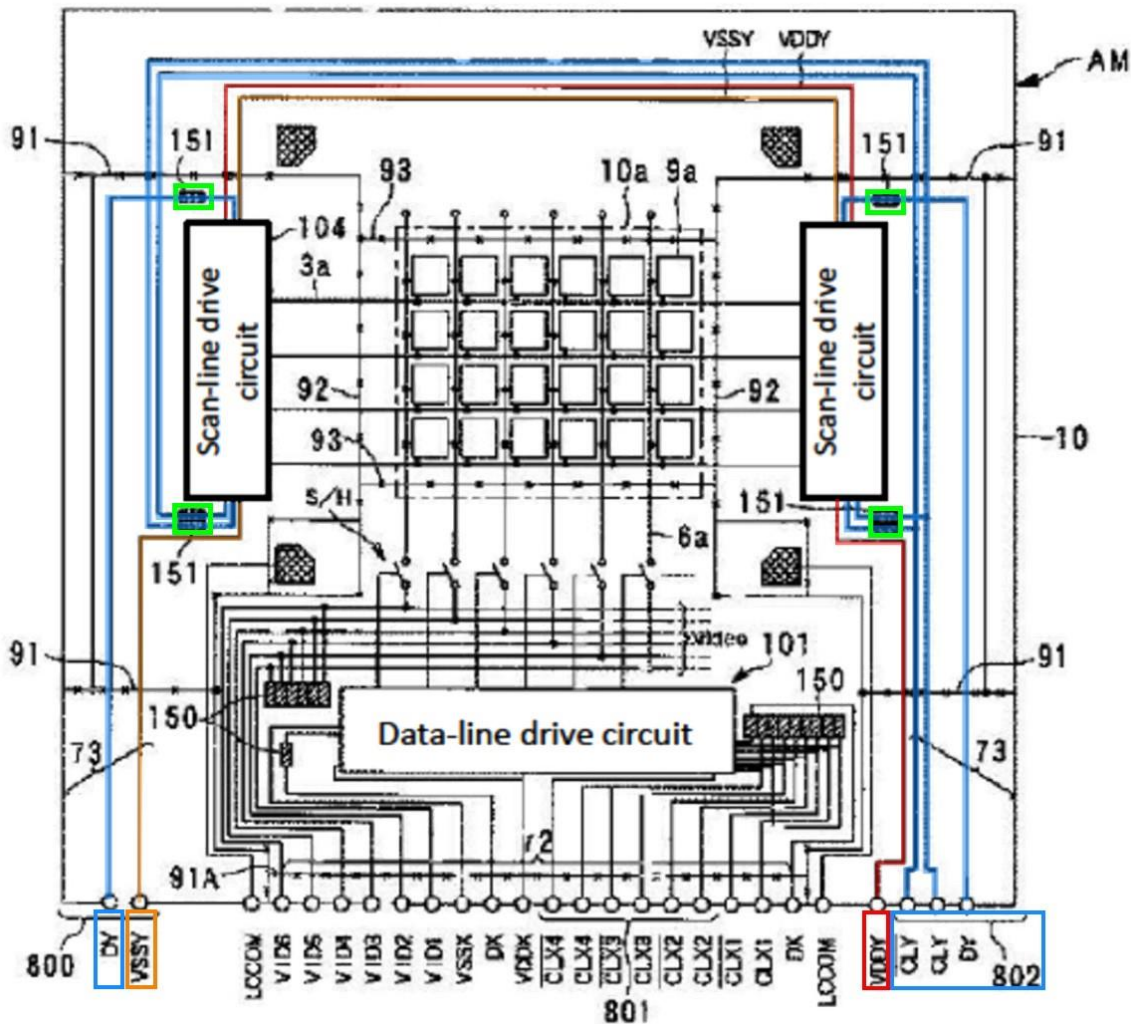
The Petition argues that *Takahara* discloses that “electrostatic-protection circuits 150 and 151 are formed at intermediate locations of the signal wirings 72 and 73” and that power supply lines VDDY and VSSY are signal wirings. Pet., 76. But *Takahara* does not disclose two protection circuits connected to a power supply line. The Petition sets aside *Takahara*’s express disclosures that show that

its protection circuits are disposed on only *signal* lines and not on power supply lines.

First, the Petition cites no evidence showing that *Takahara*'s power supplies VDDY and VSSY are "signal lines." Indeed, *Takahara*'s disclosure shows otherwise. *Takahara*'s disclosure distinguishes between power supply lines and signal lines. Signal lines "supply the signals for driving the scan-line drive circuits or the data-line drive circuit"—supplying a signal is different than supplying power. Ex. 1007, [0024]-[0025]; Ex. 2001 ¶89. In fact, *Takahara* provides that signal lines include "a start signal DY, a clock signal CLY, and an inverted-clock signal CLY bar," and "the scan-line drive circuits 104 are driven in accordance with these signals." *Id.*, [0061]; *see also id.*, [0060] (explaining that other signal lines include "image signals VID1-VID6" and "a start signal DX, clock signals CLX1-CLX4, and inverted-clock signals CLX1 bar to CLX4 bar" and "the data-line drive circuit 101 is driven in accordance with these signals"). *Takahara* does not include power lines in its discussions of signal lines.

Indeed, Figure 1 shows that **electrostatic-protection circuits 151** are formed only at intermediate locations of the **clock signal lines and start signal lines** (DY, CLY, CLY bar) that drive the scan-line driving circuit 104; they are not

formed at intermediate locations of the power supply lines **VSSY** and **VDDY**. *Id.*, [0061], [0065]; Ex. 2001 ¶90.



Id., Fig. 1. *Takahara* explains that the scan line and data line driving circuits are both “driven in accordance with” start, clock, and image signals, not power lines. *Id.*, [0060] (signals that drive the scan line driving circuit, [0061] (signals that drive the data line driving circuit); Ex. 2001 ¶91. Further, the “signal wirings” 73 shown in Figure 1 are “for driving the scan-line drive circuits 104” which are

“routed from” terminals 800 and 802. *Id.*, [0065]. The annotations identifying signal lines 73 and terminals 802 on the right side of Figure 1 include only CLY bar, CLY, and DY signal wirings and terminals, which confirms that the annotations identifying signal lines 73 and terminal 800 on the left side of Figure 1 apply only to the DY signal wiring. Ex. 2001, ¶91.

Second, recognizing that Figure 1 does not show that a protection circuit is formed on VDDY or VSSY, the Petition suggests that *Takahara* connects the power lines to protection circuits *formed on other lines* (signal lines), through short-circuit wirings 91. Pet., 76-77. But *Takahara* does not disclose that the short-circuit wirings connect the power lines to the signal lines. Instead, *Takahara* discloses that the purpose of *Takahara*’s short-circuit wiring is to diffuse static electricity “toward an outer perimeter of the substrate via . . . the short-circuit wiring” to prevent it flowing through circuits on the substrate. Ex. 1007, [0004]. This purpose contradicts the Petition’s self-serving annotation of Figure 1, for which the Petition offers no evidence to support. Pet., 76-77; Ex. 2001 ¶92.

Third, even if *Takahara* disclosed connecting the power supply lines to protection circuits formed on other lines through the short-circuit wirings 91, those short-circuit wiring lines form temporary connections that are “harmful to the normal operation of the device” and must be cut “at an appropriate stage” in the manufacturing process before the display device can operate. Ex. 1007, [0070].

Fourth, *Takahara* does not disclose two protection circuits connected to *one* power supply line to protect the scanning line driving circuit. No matter how Petitioner annotates Figure 1, *Takahara* does not disclose or render obvious a first and second protection circuit connected to a power supply line to protect the scanning line driving circuit. The Petition does not argue or show otherwise, and is careful to argue only that *Takahara* renders obvious connecting a first and second protection circuit to a scanning line driving circuit. Pet., 78. The Petition does not argue or show that *Takahara* discloses or renders obvious limitations 4[e] or [f], regarding the layout of connections between the power line, scanning line driving circuit, and protection circuits.

Thus, neither *Reiner* nor *Takahara* separately or in combination, discloses or renders obvious “a first protection circuit and a second protection circuit . . . and the first protection circuit and the second protection circuit are connected to the power supply line.”

ii. The Petition cites no evidence showing that *Takahara* would motivate a POSITA to modify *Reiner*’s ESD protection network.

The Petition cites no evidence showing that a POSITA would have been motivated to modify *Reiner* in view of *Takahara*, or “to form *Reiner*’s gate driver 63 directly on the glass substrate of *Takahara*.” Pet., 74-75. *Reiner*’s internal ESD protection network protects IC chips; the Petition cites no reason to add additional

protection circuits, akin to *Takahara*'s, outside of those integrated circuits.

Takahara, by contrast, discloses protection circuits outside of a scanning line driving circuit, which is on an active matrix substrate, to protect the driving circuit from electrical charges that could enter the scanning line driving circuit through signal lines. Ex. 1007, [0066]. *Takahara* suggests no motivation to modify *Reiner*'s driver ICs in view of *Takahara* because *Reiner*'s ESD protection network already protects source driver 61 from the risk of electrical charges entering via contact pads 72 and damaging the circuitry within the output devices 70 of source driver 61.

b. Claims 5-9

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 5-9.

c. Claim 10

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit . . . the first protection circuit and the second protection circuit are connected to the power supply line,” claim 10[d], for the same reasons that it fails to render obvious those limitations in claim 4[d]. See §VI.B.2.a.i, *supra*.

d. Claims 11-15

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 11-15.

e. Claim 16

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit . . . connected to the power supply line . . . the first protection circuit and the second protection circuit are connected to the scanning line driving circuit,” claim 16[d], for the same reasons that it fails to render obvious those limitations in claim 4[d]. See §VI.B.2.a.i, *supra*.

f. Claim 17

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit . . . connected to the power supply line . . . the first protection circuit and the second protection circuit are connected to the scanning line driving circuit,” claim 17[d], for the same reasons that it fails to render obvious those limitations in claim 4[d]. See §VI.B.2.a.i, *supra*.

g. Claim 18

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit . . . connected to the power supply line . . . the first protection circuit and the second protection circuit are connected to the scanning line driving circuit,” claim 18[d], for the same reasons that it fails to render obvious those limitations in claim 4[d]. See §VI.B.2.a.i, *supra*.

h. Claim 1

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit . . . and the first protection circuit and the second protection circuit are connected to the power supply line,” claim 1[d], for the same reasons that it fails to render obvious those limitations in claim 4[d]. See §VI.B.2.a.i, *supra*.

i. Claims 2-3

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 1 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 2-3.

VII. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. § 314 AND *FINTIV*

The Board should exercise its discretion to deny the Petition under *Fintiv* and the Director’s Interim Guidance.⁴ The *Fintiv* factors weigh against institution.

First, the United States District Court for the Eastern District of Texas has not stayed the parallel proceedings. And no evidence suggests that the district court would grant a stay were the Board to institute; three of six patents-in-suit are not subject to *inter partes* review proceedings. See *AGIS Software Development LLC v. Google LLC*, 2:19-CV-00361-JRG, 2021 WL 465424, at *2 (E.D. Tex. Feb. 9, 2021) (“It has been this Court’s consistent and long established practice to deny motions to stay pending IPR and EPR when the PTAB or PTO have instituted review on less than all asserted claims of all asserted patents because at least one or more originally asserted claims will be unaffected by the outcome of those parallel proceedings and left intact before this Court to be tried.”). Investment in the district court proceedings is ongoing.

Second, trial in the district court proceedings will take place on June 2, 2025, more than six months before the Board’s Final Written Decision deadline.

⁴ K. Vidal, INTERIM PROCEDURE FOR DISCRETIONARY DENIALS IN AIA POSTGRANT PROCEEDINGS WITH PARALLEL DISTRICT COURT LITIGATION (June 21, 2022), https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

Ex. 1015. Median time from filing to trial in the district is 21.6 months as of June 2024, which would push trial only to August 2025, as the Petition notes.⁵ The district court is, under the issued trial date and the estimated time-to-trial, expected to try this case before the Board’s Final Written Decision deadline.

Third, issues before the Board are substantially the same as those before the district court. Only claims 1-3, 6, and 12, challenged here, are not asserted in the district court. Petitioner has not submitted a *Sotera* stipulation.

Fourth, the Petition has not demonstrated a reasonable likelihood of success, much less a compelling likelihood of success. And the other factors weigh in favor of dismissal. *See CommScope Techs. LLC. v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4 (February 27, 2023) (Precedential) (“I intended for PTAB panels to only consider compelling merits if they first determined that *Fintiv* factors 1–5 favored a discretionary denial.”).

VIII. CONCLUSION

The Petition does not establish a reasonable likelihood that any of the challenged claims are unpatentable. The Board should deny institution.

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https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0630.2024.pdf.

IPR2024-00973

U.S. Patent No. 9,184,157

Date: September 20, 2024

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

I certify that this Patent Owner's Preliminary Response complies with the word count limit and contains 7,806 words in 14-point Times New Roman font as calculated by the word count feature of Microsoft Office, in compliance with 37 C.F.R. § 42.24(a)(1)(i). This word count is inclusive of all text and footnotes but does not include the table of contents, table of authorities, certificate of service or word count, or appendix of exhibits or claim listing.

Date: September 20, 2024

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CERTIFICATE OF SERVICE

I certify that on September 20, 2024, a copy of Patent Owner's Preliminary Response, including exhibits, was served in its entirety by electronic mail to Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

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