

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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BOE TECHNOLOGY GROUP CO., LTD.,  
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,  
Patent Owner.

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IPR2024-00973  
Patent 9,184,157 B2

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Before GRACE KARAFFA OBERMANN, GEORGE R. HOSKINS, and  
CHRISTOPHER M. KAISER, *Administrative Patent Judges*.

HOSKINS, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

Petitioner BOE Technology Group Co., Ltd. has filed a Petition (Paper 1, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of U.S. Patent No. 9,184,157 B2 (Ex. 1001, “the ‘157 patent”), claims 1–18.

Patent Owner 138 East LCD Advancements Limited filed a Preliminary Response (Paper 6, “Prelim. Resp.”), urging us to exercise our discretion under 35 U.S.C. § 314(a) and *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”) to deny institution, and arguing the Petition fails to satisfy the requisite threshold for instituting review on the merits.

We authorized additional briefing to address discretionary denial under *Fintiv*. Accordingly, Petitioner filed a Preliminary Reply (Paper 7, “Prelim. Reply”), and Patent Owner filed a Preliminary Sur-reply (Paper 8, “Prelim. Sur-reply”). For reasons provided below, we decide not to invoke this discretion to deny institution.

On the merits, to justify institution of review, the information presented in the record must demonstrate a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim. *See* 35 U.S.C. § 314(a). Applying that standard on behalf of the Director (37 C.F.R. § 42.4(a)), we institute the petitioned *inter partes* review.

## II. BACKGROUND

### A. *Real Parties-in-Interest and Related Proceedings*

Petitioner identifies itself (i.e., BOE Technology Group Co., Ltd.) as a real party-in-interest. *See* Pet. 92. Patent Owner identifies itself (i.e., 138

East LCD Advancements Limited) and Longitude Licensing Limited as real parties-in-interest. *See* Paper 4, 1.

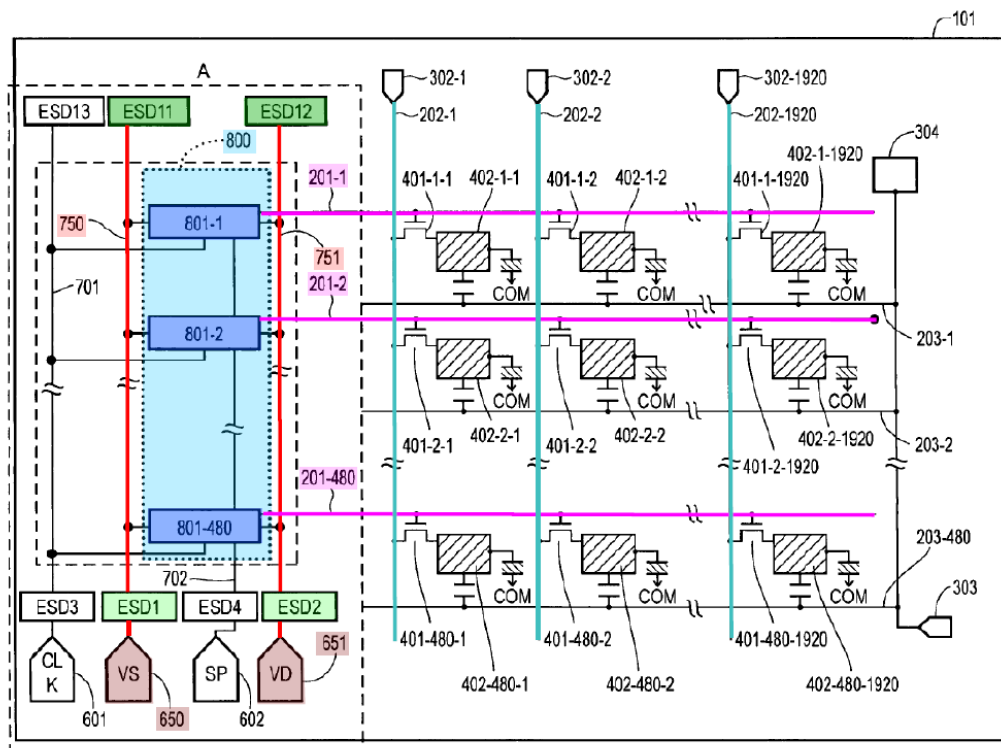
The parties also identify *Longitude Licensing Ltd., et al. v. BOE Tech. Group Co., Ltd.*, Case No. 2:23-cv-00515 (E.D. Tex.) (“the Co-Pending Litigation”) as a related matter. *See* Pet. 92; Paper 4, 1.

Petitioner has filed two other IPR challenges to patents owned by Patent Owner. They are IPR2024-00976 (U.S. Patent No. 7,502,079 B2) and IPR2024-00977 (U.S. Patent No. 9,557,606 B2).

### *B. The '157 Patent Specification*

The '157 patent is directed to a display device with a driving circuit that is protected from electrostatic damage (ESD) by protective circuits. *See* Ex. 1001, code (57), 1:10–20. Figure 1 of the '157 patent is reproduced below, with our color annotations added.

FIG. 1



**'157 Patent, Figure 1 (Annotated in Color).**

Figure 1 illustrates active matrix substrate 101 having a built-in scanning line driving circuit 800 (blue) for supplying drive signals to scanning lines 201-1 through 201-480 (purple) in a liquid crystal display device. *See id.* at 4:30–32, 4:60–66, 5:20–23. The display region of substrate 101 also has data lines 202-1 through 202-1920 (teal) and capacitance lines 203-1 through 203-480 (uncolored) which, together with scanning lines 201 (purple), control pixel elements 401 / 402 (uncolored) to create a display. *See id.* at 4:64–5:19.

Scanning line driving circuit 800 (light blue) is composed of scanning line driving unit circuits 801-1 through 801-480 (dark blue), with one unit circuit 801 provided for each scanning line 201. *See id.* at Fig. 1, 5:20–28. Each unit circuit 801 (dark blue) is powered by low potential power source line 750 (red) and high potential power source line 751 (also red). *See id.* at Fig 1, 5:28–31. Those lines 750 and 751 (red) each receive a voltage supply via respective input terminals 650 and 651 (brown) disposed on active matrix substrate 101. *See id.* at 5:36–43.

Protective circuits ESD1 and ESD2 (light green) are connected to a connecting line between each input terminal 650 and 651 (brown) and its associated power source line 750 or 751 (red). *See id.* at 5:44–51. This “prevent[s] TFTs [thin film transistors] within the scanning line driving circuit 800 from being damaged when the static electricity or noise current is input from” terminals 650 and 651 (brown). *Id.* at 1:34, 5:51–54.

Protective circuits ESD11 and ESD12 (dark green) “are disposed at far end of the opposite side” of scanning line driving circuit 800 (light blue) from protective circuits ESD1 and ESD2 (light green), on each power source line 750 and 751 (red). *Id.* at 5:55–61. “Thereby, it is possible to suppress

that a unit, (for example,  $n=1$ , etc.), located far from a terminal [650 or 651 (brown)], among scanning line driving unit circuits 801- $n$  [(dark blue)], is damaged by the static electricity during manufacturing the active matrix substrate.” *Id.* at 5:61–65.

The ’157 patent describes that its Figure 1 embodiment improves upon the “conventional art” illustrated in Figure 11, which appears to be identical to Figure 1 except that it does not have protective circuits ESD11–ESD13 (e.g., dark green) disposed on the opposite side of scanning line driving circuit 800 (light blue) from protective circuits ESD1–ESD4 (e.g., light green). *Id.* at 1:43–2:30, Fig. 11. Those additional protective circuits ESD11–ESD13, according to the ’157 patent, can be useful when substrate 101 is formed of an insulating material such as glass rather than a conductive material such as silicon, by providing additional and more proximate mechanisms to dissipate electrostatic charges away from circuit 800 (light blue). *See id.* at 1:14–56, 2:33–57, 3:6–11. This same goal can be advanced further by adding more protective circuits around scanning line driving circuit 800 (light blue). *See id.* at 7:17–47 (describing Fig. 2, including protective circuits ESD21–ESD23), 7:61–8:60 (describing Figs. 3, 7, and 8, including protective circuits disposed within buffer circuits 810).

### *C. The ’157 Patent Claims*

The ’157 patent includes eighteen claims, all of which are challenged here. *See* Ex. 1001, 11:43–15:3; Pet. 15. Claim 4 is illustrative (*see* Pet. 16; Prelim. Resp. 19 n.3), and it recites:

4. A display device, comprising:  
a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Ex. 1001, 12:25–47.

*D. Asserted Prior Art*

Petitioner relies principally on the following two references as prior art against the '157 patent. *See* Pet. 14–15.

| Name     | Reference        | Exhibit No(s).           |
|----------|------------------|--------------------------|
| Reiner   | WO 03/019657 A2  | 1005                     |
| Takahara | JP 2003-121875 A | 1006 & 1007 <sup>1</sup> |

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<sup>1</sup> Exhibit 1006 is the original reference in Japanese, and Exhibit 1007 is an English translation. We cite to the latter in this Decision.

Patent Owner does not dispute at this time that these references are prior art against the '157 patent. *See* Prelim. Resp. *generally*.

*E. Asserted Grounds*

Petitioner asserts the following two grounds of unpatentability. *See* Pet. 15.

| 35 U.S.C. §         | Reference(s)     | Claims Challenged |
|---------------------|------------------|-------------------|
| 103(a) <sup>2</sup> | Reiner           | 1–18              |
| 103(a)              | Reiner, Takahara | 1–18              |

*F. Testimonial Evidence*

Petitioner relies on the proffered expert witness testimony of Patrick Murphy, Ph.D. (Exhibit 1003). Patent Owner relies on the proffered expert witness testimony of E. Fred Schubert, Ph.D. (Exhibit 2001).

III. POTENTIAL DENIAL UNDER 35 U.S.C. § 314(a) AND *FINTIV*

Patent Owner, relying on *Fintiv*, contends we should deny institution based on the status of the Co-Pending Litigation. *See* Prelim. Resp. 40–41; Prelim. Sur-reply. Petitioner disagrees. *See* Pet. 90–91; Prelim. Reply.

As part of its Preliminary Reply, Petitioner “stipulates for the '157 patent ‘that, if the PTAB institutes *inter partes* review, Petitioner “will not pursue in [the Co-Pending Litigation] the specific grounds [asserted in

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<sup>2</sup> Amendments to 35 U.S.C. § 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”) took effect in March 2013. The '157 patent issued from an application filed in May 2009. *See* Ex. 1001, code (22). Therefore, we apply the pre-AIA version of § 103.

this IPR proceeding], or . . . any other ground . . . that was raised or could have been reasonably raised in an IPR.”” Prelim. Reply 1 (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 13–14 (PTAB Dec. 1, 2020) (precedential)). Based on that stipulation, Petitioner contends we should not exercise our discretion under 35 U.S.C. § 314(a) and *Fintiv* to deny institution here. *See id.* at 1–2 (citing USPTO Memorandum, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022) (“Guidance Memo”)<sup>3</sup>). In response to the Board’s e-mail authorizing the Preliminary Reply, which invited Petitioner to show good cause for why the *Sotera* stipulation was not filed earlier with the Petition, Petitioner argues good cause is not required and cites PTAB decisions that permitted *Sotera* stipulations to be filed after a preliminary response but before a decision on institution. *See id.* at 2–3.

Patent Owner responds that “Petitioner knew and chose to address *Fintiv* and discretionary denial in its Petition” without proffering a *Sotera* stipulation, resulting in Patent Owner “dedicating words to [discretionary denial] issues” in the Preliminary Response. Prelim. Sur-reply 1. Further according to Patent Owner: “Nothing in Petitioner’s explanation identifies a reason to change its position since filing its Petition.” *Id.*

We firstly conclude that the weight of authority presented here indicates there have been multiple instances when the Board has permitted a *Sotera* stipulation to be filed after a preliminary response but before a decision on institution, despite that this resulted in the patent owner devoting

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<sup>3</sup> Available at [www.uspto.gov/sites/default/files/documents/interim\\_proc\\_discretionary\\_denials\\_aia\\_parallel\\_district\\_court\\_litigation\\_memo\\_20220621\\_.pdf](http://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf).

pages in its preliminary response to *Fintiv* issues that were mooted later by the stipulation pursuant to the Guidance Memo. *See* Prelim. Reply 2–3 (citing, *inter alia*, *Samsung Elecs. Co., Ltd. v. Sung*, IPR2024-00533, Paper 12 at 4–5 (PTAB July 25, 2024); *BMW of N. Am., LLC v. NorthStar Sys. LLC*, IPR2023-01017, Paper 12 at 8–11 (PTAB Dec. 8, 2023); *Vector Flow, Inc. v. HID Global Corp.*, IPR2023-00353, Paper 15 at 1–2, 8–9 (PTAB Oct. 17, 2023); *Samsung Elecs. Co., Ltd. v. Apex Beam Techs., LLC*, IPR2023-00598, Paper 8 at 3 (PTAB Aug. 8, 2023)). Patent Owner does not cite any Board decisions that support its position in this case. *See* Prelim. Sur-reply 1.

We secondly conclude Petitioner’s stipulation is commensurate in scope with a *Sotera* stipulation. *See Sotera*, Paper 12, at 13–14, 18–19; Guidance Memo, at 3. The Guidance Memo states:

Consistent with *Sotera Wireless, Inc.*, the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.

Guidance Memo, 3, 7–8. Thus, applying that guidance here, we do not deny institution in view of the Co-Pending Litigation.

#### IV. PETITIONER’S GROUNDS OF UNPATENTABILITY

##### A. Legal Standards — Petitioner’s Burden

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the

grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

*B. Legal Standards — Obviousness*

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, if made available in the record, which has not happened here. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*C. Level of Ordinary Skill in the Art*

Petitioner contends a person having ordinary skill in the art pertaining to the ’157 patent “would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays,” and “[a]dditional relevant work experience can compensate for less education, and *vice versa*.” Pet. 15–16; Ex. 1003 ¶¶ 75–76.

“Patent Owner does not dispute the level of skill for a person of ordinary skill in the art . . . set forth in the Petition.” Prelim. Resp. 14; Ex. 2001 ¶¶ 19–20.

For purposes of this Decision, we adopt Petitioner’s assessment of the level of ordinary skill in the art, as it appears to be consistent with the ’157 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

#### *D. Claim Construction*

We interpret the ’157 patent claims “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). This “includ[es] construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

Petitioner argues “no terms need construction to resolve the controversy in this” IPR proceeding. Pet. 14.

“Patent Owner contends that the claims should be given their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art.” Prelim. Resp. 14. Patent Owner does not proffer any constructions for particular terms. *See id.*

Based on the arguments and evidence presented at this time, we determine no explicit construction is needed to resolve the parties’ controversy. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*E. Ground One — Obviousness over Reiner*

In Ground One, Petitioner asserts claims 1–18 of the '157 patent are unpatentable as having been obvious over Reiner. *See* Pet. 1–10, 15, 16–71. Patent Owner disagrees. *See* Prelim. Resp. 1–2, 15–28.

We firstly summarize Reiner's disclosure. Then we consider the parties' competing contentions, and we conclude the record demonstrates a reasonable likelihood that Petitioner would prevail with respect to at least claim 4. Therefore, we grant the petitioned *inter partes* review.

*1. Overview of Reiner*

Reiner is directed to an integrated circuit device with bump bridges. *See* Ex. 1005, code (54). Figure 2 of Reiner shows a first embodiment of Reiner's invention (*see id.* at 6:18),<sup>4</sup> and is reproduced below with our color annotations added.

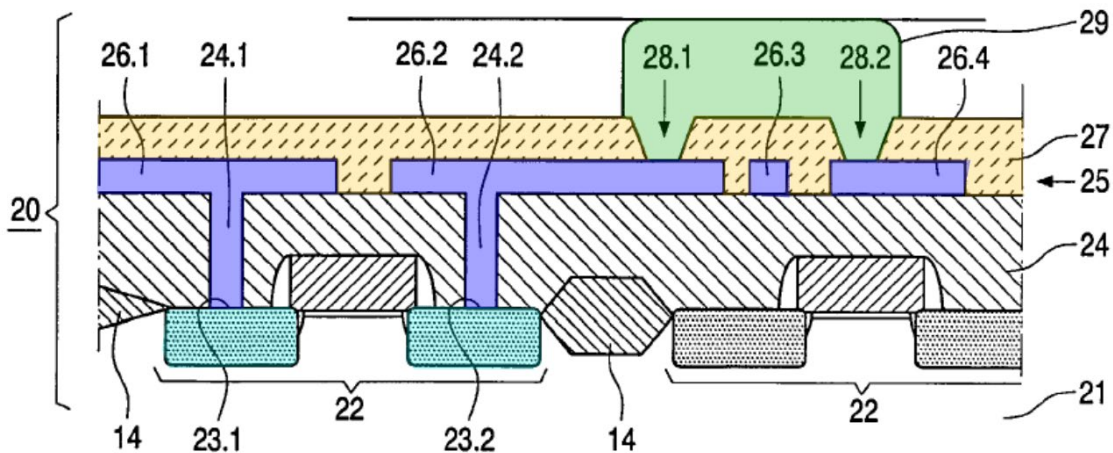


**FIG. 2**

**Reiner, Figure 2 (Annotated in Color).**

<sup>4</sup> When citing to Exhibit 1005, we refer to the pagination added by Petitioner at the bottom left corner of each page.

Figure 2 illustrates integrated circuit device 20 comprising silicon substrate 21, at least one integrated device 22 (light blue), isolating layer 24, metallization level 25 (dark blue), passivation layer 27 (yellow), and bump bridge 29 (green). *See id.* at 6:18–31, 7:12. Bump bridge 29 electrically connects metal lines 26.2 and 26.4, while isolating that connection from metal line 26.3, “to provide for a connection to an ESD [electrostatic discharge] device (not shown in Fig. 2)” that “prevent[s] the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event.” *Id.* at 2:28–3:3, 4:12–16, 7:3–18.

Figure 3 of Reiner shows a second embodiment of Reiner’s invention (*see id.* at 8:8–11, 8:18–19), and is reproduced below.

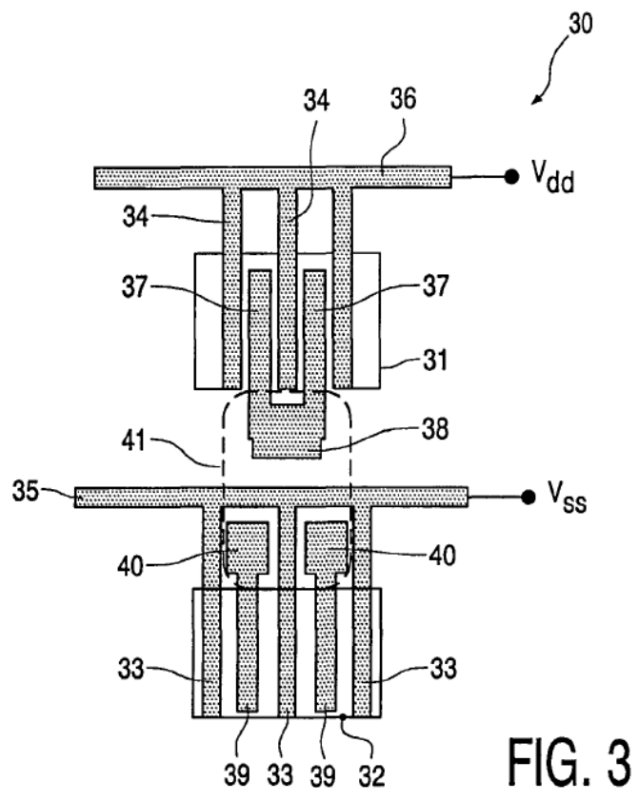


**FIG. 3**

**Reiner, Figure 3.**

Figure 3 illustrates integrated circuit device 30 comprising integrated device 31 powered by supply voltage  $V_{dd}$  via metal lines 34 and 36, and

integrated device 32 powered by supply voltage  $V_{ss}$  via metal lines 33 and 35, wherein devices 31 and 32 are electrically connected to each other by bump bridge 41. *See id.* at 8:18–9:10. This embodiment is “well suited for” incorporating “electrostatic discharge device (ESD) protection” (partly including device 31 in Figure 3) via bump bridge 41 connecting the two devices 31 and 32 “without making any connection to the metal line 35 ( $V_{ss}$ ).” *Id.* at 8:8–17, 8:31–9:10.

Reiner indicates that “[t]he bump-bridge technology presented herein” is “particular[ly] suited” for use with “[i]ntegrated circuit devices [that] have areas where the output or input metal lines have to cross power supply lines.” *Id.* at 9:11–18. One example, according to Reiner, is “an integrated circuit display driver 61 or 63 that is designed to drive many lines of an LCD display 60, as illustrated in” Figure 4, because “[s]uch a display driver 61, 63 typically has a large number of parallel outputs.” *Id.* at 9:12–15.

Figure 4 is reproduced below.

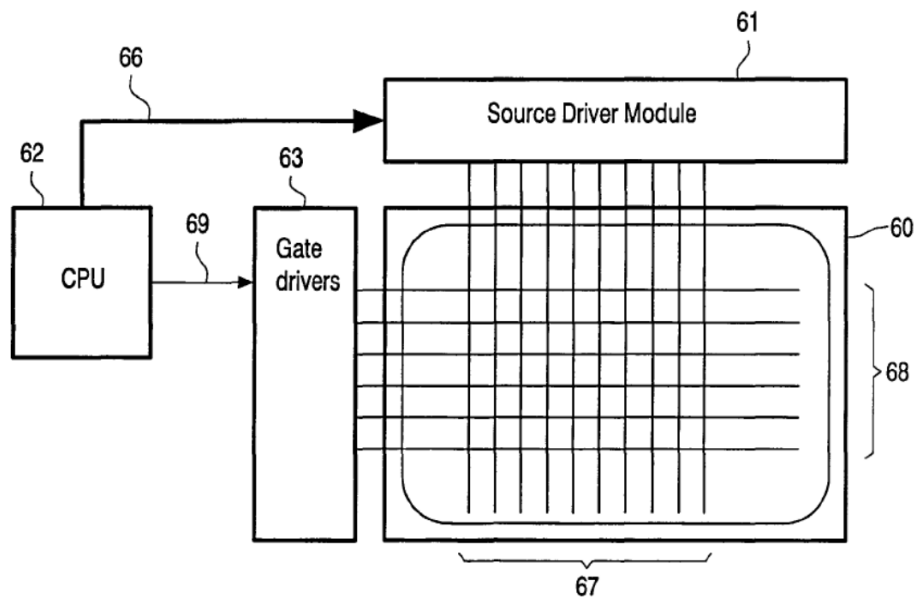


**FIG. 4**  
**Reiner, Figure 4.**

Figure 4 is a schematic block diagram of an LCD display including: LCD screen 60; source driver module 61 which drives individual source lines 67 in the display; gate driver 63 which usually drives one whole gate 68 in the display; and CPU 62 which controls the scanning of lines 67 and 68. *See id.* at 9:23–31. “The bump bridges allow many output devices of the integrated circuit device 61 or 62 [sic ‘63’<sup>5</sup>] to cross the power supply lines which provide supply voltage (e.g.,  $V_{dd}$ ) to the output devices.” *Id.* at 9:18–20.

Reiner’s Figure 5 presents “[a] schematic block diagram of a display driver 61” in which “protection means can easily be integrated.” *Id.* at 9:18–22. Figure 5 is reproduced below with our color annotations added.

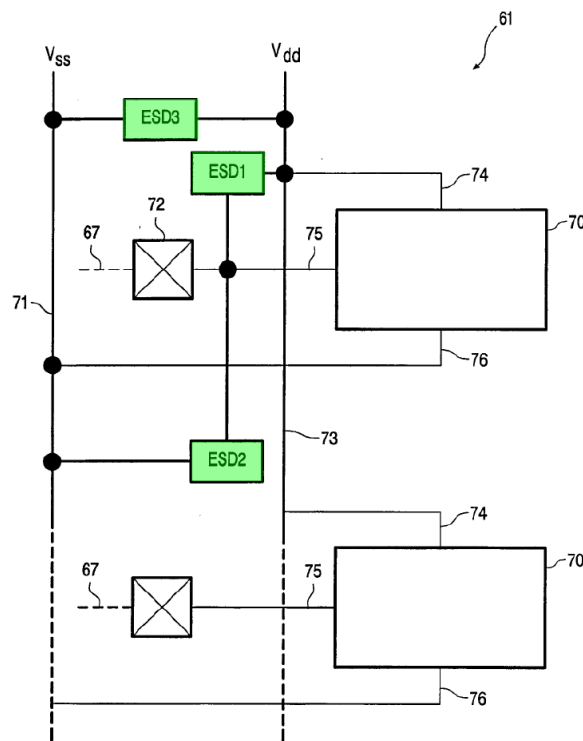


FIG. 5  
Reiner, Figure 5 (Annotated in Color).

<sup>5</sup> On the present record, we agree with Petitioner’s unopposed contention that Reiner’s reference to “62” here is a typographical error for “63.” *See* Ex. 1005, 9:11–31; Pet. 8 n.4; Ex. 1003 ¶ 56 n.5.

Figure 5 illustrates source driver module 61 that “comprise[s] several source drivers,” and in particular has one output device 70 per each source line 67, to drive the line via output line 75 and contact pad 72. *See id.* at Figs. 4–5, 9:31–10:6 (“There is an array of several parallel output devices 70 (two such output devices are shown in Fig. 5).”). Power supply line 71 provides supply voltage  $V_{ss}$  through connections 76 to each output device 70, and power supply line 73 provides supply voltage  $V_{dd}$  through connections 74 to each output device 70. *See id.* at 10:7–10. Further: “[T]hree ESD devices ESD1, ESD2, and ESD3 [(green)] are provided for each output device 70” at locations shown in Figure 5, “in order to protect the circuitry inside the devices 70” such that “to cross some of the lines, bump bridges can be employed.” *Id.* at 10:10–23, 14:33–15:21 (claims 12 and 13).

## 2. *Claim 4*

Petitioner provides arguments and evidence in support of its contention that claim 4 is unpatentable as having been obvious over Reiner, including supporting testimony from Dr. Murphy. *See* Pet. 7–10, 16–40; Ex. 1003 ¶¶ 54–56, 88–133. Patent Owner opposes, as supported by testimony from Dr. Schubert. *See* Prelim. Resp. 1–2, 15–24; Ex. 2001 ¶¶ 47–63. For the following reasons, we conclude Petitioner has demonstrated a reasonable likelihood of prevailing on its assertions for claim 4.

### (i) *The Claim Preamble*

The preamble of claim 4 refers to “[a] display device.” Ex. 1001, 12:25. Petitioner assumes the preamble is limiting, and contends Reiner discloses a display device as the LCD display shown in Figure 4. *See*

Pet. 16–17 (citing Ex. 1005, Fig. 4, 6:7, 9:24–26; Ex. 1003 ¶ 89). We conclude this contention, which Patent Owner does not oppose at this time, is supported sufficiently by the cited disclosures in Reiner and by Dr. Murphy’s testimony to justify institution of review. In particular, Reiner describes Figure 4 as illustrating LCD screen 60 and associated control circuitry. *See* Ex. 1005, 6:7, 9:23–31.

(ii) *A Scanning Line Driving Circuit*

Claim 4 next recites the display device comprises “a scanning line driving circuit.” Ex. 1001, 12:25–26. Petitioner contends Reiner’s display device correspondingly includes gate driver 63. *See* Pet. 7, 17–18 (citing Ex. 1005, Fig. 4, 9:11–14, 9:25–31; Ex. 1003 ¶¶ 90–92). We conclude this contention, which Patent Owner does not oppose at this time, is supported sufficiently by the cited disclosures in Reiner and by Dr. Murphy’s testimony to justify institution of review.

In particular, both expert witnesses testify that: (1) Reiner’s *gate line* driver 63 is analogous to the *scanning line* driving circuit 800 of Figure 1 in the ’157 patent; and (2) Reiner’s *source line* driver module 61 is analogous to the *data line* driver of Figure 1 in the ’157 patent. *See* Ex. 1003 ¶ 55 (Dr. Murphy referring to Reiner’s “gate driver / scanning line driver” 63 and “source / data line driver” 61); Ex. 2001 ¶ 48 n.2 (Dr. Schubert testifying that “‘source’ lines and ‘data’ lines refer to the same lines, and ‘gate’ lines and ‘scan’ lines refer to the same lines,” and “[t]he respective terms are interchangeable”). Therefore, we will refer hereafter to Reiner’s gate/scanning driver 63 (which is analogous to the “scanning line driving

circuit” of claim 4), and Reiner’s source/data driver module 61 (which is not recited as part of the invention in claim 4).

*(iii) A Power Supply Line*

Claim 4 next recites the display device comprises “a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line.” Ex. 1001, 12:27–30.

Petitioner contends the integrated circuit devices utilized in Reiner’s display device are powered by two power supply lines, respectively conveying a low voltage Vss and a high voltage Vdd. *See* Pet. 19–21 (citing Ex. 1005, Fig. 5, 9:12–14, 9:18–22, 10:7–9, 12:4–5; Ex. 1003 ¶¶ 93–95, 97).

Patent Owner does not oppose Petitioner’s foregoing contention at this time. Patent Owner does dispute Petitioner’s contention that Reiner’s Figure 5 “describes” an exemplary gate/scanning driver 63 as well as an exemplary source/data driver module 61. Pet. 19, 21; *see* Prelim. Resp. 19–22. For reasons provided below in Section IV.E.2(v)(b), we agree with Patent Owner in that regard, based on the present preliminary record. That is, in our present view, Reiner expressly discloses only that Figure 5 illustrates an exemplary source/data driver module 61, and Reiner does not disclose that Figure 5 also illustrates an exemplary gate/scanning driver 63.

Despite this shortcoming of Reiner’s Figure 5, we still conclude the preliminary record supports, sufficiently to justify institution, Petitioner’s contention that Reiner’s gate/scanning driver 63 is powered by a low voltage power supply line Vss and a high voltage power supply line Vdd. In particular, Reiner expressly discloses its integrated circuit device 30 is

powered by a low voltage power supply line Vss and a high voltage power supply line Vdd, and utilizes bump bridge 41 to incorporate ESD protection that avoids a connection to low voltage power supply line Vss. *See* Ex. 1005, Fig. 3, 8:8–9:10; *see also* Ex. 1003 ¶ 95 (testifying that Vss is a low potential power supply line and Vdd is a high potential power supply line).

Reiner also expressly discusses how its integrated circuit devices utilizing a bump bridge (including device 30 shown in Figure 3) are “particular[ly] suited” for use in *either* source/data driver module 61 *or* gate/scanning driver 63 as shown in Figure 4. *See id.* at 9:11–20. In this way, regardless of what is (or is not) shown in Figure 5, Reiner indicates its gate/scanning driver 63 is powered by a low voltage power supply line Vss and a high voltage power supply line Vdd.

Accordingly, on this record, Petitioner shows sufficiently, for purposes of trial institution, that Reiner discloses this power supply line limitation of claim 4.

*(iv) An Input Terminal Connected to the Power Supply Line*

Claim 4 next recites the display device comprises “an input terminal connected to the power supply line to supply power.” Ex. 1001, 12:31–32.

Petitioner contends Reiner “suggests or renders obvious” this limitation. Pet. 21. We discuss Petitioner’s contentions for utilizing power line input terminals in Reiner (which Patent Owner *does not* oppose), then we discuss Petitioner’s contentions as to where an ordinarily skilled artisan would have been led to locate the terminals in Reiner (which Patent Owner *does* oppose).

*(a) Utilizing Power Line Input Terminals in Reiner*

Petitioner asserts and Dr. Murphy testifies that a person of ordinary skill in the art “would have understood that [Reiner’s] power supply lines 71, 73 would require input terminals . . . so that power can be provided from the power source to the driver units [61 and 63] to drive the LCD display 60.” Pet. 21; Ex. 1003 ¶ 98. In the further view of Petitioner and Dr. Murphy, a person of ordinary skill in the art would have been motivated to provide such input terminals in Reiner with a reasonable expectation of success, “because it was conventional to do so and because there would need to be an input terminal to create a connection between the power lines Vdd/Vss of the scanning line driving circuit and the power source for the LCD display.” Pet. 21–24 (citing Ex. 1001, Fig. 11, 1:54–56, 2:5–14; Ex. 1005, 7:23–25, 9:12–14, 9:18–20, 9:27–29, 10:6–10, 12:4–5; Ex. 1007, Fig. 1, ¶¶ 63, 66); Ex. 1003 ¶¶ 97, 99–102. Petitioner moreover contends and Dr. Murphy testifies that utilizing input terminals would have been known “to facilitate manufacturing” when “connect[ing] the power supply lines with the corresponding power source or with the power supply lines of the substrate on which the LCD display is arranged.” Pet. 23; Ex. 1003 ¶ 101.

Patent Owner does not oppose Petitioner’s foregoing contentions at the present time. *See, e.g.*, Prelim. Resp. 22–24 (Patent Owner’s argument directed to the input terminal limitation, including that “[t]he Petition’s assertion that merely providing input terminals for power supply lines would have been obvious in view of conventional art described in the ’157 patent is irrelevant”).

We conclude the preliminary record supports, sufficiently to justify institution, Petitioner's contention that a person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner's power supply lines 71-Vss and 73-Vdd.

Importantly, Reiner does not disclose any particular mechanism or structure for supplying power to its power supply lines 71-Vss and 73-Vdd. Instead, Figure 3 simply illustrates metal line 35 being connected to supply voltage Vss by a thin black line, and metal line 36 being connected to supply voltage Vdd by a thin black line. *See* Ex. 1005, Fig. 3. Reiner's accompanying written description provides no further detail as to how power is supplied to the integrated circuit device 30 of Figure 3. *See id.* at 8:18–27.

Figure 5 similarly illustrates power supply line 71 being connected to supply voltage Vss, and power supply line 73 being connected to supply voltage Vdd, without providing any further detail as to how power is supplied to line 71-Vss and line 73-Vdd. *See id.* at Fig. 5, 10:7–10; *see also* Prelim. Resp. 18 (“Reiner does not disclose input pins on the source driver 61” and “Figure 5 shows no other inputs”).

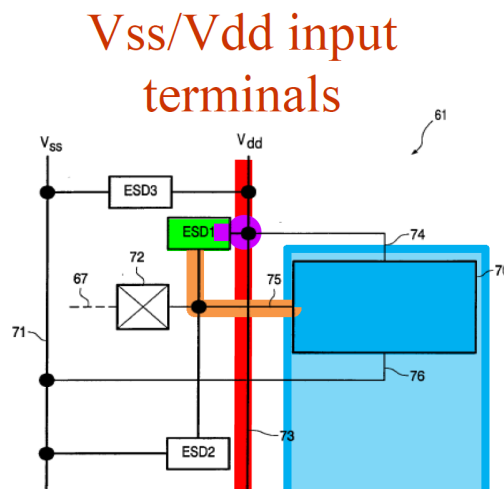
In light of that gap in Reiner's disclosure, we are persuaded by Dr. Murphy's testimony that a person of ordinary skill in the art would have been motivated to utilize input terminals to supply power to line 71-Vss and line 73-Vdd which would be required to operate Reiner's display device. *See* Ex. 1003 ¶¶ 97–102; Ex. 2001 ¶¶ 61–63 (Dr. Schubert's testimony directed to the input terminal limitation, not opposing this aspect of Dr. Murphy's testimony). Dr. Murphy's testimony is supported by the '157 patent's description of “the conventional art” as including the use of input terminals 650 and 651 for supplying power to power lines 750

and 751. *See* Ex. 1001, Fig. 11, 1:54–56, 2:5–15 (cited at Ex. 1003 ¶¶ 97, 100–102). It is also supported by Takahara’s disclosure of utilizing input terminals 800 and 802 for supplying power to power lines VSSY and VDDY which lead to scan line drive circuits 104. *See* Ex. 1007, Fig. 1, ¶¶ 63, 66 (cited at Ex. 1003 ¶¶ 101–102).

Thus, we conclude the preliminary record supports, sufficiently to justify institution, Petitioner’s contention that a person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner’s power supply lines 71-Vss and 73-Vdd.

*(b) Where to Locate the Power Line Input Terminals in Reiner*

Petitioner further asserts and Dr. Murphy testifies that a person of ordinary skill in the art “would have recognized that the input terminals *would have been [located] above the first ESD3*” in Reiner’s Figure 5, because this “was conventional in the prior art.” Pet. 22 (emphasis added) (citing Pet. 1–10 (§ II)); Ex. 1003 ¶ 100 (citing Ex. 1003 ¶¶ 49–56 (§ VI)). Dr. Murphy correspondingly annotates a portion of Reiner’s Figure 5 to illustrate this contention, as excerpted below. *See* Pet. 28; Ex. 1003 ¶ 110.



**Reiner, Figure 5 (Excerpt, Annotated by Petitioner’s Expert Witness).**

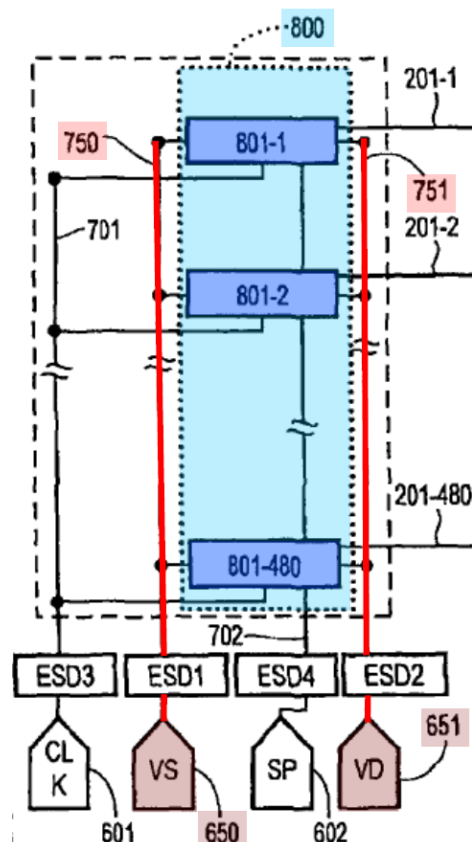
This excerpt of Reiner's Figure 5 is a schematic block diagram of source/data driver module 61 as annotated by Dr. Murphy, including that the "Vss/Vdd input terminals" would be located above the ends of lines 71-Vss and 73-Vdd. This *location* aspect of Petitioner's contentions is important because, as discussed below in Section IV.E.2(v), claim 4 specifies various positional relationships between two protection circuits and other components in the claimed display device, including the input terminal.

Patent Owner argues and Dr. Schubert testifies in opposition that Petitioner and Dr. Murphy "cite[] no evidence to support [their] conclusion that a [person of ordinary skill in the art] would have recognized that the input terminals would have been placed in a specific location, namely, 'above the first ESD3' in Reiner Figure 5." Prelim. Resp. 23 (citing Pet. 22); Ex. 2001 ¶ 62 (citing Ex. 1003 ¶ 100). Further according to Patent Owner and Dr. Schubert, Reiner does not "disclose[] or render[] obvious a particular location for input terminals of the display device." Prelim. Resp. 23; Ex. 2001 ¶ 63. As a result, Patent Owner argues Petitioner fails to show Reiner discloses or renders obvious the claimed positional relationship between the protection circuits and the input terminal. *See* Prelim. Resp. 22–24; Ex. 2001 ¶ 63.

We conclude Petitioner's contentions and Dr. Murphy's testimony in support are sufficiently articulated and supported by the evidence in the preliminary record to justify institution of review. In particular, so far as the evidence presently of record is concerned, Petitioner shows sufficiently for purposes of trial institution that a person of ordinary skill in the art would have known that the power input terminal for a scanning line driving circuit such as Reiner's gate/scanning driver 63 would have been connected to one

“end” of the circuit — that is, leading to the first scanning line or the last scanning line (depending on one’s perspective). *See* Pet. 1–10 (cited at Pet. 22); Ex. 1003 ¶¶ 49–56 (cited at Ex. 1003 ¶ 100).

This is shown, for example, in the conventional art illustrated in Figure 11 of the ’157 patent,<sup>6</sup> an excerpt of which is reproduced below with our color annotations added.



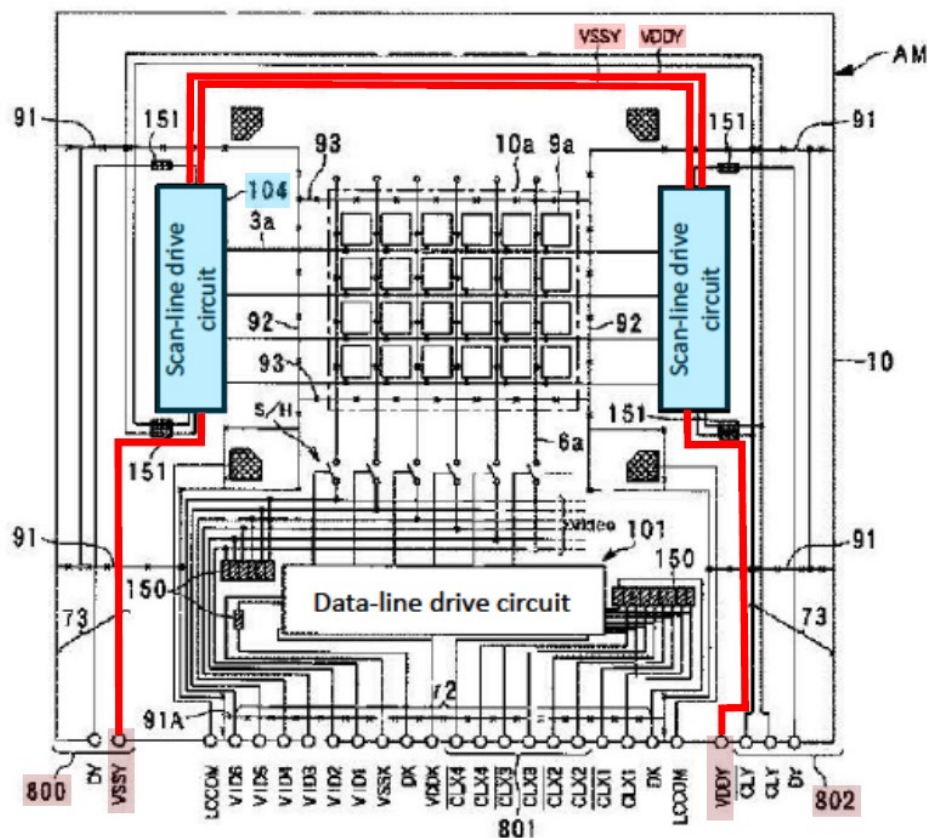
**’157 Patent, Figure 11 (Excerpt, Annotated in Color).**

<sup>6</sup> Pursuant to binding Office guidance, admissions in a challenged patent regarding the scope and content of the prior art may be used to supply missing claim limitations to establish obviousness in combination with prior art patents or printed publications in an IPR proceeding. *See* USPTO Memorandum, *Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311* (June 9, 2022) (available at [www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf](http://www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf)), 2–4.

Figure 11 illustrates “the conventional art” as utilizing input terminals 650 and 651 (brown) for supplying power to power lines 750 and 751 (red) in order to power scanning line driving circuit 800 (light blue) including scanning line driving unit circuits 801-1 through 801-480 (dark blue). *See* Ex. 1001, Fig. 11, 1:54–56, 1:66–2:15; *see also* Pet. 2–3, 22–23 (discussing the power line structure of Fig. 11); Ex. 1003 ¶¶ 50, 100–101 (same). As can be seen, power input terminals 650 and 651 (brown) are each connected to the end of circuit 800 (light blue) leading to the first / last driving unit circuit 801-480 (dark blue).

As a second example, Figure 1 of Takahara is reproduced below with our color annotations added.

FIG. 1



Takahara, Figure 1 (Annotated in Color).

Figure 1 of Takahara illustrates input terminals 800 and 802 (brown) for supplying power to power lines VSSY and VDDY (red) in order to power two scan-line drive circuits 104 (light blue) to drive scan lines 3a (uncolored). *See* Ex. 1007, Fig. 1, ¶¶ 58–59, 62–63, 66; *see also* Pet. 5–6, 23 (discussing the power line structure of Takahara’s Fig. 1); Ex. 1003 ¶¶ 53, 101 (same). As can be seen, power input terminals 800 and 802 (brown) are connected to the respective ends of circuits 104 (light blue) leading to the first / last scan line 3a (uncolored).

As a third example, Dr. Murphy’s annotations to Murai<sup>7</sup> Figure 1 reproduced at page 5 of the Petition illustrate a power line (red) connecting power circuit 151 (also red) to the end of scan line driver circuit 104 (blue) leading to the first / last scan line 3 (uncolored). *See* Pet. 3–5 (citing Ex. 1010, Fig. 1, ¶¶ 3, 21–22); Ex. 1003 ¶ 52.

Turning to Reiner, its Figure 5 is reproduced below with our color annotations added.

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<sup>7</sup> “Murai” is JP 2001-166334 A, found in the record at Exhibit 1009 (the original reference in Japanese) and Exhibit 1010 (an English translation). We cite to the latter in this Decision.

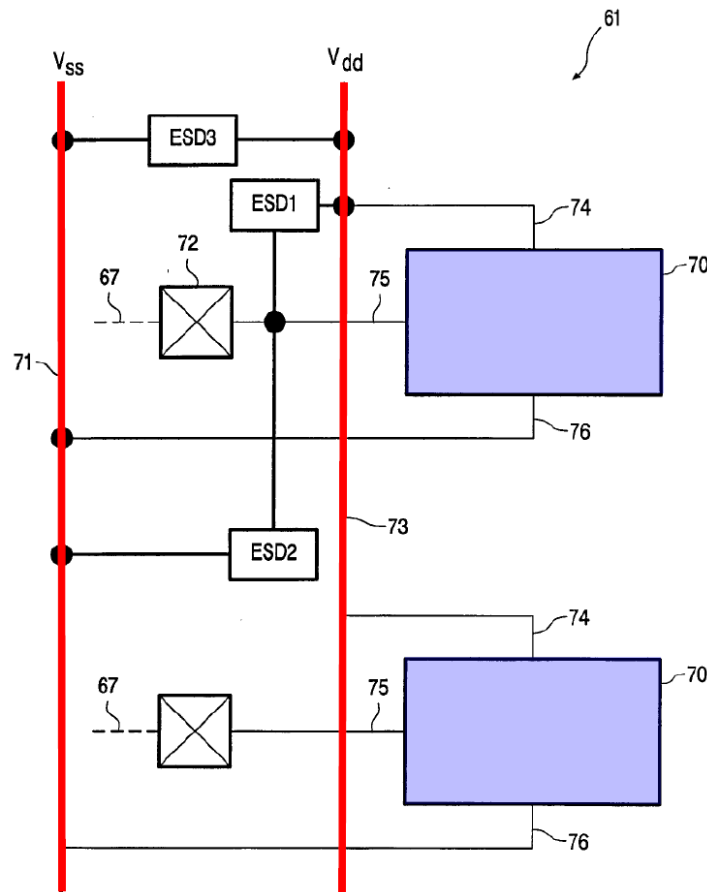


FIG. 5

**Reiner, Figure 5 (Annotated in Color).**

Figure 5 illustrates source/data driver module 61 having output devices 70 (dark blue) to drive source lines 67, each powered by two power supply lines 71-V<sub>ss</sub> and 73-V<sub>dd</sub> (red). *See* Ex. 1005, Fig. 5, 9:31–10:10. Although Figure 5 illustrates a source/data driver rather than a gate/scanning driver as recited in claim 4 (*see infra* Section IV.E.2(v)(b)), it nonetheless illustrates that the power lines (red) are fed into the end of the circuit leading to the first / last output device 70 (dark blue) and source line 67 (uncolored).

The foregoing evidence (i.e., the conventional art described in the '157 patent (Figure 11), Takahara (Figure 1), Murai (Figure 1), and Reiner (Figure 5)) supports Dr. Murphy's testimony that a person of ordinary skill

in the art “would have recognized that the input terminals would have been [located] above the first ESD3” in Reiner’s Figure 5, because this “was conventional in the prior art.” Pet. 22 (citing Pet. 1–10 (§ II)); Ex. 1003 ¶ 100 (citing Ex. 1003 ¶¶ 49–56 (§ VI)).

In particular, that location corresponds to the end of Rainer’s display driver circuit leading to the first or last output device 70 and display line 67. Therefore, based on the record presented, we disagree with Patent Owner’s argument and Dr. Schubert’s testimony in support that there is “no evidence” to support Dr. Murphy’s testimony on this point. Prelim. Resp. 23; Ex. 2001 ¶ 62.

Further, as discussed below in Section IV.E.2(v)(a), even if one were to locate the input terminal at the opposite end of Reiner’s display driver in Figure 5 (that is, at the bottom of the figure), based on the record presented, we find that a routine re-application of Petitioner’s case for why Figure 5 discloses the claimed positional relationships between two protection circuits and other components of the display device shows those relationships also exist if the input terminal is located at the bottom of the figure. We invite Patent Owner to address this issue in a timely-filed response to the Petition, and emphasize that our findings on this issue are preliminary.

*(c) Conclusion Concerning the Input Terminal Limitation*

We conclude Petitioner’s contentions and Dr. Murphy’s testimony in support as to the input terminal limitation are sufficiently articulated and supported by the evidence in the preliminary record to justify institution of review.

(v) *First and Second Protection Circuits*

The remainder of claim 4 recites that the display device comprises first and second protection circuits to protect the scanning line driving circuit, and specifies various positional relationships between the two protection circuits and other components in the claimed display device. *See* Ex. 1001, 12:33–47.

Petitioner contends Reiner “discloses or renders obvious” these limitations. Pet. 24, 34, 37. We discuss three aspects of this contention separately.

(a) *Whether Reiner’s Figure 5 Illustrates a Driving Circuit Having the First and Second Protection Circuits of Claim 4*

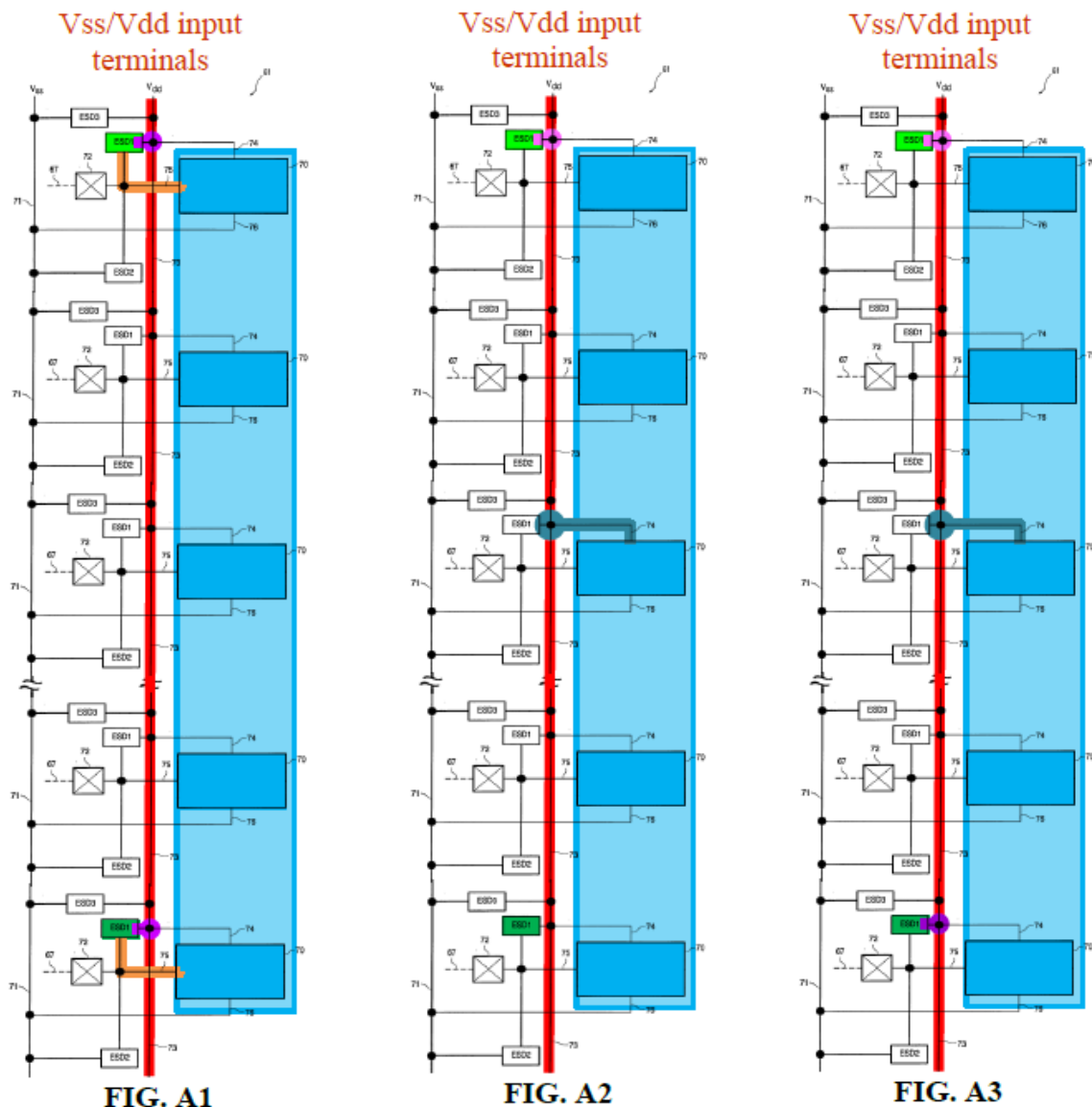
Petitioner contends the display device driving circuit illustrated in Reiner’s Figure 5 includes first and second protection circuits that protect the drive circuit, and those two protection circuits satisfy the various positional relationships specified in claim 4. *See* Pet. 24–29, 34–36, 37–40 (citing Ex. 1005, Fig. 5, 2:2–3, 2:28–3:1, 4:15–16, 8:8–15, 9:11–22, 10:10–17, 12:4–5, 12:23–25); Ex. 1003 ¶¶ 103–111, 121–132. We conclude this contention, which Patent Owner does not oppose at this time,<sup>8</sup> is supported sufficiently by the cited disclosures in Reiner and by Dr. Murphy’s testimony to justify institution of review.

In particular, Petitioner provides three different mappings A, B, and C of claim 4 to Reiner’s Figure 5 that each, in Petitioner’s view, demonstrate how the illustrated circuit includes first and second protection circuits

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<sup>8</sup> We consider Patent Owner’s argument that the display device driving circuit illustrated in Reiner’s Figure 5 is not a *scanning line* driving circuit, as recited in claim 4, below in Section IV.E.2(v)(b).

satisfying the claimed requirements. *See* Pet. 25–28, 34–36, 37–40; Ex. 1003 ¶¶ 106–111, 121–132. We focus here on mapping A, and we reproduce below Dr. Murphy’s Figures A1–A3 that illustrate this mapping. *See* Pet. 28, 35, 38; Ex. 1003 ¶¶ 110, 123, 129.



**Petitioner’s Figures A1–A3 (Annotated by Petitioner’s Expert Witness).**

Figures A1–A3 extend Reiner’s Figure 5, which shows only two output devices 70 for driving two lines 67, to include at least three more devices 70 and lines 67 on the basis that a person of ordinary skill in the art would have

understood there would be as many devices 70 as there are lines in Reiner's display device. *See* Pet. 26; Ex. 1003 ¶ 107.

Based on the preliminary record, which does not contain any opposition from Patent Owner on this point, we agree with Petitioner and Dr. Murphy that the color-coded annotations in Figures A1–A3 demonstrate the illustrates driving circuit exhibits all the protection circuit requirements recited in claim 4. *See* Pet. 27–28, 34–36, 37–39; Ex. 1003 ¶¶ 108, 110, 123–124, 128–130. That is, the annotations identify a first protection circuit (light green, at top) connected to a power supply line (red, via upper purple line in Fig. A1) between a first connecting portion (dark teal line in Figs. A2–A3) and the input terminal (brown, at top), and also connected to the driving circuit (blue, via upper orange line in Fig. A1), to protect the driving circuit (blue). The annotations further identify a second protection circuit (dark green, at bottom) connected to the driving circuit (blue, via lower orange line in Fig. A1) and the power supply line (red, via lower purple line in Fig. A1) to protect the driving circuit (blue). The annotations moreover illustrate how the driving circuit (blue) is connected to the power supply line (red, via dark teal line in Figs. A2–A3) between a second connecting portion (upper purple line in Fig. A3) and a third connection portion (lower purple line in Fig. A3).

Moreover, as mentioned above in Section IV.E.2(iv)(b) in relation to the input terminal limitation, even if one were to locate the input terminal at the bottom end of Figure 5 (instead of at the top end as described above), a routine re-application of Petitioner's case as described above shows the claimed positional relationships continue to exist. In particular, based on this preliminary record, we find that if the “first” protection circuit then is

taken as the dark green circuit at the bottom (instead of the light green circuit at the top), and the “second” protection circuit is then taken as the light green circuit at the top (instead of the dark green circuit at the bottom), with everything else being the same, then the claimed positional relationships continue to exist. Here again, we invite Patent Owner to raise any counterviews on this point in a timely-filed response to the Petition.

*(b) Whether Reiner’s Figure 5 Illustrates a Scanning Line Driving Circuit*

Petitioner also contends the display device driving circuit illustrated in Reiner’s Figure 5 is *disclosed by* Reiner as corresponding to the structural makeup of source/data driver module 61 *and* gate/scanning driver 63. *See* Pet. 24–25, 26 n.9, 29, 34, 37 (citing Ex. 1005, Figs. 4–5, 4:15–16, 9:11–22, 10:10–15, 12:4–5); Ex. 1003 ¶¶ 103–105, 107 n.12, 111, 121–122, 127–128. Patent Owner and Dr. Schubert disagree, and contend Reiner’s Figure 5 is disclosed as illustrating *only* source/data driver module 61, *not* gate/scanning driver 63. *See* Prelim. Resp. 15–21 (citing Ex. 1005, Figs. 4–5, 2:1–3, 3:2–8, 8:1–11, 9:11–10:24, 12:23–25); Ex. 2001 ¶¶ 47–56.

Based on the preliminary record presented, we agree with Patent Owner. Reiner does, as Petitioner argues, disclose that both of its display drivers 61 and 63 are “typical example[s]” of integrated circuit devices that can benefit from utilizing Reiner’s bump bridge technology for providing electrostatic discharge protection, due to the large number of parallel output lines that must cross power supply lines. *See* Ex. 1005, 4:15–16, 9:11–20 (describing Fig. 4), 12:4–5. However, in contrast to those disclosures that treat Reiner’s display drivers 61 and 63 together as a group, Reiner’s description of Figure 5 repeatedly refers *only* to Reiner’s source/data driver

module 61. *See id.* at 9:20–10:23. Based on this record, we conclude Reiner does not *disclose* that Figure 5 illustrates the structural makeup of gate/scanning driver 63.

(c) *Whether Reiner Renders Obvious a Scanning Line Driving Circuit Utilizing the First and Second Protection Circuits of Claim 4*

Petitioner further contends, in the event we find Reiner’s Figure 5 corresponds *only* to Reiner’s source/data driver module 61 (*not* Reiner’s gate/scanning driver 63), then a person of ordinary skill in the art nonetheless would have been motivated to configure Reiner’s gate/scanning driver 63 to include the ESD protection network structure of Figure 5. *See* Pet. 24–25, 29–33, 34, 37; Ex. 1003 ¶¶ 103–105, 112–120, 122, 128.

In support, Petitioner asserts and Dr. Murphy testifies that Reiner aims to provide “integrated circuit devices with ESD protection” “in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event,” wherein a “typical example is an integrated circuit display driver 61 *or* 63.” Pet. 24–25, 29 (citing Ex. 1005, 2:2–3, 2:28–3:1, 4:15–16, 8:8–15, 9:12–14, 12:4–5, 12:23–25); Ex. 1003 ¶¶ 104–105, 111–112. Petitioner and Dr. Murphy cite Reiner’s Figure 5 as illustrating how “ESD protection means can easily be integrated” into Reiner’s source/data driver module 61. Pet. 25 (citing Ex. 1005, 9:20–22); Ex. 1003 ¶ 105.

According to Petitioner and Dr. Murphy, a person of ordinary skill in the art would have understood that the ESD protection network structure of Figure 5 would have “applie[d] equally to” Reiner’s gate/scanning driver 63, because both drivers 61 and 63 are display circuit drivers, and Reiner discloses how both display drivers 61 and 63 can benefit from ESD

protection thereby “teaching, or at least suggesting, that both drivers would be protected in similar fashion.” Pet. 25, 29–32 (citing Ex. 1005, 2:28–3:3, 4:15–19, 6:12–17, 8:30–31, 9:12–14, 9:18–22, 10:10–12, 12:4–5, 12:16–18); Ex. 1003 ¶¶ 105, 111–119.

Thus, Petitioner and Dr. Murphy conclude a person of ordinary skill in the art would have been motivated to configure Reiner’s gate/scanning driver 63 to include the ESD protection network structure of Reiner’s Figure 5, with a reasonable expectation of success. *See* Pet. 30–33; Ex. 1003 ¶¶ 115–120. For example, that structure “would have protected the circuits . . . using a single metal layer [which] would have reduced the cost of fabricating gate driver 63 and made the chip less bulky.” Pet. 32 (citing Ex. 1005, 4:10–12, 4:15–19, 9:16–22, 10:15–17, 12:15–18, claim 11); Ex. 1003 ¶ 118.

Patent Owner argues and Dr. Schubert testifies that Petitioner “fails to show that Reiner . . . renders obvious applying Reiner’s source driver ESD protection network to a gate driver.” Prelim. Resp. 19; Ex. 2001 ¶¶ 53–54. Patent Owner and Dr. Schubert assert Petitioner “mischaracterizes” Reiner’s teachings as indicating that its bump bridge ESD protection technology is well suited for use in both drivers 61 and 63, and instead “[n]othing in Reiner suggests that its gate drivers 63 include an ESD protection network.” Prelim. Resp. 20–21 (citing Pet. 24; Ex. 1005, 8:1–11, 9:23–34, 10:1–24, 12:23–25); Ex. 2001 ¶¶ 55–56. Further according to Patent Owner and Dr. Schubert, “no evidence shows that the gate driver would include an ESD protection network identical to the source driver’s network and include the same number of ESD devices connected in the same way.” Prelim. Resp. 21; Ex. 2001 ¶ 56.

Patent Owner and Dr. Schubert argue Petitioner’s obviousness contentions particularly overlook the fact that Reiner’s source/data driver module 61 and gate/scanning driver 63 perform different functions in different ways when generating a display on LCD screen 60. *See* Prelim. Resp. 20–22; Ex. 2001 ¶¶ 55, 57–59. That is, Reiner’s source/data driver module 61 drives individual source lines 67 in display 60, whereas Reiner’s gate/scanning driver 63 “usually drives one whole gate line 68” in display 60 as controlled by “row timing signals” received from CPU 62 in order “to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time.” Prelim Resp. 20, 21–22 (citing Ex. 1005, Fig. 4, 9:20–34); Ex. 2001 ¶¶ 55, 57–59.

We conclude the preliminary record supports, sufficiently to justify institution, Petitioner’s contention that a person of ordinary skill in the art would have been motivated to configure Reiner’s gate/scanning driver 63 to include the ESD protection network structure illustrated in Figure 5. First, we agree with Petitioner’s position that Reiner discloses *both* of its display drivers 61 *and* 63 would benefit from ESD protection. That is, Reiner describes display drivers 61 and 63 as “typical example[s]” of integrated circuit devices that can benefit from utilizing Reiner’s bump bridge technology for providing ESD protection, due to the large number of parallel output lines that must cross power supply lines. *See* Ex. 1005, 4:15–16, 9:11–20 (describing Fig. 4), 12:4–5. Thus, based on this preliminary record, we disagree with Patent Owner’s position that Petitioner mischaracterizes Reiner’s teachings in this regard.

Second, based on the preliminary record, Dr. Murphy’s testimony that the *ESD protection network structure* of Reiner’s Figure 5 would be suitable

for implementing in Reiner's gate/scanning driver 63 due to similarities between the two drivers is supported by the evidence sufficiently to justify institution. *See* Ex. 1003 ¶¶ 104–105, 111–120. A first similarity is Reiner's indication that both display drivers 61 and 63 “have areas where the output or input metal lines have to cross power supply lines” Vdd and Vss. Ex. 1005, 9:11–20, 12:4–5, Fig. 3 (illustrating exemplary integrated circuit device 30 powered by supply voltages Vdd and Vss). A second similarity is Dr. Murphy's testimony that, at least in some embodiments of Reiner's gate/scanning driver 63, “each of the [scan] lines being driven will have its own semiconductor units . . . [that] drive that particular line,” akin to the individual output devices 70 and source lines 67 of Figure 5. Ex. 1003 ¶¶ 113, 117; *see also* Prelim. Resp. 21–22 (arguing “Reiner [discloses] that the gate driver integrated circuit comprises individual gate drivers” and “a POSITA would understand that individual gate/scan line drivers are coupled to one another”). These similarities between Reiner's display drivers 61 and 63 support Dr. Murphy's conclusion that Reiner's bump bridge technology for providing ESD protection could and would have been implemented in Reiner's gate/scanning driver 63 in the same fashion as illustrated in Figure 5 for Reiner's source/data driver module 61.

We appreciate, as Dr. Schubert testifies, that the individual circuits in gate/scanning driver 63 will drive their respective gate/scan lines 68 in different ways than the individual output devices 70 in source/data driver module 61 will drive their respective source/data lines 67. *See* Ex. 2001 ¶¶ 55–59. Nonetheless, based on the present record, we conclude such differences in the *signal outputs* of Reiner's display drivers 61 and 63 have little to do with the benefits of configuring the *power inputs* of the display

drivers to protect the individual circuits from electrostatic discharge events, or how to do so.

Thus, these signal output differences do not appear to undercut the sufficiency of Petitioner's evidence, for purposes of supporting institution of review. We take note, however, that any final findings on these factual issues may turn on conflicting witness testimony. As such, we take a prudent course and decline to provide detailed preliminary findings on these issues. We will provide detailed findings only as necessary to any final written decision, based on a fully developed trial record.

For the foregoing reasons, we conclude the preliminary record supports, sufficiently to justify institution, Petitioner's contention that a person of ordinary skill in the art would have been motivated to configure Reiner's gate/scanning driver 63 to include the ESD protection network structure of Figure 5.

*(vi) Conclusion as to Claim 4*

We conclude Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 4 is unpatentable as having been obvious over Reiner.

*3. Claims 1–3 and 5–18*

Petitioner provides arguments and evidence in support of contending claims 1–3 and 5–18 are unpatentable as having been obvious over Reiner, including supporting testimony from Dr. Murphy. *See* Pet. 40–71; Ex. 1003 ¶¶ 134–227. Patent Owner opposes, relying on arguments and testimony from Dr. Schubert discussed above in connection with claim 4. *See* Prelim. Resp. 1–2, 24–28; Ex. 2001 ¶¶ 64–80.

“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a). Thus, pursuant to USPTO rules and policy implementing *SAS Inst. Inc. v. Iancu*, 584 U.S. 357 (2018), we “either (1) institute as to all claims challenged in the petition and on all grounds in the petition, or (2) institute on no claims and deny institution.” Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019) (“CTPG”), 5–6, 64.<sup>9</sup> We “will not institute on fewer than all claims or all challenges in a petition.” *Id.* at 5, 64; *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1359–60 (Fed. Cir. 2018) (stating a decision to institute is “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Thus, because we have decided to grant institution on claim 4, we do the same for claims 1–3 and 5–18. *See supra* Section IV.E.2; 37 C.F.R. § 42.108(a); CTPG 5–6, 64. Further, Patent Owner does not address these claims apart from arguments we have considered above in connection with claim 4, so there is nothing further for us to address with respect to these claims at this time. *See* CTPG 5–6, 64.

#### 4. Conclusion as to Ground One

We conclude the record demonstrates a reasonable likelihood that Petitioner would prevail with respect to challenging claim 4 as having been obvious over Reiner, so we grant institution of review on Petitioner’s Ground One.

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<sup>9</sup> Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

*F. Ground Two — Obviousness over Reiner and Takahara*

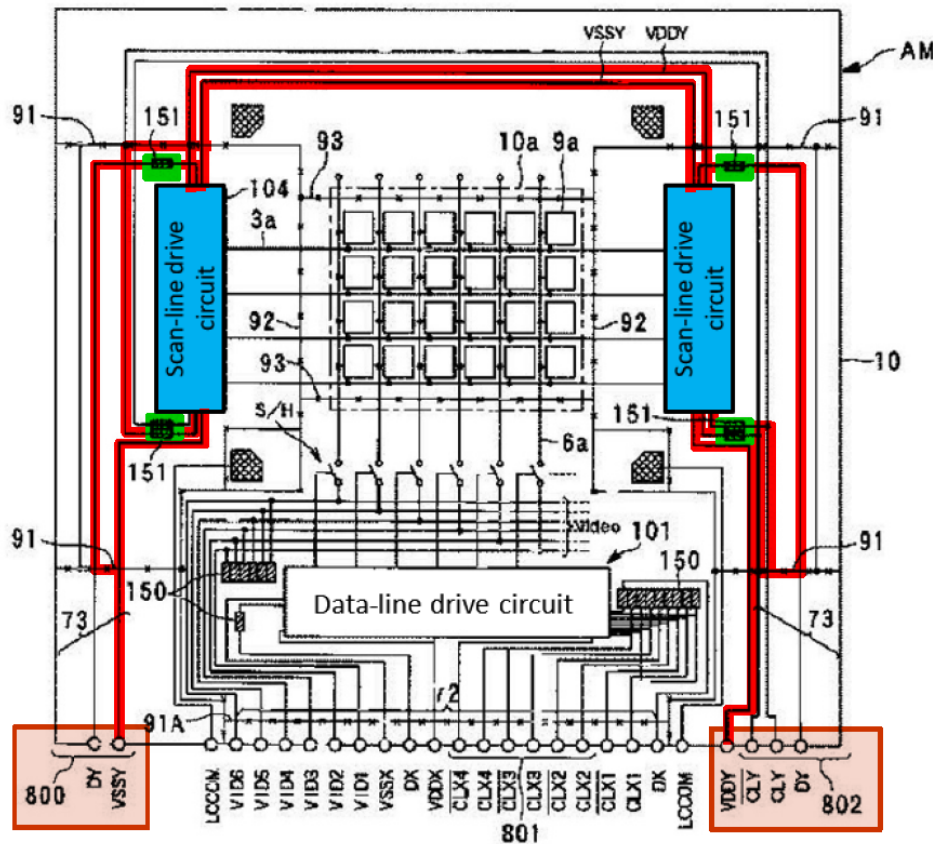
In Ground Two, Petitioner asserts claims 1–18 of the ’157 patent are unpatentable as having been obvious over Reiner and Takahara. *See* Pet. 1–10, 15, 71–89. Patent Owner disagrees. *See* Prelim. Resp. 1–2, 28–39.

As discussed above, because we have decided to grant institution on Ground One, we do the same for Ground Two. *See supra* Section IV.E.3; 37 C.F.R. § 42.108(a); CTPG 5–6, 64. Nonetheless, we will address Patent Owner’s arguments concerning Ground Two separately from Ground One, to provide guidance to the parties for the upcoming trial. *See* CTPG 6, 64.

*1. Whether the Combination of Reiner and Takahara Provides a Protection Circuit Connected to a Scanning Line Driving Circuit and a Power Supply Line*

Ground Two relies on Takahara to shore up potential deficiencies of Ground One. *See* Pet. 71–72. For example, if we determine it would not have been obvious to incorporate ESD protection measures in Reiner’s gate/scanning driver 63 based on Reiner alone in Ground One, then Petitioner cites Takahara as additional evidence of protecting scanning line driving circuits from electrostatic discharge events. *See* Pet. 71–72, 76–80; Ex. 1003 ¶¶ 228, 234–242. In support, Petitioner annotates Figure 1 of Takahara, as reproduced below.

FIG. 1



**Takahara, Figure 1 (Annotated at Pet. 77).**

Figure 1 of Takahara is a block diagram schematically illustrating a drive circuit employed in a liquid crystal display panel. *See Ex. 1007 ¶¶ 57–58.* Petitioner asserts Figure 1 illustrates electrostatic protection circuits 151 (green) “...formed at intermediate positions of the signal lines’ 73, which include power lines VDDY, VSSY” (red), to protect scan line drive circuits 104 (blue). Pet. 76 (emphasis added) (citing Ex. 1007, Fig. 1, ¶¶ 66, 70); Ex. 1003 ¶ 235.

Patent Owner objects that Petitioner’s combination of Reiner and Takahara lacks “a scanning line driving circuit connected to protection circuits, which are also connected to a power supply line,” as required by claim 4. Prelim. Resp. 29, 31–32. Patent Owner argues Reiner falls short of

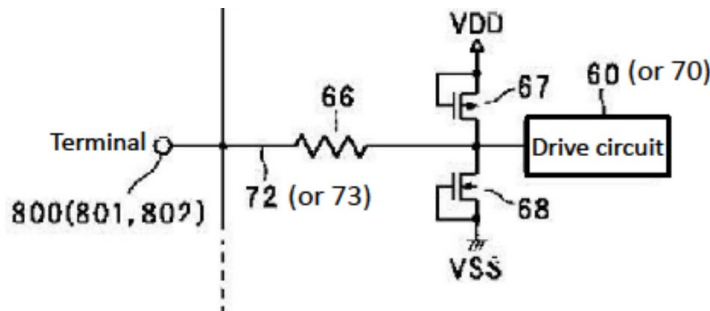
claim 4 because Reiner does not disclose or render obvious a protection circuit *connected to a scanning line driving circuit*, as discussed above in relation to Ground One. *See id.* at 1–2, 28–29, 32; Ex. 2001 ¶¶ 84, 87.

Patent Owner argues Takahara falls short of claim 4 because Takahara does not disclose a protection circuit *connected to a power supply line*. *See* Prelim. Resp. 1–2, 29, 30–31, 32–35; Ex. 2001 ¶¶ 82–83, 85, 87–93. In that regard, Patent Owner and Dr. Schubert assert Petitioner “ignores Takahara’s express disclosures directed to [placing protection circuits on] *signal* lines, not *power* lines,” and “Takahara does not disclose protection circuits [151] connected to the *power supply* lines VDDY and VSSY.” Prelim. Resp. 29, 30–31, 32–35 (citing Ex. 1007, Fig. 1, ¶¶ 4, 24–25, 61–66, 70); Ex. 2001 ¶¶ 82–83, 85, 87–93. Further according to Patent Owner and Dr. Schubert, “Takahara does not disclose *two* protection circuits connected to *one* power supply line to protect the scanning line driving circuit” as claimed. Prelim. Resp. 36; Ex. 2001 ¶ 94.

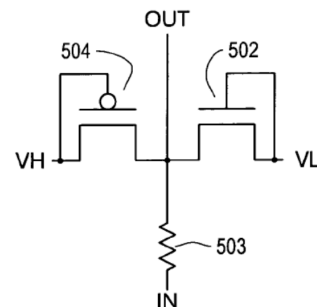
We conclude the preliminary record supports, sufficiently to justify institution, Petitioner’s contention that Takahara’s protection circuits 151 are connected to power lines VDDY and VSSY to protect scan line drive circuits 104 from electrostatic discharge events. In particular, Takahara describes how “various kinds of circuits may be utilized for the electrostatic-protection circuits 150 and 151,” including “the circuit illustrated in FIG. 3” which “utilizes protection resistors 66, and P-channel TFTs 67 and N-channel TFTs 68, which are in a push-pull layout and *constitute diodes between positive power supplies VDD and negative power supplies VSS, respectively.*” Ex. 1007 ¶ 66 (emphasis added); *see also id.*

at Fig. 3 (illustrating how power supplies VDD and VSS are connected to the illustrated circuit).

Indeed, on this preliminary record, the protection circuit illustrated in Figure 3 of Takahara closely resembles the protection circuit illustrated in Figure 4 of the '157 patent, as reproduced below.



**Takahara, Fig. 3 (Excerpt).**



**'157 Patent, Fig. 4.**

Takahara's Figure 3 illustrates protection circuit 151 disposed on signal wiring 72 and comprising resistor 66, P-channel thin film transistor 67 connected to positive power supply VDD, and N-channel thin film transistor 68 connected to negative power supply VSS. *See* Ex. 1007 ¶¶ 2, 66. The '157 patent's Figure 4 illustrates protective circuit ESD1 disposed on a wiring line ("IN" to "OUT") and comprising resistor 503, p-type transistor 504 connected to high potential power source VH, and n-type transistor 502 connected to low potential power source VL. *See* Ex. 1001, 6:3–23.

We also determine Patent Owner's arguments attack Reiner and Takahara separately, when Petitioner's case for obviousness relies on their combined teachings. In particular, Petitioner relies on Takahara only as disclosing that ESD protection circuits may be utilized to protect a scan line drive circuit; Petitioner does not propose incorporating Takahara's ESD protection structure into Reiner's gate/scanning driver 63. *See* Pet. 76–80.

Petitioner in fact proposes incorporating the ESD protection structure of Reiner's Figure 5 into Reiner's gate/scanning driver 63. *See id.* at 78–80. As discussed above in Section IV.E.2(v)(a) in connection with Ground One, Reiner's Figure 5 illustrates a driving circuit having first and second protection circuits satisfying the various positional relationships specified in claim 4, including connections to the driving circuit and the power supply line.

Thus, we conclude the preliminary record supports, sufficiently to justify institution, Petitioner's contention that the combination of Reiner and Takahara provides protection circuits connected to a scanning line driving circuit and a power supply line, as required by claim 4.

2. *Whether There is a Motivation to Combine Reiner and Takahara*

Patent Owner also argues Petitioner “cites no reason to add additional protection circuits, akin to Takahara's” to Reiner's display drivers, “because Reiner's ESD protection network already protects source driver 61.” Prelim. Resp. 36–37. This argument is unavailing on the present record. As discussed above, Petitioner proposes utilizing ESD protection structures in Reiner's gate/scanning driver 63 (not Reiner's source/data driver module 61 as Patent Owner suggests), by incorporating the ESD protection structure of Reiner's Figure 5 (not Takahara's ESD protection structure, as Patent Owner suggests).

## V. CONCLUSION

For the reasons provided above, we decline to deny institution pursuant to 35 U.S.C. § 314(a) and *Fintiv*, and we determine the information presented in the record demonstrates a reasonable likelihood that Petitioner

would prevail with respect to at least one claim of the '157 patent challenged in the Petition. Therefore, we institute an *inter partes* review of all challenged claims 1–18 on all grounds presented in the Petition. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(a).

At this preliminary stage, the Board has not made a final determination with respect to the patentability of the challenged claims or any underlying factual or legal issue. The Board's final determination will be based on the record as developed during the *inter partes* review. Any arguments not raised by Patent Owner in a timely-filed response may be deemed waived.

## VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–18 of the '157 patent on all grounds presented in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

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