

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2024-00973
U.S. Patent No. 9,184,157

PATENT OWNER'S RESPONSE

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2001	Declaration of E. Fred Schubert, Ph.D., in support of Patent Owner's Preliminary Response
2002	Declaration of Emily J. Tremblay in Support of Motion for Pro Hac Vice Admission
2003	Declaration of William R. Jones in Support of Motion for Pro Hac Vice Admission
2004	Patent Owner's Notice of Deposition of Dr. Patrick Murphy (marked during deposition) <i>*previously filed as Paper 12*</i>
2005	Annotated screenshot of <i>Reiner</i> Figure 5
2006	Image of Circuit with Red Annotation Box, Bates No. BOE_Tech_00040165
2007	Image of Circuitry, Bates No. BOE_TECH_00040167
2008	Transcript of March 7, 2025 Deposition of Dr. Patrick Murphy
2009	Declaration of E. Fred Schubert, Ph.D., in support of Patent Owner's Response

I. PATENT OWNER’S OPPOSITION TO INSTITUTED GROUNDS

Patent Owner 138 East LCD Advancements Limited (“138 East” or “Patent Owner”) submits its Response to the Petition for *Inter Partes* Review of U.S. Patent No. 9,184,157 (“the ’157 patent”). Paper 1 (“Petition” or “Pet.”). Petitioner BOE Technology Group Co., Ltd., challenges the validity of claims 1-18 of the ’157 patent.

Petitioner bears “the burden of proving a proposition of unpatentability by a preponderance of the evidence.” 35 U.S.C. § 316(e). Petitioner has failed to meet its burden. The asserted references, alone or in combination as presented in the Grounds, do not disclose all limitations of any challenged claim. *Reiner* and *Takahara* provide protection circuit arrangements distinct from those claimed in the ’157 patent: *Reiner* discloses an ESD protection network internal to an integrated circuit, and *Takahara* does not disclose more than one protection circuit connected to a signal line (much less a power supply line). Neither reference, alone or in combination, renders obvious the invention: a scanning line driving circuit connected to a power supply line *between* two protection circuits connected to that line. The Board therefore should find in favor of Patent Owner and determine all challenged claims not unpatentable.

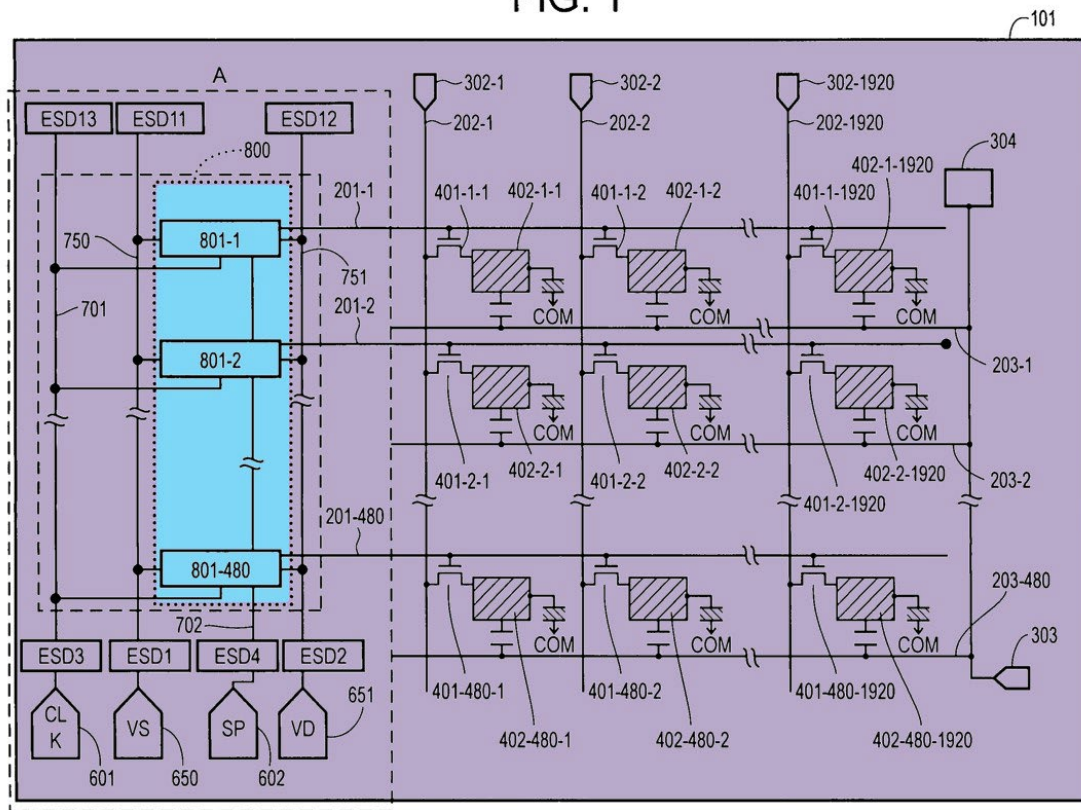
II. THE '157 PATENT

The '157 patent, titled “Semiconductor Device, Display Device, and Electronic Apparatus,” describes a “semiconductor device, display device and electronic apparatus” including improved measures to protect display circuitry from electrostatic damage when a high voltage caused by static electricity or “various noise phenomenon[a]” is “unintentionally applied to the inside of the device.” Ex. 1001, 1:10-16.

The '157 patent's improved ESD protection measures are specifically directed to “a display device having a driving circuit provided on an active matrix substrate.” *Id.*, 1:10-13. The driving circuit “in the scope of the claims” is a scanning line driving circuit that is “formed by integrating polysilicon thin film transistors [TFTs] on the active matrix substrate.” *Id.*, 5:20-28. A display device in which the driving circuit is formed directly on the active matrix display substrate (“TFT driving circuit”) is different than a display device in which the driving circuit is a “general semiconductor device”—an integrated circuit formed on a silicon wafer. In a display device including a TFT driving circuit, the driving circuit is formed as part of the active matrix substrate on which the TFTs that control each pixel of, for example, an LCD display are formed.

For example, Figure 1 shows a **scanning line driving circuit 800** formed on the **active matrix substrate 101**, which supplies driving signals to scan lines 201, which are connected to pixel switching elements 401:

FIG. 1

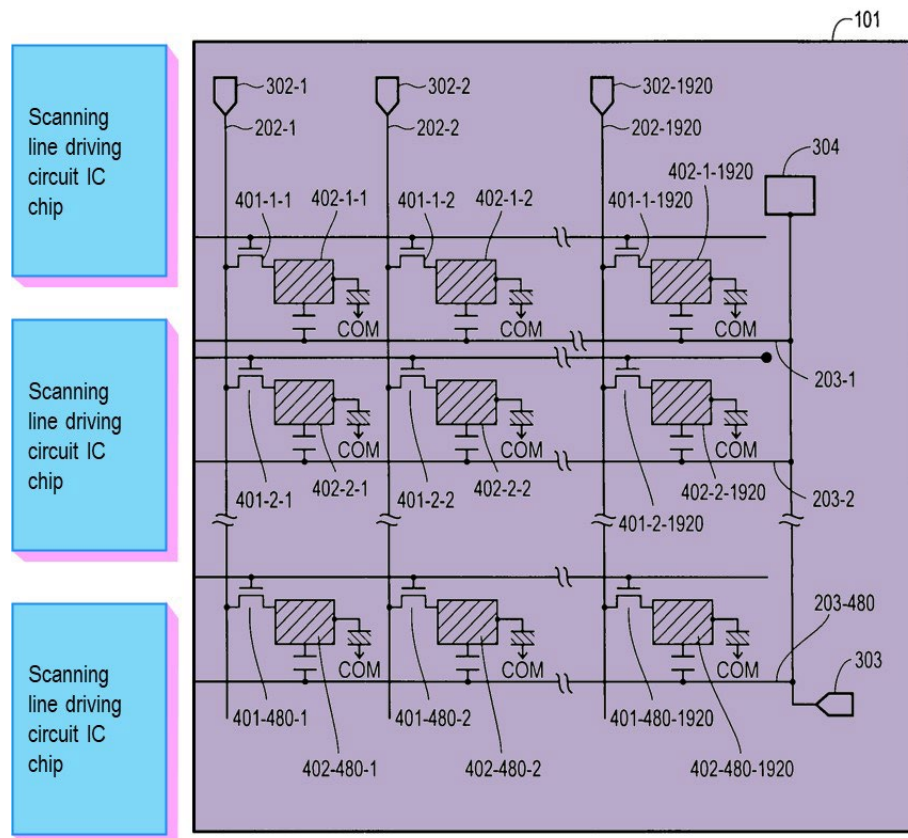


Id., Fig. 1.¹

In a display device in which the scanning line driving circuit is not a TFT driving circuit, the scanning line driving circuitry exists in a discrete integrated circuit chip (“IC chip”), or multiple IC chips, and the driving circuitry of each IC chip is formed on a silicon substrate. Ex. 2009¶36. In this type of display device,

¹ All colors and colored annotations added to Figures unless otherwise noted.

the silicon substrate of the driving circuit IC chips is different than the display substrate, typically a glass substrate, on which the pixel electrodes and associated transistors (TFTs), and the data and scan lines, are formed. *Id.* The following modified figure based on Figure 1 of the '157 patent shows an example of such a display device with three scanning line driving circuit IC chips that are formed on silicon substrates separate from the display substrate (typically a glass substrate) on which the pixel electrodes and transistors (TFTs), scan and data lines, etc., are formed.



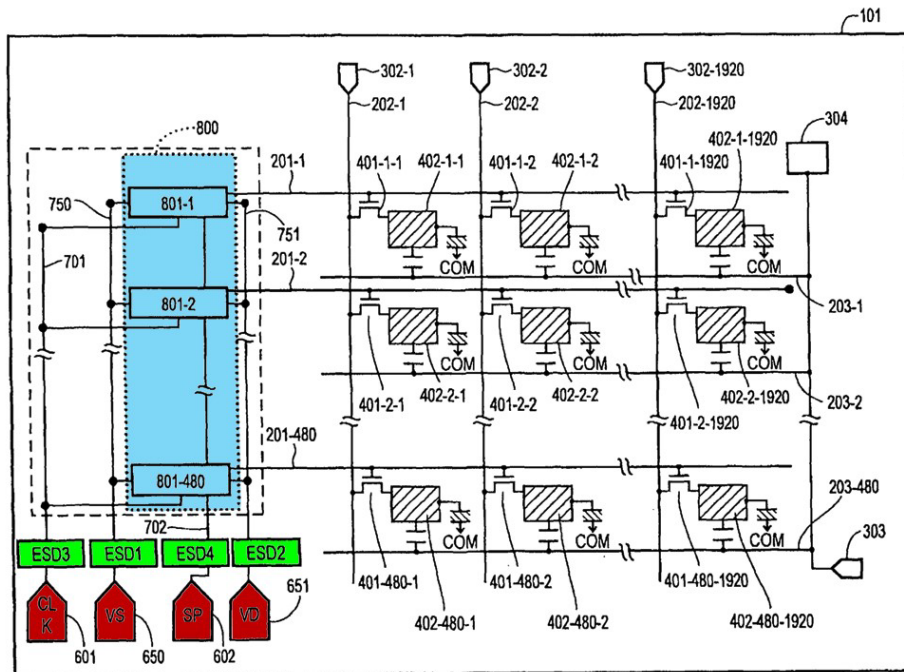
Id.

Regarding ESD protection, the '157 patent explains that for “general semiconductor devices” formed on a silicon wafer there is “little chance[]” of an ESD event occurring within the IC chip semiconductor device because the silicon wafer is conductive. Ex. 1001, 1:23-28. The “key issue to prevent” ESD events in an IC chip semiconductor device formed on a silicon wafer is therefore to prevent high voltage from entering the device via its input terminals. *Id.* The conventional solution to prevent high voltage from entering the semiconductor device and thus ESD damage inside the device is to place protection circuits between the input terminals and the semiconductor device. *Id.*, 1:28-32.

In contrast, the '157 patent explains that a display device where the active matrix circuitry (e.g., a scanning line TFT driving circuit) is formed directly on the display substrate (typically glass) is subject to different ESD problems because, unlike semiconductor devices formed on silicon (IC chips), the driving circuits are formed on an insulating substrate. *Id.*, 1:33-39. Due to the insulating substrate, ESD damage to the internal circuitry is more likely because static electricity can easily occur during the manufacturing process, and it is more difficult for such charges to escape as compared to a semiconductor device formed on a silicon substrate. *Id.*, 1:33-39, 2:33-35.

The '157 patent explains that existing layouts for protecting display devices with, for example, a scanning line TFT driving circuit, from ESD damage use the

same method used to protect IC chips: “only protective circuits for preventing the static electricity from [entering via] the input terminals are built in” to protect the driving circuit from ESD damage. *Id.*, 1:47-54, 2:20-30. Figure 11 shows the conventional art for protecting a **scanning line driving circuit 800**, comprising **protection circuits ESD1 to ESD4** placed between the **input terminals 601, 602, 650, and 651** and the **scanning line driving circuit 800** to protect the scanning line driving circuit from static charges entering via the input terminals:



Id., Fig. 11.

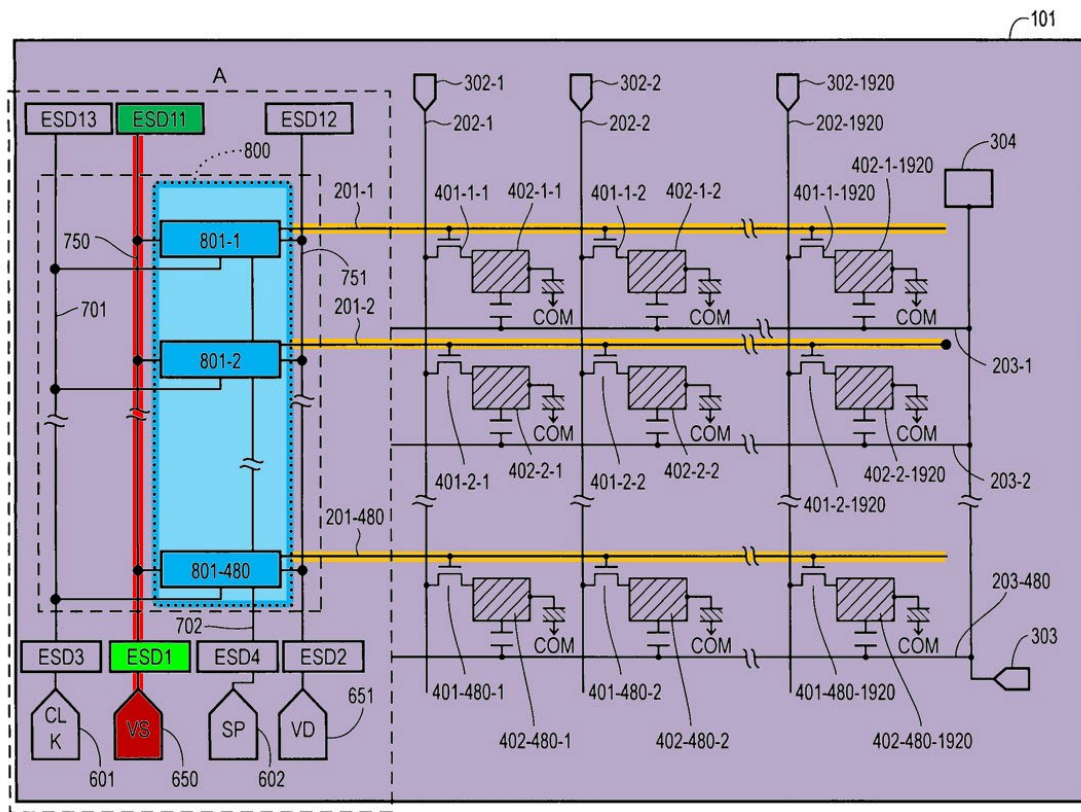
The '157 patent explains that because the driving circuit is formed on an insulating substrate, “it is difficult for charges to escape as compared to the circuit on [a] silicon wafer, and it is easy to be electrified.” *Id.*, 2:33-50. Furthermore,

because “the area of [a TFT driving circuit] is larger as compared to the IC formed on a general silicon wafer,” the ESD protection circuits located after the input terminals are insufficient to protect the driving circuitry located far from the input terminals from ESD events, particularly during the manufacturing process. *Id.* Specifically, “since there is a possibility that the static electricity is electrified on a certain location on the substrate during the manufacturing process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation.” *Id.*; *see also id.*, 3:67-4:13 (“when an active matrix used in a TFT-LCD or TFT-OLED and a driving circuit thereof are formed on the insulating substrate, the driving circuit is configured to surround the active matrix, so that it becomes larger and accordingly its line is also lengthened”).

To address these problems, the '157 patent discloses and claims placing ESD protection circuits on both ends of the scanning line driving circuit. ESD protection circuits ESD1 to ESD4 are disposed between input terminals and the scanning line driving circuit, to protect the scanning line driving circuit from charges entering via the input terminals. And ESD protection circuits ESD11 to

ESD13 are disposed at the far end of the opposite side of the scanning line driving circuit relative to the input terminals. *Id.*, 5:44-6:2.

For example, as shown below for protecting the scanning line driving circuit 800 from charges entering via the low potential power source line 750, the **scanning line driving circuit 800** composed of **driving unit circuits 801** is formed on the **active matrix substrate 101** and the **driving unit circuits 801** are connected to **scan lines 201** to supply a driving signal. The pixel switching elements 401 are connected to the **scan lines 201** and data lines 202. The **low potential power source line 750** is connected to the **scanning line driving circuit 800** and the **low potential power source terminal 650**. A **first protection circuit ESD1** is connected between the **low potential power source terminal 650** and the **low potential power source line 750**, and a **second protection circuit ESD11** connected to the **low potential power source line 750** is “disposed at [the] far end of the opposite side” from the **input terminal 650** “with a **scanning line driving circuit 800** therebetween”:



Id., Fig. 1; 4:60-5:65.

The '157 patent explains that ESD1 prevents the scanning line driving circuit 800 from being damaged when excess charges are input from the low potential power supply terminal 650. *Id.*, 5:50-54. And ESD11 prevents static charges generated “during manufacturing [of] the active matrix substrate” from entering the scanning line driving circuit 800 via the opposite end of the low potential power supply line 750 with respect to its supply terminal 650 and damaging portions of the scanning line driving circuit “located far from a terminal.” *Id.*, 5:61-65.

Independent claims 4 and 17, for example, recite this improved ESD protection scheme:

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Id., 12:25-47.

17. A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

Id., 14:16-43.

The '157 patent explains that placing the scanning line driving circuit between protection circuits in this manner confers an additional benefit because the protection circuits on either side of the scanning line driving circuit may be

“arranged at corners far from the input terminals among four corners of the active matrix” which makes it “possible to arrange large-sized protective circuits without making the peripheral area [of the active matrix substrate—i.e., the portion of the substrate that does not include pixels] large.” *Id.*, 4:14-19. In particular, arranging the second set of protection circuits “at the corner part of the active matrix substrate, particularly at the corner opposite to the input terminals” enables the scanning line driving circuit to be protected without “making the substrate area larger.” *Id.*, 5:65-6:2.

Dependent claim 8, for example, recites this improved ESD protection scheme:

8. The display device as set forth in claim 4, further comprising:
a substrate,
the scanning line driving circuit being arranged on the
substrate,
the power supply line being formed over first and second
corner portions of the substrate so as to follow a
periphery of the substrate,
the first protection circuit being arranged in the first corner
portion of the substrate, and

the second protection circuit being arranged in the second
corner portion of the substrate.

Id., 12:58-13:2 (emphasis added).

III. CLAIM CONSTRUCTION

Patent Owner contends that the claims should receive their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art. 37 C.F.R. § 100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

IV. LEGAL STANDARD

“In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.” 35 U.S.C. § 316(e).

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) as of the priority date of the ’157 patent would have had at least a bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least four years of experience designing semiconductor display devices, including LCD displays; a master’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays; or a Ph.D. in electrical engineering, computer science, physics, or a

similar field and at least one year of experience designing semiconductor display devices, including LCD displays. Ex. 2009 ¶¶19-23.

VI. THE PETITION DOES NOT ESTABLISH UNPATENTABILITY BY A PREPONDERANCE OF THE EVIDENCE.

A. *Reiner* does not render obvious claims 1-18 (Ground 1).

1. *Reiner*: Overview

Reiner relates to “integrated circuit devices with ESD protection” and, in particular, forming “bump bridges” that provide low-ohmic interconnections within an integrated circuit device including one metallization layer. Ex. 1005, 2:1-3; Ex. 2009 ¶48.

Reiner addresses a different problem than the ’157 patent: it teaches bump bridges to facilitate interconnections in an integrated circuit device comprising a silicon substrate and including a single metallization layer, providing a solution that saves space and money compared to alternatives. *See, e.g.*, Ex. 1005, 4:10-5:2. “The higher the integration density of these integrated circuit devices gets, the more difficult it is to realize the routing of all the necessary interconnections inside a single metallization layer.” *Id.*, 2:7-9. “In situations where the routing cannot be realized with a single metallization layer, one currently has two options. Either, a few polysilicon interconnections are provided where necessary, or another metallization layer is added.” *Id.*, 2:11-13. Each has its disadvantages: “polysilicon

interconnections usually are relatively big thus occupying part of the device's surface area that otherwise would be available for integrated devices,” and a second metallization layer is expensive. *Id.*, 2:16-21; Ex. 2009 ¶49.

As one application of its bump-bridge solution, *Reiner* describes integrated circuit devices including ESD protection networks. ESD protection networks “prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event,” for example, when someone touches the chip's pins (input and output points). Ex. 1005, 2:28-3:3. *Reiner* describes an ESD protection network comprising (1) “protection diodes and/or transistors,” and (2) low-ohmic “metal interconnection lines for connecting these diodes and/or transistors with inputs and/or outputs of the integrated circuit device to be protected.” *Id.*, 3:4-8. *Reiner* teaches using its bump-bridge arrangements to avoid needing to use a polysilicon interconnection or two metallization layers where lines need to cross. *Id.*, 3:8-13. Figure 2 shows that a “bump bridge crosses another metal line that is situated within the metallization level, without making contact to this metal line.” *Id.*, 4:32-33.

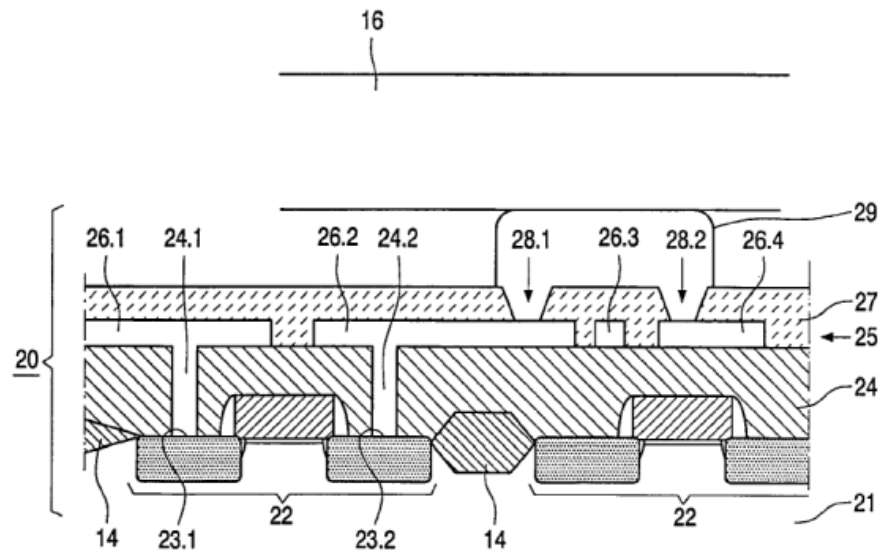
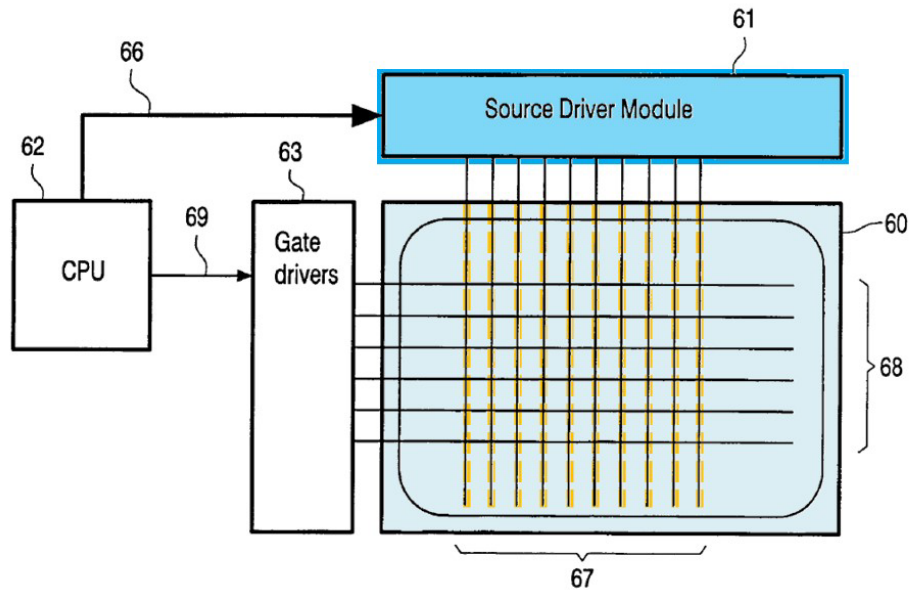


FIG. 2

Id., Fig. 2 (showing bump bridge 29); *see also* Ex. 2009 ¶50.

Relevant here, *Reiner* discloses an “integrated circuit display driver” to “drive many lines of an LCD display.” Ex. 1005, 9:11-22. *Reiner* Figure 4 shows a schematic block diagram including an LCD display and external integrated circuit display drivers. The LCD display comprises LCD screen 60, a plurality of source lines 67, and a plurality of gate lines 68. *Id.*, 9:24-26. Figure 4 also includes a source driver 61 to drive a plurality of source (i.e., data) lines 67, gate driver 63 to drive a plurality of gate (i.e., scan) lines 68, and CPU 62 that provides video

signals to the source driver 61 via bus 66 and row timing signals to gate driver 63 via bus 69:²

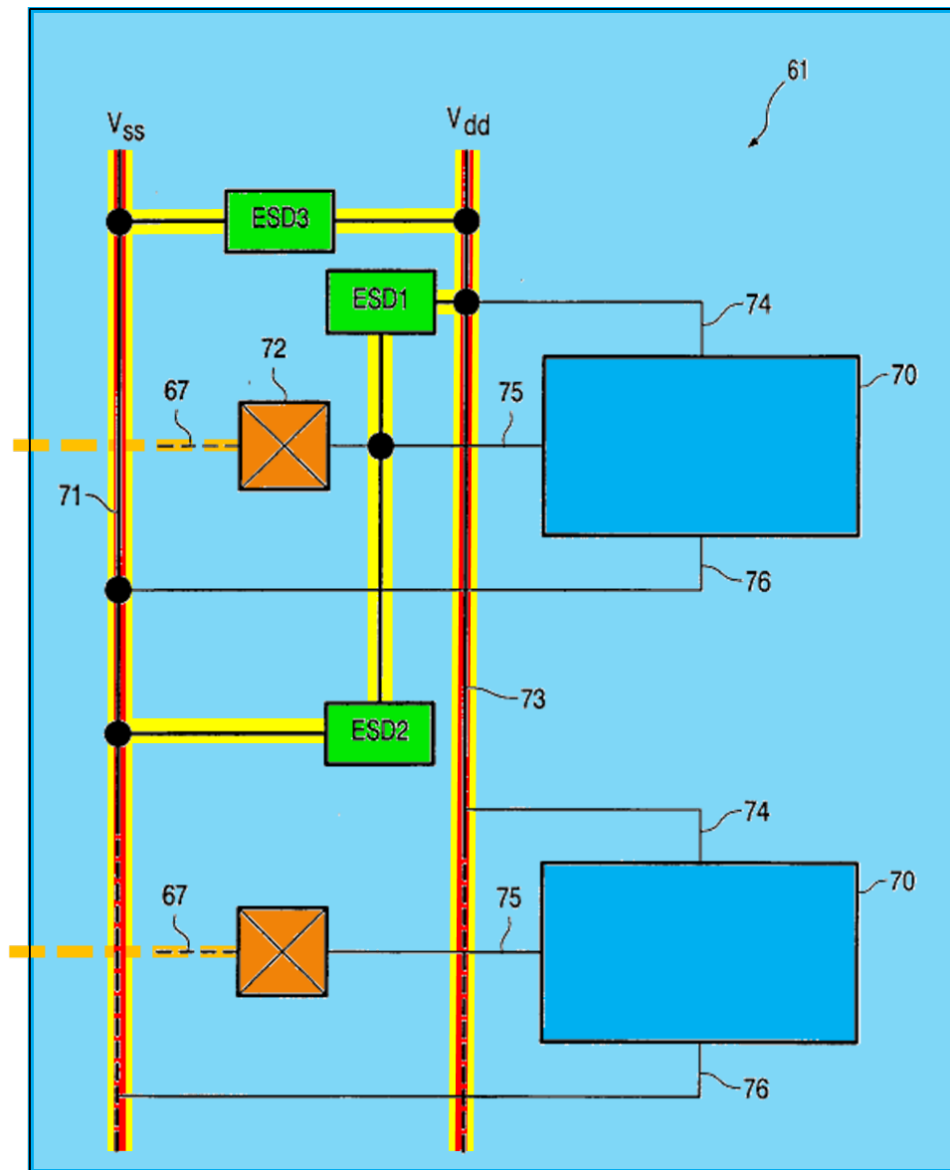


Id., Fig. 4, 9:23-35; *see also* Ex. 2009 ¶51.

Reiner describes, and Figure 5 shows, “ESD protection means” “integrated into” source driver 61. Ex. 1005, 9:21-22. *Reiner*’s **source driver 61** includes “an array of several parallel **output devices 70**,” which “drive the **source lines 67** with the voltages needed by each pixel of the LCD screen 60.” *Id.*, 10:1-24. Each output device 70 includes an output 75, which is connected to a **source line 67** via a **contact pad 72**. *Id.* (source lines 67 connected to contact pad “by means of bonding”). A **power supply line 73** provides the supply voltage Vdd to the **output**

² A POSITA would understand that “source” lines and “data” lines refer to the same lines, and “gate” lines and “scan” lines refer to the same lines. The respective terms are interchangeable. Ex. 2009 ¶52, n.2.

devices 70 via connection 74, and a second **power supply line 71** provides the supply voltage Vss to the **output devices 70** via connection 76. *Id.* Three ESD devices, **ESD1**, **ESD2**, and **ESD3**, “are provided for each **output device 70** . . . to protect the circuitry inside the **devices 70**.” *Id.* **ESD1** is connected between the output line 75 and the **power supply line 73** (Vdd); **ESD2** is connected between the output line 75 and the **power supply line 71** (Vss); and **ESD3** is situated between the two **power supply lines 71** and **73**. *Id.* “The ESD devices may comprise diodes, transistors and other circuits that are suited to provide for a low-ohmic path to a terminal (e.g., a ground terminal) in case of a voltage peak.” *Id.*, 10:15-17. Figure 5 shows low-ohmic paths in bold (highlighted in yellow). *Id.*, 10:19.



Id., Fig. 5; *see also* Ex. 2009 ¶52.

Reiner therefore discloses “ESD protection means” *inside* a source driver integrated circuit, to protect the circuitry within output devices 70 within the integrated circuit. Ex. 1005, 10:10-12; *see also* Ex. 2008 (Transcript of Deposition of Patrick Murphy, Ph.D., March 7, 2025), 98:13-99:15 (agreeing that all components shown in Figure 5 are part of source driver 61), 139:3-10 (testifying

that “it is reasonable to understand [ESD1, ESD2, and ESD3] to be within conceptually the box labeled source driver module” in *Reiner* Figure 4).

Specifically, the ESD devices protect against electrical charges that may enter the output device via contact pads 72. *Reiner* explains that IC chips, like source driver 61, often comprise ESD protection “to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event. This might happen for example when somebody induces a voltage peak in the circuitry by touching the pins of the chip.” Ex. 1005, 2:28-3:3. *Reiner* further explains that ESD protection networks within IC chips, like source driver 61, “comprise[] protection diodes and/or transistors and metal interconnection lines for connecting these diodes and/or transistors with *inputs and/or outputs of the integrated circuit device to be protected.*” *Id.*, 3:4-8 (emphasis added). In short, *Reiner* describes an ESD protection network inside an integrated circuit for protecting the IC chip’s internal circuits from electrical charges that could enter the IC chip through its input and/or output terminals. Ex. 2009 ¶53.

In *Reiner*’s source driver 61, the ESD protection network protects the individual outputs 70 from electrical charges that could enter the IC chip through its contact pads or pins. *Reiner* does not disclose input pins on the source driver 61 IC chip. Ex. 1005, 9:11-10:23. *Reiner* discloses only contact pads 72, for

connecting the source driver's outputs 75 to the source lines on the LCD display 60. *Id.*, 10:4. Figure 5 shows no other inputs/outputs. *Id.*; *see also* Ex. 2009 ¶54.

2. *Reiner* does not disclose or render obvious all limitations of any challenged claim.

a. Claim 4³

i. *Reiner* does not disclose or render obvious a display device comprising “an input terminal connected to the power supply line to supply power” (claim 4[c]).

According to the Petition, *Reiner* discloses integrated circuit drivers (e.g., source driver 61) including power supply lines and thus renders obvious “an input terminal connected to the power supply line to supply power” as part of the integrated circuit driver. Ex. 1001, claim 4[c]. But input terminals for *Reiner*'s source driver 61 would *not* be input terminals for a display device. Drivers 61 and 63 are not formed on the display substrate (in *Reiner*, LCD display 60)—a POSITA would understand that the display device would include *separate* power supply lines on the display substrate. Ex. 2009 ¶¶56-61.

Thus, even if *Reiner* renders obvious input terminals connected to lines Vdd and Vss, those input terminals would be input terminals for integrated circuit driver 61 (*Reiner* Figs. 4 and 5). The Petition does not assert otherwise. Pet., 21-22. The

³ Claims 4-18 are addressed before claims 1-3 to follow the order in which the Petition presents Ground 1.

Petition asserts only that *Reiner* suggests input terminals because a POSITA would have understood that “gate driver 63 or source driver 61 (each an integrated circuit 20)” would require input terminals “to drive” the output devices 70 within each integrated circuit. Pet., 21. Similarly, the Petition asserts that a POSITA would have found it obvious “to provide input terminals to supply the voltages Vss/Vdd to *Reiner*’s power supply lines of the gate driver 63” because “there would need to be an input terminal to create a connection between the power lines Vdd/Vss of the scanning line driving circuit [i.e., the gate driver 63 integrated circuit device or devices] and the power source for the LCD display.” *Id.*; *see also* Ex. 2008, 98:13-99:15 (referring to *Reiner*, agreeing that all components shown in Figure 5 are part of source driver module 61), 104:15-105:7 (a POSITA would understand that input terminals would be located where the “Vss” and “Vdd” labels are in Figure 5).

Nothing in *Reiner* suggests that lines Vss and Vdd also supply power to the LCD display 60. Indeed, a POSITA would understand that LCD display 60 may include separate input terminals for separate power supply lines, because LCD display 60 is formed on a separate substrate. Indeed, Dr. Murphy appears to acknowledge that LCD display 60 and its separate substrate could include separate power supply lines and corresponding input terminals. Ex. 1003 ¶101; Ex. 2009 ¶60.

Thus, *Reiner* does not disclose or render obvious a display device comprising “an input terminal connected to the power supply line to supply power.”

- ii. ***Reiner* does not disclose or render obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed (claims 4[d], 4[e] and 4[f]).**

Reiner does not disclose or render obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged as claimed. Ex. 1001, claim 4[d-f]. The Board agrees that *Reiner* does not disclose protection circuits connected to a scanning line driving circuit. Paper 9, 32-33. *Reiner* discloses, and the Petition cites, only an ESD protection network within a source (data line) driver IC chip. And the Petition fails to show that *Reiner* renders obvious applying *Reiner*’s source driver ESD protection network to a gate driver. See Ex. 1001, claim 4[d-f]. Differences between a source driver and a gate (scan line) driver would require changes to *Reiner*’s ESD protection network. See Ex. 2009 ¶¶62-68.

No evidence shows that the gate driver would include an ESD protection network identical to the source driver’s network and include the same number of ESD devices connected in the same way. The Petition ignores *Reiner*’s disclosure

that the gate driver integrated circuit comprises individual gate drivers, not output devices 70. Ex. 1005, 9:20-31; Ex. 2009 ¶¶64-65.

To the contrary, a POSITA would expect to see differences between the gate driver arrangement and the source driver arrangement. Ex. 2009 ¶66. For example, a POSITA would understand that individual gate/scan line drivers are coupled to one another, to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time. *Id.* This coupling between individual gate/scan unit drivers is not, however, required for source/data unit drivers because each individual source/data driver transmits image data signals simultaneously to each vertical column of a display. *Id.*

A POSITA would not assume that Figure 5—including its ESD protection network—applies, without alterations, to a gate driver. First, the two types of drivers are functionally different in fundamental ways. Specifically, the individual gate line unit driving circuits must communicate with the two neighboring unit drivers so that the ensemble of gate line unit driving circuits can operate as a shift register. *Id.* ¶67. Second, the two driver structures have a fundamentally different architectures. The source line unit drivers are independently operating drivers. But the gate line drivers are coupled and coordinated so that only one gate line at a time will provide an ON signal to a row of pixels and associated switching TFTs. *Id.* Furthermore, whereas the source line drivers provide analog image information

signals, the gate line drivers provide two-state, digital ON and OFF signals. *Id.* These differences demand different wiring layouts, affecting the ESD protection network that *Reiner* provides only in the source driver context. Third, the source drivers drive all data lines at all times, whereas the gate drivers drive, sequentially, one gate line at a time. A POSITA would not assume, based on *Reiner*'s limited disclosure, that a specific ESD protection arrangement for a source driver would work as ESD protection for a gate driver. *Id.*

In short, a POSITA would understand that a source driver and a gate driver would have different layouts, functions, and operations (e.g., analog versus digital). *Reiner* does not disclose or suggest that source driver 61's internal ESD layout would, or even could, apply to a gate driver. *Id.*

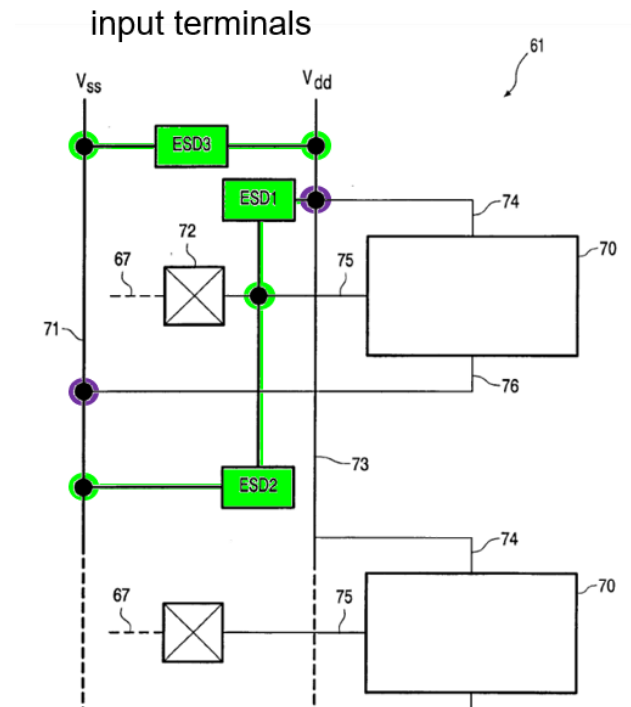
Thus, *Reiner* does not disclose or render obvious "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit" and arranged with respect to the scanning line driving circuit and power supply line as claimed in 4[e] and 4[f].

- iii. **The Petition does not show that *Reiner* discloses or renders obvious a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal” (claim 4[e]).**

If the Board accepts that *Reiner* renders obvious input terminals located at the top of *Reiner*'s Figure 5, and accepts that *Reiner*'s source driver teachings apply to *Reiner*'s gate driver, then *Reiner* discloses at most one protection circuit “being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal”—specifically, ESD3. And the Petition offers no evidence—and specifically *avoids* creating evidence—that ESD3 is “connected to the scanning line driving circuit.” *See* Ex. 1001, claim 4[d]. Thus, the Petition does not show that *Reiner* discloses the claimed first protection circuit. Ex. 2009 ¶¶69-74.

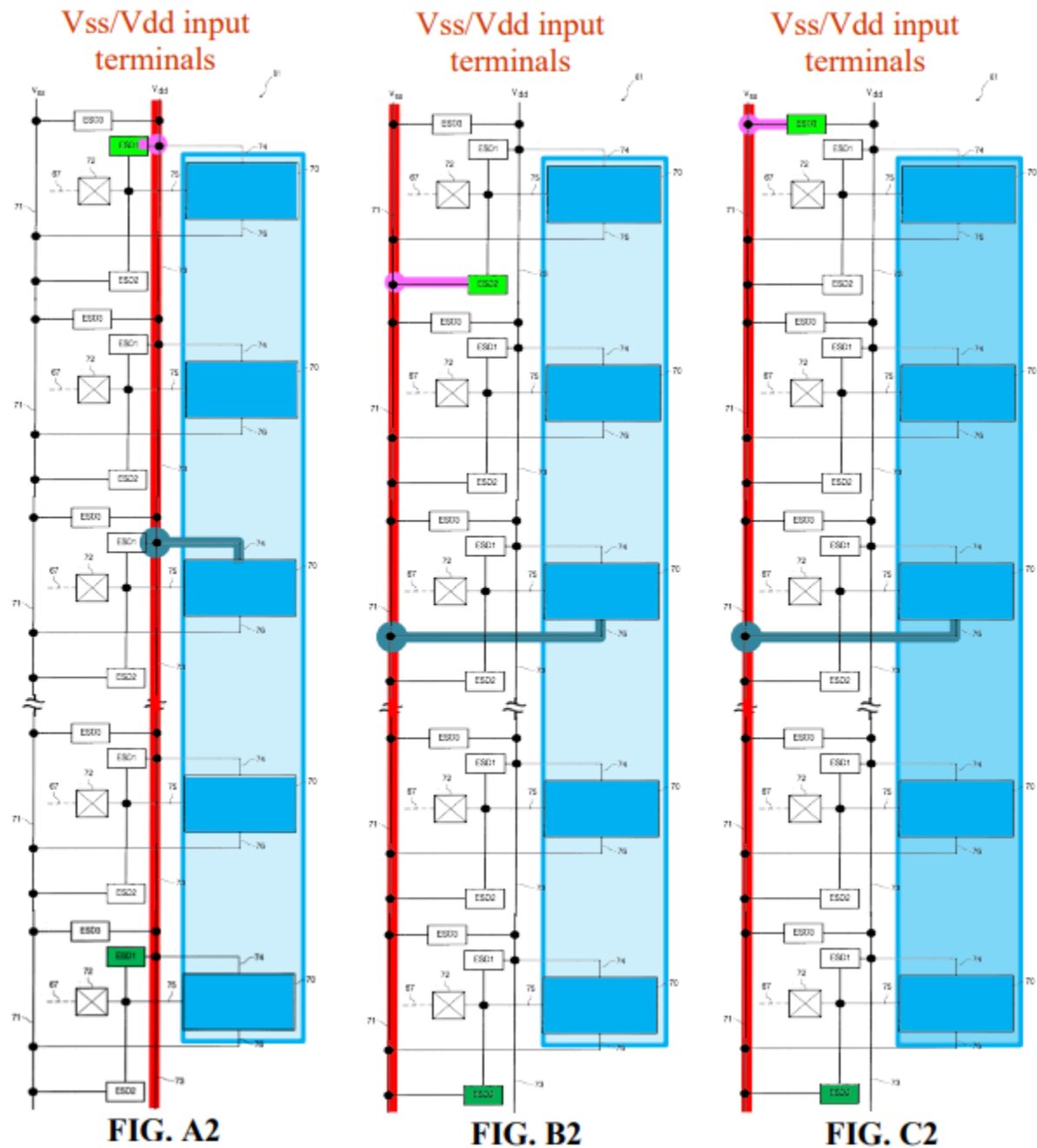
ESD1 and ESD2 are not connected to the power supply line as claimed—namely, *between* the scanning line driving circuit's connection to the power supply line and the power supply line input terminal. Rather, ESD1 is connected to line Vdd *at the same location* at which the source driver first connects to line Vdd. That arrangement does not satisfy the plain language of the claim requiring that the protection circuit be connected to the power supply line *between* (i) a first

connecting portion at which the scanning line driving circuit (in Reiner, source driver) and the power supply line are connected and (ii) the input terminal. *Id.* ¶74. Likewise, ESD2 is not connected to the power supply line *V_{ss}* *between* (i) a first connecting portion at which the scanning line driving circuit (in Reiner, source driver) and the power supply line are connected and (ii) the input terminal, either. *Id.* Rather, the source driver and line *V_{ss}* are connected to one another *between* the purported input terminals and ESD2's connection to line *V_{ss}* (purple identifying scanning line driving circuit connections):



Ex. 1005, Fig. 5. Neither ESD1 nor ESD2 is connected to the power supply line *between* (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal. Ex. 2009 ¶74.

The Petition contends that “a first connecting portion at which the scanning line driving circuit and the power supply line are connected” may be *any* connecting portion at which an output device 70 and line Vdd or Vss are connected—specifically, any of lines 74 and 76 in Reiner Figure 5 for any of output devices 70. Indeed, in Dr. Murphy’s composite images using multiple copies of Reiner Figure 5, Dr. Murphy appears to choose “a first connecting portion at which the scanning line driving circuit and the power supply line are connected” in the middle of the annotated images:



Ex. 1003 ¶123 (dark blue highlighting Dr. Murphy’s selection of “a first connecting portion at which the scanning line driving circuit and the power supply line are connected”); Ex. 2009 ¶71.

But that interpretation defeats the purpose of the invention, which places a power supply line protection circuit between that power supply line's input terminal and the power supply line's connection to the scanning line driving circuit, to protect the scanning line driving circuit from charges that could enter the device through the input terminal and travel along the power supply line and damage the scanning line driving circuit. Ex. 2009 ¶72; *see also* § II, *supra*. Indeed, limitation 4[e] understood in context with limitation 4[f] confirms that claim 4 recites a scanning line driving circuit—the circuit, not intermediate components of the circuit—connected between two protection circuits. Ex. 2009 ¶72.

Only ESD3 is connected to the power supply line *between* (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal. But the Petition cites no evidence to show that ESD3 discloses the claimed first protection circuit, because Dr. Murphy is unable to, or has refused to, opine that ESD3 is connected to the scanning line driving circuit, e.g., output device 70. Ex. 2008, 128:2-133:9. ESD3 is *not*, according to the Petition, connected to the scanning line driving circuit. *See* claim 4[d].

Thus, the Petition fails to show that *Reiner* discloses or renders obvious a “first protection circuit being connected to the power supply line between (i) a first

connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal.”

- iv. ***Reiner* does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f]).**

Reiner does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” Ex. 1001, claim 4[f]. *Reiner* teaches an integrated circuit including an internal ESD protection network, in particular, ESD devices connected between each input/output (i.e., entry point into the integrated circuit, here, the Vss and Vdd input terminals and each contact pad 72) and the integrated circuit’s output devices 70. Because *Reiner* describes only ESD protection networks *in* an integrated circuit, it does not disclose a scanning line driving circuit connected to a power supply line between first and second protection circuits. Ex. 2009 ¶¶75-84.

The plain language of the claim requires that the scanning line driving circuit connect to a power supply line *between* the protection circuit connecting portions. *Reiner*'s ESD protection network is *inside* its purported scanning line driver, to protect individual output devices 70. *See* Ex. 2008, 139:3-10 (Dr. Murphy opining that "it is reasonable to understand [ESD1, ESD2, and ESD3] to be within" *Reiner*'s source driver 61 integrated circuit device). *Reiner* is not the claimed invention. Ex. 2009 ¶77.

Indeed, *Reiner* is the conventional art on which the '157 patents improves. In its background section, the '157 patent explains that, in an integrated circuit like *Reiner*'s driver 61, "it is important to take measure[s] against the electro-static damages (ESD) when a high voltage caused by a static electricity or a various noise phenomenon is unintentionally *applied to the inside of the device* to damage an insulating film, thereby causing a fatal damage to the device." Ex. 1001, 1:14-19 (emphasis added). "[S]ince general semiconductor devices are formed on a silicon wafer made of conductive material, there are little chances of being electrified within the semiconductor device, so that it is a key issue to prevent the damage when a static electricity flows *through input terminals*." *Id.*, 1:23-28. The '157 patent explains that integrated circuit ESD protection means—the conventional art on which the '157 patent improves—are configured to protect the device by protecting the access points through which an ESD event could enter the

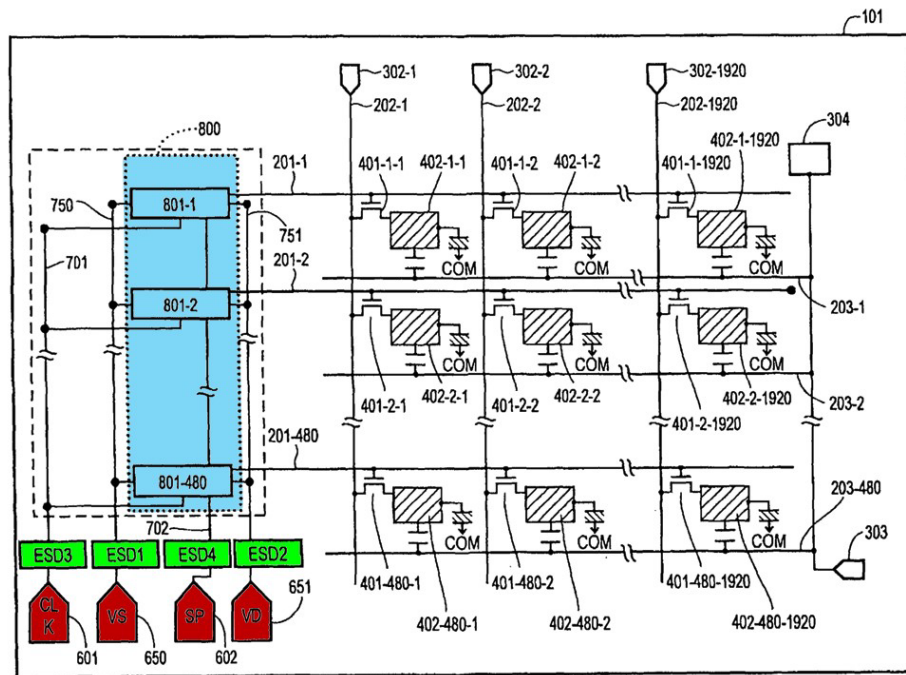
device to prevent an ESD event from damaging the device's internal circuitry.

Ex. 2009 ¶78.

Reiner teaches the same configuration. *Reiner* protects the integrated circuit, providing ESD devices between its access points and individual devices 70.

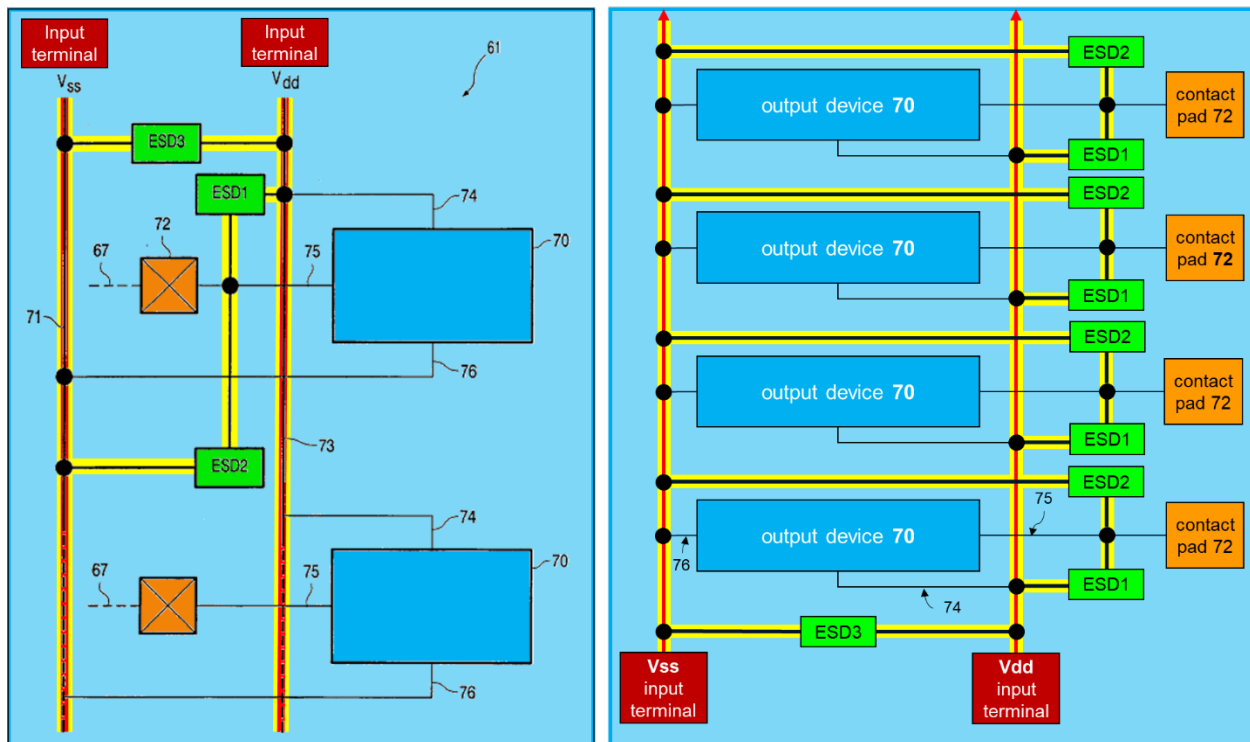
Indeed, *Reiner* describes an ESD protection network comprising (1) “protection diodes and/or transistors,” and (2) low-ohmic “metal interconnection lines for connecting these diodes and/or transistors *with inputs and/or outputs of the integrated circuit device to be protected.*” Ex. 1005, 3:4-8 (emphasis added).

The '157 patent explains that the conventional art applied these integrated circuit teachings to a display device including a scanning line driving circuit formed on an array substrate: “a conventional method used in a semiconductor on a silicon wafer is applied as it is, so that only protective circuits for preventing the static electricity from the input terminals are built in, and a conventional method of a display device not having the built-in driving circuit is used to protect the active matrix circuit from the static electricity.” Ex. 1001, 1:48-54; *see also* Ex. 2008, 56:13-57:21 (agreeing that the '157 patent discloses this conventional method, as illustrated in Fig. 11). The '157 patent shows this arrangement in Figure 11:



Id., Fig. 11, 2:25-28 (“static electricity protection circuits ESD1 to ESD4 are provided between the input terminals 601, 650 and 651 and the scanning line driving unit circuits 801-1 to 801-480, respectively”); *see also* Ex. 2009 ¶79.

Redrawing *Reiner* Figure 5—maintaining its disclosed arrangement but reorienting to compare to ’157 Figure 11—shows that *Reiner* teaches no more than the conventional arrangement, before the ’157 patent’s claimed improvements. It teaches ESD protection between input/outputs of the source driver 61 device to protect output devices 70 of source driver 61:

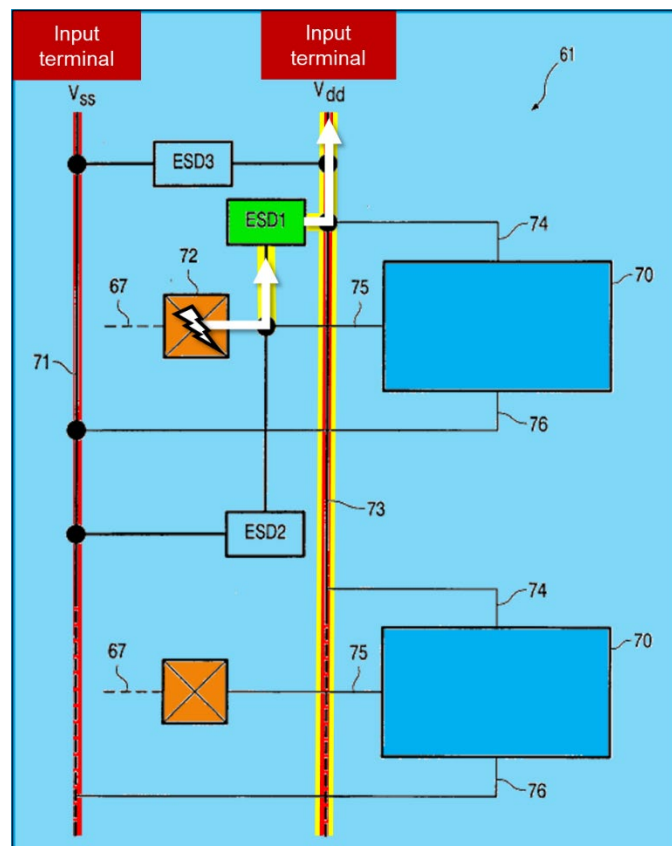


Ex. 1005, Fig. 5; Ex. 2009 ¶80 (showing **integrated circuit driver 61** and **output devices 70**, **input terminals** (not explicitly disclosed), **power supply lines Vdd and Vss**, **ESD devices**, and **contact pads 72**, and low-ohmic lines highlighted in yellow).⁴

Reiner teaches that ESD1 is connected to line 75 between contact pad 72 and output device 70 to protect output device 70 from electrostatic discharge that may enter integrated circuit device 61 through contact pad 72 and travel along line 75 to output device 70. Ex. 1005, 10:12-20; Ex. 2009 ¶80; Ex. 2008, 107:21-108:16,

⁴ Note that *Reiner* does not teach repeating ESD3. Rather, ESD3, located near the purported Vss and Vdd input terminals, provides protection for all output devices 70 down the line. There is no disclosure in *Reiner* that suggests that more than one ESD3 is needed. Ex. 2009 ¶¶80, 82.

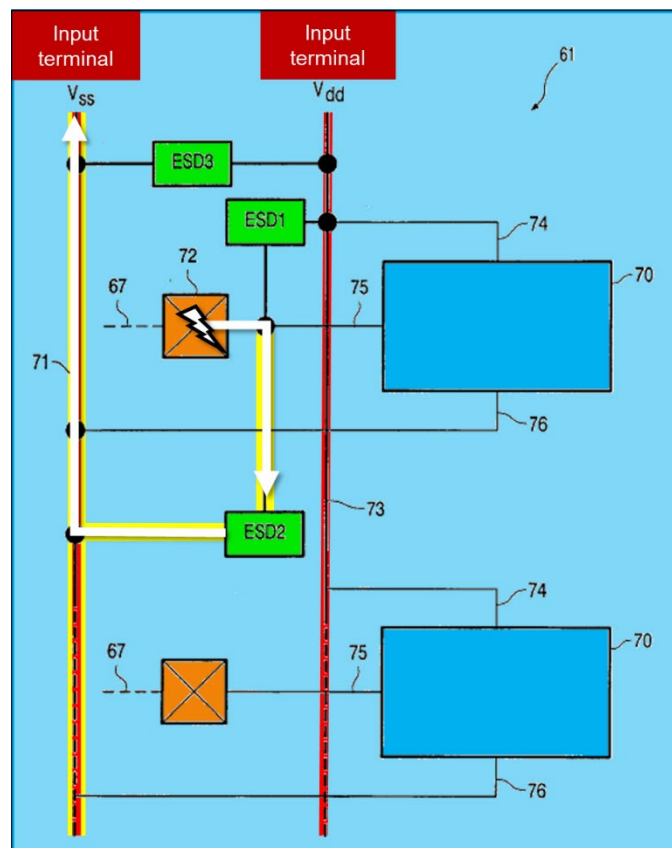
111:16-22.ESD1 prevents electrostatic charges (annotated using white lightning bolt, below) from entering output device 70 by shunting the charge to a ground terminal(not shown in Fig. 5) via ESD1 and the low-ohmic line connecting ESD1 to Vdd, which is also a low-ohmic line (white arrow). Ex. 1005, 10:12-20; Ex. 2009 ¶80.



Ex. 1005, Fig. 5; Ex. 2009 ¶80.

ESD2 is connected to line 75 between contact pad 72 and output device 70 to protect output device 70 from electrostatic discharge that may enter integrated circuit device 61 through contact pad 72 and travel along line 75 to output device

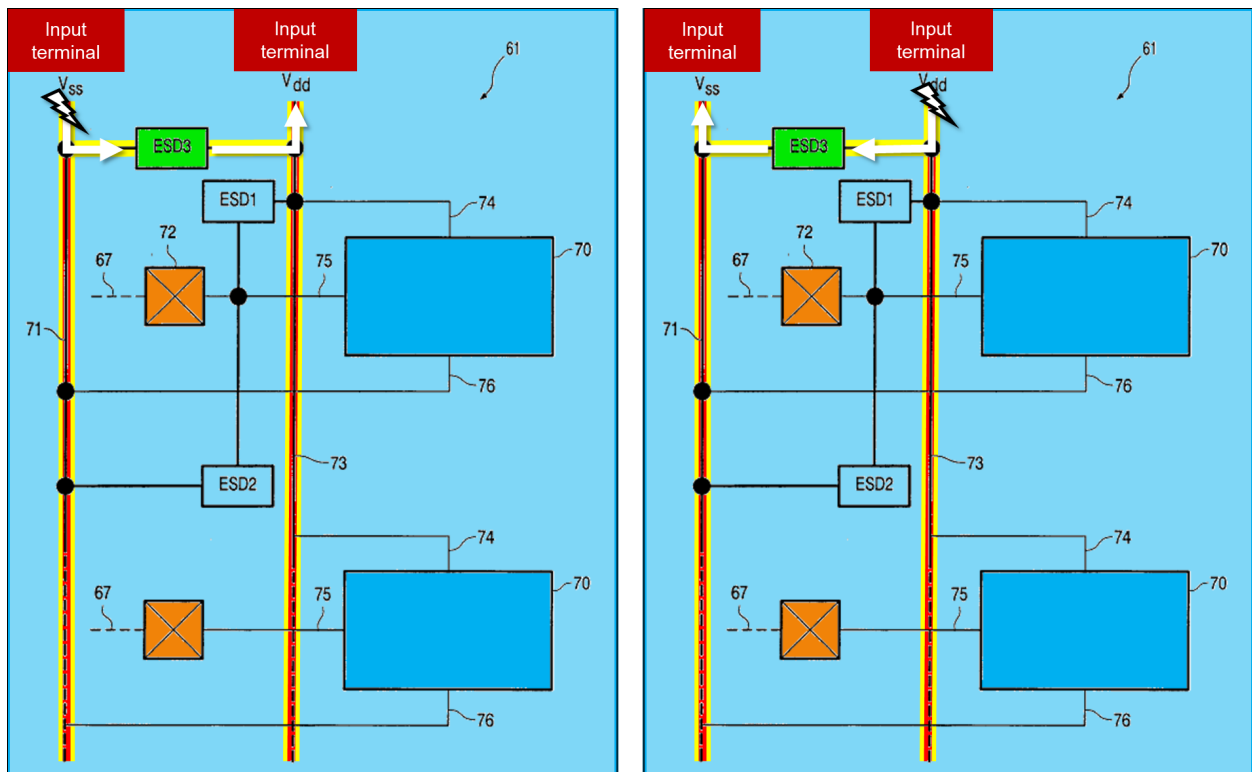
70. Ex. 1005, 10:13-20; Ex. 2009 ¶81; Ex. 2008, 122:7-9. ESD2 prevents electrostatic charges (white lightning bolt) from entering output device 70 by shunting the charge to a ground terminal (not shown in Fig. 5) via ESD2 and the low-ohmic line connecting ESD2 to Vss, which is also a low-ohmic line (white arrow). Ex. 1005, 10:15-20; Ex. 2009 ¶81.



Ex. 1005, Fig. 5; Ex. 2009 ¶81.

ESD3 is connected to lines Vss and Vdd between the purported input terminals and output devices 70 to protect output devices 70 from electrostatic charges that may enter integrated circuit device 61 through the Vss or Vdd input

terminals and travel along the power lines and enter output device 70 via connections 74 or 76, respectively. Ex. 1005, 10:14-20; Ex. 2009 ¶82; Ex. 2008, 134:10-18. ESD3 prevents electrostatic charges (white lightning bolts) from entering output device 70 by shunting the charge to a ground terminal (not shown in Fig. 5) via ESD3 and the low-ohmic line connecting ESD3 to V_{ss} and V_{dd}, which are also low-ohmic lines (white arrows). Ex. 1005, 10:15-20; Ex. 2009 ¶82.



Ex. 1005, Fig. 5; Ex. 2009 ¶82.

A POSITA would understand that *Reiner* teaches the foregoing description of the means by which ESD1, ESD2, and ESD3 function to prevent electrostatic charges from damaging output device 70 *at each of the integrate circuit's*

input/output points. Ex. 2009 ¶83. Specifically, *Reiner* discloses that the ESD devices “provide for a low-ohmic path to a [discharge] terminal,” which is why *Reiner* teaches that it is “important that certain of the lines of the device 61 provide for a low-ohmic connection to the desired [discharge] terminal,” identified using bold lines in Fig. 5. Ex. 1005, 10:15-20. In other words, each of *Reiner*’s ESD devices shown in Fig. 5 are inside integrated circuit source driver 61 between access points (terminals and contact pads 72) and connected to low-ohmic paths because the “ESD protection of integrated circuit devices relies on low-ohmic interconnections . . . for connecting” the protection diodes and/or transistors that comprise the ESD devices “with inputs and/or outputs of the integrated circuit device to be protected.” *Id.*, 3:4-8.

The Petition and Dr. Murphy ignore *Reiner*’s express disclosure regarding protecting the inputs/outputs of integrated circuit devices like source driver 61 using low-ohmic paths, as shown in Fig. 5. Ex. 2008, 119:16-19 (“Whether any particular of these lines [in Fig. 5] is bolded or not really wasn’t relevant to my analysis”), 124:15-21 (same), 125:1-6 (same), 127:2-6 (same).⁵

⁵ Dr. Murphy also testified he “was less concerned with the precise nature in which any given ESD protection circuit might function and the means exactly by which it might function,” Ex. 2008, 120:7-12, and had not analyzed *Reiner* and Fig. 5 to identify the low-ohmic bolded lines, *id.*, 125:18-127:6, but testified that an “ESD protection network such as ESD1, ESD2, or ESD3 can protect the power line” because “[i]t’s configured to provide a low ohmic path to a ground terminal,” *id.*,

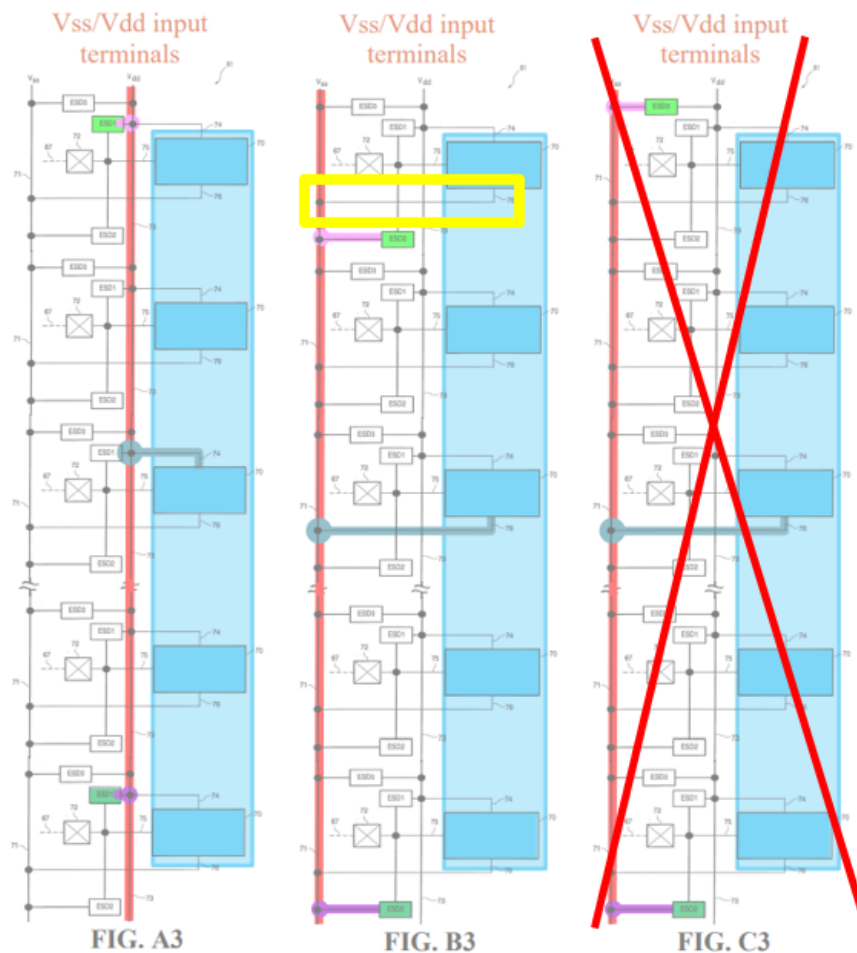
The point: unlike the '157 patent's conventional art and *Reiner*, claim 4 recites a scanning line driving circuit connected to the power supply line *between two protection circuit connections to that power supply line*. Ex. 1001, claim 4[f]; *see also id.*, 3:12-17 (describing the invention as providing “a plurality of the protective circuits are arranged on the wiring lines and the semiconductor circuit is interposed between the protective circuits. Thereby, it is possible to prevent the static electricity or noise input from the input terminals, and to protect a semiconductor circuit far from the input terminals.”). *Reiner* does not disclose a driver that is connected to a power supply line *between protection circuits*. It discloses only the prior art: an integrated circuit including internal ESD protection device near each input/output terminal. Indeed, the Petition's composite images repeating Figure 5 confirm that *Reiner* does not disclose or render obvious the claimed protection circuit arrangement. It does not disclose a scanning line driving circuit connected to the power supply line between protection circuits:

123:10-18. *See also* Ex. 1003 ¶181 (“*Reiner*'s ESD protection network, such as ESD1, ESD2, and ESD3, protect the power line because they are configured to ‘provide a low-ohmic path’ to a ‘ground terminal’ (not shown in FIG. 5) ‘in case of a voltage peak,’ which is an ESD event.”).

Fig. A3: driver 61 connected to line Vdd at ESD1 connecting portions (not between).

Fig. B3: driver 61 connected to line Vss before ESD2 (line 76, yellow box).

Fig. C3: Dr. Murphy does not opine that ESD3 is connected to driver 61. He cannot rely on ESD3.



Thus, *Reiner* does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

b. Claim 5

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* renders obvious claim 5.

c. Claim 6

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* renders obvious claim 6.

d. Claim 7

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* renders obvious claim 7.

e. Claim 8

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* renders claim 8.

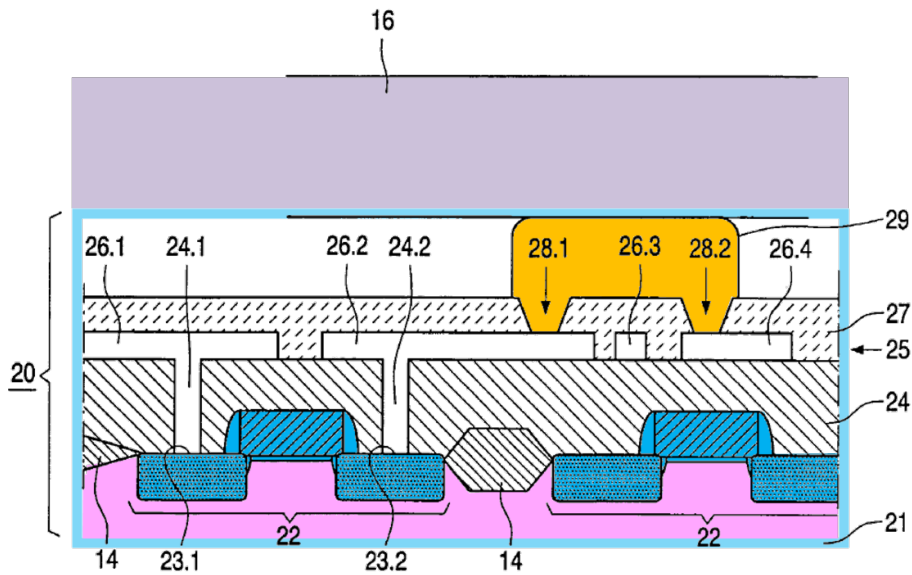
Reiner also fails to render obvious the additional limitations of claim 8.

i. *Reiner* does not disclose or render obvious a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate.”

Reiner does not disclose or render obvious a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate.” Ex. 1001, claim 8. The Petition asserts that *Reiner* discloses these elements by way of “substrates 21 or 16” of the integrated circuit 20 shown in *Reiner* Figure 2. Pet., 44-47. But the Petition does not identify a *display device* substrate and a scanning line driving circuit arranged on that substrate. *Reiner* discloses integrated circuits having their own substrates and, separate, a display to which the integrated circuits may connect (for example, via contact pads). But the Petition cannot show that

Reiner discloses or renders obvious a display device substrate and a scanning line driving circuit *arranged* on—not merely connected to—that substrate. Ex. 2009 ¶¶88-100.

Reiner Figure 2 shows a schematic cross-section of an **integrated device 20** that “comprises a **silicon substrate 21**” and at least one **integrated device 22**. Ex. 1005, 6:18-21. The **integrated device 20** includes **bump bridges** that “provide for a connection to an interconnection on a **substrate 16**,” and *Reiner* explains the **integrated circuit device 20** may be “flipped onto the **substrate 16**” so that the “**substrate 16** with its interconnections may rest on” the **bump bridges** of **integrated circuit device 20**. *Id.*, 7:22-25.



Id., Fig. 2; Ex. 2009 ¶90.

First, *Reiner*'s substrate 16 does not disclose a display device "substrate" or a "substrate" on which the integrated device 20, let alone gate driver 63, is

“arranged”: the integrated device 20 is formed on substrate 21 (the integrated circuit substrate, not the display substrate) and then flipped onto substrate 16 when it is packaged. *Compare* Ex. 1005, 6:18-21 *with* Ex. 1001, 5:20-23 (the semiconductor circuit in the scope of the claims “is *formed* by integrating polysilicon thin film transistors *on* the active matrix [glass] substrate”) (emphasis added); 1:33-36 (“in a display device using an active element such as a thin film transistor (TFT) . . . a device is *formed on* an insulating substrate”) (emphasis added); 2:35-37 (“in the case that the driving circuit of the display device is *formed on* a glass substrate”) (emphasis added); *see also* Ex. 2009 ¶91.

Second, *Reiner*’s substrate 21 does not disclose a display device “substrate”; it is the substrate on which integrated device 20 is formed. Ex. 2009 ¶92. The Petition cites no evidence disclosing a *display device* substrate on which a scanning line driving circuit is arranged.

Accordingly, the Petition fails to show that a “POSITA would have recognized that substrates 21 or 16 may include . . . the substrate on which LCD display 60’s scan/gate lines 68, source/data lines 67, and pixels are formed.” Pet., 45-46. *Reiner* is silent on this point. At most, *Reiner* discloses “an LCD display 60” and “LCD screen 60,” neither of which *Reiner* relates to the separate substrates 21 or 16 of integrated device 20, which as discussed above, do not disclose a “display substrate.” Ex. 1005, 9:11-34. The Petition simply invents a “**substrate** to

create the LCD display device described by *Reiner*” upon which “gate driver 63” would be arranged, reproduced below, and fails to point to any teaching in *Reiner* that source driver 61 or gate driver 63 are arranged on the Petition’s **substrate**. The Petition offers no evidence, only hindsight.

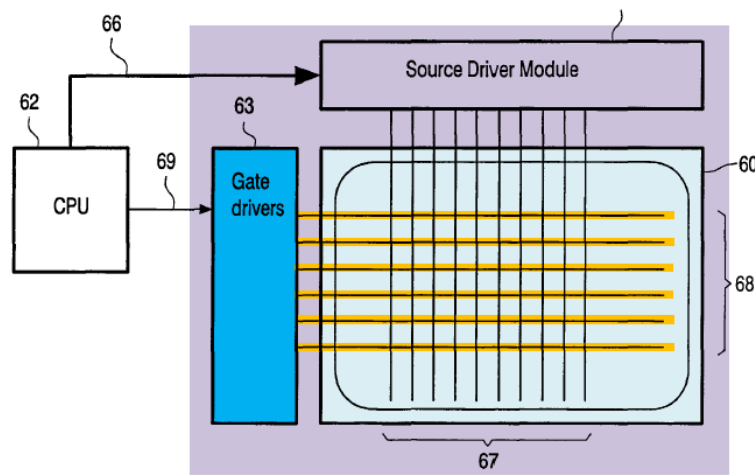


FIG. 4

Pet., 46.

Further, the Petition fails to show that arranging *Reiner*'s "gate driver[s] 63" on the display substrate "was conventional." *Id.* (citing Ex. 1007 (*Takahara*), Ex. 1010 (*Murai*), Ex. 1001 ('157 patent)). *Takahara*, *Murai*, and the '157 patent relate to devices with driving circuits formed on the display substrate, whereas *Reiner*'s source driver 61 is a discrete integrated circuit chip. Ex. 1007, [0001]; Ex. 1010, [0001]; Ex. 1001, 5:20-23. The Petition cites no evidence that it would be conventional to arrange *Reiner*'s discrete integrated circuit chip on the display substrate.

In fact, POSITA would *not* mount an integrated circuit formed on its own separate substrate, onto a display substrate. Ex. 2009 ¶¶93-100. A gate/scan line driving circuit implemented in a silicon integrated circuit chip (particularly one with bump bridges) would not fit within the 4-5 micron vertical gap between the display substrate and the counter substrate. Ex. 2009 ¶99. And if a POSITA were to arrange a gate/scan line driver directly on the display substrate, *Reiner's* integrated circuit ESD protection network for source driver 61 would necessarily change, at least because there would be no need to include contact pads 72 (output contacts of the silicon integrated circuit device, no longer needed if arranging a scanning line driving circuit on the display substrate) *or the ESD devices tied to those contact pads (ESD1, ESD2). Id.*

The Petition fails to show that *Reiner* discloses the remaining elements of claim 8 that claim “a substrate” for the same reasons. Pet., 47-50.

f. Claim 9

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* renders obvious claim 9.

g. Claim 10

The Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line to supply power” or “a first protection circuit and a second protection circuit that are connected to the scanning line

driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed. *See* § VI.A.2.a.i-ii, *supra*. Therefore, the Petition fails to show that *Reiner* renders obvious claim 10.

h. Claim 11

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* renders obvious claim 11.

i. Claim 12

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* renders obvious claim 12.

j. Claim 13

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* renders obvious claim 13.

k. Claim 14

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* renders obvious claim 14.

Reiner also fails to render obvious the additional limitations of claim 14, for the same reasons that it fails to render obvious the additional limitations of claim 8. *See* § VI.A.2.e, *supra*.

l. Claim 15

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* renders obvious claim 15.

m. Claim 16

The Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first protection circuit and a second protection circuit that are connected . . . to the scanning line drive circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.” *See* § VI.A.2.a.i-iv, *supra*. Therefore, the Petition fails to show that *Reiner* renders obvious claim 16.

n. Claim 17

The Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first protection circuit and a second protection circuit that are connected . . . to the scanning line drive circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.” *See* § VI.A.2.a.i-iv, *supra*. Therefore, the Petition fails to show that *Reiner* renders obvious claim 17.

o. Claim 18

The Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line to supply power” or “a first protection circuit and a second protection circuit that are connected to . . . the scanning line

drive circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed. *See* § VI.A.2.a.i-ii, *supra*. Therefore, the Petition fails to show that *Reiner* renders obvious claim 18.

p. Claim 1

The Petition fails to show that *Reiner* discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” *See* § VI.A.2.a.i-iv, *supra*. Therefore, the Petition fails to show that *Reiner* renders obvious claim 1.

q. Claim 2

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 1 and, thus, fails to show that *Reiner* renders obvious claim 2.

Reiner also fails to render obvious the additional limitations of claim 2, for the same reasons that it fails to render obvious the additional limitations of claim 8. *See* § VI.A.2.e, *supra*.

r. Claim 3

The Petition fails to show that *Reiner* renders obvious the display device as set forth in claim 1 and, thus, fails to show that *Reiner* renders obvious claim 3.

B. *Reiner* in view of *Takahara* does not render obvious claims 1-18 (Ground 2).

Reiner does not render obvious any of claims 1-18. § VI.A, *supra*. *Reiner* discloses only a conventional arrangement on which the '157 patent improves: a silicon integrated circuit including an ESD protection network, to protect the integrated circuit at its input/output points. Thus, *Reiner* does not disclose or render obvious key aspects of the claimed protection circuit layout to protect a scanning line driving circuit arranged on a display substrate.

Takahara discloses a display device that includes a scanning line driving circuit. But *Takahara* does not disclose the claimed inventions, either, and cannot close *Reiner*'s gaps. The Petition does not show that either reference, or the combination that the Petition proposes, discloses or renders obvious input terminals of a display device, or two protection circuits connected to a power supply line and a scanning line driving circuit connected to that power supply line

between those protection circuit connections. The arrangements remain distinct from the claimed inventions. The Petition has asserted the conventional art over which the '157 patent expressly improves.

1. *Takahara*: Overview

Takahara relates to methods for manufacturing an electro-optical device, such as an LCD device, that employs an “element-substrate device, such as an active-matrix-substrate device” formed on an insulating material, for example, glass. Ex. 1007, [0001], [0003]; Ex. 2009 ¶116.

Takahara addresses a different problem than the '157 patent, and relevant here, discloses a conventional ESD protection layout including short-circuit wiring and protection circuits located only on signal lines between the line's input terminal and its connection to the scanning line driving circuit. Ex. 2009 ¶117.

Unlike the '157 patent, *Takahara* is directed to methods to form and cut short-circuit wirings to help to diffuse to the outer perimeter of the substrate static charges that build up on the insulating substrate during manufacturing, to protect the electro-optical device. Ex. 1007, [0003]-[0004], [0007]-[0011], [0015].

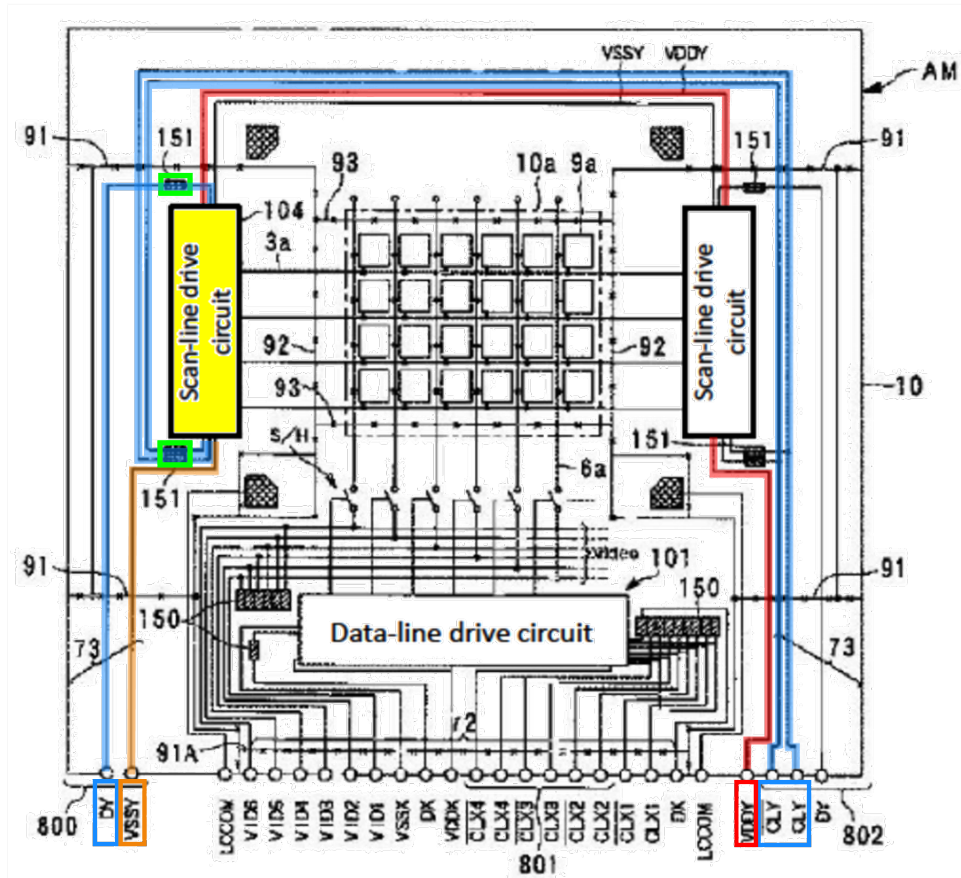
Takahara discloses forming the short-circuit wirings at an early stage of the manufacturing process—when forming the scan lines and gate electrodes on the insulating substrate—before the device is operational. *Takahara* discloses cutting those lines before completing the manufacturing process, to allow normal

operation of the electro-optical device. *Id.*, [0004]-[0005], [0008], [0068], [0070]. The short-circuit wirings electrically connect (1) the scan line wirings, (2) the data line wirings, and (3) the signal wirings that supply a signal for driving scan line and data line driving circuits. *Id.*, [0004], [0012], [0020]-[0021] (describing connecting scan lines to short-circuit wiring), [0022]-[0023] (describing connecting data lines to short-circuit wiring), [0024] (describing connecting signal lines to short-circuit wiring). The short-circuit wirings protect against electrostatic damage to or breakdown of the thin-film transistors to which the scan and data lines are connected, and the thin-film transistors in the scan and data line driving circuits, because the short-circuit wiring diffuses static charges that could otherwise accumulate on the active matrix substrate. *Id.*, [0012], [0020]-[0025]; *see also* Ex. 2009 ¶118.

Unlike the '157 patent—and *Reiner*—Takahara discloses an LCD device including an active matrix substrate that includes data and scan line driving circuits and ESD protection circuits formed on signal lines located, like in the “conventional art” on which the '157 patent expressly improves, between the line’s input terminal and its connection to the driving circuit. Ex. 2009 ¶119; *see also* Ex. 2008, 153:19-156:14. More specifically, *Takahara* discloses an LCD device including an active matrix substrate that includes data and scan line driving circuits. *Id.*, [0059]. *Takahara* discloses scan line driving circuits 104 arranged

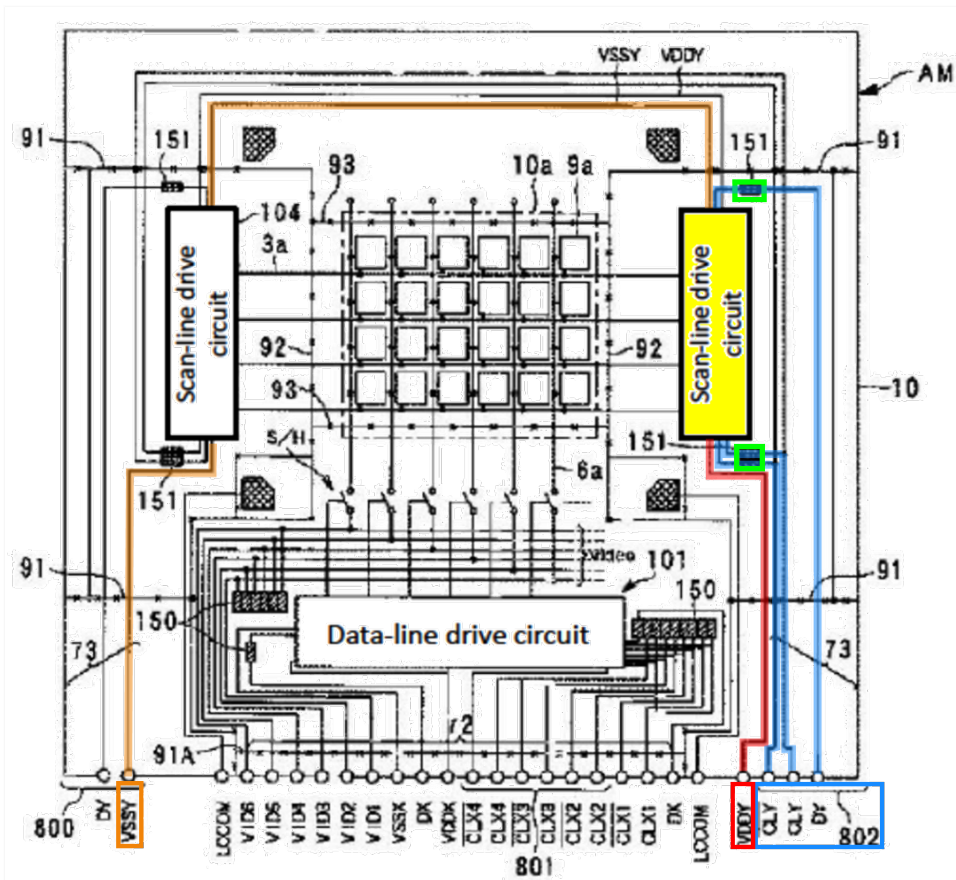
along both sides of the image display region 10a and driven by signal wirings DY (start signal), CLY (clock signal), and CLY bar (inverted clock signal), and connected to power supply lines VDDY and VSSY. *Id.*, [0062]-[0065]. *Takahara* discloses electrostatic protection circuits 150 and 151 that are formed at intermediate locations of the signal wirings (in Fig. 1, on lines DY, CLY, and CLY bar) to prevent static electricity from entering the scan line driving circuits via the signal wirings. *Id.*, [0066]; *see also* Ex. 2009 ¶119.

As shown below, the scanning line driving circuit on the left of Figure 1 (yellow) is connected to signal lines DY, CLY bar, and CLY (highlighted in blue) and power supply lines VDDY (highlighted in orange) and VSSY (highlighted in red), and protection circuits 151 (green boxes) are located on the signal lines between the input terminals (blue boxes) and where the signal lines connect to the scanning line driving circuit.



Ex. 1007, Fig. 1 (annotations added); Ex. 2009 ¶120.

Similarly, as shown below, the scanning line driving circuit on the right of Figure 1 (yellow) is connected to signal lines DY, CLY bar, and CLY (highlighted in blue) and power supply lines VDDY (highlighted in orange) and VSSY (highlighted in red), and protection circuits 151 (green boxes) are located on the signal lines between the input terminals (blue boxes) and where the signal lines connect to the scanning line driving circuit.



Ex. 1007, Fig. 1 (annotations added); Ex. 2009 ¶121.

Takahara discloses a conventional arrangement of protection circuits connected to signal lines between input terminals and a scanning line driving circuit. Ex. 2009 ¶122. Those protection circuits are not formed on or connected to the power supply lines, VDDY and VSSY, that are connected to the scanning line driving circuits. Ex. 1007, [0061]-[0066]; *see also* Ex. 1001, 1:33-2:30 (discussing the conventional ESD protection layout for a driving circuit built on an active matrix substrate using polysilicon TFTs where the ESD protection circuits ESD1 to ESD4 are located between input terminals and the driving circuit), Fig. 11

(illustrating the same); § II, *supra*; *see also* Ex. 2008, 153:19-156:14 (testifying that the ESD protection circuits 151 are connected to signal lines DY, CLY, and CLY bar between the input terminals for those signal lines and *Takahara*'s scanning line driving circuits).

2. *Reiner* in view of *Takahara* does not render obvious claims 1-18.

a. Claim 4

i. *Takahara* does not cure *Reiner*'s failure to disclose or render obvious a display device comprising "an input terminal connected to the power supply line to supply power" (claim 4[c]).

Reiner fails to disclose or render obvious a display device comprising "an input terminal connected to the power supply line to supply power." § VI.A.2.a.i, *supra*; Ex. 1001, claim 4[c]. *Reiner* and likewise *Reiner* in view of *Takahara* at most render obvious input terminals connected to *Reiner*'s lines Vdd and Vss, and those input terminals would be input terminals *of integrated circuit driver 61*. *Reiner*'s arrangement discloses drivers formed on silicon substrates, separate from the display substrate. §§ VI.A.2.a.i, VI.A.2.e, *supra*. Thus, the Petition's suggestion that *Takahara* would render obvious adding input terminals to *Reiner*'s driver 61 would not render obvious input terminals *of the display device*. Ex. 2009 ¶123.

ii. *Takahara* does not cure *Reiner*'s failure to disclose or render obvious "the scanning line

driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f]).

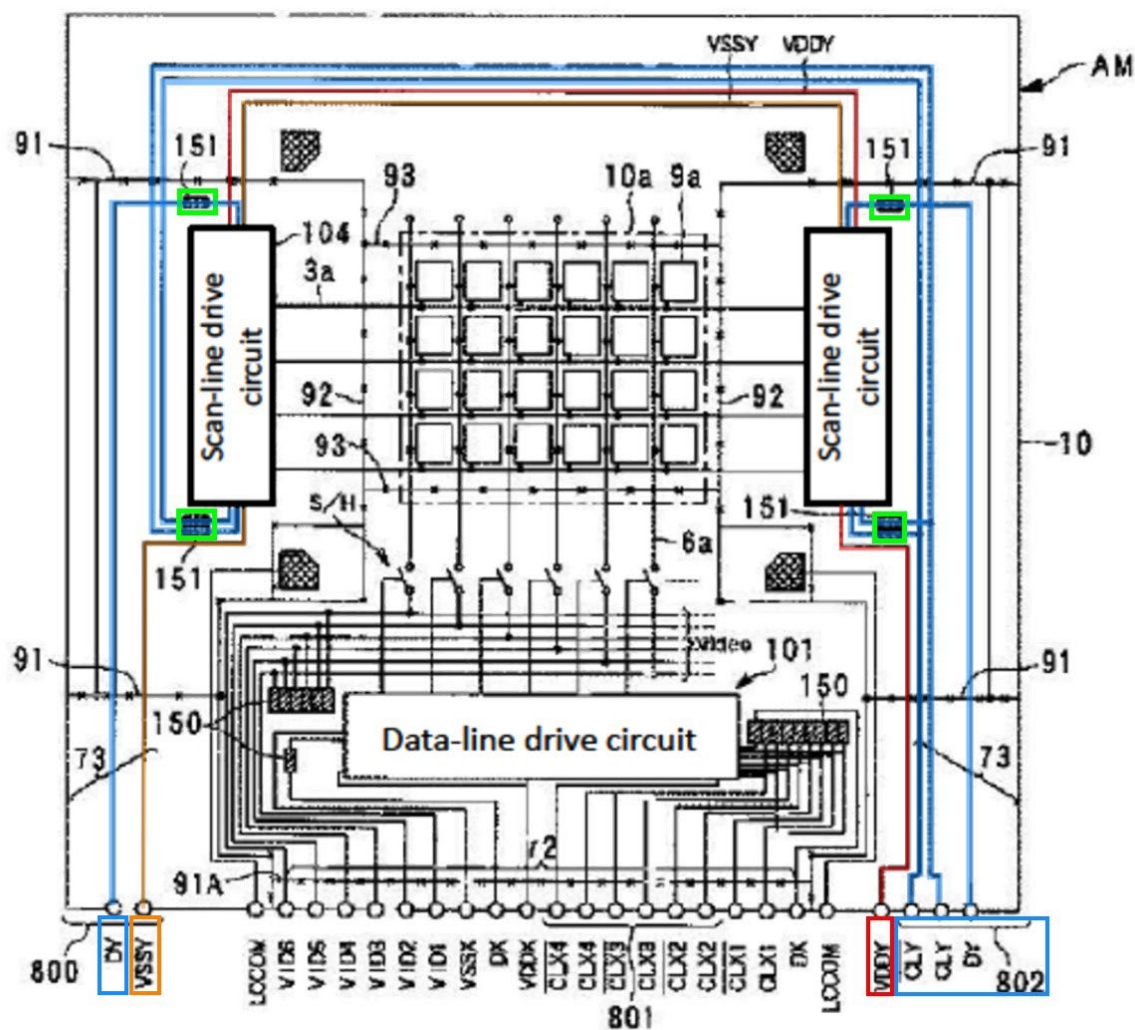
Reiner does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” § VI.A.2.a.iv, *supra*. *Takahara* does not close this gap, and the Petition does not argue otherwise. Ex. 2009 ¶¶124-137.

The Petition argues that *Takahara* discloses ESD protection circuits 151 formed on signal lines 73, which “include power lines VDDY and VSSY,” and that VDDY and VSSY “are shorted to” protection circuits 151 via short-circuit wirings 91 as shown by the ‘x’ on lines 91 between the wiring lines. Pet., 76. The Petition misrepresents *Takahara*. *Takahara* does not disclose two protection circuits connected to a power supply line (or any line for that matter), nor does *Takahara* disclose a scanning line driving circuit connected to that power supply line between those protection circuits.

Takahara does not disclose two protection circuits connected to a power supply line:

First, the Petition cites no evidence showing that *Takahara*'s signal lines 73 include power supply lines VDDY and VSSY. Indeed, *Takahara*'s disclosure states otherwise. *Takahara*'s disclosure expressly distinguishes between power supply lines and signal lines. Signal lines “supply the signals for driving the scan-line drive circuits or the data-line drive circuit”—supplying a signal is different than supplying power. Ex. 1007, [0024]-[0025]; Ex. 2009 ¶126. In fact, *Takahara* provides that signal lines include “a start signal DY, a clock signal CLY, and an inverted-clock signal CLY bar,” and “the scan-line drive circuits 104 are driven in accordance with these signals.” Ex. 1007, [0061]; *see also id.*, [0060] (explaining that other signal lines include “image signals VID1-VID6” and “a start signal DX, clock signals CLX1-CLX4, and inverted-clock signals CLX1 bar to CLX4 bar” and “the data-line drive circuit 101 is driven in accordance with these signals”). *Takahara* does not include power lines in its discussions of signal lines. Thus, it does not disclose protection circuits connected to power supply lines.

Indeed, Figure 1 shows that **electrostatic-protection circuits 151** are formed only at intermediate locations of the **clock signal lines** and **start signal lines** (DY, CLY, CLY bar) that drive the scan-line driving circuit 104; they are not formed at intermediate locations of the power supply lines **VSSY** and **VDDY**. *Id.*, [0061], [0065]; Ex. 2009 ¶127.



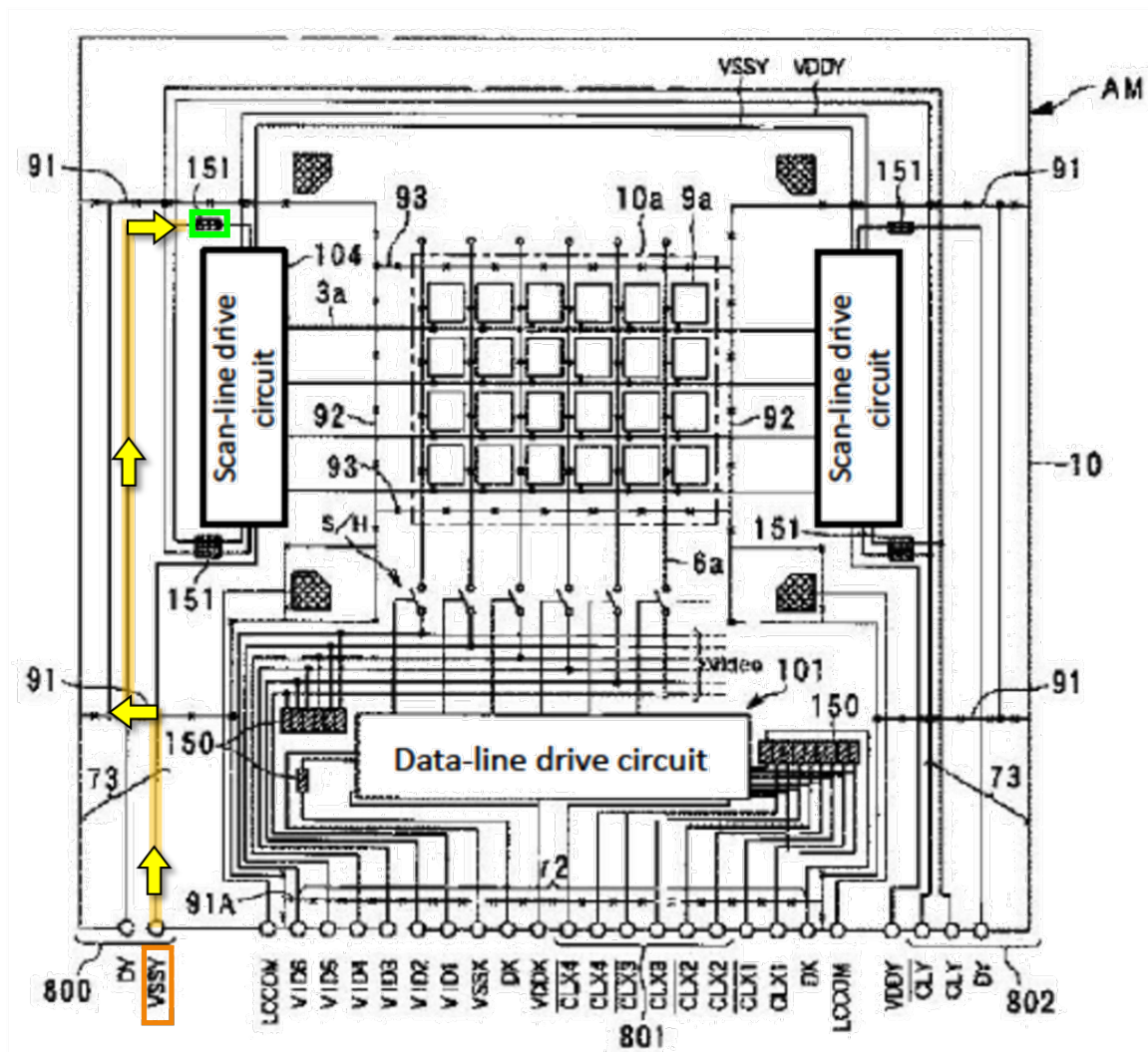
Ex. 1007, Fig. 1.

Takahara explains that the scan line and data line driving circuits are “driven in accordance with” start, clock, and image signals, not power lines. *Id.*, [0060] (signals that drive the scan line driving circuit), [0061] (signals that drive the data line driving circuit); Ex. 2009 ¶128. Further, the “signal wirings” 73 shown in Figure 1 are “for driving the scan-line drive circuits 104,” which are “routed from” terminals 800 and 802. Ex. 1007, [0065]. The annotations

identifying signal lines 73 and terminals 802 on the right side of Figure 1 include only CLY bar, CLY, and DY signal wirings and terminals, which confirms that the annotations identifying signal lines 73 and terminal 800 on the left side of Figure 1 apply only to the DY signal wiring. Ex. 2009 ¶128.

Second, the Petition's suggestion that the power supply lines are shorted to protection circuits through the short-circuit wiring is unsupported and technically flawed. Recognizing that Figure 1 does not show an ESD protection circuit formed on VDDY or VSSY, the Petition suggests that *Takahara* discloses connecting the power lines to protection circuits *formed on other lines* (signal lines), through short-circuit wirings 91. Pet., 76-77. But *Takahara* does not disclose that the short-circuit wirings connect the power lines to the signal lines (and their protection circuits). Instead, the short-circuit wirings electrically connect (1) the scan line wirings, (2) the data line wirings, and (3) the signal wirings that supply a signal for driving scan line and data line driving circuits. Ex. 1007, [0004], [0012], [0020]-[0021] (describing connecting scan lines to short-circuit wiring), [0022]-[0023] (describing connecting data lines to short-circuit wiring), [0024] (describing connecting signal lines to short-circuit wiring), Fig. 4 (showing plan view showing layout, and connection via contact holes 403, between a signal wiring 72 and a first short-circuit wiring 91); *see also* Ex. 2009 ¶129.

Even if *Takahara* disclosed that short-circuit wirings 91 electrically connect to power lines VDDY and VSSY, *Takahara* does not disclose further shorting those lines through to the signal lines. The Petition suggests that *Takahara*'s short-circuit wirings diffuse static electricity from the power lines to the more-vulnerable signal lines; the suggestion is unsupported and non-sensical. Pet., 76-77; Ex. 2009 ¶130. For example, the Petition suggests that an ESD event (voltage spike) (depicted with yellow arrows, below) that enters the VSSY input terminal (orange box) would divert to the short-circuit wiring 91 (via a connection that *Takahara* does not disclose) rather than travel along the VSSY line to the scan-line driving circuit, and then, rather than travel outwards towards the periphery of the display substrate via short-circuit wiring 91, the voltage spike would instead divert to signal line DY, and travel back toward the *center* of the substrate before reaching ESD protection circuit 151 formed on the DY signal line (green box).

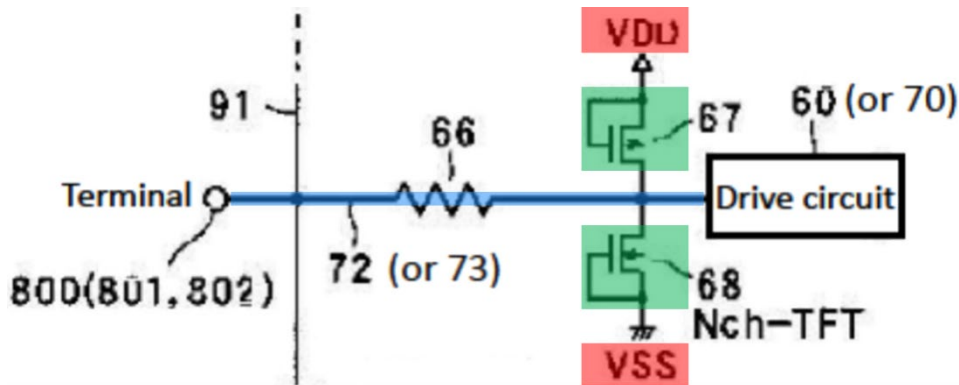


Ex. 1007, Fig. 1 (annotations added); *see also* Pet., 77 (showing Fig. 1 annotation),
Ex. 1003 ¶236 (same).

Takahara discloses the opposite: the purpose of the short-circuit wirings is to diffuse static electricity “toward an outer perimeter of the substrate via said short-circuit wiring” to prevent static electricity from flowing through circuits on the substrate, such as the scanning line driving circuit. Ex. 1007, [0004]; Ex. 2009 ¶131.

Third, Figure 3 does not show that *Takahara*'s protection circuits are connected to a power supply line. The “positive power supplies VDD and negative power supplies VSS” that are part of ESD protection circuit 150 or 151, illustrated in Figure 3, are not “the power supply line” (VSSY and VDDY) to which the scanning line driving circuit is connected. Ex. 2009 ¶132. Instead, *Takahara* discloses an ESD protection circuit layout in which the power supplies VDD and VSS serve as reference potentials that limit the potential of the current on signal lines 72 or 73 that can pass through the ESD protection circuit 150 or 151. Ex. 2009 ¶132; Ex. 1007, [0066], Fig. 3; Ex. 2008, 152:8-22 (Dr. Murphy agreeing that serving as reference potentials is “one of the functions that VDD and VSS are performing here in the context of Figure 3” and testifying this is “one way to describe how that ESD protection works” without identifying any other functions served by VDD and VSS in the context of Figure 3).

Specifically, as shown below, *Takahara* describes and illustrates in Figure 3 a P-channel TFT 67 and N-channel TFT 68 (highlighted in green) in a push-pull layout where the drain electrode of each TFT is connected to signal wiring 72 or 73 (highlighted in blue), and source and gate electrodes are connected, respectively, to power supplies VDD and VSS (highlighted in red). Ex. 2009 ¶132.

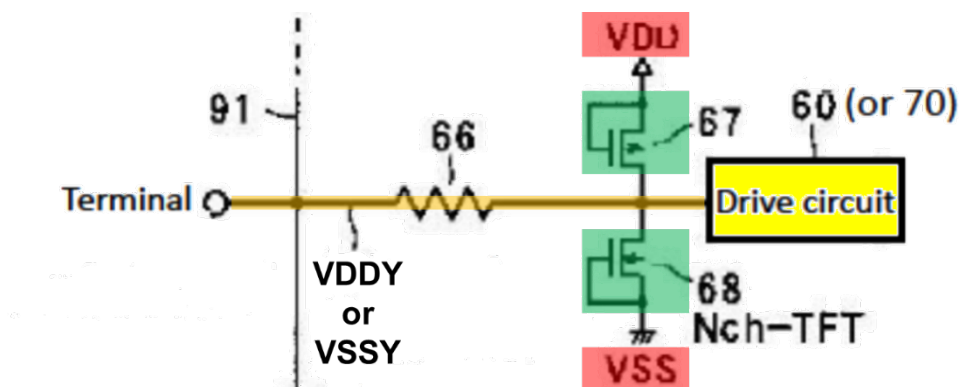


Ex. 1007, Fig. 3 (excerpt).

As *Takahara* explains, the push-pull layout of TFTs 67 and 68 forms a diode between VDD and VSS, *id.*, [0066], which functions to limit the potential on signal lines 72 or 73 (i.e., signal lines DY, CLY, or CLY bar) to not greater than the potential on VDD and not less than the potential on VSS. Ex. 2009 ¶133. In other words, if an ESD event that enters signal line 72 or 73 causes the voltage on the line to exceed the positive potential on VDD or negative potential on VSS, the ESD protection circuit activates and the excess current flows through VDD or VSS instead of entering and damaging the driving circuit. Ex. 1007, [0066]; Ex. 2009 ¶133.

Important, VDD and VSS are *not* the power supply lines for the display panel (VDDY and VSSY). *Takahara*'s ESD protection circuit layout protects against ESD events that occur on signal lines 72 or 73, not any power supply line, and the power supplies VDD and VSS are connected to limit the potential on the signal lines and provide a discharge path for excess potentials. Ex. 2009 ¶134.

Power supplies VDD and VSS are not the same as *Takahara*'s VDDY and VSSY power supply lines that are connected to the scanning line driving circuit. *Id.* For example, as shown in a hypothetical version of Fig. 3, if *Takahara* disclosed an ESD protection circuit located on VDDY or VSSY (highlighted in orange), the TFTs 67 and 68 (highlighted in green) would still need to connect to power supplies VDD and VSS (highlighted in red), to serve as reference potentials, as discussed.



Ex. 2009 ¶134.

Indeed, the description and layout of the ESD protection circuit in *Takahara* is essentially identical to the protection circuit layout described in the '157 patent and illustrated in Fig. 4. Ex. 1001, 6:3-23, Fig. 4 (describing a p- and n-type transistor connected to the wiring line being protected with source and gate electrodes connected to, respectively, a high potential and low potential power source V_H and V_L to limit “a signal level given to the wiring line being protected” to “not more than V_H and not less than V_L” such that when the potential is out of

that range, the circuit activates and “abnormal current runs through a reference potential VH line or a reference potential VL line”); Ex. 2009 ¶135. A POSITA would not understand the reference potential power supplies (VDD/VSS in *Takahara*; VH/VL in the ’157 patent) that are connected to the transistors in this ESD protection circuit layout to refer to “the power supply line” to which the first and second protection circuits are “connected” to “protect the scanning line driving circuit,” as claimed. Ex. 2009 ¶135; Ex. 1001, claim 4[d]; *see also* Ex. 2008, 152:8-22.

Takahara does not disclose a scanning line driving circuit connected to a power supply line between protection circuits:

As discussed, *Takahara* discloses one protection circuit disposed on a signal line, between the signal line’s input terminal and the signal line’s connection to the scanning line driving circuit. Like *Reiner*, *Takahara* does not disclose a scanning line driving circuit connected to a power supply line between *two* protection circuits. Ex. 2009 ¶136. The Petition does not argue otherwise.

Thus, *Reiner* in view of *Takahara* does not render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

iii. A POSITA would not have been motivated to combine *Reiner* and *Takahara*.

The Petition asserts that a POSITA would have been motivated “to provide a first and second protection circuit connected to the gate driver 63 to protect against ESD events and damage and also connected to the power supply lines that can be lines that are subject to ESD events.” Pet., 78-80. But the Petition cites to *Takahara* for only the general proposition that a POSITA would know to protect scan-line driving circuits from ESD damage. *Id.* (citing *Takahara*’s disclosures at Ex. 1007, [0063], [0066], Figs. 1, 3). *Reiner* does not disclose or render obvious the claimed protection circuit arrangement. *See* § VI.A.2.a.iv, *supra*. The Petition does not assert that *Takahara*’s disclosures would motivate a POSITA to close those gaps. Pet., 78-80.

A POSITA would have no reason to modify *Reiner* in view of *Takahara*. *Reiner* provides an ESD protection network for silicon integrated circuits. § VI.A.1-2, *supra*; Ex. 2009 ¶139. *Takahara* provides protection circuits for signal lines and a short-circuit wiring to protect its panel. The Petition cites no need to combine the teachings of *Reiner* and *Takahara*.

b. Claims 5-7, 9

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 5-7 or 9.

c. Claim 8

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 4 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 8.

Further, even though *Takahara* teaches forming a scanning line driving circuit on the display substrate, a POSITA would not have been motivated to form *Reiner*'s integrated circuit drivers 61 and 63, as described and shown in Figure 5, on a display substrate. § VI.A.2.e, *supra*.

d. Claim 10

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “an input terminal connected to the power supply line to supply power” and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 10. *See* § VI.B.2.a.i, *supra*.

e. Claims 11-15

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 10 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 11-15.

Further, even though *Takahara* teaches forming a scanning line driving circuit on the display substrate, a POSITA would not have been motivated to form *Reiner*'s integrated circuit drivers 61 and 63 on a display substrate. § VI.A.2.e, *supra*.

f. Claim 16

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit” and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 16. § VI.B.2.a.i-ii, *supra*.

g. Claim 17

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit” and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 17. § VI.B.2.a.i-ii, *supra*.

h. Claim 18

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “an input terminal connected to the power supply line to supply power” and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 18. *See* § VI.B.2.a.i, *supra*.

i. Claim 1

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power

supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claim 1. § VI.B.2.a.i-ii, *supra*.

j. Claims 2-3

The Petition fails to show that *Reiner* in view of *Takahara* renders obvious the display device as set forth in claim 1 and, thus, fails to show that *Reiner* in view of *Takahara* renders obvious claims 2-3.

Further, for the same reasons that *Reiner* in view of *Takahara* does not render obvious claim 8, the combination does not render obvious claim 2.

VII. CONCLUSION

The Petition does not establish the unpatentability of any of the challenged claims by a preponderance of the evidence. The Board should deny the request for cancellation.

Date: March 14, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

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Date: March 14, 2025

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CERTIFICATE OF SERVICE

I certify that on March 14, 2025, a copy of Patent Owner's Response, including exhibits, was served in its entirety by electronic mail to Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

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