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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x

BOE TECHNOLOGY GROUP CO., :
LTD., :
Petitioner, : Case IPR2024-00973
v. :
138 EAST LCD ADVANCEMENTS: U.S. Patent No.
LIMITED, : 9,184,157
Patent Owner. :

- - - - - x

REMOTELY CONDUCTED VIDEOTAPED DEPOSITION OF
PATRICK MURPHY, PHD
FRIDAY, MARCH 7, 2025
8:05 A.M. CST

JOB NO.: 573260
PAGES: 1 - 185
REPORTED BY: KARISA EKENSEAIR, CCR RPR RMR

1 DEPOSITION OF PATRICK MURPHY, PHD, CONDUCTED
2 VIA ZOOM VIDEOCONFERENCE.
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10 Pursuant to notice, before Karisa J.
11 Ekenseair, Certified Shorthand Reporter in and for
12 the States of Arkansas, Oklahoma, Illinois,
13 Missouri, Tennessee, Georgia, New Mexico,
14 Washington, and California; National Registered
15 Professional Reporter; National Registered Merit
16 Reporter; Notary Public.
17
18
19
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21
22

A P P E A R A N C E S

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NICK HEISLER, REMOTE TECHNICIAN

JESSE CASTRO, VIDEOGRAPHER

T A B L E O F C O N T E N T S

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WITNESS: PATRICK MURPHY, PHD

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CERTIFICATE OF REPORTER..... 184

EXHIBITS

(ATTACHED TO TRANSCRIPT)

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EXHIBIT 1003	DECLARATION OF PATRICK	
	MURPHY, PH.D, P.E., IN	
	SUPPORT OF PETITION FOR INTER	
	PARTES REVIEW OF U.S. PATENT	
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(ATTACHED TO TRANSCRIPT)

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Transcript of Patrick Murphy, Ph.D.
Conducted on March 7, 2025

6

P R O C E E D I N G S

THE VIDEOGRAPHER: Here begins Media No. 1
in the videotaped deposition of Dr. Patrick Murphy
in the matter of BOE Technology Group Company
Limited v 138 East LCD Advancements Limited, in
the United States Patent and Trademark Office
before the Patent Trial and Appeal Board, Case
Number IPR2024-00973.

Today's date is March 7, 2025. The time
on the video monitor is 8:05 a.m. The remote
videographer today is Jesse Castro representing
Planet Depos. All parties of this video
deposition are attending remotely.

Would counsel please voice-identify
themselves and state whom they represent.

MR. JONES: Will Jones on behalf of Patent
Owner from Robins Kaplan LLP, and joining me is
Emily Tremblay also of Robins Kaplan LLP.

MR. RODKEY: Kevin Rodkey for Petitioner
BOE Technology Group. I'm with the law firm
Finnegan. And with us are Chinping Long and
Yongda Ma who are client representatives of BOE

08:03:49
08:04:03
08:04:06
08:04:09
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08:04:17
08:04:20
08:04:27
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08:05:41
08:05:43
08:05:46
08:05:49
08:05:50
08:05:55
08:05:59
08:06:02
08:06:05

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Transcript of Patrick Murphy, Ph.D.
Conducted on March 7, 2025

7

1 Technology.

08:06:09

2 THE VIDEOGRAPHER: The court reporter
3 today is Karisa Ekenseair also representing Planet
4 Depos. The witness may now be sworn.

08:06:09

08:06:10

08:06:13

5 THE REPORTER: Counsel, I have a
6 stipulation regarding the oath.

08:06:17

08:06:18

7 Will counsel please stipulate that in lieu
8 of formally swearing in the witness, the reporter
9 will instead ask the witness to acknowledge that
10 their testimony will be true under penalties of
11 perjury, that counsel will not object to the
12 admissibility of the transcript based on
13 proceeding in this way and that the witness has
14 verified that they are, in fact, Dr. Patrick
15 Murphy, beginning with the noticing attorney,
16 please?

08:06:20

08:06:40

17 MR. JONES: Yes. Patent Owner so
18 stipulates.

08:06:40

08:06:46

19 MR. RODKEY: And Petitioner stipulates.

08:06:46

20 PATRICK MURPHY, PHD
21 of lawful age, being first duly sworn, deposes and
22 says in reply to the questions propounded as

08:07:01

08:07:01

08:07:01

1	follows:	08:07:01
2	EXAMINATION	08:07:02
3	BY MR. JONES:	08:07:02
4	Q Good morning.	08:07:05
5	A Good morning.	08:07:06
6	Q Could you please state your full name for	08:07:07
7	the record?	08:07:11
8	A Full name is Patrick Francis Murphy.	08:07:11
9	Q Have you ever been deposed before, Dr.	08:07:15
10	Murphy?	08:07:18
11	A Yes, I have.	08:07:18
12	Q How many times? I imagine quite a few.	08:07:21
13	A Very roughly five or six.	08:07:27
14	Q Okay. What was the most recent matter in	08:07:30
15	which you were deposed?	08:07:32
16	A I was deposed as part of a confidential	08:07:35
17	arbitration proceeding. I believe that was last	08:07:42
18	year.	08:07:46
19	Q Have you been deposed before in connection	08:07:46
20	with opinions you've offered in support of an IPR	08:07:52
21	petition?	08:07:55
22	A No. I haven't been deposed for an IPR	08:07:55

1 opinions.

08:08:01

2 Q Have you ever been deposed in a matter
3 where you offered expert opinions in district
4 court litigation?

08:08:02

08:08:07

08:08:20

5 A Yes.

08:08:21

6 Q Do you recall what those matters were?

08:08:21

7 A Well, I believe that this information was
8 provided as an attachment onto my declaration in
9 this matter, so I could refer to those. I could
10 read them off for you.

08:08:24

08:08:28

08:08:34

08:08:37

11 Q Okay. Like, that would be in your CV you
12 included with your declaration in support of the
13 IPR we're talking about today?

08:08:39

08:08:43

08:08:47

14 A I believe they're attached. Yes.

08:08:49

15 Q All right. Just to ensure we're on the
16 same page, I will give you a quick overview how
17 this will work. So, obviously, I'm going to ask
18 you questions. You should answer verbally, not
19 nodding or "huh-uh" or things like that so the
20 court reporter can get a clean record. Okay?

08:08:52

08:08:57

08:09:00

08:09:04

08:09:05

08:09:08

21 A Okay. I can do that.

08:09:10

22 Q And your attorney might object to some of

08:09:13

1	my questions but you should still answer unless	08:09:17
2	your attorney instructs you not to answer.	08:09:19
3	Understood?	08:09:22
4	A Understand.	08:09:23
5	Q And if you don't understand a question I	08:09:23
6	ask, please let me know and I'll try to clarify	08:09:28
7	it. Sound good?	08:09:31
8	A Agreed.	08:09:33
9	Q And then if you need to take a quick	08:09:33
10	break, let me know. Otherwise, we'll plan to take	08:09:39
11	a break every one or two hours. And if we make it	08:09:43
12	to lunch, we'll take a lunch break. Sound good?	08:09:46
13	A Yeah. That sounds fine.	08:09:50
14	Q Okay. Is there any reason you can think	08:09:52
15	of that you can't testify fully and truthfully in	08:09:54
16	response to my questions today?	08:09:59
17	A No.	08:10:00
18	Q Is there -- well, let me ask this: Where	08:10:00
19	are you testifying from today?	08:10:06
20	A Right now, I am sitting in the Washington	08:10:07
21	DC offices of Finnegan.	08:10:11
22	Q Is there anyone else in the room with you	08:10:17

Transcript of Patrick Murphy, Ph.D.
Conducted on March 7, 2025

11

1	right now?	08:10:20
2	A Counsel for BOE, Kevin Rodkey, is in the	08:10:20
3	room.	08:10:32
4	MR. JONES: Can we mark as Exhibit 2004	08:10:33
5	the document with the file name starting with depo	08:10:38
6	notice?	08:10:43
7	REMOTE TECHNICIAN: Stand by, please.	08:10:53
8	MR. JONES: Give Dr. Murphy control so he	08:11:13
9	can look through Exhibit 2004.	08:11:16
10	MR. RODKEY: Counsel, can you please put	08:11:18
11	this in the chat so I can view it and have a copy	08:11:20
12	as well?	08:11:26
13	MR. JONES: Yes, I can.	08:11:26
14	REMOTE TECHNICIAN: Sorry. Dr. Murphy,	08:11:36
15	one second and you can take control here. There,	08:11:38
16	you may take control now.	08:11:41
17	MR. JONES: Kevin, it looks like Nick	08:11:43
18	uploaded the exhibit. Do you have access to it?	08:11:46
19	MR. RODKEY: I believe so. I'm	08:11:49
20	downloading it now. One second. Yes. I have	08:11:50
21	access.	08:12:04
22	(Exhibit 2004 marked for identification.)	08:12:06

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1	Q Dr. Murphy. Have you seen Exhibit 2004	08:12:06
2	before?	08:12:09
3	A Yes.	08:12:10
4	Q And you understand that pursuant to this	08:12:12
5	notice, you are here today to testify regarding	08:12:14
6	your opinions you offered in support of Petitioner	08:12:16
7	BOE Technology Group Company Limited's IPR	08:12:20
8	petition which is IPR2024-00973 regarding U.S.	08:12:25
9	Patent 9,184,157?	08:12:30
10	A Yes. That's my understanding.	08:12:37
11	Q If we refer to U.S. Patent No. 9,184,157	08:12:40
12	as '157 patent today, that work for you?	08:12:45
13	A That will be fine.	08:12:48
14	Q And if we refer to IPR2024-00973 just as	08:12:49
15	the '157 IPR, that work for you?	08:12:56
16	A That will be fine.	08:13:01
17	Q And you are prepared today to testify	08:13:02
18	regarding your opinions in support of the '157 IPR	08:13:08
19	petition?	08:13:12
20	A Yes, I am.	08:13:12
21	Q Okay.	08:13:13
22	MR. JONES: We can take down Exhibit 2004.	08:13:17

1	Q Dr. Murphy, did you speak with anyone to	08:13:24
2	prepare for your deposition today?	08:13:26
3	A Not other than meetings with counsel.	08:13:28
4	Q Which counsel did you meet with?	08:13:44
5	A Counsel for BOE.	08:13:46
6	Q Does that include Mr. Rodney?	08:13:51
7	A It could include Mr. Rodkey, if I heard	08:13:56
8	you correctly.	08:14:00
9	Q Rodkey, yes. Did you speak with any other	08:14:06
10	counsel?	08:14:09
11	A You're asking me to identify individuals?	08:14:09
12	Q Yes, please.	08:14:12
13	A I believe I spoke with Mr. Chinyu, and his	08:14:13
14	last name escapes me. I apologize.	08:14:26
15	Q Did you review any documents to prepare	08:14:28
16	for your deposition?	08:14:30
17	MR. RODKEY: Object on privilege grounds.	08:14:33
18	A Generally, I reviewed a number of	08:14:42
19	documents related to my declaration and the bases	08:14:44
20	for my opinions, yes.	08:14:52
21	Q So you are currently employed as a	08:14:54
22	principal engineer at Exponent; is that right?	08:15:05

1 A That's my current position and title, 08:15:11
2 yeah. 08:15:14

3 Q What is the -- can you describe to me what 08:15:20
4 is the scope of what you do in that role at 08:15:21
5 Exponent? 08:15:26

6 A In general, my role at Exponent is to 08:15:26
7 investigate and analyze and provide consultation 08:15:34
8 services to our clients. Primarily, my area of 08:15:42
9 technical activity is electrical engineering, 08:15:43
10 computer science, semiconductor devices, electric 08:15:47
11 power systems, those related areas. And some of 08:15:50
12 my roles are -- responsibilities are managerial as 08:15:55
13 well and managing teams of consultants at 08:16:00
14 Exponent. 08:16:07

15 Q Is it correct that you're based out of 08:16:07
16 Exponent's New York office? 08:16:13

17 A Yes. That's correct. 08:16:15

18 Q What type of clients do you provide 08:16:16
19 consulting services to? And what I'm getting is 08:16:29
20 division between, you know, the role you're 08:16:34
21 playing here versus nonlitigation-related 08:16:36
22 consulting work. 08:16:40

1 A We provide -- and the projects that I work 08:16:42
2 on for clients in the manufacturing industries, 08:16:51
3 utility industries, very broadly insurance 08:16:56
4 industry as well, construction industries, and we 08:17:04
5 are retained by manufacturers companies themselves 08:17:09
6 and sometimes by counsel representing those 08:17:15
7 companies. 08:17:19

8 Q What type of manufacturing companies are 08:17:19
9 you referring to? 08:17:30

10 A Manufacturers of consumer electronic 08:17:31
11 devices, semiconductor devices, electric power 08:17:39
12 equipment, and -- and so on, similar to that that 08:17:44
13 I described as my, you know, focus of my technical 08:17:48
14 services. 08:17:54

15 Q Is it -- is it correct that you've worked 08:17:54
16 at Exponent since you obtained your PhD? 08:18:12

17 A Yes. That's right. 08:18:20

18 Q So you haven't worked anywhere else since 08:18:22
19 you finished your education? 08:18:24

20 A Well, I've spent some time as an adjunct 08:18:28
21 professor at NYU, formerly Brooklyn Polytech but 08:18:33
22 that was concurrent with my work at Exponent. So 08:18:38

1 those are the places I've worked since then. 08:18:41

2 Q Can you briefly walk me through since you 08:18:43
3 started at Exponent and where you are today the 08:18:52
4 different positions and roles you had at Exponent, 08:18:56
5 just briefly? 08:19:01

6 A Sure. And this is from the -- my best 08:19:02
7 recollection right now. The overall, my career 08:19:12
8 started at the position of an associate at 08:19:17
9 Exponent where I was a -- you might call it a 08:19:20
10 junior consultant, assisting investigations and 08:19:24
11 analysis. I was promoted to senior associate. 08:19:30

12 I received my professional engineering 08:19:35
13 license so my title was -- became senior engineer. 08:19:38
14 I then was promoted to title of managing engineer 08:19:42
15 and assumed additional responsibilities to manage 08:19:47
16 projects and manage teams to do the technical 08:19:52
17 services projects. As part of those promotions, I 08:19:56
18 was promoted to senior managing engineer and 08:20:00
19 ultimately principal engineer, again, assuming 08:20:04
20 more responsibilities for directing projects, 08:20:08
21 managing projects, and being a leader among the 08:20:12
22 electrical engineering and computer science 08:20:16

1 practice at Exponent.

08:20:19

2 Q So throughout your experience at Exponent,
3 have you ever designed an LCD display, the -- say
4 the array circuitry component of an LCD display?

08:20:24

08:20:38

08:20:46

5 A I've considered, analyzed, and reviewed,
6 and proposed alterations to display electronics
7 and including LCD displays over the course of my
8 career at Exponent. So yes, I would say yes.

08:20:52

08:21:06

08:21:17

08:21:21

9 Q When you say display electronics including
10 LCD display, what specific parts of the LCD
11 display have you been directly involved where
12 you've actually proposed alterations, have you
13 done that for the array circuitry specifically of
14 an LCD display?

08:21:39

08:21:46

08:21:53

08:21:56

08:22:00

08:22:07

15 A Specifically, the backplane which includes
16 the -- generally, the electronic devices on
17 the -- the -- to control and drive the display
18 pixels.

08:22:09

08:22:14

08:22:22

08:22:28

19 Q Can you give me an example, what do you
20 mean by backplane?

08:22:41

08:22:47

21 A Just using the terminology in the broadest
22 sense, typically I'll refer to backplane

08:22:48

08:22:52

1 electronics as opposed to the light-emitting or 08:22:58
2 light-transmitting pixel portions to distinguish 08:23:08
3 those two kind of aspects of a display. 08:23:15

4 Q So in this broad sense, can you describe 08:23:32
5 specifically what you mean by the light-emitting 08:23:37
6 or light-transmitting pixel portions as compared 08:23:41
7 to the -- the backplane? 08:23:47

8 A If we're talking about an OLED display, 08:23:56
9 the light-emitting portion would be the 08:24:02
10 light-emitting diode. There might be one or more 08:24:04
11 of those for each pixel. If we're talking about 08:24:12
12 an LED type of display, you might have the liquid 08:24:15
13 crystal itself, color filters, the electrodes that 08:24:19
14 manipulate the LCD liquid crystal material itself. 08:24:24

15 Those might be considered part of the 08:24:31
16 pixel circuitry or the pixel -- the light-emitting 08:24:35
17 components of that display, bearing in mind that 08:24:45
18 the electrodes are electrical or electronic 08:24:47
19 devices. And so it might be arguable where 08:24:51
20 exactly to draw the line between optical and 08:24:55
21 electronic components. 08:24:58

22 Q So for a liquid display, you mentioned 08:25:13

1 the -- the liquid crystal itself, color filters, 08:25:17
2 and electrodes that manipulate the liquid crystal 08:25:22
3 itself. Just to be clear, those are the parts of 08:25:25
4 an LCD display where you have not, you know, 08:25:27
5 engaged in designing or proposing alterations to 08:25:32
6 your clients for actual products, right? 08:25:36

7 MR. RODKEY: Objection, mischaracterizes 08:25:39
8 the testimony. 08:25:40

9 A No. I don't think that's what I said. I 08:25:43
10 said primarily the backplane was where the design 08:25:48
11 work specifically was focused, you know, answering 08:25:55
12 the specific question about design -- in answering 08:26:05
13 the question specifically about my work at 08:26:11
14 Exponent. 08:26:13

15 Q So can you give me an example of a project 08:26:25
16 or consulting relationship where you designed, you 08:26:48
17 know, a light-emitting component, as you put it, 08:26:53
18 of an LCD display? 08:26:55

19 A If you go outside of my work at Exponent, 08:26:59
20 during my graduate research work, we -- you know, 08:27:14
21 I developed a light-emitting liquid crystal-based 08:27:18
22 optical filter - developed, designed, and built 08:27:25

1 that device in the laboratory. So that's one 08:27:31
2 example. 08:27:38

3 Q Can you give me an example from during the 08:27:38
4 time you've worked at Exponent? 08:27:43

5 A In as much as the backplane design affects 08:28:03
6 the -- what optical devices or optical components 08:28:35
7 can be used, I think that -- my backplane design 08:28:42
8 experience is going to, you know, incorporate 08:28:47
9 considerations of the optical device, so I refer 08:28:51
10 you to those design experiences you asked me. 08:28:54

11 Q Can you give me an example of during your 08:29:06
12 time at Exponent a project where you worked on the 08:29:16
13 backplane components that would fall into the 08:29:24
14 backplane of an LCD panel, and specifically what 08:29:31
15 components you were involved with and what -- how 08:29:34
16 the work you did related to, you know, the design 08:29:40
17 of a product that was actually sold? 08:29:47

18 MR. RODKEY: Objection, form. 08:29:52

19 A Sure. We worked on a number of projects 08:29:53
20 that were related to liquid crystal displays. 08:30:06
21 We -- I directed and myself tore down and 08:30:13
22 disassembled and analyzed and identified design 08:30:18

1 alternatives for the pixel drivers themselves for 08:30:29
2 certain of the backplane circuits, like the driver 08:30:43
3 circuitry, the backlight circuitry, and the 08:30:48
4 backlight optical design. 08:30:55

5 These were, in some cases, products that 08:31:02
6 were sold on the marketplace. Don't really recall 08:31:06
7 much more detail about if they were sold other 08:31:12
8 than that. 08:31:15

9 Q I'd like to go through the components, I 08:31:19
10 guess we can call them, that you identified: The 08:31:40
11 pixel drivers, backplane circuits, like, driver 08:31:42
12 circuitry and the backlight circuitry. 08:31:48

13 So let's start with pixel drivers. What 08:31:50
14 do you mean by pixel drivers? 08:31:53

15 A When I was speaking and identifying pixel 08:32:01
16 drivers, I was identifying the transistors and 08:32:06
17 other components that may be associated with each 08:32:09
18 individual pixel and typically located at 08:32:12
19 the -- within the area, the optical area, of 08:32:18
20 the -- of the pixel -- or the -- adjacent to it. 08:32:23

21 Q Can you give me an example of a pixel 08:32:39
22 driver? 08:32:45

1	A Just broadly speaking, you know, you'll	08:33:08
2	have a -- at least one transistor in many designs	08:33:11
3	for the circuit I'm referring to that will have a	08:33:15
4	gate. And if the gate is activated, then the	08:33:19
5	current or voltage or signal is applied to the	08:33:30
6	pixel, individual pixel electronics,	08:33:34
7	electrical -- electrode to turn on or off that	08:33:40
8	particular pixel.	08:33:44
9	Q So your description of the -- of a pixel	08:33:56
10	driver, how does that fit into the distinction you	08:34:16
11	drew, you know, between the backplane and the sort	08:34:21
12	of light-emitting components as you -- as you sort	08:34:25
13	of split those into separate buckets?	08:34:31
14	A In -- in my -- in the terminology that	08:34:36
15	I've been using, the -- that pixel driver	08:34:40
16	circuitry is part of the backplane.	08:34:44
17	Q So the -- you know, the LCD display	08:34:48
18	generally has transistors connected to pixel	08:34:55
19	electrodes that are connected to the transistors	08:34:59
20	are connected to the scan and data lines and then	08:35:04
21	the transistor connect those to the pixel	08:35:07
22	electrode.	08:35:11

1	So for you, that is an example of a	08:35:12
2	backplane part of an LCD display; is that right?	08:35:17
3	A Yeah. Those electronic components are	08:35:26
4	part of the backplane.	08:35:36
5	Q All right. Let's go back to the driving	08:35:38
6	circuits that you mentioned. Can you give me an	08:35:45
7	example of what you mean by a driver circuit in	08:35:54
8	this context?	08:35:58
9	A Typically, they'll be scan line driver	08:35:59
10	circuitry, data line driver circuitry, and in	08:36:06
11	combination, working together, those circuits	08:36:13
12	provide signals to the individual pixels to create	08:36:18
13	the image using the optical components on the	08:36:27
14	display.	08:36:33
15	Q Are you familiar with a gate driver on	08:36:34
16	array or GOA LCD panel in terms of what that means	08:37:13
17	for the scanning line driver circuit?	08:37:23
18	A Not sure if I usually use the term GOA.	08:37:33
19	Is that what you said?	08:37:37
20	Q Are you familiar with that term though?	08:37:38
21	A I'd appreciate if you define it for me.	08:37:43
22	Q Have you heard GOA or GOA a driver on	08:37:46

1 array terminology used in your professional
2 experience?

08:37:55

08:37:59

3 MR. RODKEY: Objection, relevance.

08:38:01

4 A In a general sense I've heard that
5 acronym. I was being asked about GOA so I want to
6 understand what I'm being asked.

08:38:02

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7 Q Taking the example of a scanning line
8 driving circuit, the circuitry for a scan line
9 driver can be contained in a -- a chip or it can
10 be part of the -- or it can be formed on the
11 display substrate of an LCD display, right?

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08:39:09

12 A There are a number of ways that you could
13 implement a scan line driving circuit. And just
14 using the very general premise of your question,
15 the circuit could be implemented on a chip. Scan
16 line driver circuit could be implemented on the
17 substrate on which the pixels are found. It could
18 be implemented other ways.

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19 Q What is your experience, you know, working
20 on the design, proposing design alterations for
21 scan line driving circuits that are implemented on
22 the substrate on which the pixels are found?

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1	A Yeah. Some of my work has included	08:40:52
2	looking at scan line driving circuitry implemented	08:40:59
3	on the substrate where the pixels are located.	08:41:06
4	Yeah.	08:41:09
5	Q Can you give me an example?	08:41:16
6	A I'm sorry, an example of what?	08:41:20
7	Q Of your work that has included looking at	08:41:28
8	scan line driving circuits that are implanted on	08:41:30
9	the substrate where the pixels are located.	08:41:35
10	A Sure. In a general sense, the backplane	08:41:37
11	electronics can be implemented using amorphous	08:41:48
12	silicon-type of material and related materials	08:41:55
13	when the backplane electronics are manufactured	08:42:05
14	directly on the substrate where the pixels are.	08:42:07
15	And so some of my experience is looking at and	08:42:13
16	analyzing, proposing alternatives to amorphous	08:42:19
17	silicon deposition technologies other material	08:42:25
18	technologies related to the amorphous silicon	08:42:36
19	material system.	08:42:41
20	Q So the -- that example you just gave, you	08:43:04
21	were analyzing and proposing alternatives to the	08:43:29
22	amorphous deposition technologies. That is how	08:43:34

1 the circuitry would be formed in manufacturing,
2 right?

3 A In that specific example I mentioned to
4 you, the deposition technology and the material
5 selection is part of the manufacturing process.
6 Yeah.

7 Q Can you give me an example in this same
8 context of scan line driving circuit that is
9 implemented on the pixel substrate where you were
10 involved in the design of the circuitry itself?

11 A So the example I gave you is part of the
12 design of the circuitry.

13 Q Can you walk me -- walk me through that?
14 How is it part of the design of the circuitry?

15 A In at least the following sense that
16 depending on the material parameters of the
17 amorphous silicon layer, the exact manufacturing
18 specifications, and achievable outputs of the
19 manufacturing, those factors will determine the
20 electrical characteristics of the transistors,
21 other components, and among other things, the size
22 of the transistors. And if you look at the

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1 metallization, it's going to affect the 08:45:45
2 connectivity of the components. And all that 08:45:48
3 ramifies to the design of the scan line driving 08:45:54
4 circuit that you're trying to manufacture. 08:46:02

5 Q So in the -- in the example you're 08:46:15
6 referring to where you were involved in the, you 08:46:20
7 know, say the material parameters or the 08:46:33
8 deposition technologies, etcetera, that you just 08:46:35
9 mentioned, were you starting from a fixed design 08:46:38
10 or a -- does the -- does the design of the 08:46:45
11 circuitry come first and then your -- the work you 08:46:48
12 did comes after that, or does the work you did 08:46:55
13 come before the actual design of the circuitry? 08:46:59

14 MR. RODKEY: Objection, form. 08:47:03

15 A I think I just told you that the example I 08:47:04
16 provided is part of the circuitry design. So I'm 08:47:10
17 not sure I'm understanding the distinction you're 08:47:16
18 trying to draw. 08:47:19

19 Q So that -- that is one example of, you 08:47:21
20 know, work you've done at Exponent relating to 08:47:58
21 scan line drivers that are integrated on the pixel 08:48:02
22 substrate. Should we -- is it okay if we refer to 08:48:05

1 the pixel substrate moving forward to clarify what 08:48:09
2 we're talking about? 08:48:13

3 A That's fine. We can talk about the pixel 08:48:17
4 substrate as the substrate on which the pixels are 08:48:20
5 located. 08:48:24

6 Q Which in order to identify that we're 08:48:27
7 talking about a scan line driving circuit that is 08:48:31
8 on the -- not -- not in -- not a discrete 08:48:36
9 integrated circuit chip, right? 08:48:43

10 MR. RODKEY: Objection, form. 08:48:46

11 A Just have to understand what you mean by 08:48:47
12 "on" I guess if you're trying to draw some 08:48:55
13 distinction between different types of circuits. 08:48:58

14 Q Yeah. Let's make sure we're on the same 08:49:01
15 page. 08:49:03

16 So for scanning line driving circuit, 08:49:03
17 which is it true that those are also referred to 08:49:10
18 as a gate driving circuit? 08:49:14

19 A Yes. Those can be referred to as a gate 08:49:16
20 driver or gate driver circuitry, gate line driver 08:49:19
21 circuitry. 08:49:23

22 Q Those terms are effectively 08:49:24

1	interchangeable?	08:49:26
2	A I think in the analysis I did related to	08:49:27
3	the '157 patent, I've generally used "scanning	08:49:34
4	line" and "gate line" more or less	08:49:39
5	interchangeably.	08:49:43
6	Q Okay. So a scan line driving circuit, one	08:49:44
7	way it can be implemented is where it is formed on	08:49:52
8	the same substrate as the pixel array, right?	08:50:00
9	A I think when I was asked earlier, I said	08:50:09
10	that's one way it could be done.	08:50:12
11	Q What are the other ways it can be done?	08:50:13
12	A The -- could have scan line driving	08:50:17
13	circuitry that's not on the pixel substrate. That	08:50:31
14	is an alternative that, you know, that may happen.	08:50:42
15	Q When -- with that alternative, would the	08:50:49
16	circuitry be contained in a -- in a chip, like an	08:50:54
17	integrated chip that is a discrete component that	08:51:00
18	is not formed as part of the -- the actual pixel	08:51:09
19	substrate?	08:51:16
20	A In the hypothetical that I'm -- have in	08:51:18
21	mind, there are a few ways to make circuitry that	08:51:26
22	might be for a scan line driver circuit. And one	08:51:32

1 of the ways to do that would be to manufacture the 08:51:38
2 scan line driver circuitry on a chip. That's 08:51:42
3 quite common, to manufacture integrated circuits 08:51:47
4 on a chip. 08:51:50

5 Q So you have worked -- have you worked on 08:51:51
6 both types of scan line driving circuits 08:52:29
7 implemented on -- you know, formed as part of the 08:52:33
8 pixel array substrate and then formed, you know, 08:52:34
9 on a silicon substrate that is -- is a discrete 08:52:42
10 chip, right? Have you worked on both? 08:52:46

11 A Well, again, I'm not -- I made the 08:53:01
12 distinction earlier of scan line driver circuits 08:53:04
13 that are formed on the pixel array -- I'm sorry, 08:53:09
14 the pixel substrate and scan line driver circuits 08:53:14
15 that are not formed on the pixel substrate. And 08:53:25
16 yes, I have worked on both types of those 08:53:29
17 implementations. 08:53:43

18 Q And so for scan line driver that are not 08:53:43
19 formed on pixel substrate, we're talking about 08:53:47
20 integrated circuit chips, right, like a computer 08:53:53
21 chip? 08:53:56

22 A That's most commonly how scan line driver 08:53:56

1 circuits might be implemented if they're not on
2 the pixel substrate. Yeah.

3 Q And your answer is in terms of LCD
4 displays; is that right?

5 A I think generally, yes.

6 Q I just want to make sure if you're
7 referring -- if your answer was broader than that,
8 I just want to make sure we're on the same page.
9 So okay.

10 I believe you gave me one example of, you
11 know, experience you have at Exponent where you
12 worked on a scan line driver that was formed on a
13 pixel substrate, right?

14 A Yes. I talked about some of that work.

15 Q Can you give me an example of work you've
16 done on a scan line driving circuit that's
17 contained in a chip?

18 A Sure. Worked on a series of projects
19 comparing the relative performance and the
20 relative manufacturability, relative reliability
21 of a variety of different liquid crystal displays,
22 some of which had the scan line driver circuitry

1 not on the pixel substrate. 08:56:29

2 Q So when the scan line driving circuitry is 08:56:33
3 not on the pixel substrate, what -- what substrate 08:56:52
4 is the circuitry formed on? 08:57:03

5 A Well, if the circuitry is not formed on 08:57:19
6 the pixel substrate, it's going to be formed on 08:57:22
7 logically a different substrate, most commonly, a 08:57:25
8 silicon substrate for integrated circuits that I 08:57:31
9 have had experience with. 08:57:37

10 Q And in that case, the circuitry that's 08:57:37
11 formed on a silicon substrate when it's packaged, 08:57:51
12 it is in the form of a chip with, you know, pin 08:57:58
13 outs, inputs and outputs, right? 08:58:05

14 A That's -- yeah. That's a common way to 08:58:09
15 manufacture integrated circuits, yes. 08:58:13

16 Q And in the context of a scanning line 08:58:15
17 driving circuit that is formed on a silicon 08:58:19
18 substrate and is packaged as a chip, that chip has 08:58:23
19 to be connected to the circuitry that is on the 08:58:28
20 pixel substrate of an LCD panel, right? 08:58:39

21 A You would typically need a connection of 08:58:54
22 some point, some kind, from a scanning line driver 08:58:58

1 circuit that's not on pixel substrate to the pixel
2 substrate of some kind to get your display to
3 work. I think that's fair to say.

4 Q So you've -- you said that you've worked
5 on both types of scan line driving circuits formed
6 -- those that are formed on pixel substrate and
7 those that are not which are typically computer
8 chips, right?

9 A Yes. I -- that's what I said. I think
10 the premise still holds.

11 Q Okay. How many times in your professional
12 experience at Exponent have you worked on scan
13 line driving circuits that are formed on the pixel
14 substrate as compared to formed on an IC chip?

15 A That would be hard for me to count. The
16 experience I mentioned a little while ago about
17 comparing the performance of different
18 implementations was a multiyear, three or
19 four-year type of project we did. So I couldn't
20 say, you know, exactly how many I looked at, but
21 it was -- it was quite a number.

22 Q The experience you are referring to here

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1 is -- which -- which example are you talking 09:01:17
2 about? 09:01:23

3 A The one you asked me about. I was asked 09:01:23
4 about the experience related to scan line driver 09:01:31
5 circuitry that's formed not on the pixel 09:01:39
6 substrate, and that's what I was referring to. 09:01:45

7 Q Thank you. So let me ask a question in a 09:01:47
8 different way. 09:02:00

9 So in terms of the amount of time you have 09:02:00
10 spent working on scanning line driving circuits 09:02:05
11 formed on the pixel substrate versus scanning line 09:02:14
12 driving circuits that are not formed on the pixel 09:02:17
13 substrate, do you have an estimate of, you know -- 09:02:20
14 you mentioned you spent a number of years in your 09:02:24
15 last example. Can you estimate the breakdown in 09:02:28
16 terms of time spent over the course of your 09:02:35
17 professional experience at Exponent? 09:02:41

18 A It's not an easy question to answer. I 09:02:41
19 would say it's not weighted extremely to one or 09:02:49
20 the other. Very roughly and approximately equal 09:02:53
21 if I had to give an estimate. 09:03:01

22 Q And roughly and approximately, how 09:03:09

1 do -- how does the, you know, time you spent 09:03:12
2 working on scanning line driving circuits formed 09:03:16
3 in any fashion compare to the other work that 09:03:20
4 you've done at Exponent? 09:03:26

5 A Are you talking about my entire career at 09:03:40
6 Exponent? 09:03:44

7 Q Yeah. I'm just looking to get a sense 09:03:45
8 of -- well, let me ask it this way. 09:03:56

9 We've talked about work you've done 09:03:58
10 relating to the design of driving circuitry, 09:04:02
11 specifically we've been talking about scan line 09:04:05
12 driving circuitry. 09:04:08

13 And we've generally been talking about 09:04:09
14 circuitry that relates to LCD panels. What I'm 09:04:13
15 getting at is how does that -- the extent of that 09:04:19
16 work experience compare to work you've done that 09:04:24
17 is unrelated to those categories? 09:04:28

18 A I think the vast majority of my work at 09:04:40
19 Exponent has been related to those categories. 09:04:43
20 Most -- many of my projects are related to 09:04:50
21 semiconductor devices, fabrication technology for 09:04:55
22 the semiconductor devices, the performance of 09:04:59

1 semiconductor circuits and electronic products in 09:05:03
2 general. So there's -- are many, many 09:05:06
3 commonalities between the scan line driver 09:05:15
4 circuits that we're talking about, the pixel 09:05:18
5 driver circuits that I discussed earlier, whether 09:05:21
6 it's on a -- you know, one substrate or another. 09:05:25

7 And so all of that experience is common 09:05:30
8 and feeds into my, you know, understanding 09:05:35
9 of -- of the issues that are in front of us here 09:05:39
10 in regards to the '157 patent. So I think, you 09:05:42
11 know, quite a lot of experience, you know, related 09:05:47
12 to these technologies. 09:05:50

13 Q I believe you mentioned earlier, and 09:05:51
14 correct me if I'm wrong, that you -- you performed 09:06:08
15 a -- did you say you performed a tear-down of a 09:06:12
16 display product as part of one of the consulting 09:06:16
17 engagements that you have been involved with? 09:06:20

18 MR. RODKEY: I'm going to object to the 09:06:28
19 extent it asks for confidential information of a 09:06:30
20 third party. And if the witness can answer 09:06:32
21 without releasing confidential information, you 09:06:35
22 can proceed. 09:06:38

1	A I have done tear-down of, you know, liquid	09:06:39
2	crystal display product in my career. Yeah.	09:06:47
3	Q Have you -- have you done that more than	09:06:50
4	once?	09:06:58
5	A Yes.	09:07:00
6	Q And as a -- as part of that tear-down	09:07:04
7	analysis, did you identify, you know, the circuit	09:07:10
8	layout -- actually, let -- let me start with this.	09:07:17
9	For these tear-down -- work you've done	09:07:21
10	that involved doing -- performing tear-down of an	09:07:32
11	LCD product, did you look at, analyze imagery of	09:07:34
12	the pixel substrate circuitry or the circuitry	09:07:54
13	that exists on the pixel substrate?	09:07:58
14	A Yes. I believe I did. Yeah.	09:08:11
15	Q Did -- for any of the work that you've	09:08:49
16	done that related to tear-down of an LCD display,	09:08:52
17	were you analyzing the imagery of the circuitry on	09:08:57
18	the pixel substrate, did any of that work require	09:09:01
19	you to identify specific components, circuit	09:09:03
20	components, on the broader -- on the whole -- from	09:09:10
21	the whole -- let me put it this way.	09:09:14
22	In the tear-down work you've done on LCD	09:09:17

1 displays, you're analyzing imagery of the 09:09:23
2 circuitry that exists on the pixel substrate, have 09:09:28
3 you identified specific circuit components, for 09:09:31
4 example, like, yeah, there's the scan line driving 09:09:37
5 circuit that is formed on pixel substrate? 09:09:40

6 A In the most broad sense, yes, I identified 09:09:44
7 various components of the circuitry during that 09:09:53
8 tear-down work. 09:09:57

9 Q Do you know what a GDS file is? 09:09:59

10 A Heard that terminology before, yes. 09:10:10

11 Q What is your understanding of what that 09:10:21
12 terminology refers to? 09:10:25

13 A When I hear the terminology GDS file, I 09:10:34
14 understand it to mean, to me, layout files that 09:10:42
15 show the -- generally, the placement of different 09:10:52
16 components and subcomponents and materials that is 09:11:00
17 used in manufacturing design of semiconductor 09:11:09
18 devices. 09:11:17

19 Q Have you ever reviewed a GDS file for an 09:11:24
20 LCD device? 09:11:29

21 A I've reviewed a number of GDS files over 09:11:47
22 my career. I don't recall if I've ever looked at 09:11:53

1	one for an LCD product. There have been many.	09:11:56
2	Q Have you ever been to an LCD fabrication	09:12:00
3	facility?	09:12:47
4	MR. RODKEY: Objection, relevance.	09:12:50
5	A I've fabricated, like a crystal-type	09:12:52
6	devices myself in the lab so I've been to that	09:13:06
7	facility. I've also been to an industrial	09:13:09
8	facility that makes -- mass produces LCDs.	09:13:14
9	Q To the -- to the extent you can answer	09:13:34
10	this without getting into confidential consulting	09:13:37
11	relationships you've had in the past, the	09:13:40
12	industrial facility that makes -- that mass	09:13:43
13	produces LCDs you say that you've been to, what	09:13:46
14	was that project? Like, what -- what were	09:13:50
15	you -- what were you involved with doing?	09:13:55
16	A In a -- in a general sense, we were there	09:14:03
17	to observe and inspect the equipment in the	09:14:07
18	context of consulting engagements regarding the	09:14:16
19	design of liquid crystal displays.	09:14:23
20	Q Any other examples you can provide where	09:15:04
21	you've been to an LCD fabrication facility for,	09:15:07
22	you know, mass production outside of the lab	09:15:11

1	context I think you mentioned?	09:15:14
2	MR. RODKEY: Objection, relevance.	09:15:20
3	A If we're sticking to mass production, I	09:15:23
4	visited and inspected other semiconductor	09:15:39
5	manufacturing plants. There are a lot of	09:15:42
6	commonalities to the types of equipment and	09:15:49
7	materials used between other semiconductor devices	09:15:53
8	like chips, silicon chips for memory or	09:15:56
9	microprocesses or other devices. So that would be	09:16:04
10	other examples that is going to be relevant to	09:16:07
11	liquid crystal display manufacturing plants.	09:16:11
12	Q Going back to the description you gave of	09:16:19
13	the -- when you visited the LCD display mass	09:16:38
14	production facility equipment, the context	09:16:46
15	consulting -- of consulting engagements regarding	09:16:56
16	the design of the liquid crystal displays, to the	09:16:57
17	extent you can answer, again, without getting into	09:17:01
18	confidential territory, how did the design	09:17:04
19	consulting work you related -- related to, you	09:17:11
20	know, why you went to the fabrication facility to	09:17:14
21	observe?	09:17:16
22	MR. RODKEY: Objection, form.	09:17:20

1	A In -- describing it in the broadest way	09:17:23
2	that I hope is getting at your question, the	09:17:31
3	examples of consulting work where we -- I was	09:17:35
4	comparing the relative performance and materials	09:17:41
5	and manufacturability of different designs of	09:17:46
6	LCDs, that included comparative analysis of the	09:17:54
7	equipment used to manufacture the different	09:18:04
8	designs of LCDs. So the site visit to the plant	09:18:12
9	was in the context of that project.	09:18:19
10	Q Understood. Thank you.	09:18:25
11	MR. JONES: We can go off the record now	09:18:27
12	for a quick break.	09:18:29
13	(Whereupon a break was had.)	09:19:29
14	THE VIDEOGRAPHER: We're going back on the	09:25:18
15	record. The time is 9:25 a.m.	09:25:22
16	BY MR. JONES:	09:25:25
17	Q Welcome back, Dr. Murphy. I'd like to	09:25:29
18	switch over to learning more about your experience	09:25:33
19	as it relates to ways to protect circuitry from	09:25:37
20	electrostatic damage or ESD.	09:25:44
21	Do you understand what I mean by	09:25:48
22	electrostatic damage and ESD, right?	09:25:52

1 A In general, yeah. ESD can refer also to
2 electrostatic discharge.

3 Q And you know, the -- broadly speaking, the
4 '157 patent that relates to ESD protection, right?

5 A That's one of the things that is related
6 to ESD protection.

7 Q Give me a sense of your experience at
8 Exponent that relates to ESD protection for
9 integrated circuits generally.

10 A So to preface, I have experience that
11 predates my experience at Exponent, something I
12 mentioned in my declaration, education, the design
13 of ESD protection circuits, circuitry, testing of
14 electrostatic discharge.

15 But your question is related to my
16 experience at Exponent. My declaration at
17 paragraph 13, I -- and 14, I mention some of that
18 experience. Primarily, it's related to
19 identifying failures of electronic circuitry and
20 assessing whether the failures were due to ESD
21 phenomena, and in some cases testing electronic
22 components for vulnerability to ESD events.

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1 Q So for the electronic circuitry,
2 electronic components we were just -- you just
3 referred to, were those components and was the
4 circuitry contained in a silicon IC chip?

09:28:24

09:29:26

09:29:30

09:29:40

5 A If we're talking about the experience at
6 Exponent that you had asked about, if we're
7 talking about my examples of experience, primarily
8 those were devices that were fabricated on a
9 silicon chip. Yes.

09:29:50

09:29:54

09:29:56

09:30:04

09:30:07

10 Q Do you have -- do you have any experience,
11 you know, relating to ESD protection or evaluating
12 the -- whether failure was caused by ESD in the
13 context of circuitry that is formed on pixel
14 substrate of an LCD panel?

09:30:08

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09:30:32

09:30:38

09:30:48

15 A You know at the moment, I can't recall a
16 particular instance where ESD was the issue. I
17 know that when, you know, looking at LCD failures,
18 yeah, I know that's an issue. When we do failure
19 analysis, what I do failure analysis of LCDs or
20 other electronic devices, ESD is one thing to
21 investigate and rule out potentially and then move
22 on to other potential root causes. I've

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09:31:04

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1 encountered ESD protection circuits commonly and 09:31:33
2 generally in LCD circuitry that I've analyzed. 09:31:38

3 So yeah, I -- to answer your question, I 09:31:46
4 have encountered ESD protection on LCD and -- and 09:31:50
5 products manufactured on substrates other than 09:31:58
6 silicon. 09:32:04

7 Q Have you, yourself, or have you been 09:32:05
8 involved with, you know, designing the ESD 09:32:26
9 protection means for a -- for circuitry that's on 09:32:32
10 a pixel substrate of an LCD panel? 09:32:42

11 A Yes, in as much as the circuitry is for 09:32:47
12 ESD protection manufactured typically at the same 09:33:02
13 time, same processes as other circuit -- circuit 09:33:09
14 elements on glass substrates or substrates you 09:33:13
15 might use for LCDs, yeah, design of those circuits 09:33:19
16 would be included. 09:33:26

17 Q Can you give me an example of a specific 09:33:28
18 project or consulting engagement that related to, 09:33:49
19 you know, the design of circuitry that's on a 09:33:56
20 glass or LCD substrate and how it related to ESD 09:33:59
21 protection? 09:34:06

22 A Sure. I have in mind the work I discussed 09:34:09

1 earlier about amorphous silicon transistor

09:34:14

2 technology for display in liquid crystal display

09:34:22

3 backplanes. So some of the circuits that were

09:34:30

4 fabricated were -- included ESD protection

09:34:34

5 circuits.

09:34:42

6 Q Can you remind me, again, what you mean by
7 backplane?

09:34:45

09:34:52

8 A I think I mentioned earlier, in a general
9 sense, the way I'm using it today and others may,
10 you know, adopt other definitions as the context
11 might permit, using backplane to distinguish
12 electronics, electrical devices, associated with a
13 display as -- distinguished those from the optical
14 elements of a display.

09:34:55

09:35:04

09:35:12

09:35:15

09:35:20

09:35:33

09:35:37

15 Q Give me the experience you have relating
16 to ESD protection for circuitry formed on glass or
17 pixel substrate of an LCD display related
18 specifically to the scan line driving circuitry
19 and the wirings that drive that circuit.

09:35:41

09:36:32

09:36:42

09:36:45

09:36:57

20 A I don't have a specific recollection of
21 which circuits were being protected by these ESD
22 devices that were part of, you know, the work I

09:37:12

09:37:33

09:37:36

1 was doing designing the backplane for displays. I 09:37:41
2 think there are -- I think -- I think that it 09:37:48
3 would be common, and as I discuss in my 09:38:08
4 declaration, commonly understood that there are 09:38:14
5 benefits to protecting scan line driver circuitry 09:38:19
6 but I don't have a specific recollection as to 09:38:24
7 what subcircuits or circuits were being protected 09:38:27
8 during my work. 09:38:32

9 Q Fair to say you have experience with ESD 09:38:33
10 protection circuits and, you know, ESD protection 09:38:54
11 generally for both silicon ICs and circuitry 09:38:59
12 that's formed on a glass or pixel substrate of an 09:39:05
13 LCD display, right? 09:39:11

14 A Yes. 09:39:12

15 Q Can you tell me -- this was a question I 09:39:12
16 was asking earlier, you know, relatively how much 09:39:32
17 of your time that you've spent working on ESD 09:39:36
18 protection in the context of silicon ICs versus 09:39:43
19 circuitry that's formed on a glass or pixel 09:39:50
20 substrate of an LCD panel? 09:39:55

21 A I think the nature of my answer would be 09:39:57
22 imprecise. I would say more has been directed to 09:40:05

1 silicon devices on silicon substrate than the 09:40:12
2 other types of substrates. 09:40:15

3 Q Is it true that there are different 09:40:37
4 considerations for ESD protection between silicon 09:40:39
5 IC versus circuitry that's formed on glass or 09:40:46
6 pixel substrate of an LCD panel; is that right? 09:40:55

7 A I'd say the similarities when considering 09:40:59
8 ESD protection for these different type of 09:41:11
9 substrates far outweigh the differences, I think, 09:41:14
10 and this is in my declaration as well regarding 09:41:19
11 the background of the technology, that glass 09:41:28
12 substrates maybe, in some instances, have 09:41:38
13 different vulnerabilities than other substrates. 09:41:41
14 But similarities I think are -- are -- far 09:41:44
15 outweigh the differences. 09:41:52

16 Q So those different vulnerabilities you 09:41:54
17 mentioned and you -- I think you addressed this in 09:42:03
18 your declaration as well, does that relate to the 09:42:07
19 fact that the circuitry is formed on an 09:42:13
20 insulating, as compared to a noninsulating or less 09:42:17
21 insulating, silicon substrate? 09:42:24

22 A That's the nature of the difference, the 09:42:36

1 primary difference, and indeed what I discuss in 09:42:38
2 the declaration. Yes. Right. I'll direct you 09:42:42
3 to, say, paragraph 48, for instance, of my 09:42:49
4 declaration which addressed that. 09:42:53

5 Q Sounds like you have your declaration open 09:43:01
6 in front of you; is that right? 09:43:03

7 A I do. Yeah. 09:43:05

8 Q So you know, the insulating substrate, you 09:43:06
9 identified that as the primary difference. 09:43:14

10 Any other differences in your opinion? 09:43:18

11 A Not any significant differences when it 09:43:20
12 comes to ESD other than that. 09:43:41

13 Q Are you familiar with an individual named 09:43:56
14 Dr. Shukri Souri, S-O-U-R-I who also works at 09:44:00
15 Exponent? 09:44:06

16 MR. RODKEY: Objection, relevance. 09:44:06

17 A I am familiar with Dr. Shukri Souri. 09:44:08

18 Q His name is pronounced Souri? 09:44:17

19 A Yes. 09:44:20

20 Q Do you work with Dr. Souri? 09:44:20

21 MR. RODKEY: Objection, relevance. 09:44:40

22 A Yes. 09:44:41

1 Q Is he in the same -- does he work out of
2 the same office as you?

3 MR. RODKEY: Same objection.

4 A He does work out of the New York office as
5 well as I do.

6 Q Have you spoken with Dr. Souri about your
7 opinions in support of the '157 IPR?

8 A No. I have not.

9 Q Are you aware that Dr. Souri is serving as
10 a technical expert for BOE, Petitioner in this IPR
11 in a related district court litigation?

12 MR. RODKEY: Objection, relevance.

13 A I'm sorry, could you restate that part
14 about IP -- an IPR matter?

15 Q Yeah. Are you aware that Dr. Souri is
16 serving as a technical expert for BOE, which is
17 the petitioner in this IPR matter, and that
18 Dr. Souri is serving as an expert for BOE in a
19 related district court litigation matter?

20 MR. RODKEY: Objection.

21 A I am generally aware that Dr. Souri is
22 providing technical consulting services to BOE in

1 a district court matter. I'm not familiar with 09:46:27
2 how that district court matter, or others that may 09:46:31
3 exist or other litigations for that matter 09:46:35
4 involving BOE, may be related to this IPR for the 09:46:39
5 '157 patent. 09:46:45

6 Q Are you aware that Dr. Souri has opined 09:46:46
7 invalidity and noninfringement in expert reports 09:47:06
8 in district court litigation on behalf of BOE? 09:47:10

9 MR. RODKEY: Objection, relevance. 09:47:14
10 Counsel this is about the IPR matter, not district 09:47:16
11 court. 09:47:19

12 MR. JONES: I am not going to spend much 09:47:20
13 more time on this. 09:47:22

14 A I'm generally aware that his role is to 09:47:27
15 provide opinions in the district court matter that 09:47:30
16 you're referring to. I don't know the status of 09:47:32
17 expert reports so I'm not specifically aware on 09:47:36
18 whether he's provided opinions to date. 09:47:41

19 Q So you haven't spoken to him about, you 09:47:48
20 know, what his opinions are? 09:47:50

21 MR. RODKEY: Objection, relevance. 09:47:52

22 A I haven't spoken to him about his opinions 09:47:55

1 related to the district court or BOE litigations

09:47:59

2 that, you're, you know, referencing, no.

09:48:07

3 Q And just to wrap this up, the inverse of

09:48:10

4 that question: You haven't spoken to Dr. Souri

09:48:14

5 about your opinions in this, you know, in support

09:48:18

6 of the '157 IPR petition, right?

09:48:24

7 A I think I answered that already. The

09:48:28

8 answer is still no, I haven't spoken with him

09:48:30

9 about -- about that.

09:48:32

10 Q Okay.

09:48:34

11 MR. JONES: Let's mark as Exhibit 1003 the

09:48:40

12 file -- file name '157 IPR-EX 1003 Murphy

09:48:47

13 declaration.

09:48:56

14 (Exhibit 1003 marked for identification.)

09:49:05

15 MR. JONES: Kevin, would you like me to

09:49:05

16 drop that into the chat.

09:49:08

17 MR. RODKEY: Yes, please. If you'll put

09:49:09

18 all exhibits into the chat.

09:49:12

19 BY MR. JONES:

09:49:20

20 Q And Dr. Souri -- sorry, Dr. Murphy,

09:49:21

21 similar syllables in there.

09:49:24

22 If you'd like to use the copy you have

09:49:26

1	open in front of you or with you, that is fine	09:49:29
2	too. You don't need to look at the Zoom screen.	09:49:32
3	I leave it up to you.	09:49:35
4	A Okay.	09:49:37
5	Q All right. So Exhibit 1003, this is your	09:49:37
6	declaration in support of the '157 IPR petition,	09:49:43
7	right?	09:49:46
8	A Yes. That's what it looks like being	09:49:46
9	shown.	09:49:50
10	Q And it contains your opinions regarding	09:49:50
11	the patentability of claims 1 through 18 of the	09:49:55
12	'157 patent, which is all claims of the '157	09:49:59
13	patent, right?	09:50:02
14	A Yes. That's what I have at paragraph 4 of	09:50:04
15	the declaration.	09:50:09
16	Q And your opinions are two grounds and	09:50:10
17	those are based on two prior art reference, right?	09:50:31
18	A Well, one -- the first ground is based on	09:50:34
19	one prior art reference; second is based on is the	09:50:42
20	same and then an additional prior art reference.	09:50:46
21	So that's two references total.	09:50:49
22	Q Right. So the first one -- first	09:50:51

1	reference is Reiner, which is International	09:50:54
2	Publication Number WO 03/019657, right?	09:50:57
3	A It -- I agree that it's Reiner and I'll	09:51:04
4	take your word for it, the specific patent number.	09:51:10
5	Q Okay. And we refer to that as Reiner,	09:51:13
6	we're both talking about the same thing?	09:51:16
7	A Yes. That's fine.	09:51:20
8	Q Okay. And then the other prior art	09:51:21
9	reference you refer to as Takahara in your	09:51:24
10	declaration which is Japanese Patent Application	09:51:31
11	No. 2003-121875. That sound right to you?	09:51:34
12	A Yes.	09:51:41
13	MR. RODKEY: Counsel -- never mind.	09:51:41
14	MR. JONES: Sorry, Counsel, was there an	09:51:45
15	objection?	09:51:47
16	MR. RODKEY: No. I thought you misspoke	09:51:48
17	on the number, but looks like the transcript is	09:51:50
18	correct.	09:51:53
19	Q Okay. Dr. Murphy, can you describe the	09:51:54
20	process by which you formed your opinions that are	09:52:01
21	in your declaration?	09:52:06
22	A I think the general process is described	09:52:19

1 at thereabouts paragraph 33. I considered the 09:52:25
2 patent claims of the '157, reviewed the two prior 09:52:35
3 art references and did my analysis as to, you 09:52:43
4 know, whether the claims would have been 09:52:49
5 considered obvious in light of one and then the 09:52:53
6 combination. And you know, expressed the opinions 09:52:56
7 and explanations in the report that's here in the 09:53:04
8 declaration. 09:53:07

9 Q And did you speak or communicate with 09:53:08
10 anyone else in forming your opinions? 09:53:17

11 MR. RODKEY: Objection, privileged. Dr. 09:53:21
12 Murphy, to the extent you can answer without 09:53:25
13 divulging the substance of conversations with 09:53:27
14 counsel, you can proceed. 09:53:30

15 A In general, worked with counsel in 09:53:32
16 drafting the declaration and a colleague at 09:53:45
17 Exponent as part of the drafting as well. 09:53:51

18 Q Who was the colleague at Exponent you 09:53:56
19 worked with? 09:54:07

20 A That would have been Dr. Daniel Palmer. 09:54:08

21 Q And what is his role or title at Exponent? 09:54:12

22 A His current title, if I remember 09:54:20

1 correctly, is senior associate. He's a remember
2 of the consulting staff in the New York office in
3 the electrical engineering and computer science
4 practice at Exponent.

09:54:28

09:54:30

09:54:34

09:54:36

5 Q So Dr. Palmer is sort of serving as your
6 support staff for your work on this -- on your
7 declarations support of '157 IPR petition?

09:54:38

09:54:47

09:54:50

8 A Yeah. That's a fair description.

09:54:55

9 Q In other words, you know, the opinions in
10 your declaration are yours, not Dr. Palmer's?

09:54:58

09:55:00

11 A He may share them, but they are mine.

09:55:07

12 Yes.

09:55:10

13 Q All right. Then you mentioned you spoke
14 to counsel. Can you tell me who you spoke with?

09:55:16

09:55:20

15 MR. RODKEY: I'm going to object on
16 privilege grounds. To the extent you can recall
17 names, you can provide them.

09:55:27

09:55:29

09:55:33

18 A The only individual I can recall right
19 now, Mr. Kevin Rodkey, of Finnegan.

09:55:35

09:55:43

20 Q Did you speak to anyone from BOE in
21 forming your opinions in your declaration?

09:55:52

09:55:58

22 A No. I did not, to the best of my

09:56:00

1	recollection.	09:56:09
2	Q And did you write your declaration	09:56:13
3	yourself?	09:56:14
4	A As I indicated, sections were drafted by	09:56:15
5	me or by those I was working with. I reviewed and	09:56:22
6	agreed and clearly signed off on the declaration	09:56:29
7	so they're my words.	09:56:36
8	Q Could you turn please to paragraph 49	09:56:39
9	which is on page 34 of your declaration. Can you	09:57:28
10	just read paragraph 49 to refresh your memory of	09:57:37
11	what it says to the extent you need to?	09:57:40
12	A I'll do that. Okay.	09:57:43
13	Q So your opinion here in paragraph 49 is	09:58:22
14	that the '157 patent discusses known conventional	09:58:28
15	ESD protection methods, right?	09:58:35
16	A Not sure I'd call that an opinion. I'm	09:58:41
17	identifying passages where the '157 patent	09:58:44
18	discusses conventional methods, you know, for	09:58:53
19	protective circuits for protecting other circuits	09:58:57
20	from ESD.	09:59:02
21	Q More specifically, is it correct that the	09:59:05
22	'157 patent describes that conventional ESD	09:59:30

1 protection means to prevent ESD damage that can be 09:59:36
2 caused when static charge or ESD event enters the 09:59:40
3 semiconductor device through terminals? 09:59:44

4 A The '157 patent does identify conventional 09:59:52
5 solutions to a known problem. The problem being 10:00:15
6 ESD and identifies conventional methods including 10:00:23
7 protective circuits for ESD on the input 10:00:29
8 terminals. 10:00:33

9 Q Aside from protective circuits for ESD on 10:00:59
10 the input terminals, is it your opinion that the 10:01:08
11 '157 patent identifies other conventional ESD 10:01:13
12 protection means? I asked because you said 10:01:19
13 "including" in your last answer. 10:01:22

14 A With reference to Figure 11 which is 10:01:43
15 excerpted after figure -- I'm sorry, paragraph 50 10:01:49
16 of my declaration, the location of the ESD devices 10:01:51
17 is shown as being close to the input terminals. 10:01:55
18 So someone reading that in the 15 [sic] patent 10:02:00
19 would understand that it could -- they could 10:02:12
20 provide ESD protection to ESD coming from the 10:02:13
21 input terminals, yes. 10:02:18

22 Q So looking at paragraph 49 specifically, 10:02:20

1	when '157 patent discusses the conventional means	10:03:25
2	to protect against ESD, the -- looks like the	10:03:31
3	second sentence in that paragraph, so states: It	10:03:40
4	is a key issue to prevent the damage when	10:03:43
5	setting -- electricity flows through the input	10:03:47
6	terminals. Then the next sentence:	10:03:48
7	Conventionally, this problem was solved with	10:03:49
8	protective circuits formed between input terminals	10:03:52
9	and the semiconductor device.	10:03:55
10	Right. Did I get that right?	10:03:58
11	A Sounds like you read it correctly. Yeah.	10:04:00
12	Q Do you agree that the devices -- the	10:04:02
13	semiconductor device '157 patent is referring to	10:04:13
14	here refers to a general semiconductor device that	10:04:17
15	is formed on a silicon wafer made of a conductive	10:04:22
16	material?	10:04:28
17	A I don't see that limitation of the	10:04:37
18	substrate in this passage that we're reading out	10:04:40
19	here.	10:04:46
20	Q You have reviewed the '157 patent	10:04:48
21	specification, right?	10:05:15
22	A Yes.	10:05:17

1 Q Do you agree that the -- the background
2 section of the specification laying out
3 conventional ESD protection means -- begins by
4 focusing on how ESD protection is conventionally
5 achieved for silicon-based integrated circuit
6 devices?

7 A Is there a particular passage in the '157
8 you'd like me to consider? You mention the
9 beginning.

10 Q Yeah. Sure, let's --

11 MR. JONES: Let's mark as Exhibit 1001 the
12 file name with -- the document with the file name
13 '157 IPR-EX 1001. Drop one in the chat too.

14 (Exhibit 1001 marked for identification.)

15 Q All right. Dr. Murphy, we're looking at a
16 copy of the '157 patent, correct?

17 A Yes.

18 Q Could you go -- scroll down to the
19 background section of the specification?

20 MR. RODKEY: Sorry, Counsel, before you do
21 that, could you put it in the chat? It's not
22 appearing for me.

1	MR. JONES: Sorry about that. Didn't hit	10:07:31
2	Send. Just sent it again.	10:07:33
3	MR. RODKEY: Thank you.	10:07:36
4	Q All right. Dr. Murphy, the -- I'd like to	10:08:05
5	direct you to column 1 rows 23 to 26.	10:08:08
6	A Okay.	10:08:20
7	Q Dr. Murphy, I see you navigating through	10:08:20
8	Exhibit 1001. Can we go to --	10:08:42
9	A I'm sorry. I'm not scrolling through. I	10:08:44
10	have the background on my local copy here in my	10:08:47
11	line of sight. I'm not sure who is scrolling on	10:08:52
12	the copy that's being shared in the Zoom.	10:08:56
13	MR. JONES: Whoever is scrolling on the	10:09:03
14	shared copy of Exhibit 1001, could you go to PDF	10:09:04
15	page 11?	10:09:14
16	Q Okay. Dr. Murphy, so in column 1 rows 23	10:09:18
17	through 26, '157 patent states: However, since	10:09:22
18	general semiconductor devices are formed on a	10:09:25
19	silicon wafer made of conductive material, there	10:09:27
20	are little chances of being electrified within the	10:09:32
21	semiconductor device so that it is a key issue to	10:09:35
22	prevent the damage when a static electricity flows	10:09:39

1 through the input terminals.

10:09:46

2 Do you see that?

10:09:48

3 A Yes.

10:09:49

4 Q Yes. So do you agree that the general
5 semiconductor devices, the '157 -- '157 patent is
6 referring to here are silicon IC chips?

10:09:49

10:09:56

10:09:59

7 A The sentence identifies general
8 semiconductor devices which I think under -- I'm
9 understanding that to mean a broad variety of
10 semiconductor devices is formed on a silicon
11 wafer.

10:10:16

10:10:19

10:10:23

10:10:26

10:10:31

12 Q And the state of the conventional art as
13 described here is that the key issue is prevent
14 ESD damage is to prevent static electricity
15 flowing that enters through an input terminal that
16 could, you know, damage the internal circuitry of
17 the semiconductor device; is that right?

10:10:37

10:10:42

10:10:45

10:10:49

10:10:55

10:10:59

18 A So that's the issue that the '157
19 background is -- is stating to be conventional.

10:11:05

10:11:12

20 There are references around the time of the patent
21 that discuss ESD protection elsewhere not limited
22 to the input terminals. And it doesn't say here

10:11:21

10:11:24

10:11:32

1 in the background of the '157 that there's never 10:11:43
2 going to be ESD away -- ESD vulnerability to an 10:11:49
3 integrated circuit on silicon away from the input 10:11:59
4 terminals. It's really a question of emphasis and 10:12:04
5 those skilled in the art would understand that 10:12:10
6 it's possible. 10:12:12

7 And so that you have ESD vulnerabilities 10:12:13
8 at locations away from the input terminals and so 10:12:19
9 you may want to have additional protections, 10:12:23
10 additional ESD protections, and that usually these 10:12:31
11 are questions of design trade-offs, whether the 10:12:36
12 expense in terms of usually real estate or the 10:12:43
13 amount of area that a device will take up is worth 10:12:48
14 the trade-off. 10:12:54

15 And so a designer might say in some 10:12:57
16 instances that the additional area that might be 10:13:00
17 used by additional ESD devices on a silicon 10:13:06
18 device, in fact, is worth it to protect against 10:13:10
19 ESD that is not originating at the input 10:13:19
20 terminals, yeah, for example. 10:13:26

21 Q So for a general semiconductor device 10:13:29
22 formed on silicon, do you agree that a key issue 10:13:34

1 to prevent damage from ESD is to prevent current 10:13:40
2 that can flow through from an input terminal on 10:13:47
3 the general semiconductor device? 10:13:52

4 A Again, it's up to the designer and the 10:13:55
5 specific application to identify the key, the most 10:14:13
6 important issues. It is a, you know, important 10:14:17
7 issue for ESD at input terminals. 10:14:23

8 Q In your opinion, for ESD events that could 10:15:34
9 occur in a semiconductor device formed on a 10:15:44
10 silicon wafer that originate far away from the 10:15:49
11 input terminals, how does that occur? What is 10:15:54
12 the -- the entry point or how does -- how is the 10:16:03
13 static charge created in that portion that is far 10:16:07
14 away from the input terminals, again, in a general 10:16:12
15 semiconductor device that is formed on a silicon 10:16:16
16 wafer? 10:16:19

17 MR. RODKEY: Objection, form. 10:16:20

18 A One way to get that phenomenon of ESD 10:16:21
19 events that are not necessarily close or to the -- 10:16:50
20 or at the input terminals is at the manufacturing 10:16:56
21 process. This is at page -- sorry, paragraph 45 10:16:59
22 of my declaration where I discuss the generation 10:17:02

1 of static charge on sensitive components during 10:17:07
2 the manufacturing process. 10:17:12

3 And so, for example, if you have not 10:17:14
4 completed the fabrication of your semiconductor 10:17:18
5 device on silicon, you're not necessarily going to 10:17:24
6 have input terminals, per se. However, your 10:17:29
7 semiconductor device in this instance on silicon 10:17:35
8 substrate could still be vulnerable anywhere that 10:17:41
9 is exposed to the outside atmosphere and there's a 10:17:51
10 risk of charge buildup not necessarily on the 10:18:04
11 silicon wafer itself but charge buildup on the 10:18:07
12 tools that may come into contact or come into 10:18:11
13 close proximity to your silicon wafer and your 10:18:16
14 semiconductor electronic device. 10:18:21

15 Q Do you agree that the -- that risk you 10:18:24
16 just identified for charges that could build up on 10:18:48
17 a silicon wafer is lower than for semiconductor 10:18:55
18 devices formed on an insulating substrate? 10:19:05

19 A Well, what I identified was charge 10:19:08
20 accumulating on the manufacturing tool and then 10:19:20
21 potentially leading to ESD events during 10:19:25
22 manufacturing. That is less tied to the substrate 10:19:29

1 material, whether silicon or glass. And so the
2 vulnerability stands in both instances if the
3 substrate is silicon or glass.

4 Q And is it true that, you know, the charges
5 that may build up on the equipment will eventually
6 need to flow onto the device being manufactured,
7 right? And that silicon substrate is -- will more
8 easily disperse that charge than an insulating
9 substrate such as glass?

10 A Not necessarily, no. The charge will tend
11 to follow the path of least resistance and tend
12 -- going to tend to be the metal connections that
13 connect circuits and subcircuits and components.
14 Those metal lines could be similar on silicon
15 substrates and glass substrates in a general way.

16 Q Let's turn to the Reiner reference.

17 MR. JONES: So let's mark as Exhibit 1005
18 the document with the file name '157 IPR EX 1005
19 Reiner. I will drop that in the chat now as well.

20 (Exhibit 1005 marked for identification.)

21 Q Dr. Murphy, let me know when you have that
22 in front of you.

1	A Yes. I've got Reiner pulled up.	10:22:52
2	Q Do you recognize Exhibit 1005, right?	10:22:54
3	A Yes.	10:22:59
4	Q So in your declaration in support of the	10:23:05
5	'157 IPR petition, you do not opine that Reiner	10:23:18
6	anticipates any claim of the '157 patent, correct?	10:23:23
7	A According to my declaration paragraph 85,	10:23:26
8	I identified on ground 1 that the following	10:24:01
9	combinations would have rendered the claims	10:24:05
10	obvious to a person of ordinary skill in the art	10:24:08
11	for claims 1 to 18 of the '157 patent. There are	10:24:12
12	a number of claim elements that are disclosed or	10:24:16
13	would have been obvious in view of Reiner and	10:24:24
14	disclosed by Reiner but my opinions are related to	10:24:32
15	obviousness of the claims.	10:24:37
16	MR. RODKEY: Counsel, I'm sorry to	10:24:40
17	interrupt but the document -- I want to be	10:24:43
18	conscientious of privilege issues here. The	10:24:46
19	document you put in the chat has highlighting that	10:24:48
20	doesn't appear in the originally filed exhibit.	10:24:51
21	Do you want to replace that with a non-highlighted	10:24:55
22	version.	10:24:58

1	MR. JONES: I'm sorry, it does. Thank you	10:24:58
2	for pointing that out, Kevin.	10:25:42
3	All right. I'm dropping a new copy	10:25:44
4	Exhibit 1005 into the chat. Could we remark this	10:25:49
5	as Exhibit 1005? None of that highlighting gave	10:25:54
6	away the game but I appreciate it.	10:26:05
7	MR. RODKEY: Just want to be cautious of	10:26:08
8	privilege.	10:26:14
9	MR. JONES: Yeah. Can we go off the	10:26:14
10	record briefly? I apologize.	10:27:04
11	THE VIDEOGRAPHER: We are going off the	10:27:06
12	record. The time is 10:27 a.m.	10:27:07
13	(Whereupon a break was had.)	10:27:10
14	THE VIDEOGRAPHER: We are going back on	10:29:25
15	the record. The time is 10:29 a.m.	10:29:27
16	BY MR. JONES:	10:29:36
17	Q Dr. Murphy, back to Reiner Exhibit 1005.	10:29:37
18	Is it correct that you also do not opine that	10:29:47
19	Reiner discloses all limitations of any of the	10:29:50
20	claims of the '157 patent?	10:29:54
21	A That's correct.	10:30:01
22	Q And we talked earlier about driving	10:30:24

1 circuits that are formed on the pixel substrate of 10:30:29
2 an LCD panel. The driver circuits that Reiner 10:30:40
3 describes are not formed on the pixel substrate. 10:30:54

4 Do you agree with that? 10:31:03

5 A Any particular driver circuits in Reiner 10:31:06
6 that you'd like me to look at? 10:31:16

7 Q Well, Reiner refers to source driver 10:31:19
8 module 31 and gate driver 63, right. And feel 10:31:25
9 free to page through Exhibit 1005. But I'm just 10:31:28
10 trying to ask a general question. 10:31:32

11 A Right. I'd appreciate if you just repeat 10:31:40
12 the question. 10:31:43

13 Q Yeah. Let's -- why don't we go to PDF 10:31:51
14 page 18 and look at Figure 4 of Reiner. 10:31:54

15 MR. JONES: Could we give the witness 10:32:10
16 control just -- 10:32:12

17 Q Dr. Murphy, do you mind just scrolling 10:32:12
18 through the version we have up on the Zoom screen? 10:32:16

19 REMOTE TECHNICIAN: I'll bring us to 10:32:22
20 Figure 4. Here we go. 10:32:28

21 Q Okay. So the source driver module 61 in 10:32:30
22 Figure 3, do you see that? 10:32:40

1	A Yes.	10:32:42
2	Q And then the -- the box labeled gate	10:32:44
3	drivers 63, do you see that?	10:32:51
4	A Yes.	10:32:53
5	Q Reiner's description of those devices is	10:32:53
6	that they are silicon IC chips.	10:33:21
7	Do you agree with that?	10:33:25
8	A I'm not sure if 61 and 63 are chips	10:33:33
9	themselves but with reference to other figures,	10:33:38
10	Reiner discloses driver circuits on silicon	10:33:49
11	substrates with, for example, Figure 2.	10:34:00
12	Q Do you agree that whatever may comprise	10:34:03
13	source driver module 61 and gate driver 63 are not	10:34:27
14	described in Reiner as being formed on the pixel	10:34:35
15	substrate?	10:34:58
16	A No. Those are ultimately on the pixel	10:34:58
17	substrate. Reiner describes how they're put on	10:35:08
18	the pixel substrate by forming a connection by	10:35:11
19	what's called flip chip technology, and this is in	10:35:21
20	specific reference to page 7 of Reiner in the area	10:35:25
21	of lines 23 through 26 for instance.	10:35:33
22	Q Could you navigate to that portion of	10:35:41

1 Reiner in the exhibit that's shared on the Zoom
2 screen, please?

3 So is it your opinion that those display
4 drivers 61 and 63 as disclosed by Reiner, that the
5 circuitry is formed on a -- on a pixel -- on the
6 same substrate that pixels would be formed on?

7 A Not really my opinion, per se. It's what
8 is disclosed here by Reiner in this passage. I'll
9 read for you starting at 23. And I apologize,
10 earlier I said it was page 7 -- sorry. Earlier, I
11 said it was page 6, but if we look at the label,
12 you'll see that it's page 7 at the bottom of the
13 page.

14 Starting at line 23 of page 7 of Reiner:
15 When packaging the integrated circuit device, it's
16 flipped onto the substrate 16 according to
17 well-known flip chip technology.

18 So the -- in this case, the source drivers
19 are on the -- what we've been calling the pixel
20 substrate.

21 Q Is it your opinion that the circuit
22 (technical disruption) on that substrate. I mean,

1	the flip chip point here is referring to	10:37:45
2	packaging?	10:37:48
3	MR. RODKEY: Objection, form.	10:37:58
4	A I'm sorry, what's the question?	10:38:06
5	Q So the sentence, I think, on lines 23	10:38:21
6	through 25 of page 7 of Reiner: When packaging	10:38:27
7	the integrated circuit device 20, it is flipped	10:38:34
8	onto the substrate 16 according to the well-known	10:38:38
9	flip chip technology.	10:38:42
10	Do you see that?	10:38:44
11	A Yes.	10:38:45
12	Q Is that the -- the substrate 16 that	10:38:46
13	you're referring to in your last answer?	10:38:52
14	A Substrate 16 refers to potentially the	10:38:56
15	pixel substrate.	10:39:03
16	Q So my question is: Is it your opinion	10:39:07
17	that Reiner discloses that the integrated circuit	10:39:12
18	device 20 is formed on the substrate 16?	10:39:15
19	A Your question uses the terminology	10:39:47
20	"formed." I'm not sure if that's what Reiner	10:39:49
21	uses. I'm pointing out that the scan line driver	10:39:53
22	circuit in Reiner is on substrate 16, the pixel	10:39:59

1 substrate, as disclosed at least at line 23 to 26 10:40:07
2 here. You can see it says: It is flipped onto 10:40:11
3 the substrate 16, with reference to the scan line 10:40:15
4 driver circuit. 10:40:19

5 Q The scan line driver circuit as your refer 10:40:22
6 to it in Reiner of which I think -- are you 10:41:05
7 referring to gate driver 63? 10:41:09

8 A Gate driver 63 is one representation in 10:41:25
9 Reiner of what we've been calling scan line driver 10:41:33
10 circuitry. 10:41:38

11 Q Okay. I just want to be clear here. 10:41:39
12 Reiner discloses that that device, gate driver 63 10:41:52
13 scan line driving circuit, is formed on a silicon 10:42:00
14 substrate rather than being integrated with 10:42:08
15 the -- rather than being formed on the display 10:42:23
16 substrate in a way that, you know, the pixels are 10:42:27
17 formed, etcetera. 10:42:34

18 MR. RODKEY: Objection, form; asked and 10:42:42
19 answered. 10:42:46

20 A I'll just, you know, try to repeat again. 10:42:46
21 The scan line drivers, right, which is depicted in 10:42:50
22 Figure 4 at 63 in Reiner gets flipped onto the 10:42:59

1 substrate as it's disclosed in, you know, line 24 10:43:07
2 there of page 7. It comes into -- it's on, right, 10:43:12
3 specifically the scan line drivers are on that 10:43:17
4 pixel substrate; and therefore, are subject to the 10:43:21
5 same types of ESD vulnerabilities as other 10:43:25
6 circuits on the pixel substrate. 10:43:35

7 And we mentioned that in some instances, 10:43:38
8 glass substrates may have additional 10:43:45
9 vulnerabilities, different vulnerabilities 10:43:49
10 compared to integrated circuits on silicon 10:43:54
11 substrates. Once the scan line drivers are on the 10:44:00
12 pixel substrate in the way that's disclosed in 10:44:04
13 Reiner by flip chip, they also become potentially 10:44:07
14 subject to the vulnerabilities because they're 10:44:14
15 electrically connected to that glass substrate. 10:44:22

16 Q Would you scroll up to the end of page 2, 10:44:29
17 beginning of page 3 in Reiner? 10:45:00

18 A Yeah. I think we're there now. 10:45:15

19 Q Okay. Do you see the last two lines -- 10:45:17
20 starting at the last two lines of page 2, it 10:45:19
21 stays: Quite often integrated circuit devices 10:45:23
22 such as CMOS devices, for example, comprise 10:45:27

1 electrostatic discharge device, ESD, protection in
2 order to prevent the very sensitive circuits on a
3 chip from being destroyed when it is subject to a
4 discharge event. This might happen, for example,
5 when somebody induces a voltage peak in the
6 circuitry by touching the pins of the chip.

10:45:32

10:45:35

10:45:38

10:45:41

10:45:43

10:45:46

7 I get that right?

10:45:49

8 A Yes. I think you did.

10:45:50

9 Q Do you agree that the driving -- that the
10 display driver circuits --sorry, display driver
11 devices that Reiner discusses and discloses are
12 chips are pins?

10:45:52

10:46:05

10:46:09

10:46:12

13 A I'm not sure if Reiner specifically
14 identifies the scan driver circuits as having
15 pins. And what we have are, you know, connection
16 points where the scan line driver circuitry is
17 flip chipped and bonded to the glass substrate.

10:46:14

10:47:05

10:47:11

10:47:21

10:47:24

18 Q So you agree that the scan line driver
19 circuitry as you refer to it disclosed by Reiner
20 is contained in a silicon IC chip or multiple
21 chips?

10:48:05

10:48:08

10:48:15

10:48:22

22 MR. RODKEY: Objection, mischaracterizes.

10:48:24

1	A I don't know if I agree with the	10:48:25
2	description of "contained in a silicon chip."	10:49:12
3	Clearly, there's a substrate on which transistors	10:49:17
4	are formed. Silicon substrate as depicted in	10:49:29
5	Figure 2, for example, of Reiner, item 21, Figure	10:49:37
6	2 shows the connection point to the glass	10:49:47
7	substrate as well items 29 and 16 on Figure 2 on	10:49:52
8	Reiner.	10:49:59
9	Q So you agree that Reiner discloses the	10:50:19
10	transistors that are -- that comprise the driving	10:50:26
11	circuits Reiner discusses are formed on a silicon	10:50:37
12	substrate?	10:50:43
13	A You're using the word "formed" and that's	10:50:44
14	not a word that I might use. Figure 2 depicts	10:50:53
15	transistors as part of a silicon substrate. That	10:51:04
16	much is clear in Reiner.	10:51:08
17	Q Is it your opinion that the driving	10:51:50
18	circuits Reiner discusses are formed -- well,	10:51:59
19	strike that.	10:52:20
20	Earlier we were talking about the	10:52:23
21	difference between integrated chip that's part of	10:52:27
22	silicon as compared to circuitry that is formed	10:52:30

1	directly on the substrate on which, you know, the	10:52:34
2	pixel array is formed in an LCD display, right.	10:52:39
3	There's a distinction there.	10:52:44
4	Do you agree with that?	10:52:47
5	A There is a distinction between	10:52:48
6	manufacturing transistors for -- you know, for	10:52:55
7	example, directly on a glass substrate versus	10:53:01
8	in -- in a silicon wafer. There are going to be	10:53:12
9	some different manufacturing techniques that are	10:53:16
10	going to be used, somewhat different material	10:53:19
11	properties. But there are a lot of commonalities	10:53:24
12	specifically when it comes to ESD protection and	10:53:28
13	the general types of circuits.	10:53:32
14	These are transistors complementary MOS or	10:53:35
15	CMOS circuits and both are vulnerable to ESD	10:53:41
16	protection. So we could talk about similarities	10:53:51
17	or differences as well.	10:53:54
18	Q Is it your opinion that the display driver	10:53:55
19	circuits 61 and 63 that Reiner discloses, the	10:54:06
20	transistors within those driving circuits are	10:54:15
21	manufactured directly on the glass -- on a glass	10:54:20
22	substrate?	10:54:24

1	A Transistors as one part of the scanning	10:54:42
2	line driver circuitry as depicted in Figure 2 of	10:54:49
3	Reiner are in the silicon wafer if we're talking	10:54:52
4	just about the transistors.	10:55:00
5	MR. JONES: Would now be a good time for	10:55:30
6	lunch break?	10:55:33
7	THE WITNESS: That works for me.	10:55:33
8	MR. JONES: Let's go off the record.	10:55:35
9	THE VIDEOGRAPHER: We are going off the	10:55:36
10	record. The time is 10:55 a.m.	10:55:37
11	(Whereupon a break was had.)	11:32:46
12	THE VIDEOGRAPHER: We are going back on	11:32:46
13	the record. The time is 11:32 a.m.	11:32:52
14	BY MR. JONES:	11:32:55
15	Q Welcome back, Dr. Murphy. I'd like to	11:32:56
16	circle back to where we left off before lunch.	11:32:58
17	Your last answer, do you recall relating	11:33:03
18	to Figure 2 of Reiner where you said that the	11:33:08
19	transistors that are one part of the scanning line	11:33:16
20	driver circuitry as depicted in Figure 2 of Reiner	11:33:21
21	are in the silicon wafer if we're talking just	11:33:25
22	about the transistors?	11:33:28

1	Do you recall that?	11:33:31
2	A Yes. I believe I said something to that	11:33:32
3	effect.	11:33:35
4	MR. JONES: Could you -- could we put up	11:33:43
5	Exhibit 1005 on the Zoom screen?	11:33:46
6	Q Dr. Murphy, I'd like to just walk through	11:33:52
7	Figure 2 Reiner and the corresponding descriptions	11:33:57
8	of the numbered items here. So if you need to	11:34:02
9	refer back to the written description, please do	11:34:04
10	so. Okay?	11:34:10
11	A All right. Yeah. I'll do my best to	11:34:12
12	answer the questions.	11:34:14
13	Q All right. So Figure 2 shows a schematic	11:34:15
14	cross-section of an integrated circuit device	11:34:25
15	which is identified by the bracket labeled 20 in	11:34:32
16	Figure 2, right?	11:34:40
17	A Yes. In a general way, we are looking at	11:34:41
18	a cross-section of the integrated circuit device	11:35:02
19	20 that's shown in Figure 2.	11:35:05
20	Q Okay. Then as you noted before lunch, at	11:35:08
21	least one integrated device 22, for example a	11:35:14
22	transistor, is formed on the silicon substrate of	11:35:19

1 the integrated circuit device 20; is that right? 11:35:26

2 A With reference to the written description, 11:35:34

3 I don't know if a discussion -- if there's a 11:35:43

4 discussion in Reiner about how precisely circuit 11:35:47

5 device 22 is formed. In general, it's comprised 11:35:52

6 of portions of silicon and other materials and 11:35:59

7 it's located as it's shown there in contact with 11:36:03

8 the silicon conductor substrate 21. 11:36:06

9 Q Okay. And then there's an isolating layer 11:36:14

10 24 that at least partially covers the integrated 11:36:24

11 devices or devices 22; is that right? 11:36:34

12 A Yes. I can see that in the figure. 11:36:36

13 Q And then there are metal lines and 11:36:38

14 metallization layer 25. Those are labeled 26.1 11:36:49

15 through 26.4, that provide electrical connections 11:36:53

16 between the devices 22 that are integrated in the 11:36:57

17 integrated circuit device 20; is that right? 11:37:02

18 A Yeah. I think in a general way, that's 11:37:19

19 how the -- it's being described here in the 11:37:21

20 written description around page 15, bottom of 11:37:25

21 page 15 into the beginning of page 16. There's 11:37:31

22 some detail, but I think what you've said captures 11:37:35

1 the gist.

11:37:37

2 Q Okay. And then there's a passivation
3 layer labeled 27 in Figure 2, which is on top of
4 the metal lines; is that right?

11:37:40

11:37:47

11:37:50

5 A Yes. I see passivation layer 27 here
6 depicted, yes, in Figure 2.

11:37:54

11:38:01

7 Q And then we have the bump ridge 29; is
8 that right?

11:38:04

11:38:15

9 A Yes.

11:38:15

10 Q So all of those -- how would you refer to,
11 you know, the different labels that are given to
12 these different parts: For example, the bump
13 ridge, passivation layer, the metal lines? Are
14 they components? What word is used to describe
15 the different parts that are described in Figure 2
16 of integrated circuit device 20?

11:38:18

11:38:26

11:38:30

11:38:33

11:38:41

11:38:44

11:38:46

17 MR. RODKEY: Objection, form.

11:39:00

18 A Reiner itself describes them differently
19 compared -- depending on what they are, right.
20 Some are described as layers, like metal layer 25.
21 Others are the devices, 22. It's fair to say they
22 all are parts of the -- what's shown as item 20,

11:39:01

11:39:15

11:39:19

11:39:23

11:39:29

1 the integrated circuit device 20. 11:39:45

2 Q Right. As -- as -- as indicated in the 11:39:48
3 written description and then in Figure 2, the 20 11:39:53
4 label has the bracket that covers -- I'll refer to 11:39:56
5 them as components, but the different parts. And 11:40:06
6 the only portion that's outside of that bracket is 11:40:10
7 at the top labeled 16 which is a substrate; is 11:40:15
8 that right? 11:40:31

9 A Excuse me. I could see that the bracket 11:40:31
10 20 for the integrated circuit device, you know, 11:40:37
11 encompasses the parts we're talking about. You 11:40:46
12 can see where it makes contact with substrate 16. 11:40:48
13 There's also parts, I'll say, that are not 11:40:51
14 depicted in Figure 2, and that would be part of 11:40:55
15 the substrate 16 that makes a connection to the 11:41:04
16 bump ridge. 11:41:08

17 It's not depicted, so I can't identify 11:41:11
18 whether it falls within the bracket 20 or not. 11:41:15
19 But that's something that's discussed in the 11:41:18
20 written description. I could find that passage 11:41:22
21 but just -- 11:41:25

22 Q Right. I know what you're talking about. 11:41:25

1 I think Reiner describes, you know, substrate and
2 interconnections to connect to the bump ridge 29,
3 something to that effect?

4 A Something to that effect on page 7 of
5 Reiner around lines 22 through 26, yeah,
6 interconnection on the substrate 16. No such
7 interconnections are shown in Figure 2.

8 Q And it's your opinion that the source
9 driver 61 and gate driver 63 that Reiner discloses
10 would -- would be oriented the same way as Figure
11 2 in the sense that there's an integrated device
12 20 that is then flipped onto a substrate 16 which
13 you identify as the -- the LCD screen 60.

14 Am I getting that right?

15 A That may be explicitly disclosed in
16 Reiner. A person of ordinary skill reading Reiner
17 would understand that to be the case, yeah.

18 Q So looking at Figure 2 in terms of the
19 gate drivers 63, the metal lines 26.1 through 26.4
20 shown in Figure 2, what would those be in a gate
21 driver?

22 A I'm sorry, I don't exactly understand the

1 question. If you could rephrase. 11:43:50

2 Q Sure. The gate driver 63, those 11:43:53

3 integrated circuit devices would include metal 11:44:40

4 lines like the lines identified as 26.1 and 11:44:46

5 26. -- through 26.4 in Figure 2. There would be 11:44:59

6 metal lines in gate driver device? 11:45:02

7 A Again, I'm not sure if I recall if Reiner 11:45:12

8 explicitly discloses that. I know that the gate 11:45:17

9 drivers 63 that we're talking about in Figure 4 of 11:45:21

10 Reiner are depicted really schematically. When it 11:45:24

11 comes to the precise limitation, ESD protection 11:45:32

12 circuitry, I'm not sure if that is, you know, 11:45:37

13 precisely the way that the metal lines are formed 11:45:41

14 is relevant. 11:45:47

15 But you know, a person of ordinary skill 11:45:47

16 looking at the Reiner, looking at the gate 11:45:52

17 drivers, would understand that metal lines like 11:45:56

18 those depicted in Figure 2 are typically going to 11:45:58

19 be part of the -- that circuitry that's 11:46:04

20 depicted -- the circuitry that comprises the gate 11:46:10

21 drivers. Those metal -- type of metal lines 11:46:13

22 are -- are a common way that transistors are 11:46:16

1 interconnected to each other like what's shown in
2 Figure 2.

3 Q Right. So what -- what function would
4 those metal lines serve in a gate driver?

5 A If we're referring to 26.1, 2, and 4
6 there --

7 Q Yeah. And I don't mean to interrupt, but
8 in the context of a gate driver, not necessarily
9 specifically what's shown in Figure 2 but based on
10 your last answer where, you know, the gate driver
11 would have these metal lines to interconnect the
12 integrated devices 22, transistors, my question is
13 what -- what would you call those different metal
14 lines? Are they signal lines, for example?

15 A They could have a number of functions. I
16 would call them electrical interconnections.

17 Q Could they be signal lines?

18 A I think someone could call them signal
19 lines depending on what their definition of signal
20 lines would be. That's -- that's something --
21 something that they could potentially be.

22 Q Could they be power lines?

11:46:21

11:46:24

11:46:27

11:46:36

11:46:50

11:46:56

11:46:56

11:46:59

11:47:04

11:47:07

11:47:10

11:47:16

11:47:19

11:47:24

11:47:28

11:47:47

11:48:03

11:48:07

11:48:46

11:48:49

11:48:53

11:48:55

1 A And if someone was trying to identify
2 them, metal lines on a scan line driver circuit,
3 one of the things they could be is, you know,
4 signal lines or other things as well.

5 Q Would power lines be one of the other
6 things they could be?

7 A Again, without specific reference to
8 Figure 2 and the exact functionality of that
9 circuit, there are a lot of functions and
10 descriptions and power lines would reasonably be
11 among them. You know, depending on the nature of
12 exactly the connections and the circuitry that are
13 there, I can't exclude power lines based on, you
14 know, what we know from just looking at the
15 figures in the context of Reiner.

16 Q Right. Okay. And those metal lines are
17 part of integrated circuit device 20, correct?

18 A Yes. That's how they're depicted in
19 Reiner.

20 Q Let's turn back to Figure 4, please, which
21 I believe is the next page, page 18.

22 A Figure 4?

1	Q Yes. So I'd just like to walk through	11:51:11
2	this in a little bit more detail. And as I'm	11:51:15
3	asking these questions, again, feel free to refer	11:51:18
4	back to the written description which is the	11:51:21
5	paragraph at the bottom of page 9 of Reiner.	11:51:30
6	So in Figure 4, the box labeled 60 is the	11:51:38
7	LCD screen, right?	11:51:46
8	A Yes. That's called out in the written	11:51:54
9	description as 60 LCD screen.	11:51:57
10	Q And the source line 67 and the gate line	11:52:03
11	68 are on the LCD screen 60?	11:52:09
12	A Yes. That's in the written description,	11:52:25
13	page 9, around 20 -- line 26, it shows plurality	11:52:28
14	of source lines 67 and a plurality of gate lines	11:52:36
15	associated with LCD screen 60.	11:52:47
16	Q I don't believe this is in the written	11:52:50
17	description, but the circuitry that controls the	11:52:56
18	pixels, for example transistors, would also be on	11:53:04
19	LCD screen 60 in Figure 4; is that right?	11:53:12
20	A So hypothetically, if it were an active	11:53:18
21	matrix type of display, typically, you will have	11:53:22
22	what I call pixel driver -- excuse me, yeah, pixel	11:53:30

1	driver circuitry in the area of the LCD screen.	11:53:35
2	Yeah.	11:53:42
3	Q Okay. And then we have the source driver	11:53:47
4	module 61 and the box labeled gate driver 63. The	11:53:52
5	source driver module 61 drives the source line 67	11:54:01
6	and then the gate drivers in box 63 drive the gate	11:54:06
7	lines 68, right?	11:54:13
8	A Yeah. In a general way, that's how these	11:54:21
9	types of circuits function.	11:54:26
10	Q I guess just to round out the boxes here,	11:55:00
11	we have a box labeled CPU, number 62, which	11:55:04
12	provides video signals and row-timing signals to	11:55:10
13	the source driver module and the gate drivers	11:55:15
14	respectively via lines 66 and 69 respectively,	11:55:17
15	right?	11:55:34
16	A Yeah. That's generally accurate and it's	11:55:34
17	addressed explicitly in the written description on	11:55:39
18	page 9 around lines 30 through 32.	11:55:42
19	Q Okay. Could you describe to me how the	11:55:47
20	manufacturing process would work for the LCD	11:55:55
21	screen 60 and then the source driver module 61 and	11:56:04
22	then the gate driver modules 63?	11:56:09

1	MR. RODKEY: Objection, scope.	11:56:16
2	A I think the reference here, Reiner does a	11:56:17
3	fair description of the manufacturing process for	11:57:17
4	these devices. I don't think I'll need to	11:57:25
5	summarize it other than to, you know, emphasize	11:57:33
6	that the manner in which the 61 and 63 or other	11:57:37
7	types of integrated circuits are manufactured is,	11:57:48
8	in the process of making the LCD device would be	11:57:57
9	put on the glass substrate by flip chip technology	11:58:04
10	using the bump ridges that are, you know,	11:58:11
11	described in detail in the -- in Reiner itself. I	11:58:16
12	think that's a fair overview of -- of some of	11:58:20
13	those processes.	11:58:23
14	Q So the circuitry that is on the LCD screen	11:58:27
15	60, the lines such as the gate and the source	11:58:44
16	lines, that would be manufactured -- I'm not sure	11:58:49
17	if "first" is the right word, but then once the	11:58:58
18	source driver module or the gate drivers would be	11:59:01
19	mounted using the flip chip technology as you put	11:59:05
20	it after the LCD screen 60 is manufactured; is	11:59:09
21	that accurate?	11:59:19
22	A In a general way, the -- typically, how	11:59:19

1 it's done in the industry -- and I don't know if 11:59:36
2 Reiner takes pains to describe the order, but in 11:59:39
3 my experience, I've seen the circuitry on the 11:59:49
4 glass substrate deposited there and the lines are 11:59:57
5 shown in 67 and 68 and the pixel driver circuitry 12:00:12
6 in a different step from the source driver and 12:00:20
7 gate driver modules being connected to and put on 12:00:23
8 the substrate as part of the manufacturing 12:00:29
9 process. 12:00:40

10 Q Okay. For an LCD screen that uses a gate 12:00:46
11 driver that is on the pixel array substrate 12:00:58
12 integrated with the pixel array substrate, there 12:01:08
13 would not be those separate steps, right? The 12:01:11
14 gate driver circuitry would be manufactured in the 12:01:15
15 same steps as the scan lines, the gate lines, the 12:01:22
16 pixel control transistors are manufactured, 12:01:31
17 correct? 12:01:38

18 A Well, you're using some terminology 12:01:38
19 integrated with that, I don't know that we've 12:01:41
20 discussed or if it's in Reiner. Once the source 12:01:44
21 and gate driver modules are bump bonded together, 12:01:56
22 with the substrate, they could said to be 12:02:01

1 integrated, but the manufacturing process as I 12:02:05
2 indicated in my previous answer is going to be 12:02:14
3 different in some ways, if you have your source 12:02:17
4 and driver modules transistors directly on silicon 12:02:25
5 substrates instead. 12:02:33

6 I don't know that any of that is going to 12:02:34
7 affect what a person of ordinary skill is going to 12:02:38
8 learn about ESD protection from Reiner. The 12:02:41
9 manufacturing process still has its 12:02:50
10 vulnerabilities to ESD that we discussed. 12:02:57

11 Reiner's teachings of ESD protection circuitry are 12:03:00
12 not limited to the specific source driver gate 12:03:03
13 driver modules that are depicted in Figure 4. 12:03:09
14 It's more general. Figure 4 and this source 12:03:12
15 driver and gate driver modules are given as more 12:03:19
16 or less examples of the type of circuitry that 12:03:24
17 would be applicable to -- to ESD protection that's 12:03:26
18 discussed in Reiner. 12:03:33

19 Q Understood. And the last part of your 12:03:36
20 answer you said: If you have your source and 12:03:39
21 driver modules transistors directly on silicon 12:03:42
22 substrates instead, did you mean -- did you mean 12:03:48

1	silicon substrates in that part of your answer?	12:03:52
2	A I'm sorry, could you just repeat that for	12:03:56
3	me so I can listen very carefully.	12:03:59
4	Q Could we -- could we just read back Dr.	12:04:01
5	Murphy's -- the last paragraph of Dr. Murphy's	12:04:05
6	prior answer?	12:04:07
7	A Thank you.	
8	THE REPORTER: One moment.	
9	Q Starting with "if you have your."	
10	THE REPORTER: If you have your source --	
11	MR. JONES: I'll read it off.	
12	THE REPORTER: You're going to read it?	
13	Q If you have your source and driver modules	12:04:08
14	transistors directly on silicon substrates	12:04:30
15	instead, I don't know that any of that is going to	12:04:34
16	affect what a person of ordinary skill is going to	12:04:36
17	learn about ESD protection from Reiner. The	12:04:38
18	manufacturing process still has -- has its as a	12:04:40
19	rule --	12:04:44
20	MR. JONES: Okay. The transcription I'm	12:04:44
21	reading is not perfect. Could the court reporter	12:04:44
22	read that portion of the answer back?	12:04:44

1	THE REPORTER:	12:05:53
2	(Whereupon the requested question was read.)	12:05:53
3	Q Dr. Murphy, let me ask it this way -- and	12:05:53
4	I don't mean to interrupt. If you wanted to say	12:05:55
5	something, please do. Go ahead.	12:06:02
6	A I was just going to ask for a question.	12:06:02
7	Q Yeah. In previous question, you described	12:06:04
8	how, you know, the LCD screen 60 would be	12:06:08
9	manufactured and then the gate drivers and source	12:06:13
10	driver modules would be flip chip bonded to the	12:06:17
11	LCD display substrate, right?	12:06:21
12	MR. RODKEY: Objection, mischaracterizes.	12:06:28
13	A I think I said that the circuitry on the	12:06:34
14	pixel substrate would be manufactured in a	12:06:48
15	separate step than any circuitry that's on a	12:06:54
16	different substrate, and then the bump bonding	12:06:59
17	would occur of the different substrates to each	12:07:08
18	other. I think that's as far as I went.	12:07:10
19	Q Okay. For an LCD display where the gate	12:07:14
20	driving circuitry is formed on the LCD	12:07:23
21	screen -- LCD screen 60 substrate, there would be	12:07:31
22	no second step of bonding the gate drivers to the	12:07:42

1 substrate of LCD screen 60; is that right?

12:07:48

2 A Again, we're talk -- you're using some
3 terminology, "formed on," and I've been consistent
4 in saying that in Reiner, the gate drivers and
5 source drivers are on the pixel substrate by way
6 of these bump ridges and flip chip bonding. I'm
7 not sure if there's an alternative that we've
8 discussed that I understand clearly your question.

12:07:53

12:07:56

12:08:00

12:08:04

12:08:15

12:08:23

12:08:25

9 Q The flip chip bonding you mentioned, where
10 on LCD screen 60 in your opinion would -- would
11 those integrated circuit devices be located and
12 bonded to the LCD -- to the LCD screen 60 in terms
13 of Figure 4?

12:08:33

12:09:35

12:09:42

12:09:48

12:09:57

14 A I don't know that Figure 4 depicts the
15 complete physical arrangement or placement of all
16 of the parts of the display. 60 is called out as
17 an LCD screen.

12:09:58

12:10:06

12:10:10

12:10:13

18 In general, similar to what would be found
19 on other types of manufacturing processed LCD
20 screens, I would expect that the gate drivers and
21 source drivers are going to be, in general, found
22 along the periphery of the display substrate after

12:10:20

12:10:26

12:10:32

12:10:38

12:10:42

1 they're flip chip bonded. 12:10:52

2 Q Could the gate drivers and source drivers 12:11:11
3 be attached to a PCB, printed circuit board, that 12:11:34
4 is connected to the LCD screen 60 of a 12:11:43
5 flexible -- FPC, I'm not sure exactly what the 12:11:52
6 definition of the acronym is. 12:11:56

7 MR. RODKEY: Objection, form; scope; also 12:12:01
8 incomplete hypothetical. 12:12:09

9 A If we're talking about flexible connectors 12:12:16
10 used with liquid crystal displays, I'm generally 12:12:25
11 aware that additional circuitry can be connected 12:12:31
12 to the pixel substrate with flexible connectors. 12:12:37
13 I haven't considered whether that is what's going 12:12:46
14 on here with Reiner. I don't think Reiner really 12:12:50
15 gives a strong teaching either way on that 12:12:57
16 particular point, other than what's been depicted 12:13:00
17 as we've been, you know, talking about in Figure 2 12:13:12
18 where the substrate 16 is where the flip chip 12:13:16
19 makes contact making the connection to the 12:13:26
20 integrated circuit devices that are shown in 12:13:33
21 number 20 of Figure 2. 12:13:36

22 Q Let's turn to Figure 5 of Reiner, the last 12:13:43

1 page. Dr. Murphy, I'm just going to ask some 12:14:12
2 general questions on this. So again, please feel 12:14:22
3 free to refer back to the written description. I 12:14:27
4 just want to set up what we're looking at here. 12:14:29

5 So Reiner Figure 5 shows part of the 12:14:31
6 source driver module 61 integrated circuit chip 12:14:39
7 that Reiner describes in the written description. 12:14:43

8 Do you agree with that? 12:14:50

9 A The description for Figure 5 does say 12:14:53
10 page 9 line 20, schematic block diagram of a 12:14:59
11 display driver in accordance with the present 12:15:05
12 invention as shown in Figure 5. It looks like 12:15:10
13 Reiner is giving it as an example of what can be 12:15:13
14 accomplished with Reiner's teachings and a person 12:15:17
15 of ordinary skill would be looking at the rest of 12:15:22
16 the written description of Reiner to understand 12:15:25
17 that this would be a typical example of a typical 12:15:27
18 integrated circuit that may be applicable and 12:15:33
19 would be applicable to scan line drivers or data 12:15:37
20 line drivers. 12:15:50

21 Q So you mention that line 20 on page 9, go 12:15:59
22 to the next page of Reiner, page 10, lines 1 12:16:03

1 through 23. That's a fairly detailed description 12:16:08
2 of Figure 5, right? 12:16:17

3 A Yes. That has some additional details and 12:16:24
4 specific labels and is in reference to primarily 12:16:42
5 to Figure 5. 12:16:47

6 Q Okay. Let's turn back to Figure 5 itself. 12:16:48
7 Okay. To get us oriented, Figure 5 shows output 12:17:08
8 devices 70 that are -- well, shows two output 12:17:17
9 devices 70; is that right? 12:17:25

10 A Two output devices 70 are what's shown and 12:17:26
11 there are additional implied by the dashed lines 12:17:38
12 at the bottom of Figure 5 and then the written 12:17:43
13 description. 12:17:45

14 Q Right. And per the written description, 12:17:46
15 you know, Reiner describes the output devices 70 12:17:51
16 as the circuitry that drive the source line. So 12:17:55
17 there would be an output device 70 for each source 12:18:07
18 line, right? 12:18:11

19 A Yeah. In general, that's how it's 12:18:12
20 depicted here. 12:18:33

21 Q All right. Then there are two power 12:18:40
22 supply lines VSS and VDD which are labeled 71 and 12:18:44

1	73 respectively?	12:18:50
2	A Yes. I see those.	12:18:51
3	Q And each output device 70 is connected to	12:18:52
4	VSS via connection 76 and VDD via connection 74;	12:18:57
5	is that right?	12:19:07
6	A Yes. That's what's shown in Figure 5.	12:19:08
7	Q And then each output device 70 has an	12:19:12
8	output line 75, correct?	12:19:21
9	A Yes.	12:19:27
10	Q Which is connected to contact pad 72; is	12:19:28
11	that right?	12:19:37
12	A Yes.	12:19:37
13	Q And then the contact pads 72 are connected	12:19:42
14	I, think Reiner uses an example by means of	12:19:51
15	bonding, to source line 67 which are shown as the	12:19:56
16	dotted lines moving left to right in Figure 5?	12:20:00
17	A Yes. I can see that.	12:20:06
18	Q So the source line 67, the dotted lines,	12:20:09
19	those are not part of the source driver module 61	12:20:15
20	shown in Figure 5; is that right?	12:20:24
21	A It depends on where you might want to draw	12:20:25
22	your line as to the boundary of the source driver	12:20:40

1 module 61. They're shown here. Figure 5 is a 12:20:47
2 depiction of 61 source driver module. I haven't 12:20:51
3 made any firm conclusions as to exactly if they 12:20:58
4 should be considered part of it. Certainly 12:21:04
5 they're connected to the source driver module and 12:21:06
6 provide a logical connection to the source line 12:21:14
7 67. 12:21:19

8 Q All right. To your point on the -- where 12:21:19
9 you might want to draw the boundary of the source 12:21:59
10 driver 61 point, Dr. Murphy, I'm going to do that 12:22:03
11 by annotating the image that is shown on the Zoom 12:22:07
12 screen. 12:22:14

13 And my question is: What is inside of the 12:22:16
14 red box, the whole -- everything inside there is 12:22:23
15 source driver module 61 with the caveat that 12:22:28
16 obviously it would repeat, right? It's not 12:22:35
17 showing the entire module, right? There would be 12:22:39
18 an output device 70 for each source line. 12:22:41

19 A Yeah. With the caveat that potentially 12:23:01
20 not every individual device or other connection 12:23:04
21 that may be required for the device to perform may 12:23:08
22 not be depicted in Figure 5. And Figure 5 is, you 12:23:13

1 know, general arrangement, relative arrangement,
2 of these components, the Figure just by the label
3 61 shows that Figure 5 is a depiction of the
4 source driver module from Reiner.

5 Q But you agree that everything in the very
6 poor red box I drew is part of source driver
7 module 61?

8 MR. RODKEY: Objection, mischaracterizes.

9 A I think with the same caveats and the
10 caveat about deciding whether 67 is part of source
11 driver module, you know, Figure 5 shows what it
12 shows. It shows source driver 61 and the arrow
13 generally pointing to all of these components.
14 Not every component of source driver module might
15 be depicted here.

16 Q Right. But for example, you know, the two
17 power line VSS and VDD, the output devices 70, the
18 connections between the output devices and the
19 power lines, the contact pad 72, those are all
20 part of source driver module 61 as it is shown in
21 this figure, excepting that as you point out there
22 may not be things that are depicted in Figure 5?

1	A	Same answer as before.	12:25:21
2	Q	Okay.	12:25:32
3	A	The figure is -- is pretty clear to me any	12:25:33
4		ways. I -- label 61 is indicating, you know,	12:25:38
5		generally what's seen in Figure 5 and -- an arrow	12:25:45
6		associated with 61.	12:25:50
7	Q	Understood. Yeah. I wasn't trying to ask	12:25:55
8		any different question. I appreciate that.	12:25:57
9	MR. JONES:	Nick, could we screenshot or	12:26:02
10		copy that red box I drew and label this as	12:26:08
11		Exhibit 1005-1 as we discussed at the beginning?	12:26:13
12	MR. RODKEY:	Counsel, just for proprietary	12:26:18
13		sake, this needs to have a 2000 label.	12:26:21
14	MR. JONES:	Oh, good point. Let's do	12:26:24
15		Exhibit 2005 then.	12:26:30
16	REMOTE TECHNICIAN:	Okay. Sounds good. I	12:26:38
17		can do that.	12:26:40
18		(Exhibit 2005 marked for identification.)	12:26:42
19	Q	So Dr. Murphy, back to Figure 5. I	12:27:29
20		removed the red annotations I made.	12:27:34
21		So Reiner doesn't include a figure like	12:27:37
22		Figure 5 that is specific to the gate drivers 63	12:27:42

1 in Reiner; is that right? 12:27:49

2 A Figure 5 is the only one just like it. 12:28:01

3 And you know, I discussed in my declaration how a 12:28:05

4 person of ordinary skill would understand that a 12:28:09

5 source driver module be similarly arranged and be 12:28:15

6 obvious for a person of ordinary skill to apply 12:28:21

7 the teachings of Reiner related to this 12:28:24

8 example -- sorry, I think I misspoke a moment ago. 12:28:28

9 But I'll continue the -- person of 12:28:33

10 ordinary skill would understand that the teachings 12:28:38

11 of Reiner here for 61, the source driver module 12:28:39

12 would be -- could be applied because of their 12:28:44

13 similarities to gate driver module 63. But again, 12:28:49

14 that's a separate figure dedicated to and labeled 12:28:53

15 63 is not here in Reiner. 12:29:00

16 Q And there's also not a corresponding 12:29:09

17 detailed written description of gate driver 63 the 12:29:12

18 way there is for source driver 61 on lines 1 12:29:15

19 through 23 of page 10, right? 12:29:21

20 A The written description about Figure 5 12:29:24

21 is -- is about Figure 5. And it's labeled 61 12:29:48

22 which in many places is identified as a source 12:29:52

1 driver module. In other places, other many
2 places, 61 is referring to generically as a
3 display driver.

4 And a person of ordinary skill would
5 understand that, you know, both as described in
6 Reiner page 9 line 10 through about -- 10 through
7 15 both have typically -- that is both source
8 driver modules and gate driver modules typically
9 have large number of parallel outputs, among other
10 similarities.

11 MR. JONES: Can we get Figure 5 back up on
12 the Zoom screen, please?

13 Q So your source driver module as shown in
14 Figure 5 compared to a gate driver, what changes
15 would you make to Figure 5 to show those
16 differences or to -- well, let's -- I'll leave it
17 at that.

18 A Figure 5 is at a sufficient level of
19 abstraction that I wouldn't make any changes. In
20 fact, in my declaration, I use Figure 5 in a
21 modified and repeated composite image to represent
22 what a person of ordinary skill would understand a

12:29:57

12:30:01

12:30:05

12:30:08

12:30:11

12:30:16

12:30:25

12:30:31

12:30:33

12:30:40

12:30:44

12:30:47

12:31:10

12:31:14

12:31:19

12:31:27

12:31:31

12:31:37

12:31:40

12:31:43

12:31:49

12:31:55

1 source driver module would look -- sorry, I 12:32:00

2 misspoke, what a gate driver would look like. 12:32:05

3 Q Would a great -- excuse me. 12:32:19

4 Would a gate driver module require any 12:32:22

5 wirings interconnecting the output devices 70 that 12:32:32

6 would not be required in a source driver? 12:32:36

7 A Potentially. I couldn't rule that out but 12:32:39

8 I don't know -- well, I'll say that it's clear 12:32:49

9 from reviewing Reiner to a person of ordinary 12:32:53

10 skill that the general arrangement of ESD and 12:32:56

11 other driver components are the focus of this 12:33:06

12 figure. And so the presence or absence of other 12:33:12

13 less-related, unrelated connections is not really 12:33:17

14 germane to understanding Reiner's teaching with 12:33:22

15 regards to Figure 5 or ESD devices and their 12:33:28

16 placement generally. 12:33:30

17 Q Let's go back to rounding out the 12:34:05

18 components -- shown in Figure 5, specifically I'd 12:34:08

19 just like to walk through the ESD 1 through 3 12:34:12

20 protection circuits and understand how they 12:34:18

21 function. 12:34:20

22 To start that off, though, it's your 12:34:21

1 opinion that a POSITA would have recognized per 12:34:28
2 the configuration shown in Figure 5 that the input 12:34:33
3 terminal for the two power supply lines would be 12:34:36
4 located above ESD3 in Figure 5; is that right? 12:34:39

5 If helpful, I direct you to paragraph 100 12:35:34
6 of your declaration where you discuss this. 12:35:38

7 A Yeah. I'd read off in that location 12:35:57
8 paragraph 100, I address this. Cutting to the 12:36:01
9 chase, a POSITA would have generally recognized 12:36:08
10 that the configuration in Figure 5 of Reiner would 12:36:11
11 have had the input terminals above the first ESD3. 12:36:17
12 This was also conventional from the prior art and 12:36:24
13 how a person of ordinary skill would typically 12:36:27
14 understand the labeling in Figure 5 as shown. 12:36:32

15 Q So if we treat the VSS and VDD text at the 12:36:59
16 top of each power line in Figure 5 as the input 12:37:05
17 terminal, that's where they are -- well, let me do 12:37:16
18 that again. 12:37:26

19 You see the VSS and VDD text above lines 12:37:26
20 71 and 73 in Figure 5, correct? 12:37:35

21 A Yes. 12:37:38

22 Q That's -- that can -- that would represent 12:37:38

1	where, per your opinion, in your declaration a	12:37:45
2	POSITA would understand the input terminals for	12:37:48
3	those two power lines would be located relative to	12:37:50
4	everything else shown in Figure 5; is that right?	12:37:54
5	A Yes. That's a conventional way input	12:37:59
6	terminals can be labeled and a POSITA would	12:38:11
7	understand it that way.	12:38:14
8	Q If we treat the VSS and VDD text as input	12:38:16
9	terminal for the power supply lines and then those	12:38:26
10	are two connections -- two -- two connections to	12:38:28
11	outside of the source driver module 61.	12:38:37
12	MR. RODKEY: Objection, form.	12:38:46
13	Q Would you agree with that?	12:38:47
14	MR. RODKEY: Objection, form.	12:38:49
15	A There's two senses that are not clear or	12:38:49
16	the question -- other than to say that the power	12:39:36
17	supply source typically would be outside of the	12:39:42
18	entire display and VSS and VDD, the input	12:39:49
19	terminals, are going to provide connection in that	12:39:58
20	direction to these power supply that is outside of	12:40:02
21	the entire display. I think that's the sense	12:40:10
22	where I'm understanding your question.	12:40:13

1 Q Yeah. I think that was a poorly worded
2 question but I appreciate your attempt to answer
3 the bad question.

4 Let's move on to going through each ESD1,
5 2, and 3, starting with ESD1.

6 MR. JONES: Nick, would you mind zooming
7 in on Figure 5 just a little bit? Okay.

8 Q Does that work for you, Dr. Murphy, where
9 we have it displayed now?

10 A Yeah. This works.

11 Q Okay. So ESD1 is connected to output line
12 75 to the contact pad 72, and output device 70,
13 correct?

14 A Yes.

15 Q Does ESD1 protect output device 70 from
16 charges entering through contact pad 72 that would
17 otherwise travel along line 75 and enter output
18 device 70?

19 A I think, in general, and this is at line
20 106 of my declaration, Reiner discloses that three
21 ESD devices ESD1, ESD2, and ESD3 are provided for
22 each output device 70 in order to protect the

1 circuitry inside the devices. It may not be the
2 case that Reiner provides a detailed description
3 of the manner exactly in which the ESD device
4 provide the protection. You can see it's the
5 Figure 5 depicts where the arrangement and
6 connection points here.

7 Q I'm asking specifically for ESD1,
8 what -- what function it serves in terms of ESD
9 protection. So does it -- does ESD1 protect
10 (technical disruption) that otherwise travel along
11 line 75 and enter?

12 THE REPORTER: Counsel, you cut out for
13 me. Can you repeat your question?

14 Is he frozen or is it me?

15 Can we go off the record?

16 (Off-the-record discussion.)

17 MR. JONES: Can everyone hear me?

18 MR. RODKEY: Yes.

19 MR. JONES: Okay.

20 BY MR. JONES:

21 Q So Dr. Murphy, again, for ESD1 shown in
22 Figure 5, my question is, does it protect output

1 device 70 from charges entering through contact

12:45:40

2 pad 72 that would otherwise travel along line 75

12:45:44

3 and enter output device 70?

12:45:49

4 A Again, I don't think that Reiner gets into

12:46:34

5 that level of detail unless I'm just not able to

12:46:39

6 find it here in the text of Reiner, you know,

12:46:42

7 precisely how ESD1 provides the protection to

12:46:46

8 circuit -- output device and the circuitry in item

12:46:52

9 70 there.

12:46:58

10 Q Dr. Murphy, you're an expert in ESD

12:47:01

11 protection for integrated circuits, right? So in

12:47:06

12 -- what is your opinion?

12:47:09

13 A There are a number of ways ESD protection

12:47:16

14 could be provided. And what you've described, I

12:48:02

15 can't immediately rule it out that it functions

12:48:10

16 that way. It may function in other ways.

12:48:12

17 Q What other ways -- what are the other ways

12:48:17

18 in which it could function -- in which it can

12:48:22

19 function in your opinion?

12:48:26

20 A I mean, in general, ESD devices direct or

12:48:29

21 spread current so that it's not as concentrated in

12:48:45

22 a certain location. It spreads it physically or

12:48:52

1 through use of resistances generally reduce

12:48:56

2 current, you know.

12:49:04

3 Reiner is not giving that level of detail

12:49:06

4 as precisely how this ESD1 is constructed or how

12:49:10

5 it functions. And so I think we can leave it open

12:49:15

6 to other ways, you know, broadly speaking without

12:49:18

7 restricting, you know, potentially any of the ways

12:49:29

8 that ESD devices typically function.

12:49:32

9 Q Understood. But I'm -- I'm specifically

12:49:36

10 asking about ESD1, you know, the configuration

12:49:39

11 shown in Figure 5.

12:49:44

12 What other -- what are the other ways in

12:49:46

13 which it could function other than to protect

12:49:51

14 output device 70 from charges that could enter

12:49:55

15 contact pad 72 and travel along line 75 to enter

12:50:00

16 output device 70?

12:50:12

17 A I wouldn't even limit it to protecting

12:50:13

18 output device 70. It could be protecting other of

12:50:17

19 the components as well. In my analysis, I

12:50:22

20 identified it as having by virtue of its

12:50:27

21 connections providing protection, but it could be

12:50:34

22 providing protection to other components beyond

12:50:40

1	item 70.	12:50:44
2	Q What other components could it be	12:50:48
3	providing protection?	12:50:51
4	A For example, to the extent there are any	12:50:56
5	lines or connection points that it is connected	12:51:00
6	to, wires, you might call them that are depicted	12:51:07
7	schematically here, could provide protection for	12:51:12
8	those as well as shown in Figure 5.	12:51:15
9	Q So as depicted in Figure 5, ESD1 is	12:51:25
10	connected to VDD, line 74, and ESD2. That -- is	12:51:33
11	that accurate?	12:51:47
12	MR. RODKEY: Objection, mischaracterizes.	12:51:51
13	A I think it depends on your definition of	12:52:21
14	"connection." When I was answering a question, my	12:52:23
15	previous answer was, you know, identified at least	12:52:41
16	the vertical line directly below ESD1 and the	12:52:48
17	horizontal line directly to the right of the ESD1	12:52:55
18	as potentially additional components that are	12:52:59
19	being provided protection by ESD1.	12:53:02
20	MR. RODKEY: Counsel, we've been going a	12:53:10
21	little over an hour 20. Do you mind if we take a	12:53:12
22	break soon?	12:53:16

1	MR. JONES: Yeah. We can take a break now	12:53:16
2	and come back to this.	12:53:18
3	MR. RODKEY: Okay.	12:53:19
4	THE VIDEOGRAPHER: We are going off the	12:53:20
5	record. The time is 12:53 p.m.	12:53:22
6	(Whereupon a break was had.)	12:53:24
7	THE VIDEOGRAPHER: We are going back on	12:59:10
8	the record. The time is 12:59 p.m.	12:59:23
9	BY MR. JONES:	12:59:25
10	Q Can we put Reiner Figure 5 back up on the	12:59:27
11	Zoom, please?	12:59:31
12	Dr. Murphy, yes-or-no question: Does ESD1	12:59:46
13	protect output device 70 from charges entering	12:59:54
14	through contact pad 72 that would otherwise travel	12:59:58
15	along line 75 and enter through output device 70?	13:00:02
16	A I think I've answered that to the effect	13:00:07
17	that Reiner doesn't provide detailed descriptions	13:00:25
18	of how the ESD protection circuits there provide	13:00:32
19	protection that they do. I haven't excluded that	13:00:37
20	manner in which you are describing how it	13:00:41
21	functions from being one of the ways it provides	13:00:44
22	protection.	13:00:50

1	Q So yes?	13:00:53
2	A Well, yes was not my answer. My answer	13:01:03
3	was my answer and hopefully my answer could be	13:01:06
4	understood.	13:01:18
5	Q Can you give a yes-or-no answer to the	13:01:37
6	question?	13:01:40
7	A I think if it were a situation where I	13:01:44
8	could provide a very short answer, then I	13:02:17
9	certainly would have. I'm trying to do my best to	13:02:22
10	give an answer that is as complete as possible.	13:02:26
11	Q Is it your testimony that you don't know	13:02:32
12	how Reiner's ESD protection means function as	13:02:59
13	shown in Figure 5?	13:03:06
14	A No. That's not what I said.	13:03:09
15	Q So if you do know -- let's focus on ESD1.	13:03:54
16	If you do know how ESD1 works, yes or no,	13:03:58
17	does ESD1 protect output device 70 from charges	13:04:03
18	entering through contact pad 72 that would	13:04:07
19	otherwise travel along line 75 and enter output	13:04:10
20	device 70?	13:04:14
21	A I think I've answered the question a	13:04:27
22	couple times. And I haven't excluded that way	13:04:29

1 you're describing as being one of the ways it
2 could work. It could work other ways and Reiner
3 doesn't provide a detailed description exactly of
4 all the different ways it is intended to work.

5 The depiction in Figure 5 and the
6 disclosures are -- Reiner related to primarily the
7 arrangement and connection relative of -- the ESD
8 and portions of the circuitry, of the primarily
9 relied upon the teachings of Reiner and
10 disclosures of Reiner in my analysis for the
11 invalidity opinions for the '157 patent.

12 Q In the context of Figure 5 focusing
13 specifically on ESD1, what are the specific other
14 ways that, in your opinion, ESD could function to
15 provide ESD protection?

16 A Reiner at paragraph -- excuse me. Reiner
17 at page 10 lines 15 to 17 discusses how ESD
18 protection network such as ESD1, ESD2, and ESD3
19 can be configured to, among other things, protect
20 a power line and the manner in which any of those
21 ESD protection devices work is to provide a low
22 ohmic path to ground terminal in case of a voltage

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13:05:00

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13:05:44

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13:07:05

13:07:10

13:07:17

1	peak, a voltage peak being one type of an ESD	13:07:22
2	event.	13:07:26
3	Q ESD1 as shown in Figure 5, where is the	13:07:26
4	low ohmic path to ground terminal?	13:07:59
5	A I indicated in my response and in my	13:08:06
6	declaration at page 119 might not be shown all	13:08:09
7	the -- excuse me, all the connections for the ESD	13:08:16
8	circuitry may not be shown in Figure 5, does not	13:08:20
9	appear to be shown explicitly here in -- in Figure	13:08:26
10	5.	13:08:50
11	Q Can you annotate Figure 5 that we have	13:08:50
12	here shown on the Zoom to show where those other	13:08:55
13	connections would be for ESD1?	13:09:00
14	MR. RODKEY: Incomplete hypothetical;	13:09:06
15	speculation.	13:09:11
16	A There are a number of missing pieces from	13:09:37
17	Figure 5 that are not depicted. And again, the	13:09:41
18	intent here of Figure 5 is to show connections in	13:09:48
19	relative arrangements of the circuits, power	13:09:51
20	lines, and the ESD devices. So it's not a	13:10:00
21	complete depiction of all possible for all	13:10:07
22	connections.	13:10:10

1 Q I want to make sure I understand all of 13:10:32
2 your opinions about how ESD1 works. One way as 13:10:34
3 we've discussed is it can protect output device 70 13:10:39
4 from charges that could enter contact pad 72 and 13:10:46
5 travel along lines 75 into output device 70. 13:10:50

6 Can you name a second way that ESD1 as 13:10:55
7 shown in Figure 5 provides ESD protection? 13:11:05

8 A As in my previous answer, I'll read it off 13:11:10
9 again. Page 119 paragraph 181 of my declaration: 13:11:17
10 Reiner's ESD protection network such as ESD1, 13:11:29
11 ESD2, ESD3, can protect the power line because 13:11:33
12 they're configured to provide a low ohmic path to 13:11:40
13 ground terminal in case of an ESD event. The 13:11:45
14 power supply line can be protected because ESD 13:11:49
15 generated on the power supply lines that 13:11:54
16 would -- would be a voltage peak, also known as 13:12:00
17 electrostatic discharge, that could be shunted by 13:12:05
18 components of ESD 1. Some of the components that 13:12:09
19 Reiner mentions that may be inside ESD are diodes 13:12:11
20 or transistors. 13:12:15

21 Q That's not my question. How does ESD1 13:12:23
22 protect a power line as shown in Figure 5? 13:12:27

1 MR. RODKEY: Objection, asked and
2 answered.

3 A Considering Figure 5 and the descriptions
4 of the components in Figure 5, I think I'll rely
5 on my previous answer to answer your most recent
6 question.

7 A person of ordinary skill reading Reiner
8 is going to take advantage of the descriptions,
9 written descriptions, to provide additional
10 context and labeling and discussion of the
11 figures.

12 Q If a static charge were to enter the VDD
13 line 73 in Figure 5, from the input terminal how
14 would ESD1 protect VDD?

15 A I'll refer you, again, to paragraph 181
16 page 119 where I describe how in the written
17 description of Reiner it discusses how an ESD
18 device can provide a low ohmic to the ground
19 terminal. Ground terminal is not depicted
20 explicitly in paragraph 5.

21 Q Are you unable to answer that question for
22 ESD1 specifically as shown in Figure 5?

13:12:32

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13:13:53

13:13:58

13:14:06

13:14:12

13:14:59

13:15:05

13:15:10

13:15:16

13:15:19

13:15:42

13:15:46

1	MR. RODKEY: Objection, question answered.	13:15:51
2	A I refer you to my answers I gave to your	13:15:56
3	previous questions. The ESD1 is going to be	13:16:29
4	described not just in the figure but in the -- in	13:16:36
5	the written descriptions in Reiner.	13:16:44
6	Q Can you explain to me how ESD1 would	13:16:58
7	protect line VDD if a static charge were to enter	13:17:02
8	the input terminal at the top of the figure?	13:17:10
9	MR. RODKEY: Objection, asked and	13:17:21
10	answered.	13:17:45
11	A Just refer you to my previous answer. It	13:17:45
12	relies on the disclosures of Reiner.	13:18:00
13	Q Your previous answer did not answer my	13:18:12
14	question. I'll ask it one more time, then we can	13:18:23
15	move on.	13:18:26
16	Using Figure 5, can you explain to me how	13:18:27
17	ESD1 would protect VDD line if a charge enters the	13:18:31
18	input terminal at the top of Figure 5?	13:18:38
19	MR. RODKEY: Objection, asked and	13:18:41
20	answered.	13:18:43
21	A Same answer to your earlier questions,	13:18:43
22	just with the understanding that Figure 5 is going	13:19:12

1 to be understood in the full context of the rest 13:19:17
2 of the disclosures of Reiner and may not depict 13:19:23
3 every possible connection that's going to exist 13:19:30
4 and is, you know, primarily oriented around the 13:19:32
5 relative arrangements and -- and electrical 13:19:39
6 connections of the ESD circuits to power lines and 13:19:45
7 to other circuitry generally to be protected. 13:19:48

8 Q So you mentioned that the written -- in 13:20:04
9 the written description, Reiner explains that the 13:20:12
10 ESD protection circuits need to provide a low 13:20:19
11 ohmic path to ground. Reiner discloses that those 13:20:20
12 low ohmic paths are indicated in Figure 5 by 13:20:27
13 bolded lines, correct? 13:20:30

14 A Where are we in Reiner that has that, if 13:20:32
15 you don't mind? 13:20:43

16 Q Yeah. Page 10 lines 17 through 19. I'll 13:20:44
17 read it out, quote: It is important that certain 13:21:02
18 of the lines of the device 61 provide for a low 13:21:05
19 ohmic connection to the desired terminal. These 13:21:08
20 lines are shown as bold lines. 13:21:12

21 A I found you. Could you repeat the 13:21:35
22 question? 13:21:43

1 Q Where are those low ohmic connections 13:21:44
2 indicated by a bolded line in Figure 5? 13:21:59

3 A The low ohmic requirement is not for all 13:22:35
4 ESD devices, per se. The line preceding on 13:22:41
5 page 10 in Reiner starting on the end of line 15 13:22:46
6 states: The ESD devices may comprise IO 13:22:50
7 transistors and other circuits and continuing 13:22:54
8 identifies that certain of the lines provide a low 13:23:04
9 ohmic connection. 13:23:08

10 In the context of Reiner, you have poly 13:23:12
11 silicon and you have metal as being the primary 13:23:16
12 wiring or electrical connection means. So 13:23:27
13 depending on how the designer would implement the 13:23:36
14 network shown in Figure 5, they would choose 13:23:39
15 potentially different of these materials. 13:23:48

16 Whether any particular of these lines is 13:23:58
17 bolded or not really wasn't relevant to my 13:24:02
18 analysis in the context of my invalidity opinions 13:24:06
19 on the '157. So I can't express a strong view as 13:24:12
20 I sit here today as to identifying which of these 13:24:25
21 lines are -- are bold or not. 13:24:30

22 Q So it's your opinion that the low ohmic 13:24:40

1 connections to desired terminal which provide a 13:24:45
2 path to ground for ESD events is not relevant to 13:24:50
3 understanding how ESD1 or ESD2 or ESD3 in Figure 5 13:24:58
4 functions to serve an ESD protection purpose? 13:25:10

5 MR. RODKEY: Objection, mischaracterizes 13:25:14
6 testimony. 13:25:17

7 A My analysis was primarily of the 13:25:17
8 disclosures of Reiner and Takahara in relation to 13:25:26
9 the claims of the '157. And I was less concerned 13:25:38
10 with the precise nature in which any given ESD 13:25:40
11 protection circuit might function and the means 13:25:45
12 exactly by which it might function. 13:25:48

13 Q Do you have any other opinions regarding 13:26:04
14 how ESD functions to protect source driver 61 or 13:26:07
15 the devices in lines within source driver 61 from 13:26:20
16 ESD events? 13:26:24

17 A I think my opinions are laid out in my 13:26:27
18 declaration. If it's in there, it's my opinion. 13:26:30
19 I think we summarized my opinions early on but 13:26:37
20 that summary still stands. 13:26:40

21 Q In your prior answer you stated you were 13:26:56
22 less concerned with the precise nature in which 13:26:58

1 any given ESD protection circuit might function,
2 the means exactly by which it might function.

3 Does that mean you don't have a specific
4 opinion about how any of the ESD devices in Reiner
5 are shown here in Figure 5 specifically work?

6 MR. RODKEY: Objection, mischaracterizes.

7 A I also said earlier that Reiner provides
8 some description for the components that may be
9 used and whether a low ohmic path to a ground
10 terminal could be used. Those are the contents of
11 Reiner that I'm relying on to understand how the
12 ESD protection circuits might work.

13 Q Let's turn to ESD2 as shown in Figure 5.
14 ESD2 is connected to line 75 between contact pad
15 72 and output device 70; is that right?

16 A Yeah. That's how it's depicted there in
17 Figure 5, I see that connection point between 72
18 and 75.

19 Q Is it correct that ESD2 protects output
20 device 70 from charges entering through contact
21 pad 72 that would otherwise travel along lines 75
22 and enter output device 70?

13:27:01

13:27:02

13:27:06

13:27:08

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13:27:50

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13:28:58

13:29:02

13:29:03

13:29:18

13:29:22

13:29:26

1	A I'm sorry, could you repeat that	13:29:30
2	description one more time?	13:30:09
3	Q Sure. Do you agree that ESD2 protects	13:30:10
4	output device 70 from charges entering through	13:30:18
5	contact pad 72 that would otherwise travel along	13:30:22
6	line 75 and enter output device 70?	13:30:27
7	A I think Reiner doesn't give a very	13:30:37
8	detailed description, but that could be one of the	13:30:41
9	ways that ESD2 works.	13:30:46
10	Q Any other ways?	13:30:48
11	A Could you rephrase that question, please?	13:31:17
12	Q Yes. So you agreed that one of the ways	13:31:22
13	ESD works is to protect output device 70 from	13:31:38
14	charges entering through contact pad 72 that would	13:31:43
15	otherwise travel along line 75 and enter output	13:31:46
16	device 70.	13:31:51
17	Are there any other ways that ESD2 can	13:31:53
18	function to protect what is in -- what is shown in	13:32:01
19	Figure 5?	13:32:09
20	A We can go back to page 118 of my	13:32:33
21	declaration where I -- and 119 and 120 where I	13:32:38
22	identify that ESD1, 2, or 3 can protect the power	13:32:41

1 line. And the reasons are -- are given similarly 13:32:48
2 to our earlier discussion with regards to ESD1 13:32:55
3 providing protection of the power line. So that's 13:33:01
4 at least one other way ESD2 can provide protection 13:33:11
5 to what's shown on Figure 5. 13:33:14

6 Q Can you explain to me right now looking at 13:33:17
7 Figure 5 specifically how ESD2 could protect 13:33:43
8 either of the power lines, VSS or VDD, shown in 13:33:53
9 Figure 5? 13:33:56

10 A We can go back to page 119, top of 13:33:57
11 page 119 which is middle of paragraph 181 of my 13:34:13
12 declaration where I discuss how the ESD protection 13:34:18
13 network such as ESD1, ESD2, or ESD3 can protect 13:34:21
14 the power line. It's configured to provide a low 13:34:26
15 ohmic path to a ground terminal. The ground 13:34:33
16 terminal is not depicted here in Figure 5. 13:34:37

17 So that's one way in which that might 13:34:40
18 provide protection. ESD1, 2, and 3 and this is 13:34:43
19 also in that same paragraph of my declaration, can 13:34:49
20 provide protection of thermal damage. That's 13:34:53
21 another way that ESD2 can protect the power line. 13:35:06

22 Q The ground terminal is not depicted in 13:35:21

1 Figure 5, but further in description, the low 13:35:25
2 ohmic connections that provide a path to ground 13:35:30
3 are. 13:35:36

4 Can you show me where those low ohmic 13:35:39
5 connections as shown by bolded lines are with 13:35:42
6 respect to how ESD2 functions to protect either of 13:35:48
7 the power lines in Figure 5? 13:35:52

8 A I'm not sure I understand your question. 13:35:54
9 Can you read through that again, please? 13:36:31

10 Q Can you identify for me the low ohmic 13:37:08
11 pathways indicated by bolded lines in Figure 5? 13:37:14

12 A I think I'll have the same answer as 13:37:21
13 before I gave previously to this same question. 13:37:25

14 Q Which was what? 13:37:38

15 A At the risk of repeating myself and 13:37:40
16 repeating myself using slightly different words 13:37:45
17 than I used before, the particular individual low 13:37:50
18 ohmic -- excuse me, the particular individual 13:37:56
19 lines that are bolded in Figure 5 was not 13:38:01
20 something that was part of my invalidity analysis 13:38:04
21 of the '157 claims. 13:38:12

22 Q Can you identify those lines now? 13:38:18

1 A Again, not an exercise that I thought was 13:38:23
2 relevant to my invalidity analysis of '157. It's 13:39:09
3 not something that I could necessarily do on the 13:39:13
4 spot because it would involve some further 13:39:19
5 analysis of Reiner and study of the Figure 5 as 13:39:23
6 well as the written description. 13:39:30

7 Q How much time would you need to perform 13:39:32
8 that further analysis to identify the bold lines 13:39:51
9 shown in Figure 5? 13:39:54

10 A I'm not sure until I have done it. 13:39:55

11 Q You think it would be hours? 13:40:08

12 A Potentially. I don't know until I have 13:40:16
13 done it. 13:40:21

14 Q Just -- just to be clear, I'm -- I'm 13:40:38
15 asking you to identify the bold lines in Figure 5. 13:40:42
16 You tell me you cannot do that right now sitting 13:40:45
17 here looking at Figure 5? 13:40:48

18 A Bold lines have, according to what's in 13:40:56
19 Reiner, certain significance and meaning, so I 13:41:01
20 need to review in careful detail the specification 13:41:12
21 of Reiner to understand the figure appropriately. 13:41:20
22 That's not something I've done as of yet with 13:41:26

1	regard to your question about bold lines in Figure	13:41:33
2	5.	13:41:33
3	Q We can take a break to give you the chance	13:42:17
4	to review the written description relating to the	13:42:22
5	bolded lines that are the low ohmic pathways. How	13:42:24
6	much time do you think you would like?	13:42:28
7	MR. RODKEY: Absolutely not, Counsel. If	13:42:29
8	you want him to review it, it's going to be on the	13:42:31
9	record.	13:42:34
10	Q All right. Dr. Murphy, please take a look	13:42:37
11	through the Reiner written description and let me	13:42:42
12	know once you're prepared to identify the bolded	13:42:47
13	lines in Figure 5.	13:42:50
14	Dr. Murphy, it's been about 15 minutes,	13:56:55
15	are you still working on identifying the bold	13:56:58
16	lines the Figure 5?	13:57:01
17	A Still work in progress, yes.	13:57:02
18	Q Okay. We can -- we can move on for now.	13:57:04
19	Just to confirm, though, you did not consider how	13:57:08
20	Reiner depicts low ohmic pathways in Figure 5 as	13:57:12
21	part of forming your opinions in support of the	13:57:16
22	'157 IPR petition; is that right?	13:57:22

1	A That's more or less what I said earlier.	13:57:30
2	What I said earlier was that precisely which were	13:57:33
3	low ohmic paths as depicted in Figure 5, it	13:57:38
4	would -- understood in the context of the rest of	13:57:45
5	the disclosures, was not a part of my invalidity	13:57:48
6	analysis with respect to the claims of the '157.	13:57:52
7	Q Okay. Back to Figure 5. Let's move on to	13:58:08
8	ESD3. ESD3 is connected to the VSS and the VDD	13:58:12
9	line; is that right?	13:58:21
10	A So the two you identified in your question	13:58:32
11	are among the connections of ESD3. Yes.	13:59:44
12	Q What other connections of ESD3 are there	13:59:49
13	as shown in Figure 5?	13:59:56
14	A Well, if we refer to my declaration around	13:59:58
15	paragraph 110, I was asked to consider the	14:00:02
16	situation in which ESD3 is considered to be	14:00:06
17	connected to the scanning line drive circuit 70.	14:00:10
18	I didn't independently analyze whether that's the	14:00:18
19	case and haven't expressed an opinion as to	14:00:21
20	whether this is correct to say that ESD3 is,	14:00:25
21	indeed, connected to scanning line drive circuit	14:00:37
22	70. But that's another connection of ESD3 that is	14:00:42

1	the subject of my analysis.	14:00:45
2	Q So in your opinion, is ESD3 connected to	14:00:51
3	output device 70?	14:00:54
4	A I haven't developed an opinion on that	14:00:56
5	question.	14:01:00
6	Q What would you need to do to develop an	14:01:07
7	opinion on that question?	14:01:11
8	A To start with, at least have an	14:01:12
9	understanding of the definition of "connected"	14:01:23
10	that's being -- that's operative in the present	14:01:29
11	discussion or any discussion on the topic.	14:01:38
12	Q What's the -- what definition would you	14:01:55
13	use on this topic for whether ESD3 is connected to	14:01:59
14	output device 70?	14:02:06
15	A It depends what the context was and what	14:02:07
16	the ultimate goal I might be striving for would	14:02:32
17	be, what question to be answered, what	14:02:44
18	understanding to be developed, what tests to do.	14:02:47
19	Ultimately, I'd have to understand the context to	14:02:50
20	be able to -- to understand what, you know, what	14:02:53
21	the appropriate definition of connected might be	14:03:00
22	for doing an analysis.	14:03:03

1 Q In the context of the '157 patent and the
2 Reiner reference we're looking at here, that is
3 the context, do you have an opinion as to
4 whether -- or what definition you'd use for
5 connected to, to evaluate whether ESD3 is
6 connected to output device 70?

14:03:05
14:03:17
14:03:20
14:03:25
14:03:27
14:03:32

7 A You know, I don't know that there's one
8 right or single definition that's appropriate even
9 just given the context you've described. It could
10 be analyzed with using one definition, another --
11 another definition. I wouldn't know immediately
12 what the appropriate definition to use would be.

14:03:35
14:03:39
14:03:44
14:03:49
14:03:53
14:04:00

13 Q What is your opinion as someone who's
14 skilled in the relevant art here whether ESD3 is
15 connected to output device 70?

14:04:24
14:04:27
14:04:34

16 A If we're considering the context of why
17 we're gathered here today, talk about my opinions
18 relate -- in relation to the invalidity of the
19 '157 patent claims, I'll point out that
20 "connected" is a claim term; and therefore, it
21 would -- it may in some instances have a
22 construction provided to it. I've used, in

14:04:41
14:04:46
14:04:50
14:04:54
14:04:58
14:05:07
14:05:11

1 general, the plain and ordinary meaning.

14:05:18

2 Q So using the plain and ordinary meaning,
3 is ESD3 connected to output device 70?

14:05:27

14:05:44

4 A I don't have an opinion as to that
5 question. Wasn't something that was developed in
6 detail as part of my analysis for the '157 patent.
7 Like I said, in paragraph 110 of my declaration,
8 the -- I was asked to consider the situation where
9 ESD is connected, is considered to be connected to
10 the scanning line drive circuit. I made that
11 assumption and did my analysis without having to
12 develop a particular definition of "connected."

14:05:49

14:06:27

14:06:31

14:06:35

14:06:41

14:06:46

14:06:50

14:06:54

14:06:59

13 Q I understand that you did not take a
14 position on this question in your declaration.
15 I'm asking you whether as a person skilled in the
16 relevant art, is ESD3 connected to output device
17 70?

14:07:25

14:07:28

14:07:32

14:07:35

14:07:41

18 A I answered that question earlier. It
19 would -- effectively to tell you that, it depends
20 on the -- on what "connected" means.

14:07:45

14:07:49

14:07:55

21 Q And if you take the meaning of "connected"
22 in terms of the plain and ordinary meaning as you

14:08:03

14:08:07

1	understand it, can you offer an opinion as to	14:08:09
2	whether ESD3 is connected to output device 70?	14:08:18
3	MR. RODKEY: Objection, asked and	14:08:24
4	answered.	14:10:35
5	A Developing a particular definition for	14:10:35
6	connected was not part of the scope of my work in	14:10:39
7	analyzing the '157 patent and the validity or	14:10:46
8	invalidity of the claims of the '157 patent. I	14:10:54
9	was asked to consider a particular situation	14:10:57
10	and -- and did in order to, you know, reach an	14:11:03
11	opinion as to certain of the claim -- to the	14:11:09
12	validity of certain of the claims.	14:11:15
13	Q Dr. Murphy, do you the context of this	14:11:28
14	question, you have the definition -- or the	14:11:31
15	definition being plain and ordinary meaning.	14:11:36
16	What else would you need to form an	14:11:38
17	opinion as to whether ESD3 is connected to device	14:11:40
18	70?	14:11:49
19	MR. RODKEY: Objection, asked and	14:11:49
20	answered.	14:11:50
21	A Seems as if I'm being asked to provide a	14:11:50
22	definition with regards to "connected," and I	14:12:42

1 haven't developed that definition so not going to 14:12:52
2 be able to provide one, you know, in the context 14:12:57
3 of the question you're asking. 14:13:03

4 Q I'm giving you the definition. "Connected 14:13:19
5 to" receives its plain and ordinary meaning to a 14:13:25
6 person of skill in the art. You are a person of 14:13:27
7 skill in the art, right? 14:13:30

8 A Yes. 14:13:31

9 Q So using that definition, can you tell me 14:13:32
10 whether in your opinion ESD3 is connected to 14:13:41
11 output device 70? 14:13:45

12 MR. RODKEY: Objection, asked and 14:13:46
13 answered. 14:13:52

14 A I apologize. I haven't developed an 14:13:52
15 opinion on this to be able to answer your 14:13:57
16 particular question. The definition or the 14:13:59
17 assumption of what a definition could be was 14:14:02
18 provided to me for part of my analysis, 14:14:05
19 specifically the part that I'm discussing at 14:14:09
20 paragraph 110 of my declaration. I haven't 14:14:12
21 developed a definition. 14:14:18

22 Q So is it your testimony that you're unable 14:14:21

1 to form an opinion as to whether ESD3 is connected
2 to output device 70?

3 MR. RODKEY: Objection, asked and
4 answered. Counsel, it's about the fifth time.
5 Let's move on.

6 A I didn't say I was not able to. I'll just
7 refer you to my previous answers that I haven't
8 developed a specific definition for that claim
9 term.

10 Q Back to Figure 5. ESD3 is connected to
11 the VDD line between the VDD input terminal and
12 line 74 which connects VDD to output device 70,
13 right?

14 A Just going to refer to my declaration.
15 Sounds as if you're reciting a -- part of the
16 claims of the '157. If so, can you point me to
17 which of the claims or the claim elements so I can
18 read it off?

19 Q I'm not reciting any claim elements. Just
20 looking at Figure 5, ESD3 is connected to the VDD
21 line between where the VDD input terminal would be
22 based on your opinion or someone of skill in the

14:14:26

14:14:29

14:14:31

14:14:32

14:14:35

14:14:41

14:14:45

14:14:50

14:14:56

14:15:02

14:15:11

14:15:17

14:15:30

14:15:30

14:15:51

14:15:54

14:15:57

14:16:00

14:16:03

14:16:06

14:16:13

14:16:23

1 art would understand it to be located between the 14:16:27
2 input terminal and where VDD is connected to 14:16:30
3 output device 70? 14:16:35

4 A Yes. That's what Figure 5 depicts. 14:16:42

5 Q And the same is true for the VSS line, 14:16:44
6 correct? ESD3 is connected to the VSS line 14:16:53
7 between the VSS input terminal and line 76 which 14:16:56
8 connects VSS to output device 70? 14:17:02

9 A Yes. That's what Figure 5 depicts. 14:17:06

10 Q So for static charges, are there ESD 14:17:09
11 events that enter through the VDD input terminal, 14:17:20
12 is it correct that ESD3 protects output device 70 14:17:26
13 from charges that would otherwise travel along 14:17:32
14 VDD, enter output device 70 via line 74? 14:17:35

15 A Without limiting the way ESD protects and 14:17:46
16 all of the scope of the other components that ESD3 14:17:52
17 protects, the way you described is one way that 14:17:55
18 ESD3 could possibly function. 14:17:58

19 Q I'll keep this question brief so you can 14:18:00
20 say yes or no. Are you able to specifically 14:18:10
21 identify any other ways it can -- ESD3 could 14:18:12
22 function to protect circuitry inside source driver 14:18:14

1 61 from charges that enter the VDD input terminal? 14:18:19

2 A Reviewing my declaration. 14:18:25

3 Another way that ESD3 could function is to 14:21:45

4 protect one of the power lines. This is in 14:21:47

5 page 118 to 119 around paragraph 181 where I 14:21:54

6 discuss that. 14:22:03

7 Q Similarly to what I asked you for -- with 14:22:17

8 respect to ESD1 and ESD2 in Figure 5, are you able 14:23:05

9 to describe to me now in terms of Figure 5 how 14:23:08

10 ESD3 functions to protect a power line? 14:23:17

11 A Well, the ground terminal as we discussed 14:23:25

12 earlier is not explicitly shown in Figure 5. 14:23:29

13 That's generally how ESD3 could protect the power 14:23:36

14 line by providing a low ohmic path to a ground 14:23:42

15 terminal. 14:23:53

16 Q Would ESD function to protect the power 14:24:03

17 line in that fashion above where ESD3 is connected 14:24:06

18 to VSS and VDD in Figure 5? 14:24:13

19 MR. RODKEY: Objection, form. 14:24:24

20 A I don't think there's a limit that I've 14:24:25

21 identified to the portion of the power line that 14:24:35

22 ESD3 could protect so I can't exclude that 14:24:39

1 possibility, that it can provide protection to a 14:24:48
2 power line at any location that's shown. 14:24:51

3 Q So if, for example, a static charge were 14:24:59
4 to enter from VDD from the input terminal on the 14:25:03
5 top of VDD line at Figure 5, you're not -- you're 14:25:07
6 not able to say one way or the other whether ESD3 14:25:17
7 would protect VDD from that event prior to the 14:25:21
8 point where ESD3 is connected to VDD? 14:25:27

9 A I think my prior answer was that I am not 14:25:34
10 excluding that possibility, so it is possible to 14:25:40
11 provide protection to the power line at that 14:25:45
12 location above -- well, I'll say above the 14:25:47
13 connection point at ESD3 to the VDD power line 14:25:51
14 that you're talking about. 14:25:55

15 Q Can you tell me how ESD3 would provide 14:26:07
16 that protection in that specific location of VDD? 14:26:16

17 A Well, in addition to providing a low ohmic 14:26:24
18 path to the ground terminal that's not shown, ESD3 14:26:30
19 could, in principle, provide additional 14:26:47
20 resistance, therefore reducing the current through 14:26:52
21 the power line by increasing the impedance that is 14:26:56
22 seen by an ESD event at the VDD terminal. 14:27:06

1	Q	Would the same be true in your opinion for	14:27:38
2		VSS, the VSS line as shown in Figure 5 which	14:27:41
3		is -- there's a portion of it before the	14:27:47
4		connection going to ESD3?	14:27:49
5	A	I would offer, yes, a similar analysis to	14:27:56
6		what I described for VDD.	14:27:59
7	MR. RODKEY:	Counsel, we're at about an	14:28:24
8		hour and a half, so I'm not saying we need to do	14:28:26
9		now, but whenever is convenient, please. Would	14:28:28
10		you agree?	14:28:32
11	MR. JONES:	Yeah. I just have one more	14:28:32
12		thing I'd like to cover and then a break is very	14:28:34
13		appropriate.	14:28:37
14	Q	All right. Dr. Murphy, let's turn back to	14:28:38
15		Reiner Figure 4, please.	14:28:45
16	A	Sure.	14:29:06
17	Q	Okay. So in Figure 5 that we were just	14:29:06
18		looking at, that shows a portion of the source	14:29:11
19		driver 61 disclosed by Reiner, right?	14:29:17
20	A	Yes. That's how Figure 5 is described in	14:29:26
21		Reiner.	14:29:31
22	Q	Is it correct that what is shown in Figure	14:29:35

1	5, all of that would fall within the box titled	14:29:43
2	source driver module labeled 61 in Figure 4?	14:29:49
3	A The figure is schematic here in Figure 4	14:30:10
4	and shows a general arrangement and conceptual	14:30:17
5	connections. In terms of the physical location of	14:30:21
6	the source driver module, it's not clear exactly	14:30:29
7	where, for instance, you know, item 72 from Figure	14:30:32
8	5, that contact point would be on this figure. We	14:30:40
9	know from the discussions and the written	14:30:44
10	description from Reiner that those contact points	14:30:46
11	72 are, more or less, the bump ridges and those	14:30:52
12	are on the pixel substrate. It's somewhat	14:30:59
13	ambiguous precisely the location of the pixel	14:31:06
14	substrate in Figure 4, we have the item 60, the	14:31:12
15	screen, that's somewhat different terminology.	14:31:19
16	So I don't think I can agree with your	14:31:23
17	postulation that everything 61 -- well, you know,	14:31:28
18	that there's a perfect match between what's seen	14:31:36
19	in 61 and what's in Figure 4.	14:31:39
20	Q Do you agree that the output devices 70,	14:31:45
21	VSS and VDD power lines, and ESD connection	14:31:50
22	circuits ESD1 through 3 shown in Figure 5 would	14:31:56

1 be, you know, schematically represented inside the 14:32:00
2 sources driver module box in Figure 4? 14:32:04

3 A With the possible exception of power lines 14:32:08
4 VSS and VDD, the other components you identified 14:32:19
5 ESD1, 2, 3, circuit 70, I think is reasonable to 14:32:23
6 understand those to be within conceptually the box 14:32:31
7 labeled source driver module, again, with the 14:32:37
8 caveat that the precise position of that source 14:32:42
9 driver module is -- is a little bit ambiguous in 14:32:46
10 Figure 4. 14:32:52

11 You know, a person of ordinary skill would 14:33:21
12 readily adapt the teachings related to Figure 5 to 14:33:25
13 gate drivers depicted in Figure 4, in which case, 14:33:31
14 the elements that I addressed earlier would be in 14:33:36
15 the box labeled 63 on Figure 4, if that were the 14:33:41
16 case. 14:33:45

17 MR. JONES: All right. Let's go off the 14:34:00
18 record to take a break. 14:34:02

19 THE VIDEOGRAPHER: We are going off the 14:34:03
20 record. The time is 2:34 p.m. 14:34:05

21 (Whereupon a break was had.) 14:34:07

22 THE VIDEOGRAPHER: We are going back on 14:43:39

1	the record. The time is 2:43 p.m.	14:43:44
2	BY MR. JONES:	14:43:46
3	Q Dr. Murphy, you opined that ESD events	14:43:48
4	could occur on power lines and damage circuitry	14:43:52
5	such as data source drivers connected to that	14:43:57
6	power line; is that correct?	14:44:01
7	A Are you referring to a written statement	14:44:03
8	in my declaration that I can refer to?	14:44:06
9	Q You can go to paragraph 115 on page 82.	14:44:14
10	A Okay. Okay.	14:44:21
11	Q Would you like me to ask the question	14:44:36
12	again?	14:44:44
13	A Yeah. Appreciate it.	14:44:44
14	Q You opined that ESD events could occur on	14:44:45
15	power lines and damage circuitry such as gate or	14:44:49
16	source drivers connected to the power line; is	14:44:51
17	that right?	14:44:55
18	A Sounds like you're paraphrasing in here	14:44:55
19	what I have, so if it's not a direct quote I just	14:45:40
20	appreciate if you repeat that one more time.	14:45:45
21	Q Okay. Is it correct that you opined that	14:45:47
22	ESD events could occur on power lines, those ESD	14:45:56

1 events could travel down power line and damage

14:46:01

2 circuitry that is connected to that power line?

14:46:04

3 A I think as a general statement, I -- I

14:46:08

4 wouldn't say that's necessarily my opinion.

14:46:17

5 That's something that's reasonably well understood

14:46:19

6 in the art and the field. So I'll agree as a

14:46:22

7 general statement.

14:46:24

8 Q Do you agree that a scanning line driving

14:46:29

9 circuit that is formed on the active matrix

14:46:38

10 substrate of TFT LCD display generally does not

14:46:42

11 need ESD protection?

14:46:48

12 MR. RODKEY: Objection, scope.

14:46:49

13 A I don't think I have any specific opinions

14:46:50

14 specific to active matrix TFT LCD devices there,

14:47:01

15 so I'll -- it would be hard for me to agree with

14:47:14

16 you that I offered such an opinion.

14:47:19

17 Q I'm not asking whether you offered that

14:47:33

18 opinion. I'm just asking whether as someone who

14:47:35

19 is skilled in the relevant art, do you agree with

14:47:39

20 that question?

14:47:42

21 MR. RODKEY: Objection, scope.

14:47:43

22 A You'd have to restate it, if you please,

14:47:48

1 for me to hear it one more time.

14:47:52

2 Q Sure. Do you agree that a scanning line
3 driving circuit formed on the active matrix
4 substrate of a TFT LCD device generally does not
5 need ESD protection?

14:47:53

14:47:57

14:48:01

14:48:06

6 MR. RODKEY: Objection, scope; asked and
7 answered.

14:48:07

14:48:25

8 A Well, as you stated it, that's contrary to
9 some of the teachings generally regarding LCD
10 displays, scanning line, and data line circuitry
11 that is the subject of some of the prior art
12 references, in particular Reiner and others. So
13 I -- yeah, I'm not going to agree with that
14 statement as you put it.

14:48:25

14:48:29

14:48:37

14:48:41

14:48:47

14:48:52

14:48:55

15 Q Do you agree that -- and again, from
16 your -- from the perspective of you as a person of
17 skill in the art, do you agree that low resistance
18 metal lines formed on an insulating substrate of a
19 TFT LCD device generally would not be destroyed by
20 an ESD event that travels along that line?

14:49:00

14:49:16

14:49:18

14:49:27

14:49:29

14:49:33

21 MR. RODKEY: Objection, scope; relevance.

14:49:38

22 A All I can really say is that it depends on

14:49:43

1	too many factors to give a simple answer to	14:49:47
2	whether I might agree or disagree, you know, with	14:49:51
3	that statement as you formed.	14:49:56
4	MR. JONES: Let's mark as Exhibit 1007 the	14:51:07
5	file with -- the document with the file name '157	14:51:10
6	IPR EX 1007. I'll also drop it into the chat.	14:51:14
7	(Exhibit 1007 marked for identification.)	14:51:24
8	MR. JONES: I'll remember to send it this	14:51:26
9	time, Kevin.	14:51:28
10	Q Dr. Murphy, do you recognize	14:51:43
11	Exhibit 1005 -- 7, I'm sorry.	14:51:46
12	A I think that I do. Yes.	14:51:51
13	Q It is a translated copy of the Takahara	14:51:59
14	prior art reference ground 2 opinions in support	14:52:07
15	of the '157 IPR petition that are, in part, based;	14:52:08
16	is that right?	14:52:12
17	A Yes. That's what it looks like here.	14:52:12
18	Q Can you turn to page 17, Takahara, and	14:52:15
19	look at Figure 3. And if we could zoom in on	14:52:56
20	Figure 3 on the shared version. Thank you.	14:53:00
21	Dr. Murphy, Figure 3 is a block diagram	14:53:16
22	illustrating the configuration of an ESD	14:53:19

1 protection circuit 150 or 151 shown in Figure 1 of 14:53:22
2 Takahara; is that right? And if you'd like to 14:53:27
3 refer to the written description, that is in 14:53:30
4 paragraph 66. 14:53:34

5 A Yeah. I see at paragraph 57 there's a 14:53:53
6 description as well. 53 is a block diagram 14:53:57
7 illustrating detailed configuration of ESD 14:53:59
8 circuits. That's how it's described in that 14:54:05
9 paragraph too. 14:54:08

10 Q I'd like to just walk through the 14:54:09
11 components that are shown in Figure 3. And then I 14:54:17
12 have a few questions on this. 14:54:22

13 So first let me ask you this first: Is 14:54:23
14 Figure 3 -- is Figure 3 showing one or two 14:54:37
15 electrostatic protection circuits? 14:54:50

16 A If I refer to the written description at 14:54:55
17 paragraph 57 of Takahara, I'll read out what that 14:55:04
18 says about Figure 3. Figure 3 is a block diagram 14:55:10
19 illustrating a detail configuration of 14:55:14
20 electrostatic protection circuits 150 and 151. It 14:55:19
21 may depend on how you slice it where to draw a 14:55:25
22 line between different circuits. This may -- some 14:55:30

1 could consider all the components shown here as 14:55:42
2 part of one circuit. 14:55:44

3 Q Understand. In any case, the -- as 14:55:46
4 depicted in Figure 3, the block diagram that is on 14:55:50
5 the top is identical to the one on the bottom. 14:56:06

6 Do you agree with that? 14:56:11

7 A As it's depicted in a -- generally, yes. 14:56:11
8 I mean, I'll just note that the wiring switch-over 14:56:30
9 portion, there's just one of those between the two 14:56:33
10 upper half and lower half. So if that were to be 14:56:38
11 considered part of either lower half or upper 14:56:44
12 half, that's an asymmetry there. But otherwise, I 14:56:49
13 don't see a visual difference between the upper 14:56:55
14 part of that figure and the lower part that I can 14:56:58
15 find right now. 14:57:03

16 Q Okay. So Figure 3 shows a short-circuit 14:57:07
17 wiring 91, right? 14:57:23

18 A Yes. I can use that terminology, 91. 14:57:26

19 Q And then there are input terminals 800 or 14:57:34
20 801, 802, right? 14:57:42

21 A They are labeled as terminals. I don't 14:57:45
22 know if they have been to be specifically input 14:57:53

1	terminals. But those are there.	14:57:56
2	Q If you -- could you scroll up, I think	14:57:58
3	just one page, and take a quick look at Figure 1.	14:58:05
4	Do you see at the bottom the items labeled 800,	14:58:13
5	801, 802?	14:58:17
6	A Yeah. I see those labels at the left and	14:58:18
7	right lower corner areas.	14:58:25
8	Q Do you agree that those are input	14:58:27
9	terminals?	14:58:29
10	A I know that Takahara identifies them as	14:58:30
11	terminals generally. I think, you know, without	14:58:43
12	contradicting anything in Takahara, I think most	14:58:55
13	of those would be considered input terminals.	14:59:01
14	Q Okay. Let's go back to Figure 3, please.	14:59:06
15	Okay. So we have the short-circuit wiring 91, the	14:59:15
16	input terminals 800 through 802, and then there's	14:59:20
17	a wiring line 72 or 73. I believe Takahara	14:59:28
18	identifies 72 and 73 as signal wirings; is that	14:59:36
19	right?	14:59:56
20	A In the written description, Takahara says	14:59:56
21	signal wiring 72 and 73.	15:00:05
22	Q Then to the right of the 72 or 73 label in	15:00:08

1	Figure 3, we have protection resistor 66, right?	15:00:13
2	A Yep.	15:00:23
3	Q And then moving to the right, we get to 67	15:00:23
4	and 68 which are a P-channel TFT and N-channel TFT	15:00:27
5	that are configured in a push-pull layout that	15:00:37
6	constitutes a diode between positive power	15:00:41
7	supplies VDD and negative power supplies VSS	15:00:45
8	respectively; is that accurate?	15:00:49
9	A Yeah.	15:00:51
10	Q For Takahara?	15:00:52
11	A I think that you're reading from 66 and I	15:00:52
12	can see that passage, so I think you're right	15:00:57
13	there.	15:01:00
14	Q And then we have -- then Figure 3 shows	15:01:00
15	drive circuit 60 or 70. And is it your	15:01:05
16	understanding that those drive circuits as shown	15:01:10
17	in Figure 3 correspond to the scan line drive	15:01:12
18	circuit -- circuits for the data line drive	15:01:17
19	circuit as shown in Figure 1?	15:01:21
20	A At least a portion thereof.	15:01:24
21	Q So I'm just going to read from	15:01:43
22	paragraph -- paragraph 66 in the written	15:02:00

1 description. The way Takahara describes this 15:02:02
2 protection circuit block diagram as functioning is 15:02:07
3 that static electricity entering from the terminal 15:02:11
4 800, 801, 802 or the first short-circuit wiring 91 15:02:16
5 does not reach the data line drive circuit 101 and 15:02:19
6 the scan line drive circuit 104 unless it passes 15:02:23
7 through the protection resistor 66 and the 15:02:26
8 electrostatic protection circuit 150 or 151. 15:02:31

9 Did I get that right? 15:02:35

10 A Yeah. I think you read that correctly. 15:02:36

11 Q So the -- in Figure 3, the signal wirings 15:02:38
12 identified as 70 or 73, that is the wiring that is 15:02:50
13 connected to the driving circuit and it's also the 15:02:54
14 wiring that the electrostatic protection circuits 15:03:00
15 150 or 151 are on in order to protect the drive 15:03:03
16 circuit from charges that could travel down the 15:03:11
17 signal wire 72 or 73, agreed? 15:03:15

18 A I'm sorry, you have to break that down a 15:03:19
19 little bit in smaller pieces for me so I can 15:03:27
20 follow along. 15:03:29

21 Q Okay. Let's start with signal wiring 72 15:03:30
22 or 73 is shown in Figure 3 are signal wirings that 15:03:34

1	are connected to the scan line and/or data line	15:03:39
2	drive circuit which is -- which is identified as	15:03:48
3	60 or 70 in Figure 3?	15:03:52
4	A Yes. I can see that.	15:03:57
5	Q And the electrostatic protection circuit	15:04:03
6	specifically 67 and 68, they're located -- is	15:04:12
7	located on the signal wiring, 72 or 73 that is	15:04:16
8	connected to a driving circuit?	15:04:23
9	A Yeah. I mean, you can see that the label	15:04:32
10	for 72 or 73 is on the left side of that resistor	15:05:06
11	but the general connection there does go to the	15:05:10
12	drive circuit which is labeled 60 or 70.	15:05:16
13	Q So TFT 67 and 68 as shown in Figure 3,	15:05:33
14	those together function to protect the drive	15:05:43
15	circuit shown in Figure 3 from static electricity	15:05:49
16	that could enter the terminal and travel down the	15:05:54
17	signal wiring 72 or 73 that would otherwise enter	15:05:58
18	the drive circuit?	15:06:03
19	A Are you asking a question there?	15:06:29
20	Q Yeah. I guess, do you -- do you agree	15:06:31
21	with my statement?	15:06:41
22	A The specific functionality how the scan	15:06:48

1	line driver circuit specifically protects --	15:06:54
2	Q Let me ask it this way, if you don't	15:07:05
3	mind -- sorry to interrupt you. If you want to	15:07:10
4	continue your answer, please do.	15:07:20
5	A No. I'll give you another shot.	15:07:21
6	Q Okay. Just trying to ask a simple	15:07:23
7	question.	15:07:23
8	The transistor -- the TFT transistor 67	15:07:26
9	and 68 shown in Figure 3 together functioning to	15:07:28
10	protect the drive circuit which is labeled 60 or	15:07:32
11	70 in Figure 3 from charge -- static electricity	15:07:34
12	that could enter the terminal and travel along the	15:07:38
13	signal wirings 72 or 73, or static electricity	15:07:43
14	that could enter short-circuit wiring 91; is	15:07:51
15	that -- do you agree with that?	15:07:57
16	A That's one way it could function, yes.	15:07:59
17	Q So the TFT 67 and 68 also show -- or show	15:08:11
18	a connection -- let me ask it this way: 67 -- TFT	15:08:17
19	67 in Figure 3 is connected to positive power	15:08:28
20	supply VDD, right?	15:08:36
21	A Yes. That's what I'm seeing here at	15:08:39
22	Figure 3.	15:08:42

1	Q And then TFT 68 is connected to negative	15:08:43
2	power supply VSS?	15:08:47
3	A Yes. That's how it's depicted here.	15:08:50
4	Q The VSS and VDD power supply lines that	15:08:52
5	are connected to TFT 68 and 67 respectively are	15:09:01
6	not power lines that are supplying power to the	15:09:11
7	drive circuit shown in Figure 3, correct?	15:09:14
8	A Can you ask that last part one more time?	15:09:25
9	Q Yeah. The VDD and VSS power supply lines	15:09:28
10	that are connected to TFT 67 and TFT 68	15:09:39
11	respectively shown in Figure 3, those are not the	15:09:45
12	power supplies that are connected to the drive	15:09:51
13	circuit to provide power to the drive circuit; is	15:09:55
14	that right?	15:10:23
15	A A connection to VDD and VSS is not	15:10:23
16	explicitly shown in Figure 3, we refer to Figure	15:10:44
17	1, you can see that there are power supplies	15:10:49
18	connected to, for instance, the scan line driver	15:10:51
19	circuit that is explicitly shown.	15:10:57
20	Q Yeah. And in Figure 1, the power lines	15:11:08
21	that are shown connected to the scan line drive	15:11:14
22	circuits are labeled VSSY and VDDY, right?	15:11:17

1	A Yes. I can see that shown on Figure 1.	15:11:28
2	Q So turning back to Figure 3 which is still	15:11:36
3	up, do you agree that VDD and VSS are connected to	15:11:39
4	TFT 67 and 68 in order to serve as reference	15:11:46
5	potential lines that limit the voltage on the	15:11:55
6	signal wiring lines 72 or 70 -- let me ask that	15:11:59
7	again.	15:12:03
8	Do you agree that VDD and VSS as shown in	15:12:03
9	Figure 3 are connected to the transistors 68 and	15:12:07
10	67 for the purpose of serving as a reference	15:12:13
11	potential that limits the voltage that will be	15:12:18
12	allowed to travel along signal wiring 72 or 73 and	15:12:24
13	enter the drive circuit?	15:12:29
14	MR. RODKEY: Objection, scope.	15:12:32
15	A That's one of the functions that VDD and	15:12:33
16	VSS are performing here in the context of Figure	15:12:49
17	3. That's one way to describe how that ESD	15:12:52
18	protection works.	15:12:55
19	Q What other functions are -- do VDD and VSS	15:12:58
20	perform in the context of Figure 3?	15:13:08
21	A In Figure 3 here, they're -- those are the	15:13:10
22	only connections that are explicitly shown.	15:13:16

1 Q Can we go back to Figure 1? Figure 1, I
2 want to focus on the scan line drive circuits
3 shown in Figure 1 and then the electrostatic
4 protection circuits 151 that are located on the
5 signal wirings that are connected to the scan line
6 drive circuits.

7 My question is: Do you agree that each of
8 the electrostatic protection circuits 151, which
9 there are four in Figure 1, each is located on a
10 signal wiring that is between the input terminal
11 of the signal wiring and where that signal wiring
12 connects to the scanning line drive circuit?

13 A I apologize. You have to walk me through
14 that just one more time so I can follow along very
15 carefully.

16 Q Sure. Let's start with the signal wirings
17 labeled DY in Figure 1.

18 A Okay.

19 Q So for the scan line drive circuit box
20 shown in Figure 1 that is on the left --

21 A Yeah.

22 Q -- the electrostatic protection circuit

1 151 that is on the DY signal line, that
2 electrostatic that is between the input terminal
3 for DY and where DY enters the scan line driving
4 -- scan line drive circuit; is that right?

5 A Without excluding any other connections,
6 there might be two ESD protection circuit 151, I
7 think it's reasonable to agree that it does fall
8 between the terminal and the scan line drive
9 circuit.

10 Q And would you agree that the same is true
11 for the scan line drive circuit on the right-hand
12 side of Figure 1 with respect to the DY signal
13 line?

14 A Again, without excluding other connections
15 that are apparent and shown there in Takahara
16 Figure 1, like the short lines, 91, you can see
17 that scan line driving, the -- upper right ESD
18 protection circuit 151 is -- you know, can be
19 reasonably described as being between the scan
20 line driving circuit and the terminal for DY which
21 is the lower right corner of Figure 1.

22 Q Okay. And then for the signal wirings

15:16:02

15:16:08

15:16:11

15:16:16

15:16:27

15:16:38

15:16:45

15:16:51

15:16:56

15:16:57

15:17:00

15:17:04

15:17:10

15:17:14

15:17:19

15:17:23

15:17:30

15:17:38

15:17:45

15:17:48

15:17:53

15:17:56

1 labeled CLY with the bar on top, or CLY Bar and
2 CLY, let's start with the scan line drive circuit
3 on the right-hand side of Figure 1.

4 Do you agree that the electrostatic
5 protection circuit 151 that is located below the
6 scan line drive circuit on the right-hand side of
7 Figure 1 is on CLY Bar at CLY between the input
8 terminals and where they enter or connect to the
9 scan line drive circuit?

10 A Similar answer to above. You know, if we
11 caveat that there are other connections made to
12 that lower right ESD protection circuit 151, lower
13 right of scan line driving circuit on the right
14 side of the figure, could be, you know, seen from
15 Figure 1, that among other places it's between the
16 scan line circuit and the terminals if you follow
17 a certain route of connections.

18 Q All right. Then turning to the scan line
19 drive circuit that is on the left-hand side of
20 Figure 1, the electrostatic protection circuit
21 151, below that scan line drive circuit is also
22 located on CLY Bar and CLY between the input

1 terminals on the lower right corner and where CLY
2 Bar and CLY are connected to the scan line drive
3 circuit on the left-hand side of Figure 1.

4 Do you agree with that?

5 A Subject to similar caveats about other
6 connections that are made, for instance the short
7 connections indicated by 91, the upper left area
8 Figure 1, if you trace certain connection routes
9 then I could agree that scan line drive
10 circuit -- I'm sorry, the ESD protection circuit
11 151 underneath the scan line drive circuit on the
12 left-hand of 151 is in particular routings between
13 that scan line drive circuit and the terminals as
14 you've indicated of CLY and CLY Bar.

15 Q So you mentioned the short-circuit wiring
16 91 a few times. I want to ask about -- so
17 there's -- well, there's short-circuit
18 wirings -- let me ask it this way.

19 If we start with the DY terminal at the
20 lower left-hand corner of Figure 1, the
21 electrostatic protection circuit 151 that is on
22 the DY signal line is also between where DY

1 intersects with short-circuit wiring 91 in the 15:22:02
2 lower left corner and where DY connects to the 15:22:06
3 scan line driving circuit; is that right? 15:22:11

4 A Again, subject to other connections that 15:22:15
5 might be present, I do see that the scan line -- 15:22:23
6 the ESD protection circuit 151 above the left scan 15:22:28
7 line driving circuit following a certain signal 15:22:33
8 right is between the scan line drive circuit and 15:22:38
9 item 91 on the lower left area of Figure 1 of 15:22:42
10 Takahara. 15:22:48

11 Q You mentioned in your answers subject to 15:22:51
12 other connections that might be present, what are 15:22:53
13 you -- what other connections are you referring to 15:22:58
14 that might be present? 15:23:00

15 A I think I gave some examples of these 15:23:07
16 short connections that connect different of these 15:23:11
17 wires that are depicted on Figure 1 to others. 15:23:17
18 And so there are a multitude of routes that one 15:23:24
19 would have to consider to answer the questions 15:23:31
20 that you're asking about whether a certain 15:23:34
21 component is between other components. So just 15:23:37
22 trying to be as complete in my answers as 15:23:41

1 possible.

15:23:44

2 Q Can you give me an example of other routes
3 that one would have to consider to answer my
4 questions for signal line DY on the lower left
5 corner and how it connects to the scan line drive
6 circuit on the left and then whether electrostatic
7 protection circuit 151 located on the upper right
8 above the left-hand side scan line drive circuit
9 is connected between the terminal -- the DY
10 terminal?

15:24:25

15:24:30

15:24:33

15:24:40

15:24:48

15:24:56

15:25:00

15:25:02

15:25:08

11 A So for instance, in my declaration at page
12 145 paragraph 235, there's an annotated figure.
13 If I were to be asked if scan line -- excuse me,
14 if I were to be asked if ESD protection circuit
15 151 is between certain other elements, I could
16 draw an annotation such as shown in red where the
17 scan line -- sorry, where the ESD protection
18 circuit on the upper left 151 is connected between
19 the scan line drive circuit on the left-hand
20 terminal for VSS, the power -- a power supply
21 terminal. That's, you know, through one of the
22 short lines identified by number 91 in Takahara.

15:25:09

15:25:36

15:25:42

15:25:46

15:25:59

15:26:03

15:26:06

15:26:08

15:26:15

15:26:19

15:26:24

15:26:29

1 In any case, it's clear that the scan line
2 driving circuit is explicitly shown to be
3 protected here in Takahara. A person of ordinary
4 skill in the art would be motivated to apply this
5 teaching, if it couldn't be found in Takahara, to
6 teaching of Reiner.

7 Q Dr. Murphy, which -- which -- which figure
8 were you referring to in your declaration? Which
9 paragraph is that under?

10 A Yes. Paragraph 235.

11 Q 235, okay.

12 A If you were to go to page 145, the
13 declaration, it's the one I'm looking at.

14 Q On the answer you just gave, are you
15 saying it's your opinion that VSSY is connected to
16 the scan line drive circuit on the left and runs
17 through the electrostatic protection circuit 151
18 on the upper left because VSSY is connected to
19 signal line DY by short-circuit wiring 91 on the
20 lower left of Figure 1?

21 A That's a fair summary of what Takahara
22 shows and I've annotated Figure 1 to emphasize

1	something that Takahara shows.	15:29:29
2	MR. JONES: Let's go off the record for a	15:29:45
3	quick break. I should be able to wrap up shortly	15:29:47
4	thereafter.	15:29:50
5	THE VIDEOGRAPHER: We are going off the	15:29:51
6	record. The time is 3:29 p.m.	15:29:53
7	(Whereupon a break was had.)	15:32:38
8	THE VIDEOGRAPHER: We are going back on	15:46:31
9	the record. The time is 3:46 p.m.	15:46:38
10	MR. JONES: Could we mark as Exhibit 2006	15:46:42
11	the file with the -- the image file with file name	15:46:59
12	BOETech_00040165? I'll also put it through the	15:47:06
13	chat.	15:47:13
14	(Exhibit 2006 marked for identification.)	15:47:13
15	MR. RODKEY: Counsel, I need to make sure	15:47:35
16	I get this. I am going to object to this both	15:47:37
17	relevance; scope; potentially confidential	15:47:42
18	information used outside of the district court	15:47:45
19	proceeding; and potentially in violation of that	15:47:48
20	protective order.	15:47:57
21	MR. JONES: I can represent to you that	15:47:57
22	this is not confidential information.	15:47:59

1 MR. RODKEY: I am still going to object on
2 relevance and scope; also incomplete.

3 Q Dr. Murphy, do you see Exhibit 2006 in
4 front of you?

5 A Yes. I can see it here on the Zoom.

6 Q Have you seen this image before?

7 A Not to my recollection, no.

8 Q Do you recognize that this is an image
9 from a tear-down of an LCD panel?

10 MR. RODKEY: Objection, relevance; scope.

11 A I'm familiar enough with what an image
12 like that could look like, and so it may very well
13 be what you're describing.

14 Q I'm going to annotate Exhibit 2006 with a
15 box. Dr. Murphy, do you see the annotations in
16 red I've made to Exhibit 2006?

17 MR. RODKEY: I'm going to object on
18 relevance; scope; and incomplete hypothetical.

19 Counsel, this isn't in any way related to
20 his declaration on the IPR.

21 A To answer the question, I can see a red
22 annotation here on the screen. Yeah.

1	Q Can you identify the circuit that is in	15:49:54
2	the red box I drew?	15:50:01
3	MR. RODKEY: Again, objection; relevance,	15:50:03
4	scope; incomplete hypothetical.	15:50:05
5	Counsel, this is completely outside and	15:50:09
6	improper for the scope of an IPR deposition.	15:50:12
7	MR. JONES: Counsel, objection is noted.	15:50:15
8	I'm still going to ask my question unless you	15:50:16
9	instruct the witness not to answer.	15:50:19
10	MR. RODKEY: I'm going to maintain mine	15:50:23
11	on relevance and scope, and the fact he's not seen	15:50:25
12	this before and it's unfair to make him opine on	15:50:29
13	it.	15:50:35
14	A Just having seen the document, I couldn't	15:50:38
15	tell you what that's -- what kind of circuit that	15:50:40
16	might be, you know, given the understanding that	15:50:49
17	it's probably a circuit of some kind, given the	15:50:50
18	understanding that it's -- appears to me to be	15:50:54
19	something like what you'd expect to see of a	15:50:57
20	tear-down or a -- of a display device.	15:51:05
21	Q What other information would you need to	15:51:07
22	identify the circuit I've outlined with the red	15:51:14

1	box?	15:51:19
2	MR. RODKEY: Objection on relevance;	15:51:19
3	scope; incomplete hypothetical; speculation. This	15:51:20
4	is completely outside -- if you can tie it back to	15:51:23
5	his declaration somehow he can answer your	15:51:27
6	questions. Otherwise, I'm going to instruct him	15:51:30
7	not to answer.	15:51:32
8	A I would need an awful lot of additional	15:51:43
9	info to -- to start any analysis of this.	15:51:47
10	Q Can you give me some examples of the types	15:52:02
11	of additional information?	15:52:04
12	MR. RODKEY: Objection, relevance; scope;	15:52:05
13	incomplete hypothetical; speculation; completely	15:52:07
14	outside the scope of the declaration; improper for	15:52:09
15	an IPR deposition.	15:52:11
16	You don't have to answer this question	15:52:13
17	unless he ties it back to the IPR.	15:52:15
18	MR. JONES: Counsel, are you instructing	15:52:17
19	the witness not to answer the question?	15:52:19
20	MR. RODKEY: If you can tie it back to his	15:52:21
21	IPR declaration and turn this into a proper	15:52:22
22	question, he can answer. But I'm not going to let	15:52:25

1	you start asking questions about a district court	15:52:30
2	case on the record in an unrelated proceeding.	15:52:34
3	Because this appears to be a document produced in	15:52:44
4	district court given the BOE Bates number that	15:52:46
5	you've given. So tie it back to his declaration	15:52:46
6	or he doesn't have to answer.	15:52:49
7	MR. JONES: Are you objecting on the basis	15:52:52
8	of privilege?	15:52:54
9	MR. RODKEY: The scope and ask him to	15:52:56
10	opine on something unrelated to the invalidity	15:53:01
11	opinions that he's given in this proceeding. How	15:53:04
12	does this relate to the invalidity of the '157	15:53:10
13	patent based on Reiner and Takahara?	15:53:14
14	MR. JONES: Counsel, if you're going to	15:53:30
15	instruct the witness not to answer these	15:53:31
16	questions, we're going to hold this deposition	15:53:34
17	open. We can conclude it on that basis.	15:53:38
18	MR. RODKEY: You -- I'm asking you, how is	15:53:41
19	this related to his opinions based on Reiner and	15:53:43
20	Takahara to the invalidity of the '157 patent? If	15:53:47
21	you can satisfy that question for me, we can	15:53:51
22	proceed. But this appears to be a document	15:53:53

1 produced in a district court litigation under a 15:53:58
2 BOE Bates number. And I don't see any relevance 15:54:03
3 or how it's related to the scope of his 15:54:04
4 declaration. 15:54:06

5 So if you could please answer those 15:54:07
6 questions, we could figure out how to proceed. 15:54:09
7 But I'm not going to let you ask questions on a 15:54:15
8 district court case to someone who is not involved 15:54:18
9 in that district court case. You already asked 15:54:18
10 whether he was involved in that district court 15:54:22
11 case. He said he was not. He hasn't talked to 15:54:23
12 anyone. And so it's unfair to ask him about that 15:54:26
13 case. 15:54:29

14 MR. JONES: Counsel, first, relevance is 15:54:32
15 not a basis to instruct a witness not to answer. 15:54:34

16 Second, this is relevant to Dr. Murphy's 15:54:37
17 skill in this art. This is an image of an LCD 15:54:43
18 panel. 15:54:48

19 MR. RODKEY: How does it relate to 15:54:50
20 Takahara and Reiner? 15:54:52

21 MR. JONES: Counsel, are you instructing 15:54:54
22 the witness not to answer on the basis of 15:55:09

1 relevance?

15:55:12

2 MR. RODKEY: I'm going to object on
3 relevance, scope, it being completely improper.

15:55:13

15:55:16

4 If you want to ask the Board to force him to
5 answer questions about this, you can consider it
6 or you can ask your questions and he can say "I've
7 never seen this before and I don't have to answer
8 the question because I don't see the relevance."

15:55:21

15:55:24

15:55:27

15:55:31

15:55:34

9 MR. JONES: Are you instructing Dr. Murphy
10 not to answer?

15:55:54

15:55:56

11 MR. RODKEY: Not at this time. But he
12 doesn't have to answer the question on something
13 like this that's clearly a litigation document
14 that's being used improperly in the IPR
15 position -- IPR deposition.

15:55:57

15:55:59

15:56:01

15:56:04

15:56:08

16 MR. JONES: Okay. I'll ask the question
17 again.

15:56:14

15:56:16

18 BY MR. JONES:

15:56:17

19 Q Dr. Murphy, you testified that you can't
20 identify the circuit I outlined in red in
21 Exhibit 2006. What additional information would
22 you need in order to identify the circuit that

15:56:20

15:56:23

15:56:29

15:56:34

1	I -- that I -- within the red box?	15:56:42
2	MR. RODKEY: I'm going to object on scope;	15:56:47
3	relevance; and incomplete hypothetical; this is	15:56:49
4	speculation; it also misstates his prior	15:56:53
5	testimony. It's an improper use of a district	15:56:55
6	court document in the -- in the IPR proceeding.	15:56:59
7	And to the extent the witness has never seen it	15:57:01
8	before, it's -- he doesn't have to answer the	15:57:04
9	question if he doesn't want to.	15:57:06
10	Q Dr. Murphy, are you going to answer the	15:57:29
11	question? Please answer if you can.	15:57:31
12	MR. RODKEY: I'm going to repeat all my	15:57:35
13	objections. And if he chooses to not answer a	15:57:38
14	district court-related question in an IPR	15:57:40
15	proceeding that's unrelated, he can choose not to.	15:57:41
16	A Yeah. I'll repeat my previous answer that	15:57:47
17	there's really a volume of information that I or	15:57:50
18	anyone else might need to analyze the image in	15:57:58
19	front of me. And, you know, hard to identify all	15:58:03
20	the things anyone might need to know without	15:58:10
21	understanding the general scope of what's being	15:58:15
22	asked, the context of the image, and the source of	15:58:18

1 the image.

15:58:33

2 MR. JONES: Counsel, I'll note for the
3 record that your speaking objections are
4 converting to improper witness coaching.

15:58:37

15:58:39

15:58:42

5 Q Dr. Murphy, I'm just looking for examples
6 of additional information that would be helpful.
7 For example, would it be helpful to see a circuit
8 extraction analysis of the LCD circuitry that is
9 shown in this image of the LCD panel?

15:58:44

15:58:47

15:58:50

15:58:53

15:58:59

10 MR. RODKEY: I'm going to continue my
11 objections on incomplete hypothetical;
12 speculation; and improper use of a document from a
13 litigation in an IPR proceeding; relevance;
14 completely outside the scope of anything related
15 to his deposition and his declaration.

15:59:05

15:59:07

15:59:09

15:59:12

15:59:15

15:59:17

16 I appreciate your objection, Counsel, but
17 you're -- this is completely improper and he does
18 not have to answer the question.

15:59:20

15:59:22

15:59:24

19 A To answer the question posed, need to
20 understand a bit more about the hypothetical that
21 was identified, a circuit extraction analysis. I
22 can't say just given that small amount of

15:59:47

15:59:52

15:59:57

16:00:04

1 information to what degree that would be necessary
2 or helpful.

3 Q Can you think of any category of
4 information that would be helpful for you to see
5 in order to analyze the circuit that is outlined
6 in red, the annotation I made to Exhibit 2006?

7 MR. RODKEY: I'm going to continue to
8 object on relevance; scope; and incomplete
9 hypothetical; a district court document that's
10 being used in an IPR proceeding for improper
11 purpose because it's unrelated to his declaration
12 and any opinion that he's provided here, including
13 his only two opinions on Reiner and Takahara. And
14 that I'm actually going to instruct him that
15 you've gone way outside the bounds not to answer
16 the question.

17 MR. JONES: Counsel, I'll note that your
18 instruction to the witness not to answer is
19 improper.

20 Q Dr. Murphy, I understand what you're
21 saying. Is it your testimony that you would need
22 more information to identify this circuit; is that

1	fair?	16:01:45
2	MR. RODKEY: Going to continue to object	16:01:45
3	on relevance; scope; incomplete hypothetical.	16:01:46
4	This document is being used from a district court	16:01:50
5	litigation in an IPR proceeding that is unrelated	16:01:54
6	to anything that he's offered on Reiner and	16:01:56
7	Takahara. You still haven't tied that together,	16:01:59
8	Counsel. And if you can, I will stop making these	16:01:59
9	objections. Again, it's way outside the scope and	16:02:02
10	I'm going to instruct him not to answer unless you	16:02:04
11	can tell me why it's relevant or within the scope.	16:02:08
12	MR. JONES: Counsel, relevance is not a	16:02:41
13	proper basis to instruct the witness not to	16:02:43
14	answer. Are you maintaining that instruction?	16:02:45
15	MR. RODKEY: I am because this is clearly	16:02:48
16	not a proper line of questioning because you have	16:02:50
17	pulled a document from the district court into	16:02:53
18	this proceeding. If you can tell me why it's	16:02:56
19	relevant, how it relates to Reiner or Takahara or	16:02:59
20	any opinion that he's offered, I'll accept that.	16:03:02
21	But you still haven't answered that question for	16:03:05
22	me.	16:03:07

1 Q Dr. Murphy, do you intend to follow your
2 counsel's instructions not to answer?

3 A I've been instructed not to answer and
4 will intend to follow the guidance of counsel on
5 this legal subject, rather than a technical
6 subject.

7 MR. JONES: All right. Patent owner views
8 this deposition still open and we will consider it
9 held open. But otherwise, we can conclude for
10 now.

11 MR. RODKEY: We're not allowing you to
12 hold this one open. You have your seven hours and
13 you can finish it up now.

14 MR. JONES: Counsel --

15 MR. RODKEY: If he chooses not to answer
16 then, that's up to him.

17 MR. JONES: Counsel, my remaining
18 questions are all questions for which you are
19 giving the witness improper instructions not to
20 answer.

21 MR. RODKEY: You haven't asked those
22 questions. I haven't given that instruction. So

1 you can keep going, and if it's an improper
2 question and I need to instruct him not to answer,
3 I will. If it's a proper question, he can answer.

4 MR. JONES: It's these questions I'm
5 asking about the annotations -- annotation I made
6 to Exhibit 2006 and whether Dr. Murphy can
7 identify the circuit within that annotation, and
8 if he can't, what information he would need to do
9 so.

10 MR. RODKEY: You can ask your questions.
11 And if Dr. Murphy chooses to say he doesn't want
12 to answer them because they're not related to his
13 declaration, he can say that too. So you can
14 proceed. I believe you have about nine minutes
15 left.

16 BY MR. JONES:

17 Q Dr. Murphy, is it fair to say that you
18 would need to see additional information in order
19 to identify the circuit that I have outlined in
20 red in Exhibit 2006?

21 MR. RODKEY: Objection, scope; incomplete
22 hypothetical; outside the bounds of a proper IPR

1	deposition because it's a district court document	16:05:57
2	used in litigation; relevance.	16:06:00
3	A Look, I've agreed already that this looks	16:06:16
4	like it could plausibly be a circuit. I have no	16:06:21
5	basis for any additional analysis of what's in	16:06:29
6	front of me and so I really can't answer the	16:06:37
7	question as posed. Not among, you know, the	16:06:43
8	documents I've cited as the basis for my opinions	16:07:01
9	or anything that I can identify as being material	16:07:08
10	that has informed my opinion in the '157 IPR	16:07:14
11	proceeding.	16:07:23
12	MR. JONES: We can take down Exhibit 2006.	16:07:33
13	I have similar questions for another image, if you	16:07:45
14	will bear with me here.	16:07:50
15	MR. RODKEY: While he's doing that, can I	16:07:56
16	get the time left on the record?	16:07:58
17	THE VIDEOGRAPHER: About 14 minutes and	16:08:01
18	30 seconds.	16:08:06
19	MR. JONES: Could we mark as Exhibit 2007,	16:08:08
20	BOETech_00040167.	16:08:18
21	(Exhibit 2007 marked for identification.)	16:08:23
22	MR. JONES: I'll also drop that in the	16:08:33

1 chat. And I'll represent for the record this is 16:08:35
2 public information, not subject to any protective 16:08:47
3 order. 16:08:50

4 MR. RODKEY: Okay. I am going to object 16:08:50
5 to this, again, given that it has a BOE Bates 16:08:52
6 stamp in the bottom right corner, that this is 16:08:56
7 outside the scope of the declaration deposition, 16:08:59
8 and is irrelevant to this proceeding. It is an 16:09:03
9 incomplete hypothetical, given that it is an 16:09:06
10 excerpt and the context is completely off. And I 16:09:09
11 can't necessarily accept your representation given 16:09:16
12 the BOE Bates stamp in the bottom corner. 16:09:18

13 And you know what, tell me why -- and this 16:09:22
14 is not relevant to Takahara or Reiner. And so the 16:09:27
15 witness can choose not to answer if he doesn't 16:09:33
16 want to. 16:09:36

17 MR. JONES: Your objections are noted, 16:09:37
18 Counsel. 16:09:38

19 Q Dr. Murphy, have you seen this image 16:09:40
20 before? 16:09:42

21 MR. RODKEY: Objection, relevance; scope; 16:09:43
22 incomplete hypothetical. He's already testified 16:09:45

1	that he hasn't done anything with the litigation.	16:09:47
2	This is improper use of a litigation document in	16:09:50
3	an IPR proceeding to try to extract litigation	16:09:53
4	testimony. It's outside the scope. And he can	16:09:56
5	choose not to answer.	16:10:01
6	Q Do you intend to answer the question, Dr.	16:10:28
7	Murphy?	16:10:32
8	A Appreciate if you repeat it for the record	16:10:32
9	or for my -- appreciate if you repeat it for my	16:10:34
10	benefit. Thank you.	16:10:41
11	Q Yeah. My question is: Have you seen this	16:10:43
12	image before?	16:10:46
13	MR. RODKEY: Objection, relevance; scope;	16:10:47
14	incomplete hypothetical. He's already testified	16:10:48
15	he hasn't seen anything with the litigation;	16:10:50
16	improper use of litigation document in an IPR	16:10:53
17	proceedings to extract litigation testimony;	16:10:58
18	outside the scope. And he can choose not to	16:11:00
19	answer.	16:11:01
20	MR. JONES: I will, again, note for the	16:11:01
21	record that your speaking objections mount to	16:11:03
22	improper witness coaching.	16:11:06

1	Q Dr. Murphy, please answer the question.	16:11:07
2	MR. RODKEY: I'll have the same	16:11:10
3	objections.	16:11:12
4	A No, not to my recollection have I seen	16:11:13
5	this image here that's in front of me.	16:11:16
6	Q Do you recognize this image as an image	16:11:20
7	from a tear-down of an LCD panel?	16:11:23
8	MR. RODKEY: Objection, scope; assumes	16:11:26
9	facts not in evidence; incomplete hypothetical;	16:11:27
10	improper use of a litigation document to extract	16:11:31
11	litigation testimony in an IPR testimony. He can	16:11:34
12	choose not to answer if he doesn't want to.	16:11:38
13	A Without additional context, I couldn't be	16:11:42
14	certain as to what we're looking at here. It has	16:11:54
15	appearances of potentially a circuit of some kind.	16:12:03
16	But you know, without any context or -- without	16:12:11
17	any context, I can't be certain an answer as	16:12:23
18	to -- as to what we're looking at.	16:12:30
19	THE VIDEOGRAPHER: Just letting Counsel	16:12:35
20	know there's ten minutes remaining.	16:12:37
21	MR. JONES: Thank you, Jesse.	16:12:39
22	Q Dr. Murphy, what kinds of additional	16:12:42

1 information would you want to see to better
2 understand this image?

3 MR. RODKEY: Again, I'm going to object on
4 relevance; scope; assumes facts not in evidence;
5 incomplete hypothetical; improper use of a
6 litigation document to extract testimony in an IPR
7 proceeding. He can choose not to answer if he
8 doesn't want to.

9 Q Dr. Murphy, do you intend to answer my
10 question?

11 A I think I'd have to study the image
12 considerably to be able to start to give an answer
13 to the question that's posed. The image here
14 could be a number of things and going to be very
15 difficult for me to answer your questions.

16 Q All right. Dr. Murphy, we can leave it
17 there.

18 MR. JONES: I have no further questions.
19 Appreciate your time today.

20 MR. RODKEY: Okay. Give me 15 minutes to
21 consider -- give me 10 minutes to consider whether
22 I have any redirect.

16:12:44

16:12:46

16:12:48

16:12:51

16:12:54

16:12:56

16:12:58

16:13:01

16:13:02

16:13:45

16:13:48

16:13:59

16:14:08

16:14:27

16:14:37

16:14:49

16:14:52

16:14:53

16:14:55

16:14:57

16:15:00

16:15:03

1	MR. JONES: Sounds good.	16:15:05
2	THE VIDEOGRAPHER: We are going off the	16:15:07
3	record. The time is 4:15 p.m.	16:15:08
4	(Whereupon a break was had.)	16:15:10
5	THE VIDEOGRAPHER: We are going back on	16:24:05
6	the record. The time is 4:24 p.m.	16:24:09
7	MR. RODKEY: Could I have Exhibit 2004	16:24:11
8	shown on the screen, please? I apologize, 2005.	16:24:16
9	EXAMINATION	16:24:48
10	BY MR. RODKEY:	16:24:48
11	Q Dr. Murphy, do you recall when Counsel	16:24:49
12	engaged in the line-drawing exercise related to	16:24:50
13	Exhibit 5 and Patent Owner's exhibits that are	16:24:54
14	shown on the screen with the red box?	16:24:59
15	A Yes.	16:25:02
16	Q And in your declaration at page 79 and	16:25:02
17	elsewhere, do you recall discussing your various	16:25:07
18	composite figures Figure A, Figure B, and Figure C	16:25:14
19	throughout your declaration?	16:25:18
20	Do you recall discussing those as well?	16:25:19
21	A Yes.	16:25:21
22	Q And in your Figures A, B, and C throughout	16:25:21

1	your declaration, you have drawn a blue b box	16:25:24
2	around the scan line driver units to show the scan	16:25:29
3	line driver circuit, correct?	16:25:32
4	A Yes.	16:25:34
5	Q So the line drawing of what is the scan	16:25:34
6	line driving circuit, what's not the scan line	16:25:38
7	driving circuit is somewhat arbitrary; is that	16:25:41
8	right?	16:25:44
9	A Yes. That's right.	16:25:44
10	Q And even under Counsel's line drawing with	16:25:47
11	the red box done previously, is it your	16:25:51
12	understanding and your opinion that the	16:25:58
13	connections between the ESD circuits and the power	16:26:02
14	lines throughout your declarations Figures A, B,	16:26:07
15	and C would still be considered ESD -- connections	16:26:10
16	between the ESD circuits and the power lines in	16:26:13
17	accordance with the claims of the '157 patent?	16:26:17
18	MR. JONES: Objection, form.	16:26:19
19	A Yes.	16:26:21
20	Q And is it still your opinion that the	16:26:22
21	connections that you have drawn between the ESD	16:26:26
22	circuits and the -- the units, driver unit 70 in	16:26:28

1 Figures A, B, and C in your declaration would 16:26:34
2 still be considered connections between the ESD 16:26:37
3 circuits and the scan line driver circuit in 16:26:40
4 accordance with the claims of the '157 patent 16:26:45
5 under Counsel's arbitrary line drawing with the 16:26:47
6 red box around it? 16:26:51

7 MR. JONES: Objection, form. 16:26:52

8 A Yes. 16:26:53

9 Q And is it still your opinion that the 16:26:54
10 connections you have drawn between the power lines 16:26:56
11 and the units 70 in Figures A, B, and C in your 16:26:58
12 declaration would still be considered connections 16:27:03
13 between the power line and the scan line drive 16:27:06
14 circuit in Figures A, B, and C even under 16:27:09
15 Counsel's drawing of the circuit in the red box? 16:27:15

16 MR. JONES: Objection, form. 16:27:19

17 A Yes. 16:27:20

18 Q And do you recall discussing with Counsel 16:27:22
19 in Reiner Figure 5 ESD1 and ESD2 the protection 16:27:30
20 related to the output unit 70? 16:27:33

21 A Yes. 16:27:36

22 Q Okay. And in Reiner, which is 16:27:36

1 Exhibit 1005 again, for the record, at -- I'm 16:27:41
2 sorry, page 3, lines 7 to 8, it refers to the ESD 16:27:53
3 protection network protecting the inputs and/or 16:28:03
4 outputs of the integrated circuit device to be 16:28:09
5 protected. 16:28:13

6 Do you recall that? 16:28:13

7 A Yes. 16:28:15

8 Q And so ESD1 and ESD2 protect the output 16:28:15
9 units both on line 70 and from the power lines; 16:28:19
10 isn't that correct? 16:28:27

11 A That's correct. 16:28:28

12 Q And this is true even if those ESD1 and 2 16:28:29
13 don't show the exact specific circuitry that 16:28:32
14 comprises ESD1 and ESD2? 16:28:35

15 A That's correct. Yes. 16:28:37

16 Q All right. Do you recall discussing in 16:28:38
17 Figure 5 with Counsel the low ohmic or bold lines 16:28:45
18 in Figure 5 of Reiner? 16:28:49

19 A Yes. 16:28:51

20 MR. JONES: Objection, form. 16:28:52

21 A I remember that topic. 16:28:52

22 Q And regardless of which lines are bold or 16:28:54

1	low ohmic, Reiner says that ESD1, ESD2, and ESD3	16:28:57
2	protect the driver unit 70, correct?	16:29:01
3	A Yes. That's correct.	16:29:04
4	Q And thus protect the scan line driver	16:29:05
5	circuit, at least it's obvious to protect the scan	16:29:07
6	line driver circuit, correct?	16:29:10
7	A Yes.	16:29:12
8	MR. JONES: Objection, form.	16:29:13
9	Q And so in your opinion, would the claims	16:29:15
10	still be invalid regardless of which lines are	16:29:18
11	bold based on the stated function of ESD1, ESD2,	16:29:21
12	and ESD3 to protect the driver unit 70 in Reiner?	16:29:26
13	MR. JONES: Object -- objection, form.	16:29:30
14	A Yes.	16:29:33
15	Q And return to the previous topic about	16:29:33
16	Counsel's drawing the red box around Figure 5.	16:29:36
17	Even with that red box being drawn as Counsel has	16:29:40
18	annotated, is it still your opinion that the	16:29:44
19	claims would still be invalid under Reiner or the	16:29:46
20	combination of Reiner and Takahara?	16:29:50
21	MR. JONES: Objection, form.	16:29:52
22	A Yes.	16:29:53

1 Q And that's -- and both of those are true 16:29:54
2 of all claims as stated in your opinion? 16:29:57

3 A Yes. That's correct. 16:30:00

4 MR. JONES: Objection, form. 16:30:00

5 MR. RODKEY: No further questions. 16:30:01

6 MR. JONES: No redirect. 16:30:08

7 THE VIDEOGRAPHER: This marks the end of 16:30:13
8 the deposition of Patrick Murphy. The time on the 16:30:17
9 monitor is 4:30 p.m. 16:30:20

10 THE REPORTER: Mr. Rodkey, I don't believe
11 I have standing orders for you.

12 MR. RODKEY: For right now we don't need
13 either a rough or a final or the exhibits. Let me
14 confer with my team and if we need them we'll put
15 the order in separately.

16 (Off-the-record discussion.)

17 THE REPORTER: Mr. Rodkey, a realtime
18 hookup is an automatic transcript order.

19 MR. RODKEY: Oh, okay. Well then we'll
20 just get the regular, just nothing else.

21 (Whereupon the proceedings were concluded

22 at 4:33 p.m. CST)

1 CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

2 I, Karisa Ekenseair, Certified Reporter and
3 Notary Public within and for the State of Arkansas
4 do hereby certify: That PATRICK MURPHY, PHD,
5 the witness whose deposition is hereinbefore set
6 forth, was duly sworn by me before the
7 commencement of such deposition and that such
8 deposition was taken before me and is a true
9 record of the testimony given by such witness.

10 I further certify that the adverse party,
11 Petitioner, was represented by counsel at
12 the deposition.

13 I further certify that the deposition of
14 PATRICK MURPHY, PHD, occurred virtually on
15 March 7, 2025, commencing at 8:05 a.m. to 4:33
16 p.m. CST.

17 I further certify that I am not related to any
18 of the parties to this action by blood
19 or marriage, I am not employed by or an attorney
20 to any of the parties to this action, and that I
21 am in no way interested, financially or otherwise,
22 in the outcome of this matter.

My commission expires: 6-18-2028

Karen J. L.

Karisa Ekenseair, CCR RPR RMR

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