

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2024-00973
U.S. Patent No. 9,184,157

**DECLARATION OF E. FRED SCHUBERT, PH.D., IN SUPPORT OF
PATENT OWNER'S RESPONSE**

I, E. Fred Schubert, of Troy, New York, declare that:

I. ASSIGNMENT

1. I have been retained by Robins Kaplan LLP on behalf of 138 East LCD Advancements Ltd. (“138 East”) as an expert with regard to this matter. I understand that Petitioner BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”) requested that the Patent Trial and Appeal Board (“Board”) institute *inter partes* review (IPR) of U.S. Pat. No. 9,184,157 (“the ’157 patent”) (Ex. 1001). I understand that the Board instituted review, and I have reviewed the Institution Decision. I submit this declaration in support of Patent Owner’s Response to the Petition.

2. In my capacity as an expert, I have been asked to provide my independent analysis and opinions regarding the ’157 patent, the prosecution history of the ’157 patent and related applications as applicable, the alleged prior art relied upon by Petitioner, the meaning of various claim terms from the ’157 patent from the perspective of a person of ordinary skill in the art (“POSITA”), and the opinions offered by Petitioner’s expert, Patrick Murphy, Ph.D., in his declaration (“Murphy Declaration”) (Ex. 1003). My opinions and conclusions are fully discussed in later sections of this declaration.

3. I am an independent consultant, and I am not, and have never been, an employee of 138 East or BOE. I received no compensation for this declaration

beyond my normal hourly compensation (\$600) based on my time spent analyzing the '157 patent, the prosecution history of the '157 patent and related applications, the prior art publications relied upon by Petitioner, the Murphy Declaration, and other related materials. I will not receive any added compensation based on the outcome of any IPR or other proceedings involving the '157 patent.

4. This declaration and my opinions are in support of Patent Owner's Response, and I understand that the content of this declaration may be expressed and reproduced in the POR.

II. BACKGROUND AND QUALIFICATIONS

5. I am currently an active, tenured, full professor in the Department for Electrical, Computer, and Systems Engineering at the Rensselaer Polytechnic Institute (RPI) located in Troy, New York.

6. I also held other positions at RPI. For example, from 2002 to 2012, I was a professor in the Department of Physics, Applied Physics, and Astronomy. In 2008-2009, I served as the founding director for RPI's Engineering Research Center for Smart Lighting, which was funded by the U.S. National Science Foundation (NSF).

7. Before I moved to RPI, I was a professor in the Department of Electrical and Computer Engineering at Boston University, from 1995 to 2002. I

also served as the director of Boston University's Semiconductor Devices Research Laboratory.

8. Prior to my university career, I was a post-doctoral member of the technical staff, member of the technical staff, principal investigator, and member of management at AT&T Bell Laboratories in Holmdel and Murray Hill, New Jersey, from 1985 to 1995.

9. I earned my Ph.D. in 1986, Master of Science in 1981, and Bachelor's degree in 1978, all in Electrical Engineering, at the University of Stuttgart, Germany.

10. My Curriculum Vitae ("CV") is attached as **Appendix A**. As shown by my CV, I have substantial experience in the design and implementation of flat panel display devices, including the design, fabrication, processing, and packaging of the components that are commonly used in liquid crystal displays (LCDs) and light emitting diode (LED) displays.

11. I have published over 300 technical articles, mostly at competitive technical conferences and rigorously refereed technical journals. These articles relate to Liquid Crystal Displays (LCDs), LEDs, semiconductor electronics (e.g., field-effect transistors and bipolar junction transistors), semiconductor lasers, and photo-detectors, that is, the technologies which form the foundations of flat panel displays.

12. As an example of my research activities in the field of LCDs, I refer to a U.S. patent issued in 2012: Jaehee Cho, E. Fred Schubert, and Xing Yan “Liquid crystal display with refractive index matched electrodes” US Patent No. 8,164,727; filed on April 28, 2010; issued on April 24, 2012. During my tenure in industry (AT&T Bell Laboratories), I was part of a working group on LCDs. I have also performed technical consulting services in the field of LCDs and associated TFTs (thin film transistors). One project concerned the enhancement of the carrier mobility in amorphous silicon TFTs. At my university (RPI), I regularly teach courses on microelectronic devices and displays, including TFTs and LCDs. Light emitting diodes are routinely used as a back lighting source for LCDs, and I have worked on and developed LEDs for backlighting units.

13. I am also the author or editor of several books. For example, I authored the textbook “Light-Emitting Diodes,” (1st, 2nd, 3rd, and 4th editions) initially published by Cambridge University Press, Cambridge, UK, with the later editions published on Google Books. In the LED book, I provide a comprehensive review of the state-of-art technologies for designing, fabricating, processing, and manufacturing LEDs, all of which are relevant to LCDs, specifically the associated back-lighting units.

14. In addition to my research, I have been teaching for more than 25 years. I have taught numerous undergraduate and advanced graduate courses in

integrated optoelectronics, microelectronics technology, solid-state devices, semiconductor devices, display devices, and light-emitting diodes, all pertinent to the subject matter in the present case. I have also advised close to 50 Ph.D. and M.S. students while at the RPI and Boston University, in areas such as LEDs, semiconductor electronics, semiconductor lasers, and solar cells.

15. I am the co-inventor of more than 35 issued U.S. patents and associated foreign patents. I was identified as one of the top 1% inventors in the field of optoelectronics, in a 2011 study conducted by Professor Erica Fuchs of Carnegie Mellon University under the support of NSF. Examples of my issued U.S. patents include:

- U.S. Patent No. 7,560,746; issued on July 14, 2009, titled “Light emitting diodes and display apparatuses using the same.”
- U.S. Patent No. 8,164,727, issued on April 24, 2012, titled “Liquid crystal display with refractive index matched electrodes.”

16. I have been actively involved in multiple technical societies, including the American Physical Society (APS), Institute of Electrical and Electronics Engineers (IEEE), Optical Society of America (OSA), Society for Optical Engineering (SPIE). I have served in the organizing committee of multiple technical conferences, including, for example:

- Program committee member and chair of “Display and Solid-State

Lighting Devices” conference for OSA/IEEE Conference on Lasers and Electro-Optics (CLEO), 2003 – 2005.

- Member of the International Advisory Committee of First International Conference on Display LEDs (ICDL), Seoul, Korea, January 31 – February 2, 2007.
- Sub-Committee Chair of Track 6: Displays, Solid-State Lighting, Photovoltaics, and Energy-Efficient Photonics of Asia Communications and Photonics Conference (ACP), Shanghai, China, November 11 – 14, 2014. ACP is the largest and the most influential conference in Asia and Pacific Rim for communications and photonics technologies.

17. My research has been recognized by multiple organizations, universities, and institutions. The following list includes examples of honors that I have received:

- Elected Fellow of the IEEE in 1999. According to the IEEE definition, “the grade of Fellow is one of unusual professional distinction conferred by the Board of Directors only upon a person of extraordinary qualifications and experience.”
- Elected Fellow of the SPIE in 1999. According to the Society’s bylaws, a Fellow “shall be distinguished through his achievements and shall have made outstanding contributions in the field of optics, or optoelectronics,

or in a related scientific, technical, or engineering field.”

- Elected Fellow of the OSA in 2001. OSA Fellows are elected by the OSA Board of Directors.
- Elected Fellow of the APS in 2001.
- Honored with RPI Medal as Senior Constellation Chair in 2002.
- Recipient of “Scientific American 50 Award” of 2007, as published in the January 2008 issue of Scientific American.
- Received “Rensselaer Polytechnic Institute Trustee Faculty Achievement Award” in 2002, 2008, and 2012.

18. My qualifications and accomplishments are further detailed in my CV, submitted as Appendix A.

III. LEVEL OF SKILL IN THE ART AND BASIS FOR OPINIONS

19. Dr. Murphy contends that a POSITA in the field of the '157 patent would have “at least a four-year undergraduate degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional education could substitute for professional experience and vice versa. For example, a master’s degree in electrical engineering, computer science, physics, or a similar field can be a substitute for two years of experience designing semiconductor

display devices.” I understand that Petitioner has adopted that definition of a POSITA. Ex. 1002, ¶97; Petition at 26.

20. In my opinion, a bachelor’s degree recipient with two years of experience or a master’s degree recipient (in electrical engineering, computer science, physics, or a similar field) with no experience in the field of semiconductor display devices at all, who, according to Petitioner, qualifies as a POSITA, has relatively low skills in the relevant field. A master’s degree recipient with no experience in the display field would have difficulties understanding the complex issues governing the design, manufacturing, and operation of LCDs.

21. In my opinion, a person of ordinary skill in the art (“POSITA”) as of the priority date of the ’157 patent would have had at least a bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least four years of experience designing semiconductor display devices, including LCD displays; a master’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays; or a Ph.D. in electrical engineering, computer science, physics, or a similar field and at least one year of experience designing semiconductor display devices, including LCD displays.

22. Based on my experience, I am qualified to render opinions regarding the technology claimed and described in the ’157 patent. Based on my expertise

and qualifications, I am qualified to provide an opinion as to what a POSITA would have understood, known, or concluded as of approximately 2004.

23. In reaching my opinions and conclusions, I have relied upon my education, my work experience in the relevant field, and my training, and considered and relied upon my review and analysis of the Petition and its exhibits.

IV. RELEVANT LEGAL PRINCIPLES

24. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. I have applied these legal principles in rendering my opinions below.

A. Claim Construction

25. I understand that the ordinary and customary meaning of a claim term is the meaning that the term would have to a POSITA at the time of the invention.

26. In the absence of an express intent on the part of the inventor to give a special meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings in light of the relevant patent attributed to them by a POSITA.

27. I understand that it is the use of the words in the context of the written description, and as customarily used by those skilled in the relevant art, that accurately reflects both the ordinary and the customary meaning of the terms in the claims.

28. I understand that the basis for a term's ordinary and customary meaning may be derived from a variety of sources, including the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art at the time of the invention.

29. I have been instructed that dictionary definitions or definitions from technical references can be used to inform or confirm the ordinary and customary meaning of words found in a claim, but that in construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in the context of the claim itself.

30. I understand that a patent applicant is entitled to be his or her own lexicographer (in other words, provide his or her own meaning to a word or phrase) and may rebut the presumption that claim terms are to be given their plain and ordinary meaning. To do so, the applicant must clearly set forth a definition of the term that is different from its ordinary and customary meaning. Where the applicant provides an explicit definition for a term, that definition will control interpretation of the term as it is used in the claim in which it appears. I understand that the specification can also be relied on for more than just explicit lexicography to determine the meaning of a claim term. For example, I understand that the

meaning of a particular claim term may also be determined by implication, that is, according to the usage of the term in the context of the specification.

B. Obviousness

31. I understand that under U.S. patent law, 35 U.S.C. § 103, a claim is invalid as obvious if the differences sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

32. I am informed that an obviousness analysis requires an assessment of the scope and content of the prior art, the differences between the art and the claims at issue, and the level of ordinary skill in the art. I am told that it is against this backdrop that obviousness is assessed.

33. I am informed that a POSITA is a hypothetical person who is presumed to be aware of all the pertinent prior art. I am also informed that an obviousness analysis may take account of the inferences and creative steps that a POSITA would employ.

V. BACKGROUND OF THE '157 PATENT

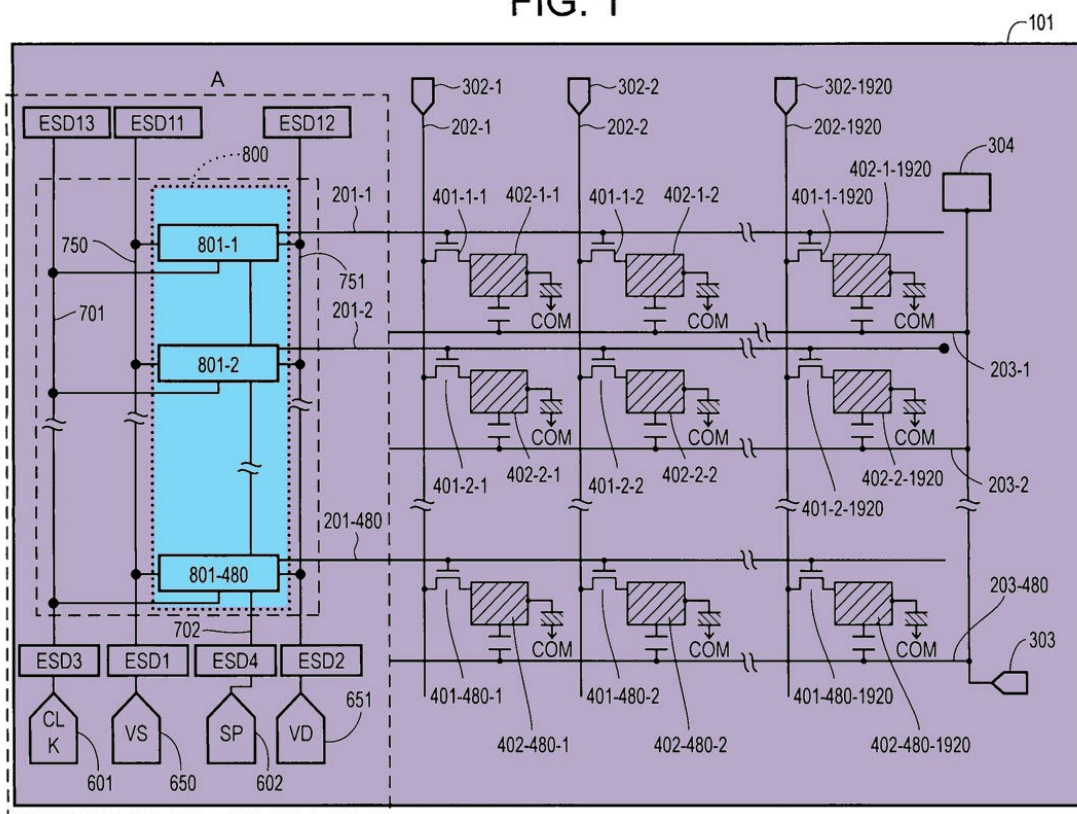
A. '157 Patent Overview

34. The '157 patent, titled "Semiconductor Device, Display Device, and Electronic Apparatus," describes a "semiconductor device, display device and

electronic apparatus” with improved measures to protect display circuitry from electrostatic damage (“ESD”) when a high voltage caused by static electricity or “various noise phenomenon” is “unintentionally applied to the inside of the device.” Ex. 1001, 1:10-16.

35. The ’157 patent’s improved ESD protection measures are specifically directed to “a display device having a driving circuit provided on an active matrix substrate.” *Id.*, 1:10-13. The driving circuit “in the scope of the claims” is a scanning line driving circuit that is “formed by integrating polysilicon thin film transistors [TFTs] on the active matrix substrate.” *Id.*, 5:20-28. A display device where the driving circuit is formed directly on the active matrix display substrate (“TFT driving circuit”) is different from a display device in which the driving circuit is a “general semiconductor device”—an integrated circuit formed on a silicon wafer. In a display device with a TFT driving circuit, the driving circuit is formed as part of the active matrix substrate in which the TFTs that control each pixel of, for example, an LCD display are formed. For example, Fig. 1 shows a scanning line driving circuit 800 formed on the active matrix substrate 101, which supplies a driving signal to scan lines 201, which are connected to pixel switching elements 401:

FIG. 1

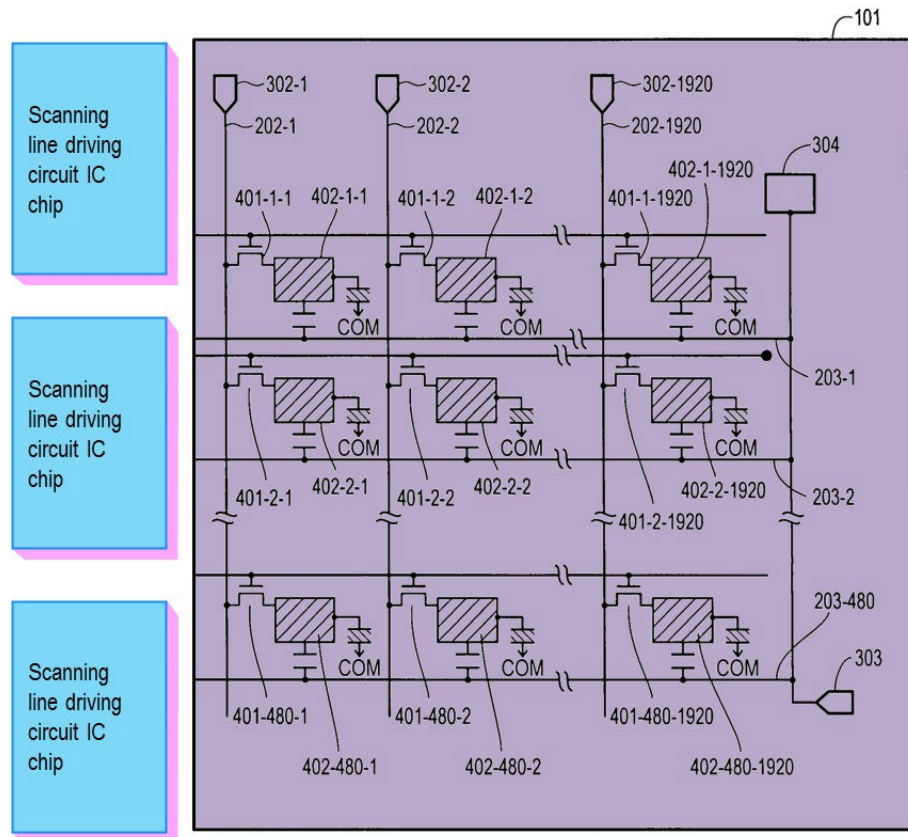


Id., Fig. 1.¹

36. In a display device where the scanning line driving circuit is not a TFT driving circuit, the scanning line driving circuitry exists in a discrete integrated circuit chip ("IC chip"), or multiple IC chips, and the driving circuitry of each IC chip is formed on a silicon substrate. In this type of display device, the silicon substrate of the driving circuit IC chips is different from the display substrate, typically a glass substrate, on which the pixel electrodes and associated transistors (TFTs), and the data and scan lines, are formed. The following exemplar

¹ All colors and colored annotations added to Figures unless otherwise noted.

figure based on Figure 1 of the '157 patent shows such a display device with three scanning line driving circuit IC chips that are formed on a silicon substrates separate from the display substrate (typically a glass substrate) on which the pixel electrodes and transistors (TFTs), scan and data lines, etc., are formed.

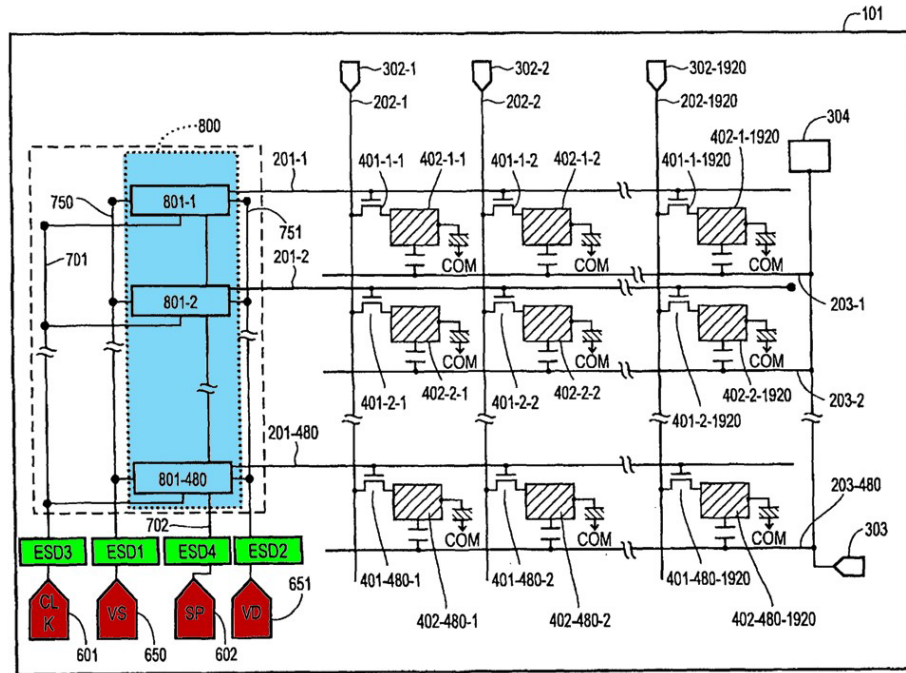


37. Regarding ESD protection, the '157 patent explains that for “general semiconductor devices” formed on a silicon wafer there is “little chance[]” of an ESD event occurring within the IC chip semiconductor device because the silicon wafer is conductive. Ex. 1001, 1:23-28. The “key issue to prevent” ESD events in an IC chip semiconductor device formed on a silicon wafer is therefore to prevent

high voltage from entering the device via its input terminals. *Id.* The conventional solution to prevent high voltage from entering the semiconductor device and thus ESD damage inside the device is to place protective circuits between the input terminals and the semiconductor device. *Id.*, 1:28-32. By contrast, the '157 patent explains that a display device where the active matrix circuitry is formed directly on the display substrate (typically glass) is subject to different ESD problems because, unlike semiconductor devices formed on silicon (IC chips), the semiconductor device is formed on an insulating substrate. *Id.*, 1:33-39. Due to the insulating substrate, ESD damage to the internal circuitry is more likely because static electricity can easily occur during the manufacturing process, and it is more difficult for such charges to escape as compared to a semiconductor device formed on a silicon wafer. *Id.*, 1:33-39, 2:33-35.

38. The '157 patent explains that the conventional solution to protect display devices with a TFT driving circuit from ESD damage uses the same method used to protect IC chips: “only protective circuits for preventing the static electricity from [entering via] the input terminals are built in” to protect the active matrix circuit from ESD damage. *Id.*, 1:47-54, 2:20-30. Figure 11 shows protecting a **scanning line driving circuit 800**, comprising **protection circuits ESD1 to ESD4** placed between the **input terminals 601, 602, 650, and 651** and the

scanning line driving circuit 800 to protect the scanning line driving circuit from static charges entering via the input terminals:



Id., Fig. 11.

39. The '157 patent explains that because the driving circuit is formed on an insulating substrate, “it is difficult for charges to escape as compared to the circuit on [a] silicon wafer, and it is easy to be electrified.” *Id.*, 2:33-50.

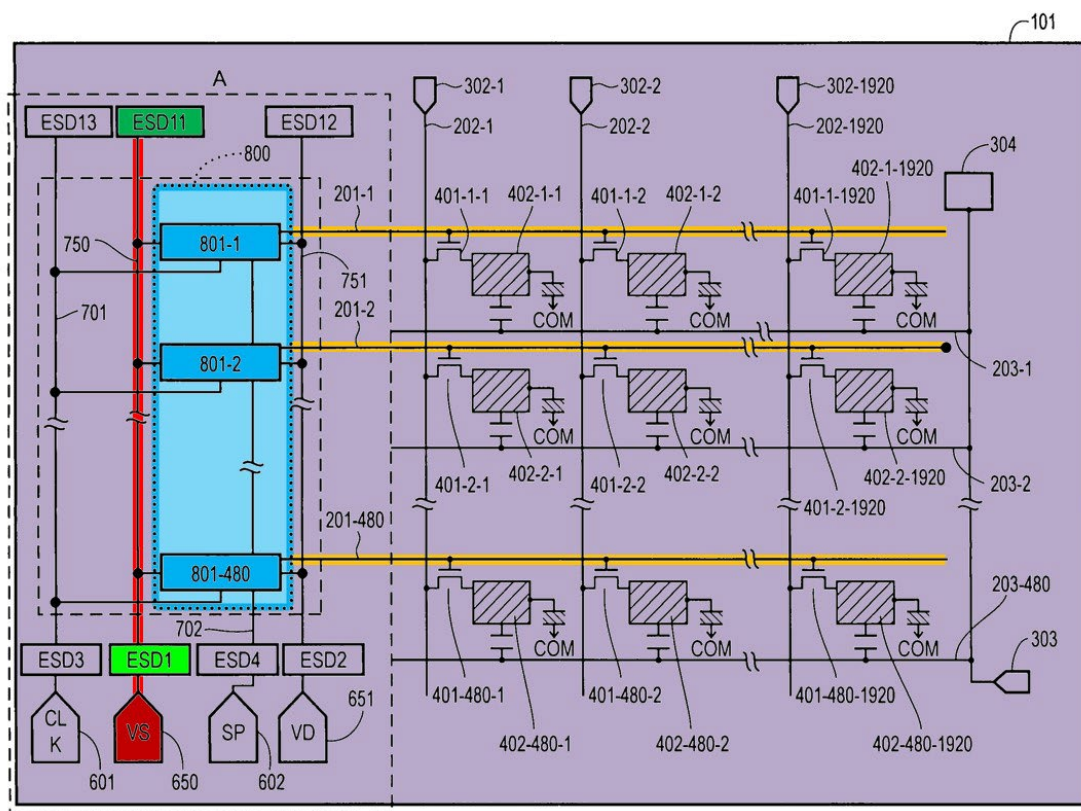
Furthermore, because “the area of [TFT driving circuit] is larger as compared to the IC formed on a general silicon wafer,” the ESD protection circuits located after the input terminals are insufficient to protect the TFT driving circuitry located far from the input terminals from ESD events, particularly during the manufacturing process. *Id.* Specifically, “since there is a possibility that the static electricity is

electrified on a certain location on the substrate during the manufacturing process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation.” *Id.*; see also *id.*, 3:67-4:13 (“when an active matrix used in a TFT-LCD or TFT-OLED and a driving circuit thereof are formed on the insulating substrate, the driving circuit is configured to surround the active matrix, so that it becomes larger and accordingly its line is also lengthened.”).

40. To address these problems, the ’157 patent discloses and claims placing ESD protection circuits on both ends of the scanning line TFT driving circuit. ESD protection circuits ESD1 to ESD4 are disposed between input terminals and the scanning line driving circuit, as in the conventional art, to protect the scanning line driving circuit from charges entering via the input terminals. ESD protection circuits ESD11 to ESD13 are disposed at the far end of the opposite side of the scanning line driving circuit relative to the input terminals. *Id.*, 5:44-6:2.

41. For example, as shown below for protecting the scanning line driving circuit 800 from charges entering via the low potential power source line 750, **scanning line driving circuit 800** composed of **driving unit circuits 801** is formed on the **active matrix substrate 101** and the **driving unit circuits 801** are

connected to **scan lines 201** to supply a driving signal. The pixel switching elements 401 are connected to the **scan lines 201** and data lines 202. The **low potential power source line 750** is connected to the **scanning line driving circuit 800** and the **low potential power source terminal 650**. A **first protection circuit ESD1** is connected between the **low potential power source terminal 650** and the **low potential power source line 750**, and a **second protection circuit ESD11** connected to the **low potential power source line 750** is “disposed at [the] far end of the opposite side” from the **input terminal 650** “with a **scanning line driving circuit 800** therebetween”:



Id., Fig. 1; 4:60-5:65.

42. The '157 patent explains that ESD1 prevents the scanning line driving circuit 800 from being damaged when excess charges are input from the low potential power supply terminal 650. *Id.*, 5:50-54. And ESD11 prevents static charges generated “during manufacturing [of] the active matrix substrate” from entering the scanning line driving circuit 800 via the opposite end of the low potential power supply line 750 with respect to its supply terminal 650 and damaging portions of the scanning line driving circuit “located far from a terminal.” *Id.*, 5:61-65.

43. Independent claims 4 and 17, for example, recite this improved ESD protection scheme for active matrix displays with TFT driving circuits.

4. A display device, comprising:
 - a scanning line driving circuit;
 - a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
 - an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that
are connected to the scanning line driving circuit to
protect the scanning line driving circuit, and the first
protection circuit and the second protection circuit
are connected to the power supply line,
the first protection circuit being connected to the power
supply line between (i) a first connecting portion at
which the scanning line driving circuit and the
power supply line are connected and (ii) the input
terminal, and
the scanning line driving circuit being connected to the
power supply line between (iii) a second connecting
portion at which the first protection circuit and the
power supply line are connected and (iv) a third
connecting portion at which the second protection
circuit and the power supply line are connected.

Id., 12:25-47.

17. A display device, comprising:
a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting

portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

Id., 14:16-43.

44. The '157 patent explains that placing the scanning line TFT driving circuit between protection circuits in this manner confers an additional benefit because the protective circuits on either side of the scanning line TFT driving circuit may be “arranged at corners far from the input terminals among four corners of the active matrix” which makes it “possible to arrange large-sized protective circuits without making the peripheral area [of the active matrix substrate—i.e., the portion of the substrate that does not include pixels] large.” *Id.*, 4:14-19. In particular, arranging the second set of protective circuits “at the corner part of the active matrix substrate, particularly at the corner opposite to the input terminals” enables the scanning line TFT driving circuit to be protected without “making the substrate area larger.” *Id.*, 5:65-6:2.

45. Dependent claim 8, for example, recites this improved ESD protection scheme:

8. The display device as set forth in claim 4, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

Id., 12:58-13:2.

46. In my opinion, none of the asserted prior art references or combinations disclose the claimed layouts that deliver the benefits of the '157 inventions, for reasons that I discuss further below.

B. Related District Court Litigation

47. I am aware of a related District Court case involving the same parties, in which the '157 patent has been asserted and validity of the '157 patent claims has been challenged. I have offered opinions in that case regarding the validity of the '157 patent claims.

VI. ANALYSIS OF REINER (GROUND 1)

A. Overview of Reiner

48. Reiner relates to “integrated circuit devices with ESD protection” and, in particular, forming “bump bridges” that provide low-ohmic interconnections within an integrated circuit device including one metallization layer. Ex. 1005, 2:1-3.

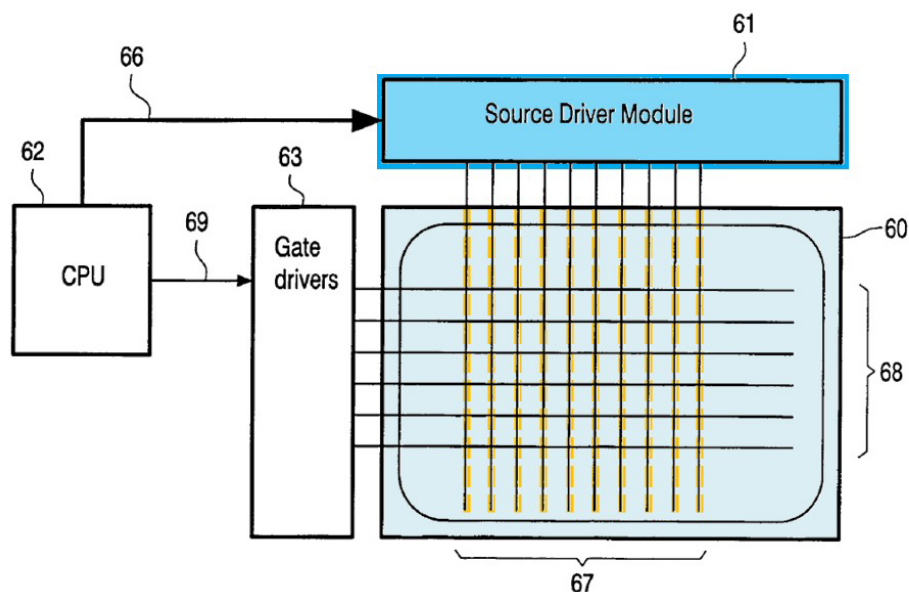
49. Reiner addresses a different problem than the '157 patent: it teaches bump bridges to facilitate interconnections in an integrated circuit device comprising a silicon substrate including a single metallization layer, providing a solution that saves space and money compared to alternatives. *See, e.g., id.*, 4:10-5:2. “The higher the integration density of these integrated circuit devices gets, the more difficult it is to realize the routing of all the necessary interconnections inside a single metallization layer.” *Id.* at 2:7-9. “In situations where the routing cannot be realized with a single metallization layer, one currently has two options. Either, a few polysilicon interconnections are provided where necessary, or another

metallization layer is added.” *Id.*, 2:11-13. Each has its disadvantages: “polysilicon interconnections usually are relatively big thus occupying part of the device’s surface area that otherwise would be available for integrated devices,” and a second metallization layer is expensive. *Id.*, 2:16-21.

50. As one application of its bump-bridge solution, Reiner describes integrated circuit devices including ESD protection networks. ESD protection networks “prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event,” for example, when someone touches the chip’s pins (input and output points). *Id.*, 2:28-3:3. Reiner describes an ESD protection network comprising (1) “protection diodes and/or transistors,” and (2) low-ohmic “metal interconnection lines for connecting these diodes and/or transistors with inputs and/or outputs of the integrated circuit device to be protected.” *Id.*, 3:4-8. Reiner teaches using its bump-bridge arrangements to avoid using a polysilicon interconnection or two metallization layers where lines need to cross. *Id.*, 3:8-13. Figure 2 shows that a “bump bridge crosses another metal line that is situated within the metallization level, without making contact to this metal line.” *Id.*, 4:32-33.

51. Relevant here, Reiner discloses an “integrated circuit display driver” to “drive many lines of an LCD display.” *Id.*, 9:11-22. Reiner Figure 4 shows a schematic block diagram including an LCD display and external integrated circuit

display drivers. The LCD display comprises LCD screen 60, a plurality of source lines 67, and a plurality of gate lines 68. *Id.*, 9:24-26. Figure 4 also includes a source driver 61 to drive a plurality of source (i.e., data) lines 67, gate driver 63 to drive a plurality of gate (i.e., scan) lines 68, and CPU 62 that provides video signals to the source driver 61 via bus 66 and row timing signals to gate driver 63 via bus 69:²

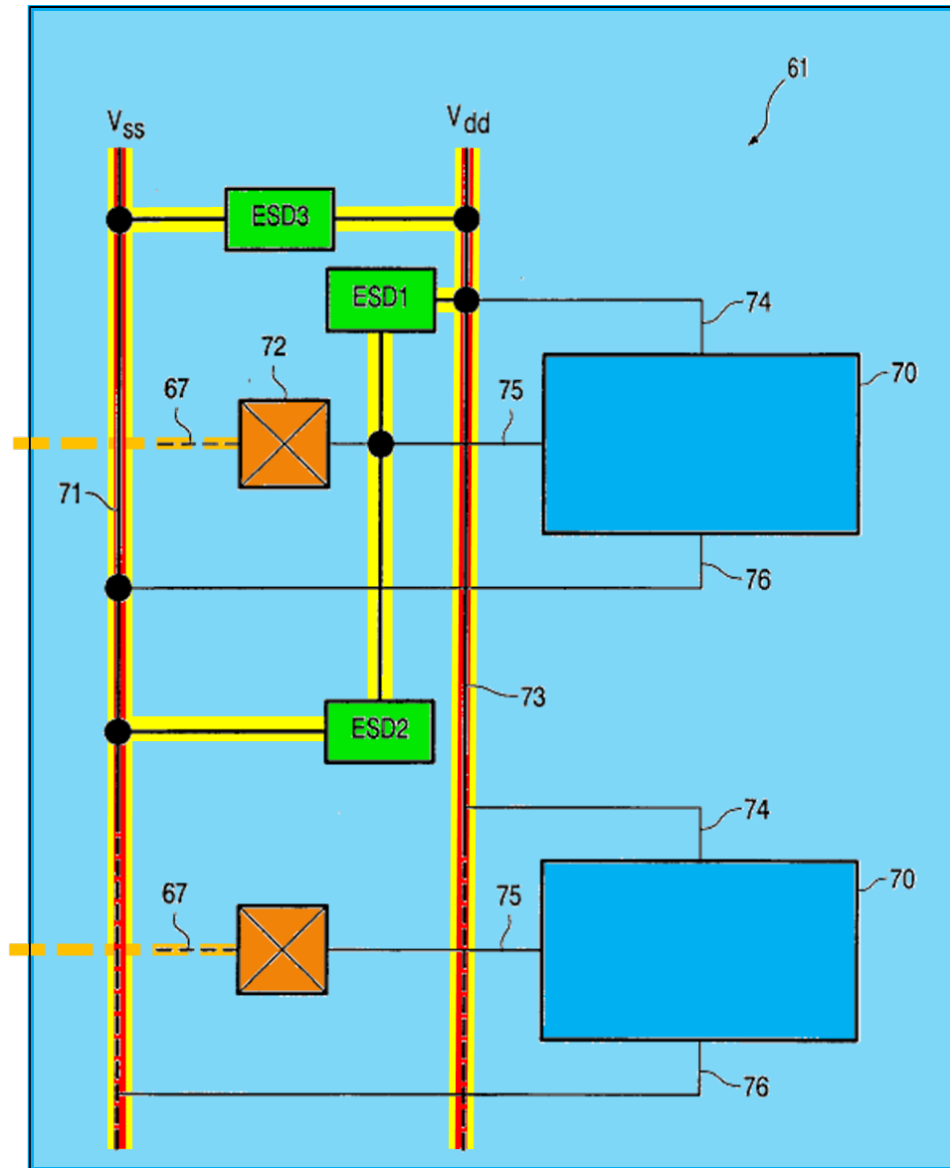


Id., Fig. 4, 9:23-35.

52. Reiner describes, and Figure 5 shows, “ESD protection means” “integrated into” source driver 61. *Id.*, 9:21-22. Reiner’s **source driver 61** includes “an array of several parallel **output devices 70**,” which “drive the **source lines 67**

² A POSITA would understand that “source” lines and “data” lines refer to the same lines, and “gate” lines and “scan” lines refer to the same lines. The respective terms are interchangeable.

with the voltages needed by each pixel of the LCD screen 60.” *Id.*, 10:1-24. Each output device 70 includes an output 75, which is connected to a **source line 67** via a **contact pad 72**. *Id.* (source lines 67 connected to contact pad “by means of bonding”). A **power supply line 73** provides the supply voltage Vdd to the **output devices 70** via connection 74, and a second **power supply line 71** provides the supply voltage Vss to the **output devices 70** via connection 76. *Id.* Three ESD devices, **ESD1**, **ESD2**, and **ESD3**, “are provided for each **output device 70** . . . to protect the circuitry inside the **devices 70**.” *Id.* **ESD1** is connected between the output line 75 and the **power supply line 73** (Vdd), **ESD2** is connected between the output line 75 and the **power supply line 71** (Vss), and **ESD3** is situated between the two **power supply lines 71** and **73**. *Id.* “The ESD devices may comprise diodes, transistors and other circuits that are suited to provide for a low-ohmic path to a terminal (e.g., a ground terminal) in case of a voltage peak.” *Id.*, 10:15-17. Figure 5 shows low-ohmic paths in bold (highlighted in yellow). *Id.*, 10:19.



Id., Fig. 5.

53. Reiner discloses an “ESD protection means” inside a source driver integrated circuit, to protect the circuitry within output devices 70. *Id.*, 10:10-12. Specifically, the ESD devices protect against electrical charges that may enter the output device via contact pads 72. Reiner explains that IC chips, like source driver 61, often comprise ESD protection “in order to prevent the very sensitive circuits

on the chip from being destroyed when it is subjected to a discharge event. This might happen for example when somebody induces a voltage peak in the circuitry by touching the pins of the chip.” Ex. 1005, 2:28-3:3. Reiner further explains that ESD protection networks within IC chips, like source driver 61, “comprise[] protection diodes and/or transistors and metal interconnection lines for connecting these diodes and/or transistors with *inputs and/or outputs of the integrated circuit device to be protected.*” *Id.*, 3:4-8 (emphasis added). In short, Reiner describes an ESD protection network inside an integrated circuit for protecting the IC chip’s internal circuits from electrical charges that could enter the IC chip through its input and/or output terminals.

54. In Reiner’s source driver 61, the ESD protection network protects the individual outputs 70 from electrical charges that could enter the IC chip through its contact pads or pins. Reiner does not disclose input pins on source driver 61 IC. *Id.*, 9:11-10:23. Reiner discloses only contact pads 72, for connecting the source driver’s outputs 75 to the source lines on the LCD display 60. *Id.*, 10:4. Figure 5 shows no other inputs/outputs. *Id.*

B. The teachings of Reiner do not disclose or render obvious all limitations of any of claims 1-18 of the ’157 patent.

55. In my opinion, Reiner does not disclose or render obvious all limitations of any challenged claim.

1. *Claim 4*³

a. “[a] display device, comprising . . . an input terminal connected to the power supply line to supply power”
(claim 4[c])

56. In my opinion, Reiner does not disclose or render obvious “[a] display device, comprising . . . an input terminal connected to the power supply line to supply power.” Ex. 1001, claim 4[c].

57. In my declaration in support of Patent Owner’s preliminary response, Ex. 2001, I noted that Dr. Murphy concedes that Reiner is silent regarding input terminals for power lines 71 (Vss) and 73 (Vdd) of source driver 61. Ex. 1003, ¶98; Ex. 1005, 9:11-10:23 (disclosing only contact pads 72 for connecting source driver 61’s outputs 75 to the source lines on the LCD display 60), Figs. 4-5.

58. I understand that in its Institution Decision, the Board noted that “Reiner does not disclose any particular mechanism or structure for supplying power to its power supply lines 71-Vss and 73-Vdd. . . . Figure 5 similarly illustrates power supply line 71 being connected to supply voltage Vss, and power supply line 73 being connected to supply voltage Vdd, without providing any further detail as to how power is supplied to line 71-Vss and line 73-Vdd.” I.D. at 21. I agree. The Board also noted that the preliminary record suggests that “a

³ I have been instructed to present my opinions regarding claims 4-18 before claims 1-3 in order to present my opinions in the same order as Dr. Murphy. Ex. 1003, ¶87.

person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner's power supply lines 71-Vss and 73-Vdd." I.D. at 21.

59. In my opinion, even if Reiner renders obvious input terminals to provide power to lines Vss and Vdd as part of source driver 61, those input terminals would not be input terminals of the display device. Those input terminals would be input terminals of the integrated circuit source driver 61, which is formed on a silicon substrate separate from LCD display 60. *See, e.g.*, Ex. 1005, 4:22-23 (describing integrated circuit device that comprises a silicon substrate, of which source drive 61 is an example). Claim 4 of the '157 patent recites a display device comprising "an input terminal connected to the power supply line to supply power." A POSITA would understand that a display device comprising an input terminal connected to the power supply line to supply power refers to an input terminal of the display device, rather than an input terminal of a separate integrated circuit connected to the display (in Reiner, connected to LCD display 60). Dr. Murphy opines that Reiner renders obvious input terminals for the integrated circuit source driver 61. That, in my opinion, does not meet the claim limitation.

60. Nothing in Reiner suggests that lines Vss and Vdd also supply power to the LCD display 60. Indeed, a POSITA would understand that LCD display 60 may include separate input terminals for separate power supply lines, because LCD

display 60 is formed on a separate substrate. Indeed, Dr. Murphy appears to acknowledge that LCD display 60 and its separate substrate could include separate power supply lines and corresponding input terminals. Ex. 1003, ¶101.

61. Thus, in my opinion, Reiner does not disclose or render obvious “[a] display device, comprising . . . an input terminal connected to the power supply line to supply power.”

b. “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed (claims 4[d], 4[e], 4[f])

62. In my opinion, Reiner does not disclose or render obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed. Ex. 1001, claim 4[d-f].

63. I disagree with Dr. Murphy’s opinion that Reiner discloses protection circuits connected to a scanning line driving circuit and arranged as claimed. *See* Ex. 1003, ¶¶103-111. In my opinion, Reiner discloses, and Dr. Murphy cites, only an ESD protection network within a source (data line) driver IC chip. And Dr. Murphy fails to show that Reiner discloses or renders obvious applying Reiner’s source driver ESD protection network to a gate driver so that the layout would

remain the same. Indeed, a POSITA would know to expect changes in the layout in view of key differences between a source driver and a gate driver.

64. Reiner discloses a particular ESD protection network for only a source driver. Reiner discloses “[a] source driver module 61” that drives “the individual source lines 67” of an LCD display 60 and “[a] gate driver 63 . . . that usually drives one whole gate line 68.” Ex. 1005, 9:23-34. Reiner’s Figure 5 shows a “schematic block diagram of a display driver 61” including “details of display driver 61 in accordance with” Reiner’s invention, including ESD devices. *Id.*, 9:20-24, 10:1-24 (describing the configuration and operation of source driver 61 shown in Figure 5). But unlike source driver 61, Reiner does not disclose a gate driver including an ESD protection network. In fact, Reiner discloses few gate driver details, except that a gate driver “usually drives one whole gate line” and that CPU 62 provides “row timing signals (control signals) via a bus 69 to the gate driver 63.” *Id.*, 9:27-31. Reiner does not disclose protection circuits connected to a gate (scan line) driver.

65. It is my opinion that Dr. Murphy does not show that Reiner renders obvious protection circuits connected to a scanning line driving circuit and arranged as claimed. Instead, Dr. Murphy argues only that a gate driver would benefit from ESD protection in general and that a POSITA would have been motivated to protect “gate driver 63 in the same way as source driver 61 to prevent

the sensitive circuits from being damaged by ESD events.” Ex. 1003, ¶115. Dr. Murphy argues that a POSITA would want to protect “each output device 70,” but Dr. Murphy does not cite evidence showing that (1) the gate drivers comprise output devices 70, or (2) the gate driver is arranged like the source driver, to accommodate the same ESD layout. Indeed, Reiner discloses that the gate driver integrated circuit comprises individual gate drivers, not output devices 70. Ex. 1005, 9:20-9:31. And Dr. Murphy’s opinion that the gate driver integrated circuit and the source driver integrated circuit would “have similar configurations” is conclusory. Ex. 1003, ¶¶117-118.

66. To the contrary, it is my opinion that a POSITA would expect to see differences between the gate driver arrangement and the source driver arrangement. For example, a POSITA would understand that individual gate/scan line drivers are coupled to one another, to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time (e.g., one would not simultaneously turn ON two horizontal rows of transistors). An LCD display functions when only one gate/scan line driver (out of the hundreds of gate/scan unit drivers) drives, at any one time, one row of transistors to their ON state. This coupling between individual gate/scan unit drivers is not, however, required for source/data unit drivers because each

individual source/data driver transmits image data signals simultaneously to each vertical column of a display.

67. Overall, substituting a source driver with a gate driver would not be obvious for the following reasons: **First**, the two types of drivers are functionally different in fundamental ways. Specifically, the individual gate line unit driving circuits are in communication with the two neighboring unit drivers so that the ensemble of gate line unit driving circuits can operate as a shift register. Whereas this functionality is disclosed in the '157 patent (for example by the SP signal line 702), Reiner is devoid of such disclosure. **Second**, the two driver structures have a fundamentally different architecture. Whereas the source line unit drivers are independently operating drivers whose signals are independent from one another, the gate line drivers are coupled and coordinated so that only one gate line at a time will provide an ON signal to a row of pixels and associated switching TFTs. Furthermore, whereas the source line drivers provide analog image information signals, the gate line drivers provide two-state, digital ON and OFF signals. **Third**, the source drivers drive all data lines at all times, whereas the gate drivers drive, sequentially, one gate line at a time, as discussed above. **Fourth**, due to the fundamental differences between source line drivers and gate line drivers (as discussed above), a specific ESD protection arrangement that works for source drivers would not necessarily be known to work as ESD protection for a gate

driver. In short, a POSITA would understand that a source driver and a gate driver would have different layouts, functions, and operations (e.g., analog versus digital). Reiner does not disclose or suggest that source driver 61's internal ESD layout would, or even could, apply to a gate driver.

68. Thus, it is my opinion that the Petition fails to show that Reiner discloses or renders obvious “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged with respect to the scanning line driving circuit and power supply line as claimed in 4[e] and 4[f].

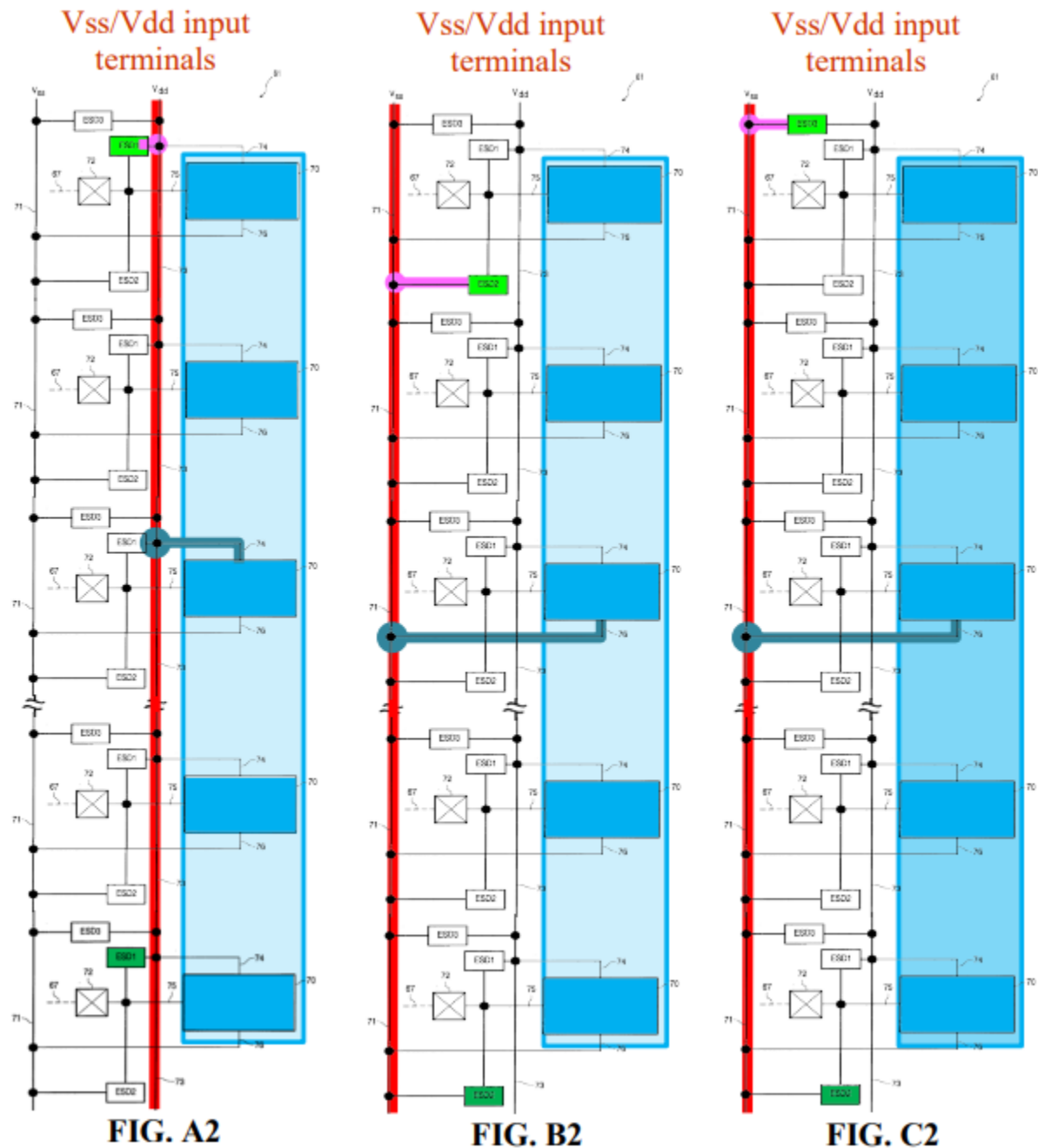
c. *“the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal” (claim 4[e])*

69. I disagree with Dr. Murphy that Reiner discloses three ESD devices and that each discloses a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal.” Ex. 1001, claim 4[e].

70. To be clear, in my opinion, Reiner does not disclose the claimed scanning line driving circuit. As discussed above, Dr. Murphy relies on Reiner's source driver 61 to support his opinion. I carry that opinion throughout my report,

including as I discuss other limitations that recite “scanning line driving circuit.” In addition, in my opinion, Reiner discloses at most one ESD device that is “connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit [in Reiner, source driver] and the power supply line are connected and (ii) the input terminal”—specifically, ESD3. I will explain why.

71. First, I note that Dr. Murphy seems to contend that “a first connecting portion at which the scanning line driving circuit and the power supply line are connected” may be *any* connecting portion at which an output device 70 and line Vss or line Vdd are connected—specifically, any of lines 74 and 76 in Reiner Figure 5 for any of output devices 70. Indeed, in his composite images using multiple copies of Reiner Figure 5, Dr. Murphy appears to choose “a first connecting portion at which the scanning line driving circuit and the power supply line are connected” in the middle of the annotated images:



Ex. 1003, ¶123 (dark blue highlighting Dr. Murphy’s selection of “a first connecting portion at which the scanning line driving circuit and the power supply line are connected”).

72. In my opinion, Reiner's source line driver is unsuitable as a gate line driving circuit for the reasons discussed above. Furthermore, Dr. Murphy's interpretation of claim 4 defeats the purpose of the claimed invention, which places a power supply line protection circuit between that power supply line's input terminal (of the display device) and the power supply line's connection to the scanning line driving circuit, to protect the scanning line driving circuit from charges that could enter the device through the input terminal and travel along the power supply line and damage the scanning line driving circuit. More important, limitation 4[e] understood in context with limitation 4[f] confirms that claim 4 plainly recites a scanning line driving circuit—rather than, for example, individual scanning line driving units—between two protection circuits. Claim 4[f] provides: “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

73. Thus, in my opinion, the claimed first protection circuit must be connected to the power supply line *between*, as claimed, that power supply line's connection to any portion of the scanning line driving circuit and the power supply line's input terminal.

74. I discuss the layout that Reiner shows in its Figure 5 to explain how neither ESD1 nor ESD2 is connected to the power supply line *between*, as claimed, that power supply line's connection to any portion of the scanning line driving circuit (again, in Reiner, a source driver) and the power supply line's input terminal (though again, I dispute that Reiner discloses the input terminals as claimed and carry this opinion throughout my report). ESD1 and ESD2 are not connected to a power supply line between the claimed reference points (namely, "(i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal"). Even if I assume that input terminals for lines Vss and Vdd are located at the top of Reiner Figure 5, as Dr. Murphy suggests, ESD1 is connected to line Vdd *at the same location* at which the source driver is first connected to line Vdd. That does not satisfy the plain language of the claim requiring that the protection circuit be connected to the power supply line *between* (i) a first connecting portion at which the scanning line driving circuit (in Reiner, source driver) and the power supply line are connected and (ii) the input terminal. Likewise, ESD2 is not connected to the power supply line Vss *between* (i) a first connecting portion at which the scanning line driving circuit (in Reiner, source driver) and the power supply line are connected and (ii) the input terminal, either. Rather, the source driver and line Vss are connected to

one another *between* the purported input terminals and ESD2's connection to line V_{ss}.

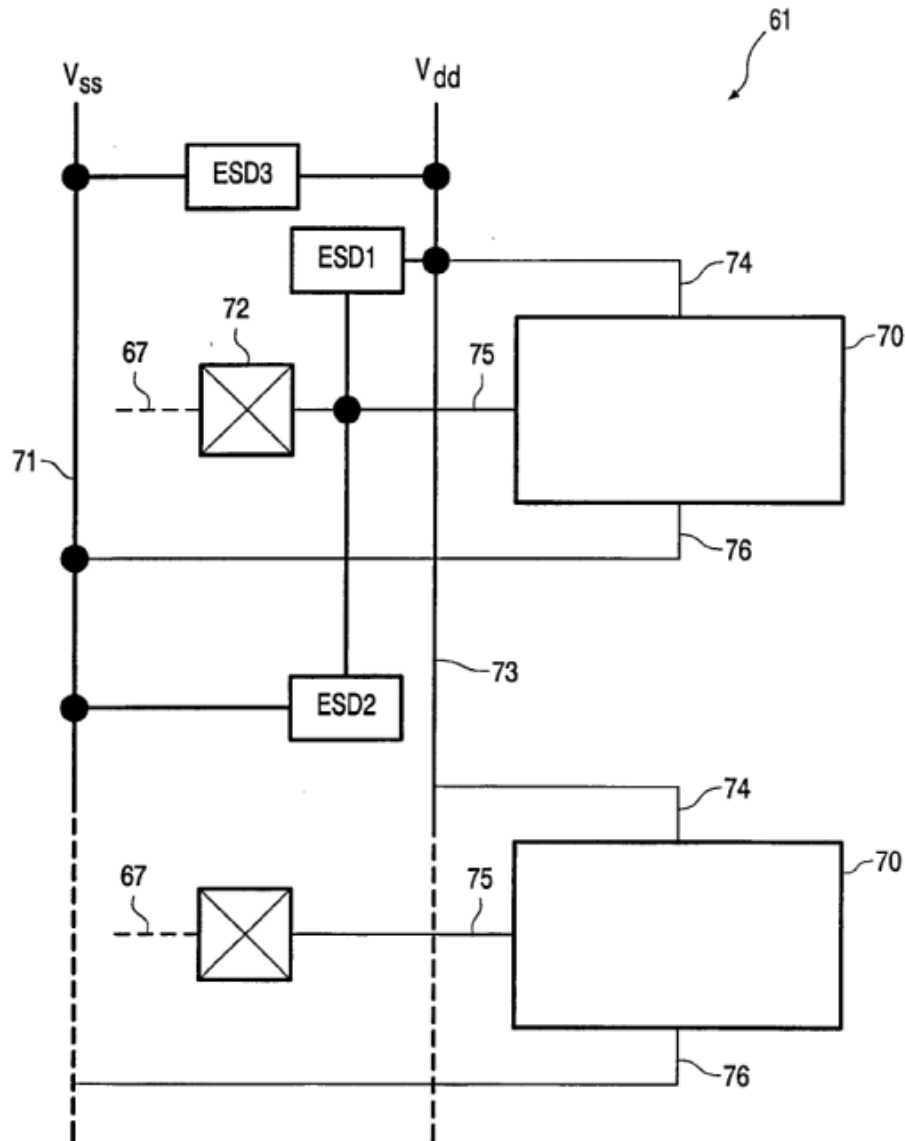


FIG. 5

Ex. 1005, Fig. 5. Neither ESD1 nor ESD2 is connected to the power supply line *between* (i) a first connecting portion at which the scanning line driving circuit and

the power supply line are connected and (ii) the input terminal. In my opinion, only ESD3 is connected to the power supply line *between* (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal (again preserving my arguments that Reiner still does not satisfy the claimed scanning line driving circuit limitations or the claimed input terminals of a display device limitations).

d. “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f])

75. In my opinion, Reiner does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” Ex. 1001, claim 4[f].

76. In my opinion, one significant difference separates Reiner from the claimed inventions of the '157 patent: Reiner teaches an integrated circuit on a silicon substrate and including an internal ESD protection network, in particular, ESD devices connected between each input/output (i.e., entry point into the integrated circuit, here, the Vss and Vdd input terminals and each contact pad 72)

and the integrated circuit's output devices 70. Reiner does not disclose the arrangement described and claimed in the '157 patent, namely, protection circuits on either end of an on-array scanning line driving circuit to protect the scanning line driving circuit from ESD damage that could accumulate on the display's insulating substrate during manufacturing. Because Reiner describes only ESD protection networks *in* an integrated circuit, it does not disclose a scanning line driving circuit connected to a power supply line between first and second protection circuits.

77. In my opinion, a POSITA would understand that the plain language of the claim requires that the scanning line driving circuit connect to a power supply line *between* the protection circuit connecting portions. Reiner's ESD protection network is *inside* its purported scanning line driver (source driver 61), to protect individual output devices 70. Reiner is not the claimed invention.

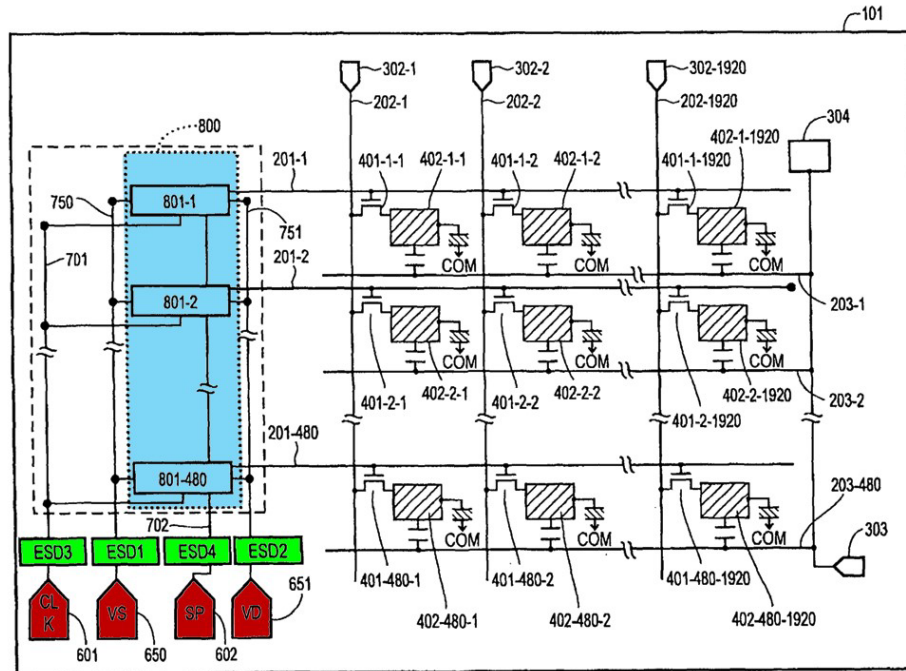
78. Reiner is the conventional art on which the '157 patent expressly improves. In its background section, the '157 patent explains that, in an integrated circuit like Reiner's driver 61, "it is important to take measure[s] against the electro-static damages (ESD) when a high voltage caused by a static electricity or a various noise phenomenon is unintentionally *applied to the inside of the device* to damage an insulating film, thereby causing a fatal damage to the device."

Ex. 1001, 1:14-19 (emphasis added). "[S]ince general semiconductor devices are

formed on a silicon wafer made of conductive material, there are little chances of being electrified within the semiconductor device, so that it is a key issue to prevent the damage when a static electricity flows *through input terminals*.” *Id.*, 1:23-28. The ’157 patent explains that integrated circuit ESD protection means—the conventional art on which the ’157 patent improves—are configured to protect the device by protecting the access points through which an ESD event could enter the device to prevent an ESD event from damaging the device’s internal circuitry. Reiner teaches the same configuration. Reiner protects the integrated circuit, providing ESD devices between its access points (inputs/outputs) and individual devices 70. Reiner describes an ESD protection network comprising (1) “protection diodes and/or transistors,” and (2) low-ohmic “metal interconnection lines for connecting these diodes and/or transistors *with inputs and/or outputs of the integrated circuit device to be protected*.” Ex. 1005, 3:4-8 (emphasis added).

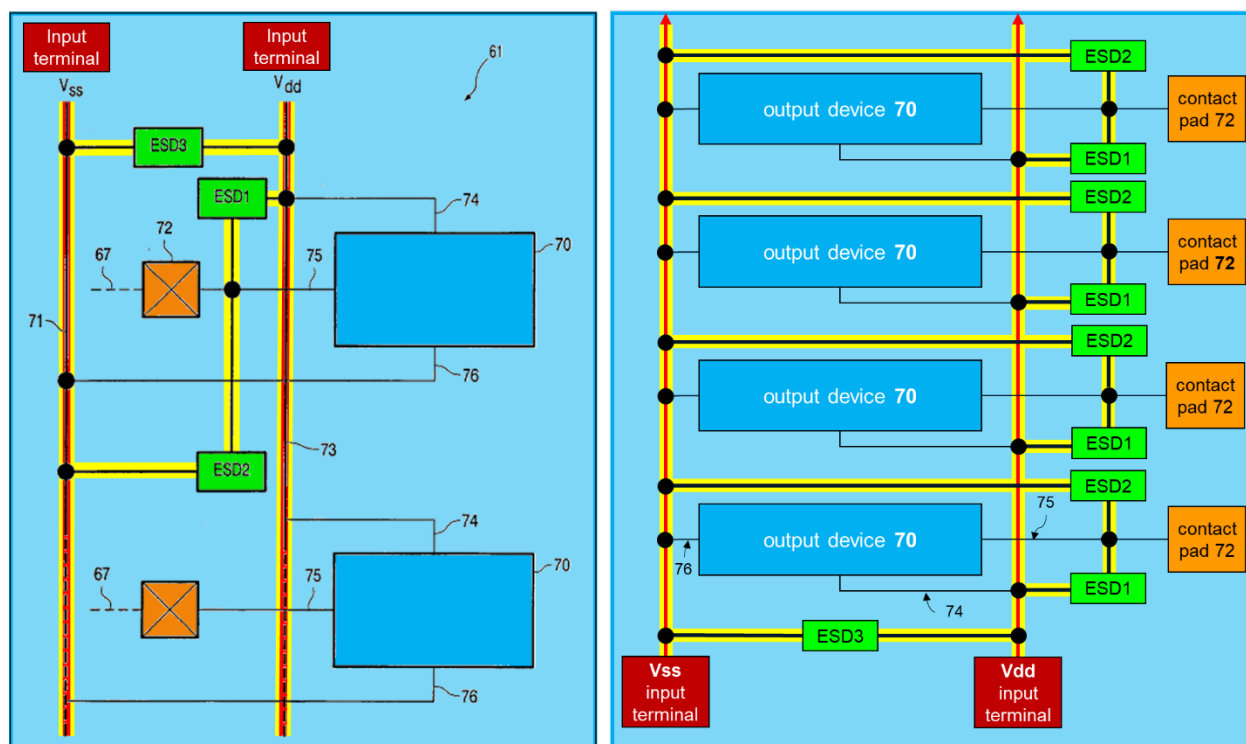
79. The ’157 patent explains that the conventional art applied these integrated circuit teachings to a display device including a scanning line driving circuit formed on the TFT array substrate: “a conventional method used in a semiconductor on a silicon wafer is applied as it is, so that only protective circuits for preventing the static electricity from the input terminals are built in, and a conventional method of a display device not having the built-in driving circuit is

used to protect the active matrix circuit from the static electricity.” Ex. 1001, 1:48-54. The ’157 patent shows this arrangement in Figure 11:

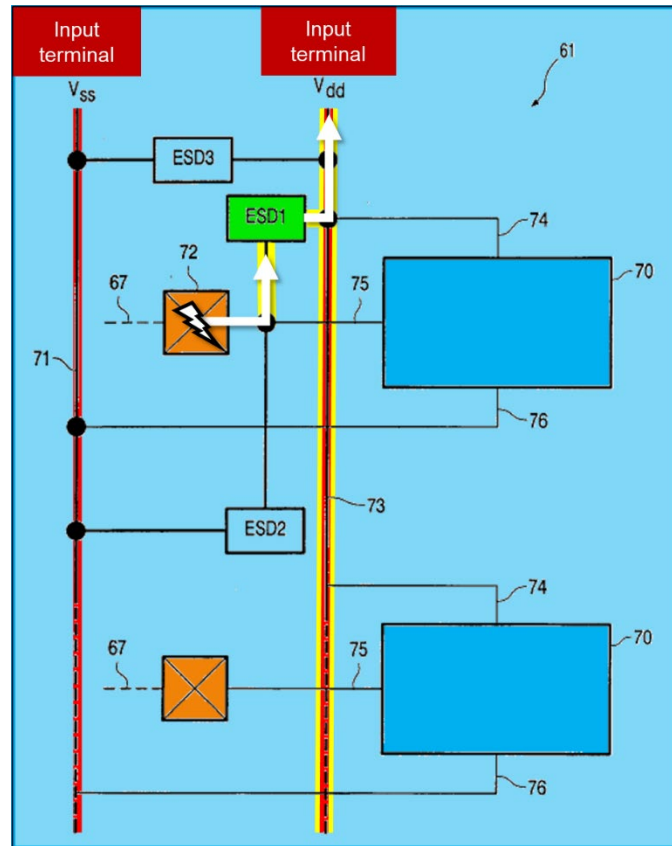


Id., Fig. 11, 2:25-28 (“static electricity protection circuits ESD1 to ESD4 are provided between the input terminals 601, 650 and 651 and the scanning line driving unit circuits 801-1 to 801-480, respectively”).

80. Redrawing Reiner Figure 5—maintaining its disclosed arrangement but reorienting to compare to ’157 Figure 11—shows that Reiner teaches no more than the conventional arrangement, before the ’157 patent’s claimed improvements. It teaches ESD protection between input/outputs of the source driver 61 device to protect output devices 70 of source driver 61:

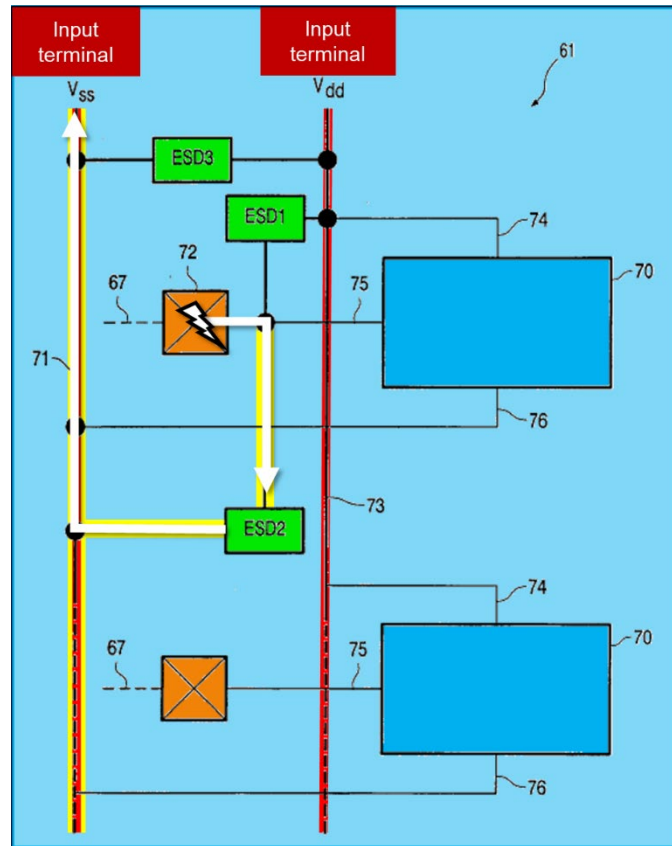


Ex. 1005, Fig. 5 (showing **integrated circuit driver 61** and **output devices 70**, **input terminals** (not explicitly disclosed), **power supply lines Vdd and Vss**, **ESD devices**, and **contact pads 72**, and low-ohmic lines highlighted in yellow). Reiner teaches that its ESD1 is connected to line 75 between contact pad 72 and output device 70, to shunt to the Vdd line (low-ohmic path) electrostatic discharge that may otherwise enter the integrated circuit through contact pad 72 and travel along line 75 to device 70. Ex. 1005, 10:12-20. ESD1 prevents electrostatic charges (annotated using white lightning bolt, below) from entering output device 70 by shunting the charge to a ground terminal (not shown in Fig. 5) via ESD1 and the low-ohmic line connecting ESD1 to Vdd, which is also a low-ohmic line (white arrow). *Id.*, 10:15-20.



Ex. 1005, Fig. 5.

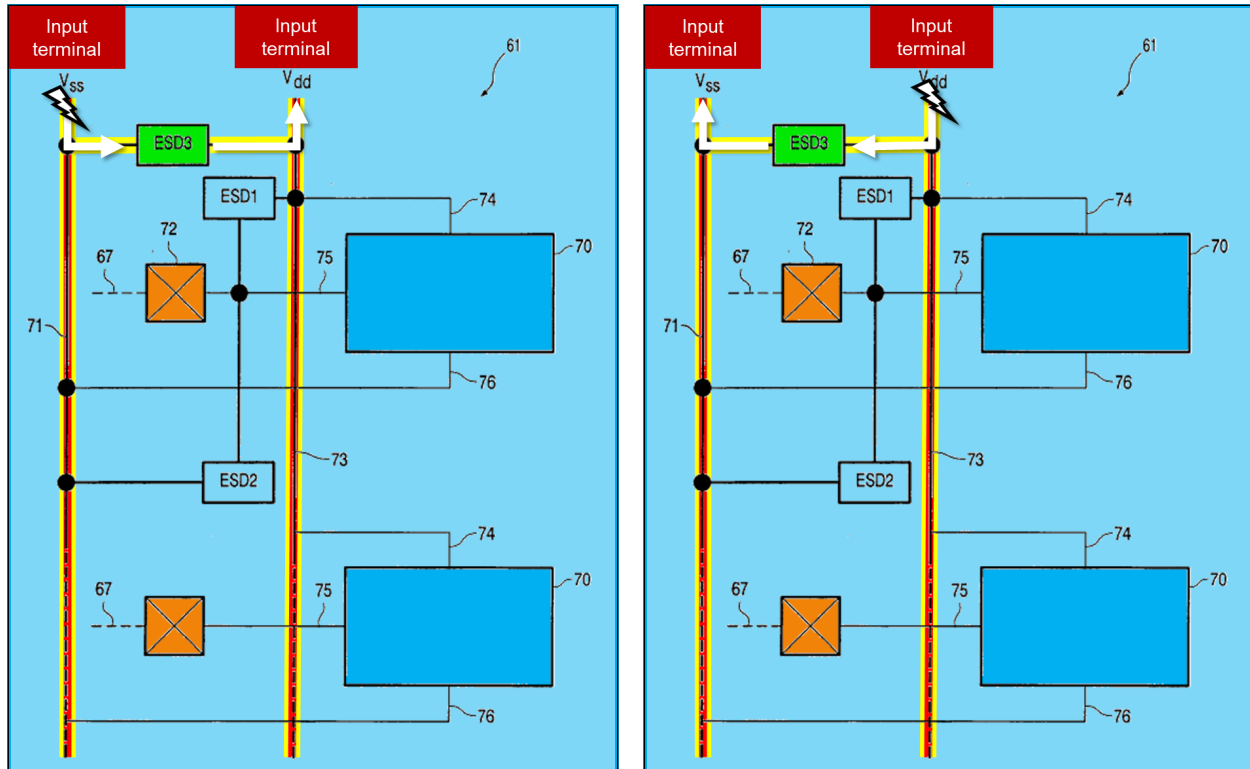
81. ESD2 is connected to line 75 between contact pad 72 and output device 70, to shunt to the V_{ss} line (low-ohmic path) electrostatic discharge that may otherwise enter the integrated circuit through contact pad 72 and travel along line 75 to device 70. Ex. 1005, 10:13-20. ESD2 prevents electrostatic charges (white lightning bolt) from entering output device 70 by shunting the charge to a ground terminal (not shown in Fig. 5) via ESD2 and the low-ohmic line connecting ESD2 to V_{ss} , which is also a low-ohmic line (white arrow). *Id.*, 10:15-20.



Ex. 1005, Fig. 5.

82. And ESD3 is connected to lines V_{ss} and V_{dd} between the purported input terminals and output devices 70, to protect output devices 70 from electrostatic charges that may enter integrated circuit device 61 through the V_{ss} or V_{dd} input terminals and travel along the power lines and enter output device 70 via connections 74 or 76, respectively. Ex. 1005, 10:14-20. ESD3 prevents electrostatic charges (white lightning bolts) from entering output device 70 by shunting the charge to a ground terminal (not shown in Fig. 5) via ESD3 and the

low-ohmic line connecting ESD3 to Vss and Vdd, which are also low-ohmic lines (white arrows). *Id.*, 10:15-20.



Id., Fig. 5.

83. Each ESD device is between an input/output and devices 70.

84. In my opinion, Reiner discloses only the prior art: an integrated circuit including an internal ESD protection network. Thus, Reiner does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

2. *Claim 5*

85. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner renders obvious claim 5.

3. *Claim 6*

86. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner renders obvious claim 6.

4. *Claim 7*

87. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner renders obvious claim 7.

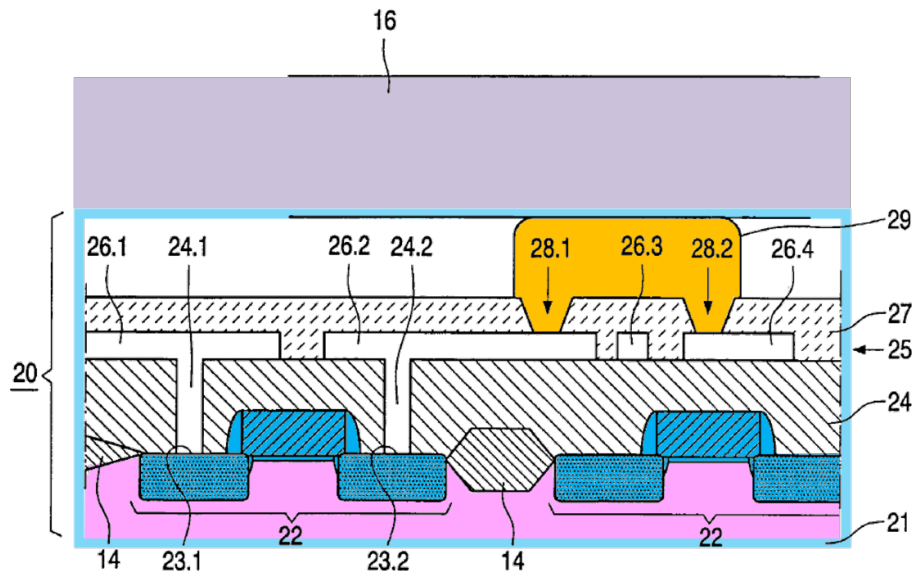
5. *Claim 8*

88. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner renders claim 8.

89. Reiner also fails to render obvious the additional limitations of claim 8. Reiner does not disclose a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate.” Dr. Murphy contends that Reiner discloses these elements by way of “substrates 21 or 16” of the integrated circuit 20 shown in Reiner Figure 2. But Dr. Murphy does not

identify a *display device* substrate and a scanning line driving circuit arranged on that substrate. Reiner discloses integrated circuits having their own substrates and, separately, a display to which the integrated circuits may connect (for example, via contact pads).

90. Reiner Figure 2 shows a schematic cross-section of an **integrated device 20** that “comprises a **silicon substrate 21**” and at least one **integrated device 22**. Ex. 1005, 6:18-21. The **integrated device 20** includes **bump bridges** that “provide for a connection to an interconnection on a **substrate 16**,” and Reiner explains the **integrated circuit device 20** may be “flipped onto the **substrate 16**” so that the “**substrate 16** with its interconnections may rest on” the **bump bridges** of **integrated circuit device 20**. *Id.*, 7:22-25.



Id., Fig. 2.

91. First, Reiner's substrate 16 does not disclose a display device "substrate" or a "substrate" on which the integrated device 20, let alone gate drivers 63, is "arranged": the integrated device 20 is formed on substrate 21 and then flipped onto substrate 16 when it is packaged. *Id.*; Ex. 1001, 5:20-23 (the semiconductor circuit in the scope of the claims "is **formed** by integrating polysilicon thin film transistors **on** the active matrix [glass] substrate") (emphasis added); 1:33-36 ("in a display device using an active element such as a thin film transistor (TFT) . . . a device is **formed on** an insulating substrate") (emphasis added); 2:35-37 ("in the case that the driving circuit of the display device is **formed on** a glass substrate") (emphasis added).

92. Second, Reiner's substrate 21 does not disclose a display device "substrate"; it is the substrate on which integrated device 20 is formed.

93. To the extent that Dr. Murphy suggests that a POSITA would simply mount Reiner's silicon integrated circuit drivers on an LCD display substrate, I disagree. Reiner discloses a silicon integrated circuit chip (Si IC chip) that is used as a data line driver circuit. Reiner's Si IC data line driver circuit is located off of the LCD glass panel and connected to the LCD panel's data lines by means of electrical connectors and metallization lines. For a full HD (high definition) display (1920 × 1080), 1920 data lines are connected to the Si IC data line driver

circuit by means of 1920 data connection lines and an associated electrical connector.

94. Similarly, when implementing a scanning line driver circuit by means of a Si IC located off the TFT substrate, the number of connection lines would need to be equal to the number of scan lines. For example, a Full HD display (1920 × 1080) would require 1080 scan lines that are routed from a Si IC driver circuit onto the TFT substrate to the scan lines. The routing of such a large number of scan lines from an off-TFT-substrate location to an on-TFT-substrate location would require electrical connectors that include at least 1080 connection points.

95. On the other hand, a scanning line driver circuit implemented by TFTs (thin film transistors) located on the TFT substrate of an LCD panel is a solution that reduces the number of external connection lines from 1080 lines to just a handful of lines. These lines include a frame start signal, a clock signal, a clock-bar signal, a positive power supply line, and a negative power supply line.

96. A POSITA, given the choice between a handful of connection lines (that is, about 5) and 1080 connection lines would clearly prefer the lower number of connection lines enabled by TFT-based scanning line driver circuits.

97. When driver Si IC data line driver circuits are used in conjunction with LCD displays, the Si ICs are typically mounted in COF (chip on flex), TCP (tape carrier package), or TAB (tape automated bonding) configurations. These

mounting technologies can also be used for the scanning line driver circuits. This is different than arranging a scanning line driving circuit on the display substrate.

98. Mounting a Si IC chip on the protruding part of the TFT substrate is rarely done because the yield of the Si IC chip mounting process will negatively affect the yield of the LCD panel. As a result, COF, TCP, and TAB mounting are preferred methods of mounting. In addition, Reiner does not show a protruding substrate, so that mounting of the Si IC chip on the TFT substrate is not an option.

99. Further, a POSITA would *not* mount an integrated circuit formed on its own separate substrate, onto a display substrate. A gate/scan line driving circuit implemented in a silicon integrated circuit chip would not fit within the 4-5 micron vertical gap between the display substrate and the counter substrate. And if a POSITA were to arrange a gate/scan line driver directly on the display substrate, Reiner's integrated circuit ESD protection network for source driver 61 would necessarily be different at least because there would be no need to include contact pads 72 (output contacts of the silicon integrated circuit device, no longer needed if arranging a scanning line driving circuit on the display substrate) or the ESD devices *tied to* those contact pads (ESD1, ESD2).

100. As a result of the above considerations, a POSITA would not employ a Si IC chip, as disclosed by Reiner, for a scanning line driving circuit. As discussed above, the number of scanning line connections would be prohibitively

high and could be reduced to just a handful of connections by employing a TFT-based scanning line driving circuit.

6. *Claim 9*

101. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner renders obvious claim 9.

7. *Claim 10*

102. The Petition fails to show that Reiner discloses or renders obvious “an input terminal connected to the power supply line to supply power” or “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, as I discuss above. Therefore, the Petition fails to show that Reiner renders obvious claim 10.

8. *Claim 11*

103. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner renders obvious claim 11.

9. Claim 12

104. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner renders obvious claim 12.

10. Claim 13

105. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner renders obvious claim 13.

11. Claim 14

106. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner renders obvious claim 14.

107. Reiner also fails to render obvious the additional limitations of claim 14, for the same reasons that it fails to render obvious the additional limitations of claim 8.

12. Claim 15

108. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner renders obvious claim 15.

13. Claim 16

109. The Petition fails to show that Reiner discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first protection circuit and a second protection circuit that are connected . . . to the scanning line drive circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.” I discuss these opinions above. Therefore, the Petition fails to show that Reiner renders obvious claim 16.

14. Claim 17

110. The Petition fails to show that Reiner discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first

protection circuit and a second protection circuit that are connected . . . to the scanning line drive circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.” I discuss these opinions above. Therefore, the Petition fails to show that Reiner renders obvious claim 17.

15. Claim 18

111. The Petition fails to show that Reiner discloses or renders obvious “an input terminal connected to the power supply line to supply power” or “a first protection circuit and a second protection circuit that are connected to . . . the scanning line drive circuit” and arranged relative to the scanning line driving

circuit and power supply line as claimed. I discuss these opinions above.

Therefore, the Petition fails to show that Reiner renders obvious claim 18.

16. Claim 1

112. The Petition fails to show that Reiner discloses or renders obvious “an input terminal connected to the power supply line to supply power,” or “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” and arranged relative to the scanning line driving circuit and power supply line as claimed, or a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal,” or “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” I discuss these opinions above. Therefore, the Petition fails to show that Reiner renders obvious claim 1.

17. Claim 2

113. The Petition fails to show that Reiner renders obvious the display device as set forth in claim 1 and, thus, fails to show that Reiner renders obvious claim 2.

114. Reiner also fails to render obvious the additional limitations of claim 2, for the same reasons that it fails to render obvious the additional limitations of claim 8.

18. Claim 3

115. The Petition fails to show that Reiner discloses or renders obvious the display device as set forth in claim 1 and, thus, fails to show that Reiner discloses claim 3.

VII. ANALYSIS OF TAKHARA (GROUND 2)

A. Overview of Takahara

116. Takahara relates to methods for manufacturing an electro-optical device, such as an LCD device, that employs an “element-substrate device, such as an active-matrix-substrate device” that is formed on an insulating material such as glass. Ex. 1007, [0001], [0003].

117. Takahara addresses a different problem than the ’157 patent, and relevant here, discloses a conventional ESD protection layout where protection circuits are located on signal lines between input terminals and a scanning line driving circuit to protect the scanning line driving circuit from ESD events that could enter the scanning line driving circuit via signal lines.

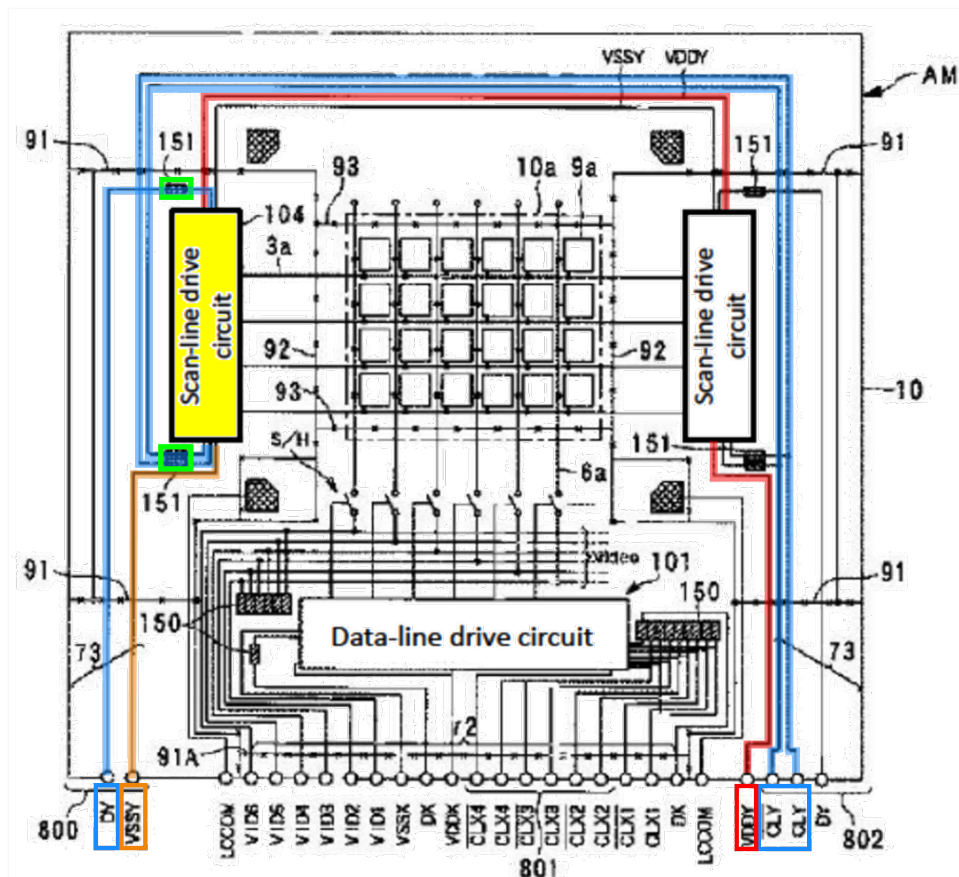
118. First, unlike the ’157 patent, Takahara is directed to methods to form and cut short-circuit wirings to help diffuse static charges that build up on the

substrate during manufacturing to the outer perimeter of the substrate, to protect the electro-optical device. *Id.*, [0003]-[0004], [0007]-[0011], [0015]. The short-circuit wirings are formed at an early stage of manufacturing—when the scan lines and gate electrodes are formed on the insulating substrate—before the device is operational, and then cut prior to completing the manufacturing process to allow normal operation of the electro-optical device. *Id.*, [0004]-[0005], [0008], [0068], [0070]. The short-circuit wirings electrically connect (1) the scan line wirings, (2) the data line wirings, and (3) the signal wirings that supply a signal for driving scan line and data line driving circuits. *Id.*, [0004], [0012], [0020]-[0021] (describing connecting scan lines to short-circuit wiring), [0022]-[0023] (describing connecting data lines to short-circuit wiring), [0024] (describing connecting signal lines to short-circuit wiring). The short-circuit wirings prevent electrostatic breakdown of the thin-film transistors to which the scan and data lines are connected, and the thin-film transistors in the scan and data line driving circuits, by diffusing static charges that can accumulate on the active matrix substrate to the periphery of the substrate. *Id.*, [0012], [0020]-[0025].

119. Second, unlike the '157 patent, Takahara discloses an active matrix substrate for an LCD device that includes data and scan line driving circuits with ESD protection circuits formed on signal wirings that are located, like in the “conventional art” on which the '157 patent expressly improves, between the

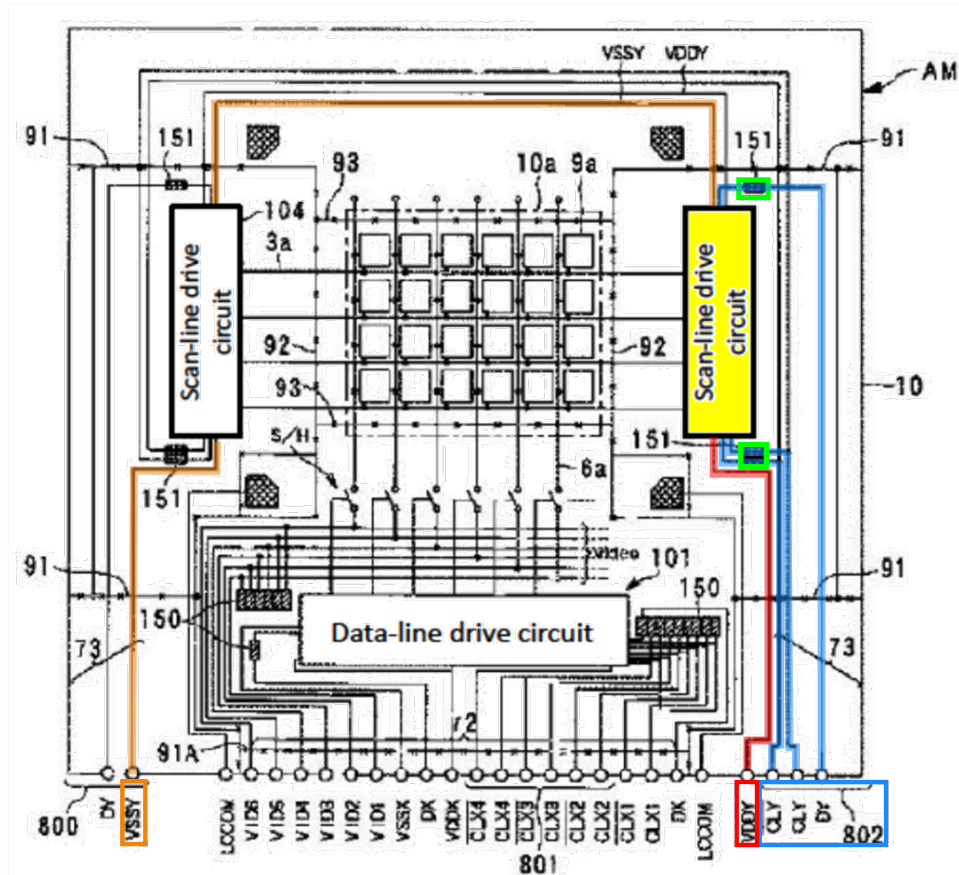
wiring input terminals and the driving circuits those protection circuits are intended to protect from ESD events. *See also*, Ex. 2008 (Murphy Dep.), 153:19-156:14 (agreeing that Takahara discloses protection circuits connected to signal wirings between input terminals and driving circuits). Specifically, Takahara discloses an active matrix substrate for an LCD device that includes data and scan line driving circuits. Ex. 1007, [0059]. Takahara discloses scan line driving circuits 104 that are arranged along both sides of the image display region 10a and driven by signal wirings DY (start signal), CLY (clock signal), and CLY bar (inverted clock signal), and connected to power supply lines VDDY and VSSY. *Id.*, [0062]-[0065]. Takahara discloses electrostatic protection circuits 150 and 151 that are formed at intermediate locations of the signal wirings (in Fig. 1, on lines DY, CLY, and CLY bar) to prevent static electricity from entering the scan line driving circuits via the signal wirings. *Id.*, [0066].

120. As shown below, the scanning line driving circuit on the left of Fig. 1 (yellow), is connected to signal lines DY, CLY bar, and CLY (highlighted in blue) and power supply lines VDDY (highlighted in orange) and VSSY (highlighted in red), and protection circuits 151 (green boxes) are located on the signal lines between the input terminals (blue boxes) and where the signal lines connect to the scanning line driving circuit.



Id., Fig. 1 (annotations added).

121. Similarly, as shown below, the scanning line driving circuit on the right of Fig. 1 (highlighted in yellow), is connected to signal lines DY, CLY bar, and CLY (highlighted in blue) and power supply lines VDDY (highlighted in orange) and VSSY (highlighted in red), and protection circuits 151 (green boxes) are located on the signal lines between the input terminals (blue boxes) and where the signal lines connect to the scanning line driving circuit.



Id., Fig. 1 (annotations added).

122. In my opinion Takahara discloses a conventional arrangement of protection circuits connected between input terminals and a scanning line driving circuit, and those protection circuits are also not formed on or connected to the power supply lines, VDDY and VSSY, that are connected to the scanning line driving circuits. *Id.*, [0061]-[0066]; *see also* Ex. 1001, 1:33-2:30 (discussing the conventional ESD protection layout for a driving circuit built in to an active matrix substrate using polysilicon TFTs where the ESD protection circuits ESD1 to ESD4 are located between input terminals and the driving circuit), Fig. 11 (illustrating the

same); § V.A, *supra*; *see also* Ex. 2008 (Murphy Dep.), 153:19-156:14 (testifying that the ESD protection circuits 151 are connected to signal lines DY, CLY, and CLY bar between the input terminals for those signal lines and Takahara's scanning line driving circuits).

B. The teachings of Reiner in view of Takahara do not disclose or render obvious all elements of claims 1-18 of the '157 patent

1. Claim 4

a. "an input terminal connected to the power supply line to supply power" (claim 4[c])

123. In my opinion, as I discuss above, Reiner fails to disclose or render obvious a display device comprising "an input terminal connected to the power supply line to supply power." Ex. 1001, claim 4[c]. Reiner and likewise Reiner in view of Takahara at most render obvious input terminals connected to Reiner's lines Vdd and Vss, and those input terminals would be input terminals *of integrated circuit driver 61*. Reiner's arrangement discloses drivers formed on silicon substrates, separate from the display substrate. I discuss these opinions above. Thus, the Petition's suggestion that Takahara would render obvious adding input terminals to Reiner's driver 61 would not render obvious input terminals *of the display device*.

- b. “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f])*

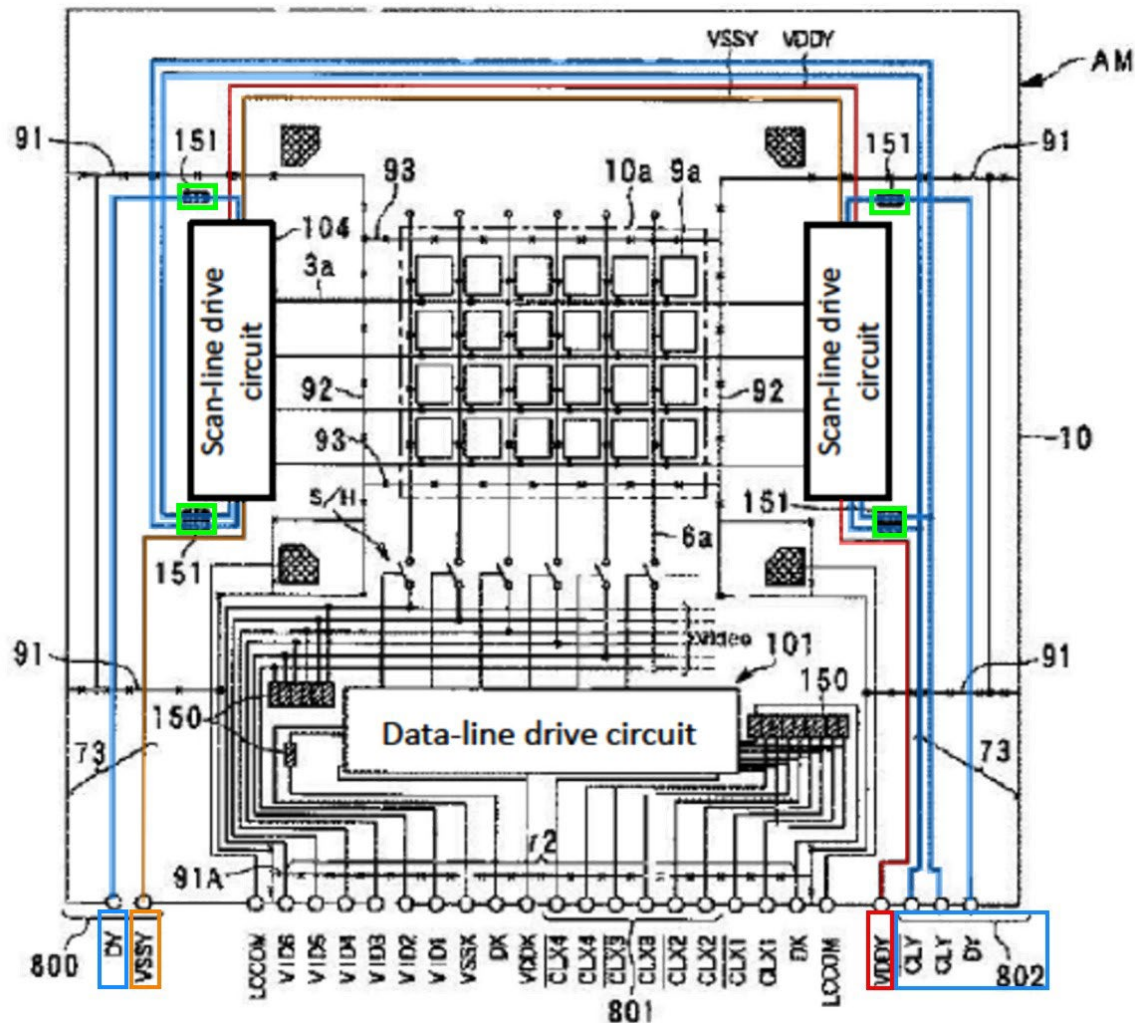
124. As I discuss above, Reiner does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.” In my opinion, Takahara does not close this gap, and the Petition and Dr. Murphy do not argue otherwise.

125. Dr. Murphy asserts that Takahara discloses ESD protection circuits 151 formed on signal lines 73, which “include power lines VDDY and VSSY,” and that VDDY and VSSY “are shorted to” protection circuits 151 via short-circuit wirings 91 as shown by the ‘x’ on lines 91 between the wiring lines. Ex. 1003, ¶235. Dr. Murphy misrepresents Takahara. Takahara does not disclose two protection circuits connected to a power supply line, nor does Takahara disclose a scanning line driving circuit connected to that power supply line between those protection circuits.

126. First, Dr. Murphy cites no evidence showing that Takahara's signal lines 73 include power supplies VDDY and VSSY. Indeed, Takahara's disclosure states otherwise. Takahara's disclosure expressly distinguishes between power supply lines and signal lines. Signal lines "supply the signals for driving the scan-line drive circuits or the data-line drive circuit"—supplying a signal is different than supplying power. Ex. 1007, [0024]-[0025]; Ex. 2001 ¶89. In fact, Takahara provides that signal lines include "a start signal DY, a clock signal CLY, and an inverted-clock signal CLY bar," and "the scan-line drive circuits 104 are driven in accordance with these signals." Ex. 1007, [0061]; *see also id.*, [0060] (explaining that other signal lines include "image signals VID1-VID6" and "a start signal DX, clock signals CLX1-CLX4, and inverted-clock signals CLX1 bar to CLX4 bar" and "the data-line drive circuit 101 is driven in accordance with these signals"). Takahara does not include power lines in its discussions of signal lines. Accordingly, in my opinion, Takahara does not disclose protection circuits connected to the power supply lines that supply power to scan and data line driving circuits.

127. Indeed, Figure 1 shows that **electrostatic-protection circuits 151** are formed only at intermediate locations of the **clock signal lines and start signal lines** (DY, CLY, CLY bar) that drive the scan-line driving circuit 104; they are not

[0061], [0065].



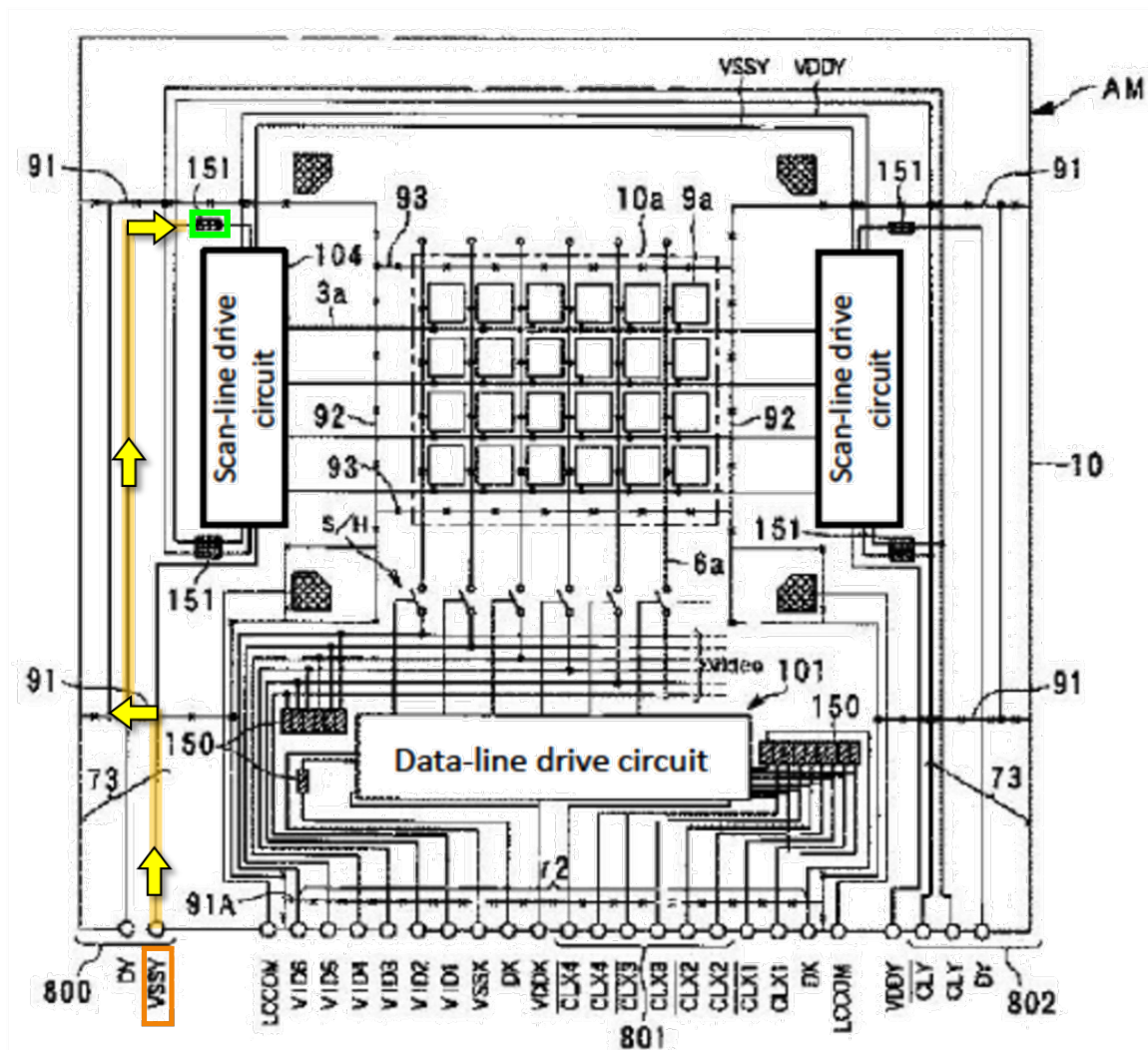
Id., Fig. 1. (annotations added).

Id., [0060] (signals that drive the scan line driving circuit, [0061] (signals that drive the data line driving circuit)). Further, the “signal wirings” 73 shown in

Figure 1 are “for driving the scan-line drive circuits 104” which are “routed from” terminals 800 and 802. *Id.*, [0065]. The annotations identifying signal lines 73 and terminals 802 on the right side of Figure 1 include only CLY bar, CLY, and DY signal wirings and terminals, which confirms that the annotations identifying signal lines 73 and terminal 800 on the left side of Figure 1 apply only to the DY signal wiring.

129. Second, recognizing that Figure 1 does not show that any ESD protection circuit is formed on VDDY or VSSY, Dr. Murphy suggests that Takahara connects the power lines to protection circuits *formed on other lines* (signal lines), through short-circuit wirings 91. Ex. 1003, ¶¶235-236. I disagree—Takahara does not disclose that the short-circuit wirings connect the power lines to the signal lines; instead, the short-circuit wirings electrically connect (1) the scan line wirings, (2) the data line wirings, and (3) the signal wirings that supply a signal for driving scan line and data line driving circuits. Ex. 1007, [0004], [0012], [0020]-[0021] (describing connecting scan lines to short-circuit wiring), [0022]-[0023] (describing connecting data lines to short-circuit wiring), [0024] (describing connecting signal lines to short-circuit wiring), Fig. 4 (showing plan view showing layout, and connection via contact holes 403, between a signal wiring 72 and a first short-circuit wiring 91).

130. The purpose of Takahara's short-circuit wirings also contradicts Dr. Murphy's position. Dr. Murphy suggests that Takahara's short-circuit wirings serve the purpose of diffusing static electricity on the perimeter of the substrate toward the center so that it is absorbed by ESD protection circuits 151. Ex. 1003, ¶¶235-236; Ex. 2008 (Murphy Dep.), 159:14-160:1. For example, as shown below, Dr. Murphy suggests an ESD event (depicted with yellow arrows) that enters the VSSY input terminal (orange box) would enter the short-circuit wiring 91 (via a connection *Takahara* does not disclose), travel outwards on short-circuit wiring 91, then enter and travel up signal line DY, and then travel back toward the *center* of the substrate before being absorbed by ESD protection circuit 151 formed on the DY signal line (green box).

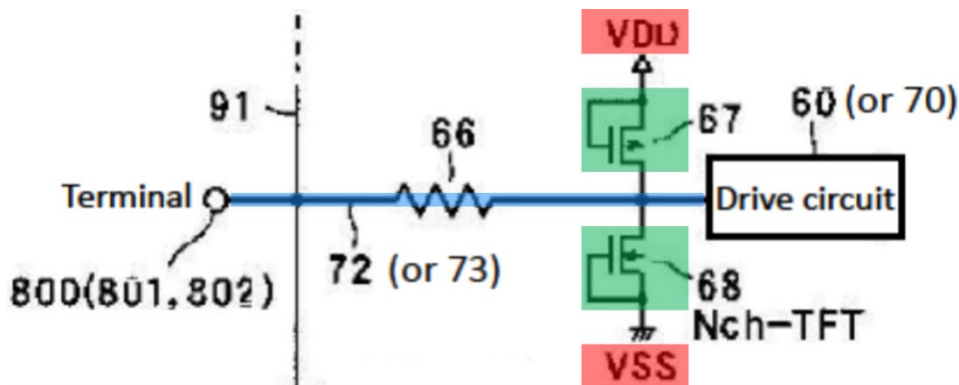


Takahara, Fig. 1 (annotations added); *see also* Ex. 1003, ¶236 (Dr. Murphy's annotations to Takahara Fig. 1). Dr. Murphy envisions that an ESD pulse propagates along the path indicated by the yellow arrows shown in the figure above. But, based on my review of Takahara, that path of propagation crosses an "x" point where the short circuit wiring (91) is cut. A cut wiring would prevent an ESD pulse from propagating.

131. Moreover, in my opinion, Takahara discloses the opposite of what Dr. Murphy suggests: the purpose of the short-circuit wirings is to diffuse static electricity “toward an outer perimeter of the substrate via said short-circuit wiring” to prevent static electricity from flowing through circuits on the substrate, such as the scanning line driving circuit. Ex. 1007, [0004].

132. Furthermore, in my opinion, Figure 3 does not show that Takahara’s protection circuits are connected to a power supply line that supplies power to the scanning line driving circuit. The “positive power supplies VDD and negative power supplies VSS” that Takahara describes are connected to TFTs that are part of ESD protection circuit 150 or 151, as illustrated in Fig. 3, are not “the power supply line” (VSSY and VDDY) to which the scanning line driving circuit is connected. Instead, in my opinion, which I understand Dr. Murphy agrees with, Takahara discloses an ESD protection circuit layout where the power supplies VDD and VSS that are connected to ESD protection circuits 150 or 151 serve as reference potential lines that limit the potential of the current on signal lines 72 or 73 that can pass through the ESD protection circuit 150 or 151. Ex. 1007, [0066], Fig. 3; Ex. 2008 (Murphy Dep.), 152:8-22 (agreeing that serving as reference potentials is “one of the functions that VDD and VSS are performing here in the context of Figure 3” and testifying this is “one way to describe how that ESD protection works” without identifying any other functions served by VDD and VSS

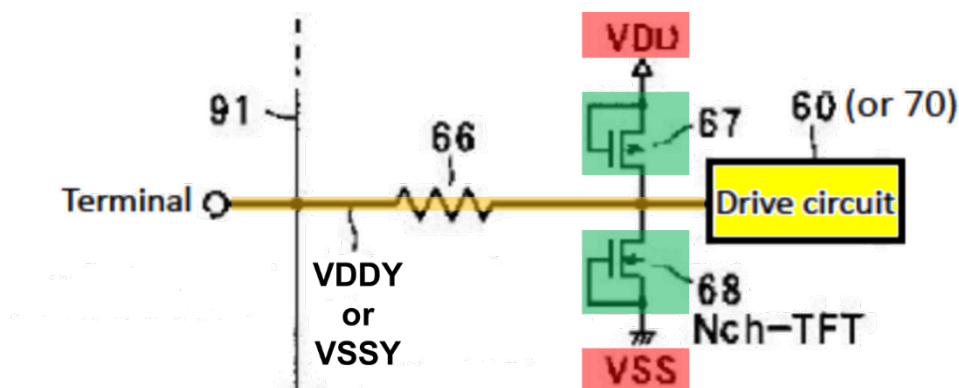
in the context of Figure 3). Specifically, as shown below, Takahara describes and illustrates in Fig. 3 a P-channel TFT 67 and N-channel TFT 68 (highlighted in green) in a push-pull layout where the drain electrode of each TFT is connected to signal wiring 72 or 73 (highlighted in blue), and source and gate electrodes are connected, respectively, to power supplies VDD and VSS (highlighted in red).



Ex. 1007, Fig. 3 (excerpt) (annotations added).

133. As Takahara explains, the push-pull layout of TFTs 67 and 68 forms a diode between VDD and VSS, *id.*, [0066], which functions to limit the potential on signal lines 72 or 73 (i.e., signal lines DY, CLY, or CLY bar) to not greater than the potential on VDD and not less than the potential on VSS. In other words, if an ESD event that enters signal lines 72 or 73 (via the terminals 800-802 or short-circuit wiring 91) causes the voltage on the line to exceed the positive potential on VDD or negative potential on VSS, the ESD protection circuit activates and the excess current flows through VDD or VSS instead of entering and damaging the driving circuit. Ex. 1007, [0066].

134. To reiterate, in my opinion, the VDD and VSS power supplies shown in Figure 3 are not the power supply lines for the scanning line driving circuit (VDDY and VSSY). Takahara's ESD protection circuit layout protects against ESD events that occur on signal lines 72 or 73, not any power line, and the power supplies VDD and VSS are connected to limit the potential on the signal lines and provide a discharge path for excess potentials. Power supplies VDD and VSS are not the same as Takahara's VDDY and VSSY power supply lines that are connected to the scanning line driving circuit. For example, as I show below in a hypothetical version of Fig. 3, if Takahara disclosed an ESD protection circuit located on VDDY or VSSY (highlighted in orange), the TFTs 67 and 68 (highlighted in green) would still need to be connected to power supply lines VDD and VSS (highlighted in red) in order to limit the potential on the power line the protection circuit is located on, VDDY or VSSY, and provide a discharge path for excess charges that would otherwise enter damage the scanning line driving circuit (highlighted in yellow) via power supply line VDDY or VSSY.



Ex. 1007, Fig. 3 (excerpt) (annotations and “VDDY or VSSY” label added).

135. Notably, the description and layout of the ESD protection circuit in Takahara is essentially identical to the protection circuit layout described in the ’157 patent and illustrated in Fig. 4. Ex. 1001, 6:3-23, Fig. 4 (describing a p- and n-type transistor connected to the wiring line being protected with source and gate electrodes connected to, respectively, a high potential and low potential power source VH and VL to limit “a signal level given to the wiring line being protected” to “not more than VH and not less than VL” such that when the potential is out of that range, the circuit activates and “abnormal current runs through a reference potential VH line or a reference potential VL line.”). In my opinion, a POSITA would not understand the reference potential power supply lines (VDD/VDDY in Takahara; VH/VL in the ’157 patent) that are connected to the transistors in this ESD protection circuit layout to refer to “the power supply line” to which the first and second protection circuits are “connected” to “protect the scanning line driving circuit” as claimed. *See also* Ex. 2008 (Murphy Dep.), 152:8-22.

136. As I discuss above, Takahara discloses one protection circuit disposed on a signal line, between the signal line’s input terminal and the signal line’s connection to the scanning line driving circuit. Like Reiner, Takahara does not disclose a scanning line driving circuit connected to a power supply line between

two protection circuits. Dr. Murphy does not argue otherwise. Ex. 1003, ¶234-236; Ex. 2008 (Murphy Dep.), 152:8-22.

137. Accordingly, in my opinion, Reiner in view of Takahara does not render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.”

c. A POSITA would not have been motivated to combine Reiner and Takahara.

138. The Petition and Dr. Murphy assert that a POSITA would have been motivated “to provide a first and second protection circuit connected to the gate driver 63 to protect against ESD events and damage and also connected to the power supply lines that can be lines that are subject to ESD events.” Pet., 78-80; *see* Ex. 1003, ¶237. But Dr. Murphy and the Petition both cite to Takahara for only the general proposition that driving circuits can be protected by ESD protection circuits to prevent damage to circuitry inside driving circuits. Ex. 1003, ¶237-241 (citing Takahara’s disclosures at Ex. 1007, [0063], [0066], Figs. 1, 3); Pet., 78-80 (same). As I discuss above, Reiner does not disclose or render obvious the claimed protection circuit arrangement. Dr. Murphy does not assert that Takahara’s disclosures would motivate a POSITA to close those gaps. Ex. 1003, ¶237-241.

139. In my opinion, a POSITA would have no reason to modify Reiner in view of Takahara. Reiner provides an ESD protection network for silicon integrated circuits. Takahara provides protection circuits for signal lines and a short-circuit wiring to protect its panel. The Petition cites no need to combine the teachings of Reiner and Takahara. Furthermore, in my opinion, a POSITA would not combine Reiner and Takahara for at least two additional reasons.

140. First, Reiner concerns a source/data line driving circuit, whereas Takahara concerns a scanning line driving circuit. As I discuss above regarding Reiner, the two circuits are fundamentally different. For example, source/data line driving unit circuits operate independently from one another, whereas scanning line driving unit circuits operate in a coupled manner to implement the functionality of a shift register. Furthermore, source/data line driving circuits provide an analog signal whereas scanning line driving circuits provide a two-state ON/OFF signal that switches the pixel TFTs ON and OFF. Second, Reiner and Takahara are directed to two fundamentally different ways to implement driving circuits for display devices. Reiner discloses a silicon integrated circuit source driver chip located off the display substrate, as I discuss above in § VI, whereas Takahara, as I discuss above, discloses a scanning line driving circuit that is located, and formed on, the display substrate.

2. *Claims 5-7, 9*

141. The Petition fails to show that Reiner in view of Takahara renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner in view of Takahara renders obvious claims 5-7 or 9.

3. *Claim 8*

142. The Petition fails to show that Reiner in view of Takahara renders obvious the display device as set forth in claim 4 and, thus, fails to show that Reiner in view of Takahara renders obvious claim 8.

143. Further, in my opinion, even though Takahara teaches forming a scanning line driving circuit on the display substrate, a POSITA would not have been motivated to form Reiner's integrated circuit drivers 61 and 63 on a display substrate. § VI.B.5, *supra*.

4. *Claim 10*

144. The Petition fails to show that Reiner in view of Takahara renders obvious "an input terminal connected to the power supply line to supply power" and, thus, fails to show that Reiner in view of Takahara renders obvious claim 10. § VI.B.1.a, *supra*.

5. *Claims 11-15*

145. The Petition fails to show that Reiner in view of Takahara renders obvious the display device as set forth in claim 10 and, thus, fails to show that Reiner in view of Takahara renders obvious claims 11-15.

146. Further, even though Takahara teaches forming a scanning line driving circuit on the display substrate, a POSITA would not have been motivated to form Reiner's integrated circuit drivers 61 and 63 on a display substrate. § VI.B.5, *supra*.

6. *Claim 16*

147. The Petition fails to show that Reiner in view of Takahara renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit” and, therefore, fails to show that Reiner in view of Takahara renders obvious claim 16. I discuss these opinions above.

7. *Claim 17*

148. The Petition fails to show that Reiner in view of Takahara renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit” and, therefore, fails to show that Reiner in view of Takahara renders obvious claim 16. I discuss these opinions above.

8. *Claim 18*

149. The Petition fails to show that Reiner in view of Takahara renders obvious “an input terminal connected to the power supply line to supply power” and, thus, fails to show that Reiner in view of Takahara renders obvious claim 18. I discuss these opinions above.

9. *Claim 1*

150. The Petition fails to show that Reiner in view of Takahara renders obvious “an input terminal connected to the power supply line to supply power” and “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and

the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” and, thus, fails to show that Reiner in view of Takahara renders obvious claim 1. I discuss these opinions above.

10. Claims 2-3

151. The Petition fails to show that Reiner in view of Takahara renders obvious the display device as set forth in claim 1 and, thus, fails to show that Reiner in view of Takahara renders obvious claims 2-3.

152. Further, for the same reasons that Reiner in view of Takahara does not render obvious claim 8, the combination does not render obvious claim 2.

VIII. ADDITIONAL REMARKS

153. I reserve any right that I may have to supplement this declaration if further information becomes available or if I am asked to consider additional information. Furthermore, I reserve any right that I may have to consider and comment on any additional expert statements and testimony of Petitioner’s expert in this matter.

154. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or

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both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: March 14, 2025



E. Fred Schubert, Ph.D.