

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case IPR2024-00973
Patent No. 9,184,157

PETITIONER'S REPLY

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I. Introduction

Patent Owner's Response (Paper 17, "POR") fails to rebut the Petition's (Paper 1, "Pet.") showing that claims 1-18 are unpatentable.

II. Patent Owner's POSITA Definition Is Flawed, but If Accepted, Confirms the Claims Are Obvious

Patent Owner's proposed POSITA is similar to Petitioner's, but adds two additional years of experience for a bachelor's and master's degree, and one year's experience for a Ph.D. POR 14-15; Pet. 15-16. Dr. Murphy qualifies as a POSITA under Patent Owner's definition and is qualified to opine on unpatentability. Ex. 1024 ("Murphy II") ¶¶10, 15-20; *Osseo Imaging, LLC v. Planmeca USA Inc.*, 116 F.4th 1335, 1340-41 (Fed. Cir. 2024). Dr. Murphy confirms claims 1-18 would have been obvious under either definition. Murphy II ¶¶20-114.

III. Patent Owner Fails to Rebut the Petition's Showing that *Reiner* Renders Obvious Claims 1-18 (Ground 1)

A. *Reiner* Renders Obvious Claim 4

1. *Reiner* Suggests or Renders Obvious the Claimed Input Terminals ([4c])

Patent Owner acknowledges *Reiner*'s Vdd/Vss terminals "would be input terminals for [an] integrated driver circuit" (scanning line driving circuit) and does not dispute that *Reiner*'s input terminals would be (or would obviously be) positioned as in Figures Ax, Bx, and Cx to power the scanning line driver (as

claimed). *See* POR 22-24. This is all that is required. Nor also has Patent Owner refuted the Board's findings in the Institution Decision. *See* Paper 9 ("D.I.") 19-28.

Patent Owner instead argues that the "input terminals for *Reiner*'s source driver 61 would *not* be input terminals for a display device" and "the display device would include *separate* power lines on the display substrate." POR 22.¹ This argument turns on the faulty premise that "display device" means only the LCD pixels, not the scanning line driving circuits. POR 22-24.

The claim does not recite LCD pixels or powering them with the claimed power supply lines that supply power to the scanning line driving circuit. *See* Ex. 1001, claim 4.² *Reiner* discloses or renders obvious [4c]. *Reiner*, 8:8-9:22;³ Pet.

¹ Patent Owner's position requires the preamble be limiting, but failed to establish those requirements. Regardless, *Reiner* discloses or renders obvious [4c]. Pet. 21-24.

² During prosecution, the applicant distinguished the claims to ***exclude*** pixels. Ex. 1002, 182 ("[T]he pixels of Lee cannot reasonably be considered to correspond to the claimed semiconductor circuit."), 207-212 (amending claims to recite "scanning line driving circuit").

³ *Reiner* citations are to Exhibit page numbers ("Page x of y") in the bottom corner.

21-24; D.I. 18-19 (“Reiner expressly discloses its integrated circuit device 30 is powered by a low voltage power supply line Vss and a high voltage power supply line Vdd” (citing *Reiner*, 8:8-9:10, FIG. 3)). The ’157 patent does not discuss “input terminals” powering the display pixels, and Patent Owner’s description of the “invention” shows power-line terminals for only the driver circuits. POR 8-9; *generally* Ex. 1001.

Patent Owner argues that “[n]othing in *Reiner* suggests that lines Vss and Vdd also supply power to the LCD display 60.” POR 23. This misidentifies “LCD display 60.” *Reiner*’s FIG. 4 shows “a block diagram of a *display with display drivers*,” of which “LCD *screen 60*” is a part along with driver circuits 61, 63. *Reiner*, 6:7, 9:23-29 (emphases added); Murphy II ¶¶24-25.

2. *Reiner* Discloses or Renders Obvious the Claimed First and Second Protection Circuits Connected to a Scanning Line Driving Circuit ([4d]-[4f])

Patent Owner argues that “*Reiner* does not disclose protection circuits connected to a scanning line driving circuit” and “*Reiner* discloses ... only an ESD protection network within a source (data line) driver IC chip.” POR 24 (citing

D.I. 32-33).⁴ Patent Owner also alleges, contrary to the D.I.'s findings, that *Reiner* does not render obvious applying ESD protection to a scanning line driver circuit. POR 24; D.I. 33-37. Patent Owner is incorrect; *Reiner* discloses or at least renders this obvious. Pet. 24-40 ([4d]-[4f]).

Patent Owner alleges that “[d]ifferences between a source driver and a gate (scan line) driver would require changes to *Reiner*’s ESD protection network.” POR 24. The Board already rejected similar arguments. D.I. 36-37. Importantly, Patent Owner does not identify any alleged “[d]ifferences” that are material to the ’157 patent’s claims. Many of Patent Owner’s “[d]ifferences” actually highlight the *similarities* between source drivers and gate drivers that confirm obviousness. *Murphy II* ¶¶37-39.

Patent Owner’s assertion that “*Reiner*’s disclosure that the gate driver integrated circuit comprises individual gate drivers, not output devices 70,” actually supports *Reiner* teaching or rendering obvious claim 4. POR 24-25 (citing *Reiner*, 9:20-31). Because *Reiner* discloses individual gate driver units—one

⁴ Patent Owner’s argument that “[n]o evidence” supports using *Reiner*’s ESD protection network to protect a scanning line driving circuit (POR 24) fails for the same reasons discussed here.

circuit device for driving each gate line—a POSITA would have understood FIG. 5 would apply to both gate drivers and source drivers because both have per-line driver units (70) to be protected. *Reiner*, 9:11-15, 9:26-28, 10:1-23, FIG. 5; Murphy II ¶¶40-42.⁵ *Reiner*'s "ESD protection network" in FIG. 5 protects individual line drivers, and its "invention" protecting "integrated circuits" with "ESD protection" ("integrated circuits" includes **both** gate and source drivers) only strengthens the obviousness of using *Reiner*'s ESD protection network to protect scan line driver units. *Reiner*, 3:4-8, 4:15-16, 8:8-10, 9:11-22, FIG. 5; Murphy II ¶41.

Patent Owner alleges "differences between the gate driver arrangement and the source driver arrangement," such as "individual gate/scan line drivers are coupled to one another" (POR 25), but fails to explain why an unclaimed signal line matters for protecting the driver circuit using ESD protection connected to the **power lines**. As Dr. Murphy explains, *Reiner*'s ESD1-ESD3 protect any circuitry inside the driver units 70 because they are rendered as a generic driver box, so whether those driver circuits 70 have **other unclaimed** lines between the units 70

⁵ The '157 patent confirms it was "conventional" to use individual per-line scanning line driver units. Ex. 1001, 1:57-2:4, FIG. 11 (items 801-*n*).

does not change the protection provided. Ex. 1003 (“Murphy”) ¶111; Murphy II ¶¶42-43; *Reiner*, 4:15-16, 9:11-22, FIG. 5. But identifying an immaterial difference does not rebut obviousness. A POSITA would not view the signal line as meaningful when finding it obvious to use *Reiner*’s ESD protection network to protect a scan line driver circuit. Murphy II ¶44. The ’157 patent treats signal and power lines as distinct (*see* Ex. 1001, FIGS. 1-2, 11) for protection purposes, and claim 4 relates to only the power lines.

Patent Owner’s argument that “[n]o evidence shows that the gate driver would include an ESD protection network identical to the source driver’s network” (POR 24) fares no better. Initially, it misunderstands obviousness law because obviousness does not require express disclosure. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415, 421 (2007) (POSITA is “a person of ordinary creativity, not an automaton”); *Bell Semiconductor LLC v. NXP B.V.*, 2024 WL 4984053, at *2 (Fed. Cir. Dec. 5, 2024) (“suggest[ion]” of applying printed circuit board teaching to integrated circuits rendered obvious claimed integrated circuits); *In re Sovish*, 769 F.2d 738, 742-43 (Fed. Cir. 1985) (rejecting argument that POSITA would not make combination because it “presume[d] stupidity rather than skill”). *Reiner* supports obviousness because its “invention relates to integrated circuit devices with ESD protection,” and “typical example[s]” of “integrated circuit devices”

include **both** “display driver 61 [source/data driver] or 63 [gate/scan line driver].” *Reiner*, 2:1-3, 9:11-15; Murphy Tr. 101:2-103:16; Murphy ¶¶103-133. This is sufficient for a POSITA to understand *Reiner* describing (or at least rendering obvious) protecting the gate driver with ESD protection like in FIG. 5. Murphy ¶¶103-133. *Reiner*’s further teaching “to prevent the very sensitive [driver] circuits ... from being destroyed” by ESD applies equally to both source/data drivers and gate/scan line drivers because it is undisputed that *Reiner*’s FIG. 5 protects whatever circuit is inside box 70. *Reiner* 2:28-3:3; Murphy ¶111; Ex. 1018 (“Schubert Tr.”), 54:15-55:11.⁶

Patent Owner alleges three reasons would have made the claims nonobvious (POR 25-26), but these merely recycle the same arguments refuted above.

Patent Owner’s “[f]irst” and “[s]econd” arguments that gate and source drivers have different structures (POR 25-26) does not render the claims nonobvious, as explained above. *Reiner*’s ESD protection protects the circuits inside box 70 of FIG. 5, including the connecting signal line. Murphy ¶111;

⁶ Dr. Murphy explained that both drivers comprise transistors and CMOS devices that *Reiner*’s ESD protection network protects. *Reiner* 2:28-3:1; Murphy ¶¶97, 104, 113; Ex. 2008 (“Murphy Tr.”) 47:3-15, 76:14-17.

Murphy II ¶48; *generally* Ex. 2009 (not disputing this protection); D.I. 34-37 (rejecting Patent Owner's same argument); *Reiner*, 2:28-3:1 (protecting "very sensitive circuits" from being "destroyed" by ESD).

Patent Owner's "[s]econd" and "[t]hird" arguments discussing *signals* output from gate and source drivers (POR 25-26) were already rejected by the Board. D.I. 34-37. Neither Patent Owner nor Dr. Schubert addresses the Board's initial findings. Regardless, this just iterates the argument that *Reiner*'s circuitry in box 70 is not identical, and fails for the same reasons. Murphy II ¶¶47-51. But *Reiner* teaches protecting both types of circuits, and the protection network in FIG. 5 protects whatever circuit is in box 70. *See supra*. Source/data driver 61 and gate/scan driver 63 are "typical example[s]" of "integrated circuit[s]" protected by *Reiner*'s ESD protection network. *Reiner*, 9:11-22. This is exactly the type of known technology (FIG. 5's ESD protection network) used to improve another known technology (gate driver 63) in the same way to achieve a predictable result found obvious as a matter of law. *KSR*, 550 U.S. at 416-17.

3. *Reiner* Discloses or Renders Obvious Element [4e]

Patent Owner argues that “the Petition offers no evidence ... that ESD3 is ‘connected to the scanning line driving circuit.’” POR 27.⁷ This is disingenuous because Patent Owner *admits* Petition Figures Cx satisfy the claims if Patent Owner’s construction is adopted. POR 27, 31. Patent Owner “cannot have it both ways” to avoid its own construction in this proceeding while asserting it in district court. Pet. 27-28 (explaining that Figures Cx are under Patent Owner’s construction); *Bristol-Myers Squibb Co. v. Ben Venue Lab ’ys, Inc.*, 246 F.3d 1368, 1376 (Fed. Cir. 2001); *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (patent is not “nose of wax” to “be twisted one way to avoid [invalidity] and another to find infringement”); *White v. Dunbar*, 119 U.S. 47, 51-52 (1886).

The Board regularly considers a patent owner’s constructions, even when the petitioner does not subscribe to them. *10X Genomics, Inc. v. Bio-Rad Lab ’ys, Inc.*, IPR2020-00088, Paper 8, 15-19 (PTAB Apr. 27, 2020) (petitioner may “rely[] on a claim construction that it believes is incorrect, for example, a claim construction relied upon by patent owner in a related district court action”); *Axonics, Inc. v.*

⁷ Patent Owner’s similar argument (POR 31) is improper for the same reasons.

Medtronic, Inc., 75 F.4th 1374, 1380-81 (Fed. Cir. 2023) (requiring Board to consider petitioner's arguments made under patent owner's construction, even though petitioner disagreed); *Parkervision, Inc. v. Vidal*, 88 F.4th 969, 979-80 (Fed. Cir. 2023) (same); *Apple Inc. v. Omni MedSci, Inc.*, No. 2023-1034, 2024 WL 3084509, at *5-6 (Fed. Cir. June 21, 2024) (same).

Regardless, Petition Figures Ax and Bx also show the claimed arrangements. Patent Owner's arguments are based on incorrect constructions.

Patent Owner argues that *Reiner*'s "ESD1 and ESD2 are not connected to the power supply line as claimed" because the first "ESD1 is connected to line Vdd at the same location at which the source driver first connects to line Vdd" and the first ESD2 is connected after the topmost connecting portion of the driving circuit. POR 27-28. Similarly, Patent Owner's argument that [4e] "recites a scanning line driving circuit—the circuit, not intermediate components of the circuit—connected between two protection circuits" (POR 31) reaches an incorrect conclusion.

Patent Owner's arguments rest on the incorrect construction that the "second" and "third" "connecting portion[s]" (first and second protection circuits) must be outside of *all* of the scan line driving circuit's "connecting portion[s]." POR 24-42. But the claims require only "a" single "first connecting portion" connecting the scanning line driving circuit and power line in [4e]-[4f].

Claim 4 is a “comprising” claim and does not exclude other “connecting portion[s].” In claim construction, “a” means “one or more”; claim 4 requires that only “one or more”—not all—“connecting portion[s]” from the scanning line drive circuit to the power line be between the “second” and “third” connecting portions of the protection circuits. *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1371-74 (Fed. Cir. 2005); *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008). Like *Gillette*, where “any blade in between the first and third blades ... is a ‘second’ blade,” and any three blades meeting the relative positions could be the claimed “subset of blades,” 405 F.3d at 1372-73, here any “connecting portion” between the scan line driving circuit and the power line can be “a first connecting portion” when it is between two ESD connecting portions, which Petition Figures Ax and Bx show. *See* Pet. 34-40; Murphy II ¶¶53-56.

Claims 10 and 18 confirm that “a first connecting portion” need only be a connection between *one* scan line driver unit (e.g., one unit 801-*x*) and the power line, not the entire scan line driver (i.e., not all units 801-1 through 801-*n*). Both recite “a first connecting portion *at which [a] circuit element* and the power supply

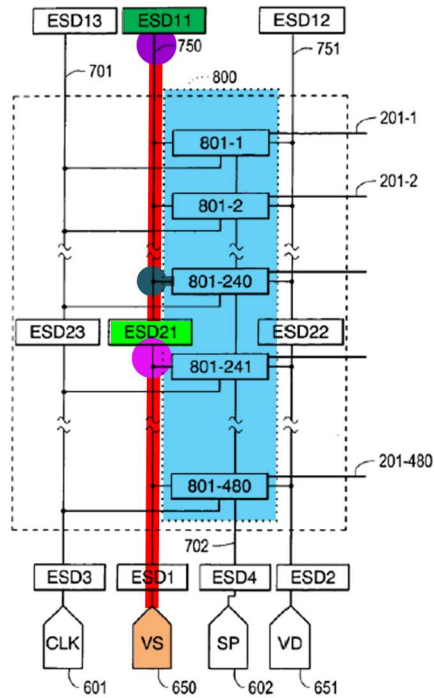
line are connected.” Ex. 1001, 13:19-21, 14:58-60 (emphasis added).⁸ The only “connect[ion]” between the scanning line driving circuit and power line recited in claim 4 is “a first connecting portion” (*id.*, claim 4), which need only be one driver unit’s connection, not all driver units’ connections. This claim term is interpreted the same across all claims. *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001).

Patent Owner incorrectly contends that the Petition’s application of this basic claim construction principle “defeats the purpose of the invention.”⁹ POR 29-31. Figures Ax and Bx align with various embodiments in the ’157 patent that include additional ESD protection circuits in various combinations, as shown in ’157 patent, FIG. 2, annotated below. Murphy II ¶¶57-59. By ignoring embodiments, Patent Owner’s narrow interpretation cannot be correct. *Gillette*, 405 F.3d at 1371-74.

⁸ The “circuit element” is “included in a scanning line driving circuit.” Ex. 1001, 13:6, 14:45.

⁹ Patent Owner’s assertion that the “conventional art” protects “access points” (POR 33-34) misrepresents FIG. 11, which discusses only one ESD protection circuit at the input terminals. Ex. 1001, 1:47-2:32; POR 34-35.

FIG. 2



First protective circuit
Second protective circuit

First connecting portion
Second connecting portion
Third connecting portion

FIG. 2

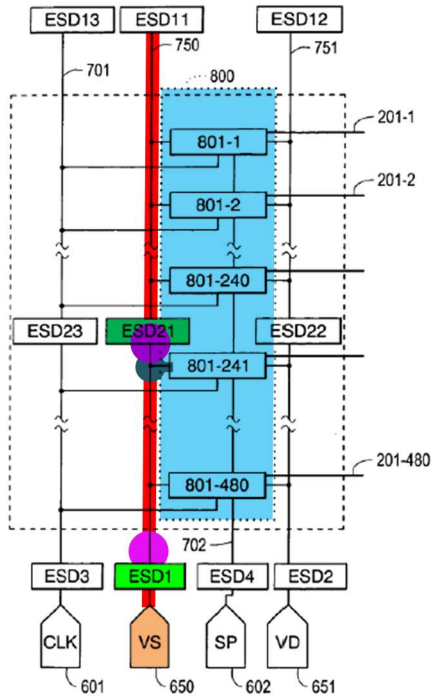
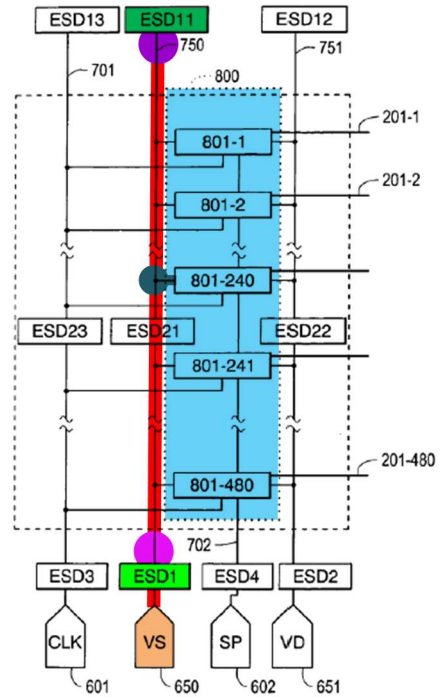


FIG. 2

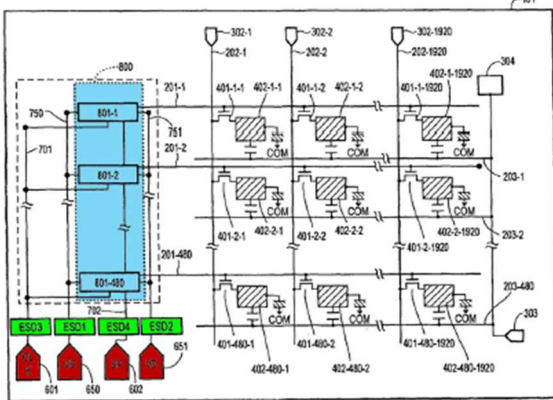


4. *Reiner* Discloses or Renders Obvious Element [4f]

Patent Owner's argument that "*Reiner* describes only ESD protection networks *in* an integrated circuit, it does not disclose a scanning line driving circuit connected to a power supply line ***between first and second protection circuits,***" and that "*Reiner*'s ESD protection network is *inside* its purported scanning line driver, to protect individual output devices 70" (POR 32-33 (second emphasis added)), relies on the same incorrect interpretation refuted above that all scanning line driver connections must be between the two protection circuit connections.

Patent Owner argues that "*Reiner* is the conventional art on which the '157 patent[] improves" to incorrectly suggest that *Reiner*'s numerous ***additional*** ESD1-ESD3 at ***each*** driver unit is somehow the "same" as one ***single*** ESD at the input terminal in FIG. 11. POR 33-35. This contradicts Patent Owner's own admission that *Reiner*'s numerous additional protection circuits "protect individual output devices 70," which highlights *Reiner* disclosing or rendering obvious the purported improvement of the '157 patent—providing additional ESD protection ***away from*** the power line input terminal. POR 32-42; Ex. 1001, 2:51-57, 3:6-17, 7:20-59, FIG. 2.

Patent Owner's own comparison of prior-art FIG. 11 (below left) and *Reiner* (below right) confirms this:

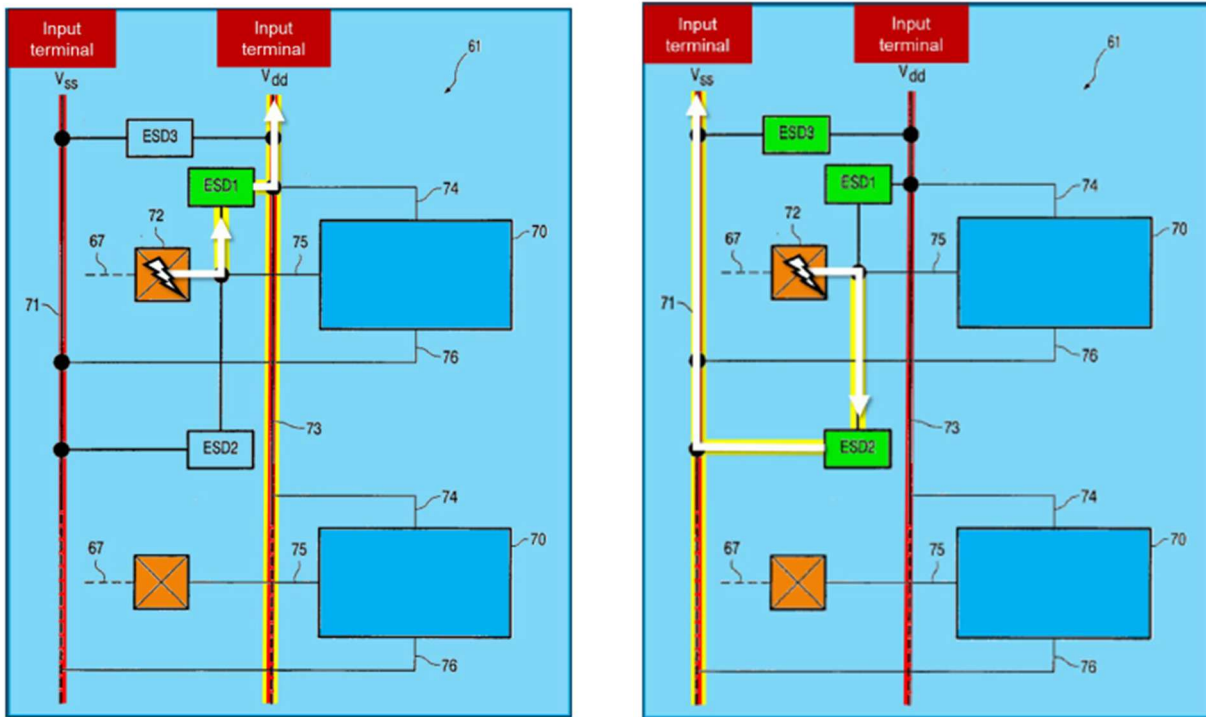


Notwithstanding Patent Owner's facially incorrect argument, Patent Owner *agrees* that *Reiner*'s ESD1 and ESD2 protect the driver circuits 70 at least from electrostatic discharge entering through the signal lines, as Patent Owner's own figures, reproduced below, show.¹² POR 36-39 (ESD1 and ESD2 "protect output device 70 from electrostatic discharge that may enter integrated circuit 61 through contact pad 72" by "shunting the [electrostatic] charge to a ground terminal (not shown in Fig. 5)"). Murphy II ¶¶66-67. That is all claim 4 requires.

"every one individually; each one"); Ex. 1023, 3 (defining "each" as "every").

Murphy II ¶63. Regardless, Petition Figures Ax and Bx do not rely on ESD3, and Patent Owner admits Figures Cx meet the claim language.

¹² Patent Owner's admission that ESD1, ESD2, and ESD3 protect the individual driver units 70 is sufficient to meet the claim language to protect the scanning line driving circuit.



POR 37-38 (annotations by Patent Owner).

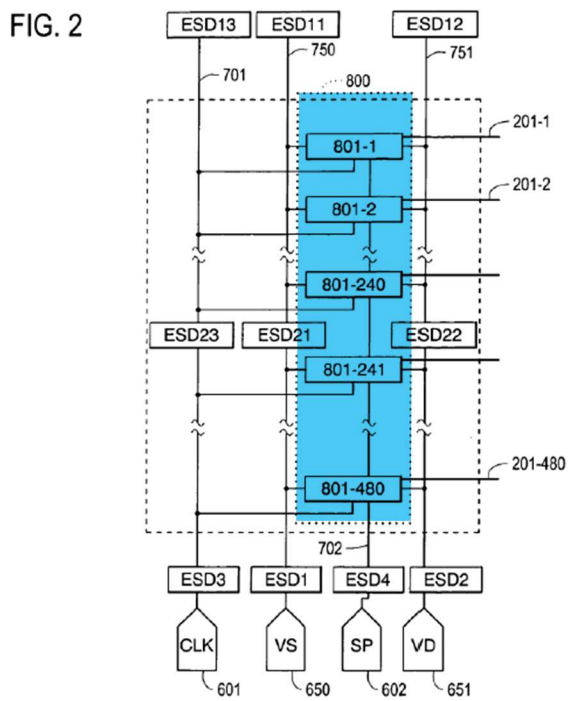
Patent Owner's assertion that *Reiner* does not disclose the claim because "*Reiner*'s ESD devices shown in Fig. 5 are inside integrated circuit source driver 61 between access points" (POR 39-40) is also incorrect.¹³ Patent Owner misstates Dr. Murphy's testimony where he was asked about a "driver *module*." *E.g.*, POR 20-21, 23, 33 (emphasis added). A "driver *module*" may include more than the

¹³ Petitioner disputes Patent Owner's description, but even if Patent Owner is correct, the claims are unpatentable, as discussed here.

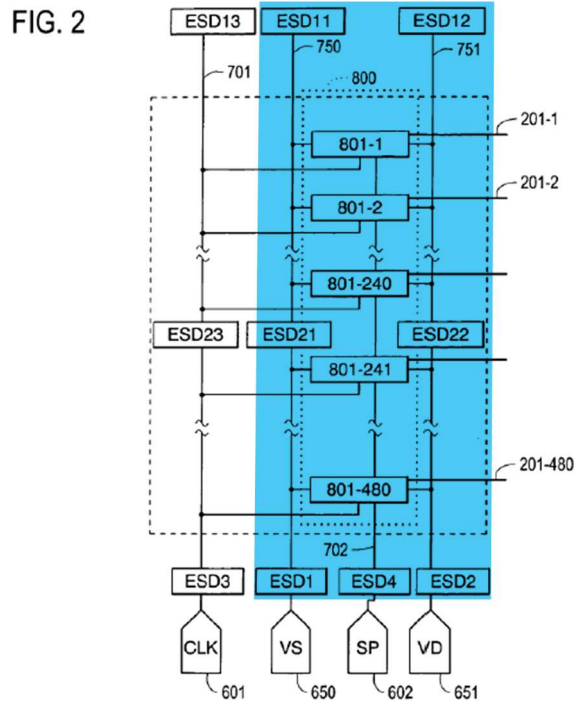
“driving *circuit*” recited in claim 4. A “module” may often include other elements, such as the power lines and ESD1-ESD3 protection circuits, but the “driving *circuit*” (recited in the claims) is the group of driver units 70 of *Reiner*. Murphy II ¶70; Pet. 26-40, Figures Ax-Cx. Each of *Reiner*’s ESD1 and ESD2 is connected to the respective driver units as shown in Figures Ax and Bx. ESD3 is connected to the driver unit as shown in Figures Cx under Patent Owner’s construction. Murphy II ¶¶68-74.

Even considering Patent Owner’s argument, it engages in arbitrary line drawing to allege that the scanning line driver circuit also includes protection circuits ESD1-ESD3. POR 39-40. This does not alter that *Reiner* discloses or renders obvious claims 1-18 because, “[b]roadly speaking, ‘to’ does not exclude the word ‘in.’” *Aspex Eyewear, Inc. v. Altair Eyewear, Inc.*, 818 F. Supp. 2d 348, 354 (D. Mass. 2011) (“secured to” includes secured “in” and “within”), *aff’d*, 484 F. App’x 565 (Fed. Cir. 2012); Murphy II ¶68; Murphy Tr. 179:5-180:17.

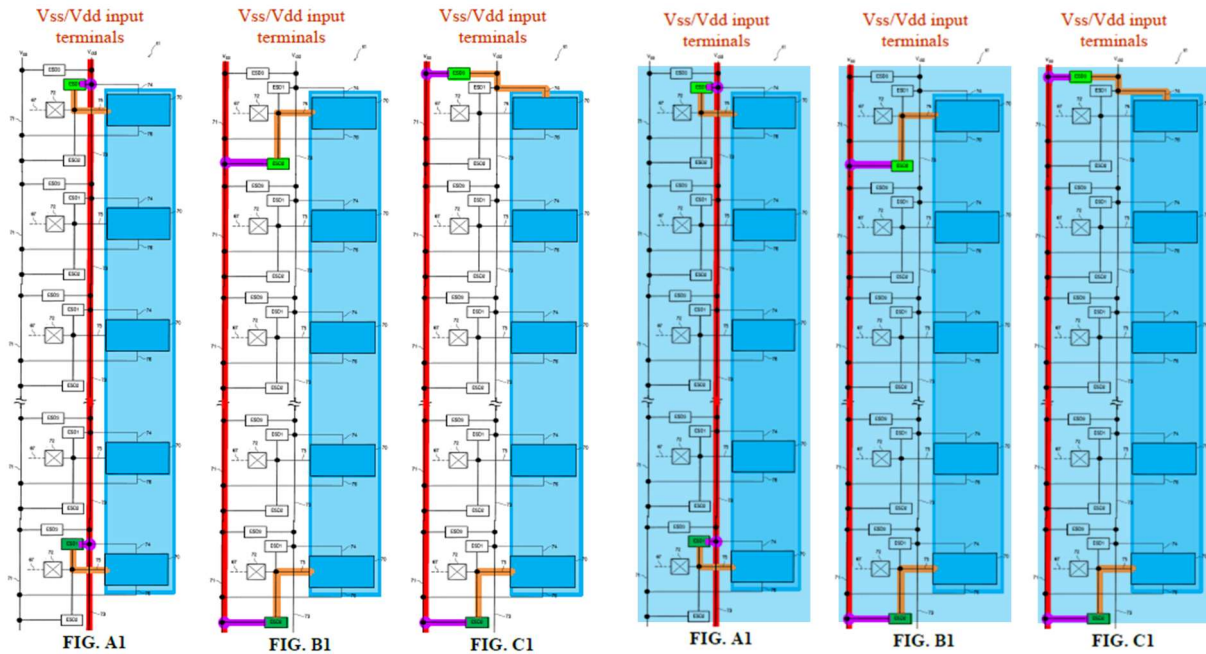
The figures below show the arbitrariness of Patent Owner’s position because, regardless of where the “box” is drawn, there is no difference in structure or operation because the protection circuits ESD1-ESD3 protect the individual driver units (801-*n* or 70) from ESD damage.



Ex. 1001, FIG. 2 (annotated).



Id. (annotated).



Pet. 28.

Id. (as described in POR).

Patent Owner's remaining arguments recycle its incorrect arguments rebutted above.

Patent Owner incorrectly argues that *Reiner* “protecting the inputs/outputs of integrated circuit devices” is “only the prior art.” POR 40, 41.¹⁴ This is incorrect as

¹⁴ Dr. Murphy's testimony in POR 40-41 n.5 is consistent. Dr. Murphy testified that ESD1-ESD3 protect driver units 70, but that the specific circuit layout of those ESD protection circuits was not important to his analysis. Murphy Tr. 180:18-

explained above. *Reiner*'s ESD protection network, when implemented in the scanning line driver circuit, discloses or renders claim 4 obvious. Pet. 16-40, Figures Ax, Bx, Cx; Murphy Tr. 101:2-103:16; Ex. 1001, 3:6-11, 3:15-17, 5:55-6:2, 7:25-51, FIGS. 1-2.

Patent Owner next re-argues that “claim 4 recites a scanning line driving circuit connected to the power supply line *between two protection circuit connections to that power supply line*” (POR 41), which fails by incorrectly arguing that *all* of the scanning line drive “connecting portion[s]” must be “between” the two ESD protection circuit connecting portions. *Supra* § III.A.3; *Rexnord*, 274 F.3d at 1342.

Patent Owner then again improperly tries to avoid its own admission that Petition Figures Cx disclose the claimed configuration under Patent Owner's claim interpretation by asking the Board to permit different positions for infringement in the district court and unpatentability in this proceeding. POR 42; *Bristol-Myers*, 246 F.3d at 1376; *Amazon.com*, 239 F.3d at 1351; *Axonics*, 75 F.4th at 1380-81; *Parkervision*, 88 F.4th at 979-80; *Apple*, 2024 WL 3084509, at *5-6.

181:15. The '157 patent claims protecting the driver circuit, not a specific type of ESD protection circuit. Ex. 1001, claim 4.

B. *Reiner* Discloses or Renders Obvious the Scanning Line Driving Circuit Being Arranged on a Substrate in Claim 8

Patent Owner incorrectly argues that “the Petition does not identify a *display device* substrate and a scanning line driving circuit arranged on that substrate,” which Patent Owner argues means *Reiner*'s scanning line driving circuits are not “*formed on*” the substrate having the display-screen pixels. POR 43-47. Patent Owner argues this, despite acknowledging that “*Reiner* explains the integrated circuit device 20 may be ‘flipped onto the substrate 16.’” POR 44-45.

Claims 4 and 8 do not, however, require that the “substrate” be the display *pixel* substrate—only that it has a “first corner” and “second corner,” with the ESD protection circuits and scan line driver being “arranged” on the substrate. Patent Owner improperly attempts to read in additional limitations.

Even if claim 8's “substrate” is interpreted as the pixel substrate, *Reiner* discloses or renders this obvious. Pet. 44-50. *Reiner* teaches that “source lines 67” and “[t]he output 75 of each output device 70” are both “connected to ... contact pad 72” such that the output lines for the pixels of LCD screen 60 are connected to the driver circuit by bonding at contact pad 72. *Reiner*, 10:1-6, FIGS. 4-5. A POSITA would have understood this is also true for the gate/scan line driver 63 and scan lines 68. *Reiner*, 9:23-28, 10:1-6, FIGS. 4-5; Murphy II ¶¶79; Murphy ¶¶145-146.

Patent Owner incorrectly asserts that Petitioner “invents a ‘substrate’” and has “no evidence” of arranging drivers on the pixel substrate. POR 45-46. *Reiner*’s substrate 16, onto which the drivers are flipped, is the pixel substrate at the contact pad for the source/gate lines, as Dr. Murphy explained. *See* Murphy ¶146; Murphy Tr. 69:12-73:15, 82:8-17, 87:19-88:13, 93:9-94:1; Murphy II ¶82. Arranging the scan lines and gate drivers on a substrate was conventional in the prior art. Murphy ¶146 (citing *Takahara*, [0001], [0064], FIG. 1; *Murai*, [0001], [0017], FIG. 1; Ex. 1001, 1:57-59). *Reiner*’s FIG. 4 shows a “display” having “display drivers,” “an LCD screen 60,” “source lines 67,” “gate lines 68,” “source driver module 61,” and “gate driver 63.” *Reiner*, 9:11-29. *Reiner* teaches connecting the drivers to the lines of the pixel substrate at contact pads 72. *Reiner*, 7:23-25, 10:1-6, FIGS. 2-5. *Reiner* uses “flip-chip technology” to attach the driver to substrate 16, which describes arranging the driver on the pixel substrate. Murphy ¶¶101, 145-146, 231, 251; Murphy Tr. 69:12-73:15, 82:8-17, 87:19-88:13, 93:9-94:1; Murphy II ¶¶74-87; *Reiner*, 7:23-25; Ex. 1019, *Kang*, 1 (chip on glass “driver IC is directly mounted on LCD panels by flip chip”); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD”; “driver ICs are mounted directly on the glass panel”); Ex. 1021, *Wu*, 20 (COG includes “[d]irect mounting of flip chip onto glass”).

The foundation of Patent Owner's argument is also wrong. Claim 8 does not require **forming** the driver circuits directly on the substrate. It instead recites "arrang[ing]" the circuits on the substrate. Ex. 1001, claim 4. The '157 patent contradicts Patent Owner's position, teaching that the driver may be a silicon chip instead of formed directly on the substrate: "***instead of a thin film transistor formed on the insulating substrate***, an active matrix substrate may be used, in which ... ***a driving circuit is formed on a crystal silicon wafer.***" *Id.*, 11:29-33 (emphases added); cf. POR 44-45 (describing *Reiner* the same as the '157 patent's alternative).

Patent Owner argues that a "POSITA would *not* mount an integrated circuit formed on its own separate substrate[] onto a display substrate," because "a silicon integrated circuit chip ... would not fit within the 4-5 micron vertical gap between the display substrate and the counter substrate" of the pixel region. POR 47. But nothing limits the claims to a "4-5 micron" pixel height and, regardless, the drivers are in the periphery, making this argument immaterial. Murphy II ¶88.

The purpose of *Reiner*'s flip-chip technology is mounting the source/data and gate/scan line drivers **on** the LCD panel to realize higher-density integrated

circuits and pixels.^{15,16} *Reiner*, 12:15-18; *Kang*, 1; *Joshi*, 4; *Wu*, 20; Murphy II ¶¶85-86. Whether other attachment options were available does not change that *Reiner* discloses, or at least renders obvious, claim 8.

Patent Owner's argument that, "if a POSITA were to arrange a gate/scan line driver directly on the display substrate, *Reiner*'s integrated circuit ESD protection network ... would necessarily change, at least because there would be no need to include contact pads 72 ... or the ESD devices tied to those contact pads (ESD1, ESD2)" (POR 47), is also incorrect. Patent Owner does not identify any needed change, let alone one material to the claims, or rebut Dr. Murphy's teaching that *Reiner*'s ESD protection network protects whatever circuit is in box 70, as explained above. To the contrary, *Reiner* discloses arranging the drivers with the ESD protection network of FIG. 5 on the pixel substrate at the substrate's contact

¹⁵ Dr. Murphy identified the motivation to use flip-chip technology *and* that *Reiner*'s described ESD network further protects such densely packed circuits. Murphy ¶¶112-113, 116-119, 157, 181, 231, 238, 239. Patent Owner does not challenge this.

¹⁶ If the Board finds *Reiner* does not disclose or render this obvious, it would have been obvious in view of *Takahara*. Pet. 81-89; *infra* § IV.

pads for the source/scan lines, while protecting the driver circuit against ESD events (which Patent Owner admits, POR 36-40). Patent Owner's assertion is unsupported and contradicted by *Reiner*.

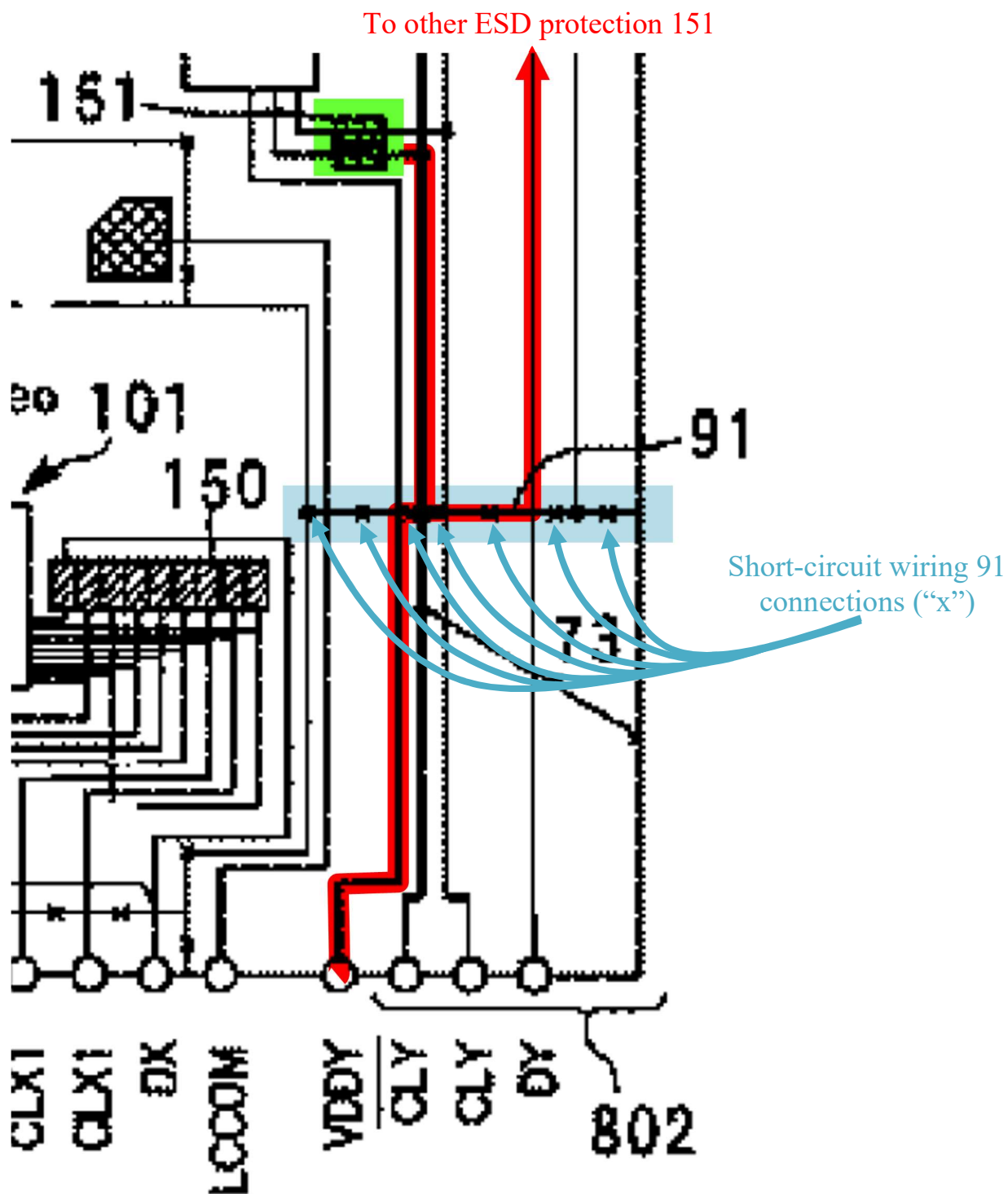
C. Claims 1-3, 5-7, and 9-18

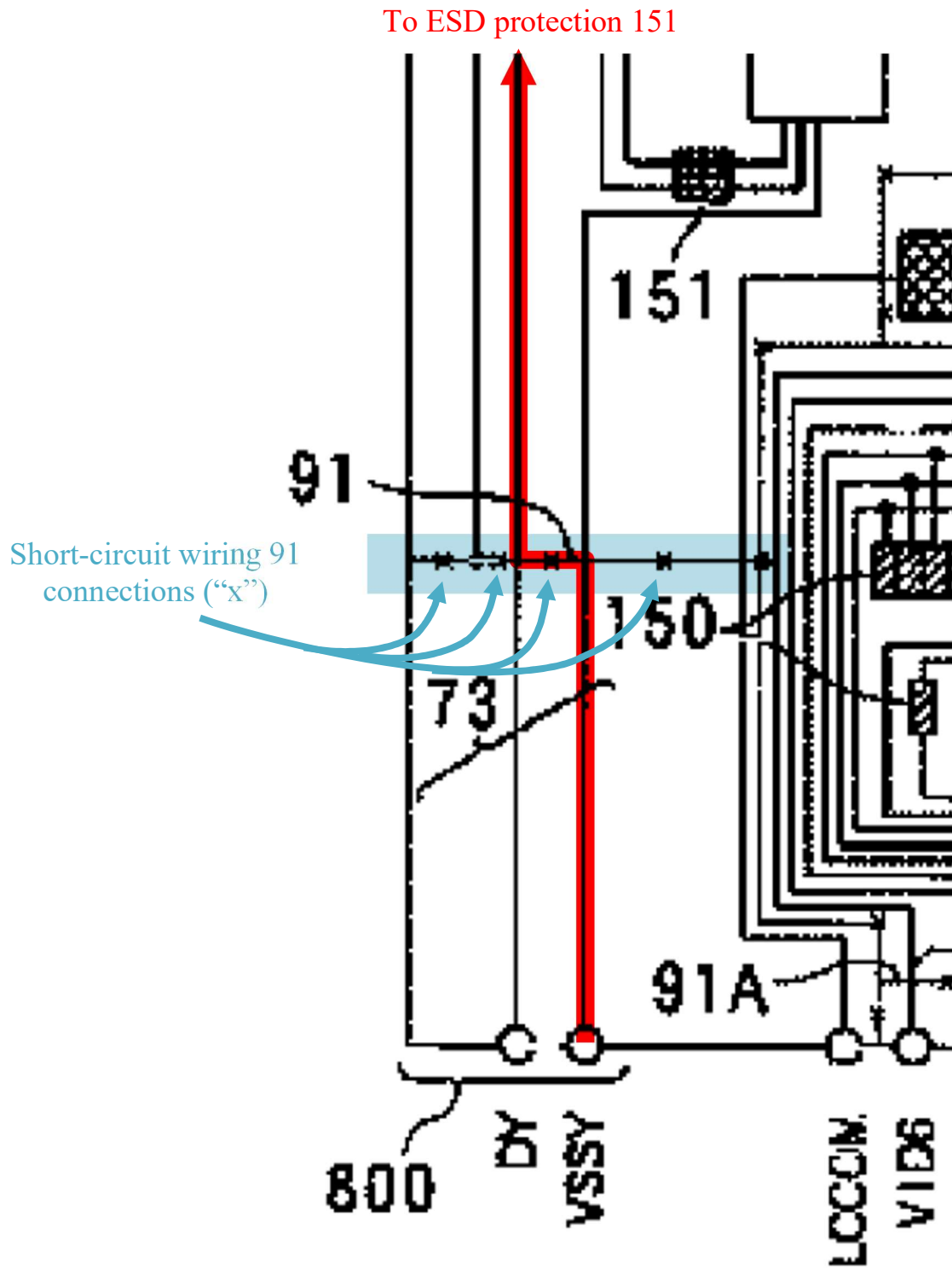
Patent Owner's arguments for claims 1-3, 5-7, and 9-18 refer back to claims 4 and/or 8 (POR 42-52) and fail for the reasons discussed above.

IV. *Reiner* and *Takahara* (Ground 2) Render Obvious Claims 1-18

Patent Owner's arguments against Ground 2 are based on the incorrect premise that short-circuit connections 91 do not connect the power lines to ESD protection circuits 151. POR 52-69 ("*Takahara* does not disclose that the short-circuit wirings connect the power lines to the signal lines (and their protection circuits).").

Takahara identifies short-circuit wirings 91 with an "x" and FIG. 1 shows these connections between the power lines and lines with ESD protection 151.





Takahara, FIG. 1 (excerpted, annotated).

Takahara contradicts Patent Owner's argument, explaining that "static electricity entering ... **first short-circuit wiring 91** does not reach ... **scan-line drive circuit 104** unless it passes through ... electrostatic-protection circuit 150 (or 151)," which "reliably protect[s]" scan-line drive circuit 104 from ESD. *Takahara*, [0066] (emphases added), FIG. 1; Murphy II ¶¶91-94.

Patent Owner's argument that *Takahara* relates to manufacturing actually supports obviousness, because so do *Reiner* and the '157 patent. *Reiner*, 7:23-26, 11:18-19; Ex. 1001, 4:20-26, 5:61-65, 7:11-15.

A. *Reiner* and *Takahara* Render Obvious the Claimed Input Terminals Connected to the Power Supply Lines ([4c])

Patent Owner's arguments against [4c] fail because they relate to *Reiner*'s disclosure, not the asserted combination that includes input terminals, such as on the substrate to power the gate/scan line driver circuits after the flip-chip mounting. Compare POR 58 (Section VI.B.2.a.i), with Pet. 72-76. Murphy II ¶95.

B. *Reiner* and *Takahara* Render Obvious [4f] as Claimed

Patent Owner's arguments against *Reiner* and *Takahara* for [4f] center around three positions: (1) that VDDY/VSSY are not "signal wirings" 72/73; (2) *Takahara* does not disclose VDDY/VSSY being "connected to" the ESD protection circuits 151 through short-circuit wiring 91; and (3) that *Takahara* must provide additional disclosure than the Petition relied on to render the claims

obvious. POR 58-68. Patent Owner is wrong on all accounts, but if considered, none change the outcome.

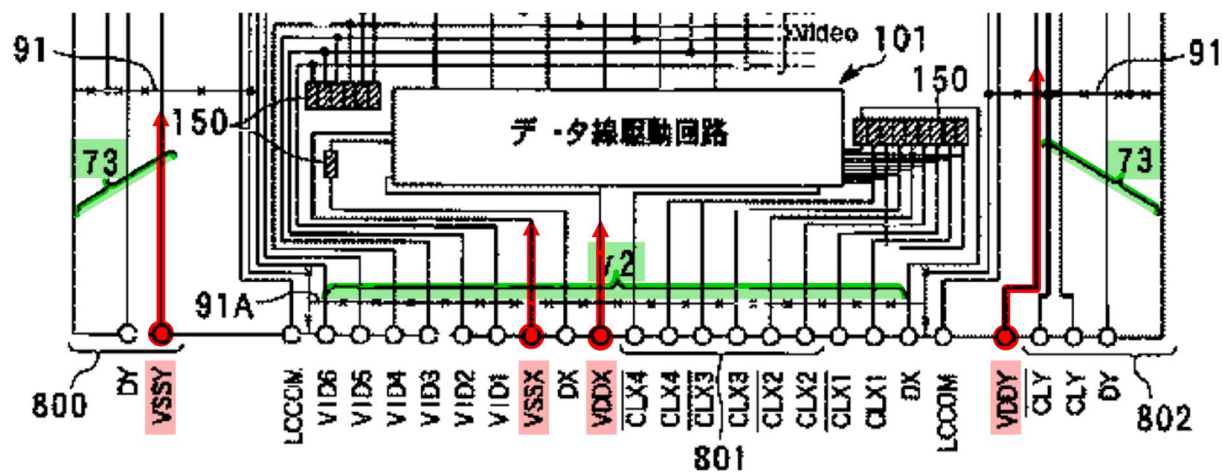
First, the Petition relies on *Takahara* for the basic, conventional teaching of protecting a scanning line driver circuit from ESD damage as motivation to protect *Reiner*'s gate/scan line driver with an ESD protection network, like in *Reiner*'s FIG. 5. Pet. 76-80. That basic teaching is sufficient to render the claims obvious. See D.I. 42-43. Patent Owner does not challenge any of the motivations identified in the Petition, such as *Reiner*'s acknowledgement that driver circuits are "very sensitive" and susceptible to being "destroyed" by ESD, and *Takahara*'s teaching that ESD protection circuits can "reliably protect[]" the scan line driver from ESD damage that can render it nonfunctional. See Pet. 77-80; Murphy ¶¶113-119, 237-240; Murphy II ¶97, ¶110; Schubert Tr. 51:15-52:19.¹⁷

Patent Owner incorrectly argues that "the Petition cites no evidence showing that *Takahara*'s signal lines 73 include power supply lines VDDY and VSSY." POR 60-62 (citing *Takahara*, [0024], [0025], [0060], [0061], [0065], FIG. 1). But

¹⁷ To the extent Patent Owner is arguing that *Reiner* and *Takahara* cannot be bodily incorporated into one another, the law has long rejected that proposition. *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012).

FIG. 1 expressly contradicts Patent Owner's position, and Patent Owner's citations do not exclude the power lines from signal wirings 72/73.

As shown below, the brackets for "signal wirings 72, 73" (green) in FIG. 1 encompass and include power lines VSSY/VSSX/VDDX/VDDY (red).¹⁸ Murphy II ¶¶101-102.



Takahara, FIG. 1 (excerpted, annotated).

Takahara paragraphs [0024]-[0025] describe connecting "wirings" that "include" data and scan lines, but **do not exclude** power lines from the "wirings." Paragraph [0060] describes parts of "data-line drive circuit 101," but does not

¹⁸ A POSITA would have recognized that brackets 73 expressly encompass VSSY (left) and VDDY (right) based on the brackets' position and consistent with all other power lines being part of the wirings 72/73. Murphy II ¶102.

mention any wirings, let alone limit them. Paragraph [0061] describes some signals “supplied to the scan-line drive circuits 104,” but does not limit the meaning of wirings 72/73 to **only** these signals. Paragraph [0065] describes “signal **wirings**” 72/73 by their structure as “metal film[s],” but also does not exclude power line wirings. (Emphasis added.) None contradict FIG. 1’s showing of wirings 72/73 including three power lines, which drive the driver circuits to powering the circuits. Murphy II ¶¶98-102.

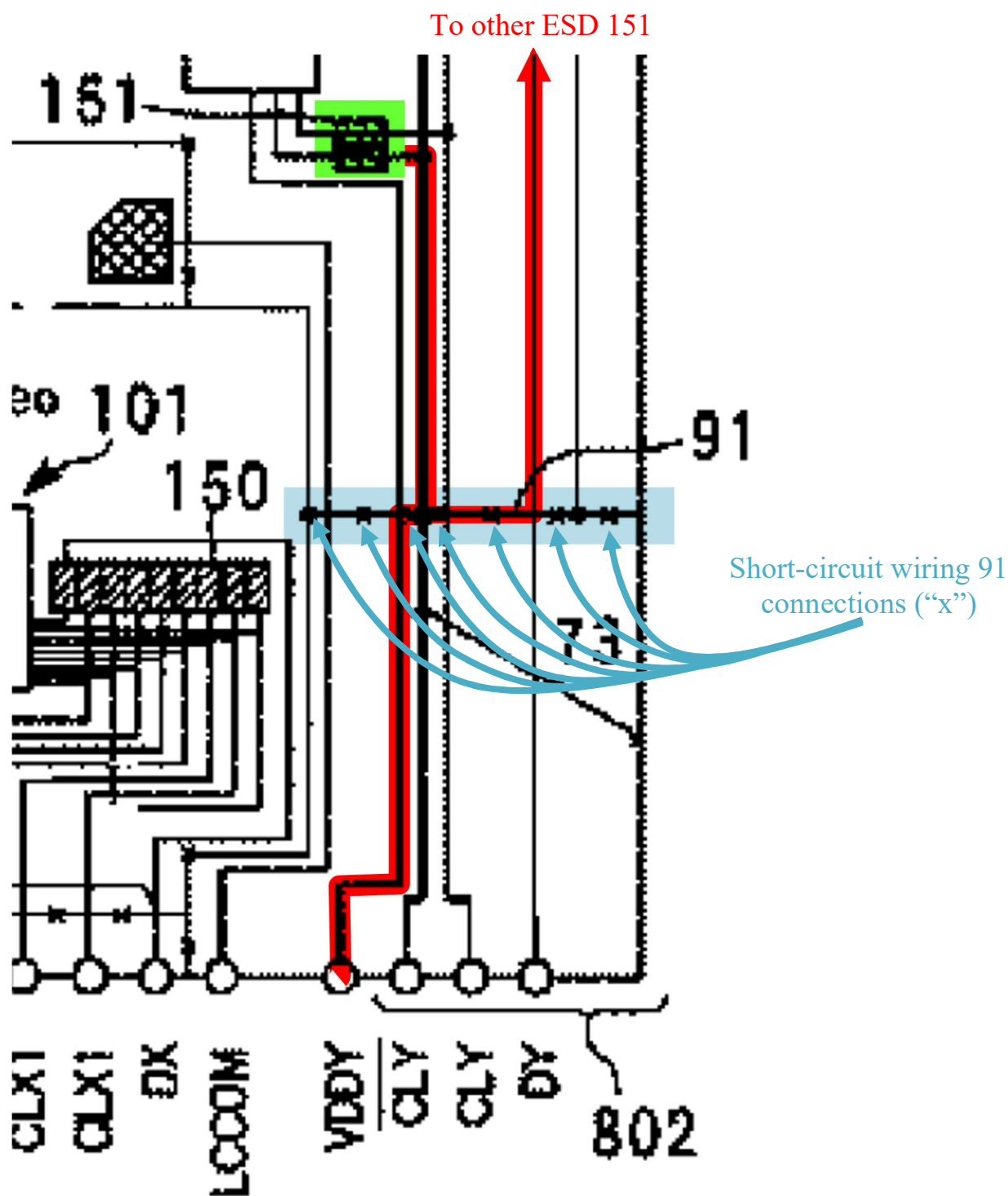
Patent Owner concludes that *Takahara*’s “Figure 1 shows that electrostatic-protection circuits 151 are formed only at intermediate locations of the clock signal lines and start single lines,” not “the power supply lines VSSY and VDDY.” POR 60-62. This is wrong and ignores the teachings of *Takahara*’s FIG. 1 and paragraph [0066], which explain that ESD protection circuit 151 protects the scan-line driving circuit against static electricity such as that passing from power lines VSSY/VDDY along short-circuit wiring 91. *Takahara*, [0066], FIG. 1; Pet. 76-80.

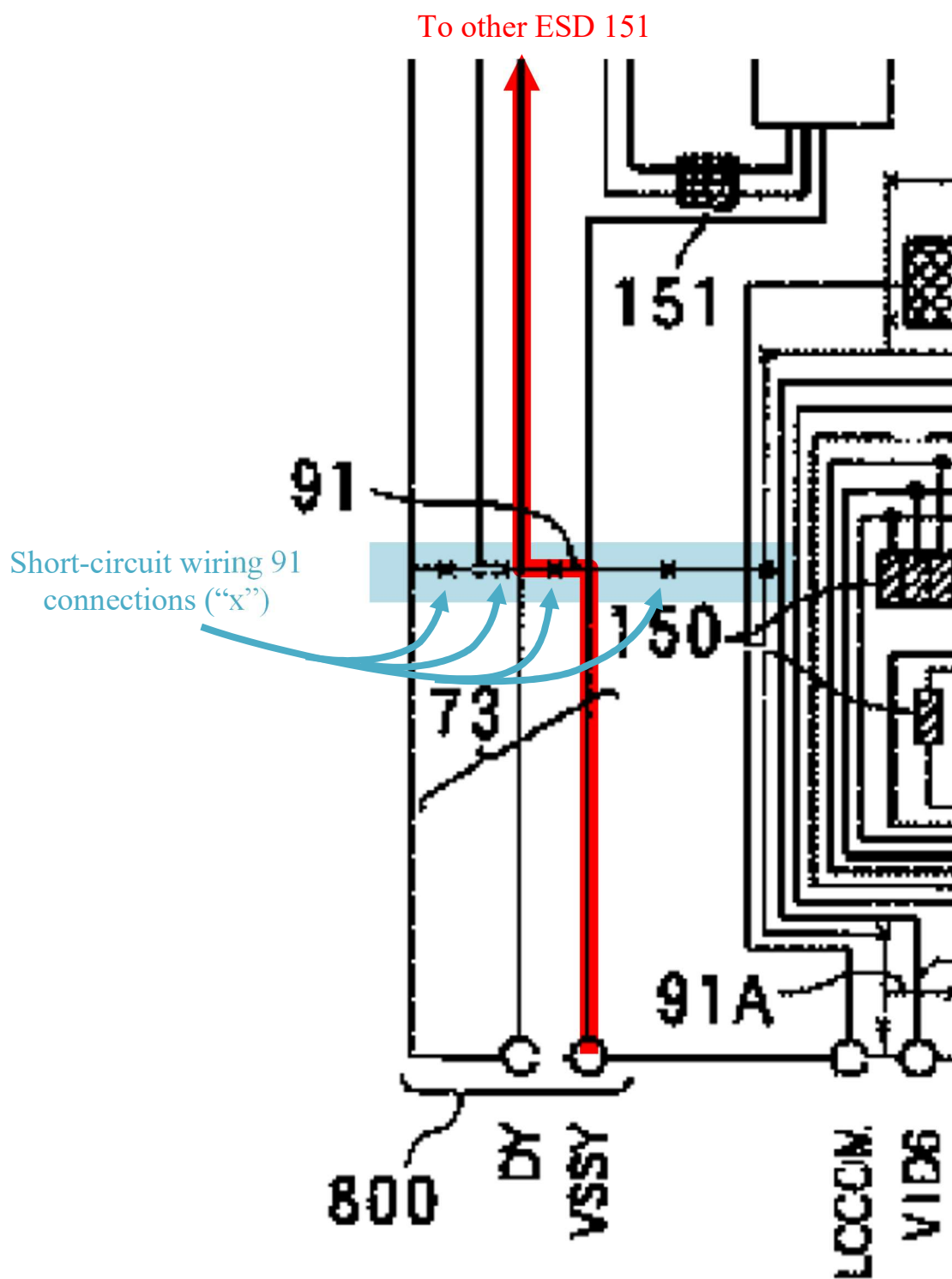
Patent Owner argues that “[t]he annotations ... on the right side of Figure 1 include only CLY bar, CLY, and DY signal wirings and terminals,” and exclude the power lines. POR 61-62. This incorrectly asks the POSITA to (1) create exclusions not recited by *Takahara* (*see supra*); (2) ignore **three** express **inclusions** of power lines (VSSY/VSSX/VDDX) in signal wirings 72/73; and (3) ignore that

the right-hand bracket is directed towards VDDY, indicating inclusion. A POSITA would not do so. Murphy II ¶¶103-106.

Patent Owner next argues that short-circuit wirings 91 (“x”) do not connect power lines VDDY/VSSY to ESD protection circuits 151 (POR 62-64), which is contradicted by *Takahara*’s FIG. 1 and paragraph [0066], as explained above.

Murphy II ¶¶91-94, 107-110.





Takahara, FIG. 1 (excerpted, annotated).

Patent Owner's arguments that ESD protection circuits 151 would not protect scan-line drive circuit 104 from ESD on short-circuit wiring 91 and about the direction of ESD flow (POR 63-64) are also contradicted by *Takahara* paragraph [0066]'s teaching that "scan-line drive circuit 104" is "reliably protected" from "static electricity entering ... first short-circuit wiring 91," as explained above.¹⁹

C. A POSITA Would Have Been Motivated to Combine *Reiner* and *Takahara*

Patent Owner's arguments against the Petition's motivations to combine *Reiner* and *Takahara* merely repeat or refer back to prior arguments. POR 69. They do not address the Petition's combination to use *Reiner*'s ESD protection network to protect a scanning line driving circuit, such as one flip-chip-arranged on the substrate. They are also incorrect as discussed above. *Supra* §§ III.A.2-III.A.4, IV.B. Murphy II ¶¶111-112.

¹⁹ Patent Owner's remaining argument that FIG. 3's VDD/VSS connections are not "connected to a power supply line" (POR 65-68), whether correct or not, is not material because of *Takahara*'s connections through short-circuit wiring 91.

D. Claims 1-3 and 5-18

Patent Owner's arguments for claims 1-3 and 5-18 refer back to previous arguments (POR 70-73) and fail for the reasons discussed above.

V. Conclusion

All claims are unpatentable and should be canceled.

Dated: June 6, 2025

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CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, Petitioner certifies that the word count of Petitioner's Reply (exclusive of any table of contents, table of authorities, mandatory notices under § 42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 5,598.

Dated: June 6, 2025

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CERTIFICATE OF SERVICE

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