

A New COG Technique Using Low Temperature Solder Bumps for LCD Driver IC Packaging Applications

Un-Byoung Kang and Young-Ho Kim

Abstract—A new chip on glass (COG) technique using flip chip solder joining technology has been developed for excellent resolution and high quality liquid crystal display (LCD) panels. The flip chip solder joining technology has several advantages over the anisotropic conductive film (ACF) bonding technology: finer pitch capability, better electrical performance, and easier reworkability. Conventional solders such as eutectic Pb–Sn and Pb–5Sn require high temperature processing which can lead to degradation of the liquid crystal or the color filter in LCD modules. Thus it is desirable to develop a low temperature process below 160 °C using solders with low melting temperatures for this application. In our case, we used eutectic 58 wt%Bi–42 wt%Sn solder for this purpose. Using the eutectic Bi–Sn solder bumps of 50–80 μm pitch sizes, an ultrafine interconnection between the IC and glass substrate was successfully made at or below 160 °C. The average contact resistance of the Bi–Sn solder joints was 19 m Ω per bump, which is much lower than the contact resistance of conventional ACF bonding technologies. The contact resistance of the underfilled Bi–Sn solder joints did not change during a hot humidity test. We demonstrate that the COG technique using low temperature solder joints can be applied to advanced LCDs that lead to require excellent quality, high resolution, and low power consumption.

Index Terms—Bi–Sn, chip on glass (COG), flip chip, liquid crystal display (LCD), solder bump.

I. INTRODUCTION

LIQUID CRYSTAL displays (LCDs) are becoming the most important display devices, because they combine a compact and flat shape with lower power consumption compared with the traditional cathode ray tubes. The LCD driver integrated circuit (IC) packaging technology has a significant influence on display performance. The electrical interconnect between the LCD panel and the driver circuit needs improvement to achieve finer pitch, easier assembly, higher interconnect reliability, lower joint resistance, and easier reworkability [1]. The trend in LCD driver IC packaging has been to move the driver IC closer to the LCD itself. Today, tape automated bonding (TAB) is the predominant packaging technology for large area LCDs. Driver IC may be easily tested and burned in prior to final assembly in TAB technology. However, one of the

limiting factors is the dimensional instability of the polyimide carrier of the TAB tape in fine pitch interconnection. Therefore, the use of chip on glass (COG) technique is proposed for a number of products such as high pixel density and small area LCDs. In this technique, the driver IC is directly mounted on LCD panels by flip chip. Several kinds of COG bonding techniques have been developed [1]–[3]: Au bump bonding using anisotropic conductive adhesive (ACA) or anisotropic conductive film (ACF), and stud bump bonding using isotropic conductive adhesive. In high volume, only the ACF technique has recently been applied for LCD driver IC packaging. It allows a flux-less, low temperature assembly process suitable for high density interconnects. Still, ACF bonding has several shortcomings. Generally, today's joints using conventional ACF bonding show high contact resistance [4]–[6]. In future high-definition LCDs, this resistance will even be larger or interconnect is prone to be open due to the reduction in pitch and contact size. In addition, bump alignment and uniformity requirements will grow.

Alternatively, there were a few studies on COG techniques with solder materials instead of ACF. Although materials and processing details differed, most of these studies used low melting metals or alloys. For example, Mori *et al.* [7] Au bumps on driving ICs that are capped with indium–tin (InSn). However, these joints also show a high contact resistance and they require an accurate alignment due to the mechanical contact bonding. Thus, this technique is difficult to apply to ultra-fine pitch packages as conventional ACF bonding.

For ultra-fine COG packaging, flip chip soldering offers several advantages over ACF [8] and mechanical contact technique.

- 1) The solder reacts with the metal film on the substrate metallurgically, whereas the ACF just forms mechanical contacts to its surface. So, flip chip solder joints have a substantially lower contact resistance.
- 2) During soldering, the contact pressure is much lower than during ACF bonding or welding. This prevents any cracks from the glass substrate.
- 3) The self-alignment capability of the liquid solder dramatically lowers the alignment and uniformity requirements of the reflow process making ultra-fine pitch applications feasible [9].
- 4) The rework process is easy by raising the temperature above the melting temperature of solder.
- 5) This technique is able to eliminate the expensive ACF.

Even though flip chip soldering has many advantages, it has not been used in LCD driver IC packaging. The most common

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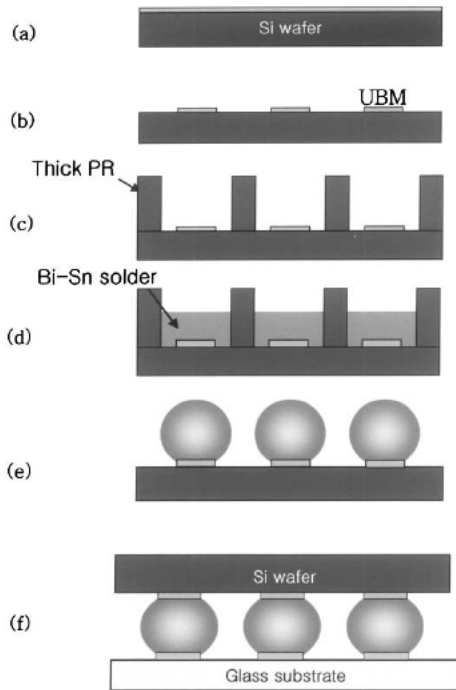


Fig. 1. Schematic view showing the basic procedure for fabricating the low temperature solder joints: (a) Au(100 nm)/Cu(1 μm)/Cr(50 nm) metal film deposition, (b) UBM formation through wet chemical etching, (c) lift-off mask formation, (d) eutectic Bi-Sn solder deposition; (e) PR strip and reflow, and (f) flip chip bonding.

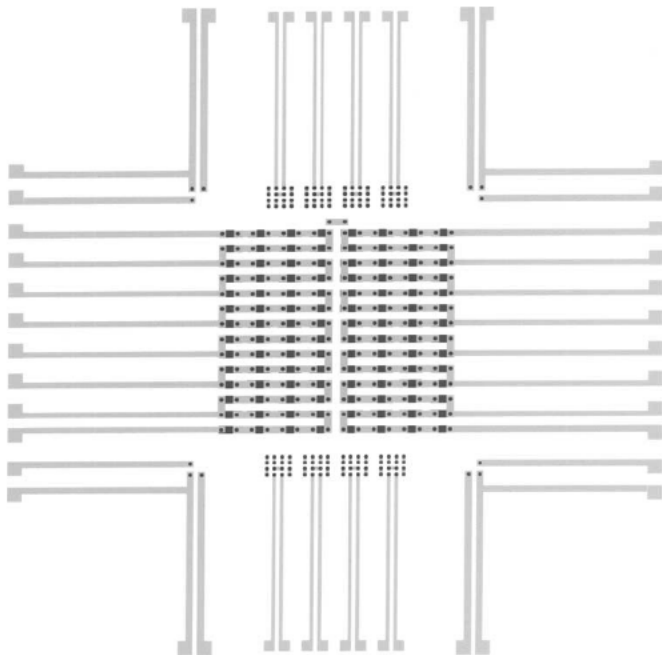


Fig. 2. Schematic view of daisy chain connection on test chip (dark gray) and glass substrate (light gray).

flip chip technology uses solders such as eutectic Pb-Sn and Pb-5Sn requiring reflow temperatures above 200 °C. However, the liquid crystals or the color filter in the LCD modules degrade at temperature higher than 160 °C. Therefore, low-melting solders are needed.

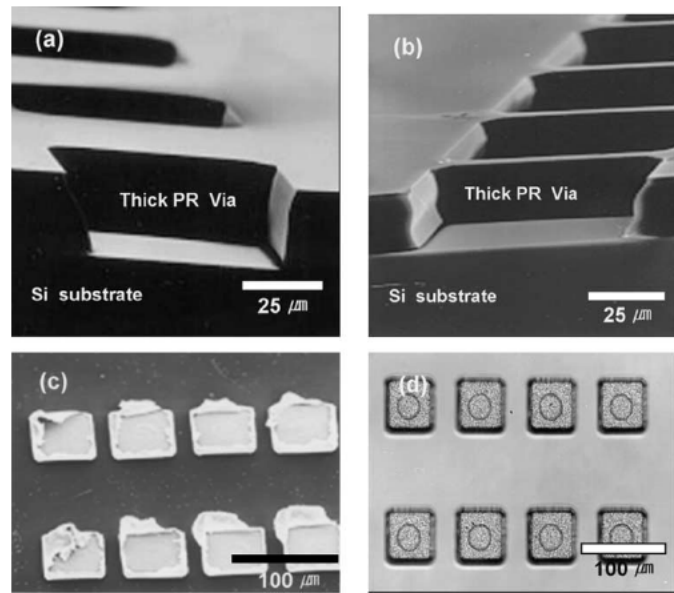


Fig. 3. SEM images of (a) solder vias in conventional lift-off mask, (b) overhang-structural solder vias in modified mask, (c) as-deposited solder bumps using conventional lift-off mask, and (d) as-deposited solder bumps using overhang-structural lift-off mask.

In this study, eutectic Bi-Sn solder (melting point: 138 °C) has been chosen for developing a COG process applicable to ultra-fine pitch LCD packages.

II. EXPERIMENTAL PROCEDURE

Cr (0.05 μm), Cu (1 μm), and Au (0.1 μm) thin films were deposited on Si wafers for under bump metallurgy (UBM) using DC magnetron sputtering system without breaking the vacuum of the chamber. Octagonal shaped UBMs with the pitches of 50 μm or 80 μm were fabricated by photolithography and wet chemical etching. Eutectic Bi-Sn solders were evaporated on the UBM and solder bumps were patterned by lift-off and formed by reflow. The thick photoresist (PR) lift-off mask was made by a two-step spin coating resulting in the adequate height of 30 μm . Then, reflow process was performed in N_2 by rapid thermal annealing. The heating rate was 90 °C/min. The peak temperature of 150 °C or 160 °C, respectively, was held for 4 min or 9 min.

The solder bumped chip was aligned to the glass substrate with the metal pads using a flip chip bonder and all solder joints were made simultaneously during the reflow process at 160 °C. The underfill process was applied to improve the reliability of solder joints. Curing the epoxy resin at 160 °C for 5 min, the solder joints were reflowed a second time. Fig. 1 summarizes the basic process flow.

For the electrical test of solder joints, Ti(0.1 μm)/Au (0.1 μm)/Cu (3 μm)/Ti (0.05 μm) or Ti (0.1 μm)/Au (0.1 μm)/Ni (0.5 μm)/Cu (3 μm)/Ti (0.05 μm) metal films were deposited to form daisy chain links on SiO_2/Si wafer. The UBMs were fabricated by the wet chemical etching of Ti top layer. Fig. 2 is a sketch of the structures for the electrical test. The dots, the light gray lines, and the dark gray lines indicate the solder joints, the conductors on the glass substrate, and the

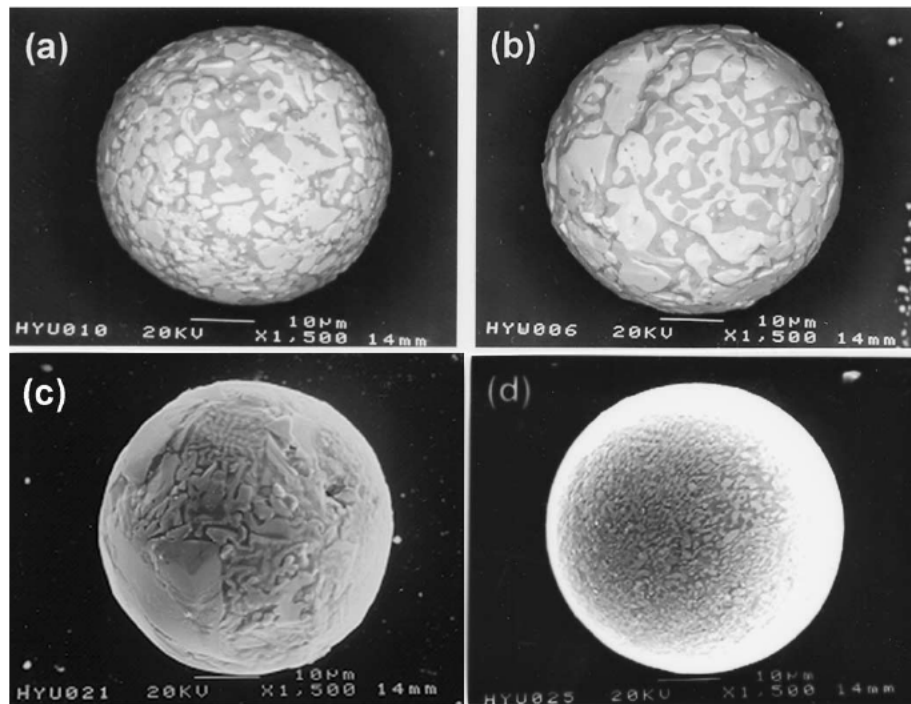


Fig. 4. SEM micrographs showing the plane view of Bi-Sn solder bumps after reflow (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

conductors on the test chip, respectively. The daisy chains have a total of 112 links. The electrical resistance (R_c) of samples with Bi-Sn solder joints of 80 μm pitch was measured by four point probing. The average resistance was obtained from four samples at least. For reliability testing, the specimens were stored at 85 °C/85% RH up to 500 h.

III. RESULTS AND DISCUSSION

A. Solder Bump Formation and Flip Chip Bonding

The SEM images (Fig. 3) show the thick PR lift-off mask and the as-deposited solder bumps after the lift-off process. The lift-off mask formed by the conventional process have inverse-trapezoid vias [Fig. 3(a)]. It allows solder deposition at the wall of the via resulting in irregular bump shapes after lift-off [Fig. 3(c)], large variations in bump height after reflow, which increases the possibility of bonding failure during joining. Therefore, the solder mask process has been modified as follows: first spin coating, blank exposure without E-beam mask, second spin coating, and exposure. This way, an overhang lift-off mask was fabricated [Fig. 3(b)], which leads to perfectly square and uniform solder bump as shown in Fig. 3(d). Preventing solder deposition at the via side walls, the overhang produces discontinuities around the top via edges providing for perfect solder removal later on. Thus, it is the key to successful liftoff.

When Bi and Sn are evaporated together at the same time, Bi evaporates first due to its lower vapor pressure. In this case, the solder has a poor wettability because Cu does not react with Bi [10]. However, evaporating Sn first, the wettability is good since Sn and Cu easily react with each other. This also helps generating uniform spherical solder bumps [11]. Therefore, it is

more effective to deposit Sn first on UBM than to deposit Bi and Sn at the same time.

Fig. 4 shows secondary electron images of Bi-Sn solder bumps after reflow at 150 °C and 160 °C for 4 min and 9 min, respectively. The solder bumps reflowed at 150 °C showed a slightly rough surface regardless of the reflow time. The solder bump reflowed at 160 °C for 9 min had the smoothest surface. Fig. 5 adds the backscattered electron (BSE) images of the bumps shown in Fig. 4, which provide more information on the microstructure of eutectic solder as the BSE signal is stronger for heavier elements. Thus in Fig. 5, the Bi phase appears light while the Sn phase appears dark. The solder bumps reflowed at 150 °C all show large Bi phases at their surface. The solder bumps reflowed at 160 °C for 4 min have the mixed surface microstructure consisting in part of large Bi phases but also of lamellae Bi-Sn regions. For the solder bump reflowed at 160 °C for 9 min, the microstructure all appeared lamellar. This is similar to that of eutectic Pb-Sn bumps. Fig. 6 shows the BSE images of the cross sections of Bi-Sn solder bumps. Only the bump reflowed at 160 °C for 9 min has the fine and uniform mixture of Bi and Sn. The other bumps consist of large Bi-rich phases in a Sn matrix. The large Bi phases are prone to be formed at the solder surface of Bi-Sn solder bumps and to increase the roughness of solder bumps. On the other hand, the fine mixture of Bi and Sn leads to a smooth surface. It is believed that the Bi-Sn solder bumps having a smooth surface and uniform shape are most suitable for flip chip bonding process. Thus the microstructure should be controlled carefully by choosing the appropriate reflow parameters. In the case of Bi-Sn solder bumps of 50 μm pitches, morphology and microstructure were similar to those of 80 μm pitch solder bumps.

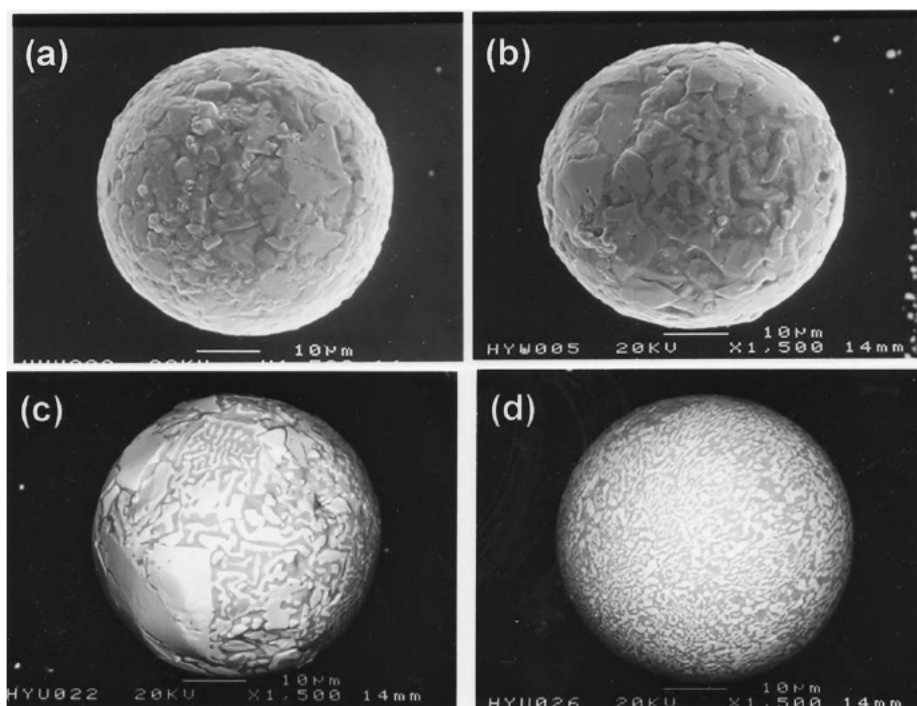


Fig. 5. Backscattered electron images of Bi-Sn solder bumps after reflow (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

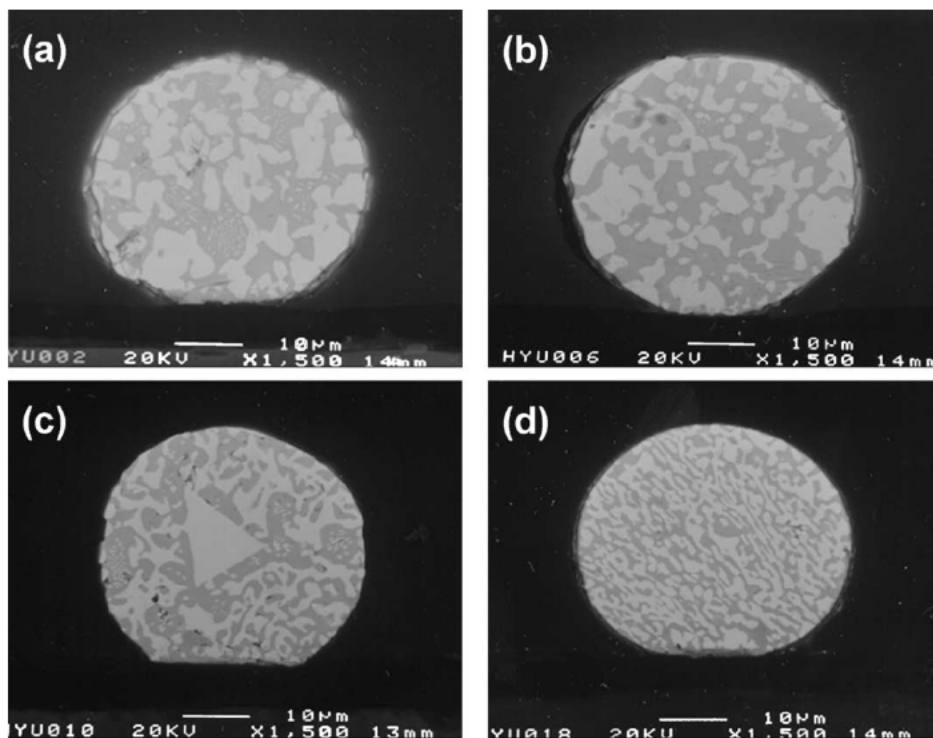


Fig. 6. Backscattered electron images showing the cross section of the Bi-Sn solder bumps after reflow: (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

In Fig. 7, eutectic Bi-Sn solder arrays with two different pitches are shown after the reflow at 160 °C for 9 min and a rapid cool down. The bumps are uniform and smooth. In the case of 80 μm pitch [Fig. 7(a)], height and diameter of the solder bumps are about 40 μm and 46 μm , respectively, while they are about 24 μm and 27 μm in the 50 μm pitch arrays.

During assembling, the solder bumps of the test chip were aligned to the metal pads of the glass substrate and then heated to 160 °C for joining. A no-clean type flux was applied prior to the joining. Fig. 8 gives a cross-sectional SEM micrograph of a 50 μm pitch Bi-Sn solder joint assembled at 160 °C. The spherical-shaped solder joint was successfully connected to the

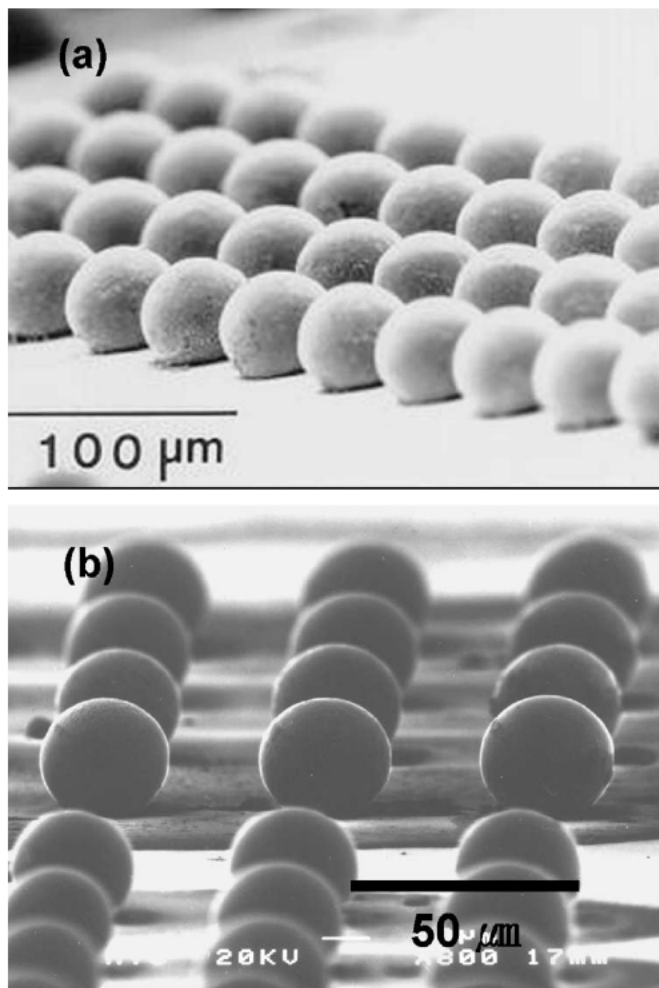


Fig. 7. SEM images of eutectic Bi-Sn solder bump arrays having: (a) 80 μm pitches and (b) 50 μm pitches.

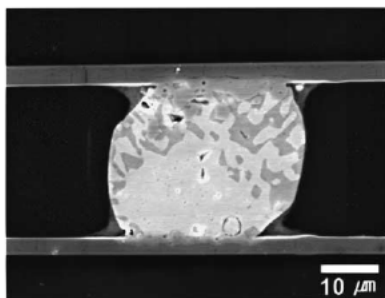


Fig. 8. SEM micrographs of eutectic Bi-Sn solder joint of 50 μm pitches.

metallization between Si and glass substrate. This demonstrates that ultra-fine interconnections with pitches of 50 μm can easily be formed using this technique due to the self-alignment capability of the joints driven by the surface tension of liquid solder.

B. Contact Resistance Measurement & Reliability Test

Table I lists the average contact resistances (R_c) per link of daisy chain. These values include the contact resistance of one Bi-Sn solder joint and a conductor line. Table I clearly shows for both metallizations that R_c of Bi-Sn solder joint is much lower than that of conventional ACF joints [4]–[6], although it even

TABLE I
CONTACT RESISTANCES OF Bi-Sn SOLDER JOINTS
BEFORE UNDERFILL PROCESS

Glass metallization	R_c (m Ω)	Standard deviation
Au/Cu/Ti	19	3
Au/Ni/Cu/Ti	35	6

TABLE II
CONTACT RESISTANCES OF Bi-Sn SOLDER JOINTS
BEFORE AND AFTER UNDERFILL PROCESS

Glass metallization	Underfill	R_c (m Ω)	Standard deviation
Au/Cu/Ti	X	19	4
	O	23	7

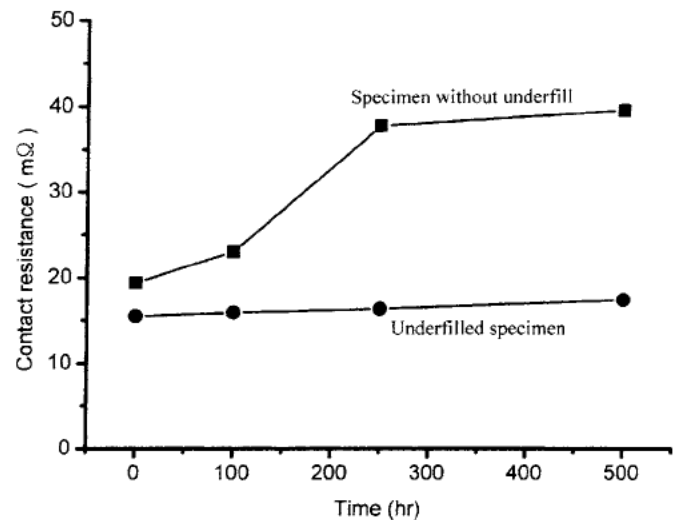


Fig. 9. Contact resistances of Bi-Sn solder joint without and with underfill after storage at 85 $^{\circ}\text{C}$ /85% RH condition.

includes the resistances of the conductor line. Calculating the resistances of conductor lines on chip and substrate and subtracting them from R_c presented in Table I, the real contact resistances of Bi-Sn solder joints is 8 m Ω and 12 m Ω in both cases.

Table II shows the R_c s before and after the underfill process. The solder joints were additionally reflowed at 160 $^{\circ}\text{C}$ for 5 min because the epoxy resin required a curing. After this process, the contact resistance remained within the range of standard deviation from the initial value, i.e., much lower than in ACF joints. This result can be explained by the bonding characteristics and bonding area. The metal particles in the ACF provide only a few conductive paths from the Au bump of the driver IC to the pad of the LCD panel. On the other hand, the metallurgical solder joints form electrical contacts between the whole area of the UBM at the driver IC and the metal pad at the LCD panel.

The R_c s of the Bi-Sn solder joints without or with underfill process have been measured during storage in the 85 $^{\circ}\text{C}$ /85% relative humidity condition up to 500 h. The results are shown in Fig. 9. Without underfill, the R_c of the Bi-Sn solder joint

increased by 100% during the test—still being lower than the contact resistance of conventional ACF joints. However, the R_c of the Bi–Sn solder joint with underfill remained almost completely unchanged. Obviously, the epoxy underfill prevented any corrosion of the solder surface and the conductor lines, which otherwise had been responsible for the increase. Therefore, the use of underfill provides for an excellent reliability of the COG modules with eutectic Bi–Sn solder joints.

IV. CONCLUSION

A COG bonding technique has been developed. Using eutectic Bi–Sn solder materials, maximum bonding temperature was below 160 °C. The solder is applied to the chip by a bumping process, in which an overhang-structural lift-off mask was found being effective for perfect lift-off. The morphology of the Bi–Sn solder bumps was greatly affected by its microstructure. Smooth spherical uniform solder bumps have been fabricated by controlling the microstructure of Bi–Sn solder bumps. The bumps, whose minimum pitch was 50 μm , were successfully soldered to metal pads on glass substrate. The self-alignment capability of liquid solder provided ultra-fine pitch applications easily feasible.

The average contact resistance of Bi–Sn solder joint was as low as 19 m Ω including the resistances of the conductor line. This value is much lower than that of the conventional ACF joints. COG modules with eutectic Bi–Sn solder joints and underfill have an excellent reliability even in a hot humid environment. The contact resistance did not change during 500 h at 85 °C/85% RH. Thus, the low temperature soldering process developed is well suited for COG modules with ultra-fine pitch LCD driver ICs and offers a number of advantages over the ACF technique. It allows the fabrication of advanced LCDs to require excellent quality, high resolution and low power consumption.

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