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# MICROELECTRONICS JOURNAL

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# Chip on glass—interconnect for row/column driver packaging

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New liquid crystal active matrix color flat panel displays and super twisted nematic liquid crystal displays and other flat panel displays are driving new interconnect technologies to make low cost, thin, compact, mass terminations with high resolution capabilities. Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD. FCOG and COG offer the highest density possible in packaging. Several interconnect technologies in FCOG/COG have been developed; their strengths and weaknesses are discussed in this paper. The challenges for COG adoption are also discussed. © 1998 Elsevier Science Ltd. All rights reserved.

## 1. Introduction

The liquid crystal display (LCD) market can be considered to be a large application of the flip chip market in the form of chip on glass (COG). It is estimated that about 60% of the displays use tape automated bonding (TAB) technology. In Japan, COG is typically used for LCDs that are under 6 inches in size. Figure 1 gives typical adoption rates for COG as a function of the panel size.

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For display driver IC to glass interconnect, a key requirement of the process is that it should be low cost, manufacturable and reworkable.

Several methods have been used historically to interconnect driver ICs to the glass. For example, conventional packages like a thin quad flat package (TQFP) on a printed wiring board, which in turn is connected to the glass using flex. A fine pitch chip on tape package like the tape carrier package (TCP) is also currently used. The outputs of the driver IC on the TCP are connected to the glass using anisotropic conductive epoxy. In COG, the bare (unpackaged) driver ICs are mounted directly on the glass panel. Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.

One method to connect the mounted die is by wire bonding the IC to the metallization on the glass. In this method, the interconnects are made to the metallization one bond pad at a time. This method is also not very efficient in

supporting high density or fine pitch interconnect, though it is an inexpensive and mature interconnect method in the industry.

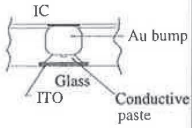
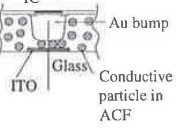
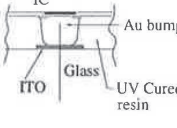
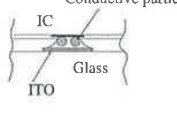
An alternative interconnect process is flip chip on glass (FCOG). FCOG is a system level interconnect and should be treated as such.

## 2. COG

Several methods exist for attaching bare driver ICs on to glass. A review of their technologies along with their key attributes is given in Table 1.

From Table 1 the method that uses modified conventional assembly equipment is stud bumping, which eliminates the need for lithography and associated mask costs. The most common method, however, for COG, is the use of adhesives for accomplishing the interconnect. Figure 2 gives the process flow for these two processes.

Two types of adhesive processes exist: one where the epoxy which facilitates electrical contact between the bump and the trace metallization without itself being in the conduction path, as in UV curable resins, or are in the

| Method                  | Stud Ball Bumps                                                                    | Anisotropic Conductive Film (ACF)                                                  | Micro Bump Bonding (UV Resin)                                                       | Conductive Particle                                                                  |
|-------------------------|------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
|                         |  |  |  |  |
| Interconnect            | Conductive Paste                                                                   | ACF                                                                                | None                                                                                | Conductive Particle                                                                  |
| IC Electrode            | Au Ball on Al Pad                                                                  | Au Bump                                                                            | Au Bump                                                                             | Al Pad                                                                               |
| Conductor on Substrate  | ITO                                                                                | ITO                                                                                | ITO                                                                                 | ITO                                                                                  |
| Pitch ( $\mu\text{m}$ ) | 60-130                                                                             | 150-200<br>(recent work shown up to 40 micron)                                     | 50                                                                                  | 60-130                                                                               |
| Bond Temperature        | 100-120 C                                                                          | 160-180 C                                                                          | room temp                                                                           | 150-200 C                                                                            |
| Bond Pressure           | 1-2 g/pad                                                                          | 20-50 g/pad                                                                        | 10-20 g/pad                                                                         | 10-20 g/pad                                                                          |
| Cure Method             | Thermal                                                                            | Thermal                                                                            | UV                                                                                  | Thermal                                                                              |
| Repairability           | Poor after underfill                                                               | difficult                                                                          | very difficult                                                                      | difficult                                                                            |
| Benefits                | - Flexible bumping method<br>- low capital                                         |                                                                                    | -Low cost<br>High thru'put                                                          | -No bumps needed                                                                     |
| Drawbacks               | -one at a time bumping                                                             |                                                                                    |                                                                                     | -Unreliable connection with Al                                                       |

| Application       | 1995 | 1996 | 1997 | 1998 |
|-------------------|------|------|------|------|
| Character LCD     | 85%  | 100% |      |      |
| 4-6" Panels       | 20%  | 50%  | 100% |      |
| Large panel (7"+) |      | 10%  | 30%  | 70%  |

Fig. 1. COG adoption roadmap.

conduction path as in *Z*-axis (anisotropically) conductive adhesives. Both these systems have been well documented by researchers [2–6]. In the former, an acrylic resin is used which shrinks after cure forming a bond between the bumps and the substrate metallization. There are some issues with this form of interconnect: chip to glass coplanarity and the *Z*-axis adhesive growth due to thermal expansion. In the latter the adhesive itself is in the conduction path of the two electrodes.

The issues of the UV cured resins are overcome in the anisotropic conductive film (ACF) technology. Conductive particles (metallized resin balls) are dispersed in ACF with the conductive particles making contact

with the bumps on the die and with the traces on the substrate. The interconnection is retained by the compressive force between the electrode surfaces due to the shrinkage of the epoxy after curing. During bonding, the adhesive resins are squeezed out and the conducting particles are trapped between the conductor surfaces. Consequently, electrical conduction is restricted to the *Z*-direction while electrical isolation is maintained in the *xy* plane. Conduction can be accomplished in several ways: using metal particles such as Ni- or In-based alloys or gold coated resin particles which are more compliant than the former. Using the latter, one could obtain an ohmic contact carrying current up to 2000 mA per bump with as low an interconnect resistance as 3 mΩ [5]. Typically, the resins that comprise the ACF are thermoplastic, thermoset or a mixture of both. While the advantages of a thermoplastic adhesive are superior reworkability and pot life, they do not have as good adhesive properties as thermosets. The technology has been extended to apply to fine pitch bonding (<40 μm) using a 'double sided ACF' concept [7], where an unfilled top layer

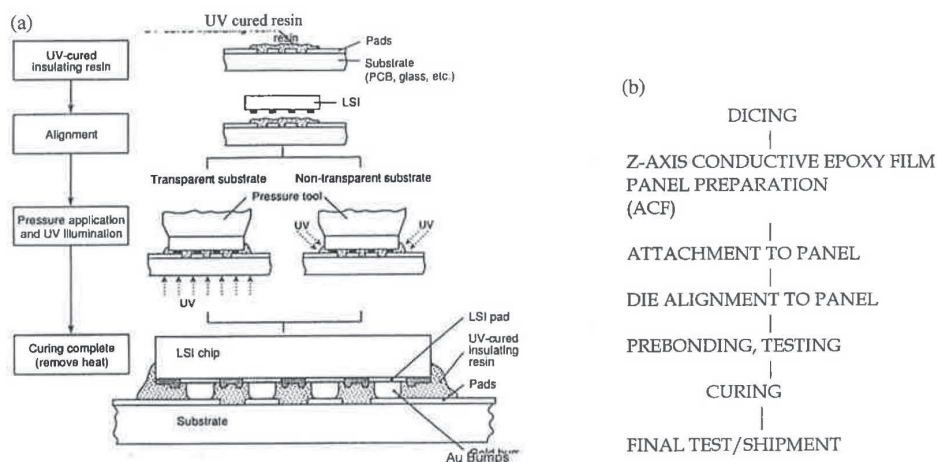


Fig. 2. (A) Process flow using UV cured resin. (B) Process flow for COG using ACF.

of the adhesive film faces the bumps and adds additional insulation between bumps due to its flow properties during bonding.

One issue about FCOG using ACF is that the die does not self-align as in conventional solder-based flip chip, thus requiring excellent alignment capabilities of the bonding equipment [8]

### 3. COG die requirements

The mechanical layout of the die should enable easy implementation of COG.

#### 3.1. bump

Bump area should be maximized to facilitate connection with as large a number of conductive particles as possible. However, in doing this one should also consider that a certain spacing between adjacent bumps needs to be maintained (approximately three times the average conductive particle size in the ACF) to ensure good insulation resistance between bumps. Two approaches are possible: an in-line bump pattern and a staggered bump pattern as shown in Fig. 3. Since one of the objectives of COG is to save as much space on the viewing glass as possible, an orthogonal trace layout with respect to bumps is preferred, hence active bumps on the die width (shorter side) of the driver ICs are not preferred as they can lead to non-optimum fan-out patterns of the ITO traces. Bump metallization traditionally has been plated up 100% Au, though a less expensive method of metallization using electroless nickel has been reported to have been used with good results [9]. Good bump uniformity is required and typical top surface uniformity of the order of a third of the particle size of the ACF is needed so as mechanically to entrap conductive particles between the bump and the metallization trace.

#### 3.2. Die size

Although the use of an ACF does enable some stress relief due to coefficient of thermal expansion mismatch, it is still a concern. Delamination

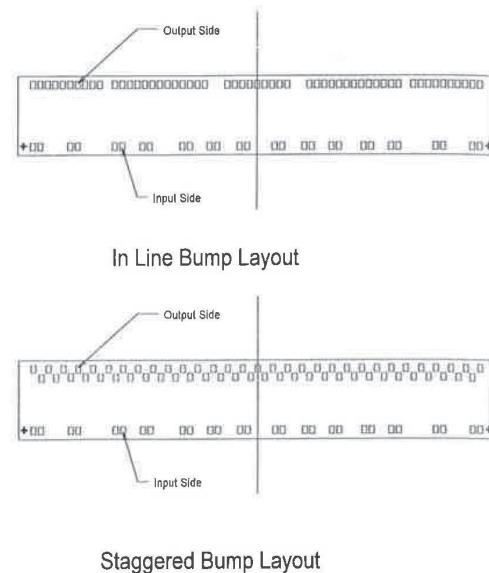


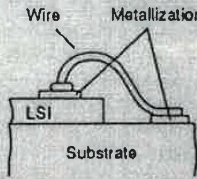
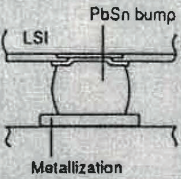
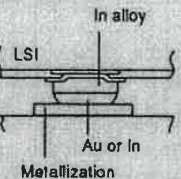
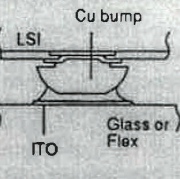
Fig. 3. Bump layouts for COG.

and tensile stress cracking have been reported under Mil Std 883 Schedule B thermal cycling for assemblies made with Z-axis epoxies [10].

In addition, especially at fine pitch, there is an even greater danger of cumulative misalignment between the bumps and the traces during bonding. Most COG bonders place an upper limit of 20mm on the die length for these reasons.

#### 3.3. COG adhesives

As summarized in Tables 1 and 2, using a UV cured adhesive typically results in a difficult to rework process flow and also, by the nature of the chemistries of the materials used in the resin manufacture, there are concerns of electrical instability in accelerated temperature, humidity and bias tests. The UV cured bonding process is fast and occurs at a low temperature resulting in less stress on the die and fewer issues of misalignment due to differing coefficients of expansion.

| Method                 | Wire Bonding                                                                                                | Flip Chip                                                                                           | Low Melting Point Metal                                                                                             | Solder Paste                                                                                           |
|------------------------|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
|                        |                            |                    |                                   |                     |
| Interconnect           | Au or Al wire                                                                                               | solder                                                                                              | In alloy                                                                                                            | conductive paste                                                                                       |
| LSI Electrode          | Al pad                                                                                                      | Pb/Sn bump                                                                                          | Au/In bump                                                                                                          | Cu/Au bump                                                                                             |
| Conductor on substrate | Au, Al                                                                                                      | Au, Cu, Ni, or W                                                                                    | Al, Au, or ITO                                                                                                      | ITO, Cu, or Au                                                                                         |
| Bump Pitch             | min. 150µm                                                                                                  | 200~300µm                                                                                           | 50~150µm                                                                                                            | 150~200µm                                                                                              |
| Bonding Temperature    | 150°C                                                                                                       | 300~350°C                                                                                           | ambient~150°C                                                                                                       | 80~120°C                                                                                               |
| Bonding Pressure       | —                                                                                                           | —                                                                                                   | ~20g/pad                                                                                                            | 1~2g/pad                                                                                               |
| Other                  | —                                                                                                           | —                                                                                                   | —                                                                                                                   | —                                                                                                      |
| Repairability          | OK                                                                                                          | good*                                                                                               | good*                                                                                                               | good*                                                                                                  |
| Benefits               | <ul style="list-style-type: none"> <li>• uses current equipment</li> <li>• no bumps</li> </ul>              | <ul style="list-style-type: none"> <li>• testable IC</li> <li>• reflowable bumps</li> </ul>         | <ul style="list-style-type: none"> <li>• low temp. bonding</li> <li>• Reliable at liquid nitrogen temps.</li> </ul> | <ul style="list-style-type: none"> <li>• low cost</li> <li>• low pressure bond</li> </ul>              |
| Drawbacks              | <ul style="list-style-type: none"> <li>• peripheral pads only</li> <li>• low yield for high I/Os</li> </ul> | <ul style="list-style-type: none"> <li>• high temp. connection</li> <li>• solder fatigue</li> </ul> | <ul style="list-style-type: none"> <li>• Indium bumps are difficult to form</li> </ul>                              | <ul style="list-style-type: none"> <li>• gross pitch</li> <li>• low control of paste spread</li> </ul> |

\*Repairability not good after underfill

Recently, a UV curable, reworkable adhesive has been reported [11].

For ACF adhesives it is recommended to use at least a minimum film thickness of about 80% of the bump height in order to minimize voiding. Some work has been done on fast cure ACF, however rework of these films is difficult as they tend to be thermoset adhesives. In addition, depending on the bump spacing it may be necessary to select an adhesive with a specific particle size as well as either a single or a double layer ACF.

### 3.4. COG equipment

Selection of COG equipment depends on the process used in bonding the die to the substrate.

Alignment accuracy, bonding accuracy, handling systems for both the substrate and the adhesives, process zones (bonding stages and rework stages), throughput and cost are some of the key attributes that need to be considered.

### 4. Other COG technologies

Resin and flexible metal bumps have been studied [10,12] as a means of achieving good thermal cycle reliability and rework at fine pitch. In one method, a polymer bump is plated with gold to form a compliant polymer bump [10] using either a dry etch, wet etch or photo-imagible process. This method still would require an adhesive for connection to the traces,

but being compliant would absorb the mismatch more readily. In the other method, a new photo-thermosetting resin was developed which can adhere to a substrate and flexible indium bumps on the bond pad of the resin. The photoimageable thermosetting resin takes the place of the adhesive in the previous approach.

### 5. COG adoption

From a driver IC manufacturer's view point COG implementation is positive as it enables a faster and lower cost design turn (eliminating TCP tape tool-up time and expenses); however, there are some barriers to an easy adoption of COG for large panel size displays. Some key barriers to COG adoption are: the lack of ease of rework during assembly as well as during field repairs. While this may not be a critical issue for small panel size low resolution displays, it is a concern for large panel size displays which often use several row and column driver ICs. In addition, there is a need to invest in new equipment to assemble COG devices with a probably lower throughput as compared to the conventional TCP row and column driver ICs. The perception of a larger than TCP 'dead space' for COG versus the TCP (flex) package has not helped in facilitating a quick adoption. The interconnect resistance of the COG interconnect has been a concern, especially for large high resolution panels, but with new adhesive technology available it has approached that of the TCP package.

With high resolution driving pixel size, outer lead pitch bonding is likely to shrink and with IC manufacturers shrinking their die sizes to meet the cost targets the inner lead pitch bonding is likely to shrink as well. For high resolution displays with fine pixel size there is a possibility of greater misalignment between the TCP outer leads and the substrate metallization traces. Below 50  $\mu\text{m}$  inner lead pitch bonding there are concerns about TCP lead strength, cost, especially for the flex tape, and at which

point COG will be a compelling interconnect technology for large panels. The emerging technology in the area of repair/rework of COG both during bonding and in field service is an exciting one and should benefit the industry upon its maturity.

### 6. Conclusion

Key COG technologies have been reviewed with their attributes. Factors that need to be considered when designing or implementing COG with respect to the driver IC and the materials and equipment have been discussed. Hindrances to COG adoption for large panel size displays have been discussed at length as well as when COG could become a compelling system interconnect technology of choice for LCD displays.

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