

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case IPR2024-00973
Patent No. 9,184,157

REPLY DECLARATION OF PATRICK MURPHY, PH.D., P.E.

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I. INTRODUCTION

1. I, Dr. Patrick Murphy, submit this declaration to state my opinions on the matter described below. I am over the age of 21 and I am competent to make this declaration.

2. I have been retained by counsel for BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”), as an independent expert in this proceeding before the United States Patent and Trademark Office (“USPTO”). I am a salaried employee of Exponent. Exponent charges \$575 per hour for my time plus expenses for work performed in connection with this project, and I am being paid my regular salary for time spent on this project. I have received no additional compensation for work in this case. My compensation does not depend upon the contents of this declaration, any testimony I may provide, or the ultimate outcome of the case. I have no other interest in this proceeding.

3. I am aware that this proceeding involves U.S. Patent No. 9,184,157 (“the ’157 patent”) (Ex. 1001).

4. I previously provided my opinions as to the patentability of claims 1-18 of the ’157 patent in the Declaration of Patrick Murphy, Ph.D., P.E., in Support of Petition for *Inter Partes* Review of U.S. Patent No. 9,184,157, which I understand was filed as Exhibit 1003.

5. I understand that, after my previous declaration was filed, the Patent Owner filed a Patent Owner's Response (Paper 17) and the Declaration of E. Fred Schubert, Ph.D., in Support of Patent Owner's Response (Ex. 2009, "Schubert Declaration"). I have reviewed both Patent Owner's Response and the Schubert Declaration.

6. I have been asked to consider the arguments made by Dr. Schubert in the Schubert Declaration. While I have responded to the positions taken by Dr. Schubert in the Schubert Declaration, I note that the arguments in the Patent Owner's Response appear to parallel the Schubert Declaration in many respects. As such, my rebuttals here apply equally to the Patent Owner's Response.

7. As discussed in my previous declaration, it is my opinion that claims 1-18 of the '157 patent would have been obvious based on *Reiner* (Ex. 1005) (Ground 1) or, alternatively, based on the combination of *Reiner* and *Takahara* (Ex. 1006 (original document); Ex. 1007 (English translation)) (Ground 2). *See* Ex. 1003.

8. After reviewing the Schubert Declaration and Patent Owner's Response, my opinion has not changed. It is still my opinion that claims 1-18 of the '157 patent would have been obvious based on *Reiner* (Ground 1) or, alternatively, the combination of *Reiner* and *Takahara* (Ground 2), as set forth in my previous declaration. *See* Ex. 1003.

9. My opinion does not change regardless of whether I apply my definition of a person of ordinary skill in the art in my previous declaration or the definition of a person of ordinary skill in the art specified in Dr. Schubert's declaration, as explained below.

10. I am qualified as a person of ordinary skill in the art under either definition and I am competent to opine and offer expert testimony regarding a person of ordinary skill in the art under either definition at the '157 patent's earliest priority date of July 5, 2004.

II. EXPERIENCE AND QUALIFICATIONS

11. My experience and qualifications are recited in my previous declaration filed as Exhibit 1003.

12. My curriculum vitae has been submitted as Exhibit 1004.

III. MATERIALS CONSIDERED

13. In forming my opinions, I have reviewed my prior declaration. I also reviewed the materials listed below and any other materials cited throughout my declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,184,157 to Kobashi ("the '157 patent")
Ex. 1002	File History for U.S. Patent No. 9,184,157

Reply Declaration of Patrick Murphy, Ph.D., P.E.
U.S. Patent No. 9,184,157

Exhibit	Description
Ex. 1003	Declaration of Patrick Murphy, Ph.D., P.E., in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,184,157
Ex. 1005	International Publication No. WO 03/019657 A2 to Reiner et al. (“ <i>Reiner</i> ”)
Ex. 1006	Japanese Patent Application Publication No. JP2003-121875 to Takahara
Ex. 1007	Certified English Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara (“ <i>Takahara</i> ”)
Ex. 1008	Certificate of Translation of Japanese Patent Application Publication No. JP2003-121875 to Takahara to English
Ex. 1009	Japanese Patent Application Publication No. JP2001-166334 to Murai
Ex. 1010	Certified English Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai (“ <i>Murai</i> ”)
Ex. 1011	Certificate of Translation of Japanese Patent Application Publication No. JP2001-166334 to Murai to English
Ex. 1012	James E. Vinson & Juin J. Liou, “Electrostatic Discharge in Semiconductor Devices: An Overview,” Proceedings of the IEEE, Vol. 86, No. 2, pp. 399-418 (Feb. 1998)
Ex. 1013	Toshio Murakami et al., “Electrostatic problems and ionization solutions in TFT-LCD Production,” Solid State Technology, Vol. 40, No. 1, pp. 99-102 (Jan. 1997)
Ex. 1019	Un-Byoung Kang and Young-Ho Kim, “A New COG Technique Using Low Temperature Solder Bumps for LCD Driver IC Packaging Applications,” IEEE Transactions on Components and Packaging Technologies, Vol. 27, No. 2, pp. 253-258 (IEEE June 2004) (“ <i>Kang</i> ”)

Exhibit	Description
Ex. 1020	Rajeev Joshi, “Chip on glass—interconnect for row/column driver packaging,” <i>Microelectronics Journal</i> , Vol. 29, No. 6, pp. 343-349 (Elsevier Science Limited June 1998) (“ <i>Joshi</i> ”)
Ex. 1021	Fei-Jain Wu et al., “Assembly of a Prototype Flip-Chip-On-Glass Liquid Crystal Display,” 1995 Proceedings 45th Electronic Components and Technology Conference, pp. 674-681 (IEEE 1995) (“ <i>Wu</i> ”)
Ex. 1022	<i>Random House Webster’s Unabridged Dictionary</i> (Random House 2d ed. 2001) (definition of “each”)
Ex. 1023	<i>The American Heritage® Dictionary of the English Language</i> 560 (Houghton Mifflin Co. 4th ed. 2000) (definition of “each”)
Paper 17	Patent Owner’s Response
Ex. 2008	Deposition Transcript of Patrick Murphy, Ph.D., P.E.
Ex. 2009	Declaration of E. Fred Schubert, Ph.D., in Support of Patent Owner’s Response

IV. LEGAL STANDARDS

14. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is set forth in Exhibit 1003 and is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

V. PERSON OF ORDINARY SKILL IN THE ART

15. In my prior declaration, I explained my opinion that a person of ordinary skill in the art (“POSITA”) pertinent to the ’157 patent as of its earliest priority date would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional relevant work experience can compensate for less education, and *vice versa*. For example, a master’s degree in electrical engineering, computer science, physics, or a similar field can be a substitute for two years of experience designing semiconductor display devices.

16. I understand that Dr. Schubert has provided his opinion that a POSITA would have “at least a bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least four years of experience designing semiconductor display devices, including LCD displays; a master’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays; or a Ph.D. in electrical engineering, computer science, physics, or a similar field and at least one year of experience designing semiconductor display devices, including LCD displays.” Schubert Declaration ¶21.

17. Notwithstanding my disagreement with Dr. Schubert's definition, I am qualified as a POSITA under Dr. Schubert's definition.

18. I am competent to testify to the understanding of either my definition or Dr. Schubert's definition of a POSITA at the earliest claimed priority date of the '157 patent: July 5, 2004. My opinions would not change if I assumed a later date of invention.

19. As I explain in my previous declaration, the claims of the '157 patent would have been obvious to a person of skill in the art under my definition of a POSITA. Considering the prior art and claims under Dr. Schubert's definition does not change my opinion. Dr. Schubert believes that a POSITA would have additional work experience. A POSITA with that additional experience would still have found the claims obvious because a POSITA under that definition would have known even more than a POSITA under my definition that would have already found the claims obvious.

20. As such, Dr. Schubert's definition does not change that, in my opinion, claims 1-18 of the '157 patent would have been obvious to a POSITA based on *Reiner* (Ground 1) or, alternatively, the combination of *Reiner* and *Takahara* (Ground 2), as stated in my previous declaration.

VI. REINER DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-18

21. After having reviewed Dr. Schubert's Declaration, it is still my opinion that a POSITA would have found claims 1-18 obvious based on *Reiner*. This remains my opinion both under my definition of a POSITA and under Dr. Schubert's definition of a POSITA.

A. Reiner Discloses or Renders Obvious Claim 4¹

1. Reiner Discloses or Renders Obvious the Claimed Input Terminals ([4c]) (POR 22-24)

22. In my opinion, *Reiner* discloses or renders obvious element [4c] for the reasons set forth in my previous declaration.

23. Dr. Schubert asserts that *Reiner*'s source driver 61's "input terminals would not be input terminals of the display device," and that "a POSITA would understand that LCD display 60 may include separate input terminals for separate power supply lines, because LCD display 60 is formed on a separate substrate." Schubert Declaration ¶¶59-60.

¹ Dr. Schubert, throughout paragraphs 56-84 (discussing claim 4), repeats many of the same arguments discussed below in various places. Even if I do not expressly discuss the same argument in each section, my opinion regarding an argument applies to everywhere it is discussed by Dr. Schubert.

24. Dr. Schubert is mistaken as to what constitutes the claimed “display device” in *Reiner* and how a POSITA² would have understood the “display device” in claim 4.

25. As an initial matter, *Reiner*’s item 60 is the “LCD *screen* 60,” and the entire device, shown in *Reiner*’s FIG. 4, also includes at least the gate driver 63 and source driver 61. *Reiner*, 9:23-34 (emphasis added), FIG. 4.³ Indeed, the ’157 patent in FIG. 6 depicts a “display device according to a first embodiment” of the alleged invention that includes “one or a plurality of external ICs” (e.g., external to the active matrix substrate) for supplying “necessary electrical signal and potential.” *See* Ex. 1001, 4:42-44, 6:47-49, 6:58-64, FIG. 6.

26. Indeed, a POSITA reading the prosecution history of the ’157 patent would have recognized that the applicant excluded Dr. Schubert’s interpretation that the power lines for the “display device” must be for the screen pixels. *See* Ex. 1002, 182 (stating that “[s]pecifically, the pixels of Lee cannot reasonably be considered to correspond to the claimed semiconductor circuit”). A POSITA

² Unless stated otherwise, my references to a POSITA apply to both my definition of a POSITA and Dr. Schubert’s definition of a POSITA.

³ For consistency with my previous declaration, my citations to *Reiner* are to the exhibit page numbers (e.g., “Page x of y”) at the bottom of Exhibit 1005.

reading the claim also would understand this because the '157 patent does not recite the screen pixels in any of its claims. *See* Ex. 1001, claims 1-18.

27. A POSITA would have also understood from reading the '157 patent that Dr. Schubert's interpretation is not supported because the '157 patent also does not disclose that any "input terminals" for the power supply line connected to the scanning line drive circuit *must also* provide power to the pixels of the display matrix. *See generally* '157 patent.

28. As I explain in my previous declaration, *Reiner* suggests or renders obvious the use of input terminals for powering power supply lines Vdd and Vss of the source driver 61 and data driver 63. *See* Ex. 1003, ¶¶96-102.

29. Dr. Schubert also asserts that "[n]othing in *Reiner* suggests that lines Vss and Vdd also supply power to the LCD display 60," and "LCD display 60 may include separate input terminals for separate power supply lines, because LCD display 60 is formed on a separate substrate." Schubert Declaration ¶60. Again, Dr. Schubert misunderstands *Reiner*'s disclosure. A POSITA would have known and understood that a "display" or "display device" would include control driver circuits in addition to the screen. Ex. 2008, Murphy Tr., 93:9-94:1. It would not be limited to the "LCD screen 60" as Dr. Schubert suggests because the "display" of *Reiner*'s FIG. 4 also includes at least the driver circuits 61, 63. *Reiner*, 9:11-15, 9:23-10:10, FIG. 4.

30. As I explain above, *Reiner*'s "Fig. 4 is a block diagram of a display with display drivers." *Reiner*, 6:7, 9:23-34, FIG. 4. The "LCD screen 60" is part of the display, but the display device also includes at least the drivers 61, 63 to power the LCD screen, as shown in FIG. 4. This is confirmed by FIG. 3 and *Reiner*'s disclosure that the drivers are "flipped onto the substrate 16, according to the well-known flip-chip technology." *Reiner*, 7:23-26. I explain more about flip chip technology below and in my original declaration at Ex. 1003, ¶101. *See also* Ex. 1003, ¶¶120, 145, 231, 233, 251 (citing *Reiner*'s discussion of "flip-chip technology" at 7:23-25). That *Reiner*'s display device includes the driver circuits is also confirmed by FIG. 5, which shows the driver circuits bonded to the contact pad 72 of the scan/source lines for the LCD screen 60.

31. *Reiner*'s FIG. 4 shows the display device, which includes, but is not limited to, "LCD screen 60." *Reiner*, 9:23-29 ("Before addressing details of a display driver 61 in accordance with the present invention, a brief description of Fig. 4 is given. ***This Fig. shows a schematic block diagram of an LCD display with control circuitry. The LCD display comprises an LCD screen 60 with a plurality of source lines 67 and a plurality of gate lines 68. A source driver module 61 is employed to drive the individual source lines 67. A gate driver 63 is employed that usually drives one whole gate line 68.***" (emphases added)).

32. Dr. Schubert's misunderstanding appears to come from *Reiner*'s single mention of "LCD display 60," which he then extrapolates while isolating this from all other discussions of *Reiner*. A POSITA would not have understood that this means item 60 is the entire display device at least because *Reiner* refers twice to "LCD screen 60" and states that the "LCD display *comprises* an LCD screen 60," but is *not limited to* the screen. *Reiner*, 9:25-27 (emphasis added), 10:1-3, FIG. 4. As a matter of basic design and engineering, a POSITA would have understood that the "display device" comprises more than just the pixel matrix screen. It includes at least the drivers that power and make the device operational as shown in *Reiner*'s FIGS. 3, 4, and 5.⁴ This is confirmed by *Reiner*, which explains that the LCD display in FIG. 4 "employ[s]" drivers to drive the gate lines 68 and source lines 67. *Reiner*, 9:23-28, FIG. 4. It is confirmed also by the use of "flip-chip technology," such as in FIG. 3, and FIG. 5's description of the driver being connected to the "contact pad" of the scan/source lines, such as by pins. *Reiner*, 7:22-26, 10:1-6, FIGS. 3, 5.

⁴ It may typically also include additional components, such as input/output connections to external devices, external power connections, audio connections, etc.

33. A POSITA would have understood that these descriptions describe conventional flip-chip technology, which is also called “flip chip on glass” or “FCOG,” and is also referred to as “chip on glass” or “COG.” Flip chip refers to directly mounting the IC driver circuit (e.g., *Reiner*’s gate driver 63 and source driver 61) on the glass substrate having the screen pixels. Ex. 1019, *Kang*, 1⁵ (“[T]he use of chip on glass (COG) technique is proposed for a number of products such as high pixel density and small area LCDs. In this technique, ***the driver IC is directly mounted on LCD panels by flip chip.***” (emphasis added)); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to ***mount the driver IC directly on to the glass LCD.*** FCOG and COG offer the highest density possible in packaging,” and “[i]n COG, the bare (unpackaged) ***driver ICs are mounted directly on the glass panel.*** Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.” (emphases added)); Ex. 1021, *Wu*, 20 (“With increasing needs for higher resolution displays, higher density interconnect technology becomes inevitable. ***Direct mounting of flip chip onto glass*** using ACA’s (see Figure 1) became the

⁵ My citations to exhibits are to the exhibit page numbers (e.g., “Page x of y”) in the bottom corners.

topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.” (emphasis added)).

34. As such, Dr. Schubert misapprehends *Reiner*’s disclosure.

35. I also observe that he does not appear to refute that the power lines shown in *Reiner*’s FIG. 5 would supply power to the gate and source drivers, as I explain in my previous declaration, which meets the claim language. He also does not appear to dispute the obviousness of the input terminals for powering the gate and source drivers, which I explain in my previous declaration. *See* Ex. 1003, ¶¶96-102.

2. *Reiner* Discloses or Renders Obvious the Claimed First and Second Protection Circuits Connected to a Scanning Line Driving Circuit ([4d]-[4f])

36. Dr. Schubert states that he “[d]isagree[s] with [my] opinion that *Reiner* discloses protection circuits connected to a scanning line driving circuit and arranged as claimed” because, “[i]n [his] opinion, *Reiner* discloses ... only an ESD protection network within a source (data line) driver IC chip.” Schubert Declaration ¶63. Dr. Schubert also asserts that *Reiner* “fails to show that *Reiner* discloses or renders obvious applying *Reiner*’s source driver ESD protection network to a gate driver so that the layout would remain the same.” Schubert Declaration ¶¶62-63. I disagree both on *Reiner*’s disclosure and his characterizations of my previous declaration. Indeed, Dr. Schubert appears to be

taking an overly narrow reading of *Reiner*, failing to read it as a POSITA would have understood it. Dr. Schubert's extremely narrow reading is at odds with the skill of a POSITA, under either definition, who has an engineering degree and work experience. A POSITA would have been more than capable of recognizing that *Reiner*'s FIG. 5 applies to both gate and source drivers.

37. As I explain in my previous declaration, *Reiner* does not limit itself to ESD protection on the source driver. *See* Ex. 1003, ¶¶93-133. For example, *Reiner* explains that its “present invention relates to integrated circuit devices with ESD protection,” and “[a] typical example is an integrated circuit display driver 61 *or* 63 that is designed to drive many lines of an LCD display 60, as illustrated in Fig. 4.” *Reiner*, 2:1-3, 9:12-14 (emphasis added). *Reiner* also does not differentiate between gate driver 63 and source driver 61 when explaining that “integrated circuit devices, such as CMOS devices[,] for example, comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1. Given that these paragraphs in *Reiner* discuss gate drivers and source drivers together with respect to ESD protection, a POSITA would have understood that *Reiner* discloses providing ESD protection for *both* source driver 61 and gate driver 63, as I previously explained. Ex. 1003, ¶¶103-133.

38. As I explain in my previous declaration, although *Reiner*'s FIG. 5 expressly labels source driver 61, a POSITA would have understood that the protection network applies equally to gate driver 63. Ex. 1003, ¶¶105, 111-120, 150, 238-242.

39. Dr. Schubert spends several paragraphs arguing that "differences between a source driver and a gate driver" would have precluded a POSITA from finding the claims obvious. *See* Schubert Declaration ¶¶63-68. I disagree with Dr. Schubert that any such differences would have rendered the claims nonobvious. Even if the differences he identifies were present, they would not have prevented a POSITA from finding it obvious to apply *Reiner*'s ESD protection network to a gate driver because they are immaterial to ESD protection. Indeed, some of Dr. Schubert's alleged "differences" actually highlight the similarities that would have made it more obvious to a POSITA.

40. As one example, where Dr. Schubert asserts that "Reiner discloses that the gate driver integrated circuit comprises individual gate drivers, not output devices 70" (Schubert Declaration ¶¶64, 65), he appears to misunderstand how gate and source drivers operate by alleging that the same general structure is somehow different. A POSITA would have known and recognized that "individual gate drivers" that "drive one whole gate line 68" describes a gate driver unit for each gate or scan line, which is the same as the individual driver units 70 shown in

FIG. 5 to drive each individual line (like the individual source driver units that drive each individual source line). *See Reiner*, 9:27-28. Indeed, the '157 patent explains that this setup is conventional, as shown in FIG. 11. It was, in fact, commonplace and conventional. Because a gate driver line circuit (e.g., what would be inside box 70 in *Reiner*'s FIG. 5) is used to drive each gate line to turn it on and off, there would have been a driver unit for each line to control and time the scanning of the display. As such, Dr. Schubert's alleged "difference" actually **supports** applying *Reiner*'s ESD protection network in FIG. 5 to gate driver 63 because that network protects **any** circuit inside box 70 whether it has a gate driver line unit configuration or a source driver line unit configuration. *See* Ex. 1003, ¶111 (explaining that a POSITA would have recognized that line unit circuit 70 is a "black box," and any circuit inside would be protected by *Reiner*'s ESD protection network).

41. *Reiner*'s teaching that the "ESD protection network" in FIG. 5 protects each of the individual line drivers (e.g., unit 70) and the "invention" provides for "integrated circuit devices with ESD protection," while explaining that "typical examples" of "integrated circuit devices" being protected can be either "integrated circuit display driver 61 **or** 63," strengthens, not hinders, my opinion that a POSITA would have found it obvious to use *Reiner*'s ESD protection network of FIG. 5 to protect each of the scan line driver units. *See*

Reiner, 2:2-3, 3:4-8, 4:15-16, 8:8-15, 9:11-22 (emphasis added), FIGS. 3-5.

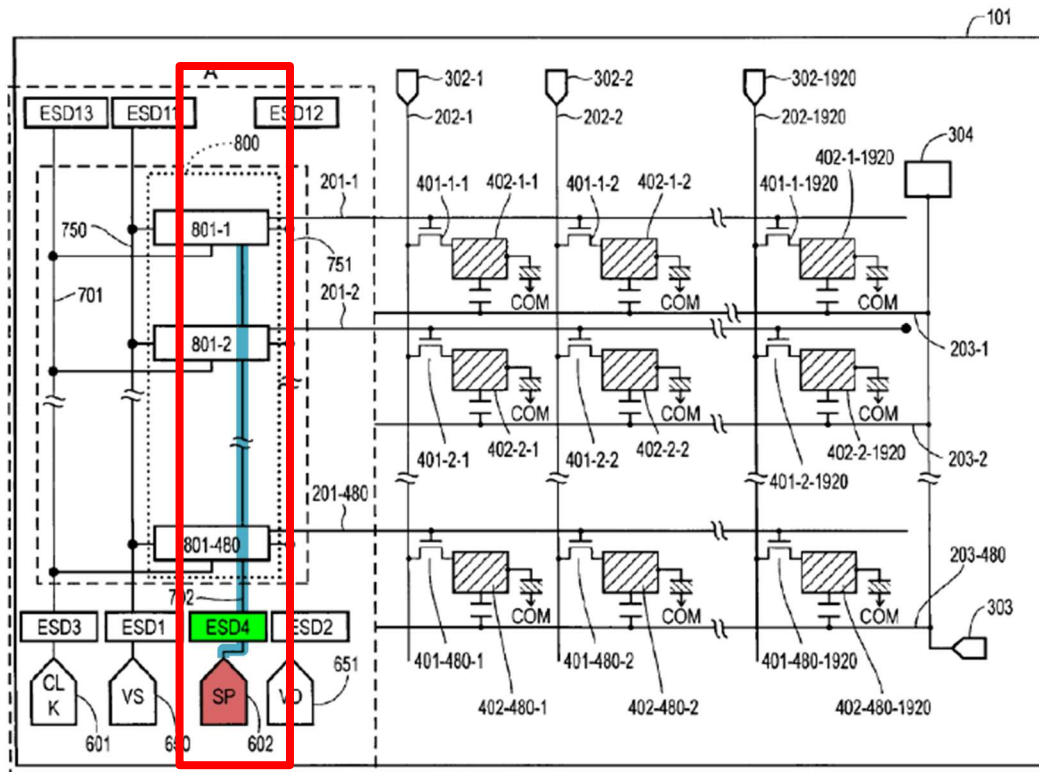
Indeed, this would have made the most sense because, as I explained before and Dr. Schubert does not appear to dispute, an LCD display can be rendered unacceptably or irreparably damaged if either the gate driver (scanning line driving circuit) or the source driver (data line driving circuit) is damaged by ESD because damage to either driver impairs activating parts of the screen, such as pixel rows or columns of the LCD screen. Ex. 1003, ¶¶103-133; *Reiner*, 2:28-3:3. A POSITA would not have overlooked this disclosure.

42. Dr. Schubert also asserts that “a POSITA would expect to see differences between the gate driver arrangement and the source driver arrangement,” for example, “that individual gate/scan line drivers are coupled to one another, to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time (e.g., one would not simultaneously turn ON two horizontal rows of transistors).” Schubert Declaration ¶66. Dr. Schubert claims to identify additional differences in paragraph 67 of the Schubert Declaration. *See* Schubert Declaration ¶67. A POSITA would not have found that any of these differences are material to whether *Reiner* discloses or renders obvious the claims of the ’157 patent. Indeed, many do not relate to the claimed structures at all, as I explain below.

43. Regarding the “coupling” of gate driver units together (*see* Schubert Declaration ¶¶66-67), the means for such coupling (e.g., lines or other structures that Dr. Schubert suggests but fails to depict or define) would be understood by a POSITA to be within the “black box” line driver unit 70 of *Reiner*’s FIG. 5, and thus not material to whether a POSITA would have found it obvious to protect against ESD on the power lines Vss and Vdd shown in *Reiner*’s FIG. 5 and recited in the claims of the ’157 patent.

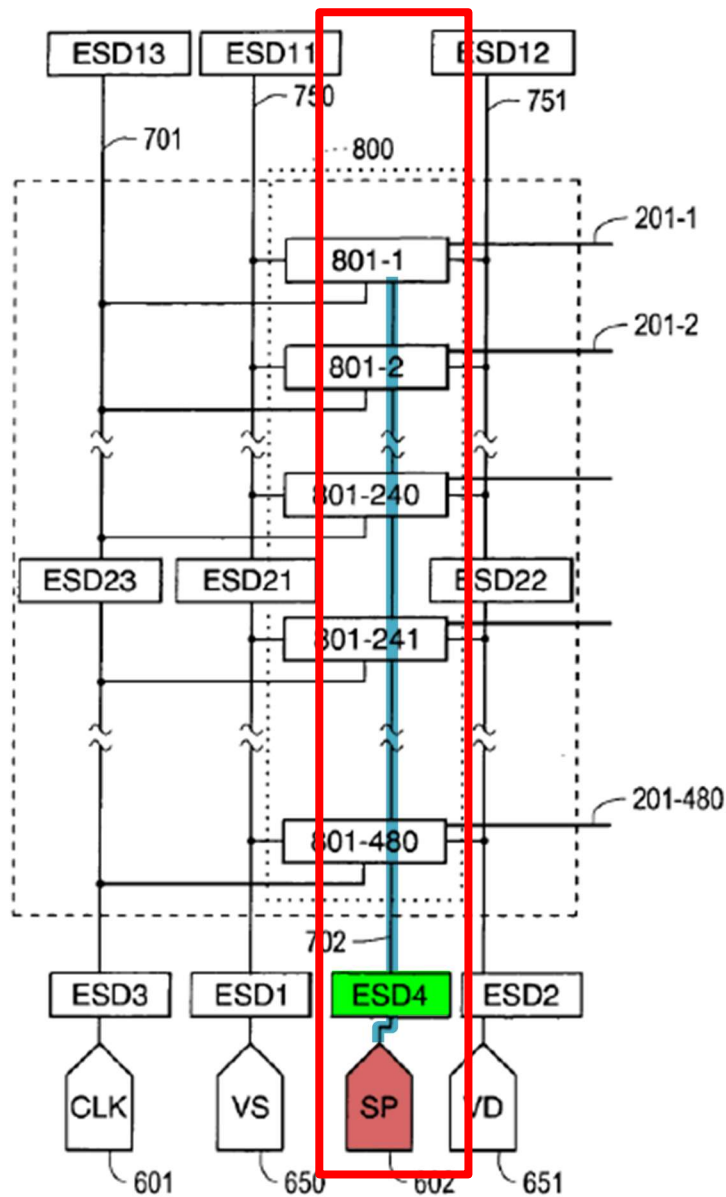
44. I would also note that the ’157 patent does not view this as a material difference either. As shown in ’157 patent FIGS. 1 and 2, the signal line SP **does not have** the additional claimed ESD protection circuits that the ’157 patent purports are its invention, and does not affect the ESD protection on the power lines VD and VS. As shown below, the ’157 patent FIGS. 1 and 2 show additional ESD protection circuits ESD11, ESD12, and ESD13 on the lines VS, VD, and CLK, respectively. FIG. 2 also shows ESD protection circuits ESD21, ESD22, and ESD23 at the center of lines VS, VD, and CLK, respectively, between the two middle driver units 801-240 and 801-241. Signal line SP contains no such additional protections, as I show below. A POSITA would not have viewed this signal line as material to protecting the gate driver circuit units from ESD on other lines, such as the power line or scan lines.

FIG. 1



Ex. 1001, FIG. 1 (annotated).

FIG. 2



Ex. 1001, FIG. 2 (annotated).

45. Dr. Schubert's four alleged differences in paragraph 67 are also either not relevant to whether a POSITA would have found it obvious to protect a scanning line driving circuit from ESD by providing ESD protection circuits

connected to a power line, or they actually support the similarities such that a POSITA would have found it obvious.

46. Dr. Schubert's "[f]irst" position that individual gate driver units may be connected to operate as a shift register (e.g., the SP line in the '157 patent) (Schubert Declaration ¶67 (bold emphasis omitted)) is not material to protecting the driver units by ESD protection circuits coupled to the power lines for the reasons explained above.

47. Dr. Schubert's "[s]econd" and "[t]hird" positions that gate lines are driven one at a time and source lines are driven together (Schubert Declaration ¶67 (bold emphases omitted)) is also not material because that relates to the operation of the signal lines, not protection by connecting ESD protection circuits to the power lines during manufacturing when ESD is most likely to occur. Moreover, as I also explain above, this supports obviousness because each of the gate and source drivers has one driver circuit per line such that the overall structure is similar. Because *Reiner*'s ESD protection network in FIG. 5 would have been understood to protect whatever circuit is in box 70, a POSITA would have found it obvious to apply *Reiner*'s ESD protection to gate driver 63. *See* Ex. 1003, ¶¶103-133.

48. Dr. Schubert's "[f]ourth" position that "a specific ESD protection arrangement that works for source drivers would not necessarily be known to work as ESD protection for a gate driver" (Schubert Declaration ¶67 (bold emphasis

omitted)) appears to tacitly acknowledge, correctly in my opinion, that ESD protections *could* work for gate drivers.⁶ A POSITA would have understood that *Reiner*'s ESD protection in FIG. 5 protects whatever circuit is in box 70, because it protects each of the lines connecting box 70 to the output line (e.g., gate or source line) and the power lines. By protecting all of these connections, a POSITA would have recognized that *Reiner*'s ESD protection circuit network protects whatever is in box 70 as a "black box" because it prevents ESD from damaging the circuit, irrespective of the specific way in which the circuitry is implemented. *See* Ex. 1003, ¶111; *Reiner*, 9:18-22; *see also Reiner*, 4:15-16, 9:11-22 (describing protecting "integrated circuit[s]" generally). By "black box," I mean that a POSITA would have understood that *Reiner*'s ESD protection network in FIG. 5 protects the circuitry inside box 70, but that the circuitry's specific configuration is not material to this protection because the purpose of ESD protection circuits is to prevent the ESD from proceeding past the protection circuit to whatever is on the

⁶ I note that Dr. Schubert stops short of saying that *Reiner*'s ESD protection circuit would not work for a gate driver. As explained above and in my previous declaration, a POSITA would have recognized that it would have understood this use from *Reiner* or at least found this use obvious and expected that use to be successful. Ex. 1003, ¶¶103-133.

other side. *See* Ex. 1003, ¶111. This is a like a fence around a yard—it protects the yard from intrusion (ESD events), regardless of what the landscaping is like within the yard (e.g., whether it has a pool or a patio in the yard). A POSITA would have understood that both the gate drivers and source drivers within a device are composed of the same materials (e.g., CMOS), same circuit devices (e.g., transistors), similar circuit designs, same substrate, etc., and as such, the ESD protection network *Reiner* describes for FIG. 5 would have been expected to protect either source driver circuitry or gate driver circuitry equally. *See* Ex. 1003, ¶¶97, 105, 111, 113, 117, 120. This is borne out by that fact that *Reiner*’s ESD protection network in FIG. 5 is agnostic to the composition and layout of the circuits in box 70 because the very purpose of the ESD protection network is to prevent ESD from entering box 70, making the internal composition and layout of box 70 (e.g., source driver circuit or gate driver circuit) immaterial.

49. As I explained in my previous declaration and above, *Reiner* discloses that the ESD1-ESD3 protect any circuitry inside of the driver units 70, but the exact circuitry is like a “black box” and would be protected because each of the connections into unit driver 70 is protected from ESD discharge in *Reiner*’s FIG. 5. *See* Ex. 1003, ¶111; *Reiner*, 9:18-22; *see also Reiner*, 4:15-16, 9:11-22 (describing protecting “integrated circuit[s]” generally).

50. Even if the signal lines (SP) between gate driver units are relevant to the final operation after manufacturing is complete, they would not have affected a POSITA's understanding of *Reiner*'s "bump bridges" that allow for crossing a metal line (signal lines are metal lines) and also providing "integrated circuit devices with ESD protection." *Reiner*, 2:1-3, 4:29-34, 5:16-20, 7:16-18, 9:8-22, 10:20, 11:6-10, 12:4-7, FIGS. 2, 3. In other words, many of Dr. Schubert's alleged "differences" do not relate to whether a POSITA would have found it obvious to use *Reiner*'s protection network coupled to ***power lines*** and the scanning line driving circuit (gate driver), and do not change my opinion that a POSITA would have found it obvious to do so, as stated in my previous declaration. For example, as I previously explained, both gate driver units and source driver units (e.g., units 70 in both) comprise transistors and CMOS devices, which are the types of devices that *Reiner* discloses protecting. *See Reiner* 2:28-3:1 (explaining that CMOS devices are very sensitive and need to be protected); Ex. 1003, ¶97.

51. Dr. Schubert's apparent position that a POSITA would have accepted "destroy[ing]" the "very sensitive circuits" of a gate/scan line driver on the power line, rather than protect the power lines as taught by *Reiner*, would have been flatly rejected by a POSITA. To the contrary, in my opinion, a POSITA reading *Reiner* would have immediately recognized the desire to protect both driver types and would have started with the ESD protection disclosed in *Reiner*'s FIG. 5 to protect

the gate driver. A POSITA would have done this based on the immediate recognition that damage to a single gate driver can possibly affect the operation of multiple gate line unit driving circuits because (as Dr. Schubert points out in paragraph 67 of the Schubert Declaration) each is in communication with the two neighboring gate drivers. Additionally, a POSITA would have recognized that destruction by ESD damage of either source driver or gate driver units is detrimental to the overall function of the display device. Because *Reiner* already discloses an ESD protection network suitable for driver units, a POSITA would have found it obvious to use that network, as I explain in my previous declaration. Ex. 1003, ¶¶103-133.

3. *Reiner* Discloses or Renders Obvious the First Protection Circuit Connected to the Power Supply Line Between a First Connecting Portion and the Input Terminals ([4e])

52. Dr. Schubert has asserted that

Dr. Murphy's interpretation of claim 4 [in Figures Ax, Bx, and Cx of Exhibit 1003] defeats the purpose of the claimed invention, which places a power supply line protection circuit between that power supply line's input terminal (of the display device) and the power supply line's connection to the scanning line driving circuit, to protect the scanning line driving circuit from charges that could enter the device through the input terminal and travel along the power supply line and damage the scanning line driving circuit. More important, limitation 4[e] understood in context

with limitation 4[f] confirms that claim 4 plainly recites a scanning line driving circuit—rather than, for example, individual scanning line driving units—between two protection circuits.

Schubert Declaration ¶72. I disagree.

53. The '157 patent describes its purported improvement as providing ESD protection away from the input terminals: “[T]here is an effect that *the protection against the static electricity is sufficiently obtained even in a place far from the terminal*, by providing internal protective circuits in an area which is not connected to the input terminals of the wiring lines as well as providing the protective circuits around the input terminals as in the conventional art.” Ex. 1001, 3:6-11 (emphasis added); *see also* Ex. 1001, 3:15-17 (“[I]t is possible to prevent the static electricity or noise input from the input terminals, and to protect a semiconductor circuit *far from the input terminals*.” (emphasis added)). The '157 patent explains that, in one example, the 120th, 240th, and 360th driver units are considered “far from” other protection and need protecting against ESD in those regions. Ex. 1001, 7:20-59. The '157 patent also describes placing additional ESD protection circuits between every individual driver unit. Ex. 1001, 7:20-59. A POSITA would have recognized that the claim’s language refers to different combinations of these protection circuits, as I explain in my previous declaration.

54. A POSITA would not have understood, as Dr. Schubert asserts, that *all* of the connecting portions of the scanning line driving circuit must be between the first and second protection circuits because the '157 patent discloses examples where the protection circuits are between some of (but not all of) the connecting portions that connect the scanning line driving circuit with the power line. *See* Ex. 1001, 7:20-59, FIG. 2. This is consistent with my Figures Ax, Bx, and Cx in my previous declaration.

55. I note that Dr. Schubert asserts that, “in [his] opinion, the claimed first protection circuit must be connected to the power supply line *between*, as claimed, that power supply line’s connection *to any portion of the scanning line driving circuit and the power supply line’s input terminal*.” Schubert Declaration ¶73 (bold italics emphasis added, regular italics original). I disagree. Claim 4 recites only one connection between the scanning line driving circuit and the power line: “a first connecting portion.” A POSITA, reading the '157 patent and the claims, would have recognized that a “portion” may be part of the whole, e.g., only one of the scanning-line-driving-circuit-to-power-line connections, not *all* of them, as Dr. Schubert asserts. As I explain above, my Figures Ax, Bx, and Cx in my previous declaration are consistent with the other embodiments described under the “Second Embodiment” heading of the '157 patent.

56. Dr. Schubert's discussion in paragraph 74 is flawed for the same reason because, even if one ESD1 or ESD2 connection is at the same location as one of the connecting portions of the scanning line driving circuit, there are other "first connecting portion[s]" between the scanning line driving circuit and the power lines, as shown in Figures Ax, Bx, and Cx in my previous declaration.

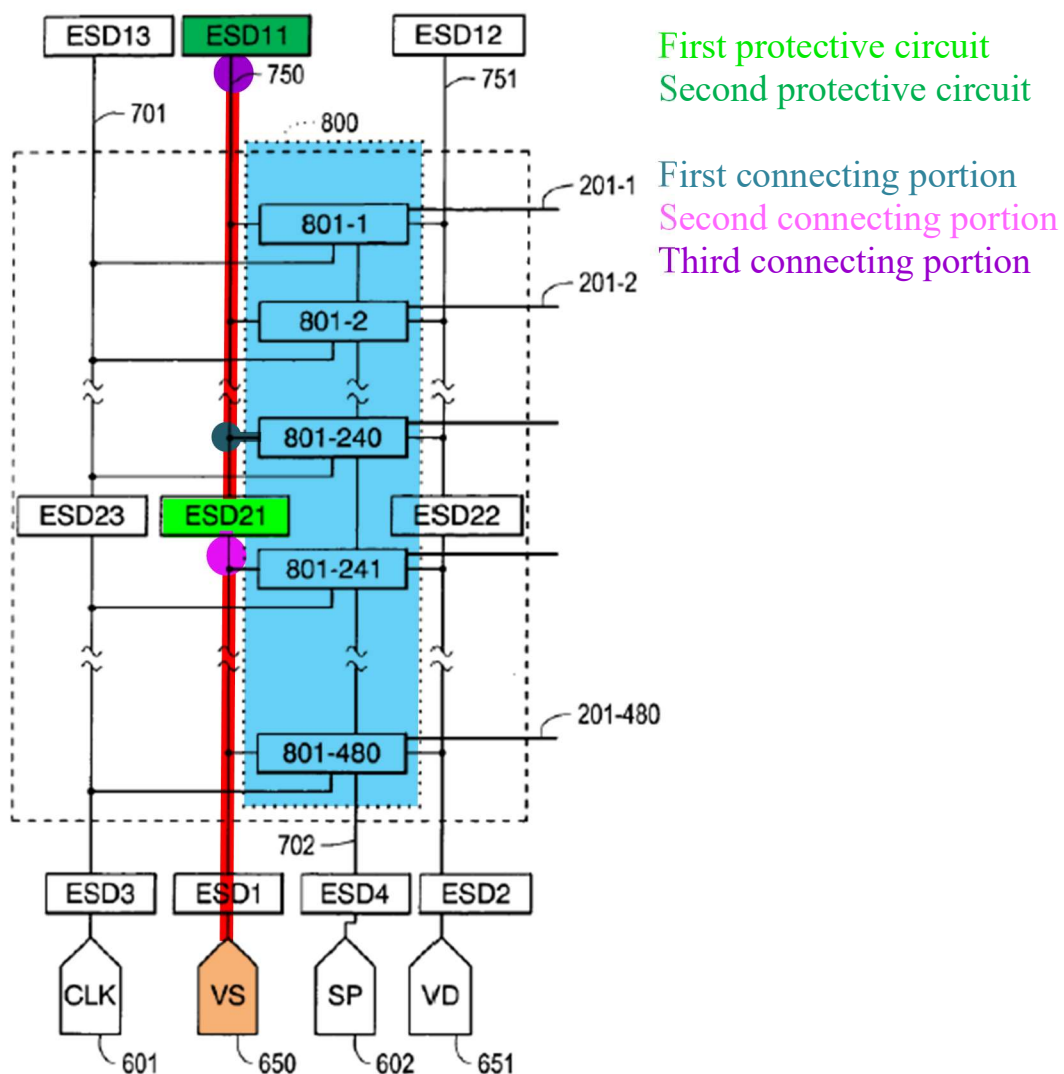
57. A POSITA would have understood that a "first connecting portion" in the '157 patent refers to the connection of an individual scan line driver unit (e.g., only one of the units 801-*n*) to the power supply line, not all of them, because that same term is used in claims 10 and 18, which make this explicit:

Claim 10: "a first connecting portion at which the circuit element and the power supply line are connected." Ex. 1001, 13:19-21.

Claim 18: "a first connecting portion at which the circuit element and the power supply line are connected." Ex. 1001, 14:58-60.

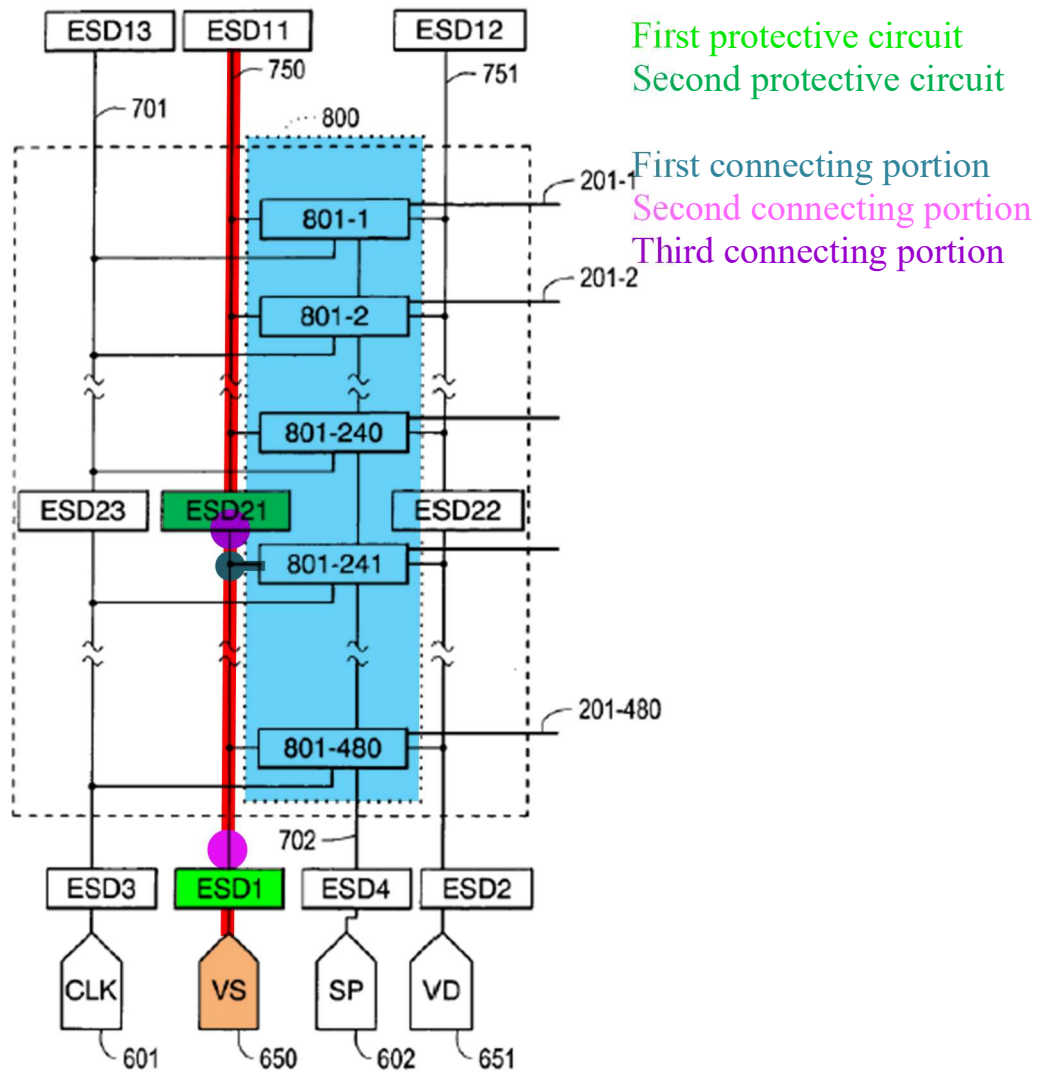
58. I have annotated the '157 patent's FIG. 2 with some examples of how a POSITA would have understood the claim language in view of the specification.

FIG. 2



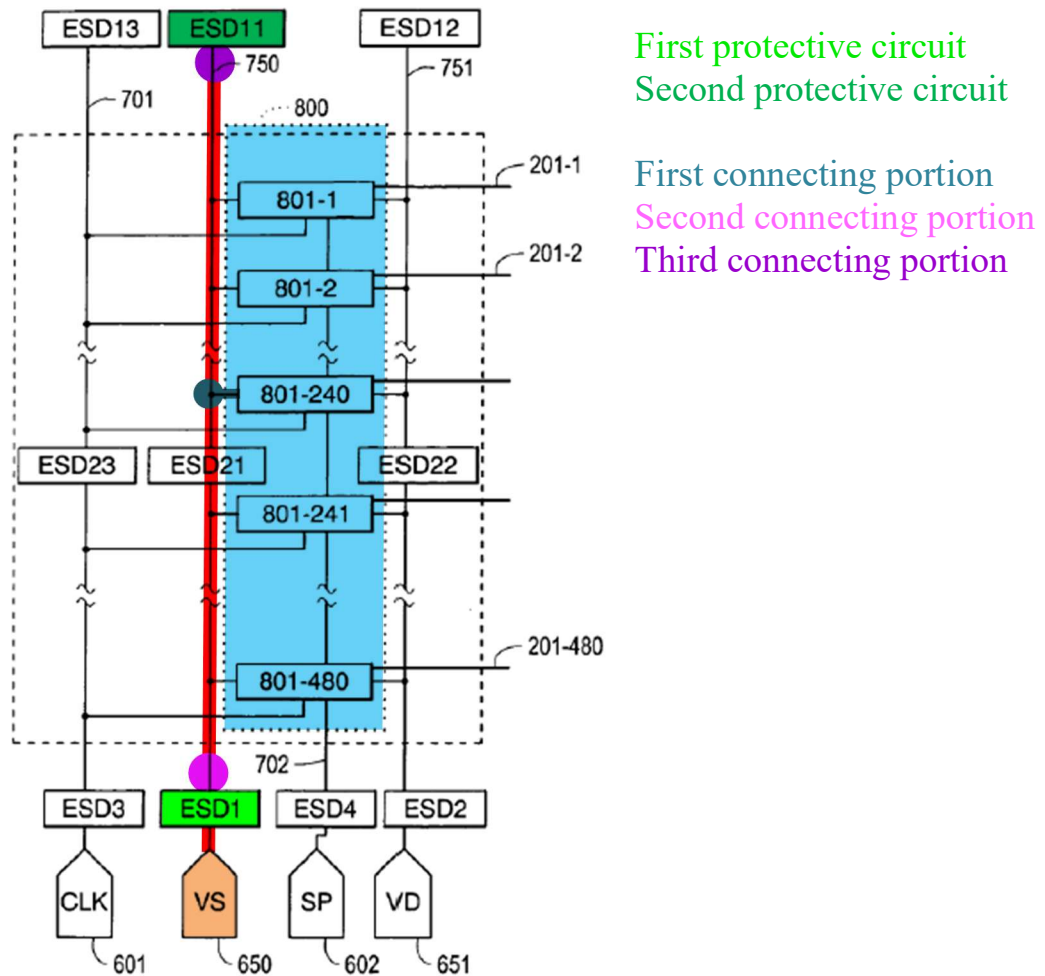
Ex. 1001, FIG. 2 (annotated).

FIG. 2



Ex. 1001, FIG. 2 (annotated).

FIG. 2



Ex. 1001, FIG. 2 (annotated).

59. *Reiner's* protection circuits achieve the same result as claimed in the '157 patent—preventing driver circuit units on individual source or gate lines “from being destroyed” during an ESD “discharge event.” *Reiner*, 2:28-3:1. *Reiner* provides such protection for *every* line driver unit, which is the “[m]ost prefer[red]” configuration of the '157 patent. *Compare Reiner*, 10:10-15, FIG. 5, with Ex. 1001, 7:46-47.

4. *Reiner* Discloses or Renders Obvious the Scanning Line Driving Circuit Being Connected to the Power Supply Line Between a Second Connecting Portion at Which the First Protection Circuit Is Connected to the Power Supply Line and a Third Connecting Portion at Which the Second Protection Circuit Is Connected to the Power Supply Line ([4f])

60. Dr. Schubert argues that

Reiner teaches an integrated circuit on a silicon substrate and including an internal ESD protection network, in particular, ESD devices connected between each input/output[;]

and that

Reiner describes only ESD protection networks *in* an integrated circuit, it does not disclose a scanning line driving circuit connected to a power supply line between first and second protection circuits.”

Schubert Declaration ¶76.

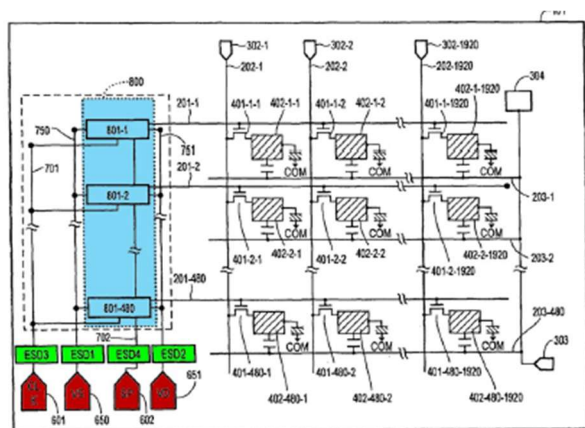
Dr. Schubert concludes that,

[i]n [his] opinion, a POSITA would understand that the plain language of the claim requires that the scanning line driving circuit connect to a power supply line *between* the protection circuit connecting portions. *Reiner*’s ESD protection network is *inside* its purported scanning line driver (source driver 61), to protect individual output devices 70.

Schubert Declaration ¶77. I disagree both with Dr. Schubert’s characterization of *Reiner* and his conclusions.

61. First, *Reiner*'s driver circuits are attached to and arranged on the glass substrate using "flip-chip technology," as I describe elsewhere and in my previous declaration. The '157 patent also supports this, explaining that "instead of a thin film transistor formed on the insulating substrate, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is formed on a crystal silicon wafer." Ex. 1001, 11:29-33. Dr. Schubert's attempt to distinguish between silicon chips mounted on the display substrate using flip-chip technology, as in *Reiner*, appears to ignore this disclosure. A POSITA would have instead understood that *Reiner*'s described technology is in line with the disclosures of the '157 patent, including the example above.

62. Dr. Schubert's assertion that *Reiner* discloses only the "conventional art" in FIG. 11 of the '157 patent (Schubert Declaration ¶¶78-80) appears to ignore that *Reiner* discloses hundreds or thousands of ***additional*** ESD protection circuits far away from the input terminals, as I show in Figures *Ax*, *Bx*, and *Cx* of my previous declaration. Dr. Schubert's own figure confirms this difference, which I reproduce below.



Additional
ESD protection
circuits not
shown in '157
patent, FIG. 11

Schubert Declaration ¶79 (annotating Ex. 1001, FIG. 11).

Schubert Declaration ¶80 (red text and box annotations added, other annotations in original).⁷

⁷ Dr. Schubert's figure has rearranged the locations of ESD1 and ESD2 from what is shown in *Reiner*'s FIG. 5. This rearrangement does not change my opinion that *Reiner* discloses or renders obvious all claims of the '157 patent because the claimed connections remain present in the claimed arrangement and the ESD protection circuits ESD1, ESD2 continue to protect the scanning line driving circuit.

63. As an initial matter, I note that Dr. Schubert's figure (above right) omits all of the intermediary ESD3 protection circuits at each of the driver units 70. This omission shows Dr. Schubert's misunderstanding of *Reiner* and the technology at issue. *Reiner* teaches that "three ESD devices ESD1, ESD2, **and ESD3** are provided **for each output device 70**, in order to protect the circuitry inside the devices 70." *Reiner*, 10:10-12, FIG. 5 (emphases added). The use of "each" would have been understood by a POSITA to mean that every driver unit 70 has (or all driver units 70 have) corresponding ESD1, ESD2, and ESD3 protection circuits. See Ex. 1022, *Random House Webster's Unabridged Dictionary*, 3 (defining "each" as "every one of two or more considered individually or one by one" and "every one individually; each one"); Ex. 1023, *American Heritage Dictionary*, 3 (defining "each" as "every"). A POSITA would have understood this is the same as saying "each of John, Sally, and Susie has a blue hat and a black shirt." That is, John has a blue hat and a black shirt, Sally has a blue hat and a black shirt, and Susie has a blue hat and a black shirt. Here, the first driver unit 70 at the first line has a corresponding ESD1, ESD2, and ESD3 protection circuit; the second driver unit 70 at the second line has a corresponding ESD1, ESD2, and ESD3 protection circuit; and so on for every driver unit 70.

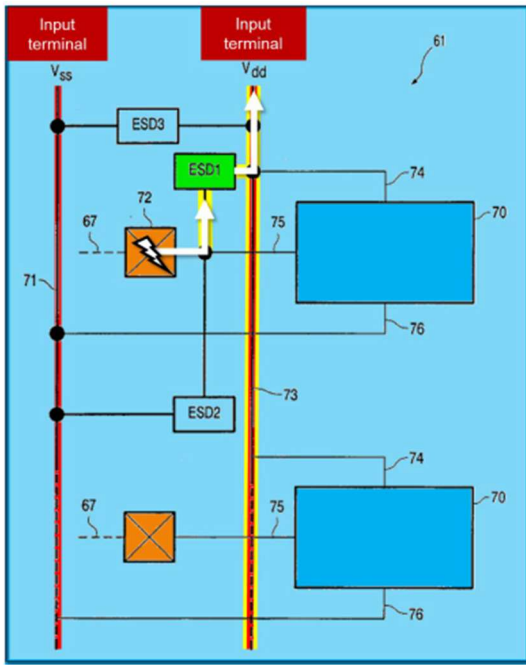
64. Regardless, even considering Dr. Schubert's incorrect configuration showing only one ESD3, all of my Figures Ax, Bx, and Cx in my previous

declaration demonstrate that a POSITA would have understood that *Reiner* discloses or renders obvious all claims of the '157 patent or, alternatively, *Reiner* and *Takahara* render obvious all claims of the '157 patent because I either rely on ESD1 and ESD2 (Figures Ax and Bx) or only the first ESD3, which Dr. Schubert acknowledges (Figures Cx).

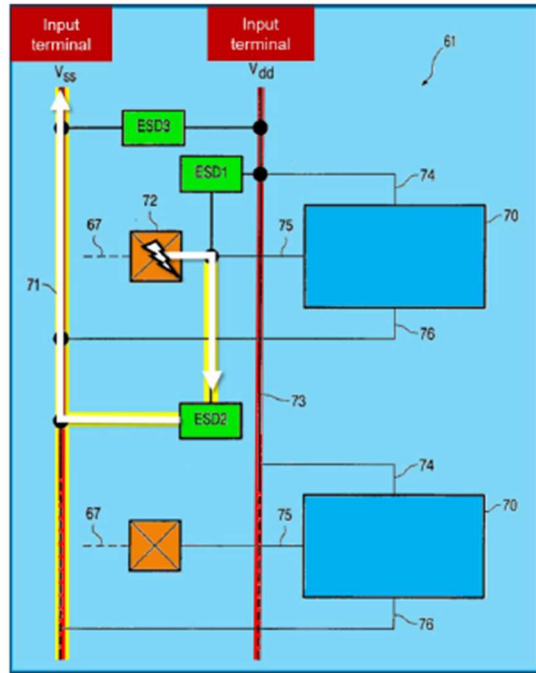
65. Dr. Schubert is incorrect that “Reiner teaches no more than the conventional arrangement, before the '157 patent’s claimed improvements,” because “[i]t teaches ESD protection between input/outputs of the source driver 61 device to protect output devices 70 of source driver 61.” Schubert Declaration ¶80. As Dr. Schubert’s own figure above shows, *Reiner*’s protection circuit network provides for hundreds of additional ESD protection circuits that protect the driver units far away from the input terminals—indeed all the way to the other end of the driver circuit—which is the alleged “improvement[]” of the '157 patent. *See* Ex. 1001, 2:51-57, 3:6-17, 7:20-59, FIGS. 1, 2; *see also* Ex. 1002, 375 (“[T]he addition of the second protection circuit is not just a mere duplication of parts Instead, the second protection circuit, as disclosed in the specification, provides additional ESD protection not provided by just the first protection circuit.”). The “conventional art” of FIG. 11 of the '157 patent has only the one protection circuit on the power line, markedly different from *Reiner*’s teachings.

66. Contrary to his own assertions, Dr. Schubert appears to *agree* that *Reiner*'s ESD1, ESD2, and ESD3 protection circuits protect the driver circuits 70 from static electricity and ESD damage entering through the signal lines and power lines, as shown in Dr. Schubert's own created figures, reproduced below.⁸

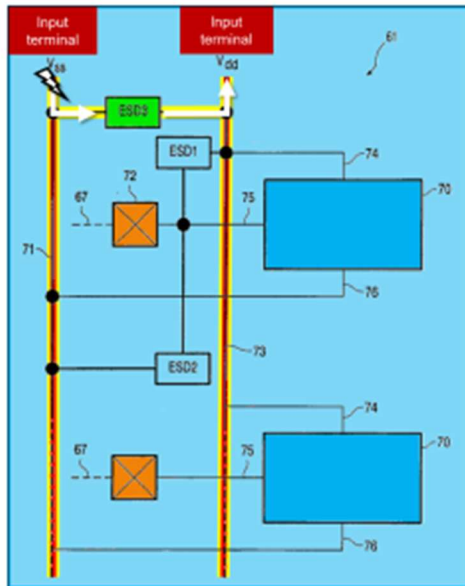
⁸ Dr. Schubert's acknowledgement that ESD1, ESD2, and ESD3 protect the driver units on each line of the display from ESD damage, which is the same as the "[m]ost prefer[red]" embodiment of the '157 patent (having "protective circuits [that] are interposed between all stages" of the driver unit), confirms that it provides the additional claimed protection that is not part of the "conventional art" of FIG. 11 of the '157 patent. Ex. 1001, 7:46-47, FIG. 11.



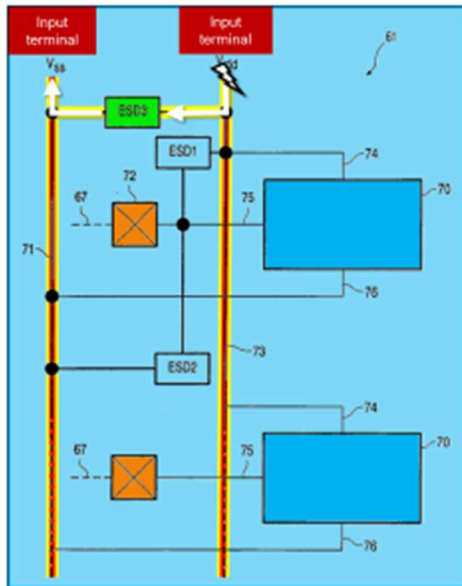
Schubert Declaration ¶80 (annotating
Reiner, FIG. 5).



Schubert Declaration ¶81 (annotating
Reiner, FIG. 5).



Schubert Declaration ¶82 (annotating *Reiner*, FIG. 5).



67. Dr. Schubert's acknowledgement that *Reiner*'s ESD protection circuits protect both the "input[s]/outputs" and all along the power lines, rather than just before the first driver circuit unit at the input terminal (Schubert Declaration ¶78), only highlights *Reiner*'s teachings of the claims, rather than distinguishing *Reiner*.

68. Dr. Schubert also asserts that *Reiner*'s ESD protection circuits are "inside" the scanning line driving circuit and, therefore, not "connected to the scanning line driving circuit." Schubert Declaration ¶¶77, 78. They are not "inside." But even if they were considered "inside," a POSITA would have recognized that the ESD protection circuits are still connected to the scanning line driving circuit (e.g., the driver units 70) through the wiring connections. This is similar to the way screws holding together two pieces of wood are both connected to the pieces of wood and inside the pieces of wood.

69. A POSITA would have understood, as I show in Figures Ax, Bx, and Cx in my previous declaration, that the claimed "scanning line driving circuit" is composed of the individual driver units 70 in *Reiner*'s FIG. 5. Each of *Reiner*'s ESD1 and ESD2 is connected to the respective driver units 70, as shown in Figures Ax and Bx. Dr. Schubert also states that ESD3 is connected to the respective driver

units under Patent Owner's construction, as shown in my Figures Cx. Schubert Declaration ¶70.⁹

70. I recognize that, during my deposition (Ex. 2008), Patent Owner drew an arbitrary line around the scanning line driver units (group of units 70) that also includes the ESD circuits ESD1-ESD3. Patent Owner appears to take my statements out of context. In my deposition, I was asked about a “source driver *module*,” which a POSITA would have understood is more than just the scanning line driver *circuit* itself. *See, e.g.*, Ex. 2008, Murphy Tr., 94:22-103:16, 137:22-139:16 (emphasis added). A POSITA would have recognized that a “module” may often include more than the circuitry itself, for example, would also include the power supply lines and ESD protection circuits of *Reiner*. But the driver *circuit*, recited in the claims, is the group of circuitry in driver units 70, as I annotated in Figures Ax, Bx, and Cx of my previous declaration.

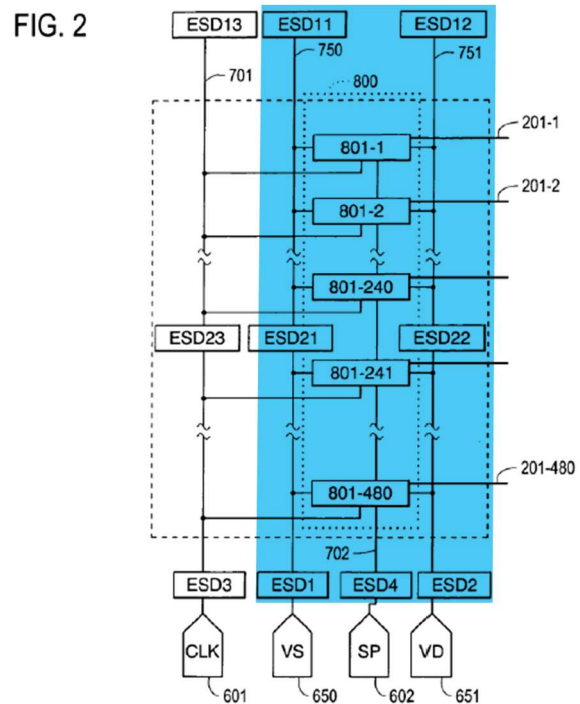
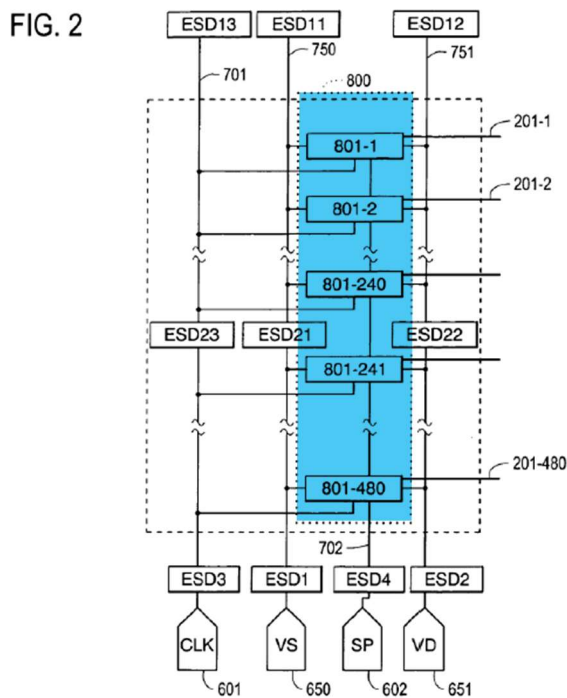
71. Regardless, even if I consider Patent Owner's argument at face value, that does not change my opinion. As I also stated in my deposition, there is no difference in structure or function. Ex. 2008, Murphy Tr., 178:11-180:17,

⁹ As I state in my previous declaration, if that construction is adopted by the Board, my Figures Cx meet these limitations, but I have no opinion on the correctness of the construction itself.

182:15-22. No matter how the line is drawn, *Reiner*'s ESD protection circuits connect to the power line(s) that provide power to the scanning line driving circuit in the configuration claimed in the claims of the '157 patent, as shown in my previous declaration.

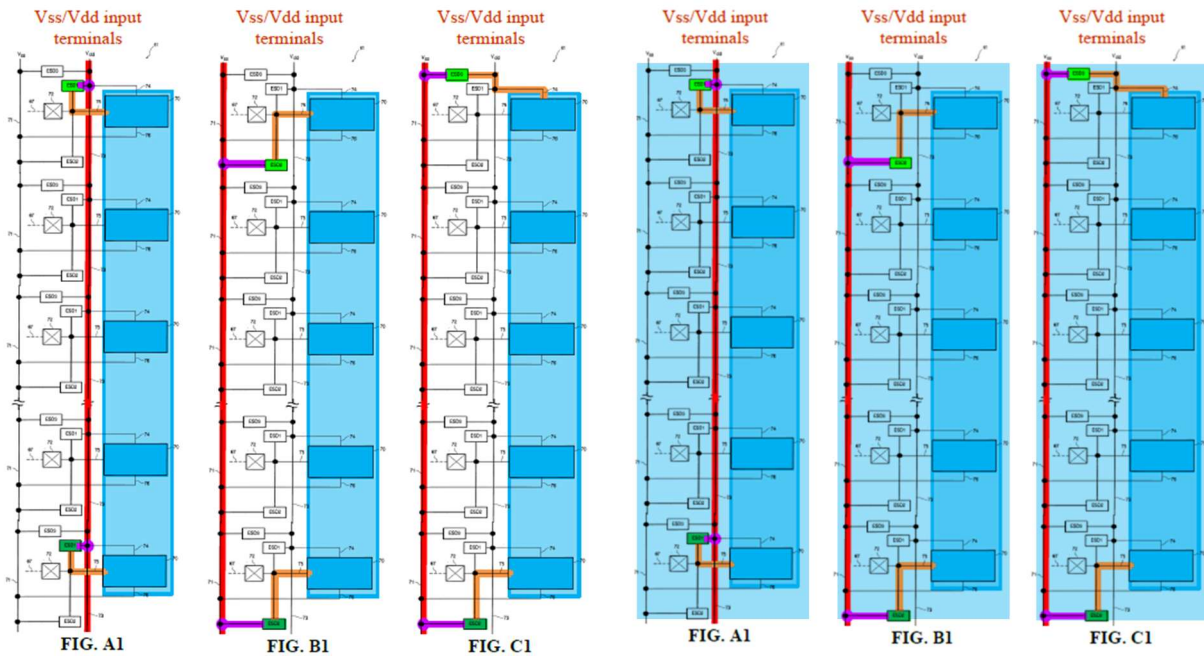
72. Indeed, a POSITA would have recognized that *Reiner*'s ESD1, ESD2, and ESD3 are formed on the same substrate as the individual driver units 70 and are connected.

73. I illustrate that Patent Owner's attempted characterization is arbitrary and not meaningful to either the claims or operation of *Reiner* or the '157 patent. Indeed, nothing changes in either structure or function.



Ex. 1001, FIG. 2 (annotated).

Ex. 1001, FIG. 2 (annotating Patent
Owner's arbitrary line drawing from my
deposition).



Figures Ax-Cx (annotations original).

Figures Ax-Cx (additional annotations
showing Patent Owner's arbitrary line
drawing from my deposition).

74. *Reiner* teaches protecting the “very sensitive” driver circuits of a driver unit from ESD that may enter through any of the contact pads—such as those at the opposite end of the circuit from the power terminals; *see* my Figures Ax, Bx, Cx—which is precisely the type of “protection against the static electricity

... in a place far from the terminal, by providing internal protective circuits in an area which is not connected to the input terminals of the wiring lines,” that the ’157 patent alleges is its invention. *See Reiner*, 2:28-3:1; Ex. 1001, 3:6-11; *see also* Ex. 1001, 2:38-42, 2:55-57, 3:15-17, 5:55-6:2, 7:25-51 (describing the quarter and half-way points as “far from” the input terminals), FIGS. 1-2.

B. *Reiner* Discloses or Renders Obvious the Scanning Line Driving Circuit Being Arranged on the Substrate in Claim 8

75. I disagree with Dr. Schubert that “Reiner does not disclose a display device comprising ‘a substrate’ and ‘the scanning line driving circuit being arranged on the substrate.’” Schubert Declaration ¶¶88-100. Dr. Schubert contends that I “do[] not identify a *display device* substrate and a scanning line driving circuit arranged on that substrate,” and that “Reiner discloses integrated circuits having their own substrates and, separately, a display to which the integrated circuits may connect (for example, via contact pads).” Schubert Declaration ¶89. Dr. Schubert misunderstands *Reiner*. In fact, *Reiner*’s “flip-chip technology” (also called FCOG or COG) is exactly arranging the gate and source drivers onto the pixel substrates at contact pads, like those disclosed in *Reiner*. This technology dates back to the 1980s and was common in LCD displays in the late 1990s and early 2000s. *See, e.g.*, Ex. 1019, *Kang*, 1 (“[T]he use of chip on glass (COG) technique is proposed for a number of products such as high pixel density and

small area LCDs. In this technique, *the driver IC is directly mounted on LCD panels by flip chip.*” (emphasis added)); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to *mount the driver IC directly on to the glass LCD.* FCOG and COG offer the highest density possible in packaging,” and “[i]n COG, the bare (unpackaged) *driver ICs are mounted directly on the glass panel.* Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.” (emphases added)); Ex. 1021, *Wu*, 20 (“With increasing needs for higher resolution displays, higher density interconnect technology becomes inevitable. *Direct mounting of flip chip onto glass* using ACA’s (see Figure 1) became the topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.” (emphasis added)).

76. Dr. Schubert acknowledges that “Reiner explains [that] the integrated circuit device 20 may be ‘flipped onto the substrate 16’ so that the ‘substrate 16 with its interconnections may rest on’ the bump bridges of integrated circuit device 20.” Schubert Declaration ¶90 (coloration omitted) (quoting *Reiner*, 7:22-26). But Dr. Schubert then asserts that “Reiner’s substrate 16 does not disclose a display device ‘substrate’ or a ‘substrate’ on which the integrated device 20, let alone gate drivers 63, is ‘arranged.’” Schubert Declaration ¶91. Reiner expressly states, and a

POSITA would have understood, that a “typical example” of an “integrated circuit” is “display driver 61 *or* 63.” *Reiner*, 9:11-15 (emphasis added).

77. The crux of Dr. Schubert’s positions related to claim 8 appears to be that *Reiner*’s scanning line driving circuit 63 is not “**formed on**” (1) the substrate having the display matrix pixels or (2) the substrate 16 that includes the display matrix pixels in *Reiner*. See Schubert Declaration ¶¶88-100 (emphasis added). I disagree with Dr. Schubert on each point.

78. The claims do not require any particular type of substrate and do not recite the “pixel” substrate specifically. Regardless, *Reiner* teaches using “flip-chip technology” to arrange the driver units onto the substrate having the gate lines and source lines (i.e., the substrate for the pixels).

79. As explained in *Reiner*:

Each output device 70 of a source driver module 61, for example, may comprise a digital-to-analog (D/A) converter, a buffer as well as other devices. The buffers drive the source lines 67 with the voltages needed by each pixel of the LCD screen 60. ***The source lines 67 are connected (e.g. by means of bonding) to contact pads 72, as illustrated in Fig. 5. There is an array of several parallel output devices 70 (two such output devices are shown in Fig. 5). The output 75 of each output device 70 is connected to a contact pad 72.***

Reiner, 10:1-6 (emphases added). This teaching, in conjunction with FIGS. 4-5, makes clear that the drivers are bonded directly to the gate/source lines at the contact pads. That is consistent with *Reiner*'s FIG. 2, which shows the drivers bonded directly to the substrate. *See* Ex. 1003, ¶¶145-146.

80. Dr. Schubert's supposition that the drivers must be "formed on" the pixel substrate appears to ignore the '157 patent's teaching that "***instead of a thin film transistor formed on the insulating substrate***, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is formed on a crystal silicon wafer." Ex. 1001, 11:29-33 (emphasis added). Indeed, Dr. Schubert's description of *Reiner* throughout the Schubert Declaration similarly describes this embodiment of the '157 patent.

81. Moreover, a POSITA would not understand "arranged on" to require being "formed on," as Dr. Schubert appears to apply "formed on" (to mean a thin film transistor (TFT) grown on the pixel substrate itself). Rather, a POSITA would have recognized that "arranged on" also includes other configurations, such as flip-chip bonding to the substrate. Dr. Schubert's argument is akin to saying that children's letter magnets cannot be "arranged on" a refrigerator to form words because they are not "formed on" or "grown on" the refrigerator itself. Similarly, Dr. Schubert's interpretation is akin to saying that someone cannot arrange pens on a desk or table because they are not "formed on" the desk or table. Dr. Schubert's

overly narrow interpretation of “arranged on” to require being “formed on” does not reflect how a POSITA would have understood “arranged on,” which describes positioning on the substrate, not the method of placement.

82. I also note that the Patent Owner’s responses assert that the Petition, relying on my prior testimony, “simply invents a ‘substrate.’” Patent Owner’s Response at 45-46 (quoting Pet. 45-46). This is incorrect. As I explained in my previous declaration, the substrate 16 onto which the drivers are flipped is the pixel substrate at the contact pad for the source/gate lines. Ex. 1003, ¶146. Moreover, as I explained in my deposition, once the driver is flipped onto the glass substrate, it is subject to the same vulnerabilities as drivers formed directly on the glass substrate. *See* Ex. 2008, Murphy Tr., 69:2-77:4, 93:9-94:1.

83. Dr. Schubert’s “disagree[ment]” that a POSITA would have “mount[ed] Reiner’s silicon integrated circuit drivers on an LCD display substrate” (e.g., substrate 16 in *Reiner*) (Schubert Declaration ¶93) is misplaced. As I explain above, this is what “flip-chip technology” *is*, in particular COG and FCOG.

84. Dr. Schubert’s suggestion that “Reiner’s Si IC data line driver circuit *is located off of the LCD glass panel* and connected to the LCD panel’s data lines by means of electrical connectors and metallization lines” (Schubert Declaration ¶93 (emphasis added)) is misplaced. *Reiner*’s FIGS. 3, 4, and 5, and the disclosure

of “flip-chip technology,” in fact describe this because the driver circuits are connected directly to the gate/source lines on the pixel substrate 16.

85. Dr. Schubert also makes reference to “Full HD display” in paragraphs 93-96 of the Schubert Declaration, but this does not change the outcome in my opinion. A POSITA would not have understood the ’157 patent to require full HD, not the least because the only disclosure of size in the ’157 patent is a screen with 480 scan lines (less than half what is in full HD) and also because the ’157 patent never refers to “Full HD.” To the contrary, full HD would make *Reiner*’s teachings rendering the claims ***more obvious*** because *Reiner* and flip chip (e.g., FCOG) technology are better for smaller pixel pitches and higher densities, contrary to the tape connections that Dr. Schubert describes in the Schubert Declaration. *See, e.g.*, Schubert Declaration ¶¶97-100.

86. Indeed, ***flip chip*** technology was known to be advantageous for smaller pixel pitch sizes to create higher resolution displays, which *Reiner* itself notes and provides ESD protection for. *Reiner*, 2:7-9, 4:15-16, 12:16-18, FIG. 5; Ex. 1019, *Kang*, 1 (“[T]he use of chip on glass (COG) technique is proposed for a number of products ***such as high pixel density and small area LCDs***. In this technique, the driver IC is directly mounted on LCD panels by flip chip.” (emphasis added)); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD. ***FCOG***

and COG offer the highest density possible in packaging,” and “[i]n COG, the bare (unpackaged) driver ICs are mounted directly on the glass panel. Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.” (emphasis added)); Ex. 1021, *Wu*, 20 (“***With increasing needs for higher resolution displays, higher density interconnect technology becomes inevitable.*** Direct mounting of flip chip onto glass using ACA’s (see Figure 1) became the topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.” (emphasis added)).

87. Nothing in *Reiner* suggests the use of COF, TCP, or TAB, as Dr. Schubert alleges. Even though these were alternative technologies, *Reiner* expressly discloses “flip-chip technology” for mounting to the pixel substrate, and a POSITA would have found it obvious to do so. *Reiner*, 7:23-25; Ex. 1003, ¶¶101, 120, 145, 231, 233, 251 (citing *Reiner*’s discussion of “flip-chip technology” at 7:23-25). In fact, the very purpose of flip-chip technology is to allow mounting the source/data and gate/scan line drivers directly on the LCD display substrate to

realize higher-density integrated circuits.¹⁰ Ex. 1019, *Kang*, 1 (“[T]he use of chip on glass (COG) technique is proposed for a number of products such as high pixel density and small area LCDs. In this technique, ***the driver IC is directly mounted on LCD panels by flip chip.***” (emphasis added)); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to ***mount the driver IC directly on to the glass LCD.*** FCOG and COG offer the highest density possible in packaging,” and “[i]n COG, the bare (unpackaged) ***driver ICs are mounted directly on the glass panel.*** Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.” (emphases added)); Ex. 1021, *Wu*, 20 (“With increasing needs for higher resolution displays, higher density interconnect technology becomes inevitable. ***Direct mounting of flip chip onto glass*** using ACA’s (see Figure 1) became the topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.” (emphasis added)); *see also Reiner*, 12:15-18.

¹⁰ I previously identified this as a motivation to mount the drivers on the pixel substrate using flip-chip technology ***and*** that *Reiner*’s described ESD network further protects such densely packed circuits. *See* Ex. 1003, ¶¶112, 113, 116, 118, 119; *see also* Ex. 1003, ¶¶157, 181, 231, 238, 239. This remains true.

88. Dr. Schubert's reference to a "4-5 micron vertical gap between the display substrate and the counter substrate" (Schubert Declaration ¶99) is also misplaced. The gap he describes is between the display *pixels* and the display glass covering the pixels; it does not apply to the bezel region where the drivers and other control circuitry is found in LCD displays. Regardless, the '157 patent expressly contemplates the use of IC chips mounted to the substrate, like in *Reiner*, making Dr. Schubert's (incorrect) opinion not material or relevant to whether a POSITA would have found the claims obvious.

89. Finally, Dr. Schubert's conclusion that "a POSITA would not employ a Si IC chip, as disclosed by Reiner, for a scanning line driving circuit" (Schubert Declaration ¶100) is again contradicted by the fact that the '157 patent expressly contemplates silicon chips: "*instead of a thin film transistor formed on the insulating substrate*, an active matrix substrate may be used, in which ... *a driving circuit is formed on a crystal silicon wafer.*" Ex. 1001, 11:29-33 (emphases added). A POSITA reading the '157 patent's disclosure would have understood this alternative and would not have held the opinion that Dr. Schubert ascribes to them. Indeed, they would have understood that the example describes the "Si IC chip" that Dr. Schubert refers to.

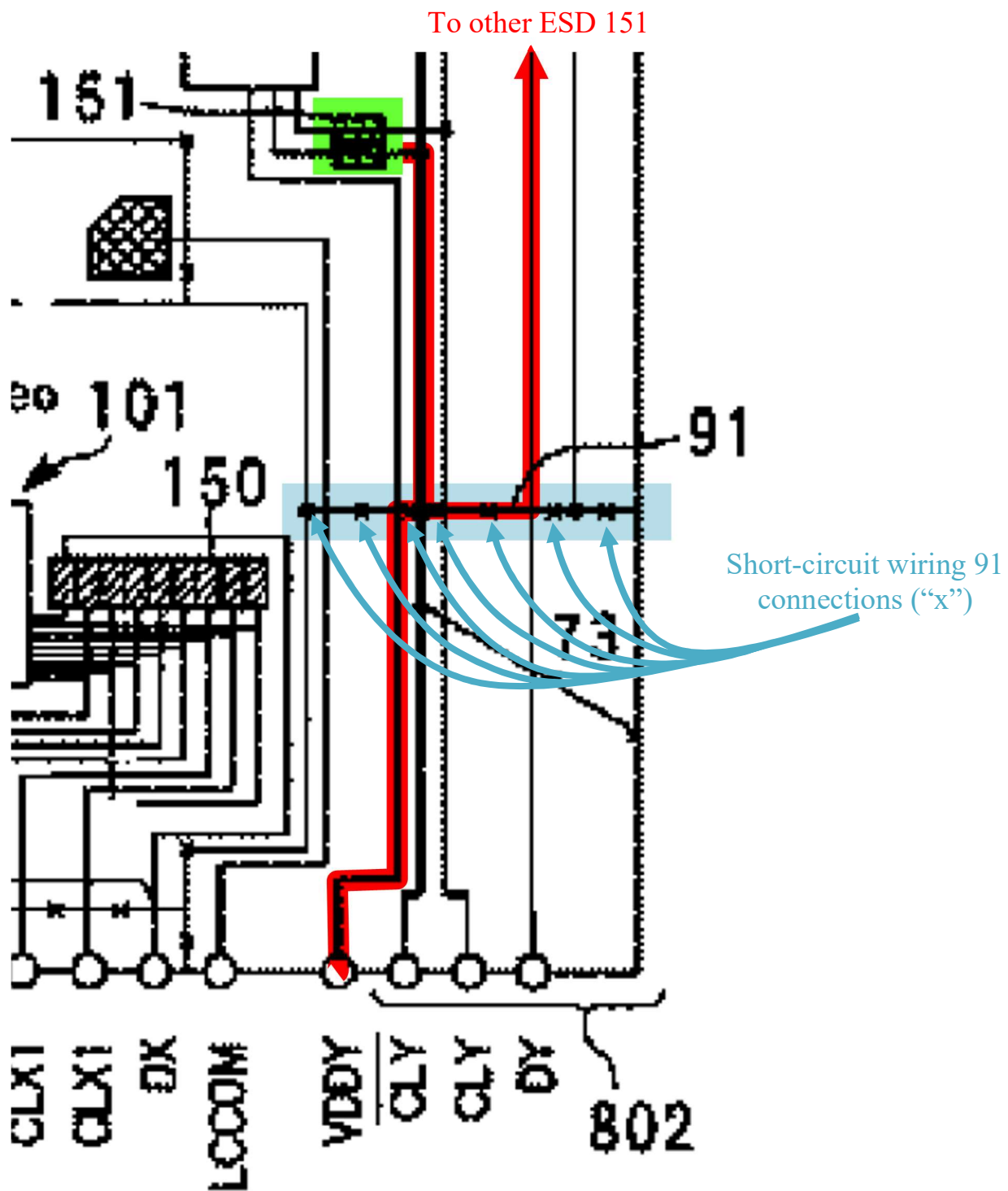
C. Claims 1-3, 5-7, and 9-18 Would Also Have Been Obvious

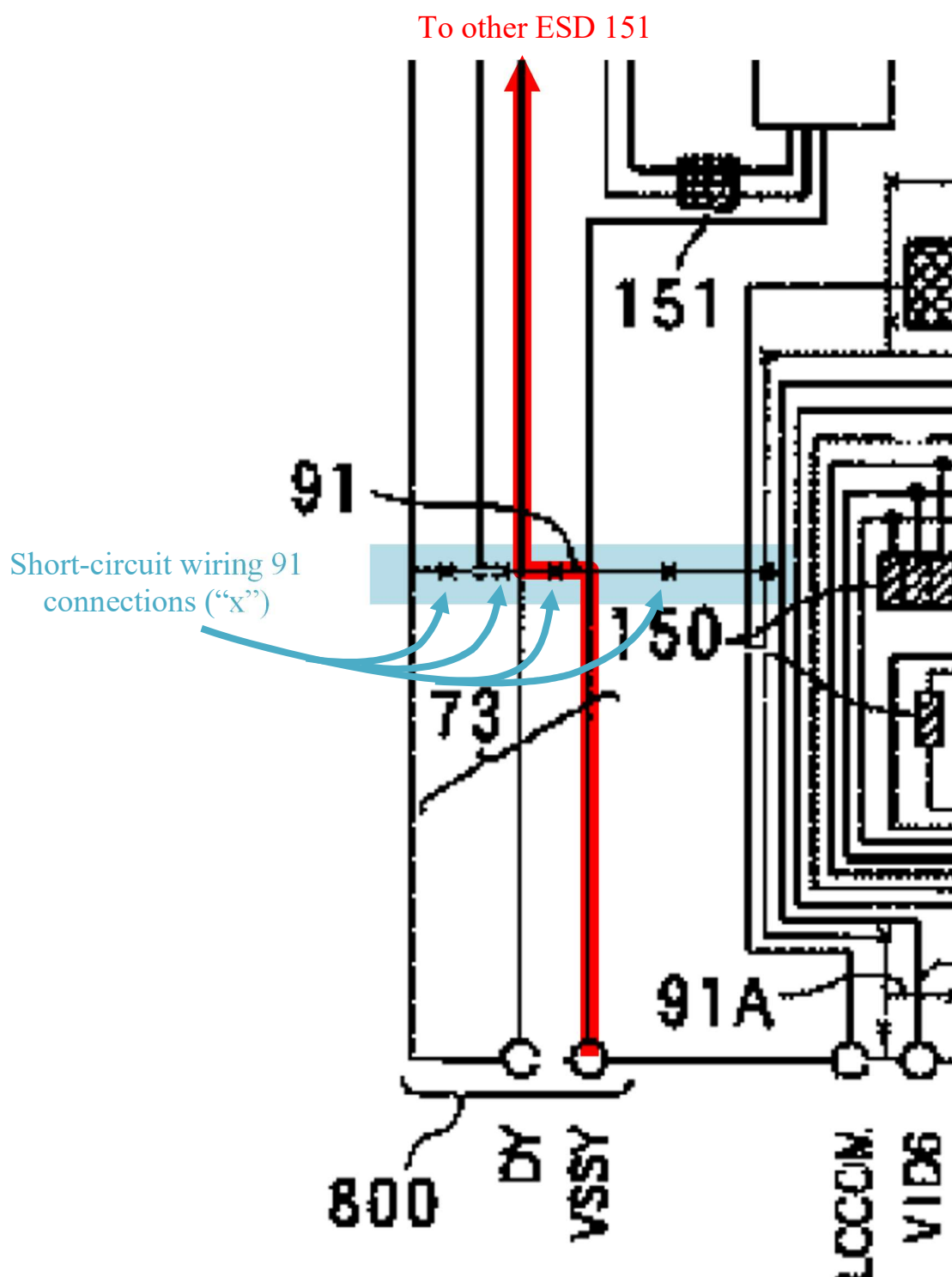
90. Dr. Schubert appears not to dispute my prior opinion for any other claims or claim elements, except on the bases above. Therefore, I do not further address claims 1-3, 5-7, and 9-18, but instead refer back to the reasoning above.

VII. The Combination of *Reiner* and *Takahara* Would Have Rendered All Claims Obvious

91. After having reviewed Dr. Schubert's Declaration, it is still my opinion that a POSITA would have found claims 1-18 obvious based on the combination of *Reiner* and *Takahara*. This remains my opinion both under my definition of a POSITA and under Dr. Schubert's definition of a POSITA.

92. Dr. Schubert's opinions related to the combination of *Reiner* and *Takahara* appear to be based on the faulty premise that *Takahara*'s short-circuit connections 91 do not connect the power lines to the ESD protection circuits. See Schubert Declaration ¶¶123-140. Dr. Schubert is incorrect. *Takahara* marks the short wirings with an "x" and clearly shows connections between the signal and power lines as shown in both FIGS. 1 and 3. I have annotated these below, where the "x" for the short-circuit wiring 91 can clearly be seen such that the power lines VDDY and VSSY are then connected to the ESD protection circuits 151.





Takahara, FIG. 1 (excerpted, annotated); *see also* *Takahara*, FIG. 3 (showing short-circuit wiring 91 between two ESD-protected lines).

93. *Takahara*'s description confirms this because it states that "static electricity entering from ... ***the first short-circuit wiring 91*** does not reach ... the scan-line drive circuit 104 unless it passes through the protection resistor 66 and the electrostatic-protection circuit 150 (or 151). With this kind of configuration, static electricity is reliably absorbed by the electrostatic-protection circuit 150 (or 151), and ... the scan-line drive circuit 104 can be reliably protected." *Takahara*, [0066] (emphasis added), FIG. 1.

94. Thus, the premise of each of Dr. Schubert's arguments is incorrect.

A. The Combination of *Reiner* and *Takahara* Renders Obvious the Claimed Input Terminals Connected to the Power Supply Lines ([4c])

95. It appears that Dr. Schubert's arguments related to the combination of *Reiner* and *Takahara* related to element [4c] rely on *Reiner*'s disclosure, not *Takahara*'s. See Schubert Declaration ¶123. Dr. Schubert, however, does not appear to dispute that *Takahara* discloses input terminals (800, 802) for power lines VDDY/VSSY that supply power to the scan-line drive circuits 104. See Schubert Declaration ¶123; *Takahara*, [0066], FIG. 1. Nor does he appear to dispute my opinion that a POSITA would have found it obvious to include such

terminals in *Reiner*'s display device based on the combination of *Reiner* and *Takahara*. See Schubert Declaration ¶123; see Ex. 1003, ¶¶229-233.¹¹

B. The Combination of *Reiner* and *Takahara* Renders Obvious [4f] as Claimed

96. The bulk of Dr. Schubert's positions related to the combination of *Reiner* and *Takahara*, despite their length, center around three arguments: (1) that VDDY and VSSY are not "signal wirings 73"; (2) that *Takahara* does not disclose VDDY and VSSY are connected to the ESD protection circuits 151 through short-circuit wirings 91; and (3) that *Takahara* must provide additional teachings other than protecting scan line driver circuits from ESD protection (what I rely on it for in my prior declaration). See Schubert Declaration ¶¶124-137.

97. I disagree with Dr. Schubert on all three accounts. But, regardless of Dr. Schubert's opinions, my prior opinion shows that a POSITA would have found it obvious to use *Takahara*'s teaching of protecting the scanning line driver circuit

¹¹ I note Dr. Schubert's statement that "the Petition's suggestion that *Takahara* would render obvious adding input terminals to *Reiner*'s driver 61 would not render obvious input terminals *of the display device*." Schubert Declaration ¶123. Although this argument lacks substance, *Reiner* teaches a display device having drivers, as I explain above.

from ESD to avoid damage to the scanning line driver circuit. That particular teaching, and my conclusion based on it in my prior declaration, does not appear to be disputed by Dr. Schubert. Instead, he appears to challenge other disclosures of *Takahara*. I disagree with his opinions, but even if he were correct (which he is not, as I explain below), none would alter my conclusion.

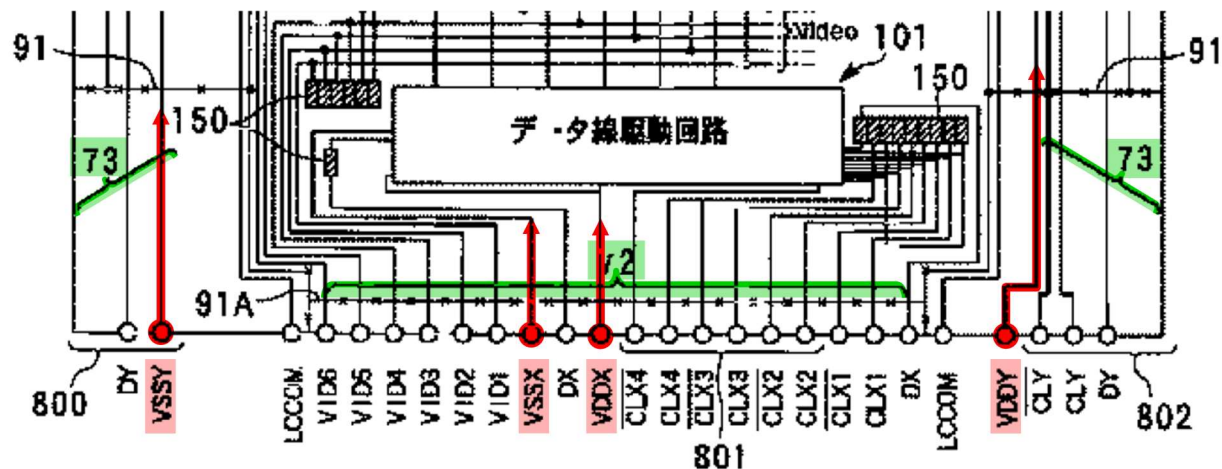
98. Dr. Schubert, relying on *Takahara*'s paragraphs [0024], [0025], [0060], [0061], [0065], and FIG. 1, appears to allege that none of the signal wirings 72, 73 include power lines. Schubert Declaration ¶¶125-127. That is incorrect.

99. As an initial matter, Dr. Schubert confuses the *wirings* with the signals transmitted on the wirings, and it is clear that *Takahara*'s use of the term "signal wirings" includes transmission of power on VDDY and VSSY in order to power the various circuits of the display, including the driver circuits.

100. A POSITA would not have understood any of the paragraphs cited by Dr. Schubert to exclude the power lines for VDDY and VSSY from signal wirings 72, 73. *Takahara* paragraphs [0024] and [0025] describe connecting "wirings" that "include" data and scan lines. *Takahara* paragraph [0060] describes parts of the "data-line drive circuit 101," but does not mention wirings at all, let alone limit them, as Dr. Schubert asserts. *Takahara* paragraph [0061] describes certain signals "supplied to the scan-line drive circuits 104," but nothing *limits* the meaning of wirings 72, 73 to *only* these signals. *Takahara* paragraph [0065] describes signal

wirings 72, 73 by their structure, stating: “the plurality of signal wirings 72 and 73, which are composed of a low-resistance metal film such as aluminum film, or a metal-silicide film, for driving the scan-line drive circuits 104” A POSITA would have understood here that “driving” the circuit also includes powering the circuit or the circuit would not function.

101. Quite the contrary to Dr. Schubert’s opinions, *Takahara*’s FIG. 1 shows that signal wirings VDDY, VSSY, VDDX, and VSSX (annotated red below) are encompassed by signal wirings 72, 73, shown by the brackets (green).



Takahara, FIG. 1 (excerpted, annotated).

102. As shown above, *Takahara*’s brackets identifying signal wirings 72, 73 (green) clearly encompass power lines VSSY, VSSX, and VDDX (red). A POSITA would have recognized that they also encompass VDDY based on the brackets’ positions and directions, either overlapping or facing VDDY, VSSY, VDDX, and VSSX for consistency.

103. Dr. Schubert argues that *Takahara*'s "Figure 1 shows that electrostatic-protection circuits 151 are formed only at intermediate locations of the clock signal lines and start signal lines (DY, CLY, CLY bar) that drive the scan-line driving circuit 104; they are not formed at intermediate locations of the power supply lines VSSY and VDDY." Schubert Declaration ¶127 (coloration omitted). Dr. Schubert's position ignores both the teachings of Figure 1 and *Takahara*'s paragraph [0066], which explains that

static electricity entering from ... the first short-circuit wiring 91 does not reach ... the scan-line drive circuit 104 unless it passes through the protection resistor 66 and the electrostatic-protection circuit 150 (or 151). With this kind of configuration, static electricity is reliably absorbed by the electrostatic-protection circuit 150 (or 151), and ... the scan-line drive circuit 104 can be reliably protected.

Takahara, [0066] (emphases added).¹² In other words, *Takahara* teaches that ESD 151 protects the scanning line driver circuit from static electricity such as that

¹² Dr. Schubert does not discuss *Takahara*'s paragraph [0066] when discussing FIG. 1. As such, he misses important disclosures of *Takahara* that explain FIG. 1 and are contrary to his positions.

passing from power lines VSSY and VDDY through short-circuit wiring 91, exactly as shown in my previous declaration. *Takahara*, [0066], FIG. 1.

104. Dr. Schubert's position that the scan line driver is "'driven in accordance with' start, clock, and image signals, not power lines" (Schubert Declaration ¶128 (quoting *Takahara*, [0060])), misunderstands *Takahara* and the technology because *Takahara* does not exclude the power lines that are bracketed in *Takahara*'s disclosures above.

105. Nor does Dr. Schubert's assertion that "[t]he annotations identifying signal lines 73 and terminals 802 on the right side of Figure 1 include only CLY bar, CLY, and DY signal wirings and terminals, which confirms that the annotations identifying signal lines 73 and terminal 800 on the left side of Figure 1 apply only to the DY signal wiring." Schubert Declaration ¶128. A POSITA would not understand *Takahara* this way because it is contradicted by *Takahara*'s disclosures. Indeed, ***including*** VDDY in signal wirings 73 on the right side is more consistent with *Takahara*.

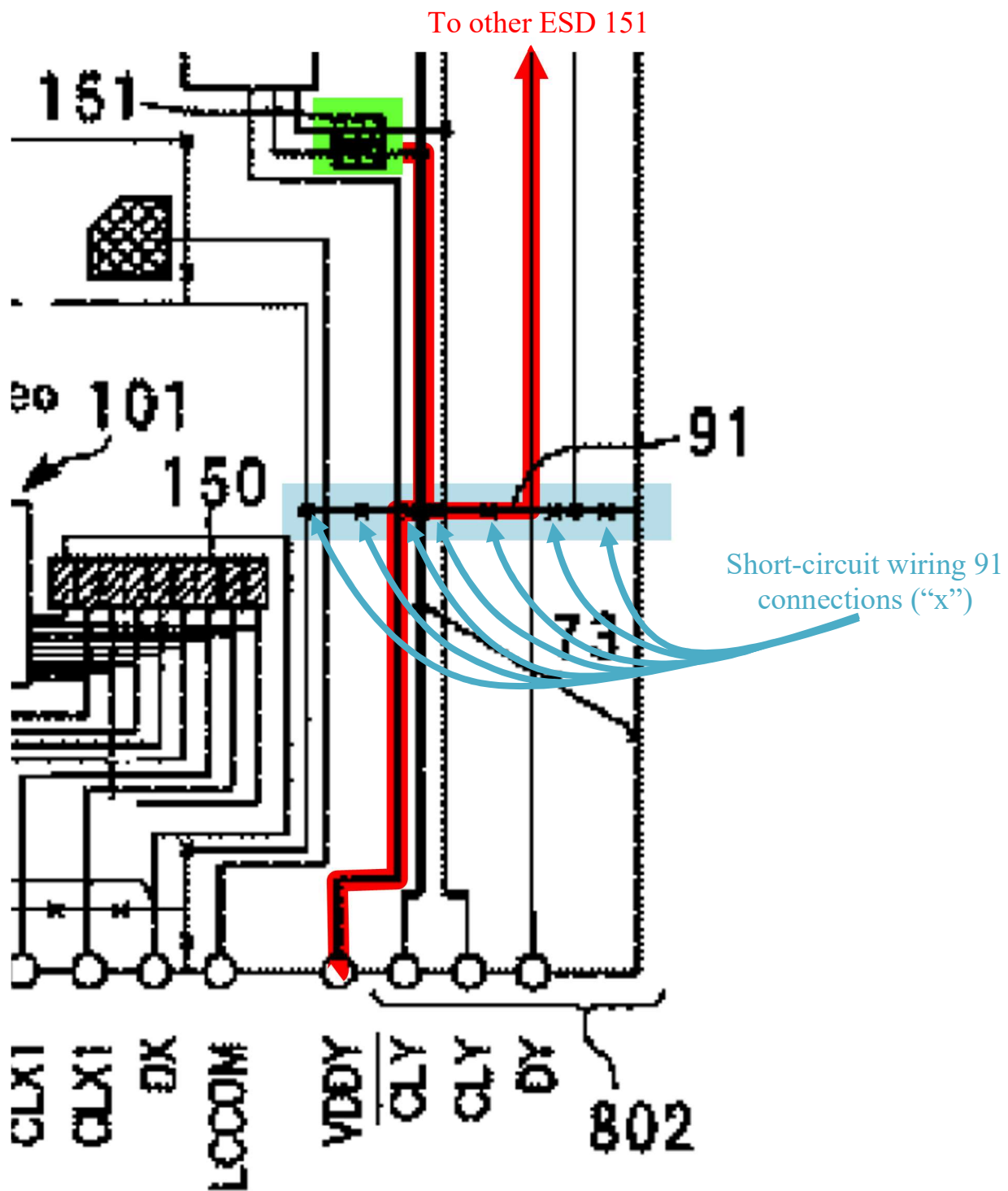
106. To accept Dr. Schubert's argument, a POSITA would have to ***reject three teachings*** shown in (1) the brackets expressly including the power lines VSSY, VSSX, and VDDX; (2) the bracket that is pointed towards VDDY; ***and*** (3) *Takahara*'s disclosure that the "signal wirings" are merely metal films (*see Takahara*, [0065]). Against these multiple express teachings including the power

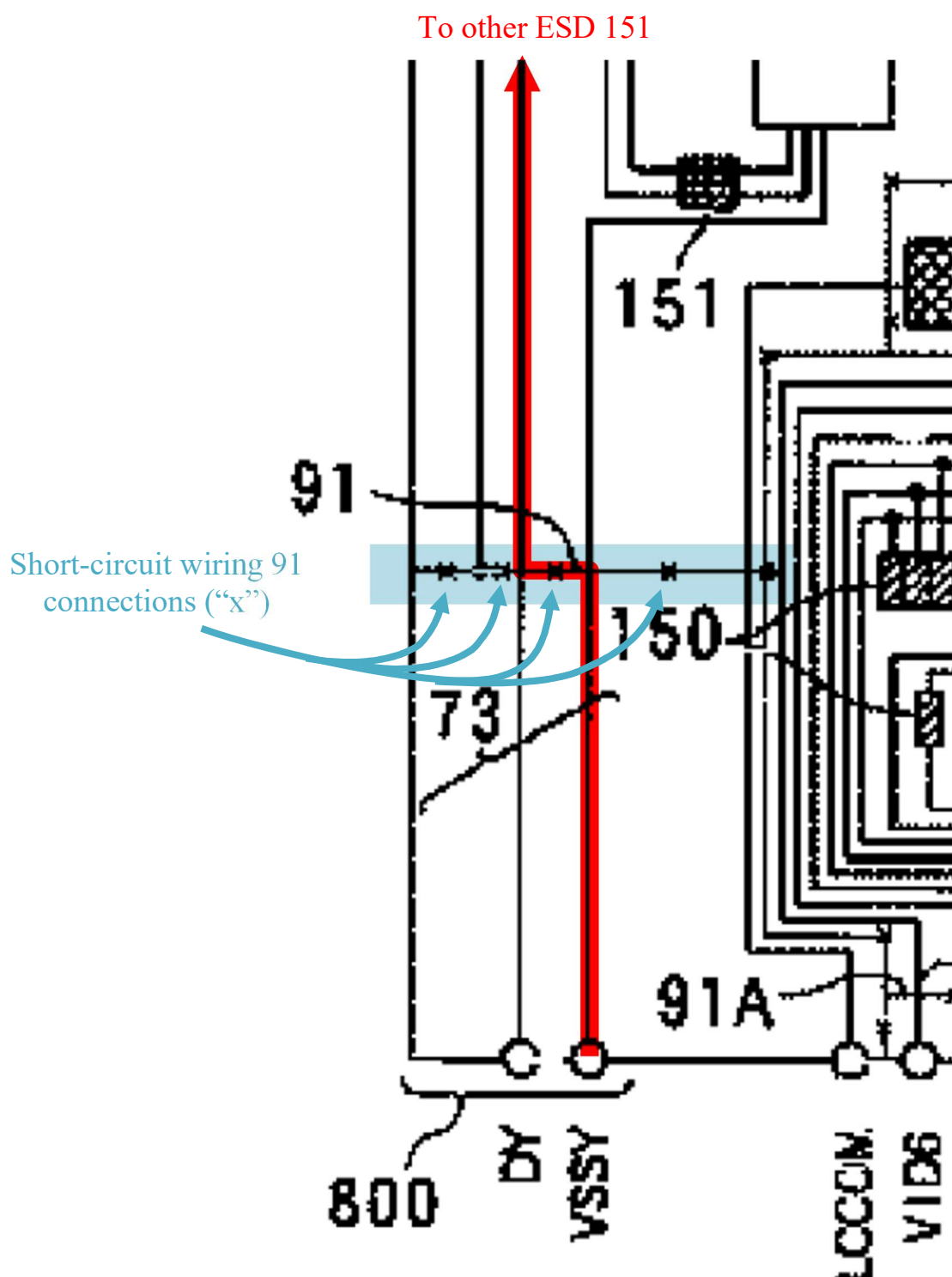
lines as part of the signal wirings, Dr. Schubert asks a POSITA to instead assume that they are all incorrect and should be rejected because the single right-hand bracket of FIG. 1 is next to and merely pointing towards power line VDDY. A POSITA would not reject *Takahara*'s multiple express disclosures based on the position of the right-hand bracket 73 in FIG. 1 that is, in fact, pointing towards the VDDY power line, especially when the other power lines are expressly encompassed by the brackets and (at a minimum) strongly suggested for VDDY.¹³

107. Dr. Schubert's second argument that *Takahara* does not disclose the short-circuit wirings 91 connecting the power lines VDDY/VSSY to the ESD protection circuits 151 (*see* Schubert Declaration ¶129) is contradicted by *Takahara*'s FIG. 1 and paragraph [0066]. *Takahara*'s short-circuit wirings are "marked with [an] 'x' in FIG. 1." *Takahara*, [0070]. As shown below in excerpted annotated FIG. 1, short-circuit wirings 91 ("x") connect the ESDs 151 to the power lines VDDY, VSSY. *Takahara* explains that "static electricity entering from ... the first short-circuit wiring 91" (e.g., from VSSY/VDDY) is diffused by the ESD protection circuit 151 to protect the scan-line drive circuit 104—that is, the ESD

¹³ I note that VSSY also provides the motivation for combining *Takahara* and *Reiner*. Thus, even if a POSITA were to adopt Dr. Schubert's inconsistent interpretation that VDDY is not part of the signal wirings, VSSY clearly is.

traveling on the short-circuit wirings 91 from the power lines VSSY/VDDY to other lines cannot reach the scan-line drive circuit 104 because of the ESD protection circuits 151. *Takahara*, [0066], FIG. 1. Such short-circuit connections also assist with connecting the wiring lines to the outer substrate. *See Takahara*, [0027].





Takahara, FIG. 1 (excerpted, annotated); *see also* *Takahara*, FIG. 3 (showing short-circuit wiring 91 between two ESD-protected lines).

108. Dr. Schubert is incorrect that “[t]he purpose of Takahara’s short-circuit wirings also contradicts [my] position,” and the “purpose of the short-circuit wirings ... to diffuse static electricity ‘toward an outer perimeter of the substate’” would preclude damage to the scan-line driver circuit. Schubert Declaration ¶¶130-131 (quoting *Takahara*, [0004]). Quite the contrary, *Takahara* expressly teaches disclosure that these protection circuits 151 perform precisely this function, as quoted above. *Takahara*, [0066]. Dr. Schubert’s statement that this requires the ESD to travel back towards the center of the substrate is not to the contrary. *See* Schubert Declaration ¶130. As is taught in basic electrical circuits courses, and certainly known to a POSITA, electrical current and voltage follow conductors such as metal lines, regardless of the orientation or direction of the conductors, which is why *Takahara* explains that ESD on short-circuit wiring 91 poses a risk to the scan-line drive circuit 104—because an ESD event on a wiring connected by the short-circuit wiring 91, such as VDDY/VSSY, could still damage the scan-line driver circuit 104. *See Takahara*, [0066].

109. Dr. Schubert’s third argument that the VDDY and VSSY connections in FIG. 3 are not “connected to the power supply line” would not change my opinion. Schubert Declaration ¶¶132-136. As I have stated above, *Takahara* clearly describes the connections through the short-circuit wirings 91.

110. Notwithstanding Dr. Schubert's arguments, none of the arguments in the Schubert Declaration address the **combination** of *Reiner* and *Takahara* in my previous declaration and based on *Takahara*'s basic teaching to protect scanning line driving circuits from ESD damage. As I previously explained, *Reiner* teaches that driver circuits are "very sensitive" and susceptible to ESD damage and being "destroyed" by ESD, and *Takahara* teaches using ESD protection circuits to "reliably protect[]" the scan line driver from ESD damage. *Takahara*, [0066]; Ex. 1003, ¶¶234-242; *Reiner*, 2:28-3:3.

C. A POSITA Would Have Been Motivated to Combine *Reiner* and *Takahara*

111. Dr. Schubert next argues that (1) "Reiner does not disclose or render obvious the claimed protection circuit arrangement" (Schubert Declaration ¶138); and (2) "Reiner provides an ESD protection network for silicon integrated circuits," while "Takahara provides protection circuits for signal lines and a short-circuit wiring to protect its panel" (Schubert Declaration ¶139). Neither of Dr. Schubert's opinions appears to address the reasons in my previous declaration that a POSITA would have found the claims obvious. As one example, I explained that *Reiner* discloses protecting **driver circuits** from ESD damage and, although suggested in *Reiner*, *Takahara* expressly discloses protecting scanning line driving circuits from ESD damage; thus, a POSITA would have found it obvious to also

protect *Reiner*'s scanning line driving circuit from ESD damage. *See Takahara*, [0066], FIG. 1; Ex. 1003, ¶¶234-242.

112. Dr. Schubert's remaining arguments related to purported differences between scanning line driver circuits and data drivers and allegedly different substrates (Schubert Declaration ¶140) are contradicted or not relevant for the reasons I describe above.

D. Claims 1-3 and 5-18 Would Also Have Been Obvious

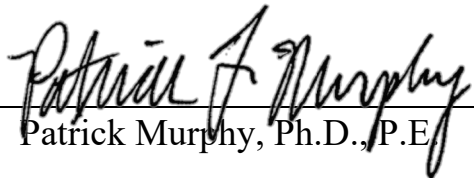
113. Dr. Schubert's opinions related to claims 1-3 and 5-18 merely incorporate previous arguments. Schubert Declaration ¶¶141-152. I disagree with his positions for the reasons stated above.

VIII. Conclusion

114. For the reasons set forth above, it remains my opinion that claims 1-18 of the '157 patent would have been obvious to a POSITA.

115. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 2, 2025

By: 
Patrick Murphy, Ph.D., P.E.