

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2024-00973
U.S. Patent No. 9,184,157

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	<i>REINER</i> DOES NOT RENDER OBVIOUS CLAIMS 1-18 (GROUND 1).....	2
A.	Petitioner Fails to Show that <i>Reiner</i> Renders Obvious Claim 4.....	2
1.	Petitioner’s reply fails to rebut Patent Owner’s arguments that <i>Reiner</i> does not disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f]).	2
2.	Petitioner’s reply fails to rebut Patent Owner’s argument that <i>Reiner</i> does not disclose or render obvious a “first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal” (claim 4[e]).	9
3.	Petitioner’s reply fails to rebut Patent Owner’s arguments that <i>Reiner</i> does not disclose or render obvious applying <i>Reiner</i> ’s ESD protection network for a source (data) driver to a gate (scanning line) driver given the differences between source and gate drivers (claims 4[d], 4[e], and 4[f]).	17
B.	Petitioner Fails to Show that <i>Reiner</i> discloses or renders obvious a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate” (claim 8).	18
III.	<i>REINER</i> IN VIEW OF <i>TAKAHARA</i> DOES NOT RENDER OBVIOUS CLAIMS 1-18 (GROUND 2)	18
A.	<i>Takahara</i> does not cure <i>Reiner</i> ’s failure to disclose or render obvious a display device comprising “an input terminal	

	connected to the power supply line to supply power” (claim 4[c]).	20
B.	<i>Takahara</i> does not cure <i>Reiner</i> ’s failure to disclose or render obvious “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” (claim 4[f]).	20
C.	Petitioner Fails to Show that a POSITA Would Have Been Motivated to Combine <i>Reiner</i> and <i>Takahara</i> .	21
IV.	CONCLUSION.	22

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Seachange Intern., Inc. v. C-COR, Inc.</i> , 413 F.3d 1361 (Fed. Cir. 2005).....	14, 15
Regulations	
37 C.F.R. § 42.24(a)(1)(i)	24

I. INTRODUCTION

Reiner is the conventional art on which the '157 patent improves, not the claimed invention. The claims specifically require that the scanning line driving circuit is connected to a power supply line *between* first and second protective circuits connected to that power supply line, to protect the scanning line driving circuit. *Reiner* teaches protective circuits inside a driving circuit chip connected between the chip's input and output pads or pins—access points through which static charges can enter an integrated circuit chip—and the chip's internal circuitry. The '157 patent expressly discloses the same arrangement—protective circuits connected between input terminals and internal circuitry to protect that internal circuitry—as the art upon which the '157 patent's claimed invention improves. Petitioner has not met its burden to show otherwise, and therefore has not met its burden to show the unpatentability of the '157 patent claims. Patent Owner maintains the arguments advanced in its Response and focuses on this critical distinction between *Reiner* and the patented invention in its Sur-Reply.

II. ***REINER* DOES NOT RENDER OBVIOUS CLAIMS 1-18 (GROUND 1).**

A. **Petitioner Fails to Show that *Reiner* Renders Obvious Claim 4.**

1. **Petitioner's reply fails to rebut Patent Owner's arguments that *Reiner* does not disclose or render obvious "the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected" (claim 4[f]).**

Petitioner's reply arguments fail to rebut that *Reiner* does not disclose or render obvious claim 4[f]. *See* POR, 32-42. The plain claim language requires that the "scanning line driving circuit [be] connected to the power supply line between" connections of first and second protection circuits to the power supply line. POR, 32-33. Petitioner does not dispute that *Reiner* does not disclose a driver that is connected to a power supply line between protection circuits. *Reiner* discloses only the prior art: an integrated circuit including internal ESD protection device near each input/output terminal. Petitioner concedes the limits of *Reiner*'s teachings and instead argues that claim 4 is broad enough to cover a layout in which protection circuits are connected *within* a scanning line driving circuit.

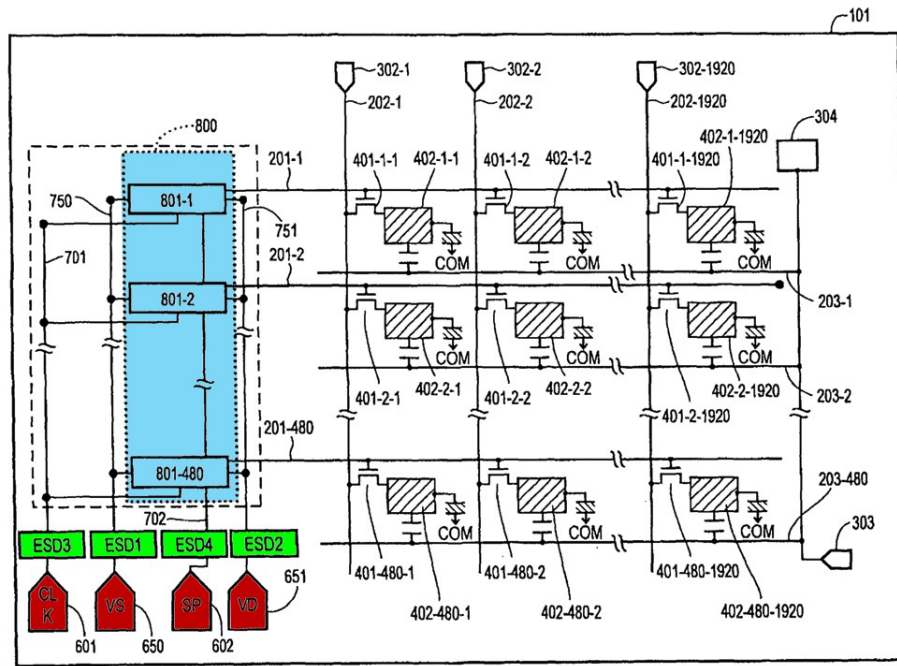
First, as discussed in detail below regarding claim 4[e], Petitioner fails to refute Patent Owner's correct interpretation that all scanning line driver

connections must be between the two protection circuit connections. Reply, 8, 13; *see* § II.A.2, *infra*.

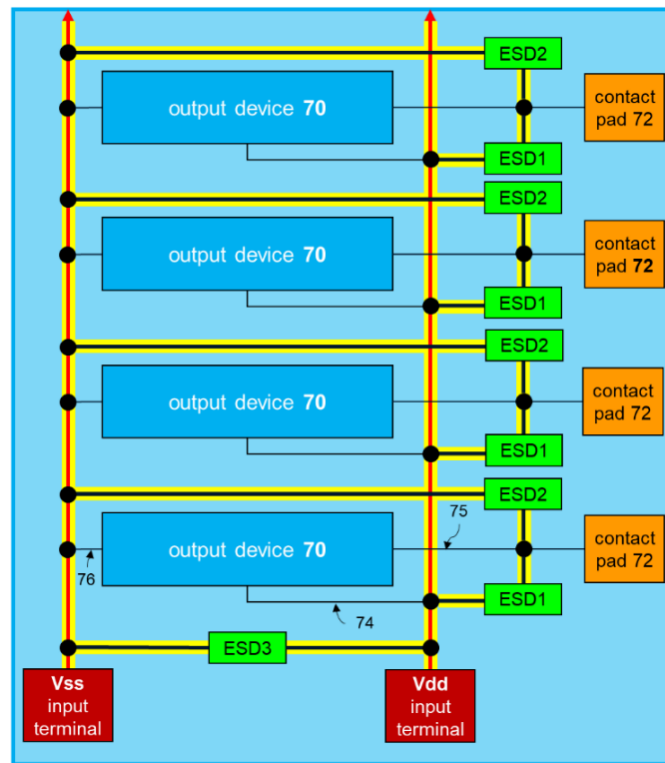
Second, Petitioner mischaracterizes and misunderstands Patent Owner's comparison of *Reiner* to the conventional art disclosed by the '157 patent. Reply, 14-15.

As laid out in Patent Owner's Response, the '157 patent explains that conventional ESD protection means protected conventional integrated circuits by preventing static charges from entering a device through its input terminals—i.e., ESD protection circuits are located between access points to the device (e.g., input terminals) and its internal circuitry. POR, 5-7, 33-35. The '157 patent explains that this ESD protection for conventional integrated circuits—placing protective circuits between input/output terminals and the internal circuitry—was applied to a display device including a built-in scanning line driving circuit to protect the active matrix from ESD damage, as shown in '157 Figure 11. *Id.*, 34-35. *Reiner* teaches the same configuration: protecting integrated circuit devices by protecting access points. POR, 34-40; Ex. 1005, 3:4-8 (an “ESD protection network” to protect integrated circuit devices comprises “protection diodes and/or transistors” connected to the “inputs and/or outputs of the integrated circuit device to be protected”).

Patent Owner's reoriented *Reiner* Figure 5 shows this—*Reiner* Figure 5, like Figure 11 of the '157 patent, teaches ESD protection between input/outputs of the circuitry to be protected. POR, 35-36. Patent Owner's reoriented Figure 5 does *not* include an arrangement dissimilar from '157 Figure 11, as shown in the following figures from Patent Owner's Response.



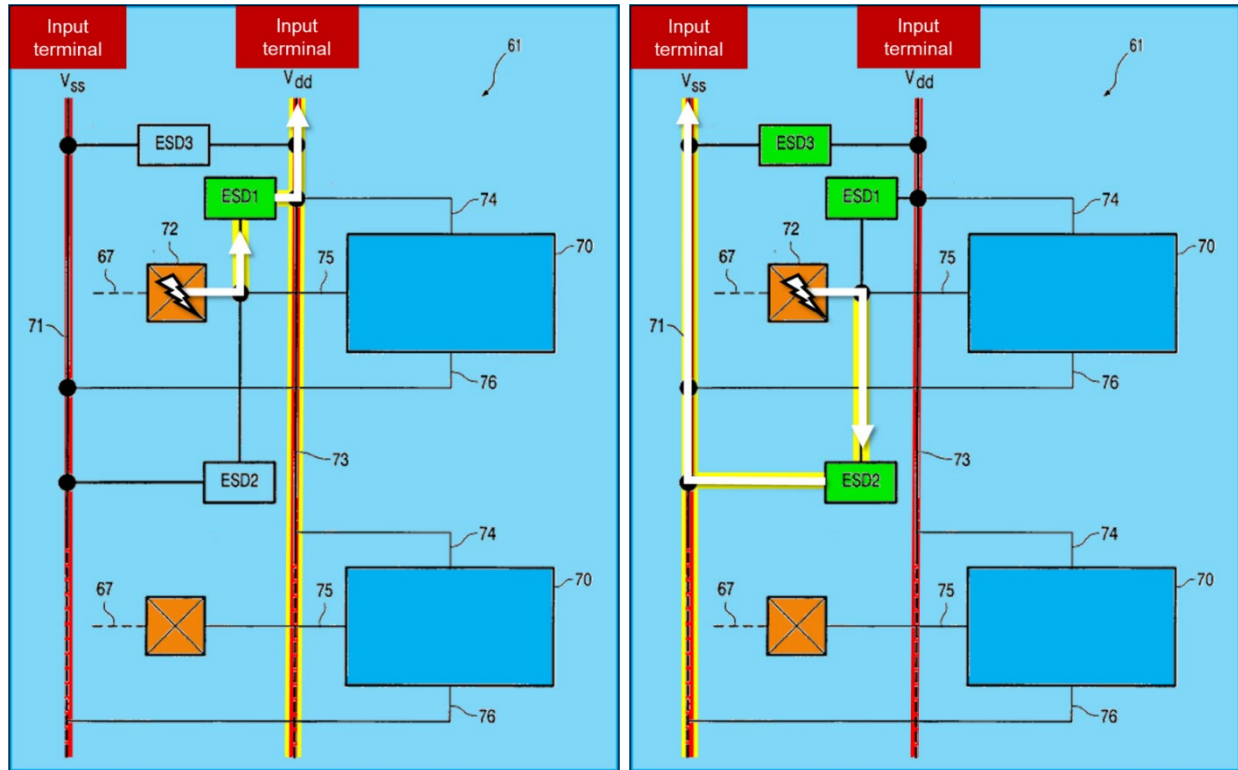
POR, 35 ('157 patent Fig. 11, annotated).



POR, 36 (*Reiner* reoriented Fig. 5, annotated).

Patent Owner's identification of an ESD1 and ESD2 protection circuit to protect individual output devices 70 does not, as Petitioner suggests, contradict the foregoing or in any way support "*Reiner* disclosing or rendering obvious . . . providing additional ESD protection away from the power line input terminal." Reply, 14. To the contrary, as shown in the annotated figures reproduced below, *Reiner's* ESD1 and ESD2 protect an access point to each output device 70: contact

pads 72 (the output pins of *Reiner*'s source driver 61 integrated circuit chip, highlighted in orange), as in the '157 conventional art.¹ POR, 20-22, 34-40.



POR, 37 (ESD1), 38 (ESD2).

Petitioner cites no evidence suggesting that *Reiner* discloses or renders obvious providing additional ESD protection away from input/output terminals.

Reply, 14-15.

¹ Dr. Murphy's opinions and testimony are not consistent with *Reiner*'s express disclosure regarding protecting the inputs/outputs of integrated circuit devices using low-ohmic paths because he did not analyze how *Reiner*'s ESD protection network functions to protect driver units 70, which necessarily implicates the "specific circuit layout of [the] ESD protection circuits." Reply, 20-21, n.14; POR, 40-41, n.5.

Figure 11 of the '157 patent shows fewer ESD protection circuits compared to *Reiner* only because it shows a scanning line driving circuit 800 (highlighted in blue in '157 patent Fig. 11, annotated shown above) that is formed on the array substrate of a display device and thus, by definition, does not have output access points external to the array substrate that require ESD protection. POR, 5-7, 33-35. The driving circuit and the scan lines to which it outputs scan signals are formed on the same array substrate and thus are not discrete components that must be connected—in short, no contact pads. *Id.* *Reiner*'s source driver 61, by contrast, is an integrated circuit chip that necessarily has output access points (contact pads 72) that require ESD protection, which *Reiner* provides with ESD1 and ESD2. POR, 20-22, 34-40.

Petitioner's assertion that Patent Owner agrees that "*Reiner*'s ESD1 and ESD2 protect the driver circuits 70 at least from electrostatic discharge entering through the signal lines," and that this is "all claim 4 requires," is incorrect and ignores critical claim language. Reply, 16. Patent Owner correctly identifies ESD1 and ESD2 as internal protection circuits that protect output devices 70 from electrostatic discharge that could enter through output access points (contact pads 72) not "signal lines." POR, 41-42. This point does not suggest that *Reiner* discloses a scanning line driving circuit that is connected to a power supply line between protection circuits, as claim 4 requires. POR, 41-42.

Third, Petitioner fails to rebut Patent Owner's assertion that *Reiner* does not disclose claim 4[f] because *Reiner*'s ESD devices shown in Figure 5 are *inside* integrated circuit source driver 61. Reply, 17-18. Dr. Murphy's testimony under cross-examination contradicts the distinction that he attempts to draw between "module" and "driving circuit" in his declaration supporting Petitioner's reply. Reply, 17-18; Ex. 1024 ("Murphy II"), ¶70 (opining that a "POSITA would have recognized that a 'module' may often include more than the circuitry [of the driver circuit] itself," such as *Reiner*'s power supply lines). However, Dr. Murphy testified that "a person of ordinary skill . . . looking at [*Reiner*'s gate drivers] would understand that metal lines like those depicted in Figure 2 are typically going to be part of . . . the circuitry that comprises the gate drivers" and that "power lines would reasonably be among" the functions served by those metal lines. Ex. 2008, 83:1-85:19. Further, Dr. Murphy's argument that a "module" may include other elements but the "driving circuit" is "the group of driver units 70 of *Reiner*" contradicts *Reiner*'s express disclosure: Figure 5 is "[a] schematic block diagram of a display driver 61 in accordance with the present invention" and "ESD protection means can easily be integrated into such a display driver 61." Ex. 1005, 9:20-23.

Finally, Petitioner fails to show that *Reiner* renders the claims unpatentable even "considering Patent Owner's argument" that *Reiner*'s ESD devices shown in

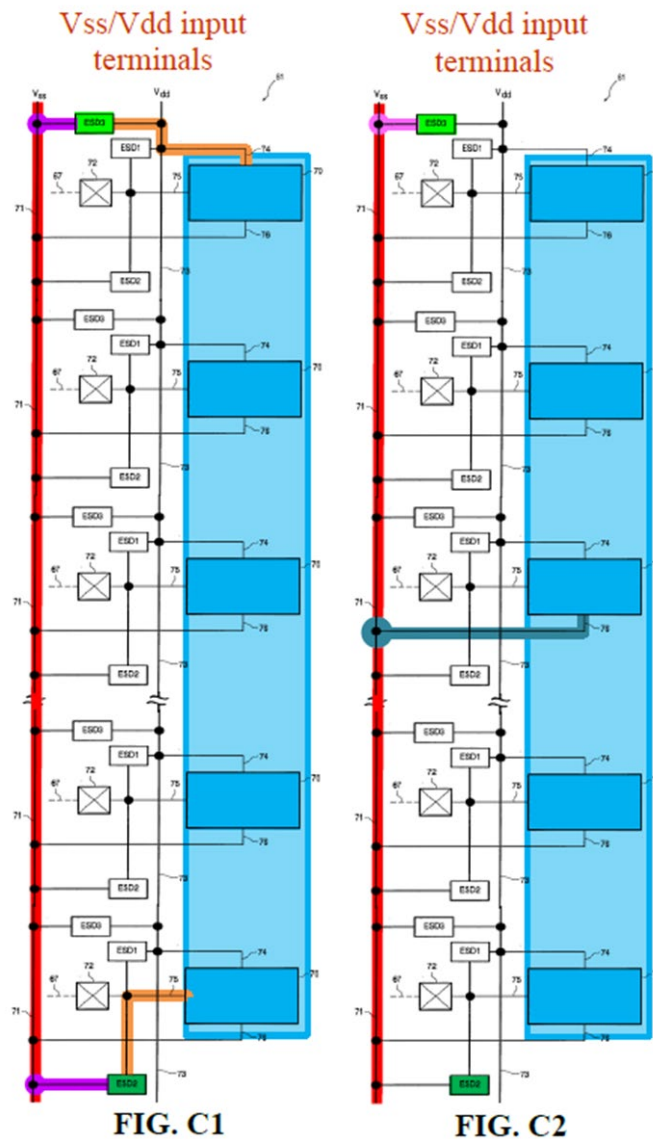
Figure 5 are inside *Reiner*'s source driver 61 integrated circuit chip. Reply, 17-21. Petitioner's comment that "broadly speaking" "to" does not exclude the word "in" is meaningless: the critical claim language preposition recites the scanning line driving circuit being connected to the power supply line *between* protection circuit connections to the power line. Petitioner's assertion that "there is no difference in structure or operation" per its annotated figures² fails to rebut Patent Owner's arguments that there are key differences between *Reiner* and the claims of the '157 patent—*Reiner* does not disclose a scanning line driving circuit connected to the power supply line between first and second protection circuits—that render those claims patentable. *See* POR at 32-42.

2. Petitioner's reply fails to rebut Patent Owner's argument that *Reiner* does not disclose or render obvious a "first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal" (claim 4[e]).

To start, Patent Owner does *not* admit that Petitioner's Figures Cx disclose all limitations of claim 4. Relevant to this claim limitation, Petitioner's expert, Dr.

² Patent Owner disputes Petitioner's annotations, specifically, Petitioner's annotations to Figure 2 showing the scanning line driving circuit as encompassing more than the dashed-line box 800, and Figures A1-C1 from the original Petition. Reply, 19-20. Those annotations are contrary to the patent's written description of Figure 2.

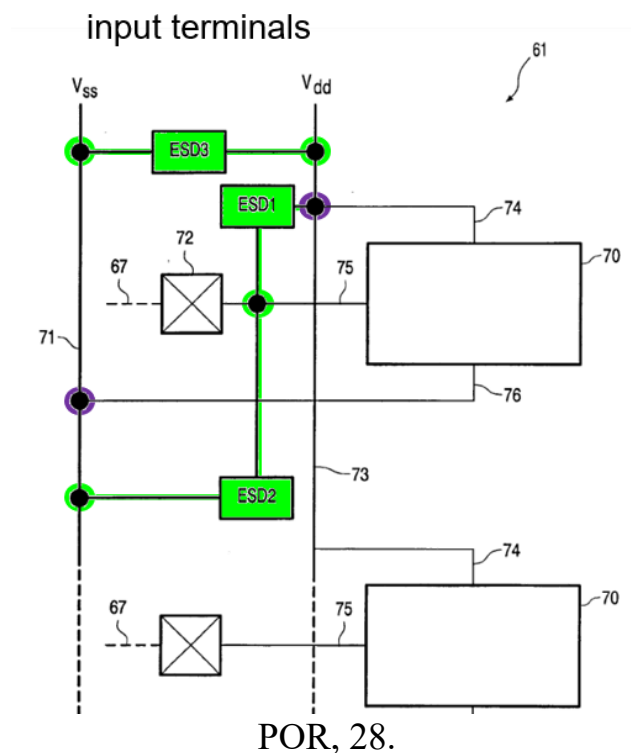
Murphy, has not opined that ESD3, as shown in Petitioner’s Figure C1, is “connected to” the top output device 70 (the claimed “scanning line driving circuit”)—under cross-examination, he could not or would not offer an opinion, including applying Patent Owner’s “construction” with which he disagrees. Ex. 2008 (Murphy Tr.), 128:2-5 (“Q So in your opinion, is ESD3 connected to output device 70? A I haven’t developed an opinion on that question.”), 128:6-133:9 (confirming he has no opinion as to whether ESD3 is connected to output device 70 as a person of skill in the art applying the plain and ordinary meaning of “connected to”). Therefore, Petitioner has not met its burden to show the unpatentability of claim 4 under its mappings C1 and C2 (reproduced below). *See* POR, 27-32.



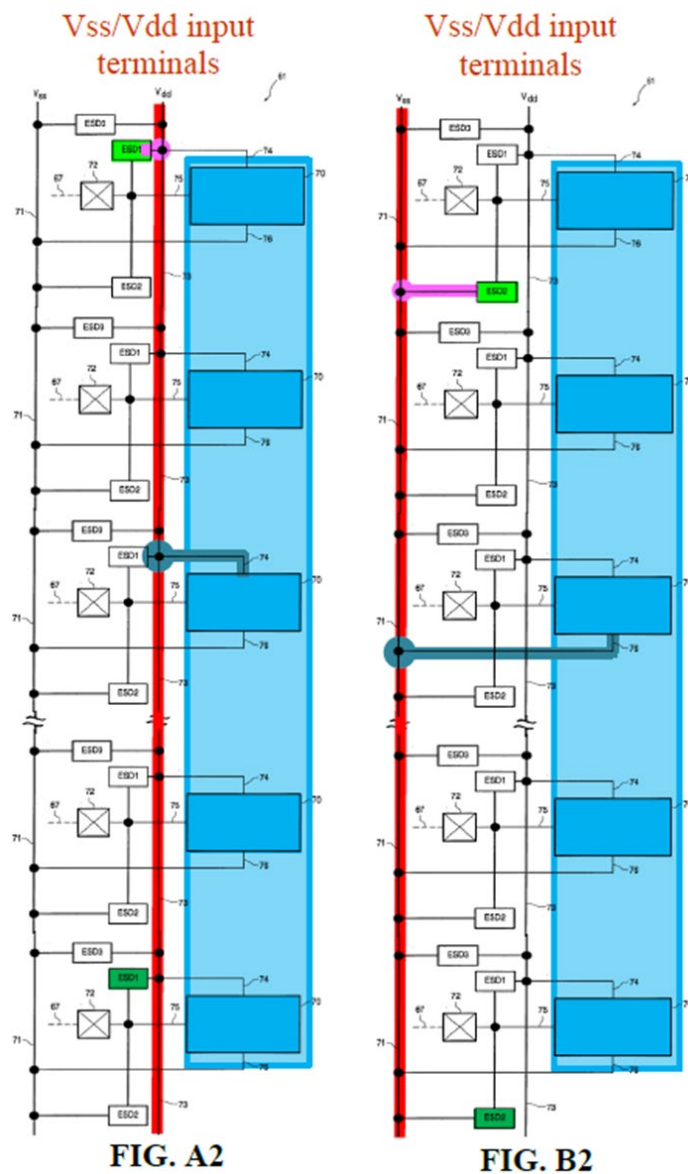
Ex. 1003, ¶¶110, 123 (excerpted, showing Petitioner’s annotations).

Petitioner’s assertion that Patent Owner avoids its “own” claim construction in this proceeding is incorrect. Reply, 9-10. Rather, Patent Owner points out that Petitioner has not adduced sufficient evidence to support an argument that ESD3 is connected to the claimed scanning line driving circuit. *See id.* (citing Ex. 1014, ¶¶136-144); Pet., 27-28 (Figure C1), 35-36 (Figure C2), 38-39 (Figure C3).

Further, Petitioner cannot show that *Reiner's* ESD1 or 2 discloses or renders obvious a claim 4[e] because neither ESD1 nor ESD2 is “connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal” as shown in Patent Owner’s following POR figure. *See* POR, 27-28 (ESD1 is connected to line Vdd *at the same location* at which the source driver first connects to line Vdd (highlighted in purple); ESD2 is connected to connected line Vss *after* the location at which the source driver first connects to line Vss (highlighted in purple)).



Petitioner manufactures a claim construction dispute to try to save its mappings A2 and C2, reproduced below, which show the scanning line driving circuit connected to the power line (dark blue highlighting) *after* the location where the first protection circuit (light green highlighting) is connected to the power supply line (pink highlighting).



Ex. 1003, ¶¶110, 123 (excerpted, showing Petitioner's annotations).

But the plain claim language, understood in view of the claim as a whole and the '157 specification, confirms that claim 4 recites a first protection circuit connected to the power supply line *between* where the scanning line driving circuit is connected to the power supply line—the scanning line driving circuit *as a whole*, not a component of the scanning line driving circuit—and the input terminal. POR, 27-28.

Petitioner's citation to claims 10 and 18 make Patent Owner's point. Petitioner asserts, in view of claims 10 and 18, that "a first connecting portion" in claim 4 connecting the scanning line driving circuit and power line "need only be one driver unit's connection, not all driver units' connections." Reply, 11-12. Petitioner's argument ignores the doctrine of claim differentiation. *Seachange Intern., Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1368-69 (Fed. Cir. 2005) ("The doctrine of claim differentiation stems from the common sense notion that different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope.") (quotation and citation omitted).

Claims 10 and 18 recite "a first connecting portion" and a second and third connecting portion in terms of where a circuit element—a *part* of the scanning line driving circuit—is connected to the power supply line. Ex. 1001, claims 10[e] and 18[e] ("a first connecting portion at which **the circuit element** and the power supply line are connected"), 10[f] and 18[f] ("**the circuit element** being connected

to the power supply line between [a second and a third connecting portion]”) (emphasis added).

By contrast, claim 4 recites “a first connecting portion” in terms of where the scanning line driving circuit—not a part of the scanning line driving circuit—is connected to the power supply line. *Id.*, claim 4[e] (“a first connecting portion at which **the scanning line driving circuit** and the power supply line are connected”), 4[f] (“**the scanning line driving circuit** being connected to the power supply line between [second and third connecting portions]”) (emphasis added). *Seachange*, 413 F.3d at 1369 (there is “a presumption that two independent claims have different scope when different words or phrases are used in those claims”). Indeed, claim 4[f] confirms that claim 4 recites a scanning line driving circuit—the circuit, not intermediate components of the circuit—connected between two protection circuits. POR, 31. Petitioner’s assertion that “a first connecting portion at which the scanning line driving circuit and the power supply line are connected” (claim 4) must be “interpreted the same” as “a first connecting portion at which the circuit element and the power supply line are connected” (claims 10, 18), Reply at 11-12, is similarly contrary to the plain claim language. Petitioner’s argument that claim 4 “does not exclude other ‘connecting portion[s],’” Reply at 10-11, fails for the same reason.

Furthermore, Petitioner’s argument that its Figures Ax and Bx—and its newly annotated versions of ’157 patent Fig. 2, Reply at 13—“align with various embodiments” of the ’157 patent that include “additional ESD protection circuits in various combinations” falls flat. Reply, 12-13. First, Petitioner’s self-serving annotations, without citation to the ’157 specification, cannot change the scope of the plain claim language. Second, and more important, Petitioner overlooks portions of the specification (specifically, the Second Embodiment) and claim 1, which describe ESD protection circuits *at intermediate locations* within the scanning line driving circuit *and* protection circuits between input terminals and the scanning line driving circuit. Figure 2 discloses protection circuits connected to the power supply line between a first connecting portion at which the scanning line driving circuit and the power supply line are connected, and also *other* protection circuits that are not positioned as claim 4 recites. Ex. 1001, 7:25-34 (describing Fig. 2 and noting that “[i]n the present embodiment, not only the input part protective circuits ESD1 to ESD3 between the terminals 601, 650 and 651 and the scanning line driving circuit 800, and the internal protective circuits ESD11 to ESD13 located at the far end with the driving circuit 800 therebetween as seen from the input terminals 601, 605 and 651, but also eighth to tenth protective circuits ESD21 to ESD23 are provided between the unit driving circuit 801-240 at

the 240th stage, which is an intermediate stage of the driving circuit 800, and the unit driving circuit 801-241 at the 241st stage.”).

Notably, unlike Petitioner, Patent Owner’s arguments are consistent with the different claim limitations between claim 4 and claims 10 and 18. *Compare* POR, § VI.A.2.a.iii-iv (claim 4) *with* POR, §§ VI.A.2.h (claim 10) and VI.A.2.o (claim 18).

3. Petitioner’s reply fails to rebut Patent Owner’s arguments that *Reiner* does not disclose or render obvious applying *Reiner*’s ESD protection network for a source (data) driver to a gate (scanning line) driver given the differences between source and gate drivers (claims 4[d], 4[e], and 4[f]).

Patent Owner’s POR offers expert testimony highlighting Petitioner’s failure to provide evidence or argument sufficient to prove that *Reiner*’s ESD protection network applies, unaltered, to a scanning line driving circuit, and explaining that a POSITA would not expect *Reiner*’s source driver ESD protection network to translate, without any alteration, to a gate (scanning line) driver. In its reply, Petitioner offers no new evidence or explanation. Protecting an integrated circuit is not a reason to provide an ESD protection network in a particular layout (source driver) within a different integrated circuit (gate driver) with a different layout, function, and operation.

Petitioner fails to rebut that a POSITA would not assume that the ESD protection network within a source driver IC chip shown in *Reiner* Figure 5 would

apply without alteration to a gate driver in light of the different layouts, functions, and operations of a source driver compared to a gate driver. Reply, 3-8; POR, 24-26.

B. Petitioner Fails to Show that *Reiner* discloses or renders obvious a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate” (claim 8).

Patent Owner disputes Petitioner’s assertions that Patent Owner’s arguments under this claim are incorrect. *See* Reply, 23-26.³ Patent Owner’s arguments in its Response show that *Reiner* does not disclose or render obvious a display device comprising “a substrate” and “the scanning line driving circuit being arranged on the substrate.” POR, 43-47.

III. *REINER* IN VIEW OF *TAKAHARA* DOES NOT RENDER OBVIOUS CLAIMS 1-18 (GROUND 2)

Petitioner’s Ground 2 arguments rest on its flawed assertion that short-circuit wirings 91 connect the power lines to ESD protection circuits 151. Reply, 26-29. Petitioner is incorrect; *Takahara* does not disclose that the short-circuit wirings connect the power lines to the signal lines and the ESD protection circuits 151 disposed on the signal lines. *See* POR, 52-58, 59-68.

³ Patent Owner disputes Petitioner’s assertion that the purpose of or motivation to use *Reiner*’s “flip-chip” technology relates to “mounting the source/data and gate/scan lines drivers on the LCD panel.” *See* Reply, 24-25, n.15; POR, 43-47; Ex. 2009 (Schubert Declaration), ¶¶88-100.

Petitioner’s new assertion that *Takahara* identifies where short-circuit wirings 91 connect the power lines (which lack ESD protection circuits) to the signal lines with an “x,” as shown in Figure 1, is wrong. Reply, 26-28. *Takahara* explains that “x” marks on the short-circuit wirings 91 shown in Figure 1 show where the short-circuit wirings are cut. Ex. 1007, ¶[0070] (short-circuit wirings 91 “are cut at the locations marked with ‘x’ in FIG. 1 at an appropriate stage in the manufacturing process.”). Furthermore, *Takahara* discloses only connections between the short-circuit wirings 91 and signal wirings 72 or 73, not VSSY or VDDY as Petitioner erroneously asserts. *See* POR, 52-58, 59-68. Specifically, as shown in *Takahara* Figure 4, “contact hole[s] 403” are the connections between “the first short-circuit wiring 91 and the signal wirings 72 and 73. Ex. 1007, ¶¶[0068]-[0069], Fig. 4.

Petitioner’s assertion that *Takahara*’s disclosure contradicts Patent Owner’s argument is also wrong. Reply, 29. *Takahara* explains that “what connects the first short-circuit wiring 91 to the signal wiring 72 (or 73)”—i.e., contact holes 403 shown in Figure 4 not the “x” marks in Figure 1—“is between” the signal wiring input terminals and ESD protection circuits 151 such that static electricity entering from the terminals or the short-circuit wiring 91 “does not reach . . . the scan-line driving circuit 104 unless it passes through” ESD protection circuits 151. Ex. 1007, ¶[0067], Fig. 3. Petitioner fails to rebut Patent Owner’s correct position that

Takahara does not disclose that short-circuit wirings 91 connect the power lines to the signal lines. *See* POR, 52-58, 59-68.

A. *Takahara* does not cure *Reiner*'s failure to disclose or render obvious a display device comprising "an input terminal connected to the power supply line to supply power" (claim 4[c]).

Petitioner's claim 4[c] arguments, Reply at 29, fail to show that *Reiner* in view of *Takahara* disclose or render obvious a display device comprising "an input terminal connected to the power supply line to supply power" for the reasons identified in Patent Owner's Response. *See* POR, 58.

B. *Takahara* does not cure *Reiner*'s failure to disclose or render obvious "the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected" (claim 4[f]).

Petitioner's claim 4[f] arguments, Reply at 29-36, fail to show that *Reiner* in view of *Takahara* disclose or render obvious "the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected" for the reasons identified in Patent Owner's Response. *See* POR, 58-68. Petitioner does not address this argument at all and concedes that

if *Reiner* does not disclose or render obvious claim element 4[f], then *Takahara* cannot fill that gap.

And Petitioner's new argument that *Takahara* discloses power lines VDDY and VSSY being "connected to" ESD protection circuits 151 through short-circuit wirings 91 as indicated by the "x" marks in Figure 1, Reply at 33-36, is incorrect, as discussed above.

Furthermore, Petitioner fails to rebut Patent Owner's argument that *Takahara* Figure 3 does not show that *Takahara*'s protection circuits are connected to a power supply line. Reply, 36 n. 19. Petitioner is incorrect that this argument, which it fails to rebut at all, is "not material" because *Takahara*'s power supply lines VDDY and VSSY are not connected to ESD protection circuits 151 through short-circuit wirings 91, as discussed above.

C. Petitioner Fails to Show that a POSITA Would Have Been Motivated to Combine *Reiner* and *Takahara*.

Patent Owner's arguments against Petitioner's motivations to combine *Reiner* and *Takahara* address Petitioner's asserted combination and show that a POSITA would not have been motivated to combine *Reiner* and *Takahara*. See POR, 69.

IV. CONCLUSION

The Petition and Petitioner's reply do not establish the unpatentability of any of the challenged claims by a preponderance of the evidence. The Board should deny the request for cancellation.

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Date: August 1, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

I certify that this Patent Owner's sur-reply complies with the word count limit and contains 3,870 words in 14-point Times New Roman font as calculated by the word count feature of Microsoft Office, in compliance with 37 C.F.R. § 42.24(a)(1)(i). This word count is inclusive of all text and footnotes but does not include the table of contents, table of authorities, certificate of service or word count.

Date: August 1, 2025

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CERTIFICATE OF SERVICE

I certify that on August 1, 2025, a copy of Patent Owner's Sur-Reply, including exhibits, was served in its entirety by electronic mail to Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

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