

**BOE Technology Group Co., Ltd.,
Petitioner**

v.

**138 East LCD Advancements Limited,
Patent Owner**

IPR2024-00973

U.S. Patent No. 9,184,157

Oral Argument October 8, 2025

Patent Owner's Demonstrative Exhibits

Petitioner cannot meet its burden.

- **Reiner** discloses an ESD protection network inside an integrated circuit.
- **Takahara** discloses signal lines (not power supply lines) connected to only one protection circuit.
- Neither reference, alone or in combination, renders obvious the invention: a scanning line driving circuit connected to a power supply line between two protection circuits connected to that line.

See generally POR.

The '157 Patent



US009184157B2

(12) **United States Patent**
Kobashi

(10) **Patent No.:** **US 9,184,157 B2**
(45) **Date of Patent:** **Nov. 10, 2015**

(54) **SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS**
(75) **Inventor:** **Yutaka Kobashi, Fujimichou (JP)**
(73) **Assignee:** **SEIKO EPSON CORPORATION, Tokyo (JP)**

(58) **Field of Classification Search**
CPC H01L 27/0251; G02F 1/136204
USPC 361/56, 111
See application file for complete search history.

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 207 days.

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(22) **Filed:** **May 6, 2009**

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US 2009/0251834 A1 Oct. 8, 2009

(63) **Continuation of application No. 11/101,450, filed on Apr. 8, 2005, now Pat. No. 7,755,875.**

(30) **Foreign Application Priority Data**
Jul. 5, 2004 (JP) 2004-198040

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H02H 9/00 (2006.01)
H01L 27/02 (2006.01)
G02F 1/1362 (2006.01)
G09G 3/32 (2006.01)
G09G 3/36 (2006.01)
H01L 27/12 (2006.01)

(52) **U.S. Cl.**
CPC **H01L 27/0251** (2013.01); **G02F 1/136204** (2013.01); **G09G 3/3208** (2013.01); **G09G 3/36** (2013.01); **H01L 27/1214** (2013.01); **G09G 2300/043** (2013.01); **G09G 2300/0819** (2013.01); **H01L 27/12** (2013.01)

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(Continued)

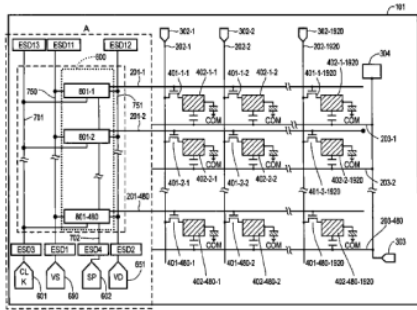
Primary Examiner — Rexford Barrie
Assistant Examiner — Tien Mai
(74) **Attorney, Agent, or Firm** — Oliff PLC

US 9,184,157 B2

SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

(57) **ABSTRACT**

To prevent an electrostatic damage on a display device formed with a driving circuit. Protective circuits are provided not only at input terminal parts, but also at intermediate parts of a circuit or at the ends of wiring lines. Otherwise, the protective circuits are provided at the ends of the wiring lines and at the places immediately before and after the input terminals, respectively, and then the circuit is interposed therebetween. Further, the protective circuits are provided around a circuit with a large current consumption.



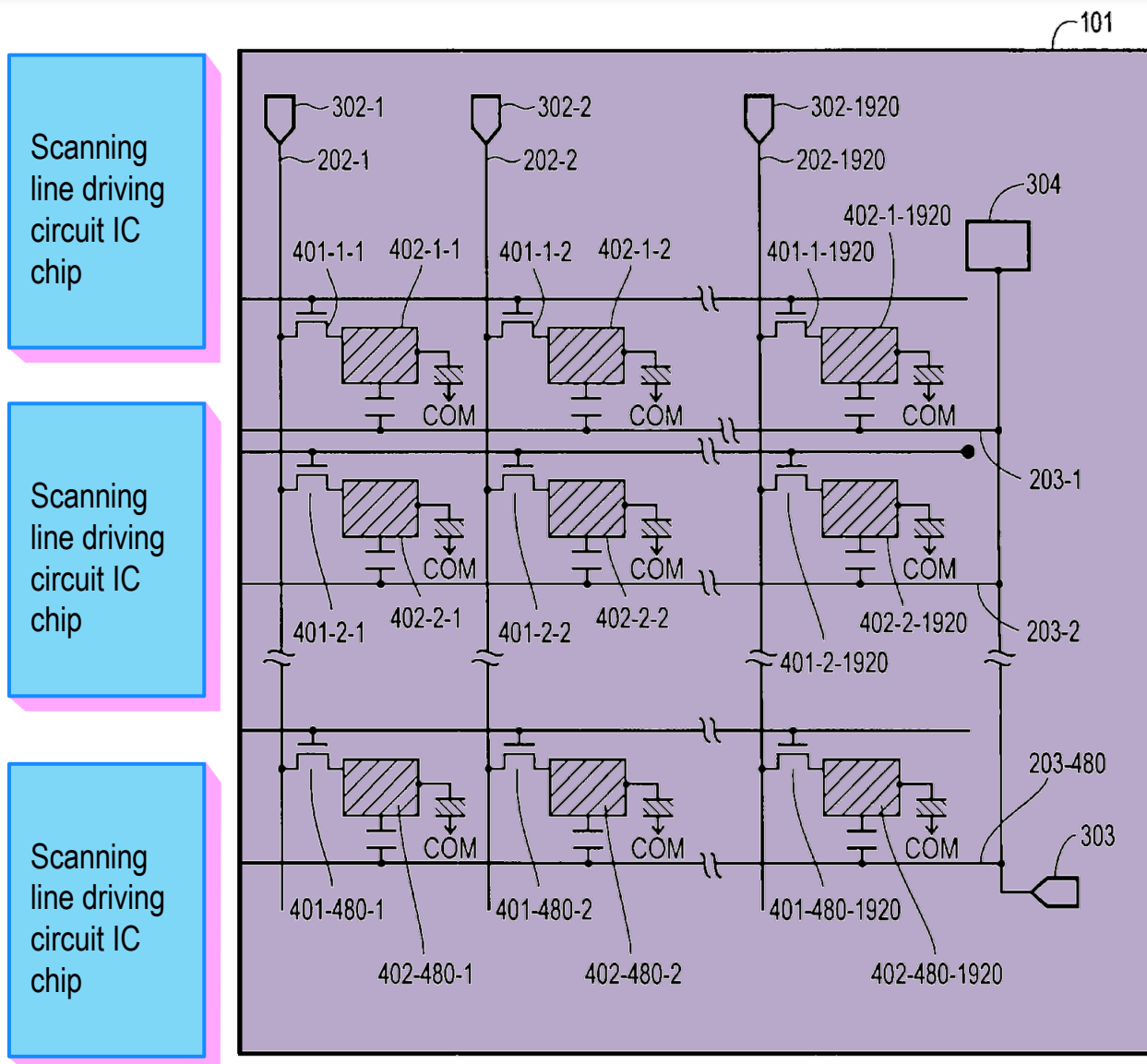
The '157 Patent: The Problem

In a semiconductor device, it is important to take measure against the electro-static damages (ESD) when a high voltage caused by a static electricity or a various noise phenomenon is unintentionally applied to the inside of the device to damage an insulating film, thereby causing a fatal damage to the device. In order to prevent the problem, various protective circuits have been proposed. For example, in Patent Documents 1 and 2, it has been proposed that an abnormal voltage applied to lines is discharged to GND, etc. by proper combination of diodes. However, since general semiconductor devices are formed on a silicon wafer made of conductive material, there are little chances of being electrified within the semiconductor device, so that it is a key issue to prevent the damage when a static electricity flows through input terminals. To solve such a problem, conventionally, protective circuits are formed between input terminals and the semiconductor device forming a circuit, i.e., immediately after the input terminals, so that it is prevented that the high voltage from the input terminals is transmitted to the device.

The present invention relates to a semiconductor device, display device and electronic apparatus, and more particularly, to a display device having a driving circuit provided on an active matrix substrate.

The scanning lines **201-1** to **201-480** are connected to the scanning line driving circuit **800**, which is formed by integrating polysilicon thin film transistors on the active matrix substrate, thereby being supplied to a drive signal. Herein, the scanning line driving circuit is composed of 480 scanning line driving unit circuits **801-1** to **801-480**, which are connected to each of the scanning lines. In the present invention, the semiconductor circuit in the scope of claims is the scanning line driving circuit **800**. Further, the wiring lines in the scope of claims represents a CLK signal line **701**, a SP signal line **702**, a high potential power source line **751**, and a low potential power source line **750**.

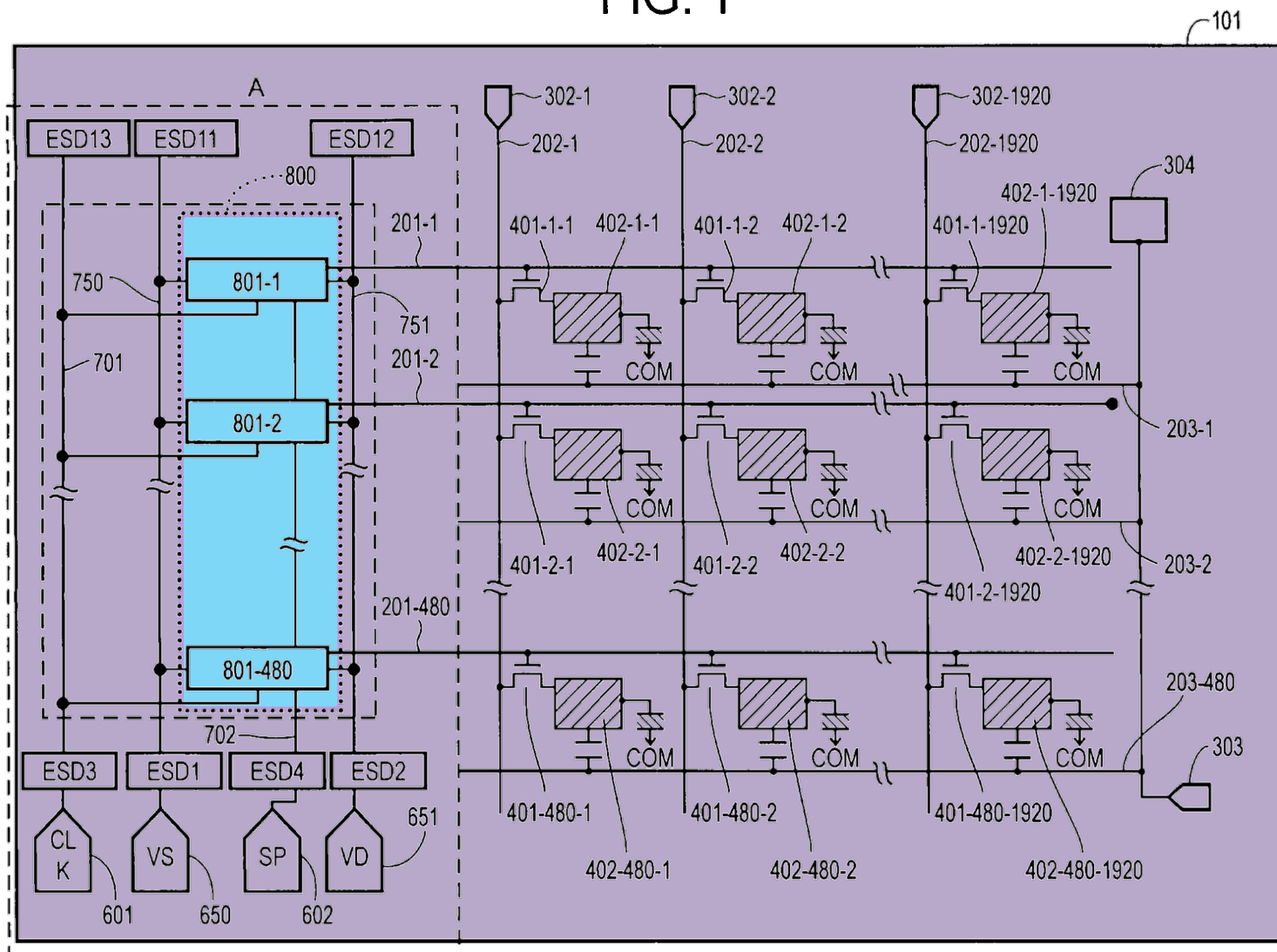
The '157 Patent: The Problem



Ex. 1001 at Fig. 1; POR at 3-5.

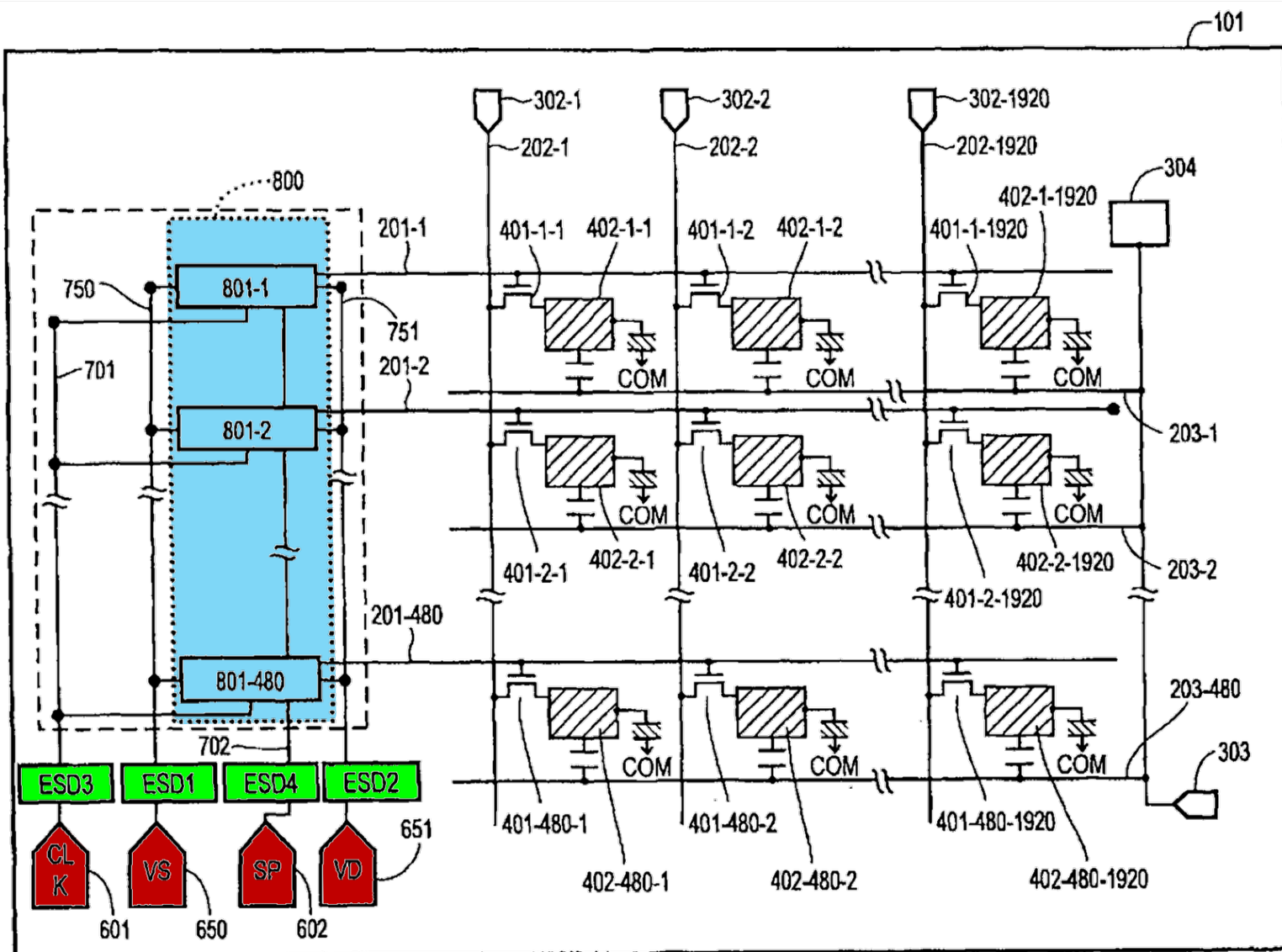
The '157 Patent: The Problem

FIG. 1



Ex. 1001 at Fig. 1; POR at 3-5.

The '157 Patent: The Problem



Ex. 1001 at 1:47-54, 2:20-30, Fig. 11; POR at 5-6.

The '157 Patent: The Problem

On the other hand, in a display device using an active element such as a thin film transistor (TFT), which has been rapidly spread in recent years, a device is formed on an insulating substrate. As a result, there is a problem in that it is easy that the device is easily electrified by static electricity, and that the electro-static damage is generated during the manufacturing process. On this account, for example, an electro-static measure is taken by forming an antistatic line, called as a guide ring or a short ring, at the periphery of an active matrix circuit.

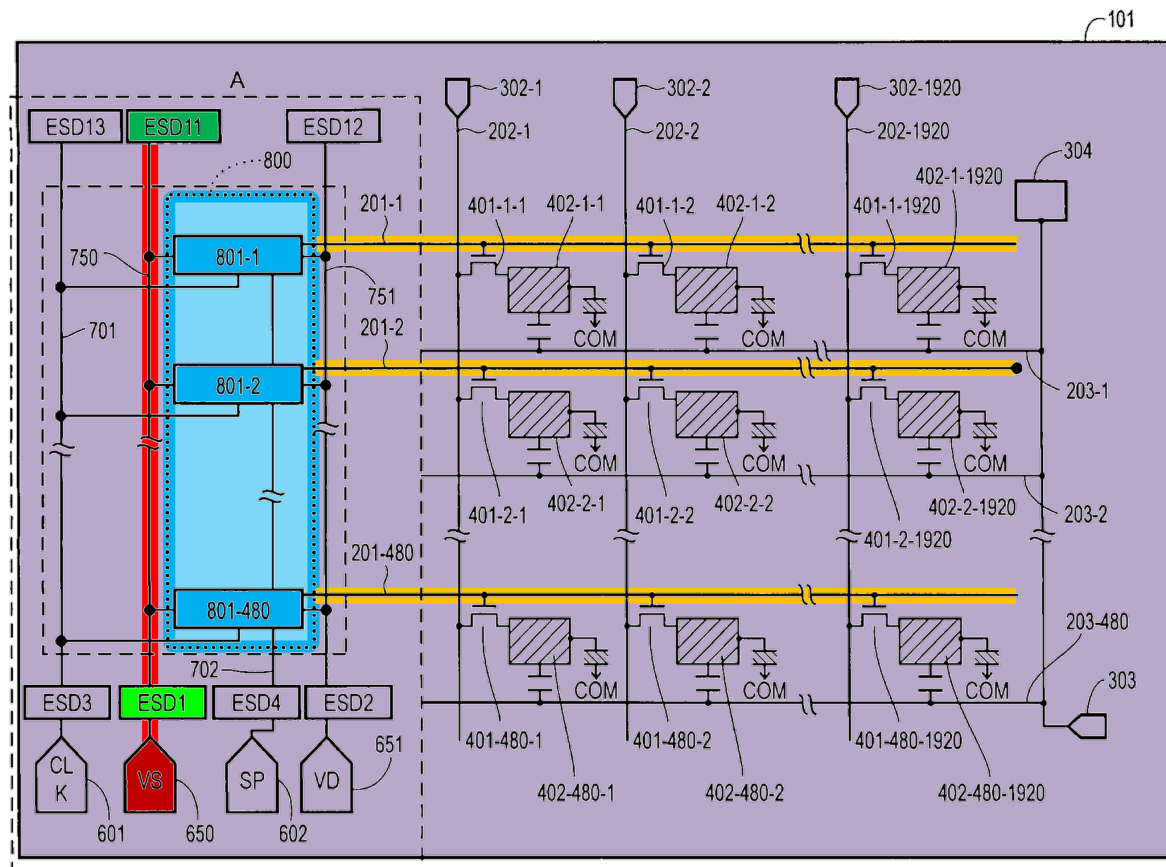
However, in the driving circuit on an insulating substrate, it is difficult for charges to escape as compared to the circuit on silicon wafer, and it is easy to be electrified. In addition, in the case that the driving circuit of the display device is formed on a glass substrate, the area of the circuit is larger as compared to the IC formed on a general silicon wafer. Therefore, in such a configuration, there is a problem in that a protection of the wiring lines far from the input terminals against the static electricity is not sufficient, especially during a manufacturing process. Specifically, since there is a possibility that the static electricity is electrified on a certain location on the substrate during the manufacturing process, when the distance from the electrified location to the static electricity protection circuit is long and the line resistance is high, a transistor within a circuit located closer than the static electricity protection circuit is damaged by the static electricity even before the static electricity protection circuit starts the operation. Such a problem is the same in a semiconductor device using a SOI substrate.

Ex. 1001 at 1:33-43, 2:33-50; POR at 5.

The '157 Patent: The Solution

ESD1 is connected to “a connecting line between the low potential power terminal 650 and the low potential power source line 750, . . . thereby preventing TFTs within the scanning line driving circuit 800 from being damaged when the static electricity or noise current is input from [terminal 650].”

ESD11 is “disposed at far end of the opposite side, as seen from . . . the low potential power source terminal 650 on the low potential power source line 750, with a scanning line driving circuit 800 therebetween. Thereby, it is possible to suppress that a unit, (for example, $n=1$, etc.), located far from a terminal, among scanning line driving unit circuits 801- n , is damaged by the static electricity during manufacturing the active matrix substrate.”



Ex. 1001 at 5:44-6:2, Fig. 1; POR at 7-9.

U.S. Patent No. 9,184,157: Claim 4

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Ex. 1001 at claim 4.

**Ground 1: Reiner does not
render obvious any challenged
claim.**

Reiner does not render obvious any challenged claim.

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Ex. 1001 at claim 4; POR at 22-42.

Reiner: Overview

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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International Bureau



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WO

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Holstlaan 6, NL-5656
ZALDIVAR, Jose; hoven (NL).

(21) International Application Number: PCT/IB02/03410

(22) International Filing Date: 21 August 2002 (21.08.2002)

(74) Agent: VOLMER, B.V., Prof. Holstlaan

(25) Filing Language: English

(81) Designated States (f

(26) Publication Language: English

(84) Designated States (f BG, CH, CY, CZ, DE LU, MC, NL, PT, SI

(30) Priority Data: 01120555.6 29 August 2001 (29.08.2001) EP

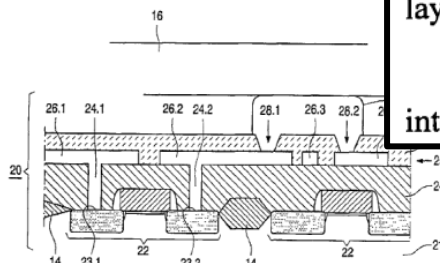
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Published: — without international upon receipt of that

(72) Inventors: REINER, Joachim, C.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). RZITTKA, Eckart; Prof.

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ning of each regular issue

(54) Title: INTEGRATED CIRCUIT DEVICE WITH BUMP BRIDGES AND METHOD FOR



(57) Abstract: Text Integrated circuit device (20) comprising a silicon substrate (21), integrated devices (22) with contacts (23.1, 23.2), an isolating layer (24) at least partially covering the integrated devices (22) and comprising conducting areas (24.1, 24.2) which establish a conductive path to the contacts (23.1, 23.2) of the integrated devices (22). A metallization level (25) with metal lines (26.1, 26.2, 26.3, 26.4) is provided which connect to one of the contacts (23.2). The metal lines (26.1, 26.2, 26.3, 26.4) are situated above the isolating layer (24). A passivation layer (27) - situated above the metallization level (25) - comprises at least two contact areas (28.1, 28.2) for partially exposing at least two of the metal lines (26.2, 26.4). A bump bridge (29) comprising a conductive, low-resistance material, is situated on the passivation layer (27). The bump bridge (29) has a high aspect ratio and provides for a conductive connection between at least two of the metal lines (26.2, 26.4). It crosses another metal line (26.3) that is situated within the metallization level (25), without making contact to this metal line (26.3), and a substantial part of the bump bridge (29) is supported by the passivation layer (27).

Integrated circuit device with bump bridges and method for making the same

It is an object of the present invention to provide a scheme that overcomes the disadvantages of known approaches that are either too expensive or too bulky.

It is an object of the present invention to provide a scheme that allows for an improved interconnection of metal lines in integrated circuit chips having just one metallization layer.

It is an object of the present invention to provide a scheme that allows to add an ESD protection network to densely packed integrated circuit devices.

It is another object of the present invention to provide a method for making low-ohmic interconnections on an integrated circuit device having just one metallization layer.

This invention concerns a scheme that allows to provide low-ohmic interconnections on an integrated circuit device.

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Reiner: Overview

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 March 2003 (06.03.2003)

PCT

(51) International Patent Classification: H01L 23/60

(21) International Application Number: PCT/IB02/03410

(22) International Filing Date: 21 August 2002 (21.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
01120555.6 29 August 2001 (29.08.2001) EP

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: REINER, Joachim, C.; Prof., Holstlaan 6, NL-5656 AA Eindhoven (NL); RZITTKA, Eckart; Prof.

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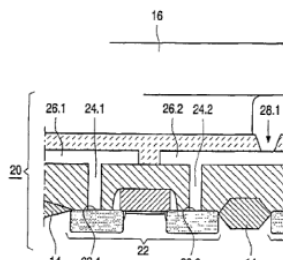
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(54) Title: INTEGRATED CIRCUIT DEVICE WITH BUMP BRIDGES



(57) Abstract: Text Integrated circuit device (20) comprising a silicon substrate (20), an isolating layer (24) at least partially covering the integrated device, which establish a conductive path to the contacts (23.1, 23.2) of the integrated circuit device (20). A conductive layer (26.1, 26.2, 26.3, 26.4) is provided which connect to one of the contacts (23.1, 23.2) situated above the isolating layer (24). A passivation layer (27) - situated above the conductive layer (26.1, 26.2, 26.3, 26.4) - provides for a conductive connection between at least two of the metal lines (28.1, 28.2) for partially exposing at least two of the metal lines (28.1, 28.2) situated within the metallization level (25), without making contact to the bridge (29) is supported by the passivation layer (27).

There are many integrated circuit devices that comprise just one metallization layer being patterned to provide for connections between the integrated circuits and to provide for connections to the outside.

The higher the integration density of these integrated circuit devices gets, the more difficult it is to realize the routing of all the necessary interconnections inside a single metallization layer. One of the problems is that one has to avoid crossings where a first metal line crosses a second metal line.

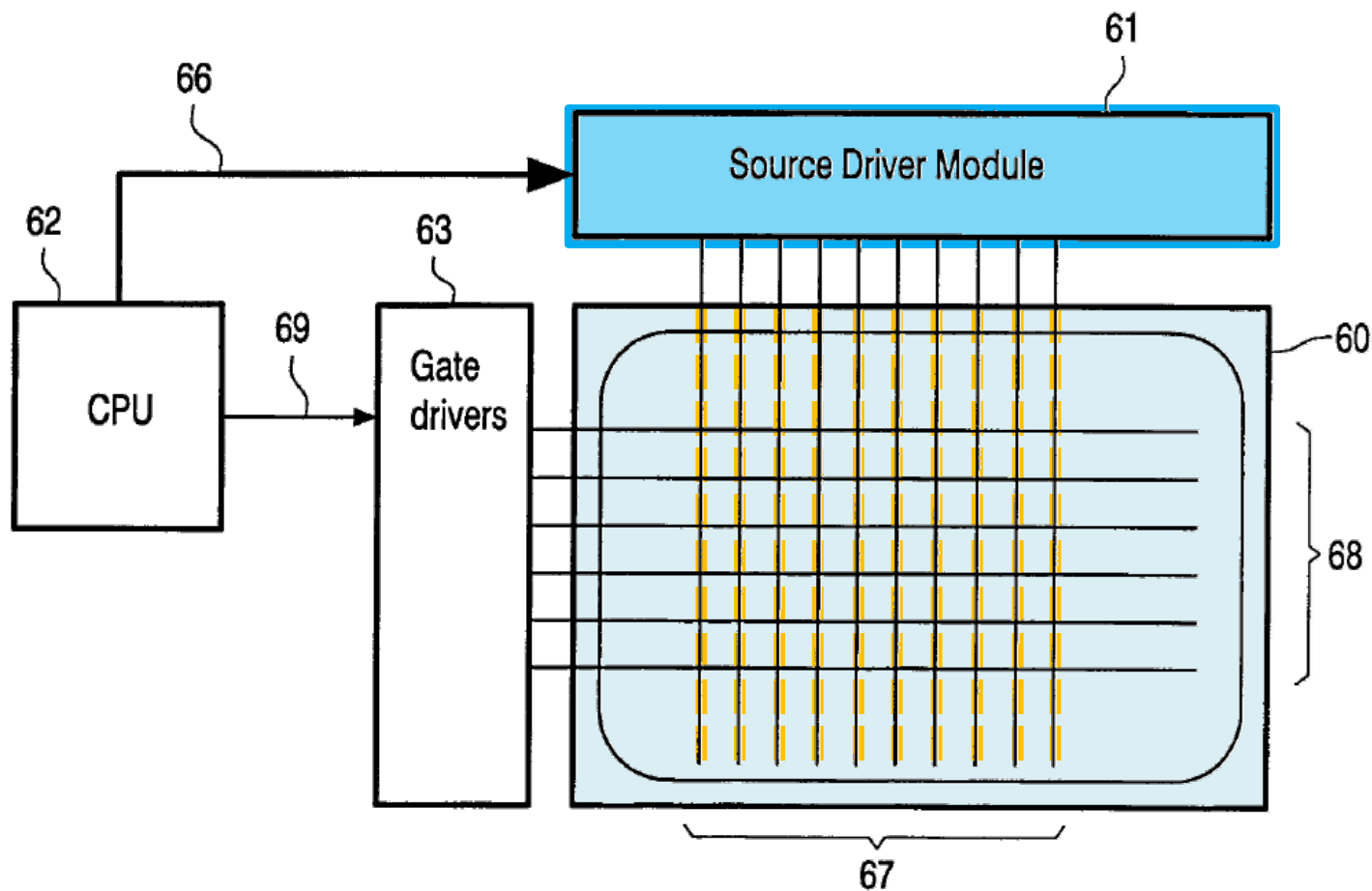
In situations where the routing cannot be realized with a single metallization layer, one currently has two options. Either, a few polysilicon interconnections are provided where necessary, or another metallization layer is added.

It is a disadvantage of the polysilicon interconnections, that due to the fact that the polysilicon has a low conductivity, the dimension of the polysilicon interconnections has to be chosen such that a sufficiently low resistance is obtained. This means that polysilicon interconnections usually are relatively big thus occupying part of the device's surface area that otherwise would be available for integrated devices.

A second metallization layer has the disadvantage that the costs for making such a device are impacted, since a second metallization layer requires additional processing and testing steps. In many cases this would render the integrated circuit device too expensive.

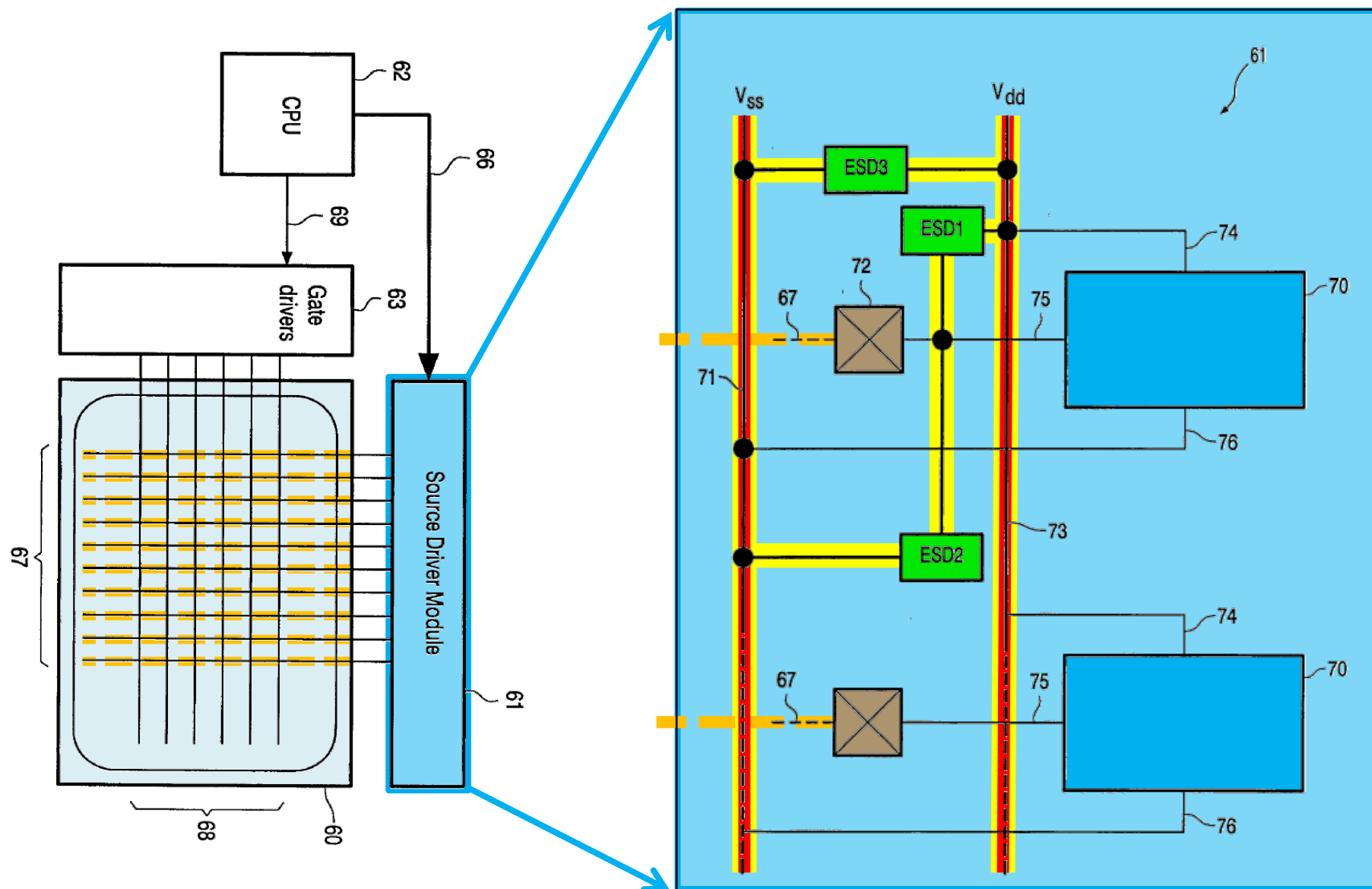
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Reiner: Overview



Ex. 1005 at 9:11-35, Fig. 4; POR at 17-18.

Reiner: Overview



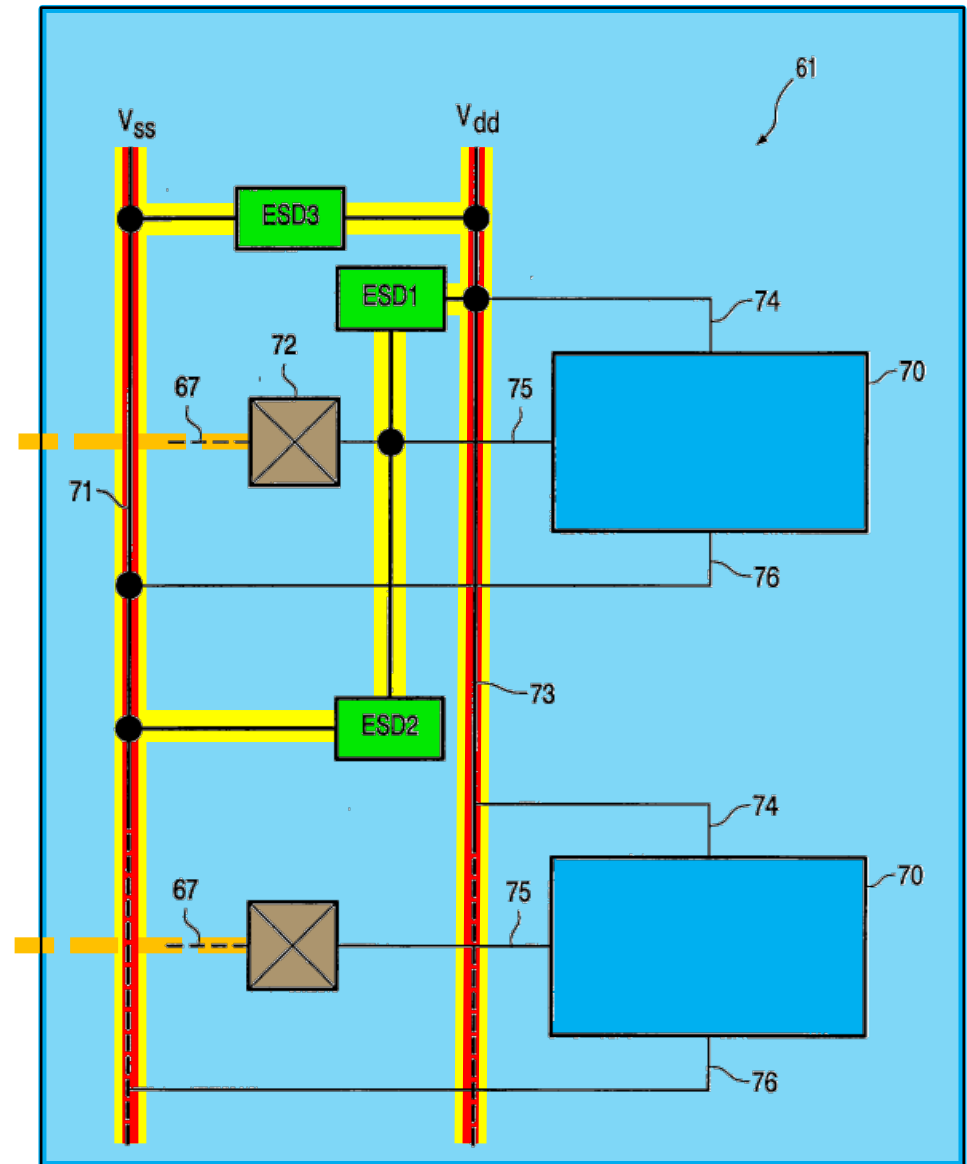
Ex. 1005 at 10:1-24, Figs. 4, 5; POR at 18-20.

Reiner teaches ESD protection *inside* an integrated circuit.

ESD1, ESD2, ESD3:

protection means *inside*
source driver integrated circuit

Dr. Murphy: “the other
components you identified
ESD1, 2, 3, circuit 70, I think is
reasonable to understand those
to be within conceptually the box
labeled source driver module”
(Ex. 2008 at 139:3-10)



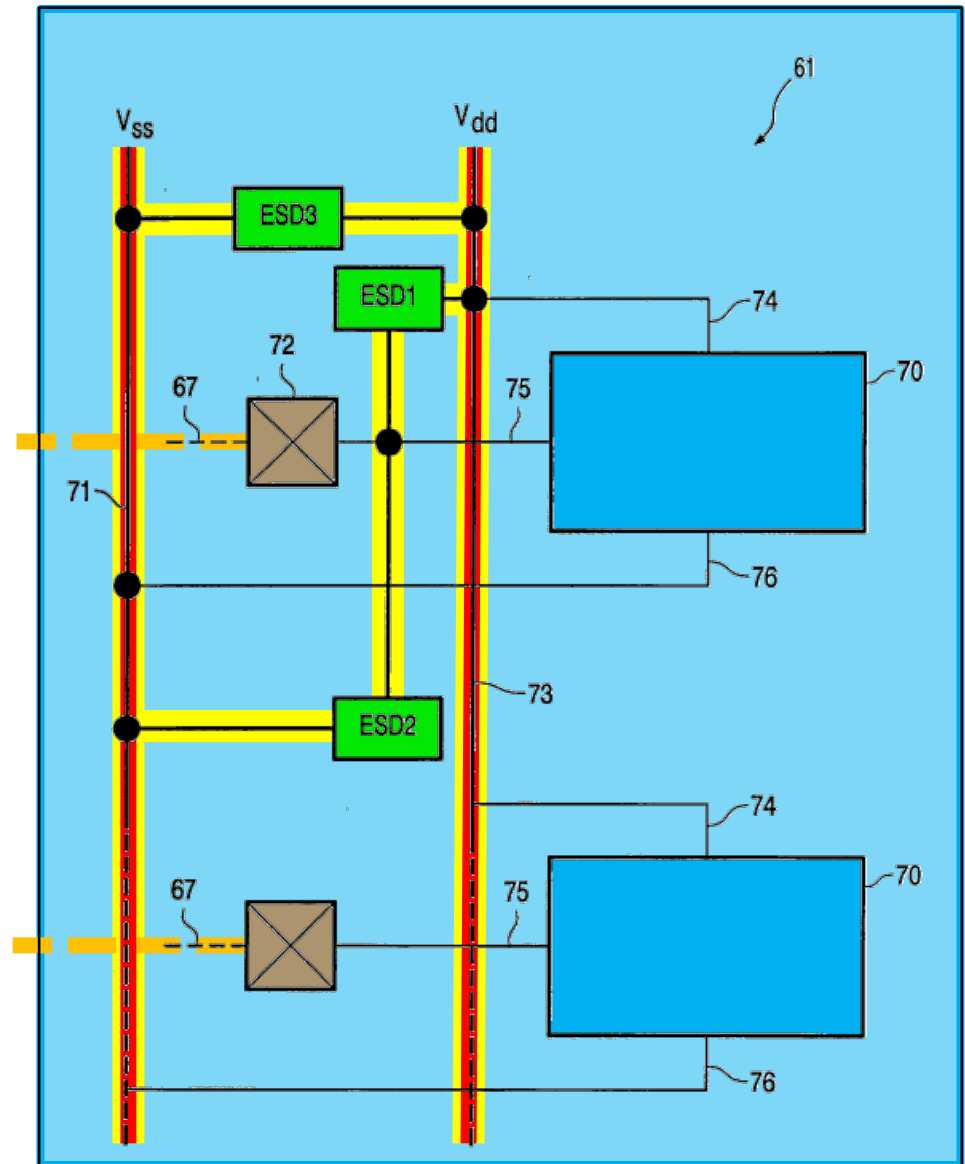
Ex. 1005 at 10:1-24, Fig. 5; POR at 20-21.

Reiner teaches ESD protection *at inputs/outputs*.

ESD1, ESD2, ESD3:

protection means *at inputs/outputs*.

ESD protection networks within IC chips, like source driver 61, “comprise[] protection diodes and/or transistors and metal interconnection lines for connecting these diodes and/or transistors with inputs and/or outputs of the integrated circuit device to be protected.”
(Ex. 1005 at 3:4-8)



Ex. 1005 at 10:1-24, Fig. 5; POR at 20-22.

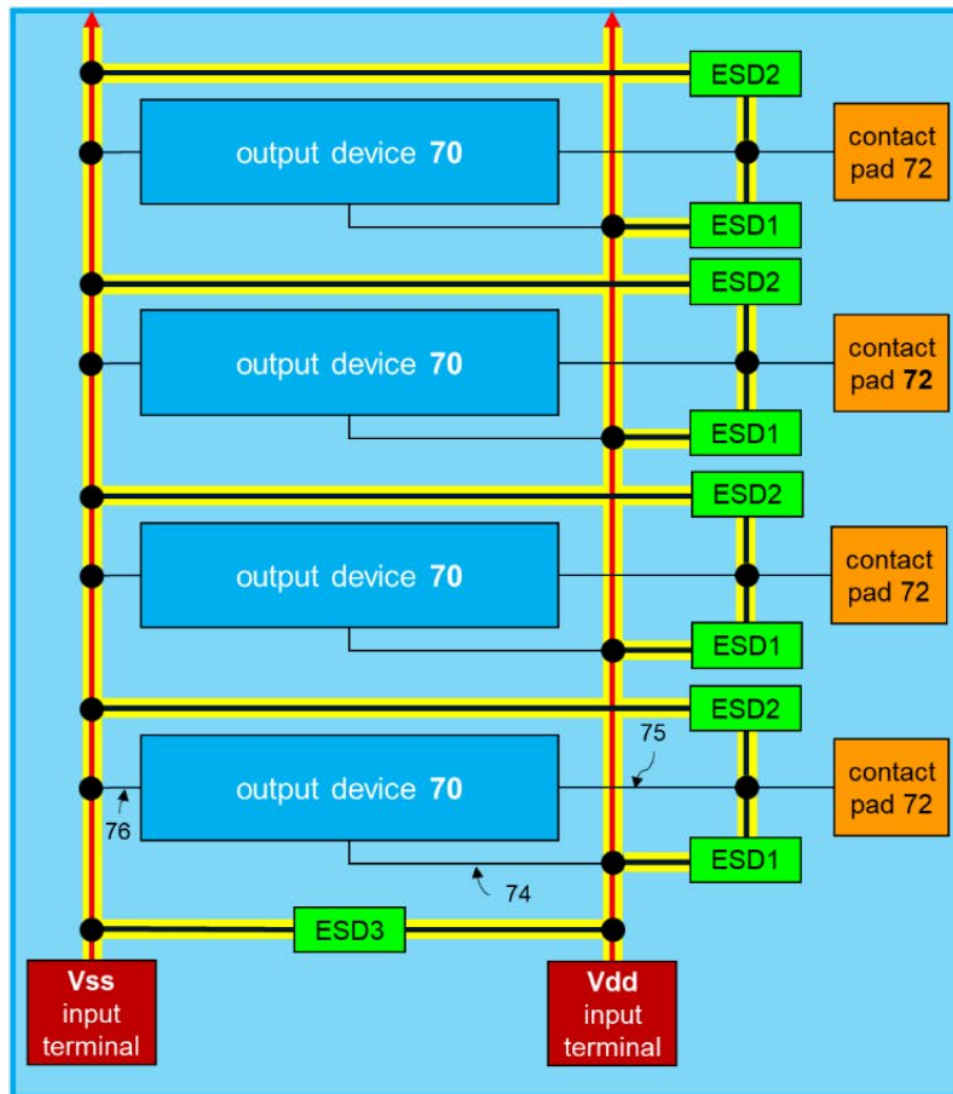
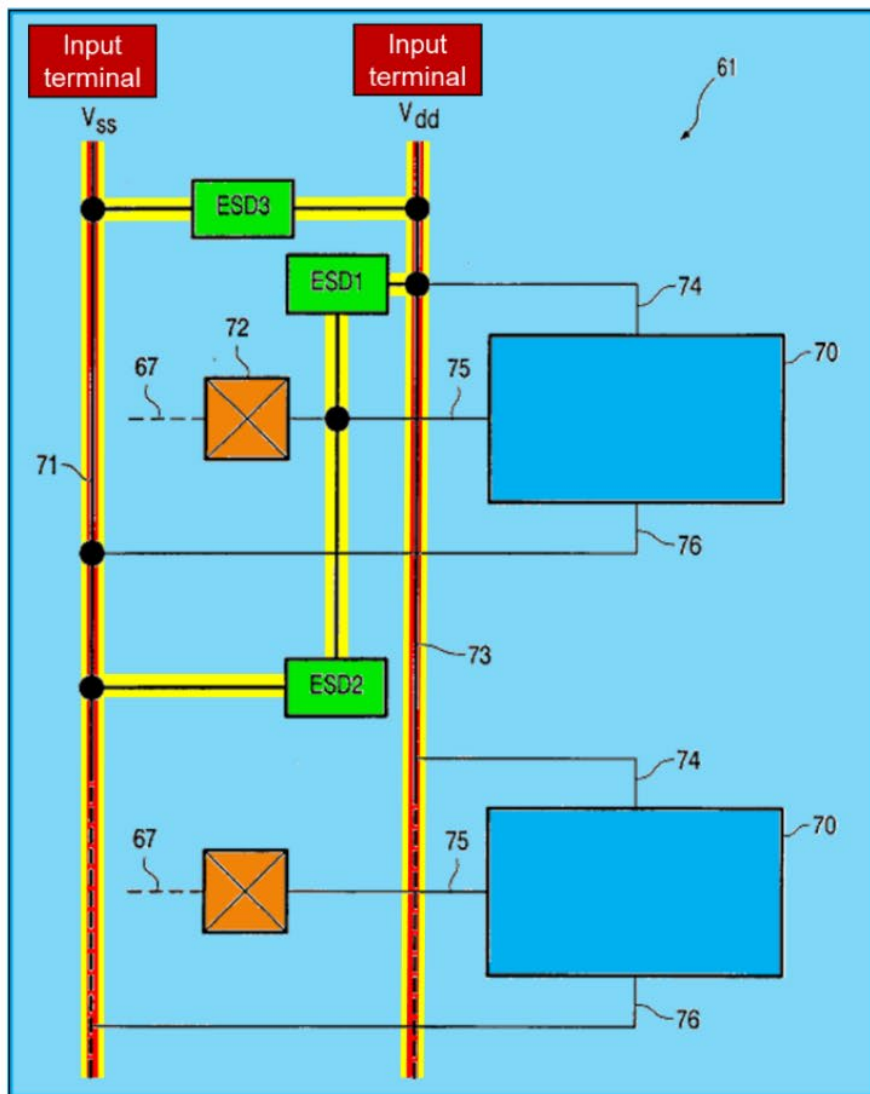
Reiner does not disclose claim 4[f].

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

The claim requires that the scanning line driving circuit is connected to a power supply line **between first and second protective circuits** connected to that power supply line.

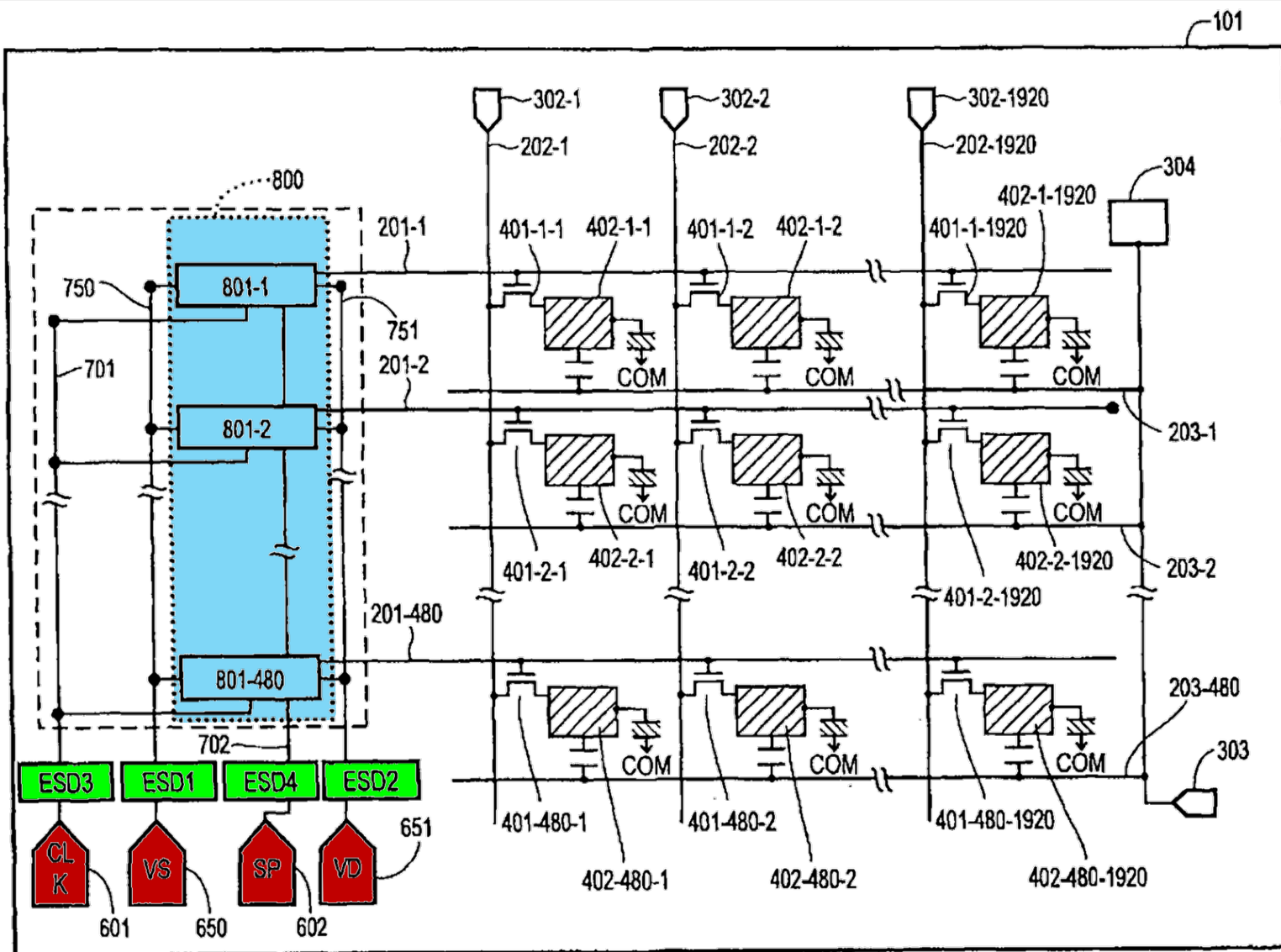
Ex. 1001 at claim 4; POR at 32-42; Sur-Reply at 2-9.

Reiner Fig. 5 Redrawn: ESD at Inputs/Outputs



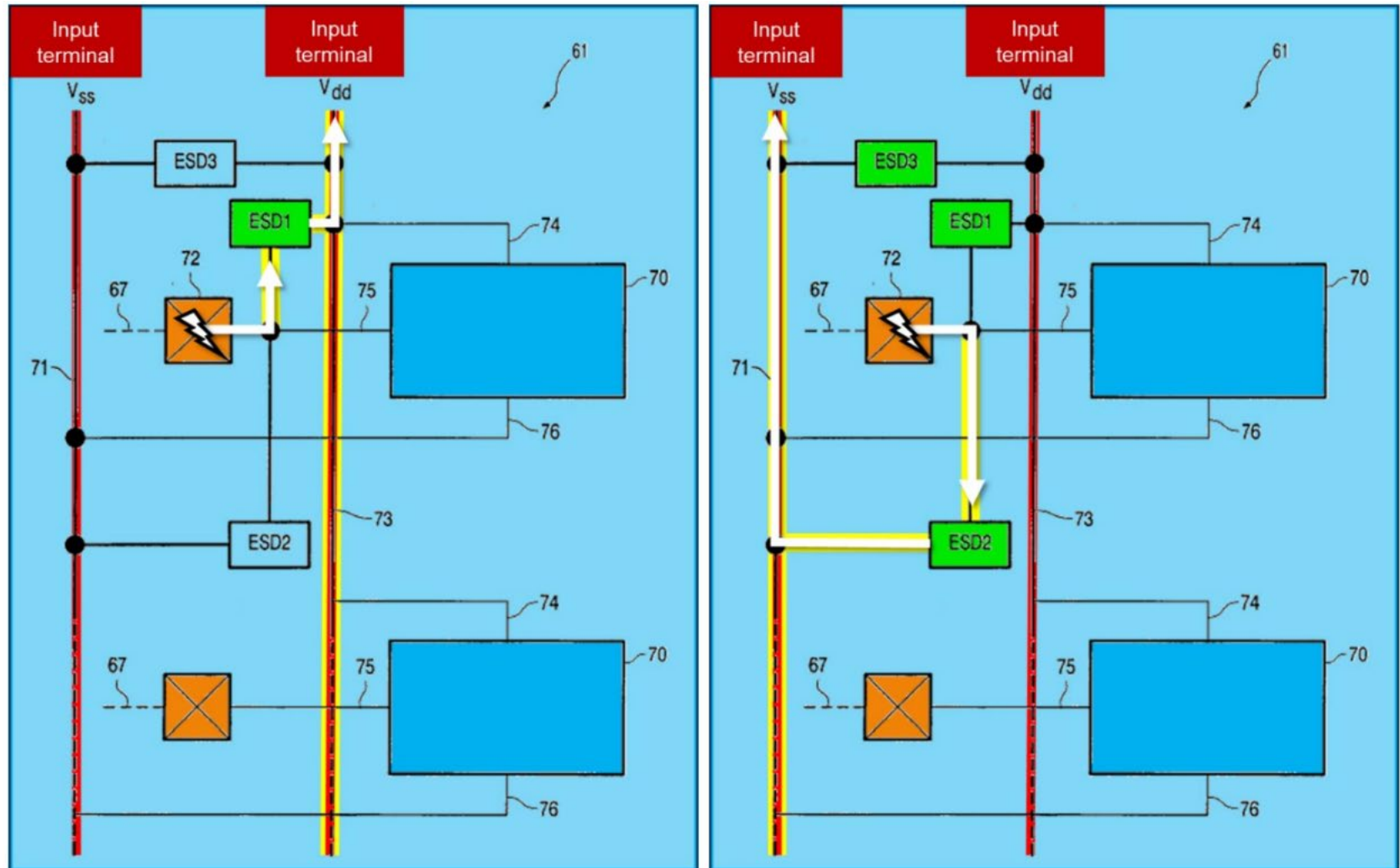
Ex. 1005 at 10:1-24, Fig. 5; POR at 35-36; Sur-Reply at 2-9.

Reiner discloses the arrangement on which the '157 patent improves.



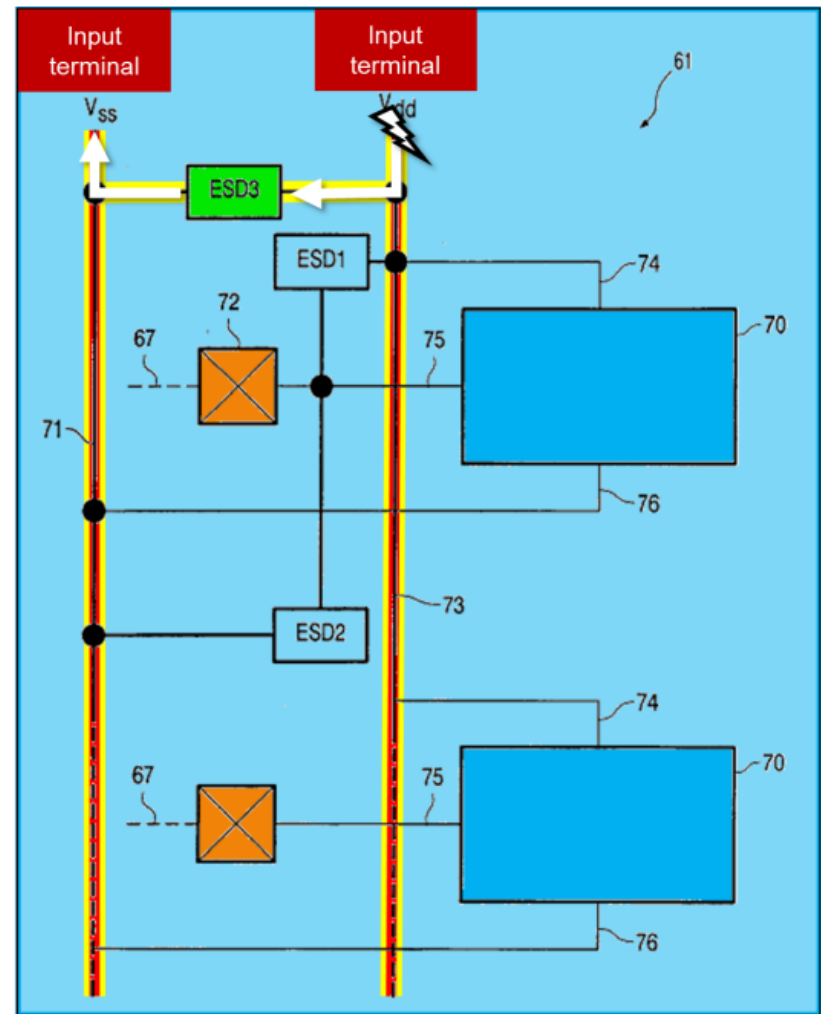
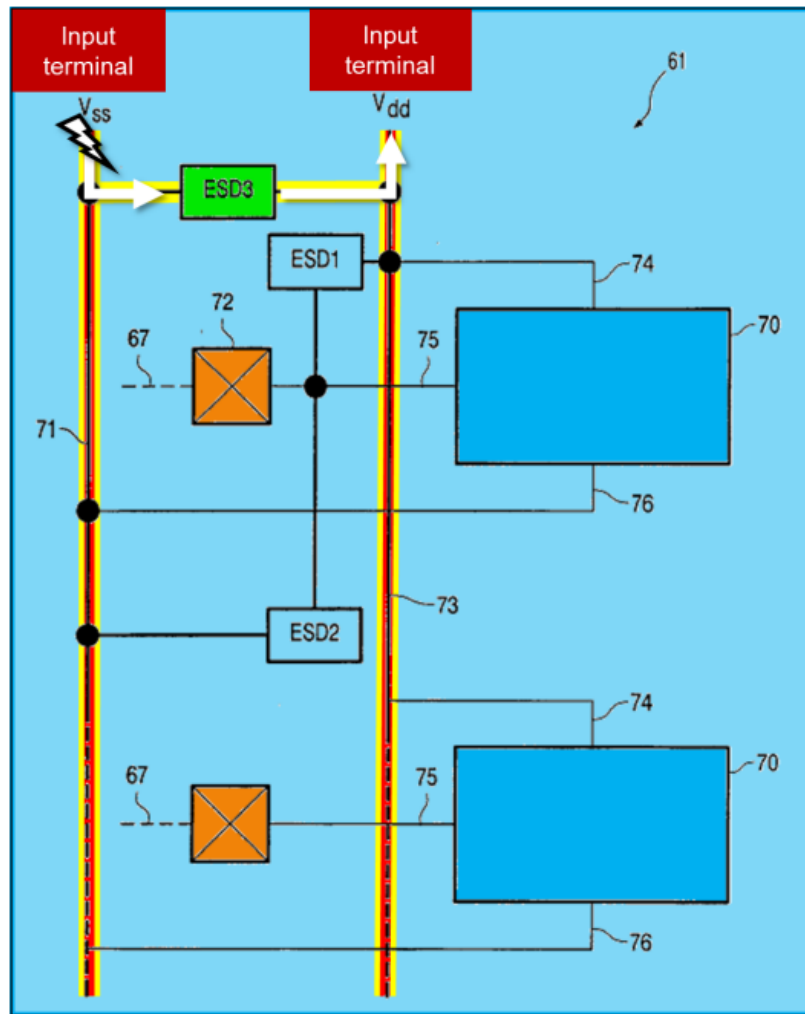
Ex. 1001 at 1:47-54, 2:20-30, Fig. 11; POR at 34-35; Sur-Reply at 4, 7.

Reiner discloses ESD protection *inside* IC and *at* inputs/outputs.



Ex. 1005 at 10:1-24, Fig. 5; POR at 36-38; Sur-Reply at 2-9.

Reiner discloses ESD protection *inside* IC and *at* inputs/outputs.



Ex. 1005 at 10:1-24, Fig. 5; POR at 38-39; Sur-Reply at 2-9.

Petitioner ignores Reiner's disclosure regarding inputs/outputs and low-ohmic paths.

Dr. Murphy:

Whether any particular of these lines is bolded or not really wasn't relevant to my analysis in the context of my invalidity opinions on the '157. So I can't express a strong view as I sit here today as to identifying which of these lines are -- are bold or not.

A At the risk of repeating myself and repeating myself using slightly different words than I used before, the particular individual low ohmic -- excuse me, the particular individual lines that are bolded in Figure 5 was not something that was part of my invalidity analysis of the '157 claims.

Q: Can you identify those lines now?

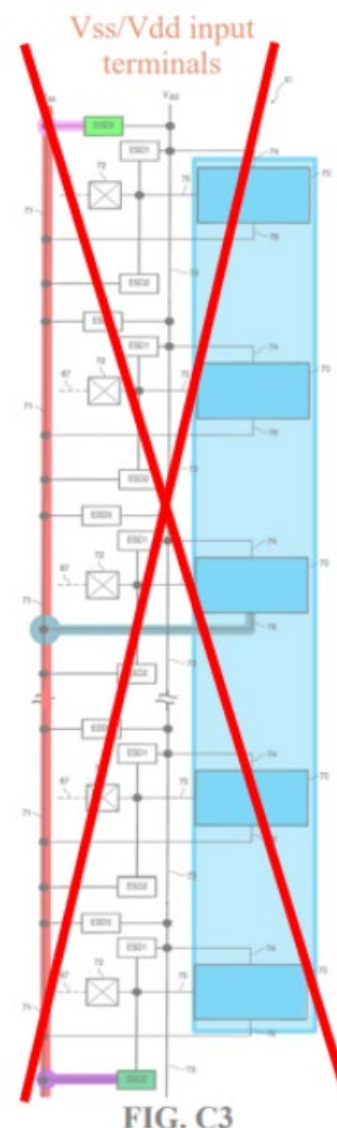
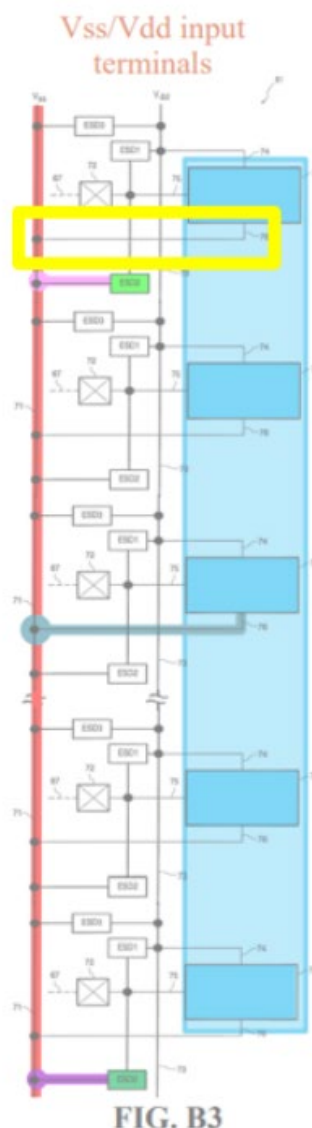
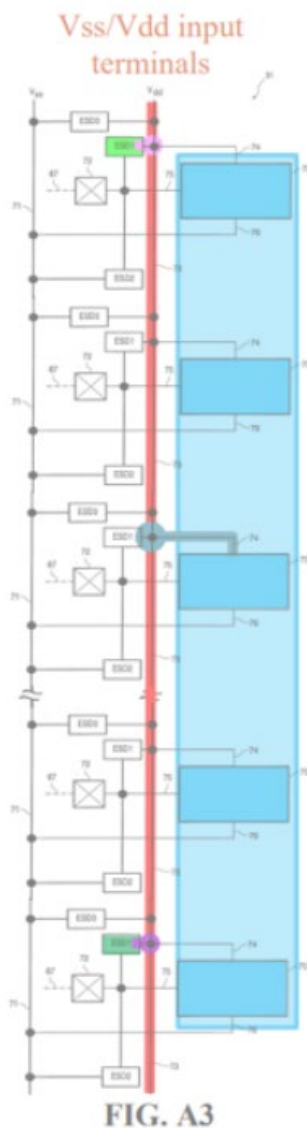
A Again, not an exercise that I thought was relevant to my invalidity analysis of '157. It's not something that I could necessarily do on the spot because it would involve some further analysis of Reiner and study of the Figure 5 as well as the written description.

Ex. 2008 at 119:16-19, 124:15-21, 125:1-6; POR at 40.

Fig. A3: driver 61 connected to line Vdd at ESD1 connecting portions (not between).

Fig. B3: driver 61 connected to line Vss before ESD2 (line 76, yellow box).

Fig. C3: Dr. Murphy does not opine that ESD3 is connected to driver 61. He cannot rely on ESD3.



Reiner does not disclose claim 4[f].

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

The claim requires that the scanning line driving circuit is connected to a power supply line **between first and second protective circuits** connected to that power supply line.

Reiner discloses ESD protection means *inside* source driver integrated circuit and *at inputs/outputs*.

Ex. 1001 at claim 4; POR at 32-42; Sur-Reply at 2-9.

Reiner does not disclose claim 4[e].

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

The claim requires a first protection circuit connected to the power supply line between where the scanning line driving circuit is connected to the power supply line—the **scanning line driving circuit as a whole, not a component of the scanning line driving circuit**—and the input terminal.

Ex. 1001 at claim 4; POR at 27-32; Sur-Reply at 9-17.

Reiner does not disclose claim 4[e].

Claim 4:

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

Claim 10:

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and

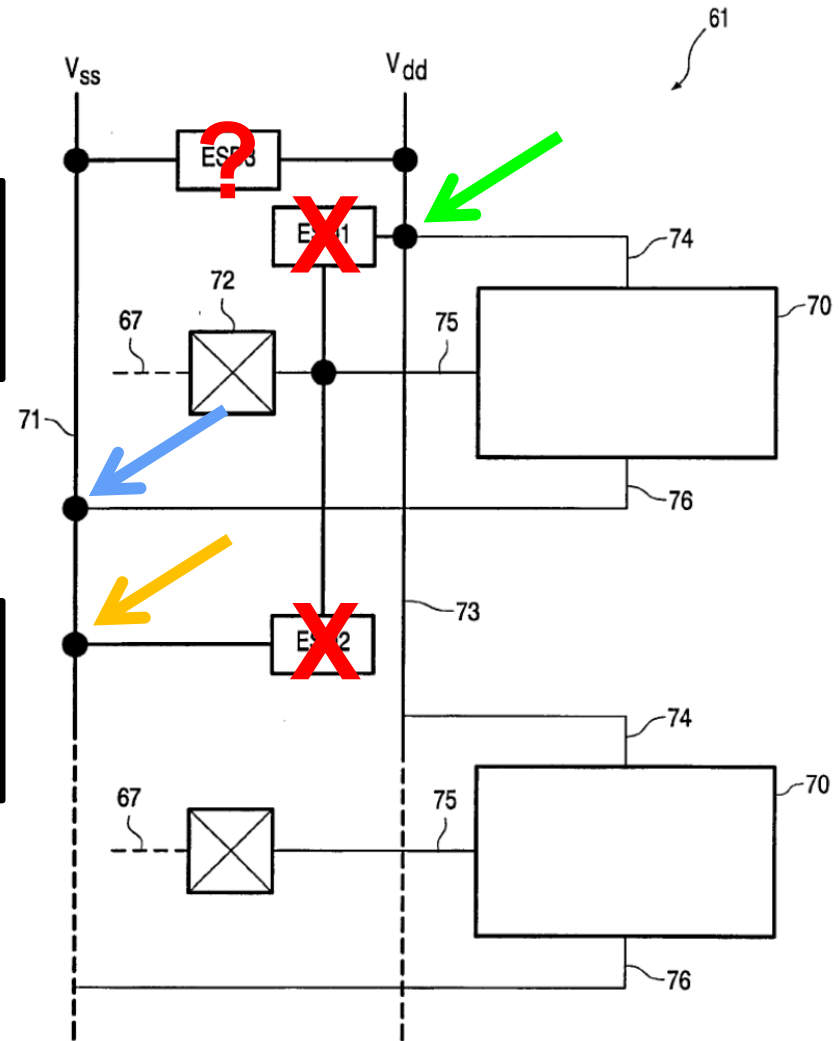


FIG. 5

Ex. 1001 at claim 4, claim 10; Ex. 1005 at Fig. 5; POR at 27-32; Sur-Reply at 14-17.

Reiner does not disclose the claimed scanning line driving circuit arrangement.

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Petitioner handwaves over Reiner's source (data line) driver and its silence regarding a gate (scanning line) driver.

Ex. 1001 at claim 4; POR at 24-26; Sur-Reply at 17-18.

Reiner does not disclose claim 8.

8. The display device as set forth in claim 4, further comprising:
a substrate,
the scanning line driving circuit being arranged on the substrate,
the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,
the first protection circuit being arranged in the first corner portion of the substrate, and
the second protection circuit being arranged in the second corner portion of the substrate.

Claim 8 recites the scanning line driving circuit being arranged on the substrate.

Reiner does not disclose the claimed substrate.

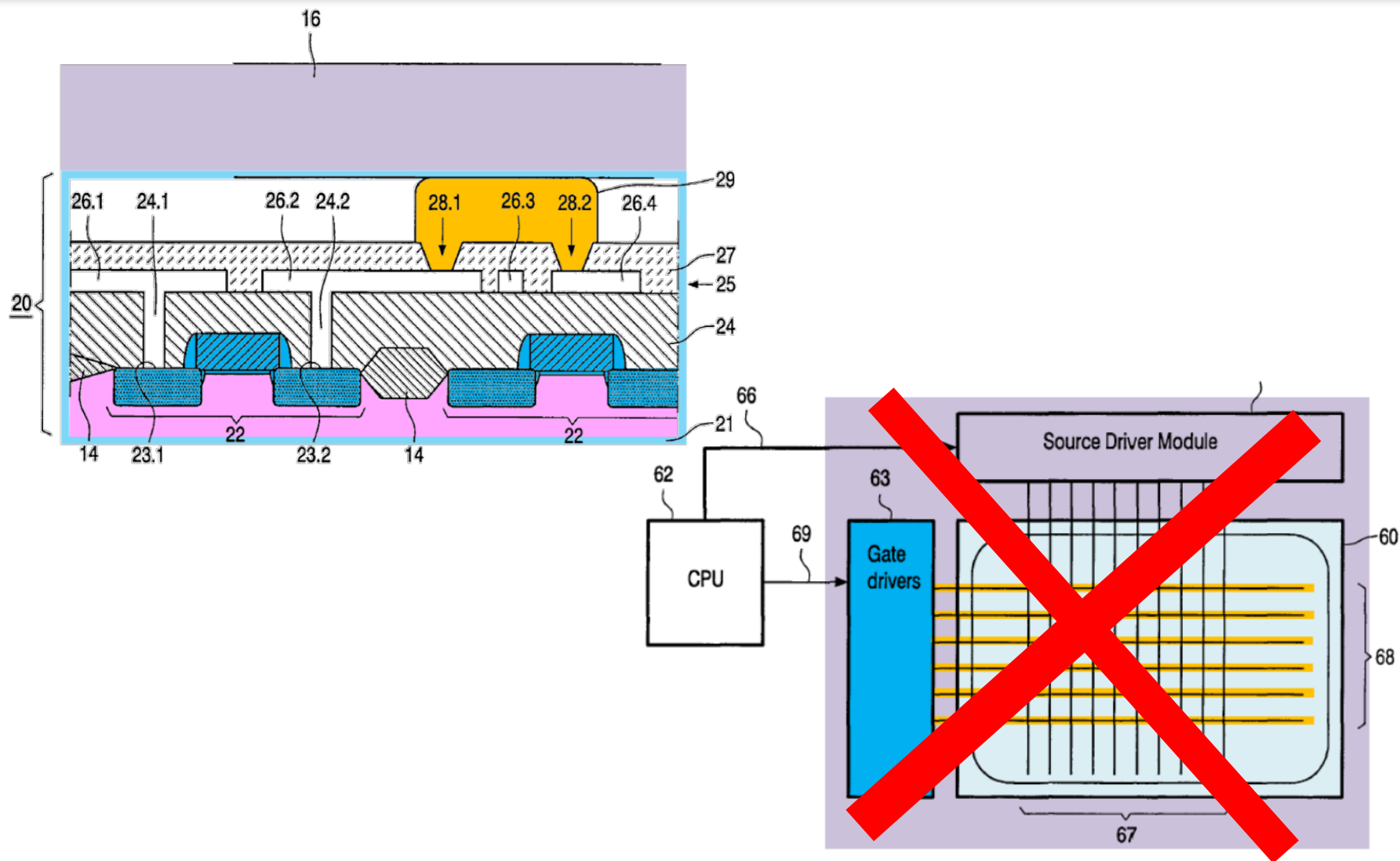


FIG. 4

Ex. 1005 at Figs. 2, 4; POR at 43-47; Pet. at 46.

**Ground 2: Reiner in view of
Takahara does not render
obvious any challenged claim.**

Reiner + Takahara does not render obvious any challenged claim.

4. A display device, comprising:
a scanning line driving circuit;
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
an input terminal connected to the power supply line to supply power; and
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Ex. 1001 at claim 4; POR at 58-68.

Takahara: Overview

(19) Japan Patent Office (JP)

(12) Published Unexamined Patent Application (A)

(11) Publication No. of Unexamined Application: **Kokai No. 2003-121875 (P2003-121875A)**
 (43) Date of Publication of Unexamined Application: **April 23, 2003 (2003.4.23)**

(51) Int. Cl. ⁷	ID	FI	Theme Code (Refer
G02F 1/1368		G02F 1/1368	2F
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Request for Examination: Not requested
 Number of Claims: 14
 Method of Filing: OL (Online)
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Continued on last

(21) Patent Application No.: 2001-311846 (P2001-311846)	(71) Applicant: 000002369 SEIKO EPSON CORPORATION 2-chome 4-ban 1-go Nishishinjuku, Shing ku, Tokyo-to
(22) Filing Date: October 9, 2001 (2001.10.9)	(72) Inventor: Kenichi TAKAHARA c/o SEIKO EPSON CORPORATION 3-chome 3-ban 5-go Owa, Suwa City, Na
	(74) Agent: 100095728 Patent Attorney Masataka KAMIYANAC (and 2 others)

Continued on las

(54) Title of Invention

MANUFACTURING METHOD FOR ELEMENT-SUBSTRATE DEVICE AND
 MANUFACTURING METHOD FOR ELECTRO-OPTICAL DEVICE, AND RETICLE

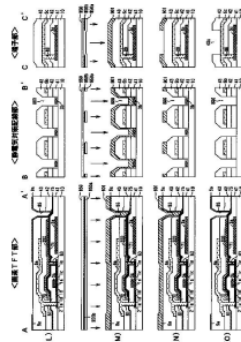
(57) Abstract

Problem

To make it possible to effectively carry out antistatic measures by forming short-circuit wiring and to effectively carry out the cutting thereof in the manufacturing of an element-substrate device.

Solution

A reticle (950), which has one light transmittance at a location opposing a cutting hole (880) formed in interlayer-insulating films (41-43) on a short-circuit wiring (3b) and has another light transmittance that is lower than the one light transmittance at a location not opposing the cutting hole, is used to cut the short-circuit wiring according to the present invention



To make it possible to effectively carry out antistatic measures by forming short-circuit wiring and to effectively carry out the cutting thereof in the manufacturing of an element-substrate device.

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[0004]

Accordingly, a process in which the scan lines or the data lines are formed is conventionally performed in combination with forming short-circuit wirings, which electrically connect the scan lines or the data lines, respectively. If this short-circuit wiring is formed, then the electric charge or the static electricity that has accumulated on the surface of the insulating substrate is diffused toward an outer perimeter of the substrate via said short-circuit wiring, and therefore sudden excessive electric current no longer flows through the other circuit elements or the like, such as the TFTs, via the scan lines or the data lines, and an electrostatic breakdown of said circuit elements or the like can be prevented before it happens.

Takahara: Overview

(19) Japan Patent Office (JP)

(12) Published Unexamined Patent Application (A)

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G03F	1/08	G03F	1/08
	7/20		L
			7/20

Request for Examination: Not requested
Number of Claims: 14
Method of Filing: OL (Online)
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(71) Applicant: 000002369
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ku, Tokyo-to

(72) Inventor: Kenichi TAKAHARA
c/o SEIKO EPSON CORPORATION
3-chome 3-ban 5-go Owa, Suwa City, Na

(74) Agent: 100095728
Patent Attorney Masataka KAMIYANAC
(and 2 others)

Continued on last page

(54) Title of Invention

MANUFACTURING METHOD FOR ELEMENT-SUBSTRATE DEVICE AND
MANUFACTURING METHOD FOR ELECTRO-OPTICAL DEVICE, AND RETICLE

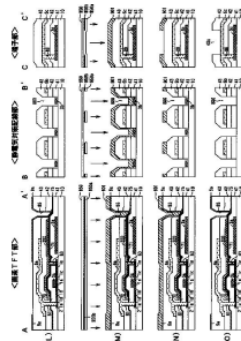
(57) Abstract

Problem

To make it possible to effectively carry out antistatic measures by forming short-circuit wiring and to effectively carry out the cutting thereof in the manufacturing of an element-substrate device.

Solution

A reticle (950), which has one light transmittance at a location opposing a cutting hole (880) formed in interlayer-insulating films (41-43) on a short-circuit wiring (3b) and has another light transmittance that is lower than the one light transmittance at a location not opposing the cutting hole, is used to cut the short-circuit wiring according to the present invention



[0005]

However, because the short-circuit wiring described above must be cut prior to completing the manufacturing process for the electro-optical device to allow normal operation of aforesaid electro-optical device, the applicant of the present application proposes a method of forming cutting holes on the short-circuit wiring in combination with an intermediate process thereof, and cutting prescribed locations of the short-circuit wiring via these cutting holes to separate the short-circuit wiring and the scan lines or the data lines (see Japanese Laid-open Examined Patent Publication H8-14667).

Takahara: Overview

(19) Japan Patent Office (JP)

(12) Published Unexamined Patent Application (A)

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 ku, Tokyo-to
 (72) Inventor: Kenichi TAKAHARA
 c/o SEIKO EPSON CORPORATION
 3-chome 3-ban 5-go Owa, Suwa City, Na
 (74) Agent: 100095728
 Patent Attorney Masataka KAMIYANAC
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Continued on las

(54) Title of Invention

MANUFACTURING METHOD FOR ELEMENT-SUBSTRATE DEVICE AND
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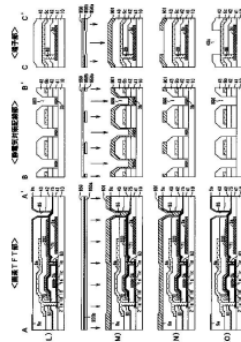
(57) Abstract

Problem

To make it possible to effectively carry out antistatic measures by forming short-circuit wiring and to effectively carry out the cutting thereof in the manufacturing of an element-substrate device.

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A reticle (950), which has one light transmittance at a location opposing a cutting hole (880) formed in interlayer-insulating films (41-43) on a short-circuit wiring (3b) and has another light transmittance that is lower than the one light transmittance at a location not opposing the cutting hole, is used to cut the short-circuit wiring according to the present invention



[0021]

According to this aspect, given that the wirings include **scan lines**, electrically connecting by way of the short-circuit wiring includes at least said scan lines. Accordingly, according to the present aspect, it becomes possible to prevent electrostatic breakdown of the thin-film transistor due to the static electricity that passes through the scan lines.

[0022]

In another aspect of the element-substrate device of the present invention, the wirings include a data line.

[0023]

According to this aspect, given that the wirings include **data lines**, electrically connecting by way of the short-circuit wiring includes at least said data lines. Accordingly, according to the present aspect, it becomes possible to prevent electrostatic breakdown of the thin-film transistor due to the static electricity that passes through the data lines.

[0024]

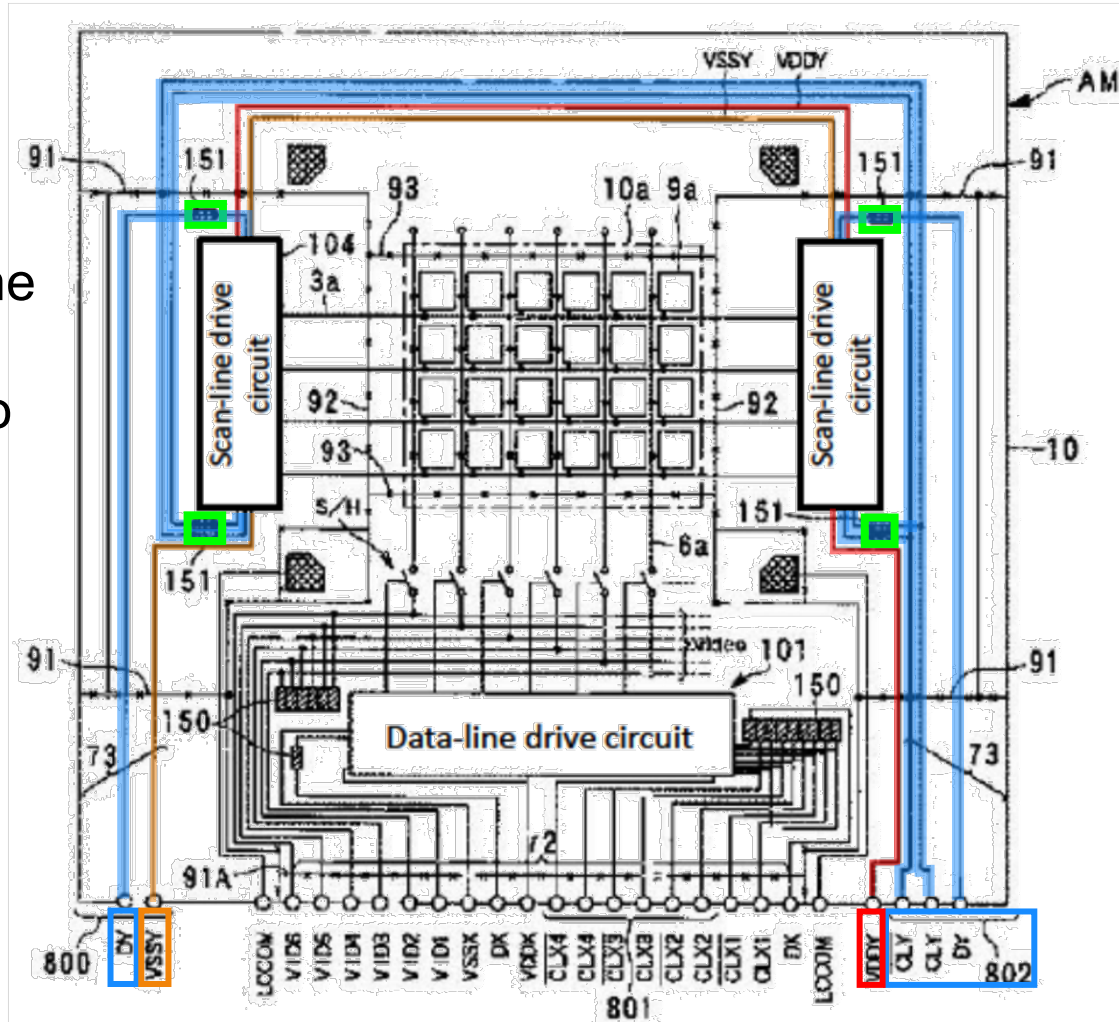
Especially in such an aspect in which the wirings include the scan lines or the data lines, in particular, the wirings may include **signal wirings** that supply a signal for driving at least one of a scan-line drive circuit connected to the scan lines and a data-line drive circuit connected to the data line.

[0025]

According to this kind of configuration, the signal wirings, which supply the signals for driving the scan-line drive circuits or the data-line drive circuit, which generally include the thin-film transistor, such as a CMOS type, other circuit elements, are electrically connected by the short-circuit wiring. Accordingly, according to the present aspect, the possibility of a defect arising, such as an electrostatic breakdown, can be reduced in said scan-line drive circuits and said data-line drive circuit as well, and thereby an even more reliable element-substrate device can be manufactured.

Takahara does not disclose protection circuits connected to power supply lines.

1. Signal line $\neq$ power supply line
2. No signal line is connected to more than one protection circuit 151



Ex. 1007 at Fig.1; POR at 55-64.

Takahara does not disclose protection circuits connected to power supply lines.

FIG. 1

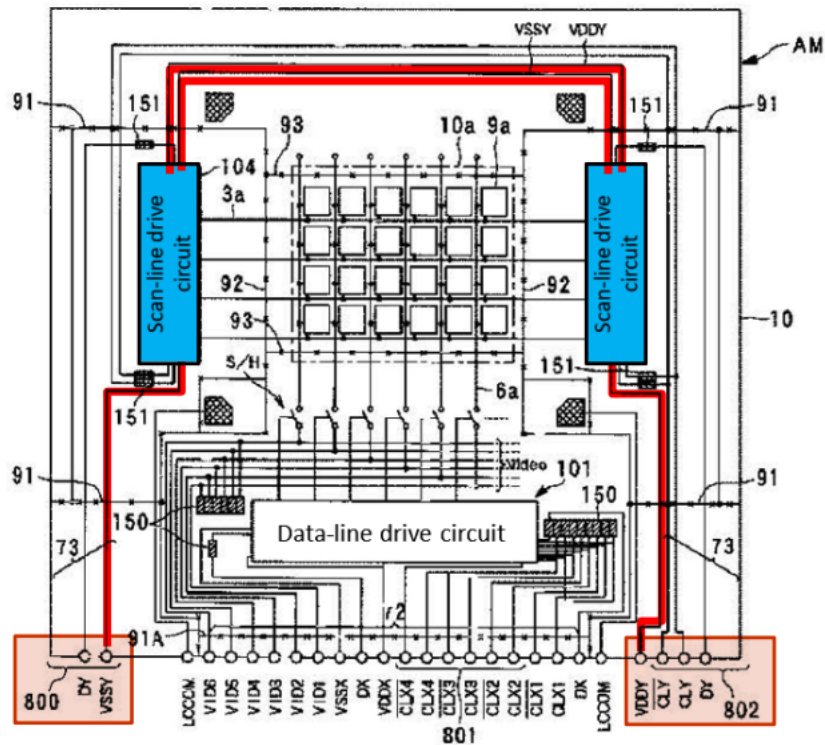
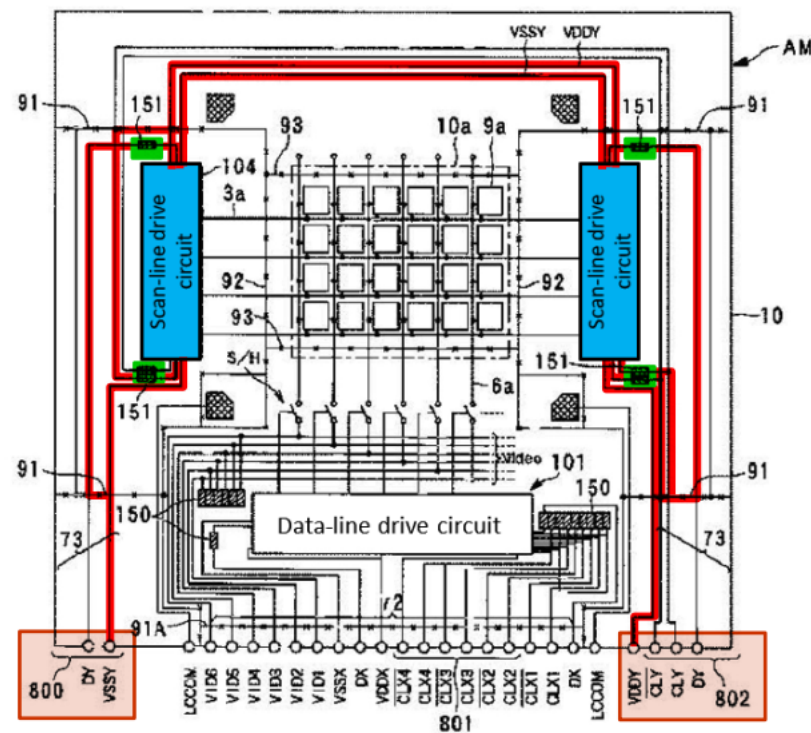
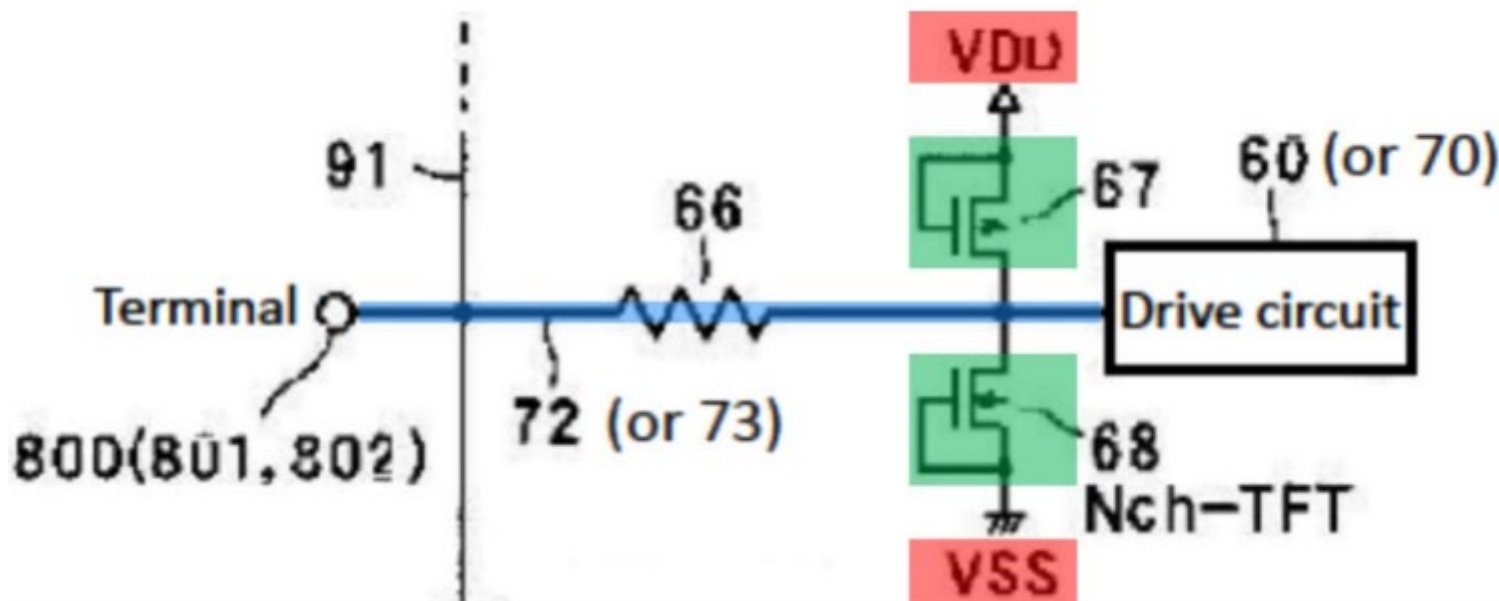


FIG. 1



Ex. 1007 at Fig.1; Pet. at 73, 77.

Takahara does not disclose protection circuits connected to power supply lines.



Ex. 1007 at Fig.3; POR at 65-68.

No Motivation To Combine

Reiner provides an ESD protection network internal to and presumably sufficient for an integrated circuit. Petitioner cannot show that a POSITA would have been motivated to change that protection network in view of Takahara.

A POSITA would have no reason to modify *Reiner* in view of *Takahara*.

Reiner provides an ESD protection network for silicon integrated circuits.

§ VI.A.1-2, *supra*; Ex. 2009 ¶139. *Takahara* provides protection circuits for signal lines and a short-circuit wiring to protect its panel. The Petition cites no need to combine the teachings of *Reiner* and *Takahara*.

Petitioner cannot meet its burden.

- **Reiner** discloses an ESD protection network internal to an integrated circuit.
- **Takahara** discloses signal lines (not power supply lines) connected to only one, not two, protection circuit.
- Neither reference, alone or in combination, renders obvious the invention: a scanning line driving circuit connected to a power supply line between two protection circuits connected to that line.

See generally POR.

Thank you