

# Petitioner's Demonstratives

**BOE Technology Group Co., Ltd.**  
**v.**  
**138 East LCD Advancements Limited**

**IPR2024-00973**  
**U.S. Patent No. 9,184,157**

**October 8, 2025**

# U.S. Patent No. 9,184,157

## (54) SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND ELECTRONIC APPARATUS

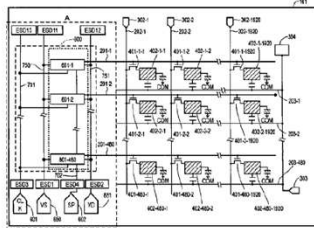


US 9,184,157 B2  
Date of Patent: Nov. 10, 2015

International Search Report  
P011, 27/0251; G02F 1/136204  
361/56, 111  
for complete search history.

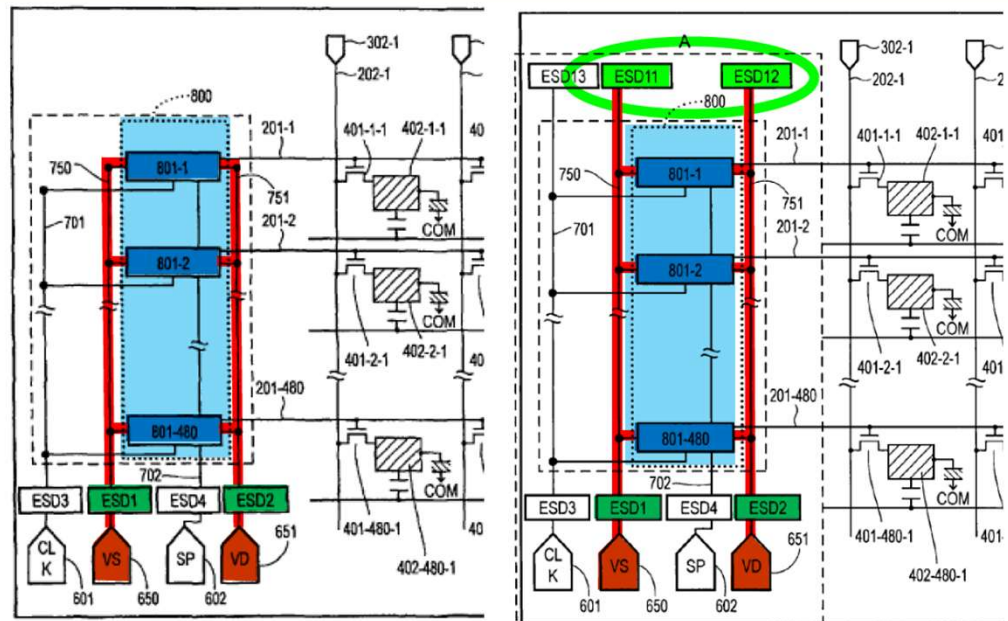
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CPC: H01L 27/0251 (2013.01); G02F 1/136204 (2013.01); G09G 3/3208 (2013.01); G09G 3/39 (2013.01); H01L 27/1214 (2013.01); G09G 2300/043 (2013.01); G09G 2300/0812 (2013.01); H01L 27/12 (2013.01)
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- (57) ABSTRACT  
To prevent an electrostatic damage on a display device formed with driving circuit. Protective circuits are provided not only at input terminal parts, but also at intermediate parts of a circuit or at the ends of wiring lines. Otherwise, the protective circuits are provided at the end of the wiring lines and at the places immediately before and after the input terminals, respectively, and then the circuit is interposed therebetween. Further, the protective circuits are provided around a circuit with a large current consumption.

18 Claims, 8 Drawing Sheets



Page 1 of 18

BOE Tech. Group Exhibit 1001



Id., FIG. 11 (excerpted)

Id., FIG. 1 (excerpted)

(admitted prior art)

Petition 12 (annotating Ex. 1001, FIGS. 1, 11)

See, e.g., Petition 12

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

## Independent claim 4; Dependent claim 8

4. A display device, comprising:  
a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and  
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

8. The display device as set forth in claim 4, further comprising:  
a substrate,  
the scanning line driving circuit being arranged on the substrate,  
the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,  
the first protection circuit being arranged in the first corner portion of the substrate, and  
the second protection circuit being arranged in the second corner portion of the substrate.

*See, e.g., Ex. 1001, claim 4*

## Grounds of unpatentability

| Ground | Claims | Basis | Prior Art                  |
|--------|--------|-------|----------------------------|
| 1      | 1-18   | § 103 | <i>Reiner</i>              |
| 2      | 1-18   | § 103 | <i>Reiner and Takahara</i> |

*See, e.g.,* Petition 1, Pet'r Reply 1-2, 26-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

# Issues in Dispute

- **Claim 4:**

- **Input Terminal Limitation [4c]:**

- “an input terminal connected to the power supply line to supply power” ([4c])

- **Scanning Line Driver Circuit Protection Limitations: [4d]-[4f]:**

- “a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit” ([4d])
    - “the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal” ([4e])
    - “the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected” ([4f])

- **Claim 8:**

- **Substrate Limitations:**

- “a substrate” and “the scanning line driving circuit being arranged on the substrate”

*See, e.g., Patent Owner's Response 22-73*

# Ground 1: *Reiner*

# Prior art: *Reiner* – ESD protection for driver circuits

Quite often integrated circuit devices, such as CMOS devices for example, comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event. This might happen for example when somebody induces a voltage peak into the circuitry by touching the pins of the chip.

*Reiner*, 2:28-3:1

include bipolar transistors or DMOS/VDMOS transistors as well. Accordingly, the invention is applicable to CMOS and BICMOS integrated circuit devices in general.

*Reiner*, 6:16-17

The present invention is well suited for use in integrated circuit devices, such as CMOS devices for example, that comprise an electrostatic discharge device (ESD) protection. Part of an integrated circuit device 30 with a ESD output protection means is

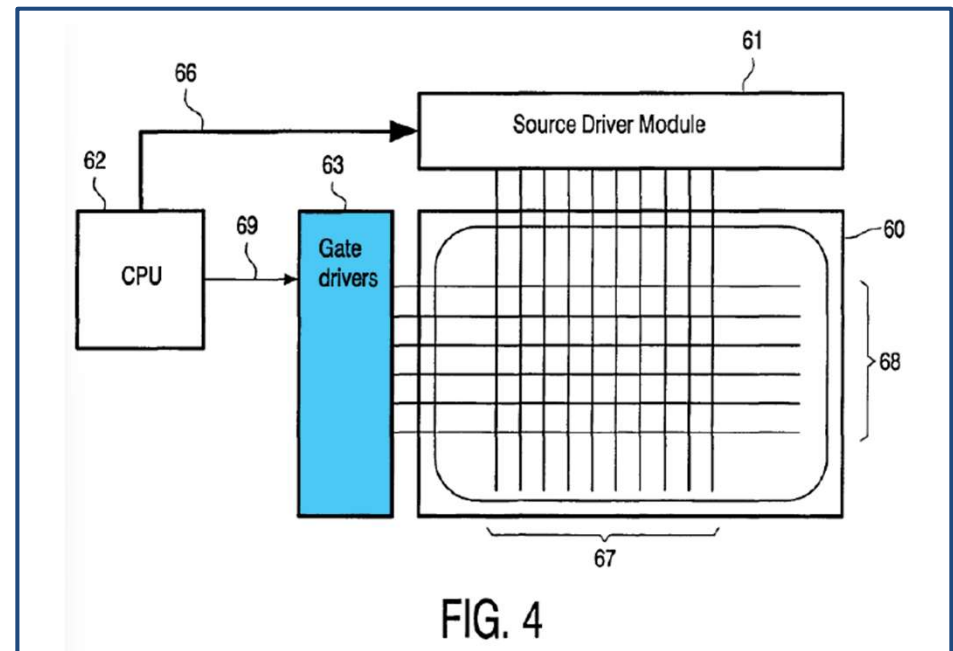
*Reiner*, 8:8-10

Integrated circuit devices quite often have areas where the output or input metal lines have to cross power supply lines. A typical example is an integrated circuit display driver 61 or 63 that is designed to drive many lines of an LCD display 60, as illustrated in Fig. 4. Such a display driver 61, 63 typically has a large number of parallel outputs. In order to keep the cost for making such display drivers in an affordable range, one

*Reiner*, 9:11-15

Before addressing details of a display driver 61 in accordance with the present invention, a brief description of Fig. 4 is given. This Fig. shows a schematic block diagram of an LCD display with control circuitry. The LCD display comprises an LCD screen 60 with a plurality of source lines 67 and a plurality of gate lines 68. A source driver module 61 is employed to drive the individual source lines 67. A gate driver 63 is employed that usually drives one whole gate line 68. The CPU 62 controls the scanning of all the gate lines 68 and source lines 67. For this purpose, the CPU 62 provides video signals (data signals and control

*Reiner*, 9:23-29



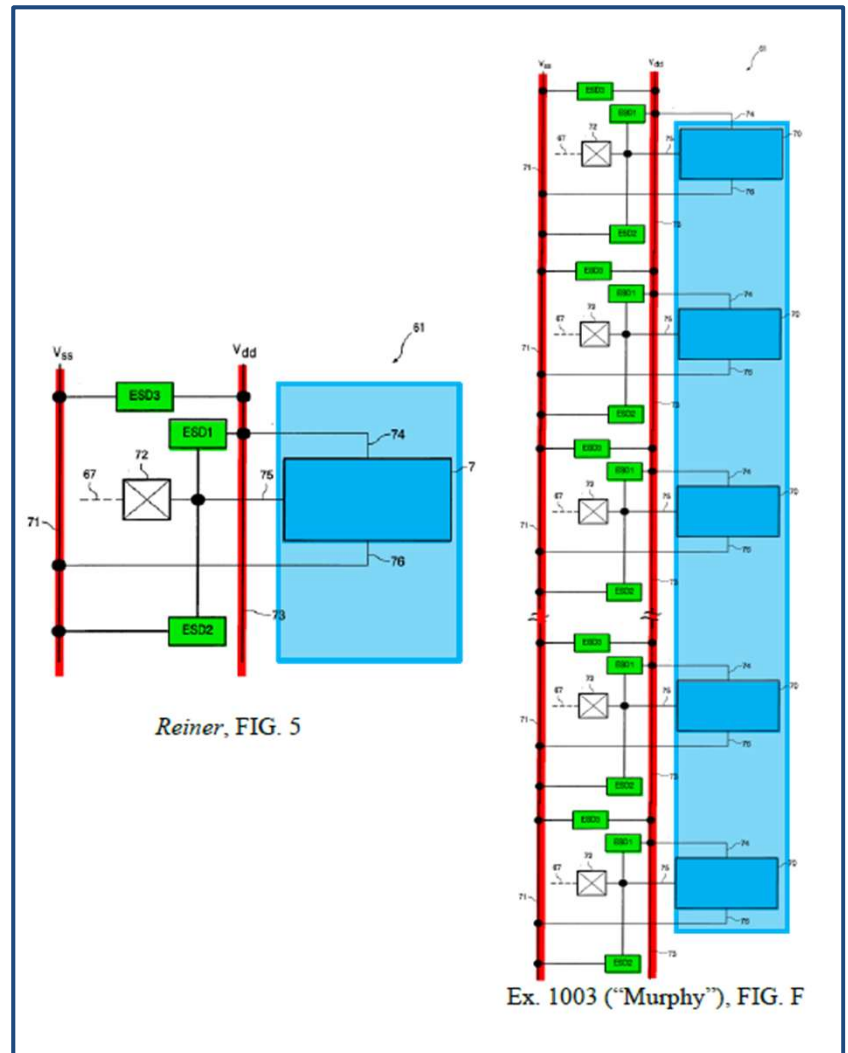
*Reiner*, FIG. 4

See, e.g., Petition 8-10

# Prior art: *Reiner* – Arrangement of ESD protection

Each output device 70 of a source driver module 61, for example, may comprise a digital-to-analog (D/A) converter, a buffer as well as other devices. The buffers drive the source lines 67 with the voltages needed by each pixel of the LCD screen 60. The source lines 67 are connected (e.g. by means of bonding) to contact pads 72, as illustrated in Fig. 5. There is an array of several parallel output devices 70 (two such output devices are shown in Fig. 5). The output 75 of each output device 70 is connected to a contact pad 72. There is a power supply line 73 which provides the supply voltage  $V_{dd}$  through connection 74 to the output devices 70. There is at least a second power supply line 71 which provides the supply voltage  $V_{ss}$  through connection 76 to the output devices 70. These power supply lines 71 and 73 run perpendicular to the output lines 75 of the output devices 70. In the present embodiment, three ESD devices ESD1, ESD2, and ESD3 are provided for each output device 70, in order to protect the circuitry inside the devices 70. A first ESD device ESD1 is connected between the output line 75 and the power supply line 73. The second ESD device ESD2 is connected between the output line 75 and the power supply line 71. A third ESD device ESD3 is situated between the two power supply lines 71 and 73. The ESD

*Reiner*, 10:1-15



Murphy ¶56, FIG. F (annotating *Reiner*, FIG. 5)

See, e.g., Petition 8-10

## **Input Terminal Limitation:**

**“an input terminal connected to the power supply line to supply power ” [4c]**

# Petitioner's expert explained why including input terminals for Reiner's power lines would have been obvious

97. For at least the reasons explained for [4b], *Reiner* discloses power supply lines for Vdd and Vss that supply power to the integrated circuits 61 (source driver) and 63 (gate driver or scanning line driver circuit). For example, “power supply line 73” “provides the supply voltage Vdd through connection 74 to the output devices 70” of source driver 61, and a POSITA would have understood that this is exemplary and that the disclosure also applies to gate driver 63 (scanning line driving circuit). *Reiner*, 10:7-8 (emphasis added). Similarly, a “second power supply line 71” “provides the supply voltage Vss through connection 76 to the output devices 70.” *Reiner*, 10:8-9 (emphasis added). In my opinion, a POSITA would have also understood that this description is exemplary and also applies to gate driver 63 (scanning line driving circuit), for at least the reasons explained for [4a] and [4b]. *Reiner*, 10:8-9 (emphasis added). A POSITA

Murphy ¶97

*Reiner*, 2:28-3:3, 6:12-17, with Ex. 1001, 1:66-2:4. As such, a POSITA would have recognized that input terminals would have been connected to the power supply lines based on the conventionality in the prior art to use such terminals to power both types of driving circuits, which would not be able to function to control the display matrix without the power lines being powered.

Murphy ¶97

98. In my opinion, a POSITA would have understood that the power supply lines 73 (Vdd) and 71 (Vss) would require input terminals to drive the output devices 70 that form the integrated circuit 20 (which include gate driver 63 and source driver 61) so that power can be provided from the power source to the driver units to drive the LCD display 60.

Murphy ¶98

See, e.g., Petition 21-23

## *Reiner* suggests or renders obvious input terminals for the power lines

9:12-14. A POSITA would have recognized that *Reiner*'s integrated circuits, such as gate driver 63, can be fabricated and then attached to a substrate by being "flipped onto the substrate 16[] according to the well-known flip-chip technology" and therefore there would need to be input terminal power connections to the substrate because the wiring lines for the display 60 often run along the substrate, such as shown in FIG. 1 of *Takahara*. *Reiner*, 7:23-25; *Takahara*, [0063], [0066]. FIG. 1 (power supply lines VSSY, VDDY have input terminals 800, 802 for driving scan-line drive circuit 104); *see also* Ex. 1001, 1:54-56, 2:5-14, FIG. 11 (items 650, 651, 705, 751) (acknowledging that "conventional art" related to protecting driving circuits used input terminals to supply power via power lines). A POSITA would have been motivated to provide input terminals connected to the power supply lines to supply power to *Reiner*'s gate driver 63 to ensure proper electrical connections with the power supply and to facilitate manufacturing to connect the power supply lines supplying the gate driver 63 with the corresponding power source or with the power supply lines of the substrate on which the LCD display is arranged.

Murphy ¶101

*See, e.g.*, Petition 21-23

# Patent Owner incorrectly argues that power lines must power pixels, which are not claimed and were distinguished in prosecution

Thus, even if *Reiner* renders obvious input terminals connected to lines Vdd and Vss, those input terminals would be input terminals for integrated circuit driver 61 (*Reiner* Figs. 4 and 5). The Petition does not assert otherwise. Pet., 21-22. The Petition asserts only that *Reiner* suggests input terminals because a POSITA would have understood that “gate driver 63 or source driver 61 (each an integrated circuit 20)” would require input terminals “to drive” the output devices 70 within each integrated circuit. Pet., 21. Similarly, the Petition asserts that a POSITA would

Patent Owner’s Response 22-23

Nothing in *Reiner* suggests that lines Vss and Vdd also supply power to the LCD display 60. Indeed, a POSITA would understand that LCD display 60 may include separate input terminals for separate power supply lines, because LCD display 60 is formed on a separate substrate. Indeed, Dr. Murphy appears to acknowledge that LCD display 60 and its separate substrate could include separate power supply lines and corresponding input terminals. Ex. 1003 ¶101; Ex. 2009 ¶60.

Patent Owner’s Response 23

Specifically, the pixels of Lee cannot reasonably be considered to correspond to the claimed semiconductor circuit. For example, as described in the present specification, one possibility for the semiconductor circuit is the scanning line driving circuit 800 (see paragraph [0037]). One of ordinary skill in the art would recognize that the pixels of Lee do not correspond to the claimed semiconductor circuit.

Ex. 1002, 182

See, e.g., Patent Owner’s Response 22-23

# **Scanning Line Driver Circuit Protection Limitations:**

## **Motivation to Protect Scanning Line Driving Circuit with ESD Protection ([4d])**

# Reiner discloses or suggests protecting the scanning line driving circuit from ESD damage

Quite often integrated circuit devices, such as CMOS devices for example, comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event. This might happen for example when somebody induces a voltage peak into the circuitry by touching the pins of the chip.

*Reiner, 2:28-3:1*

The present invention is well suited for use in integrated circuit devices, such as CMOS devices for example, that comprise an electrostatic discharge device (ESD) protection. Part of an integrated circuit device 30 with a ESD output protection means is

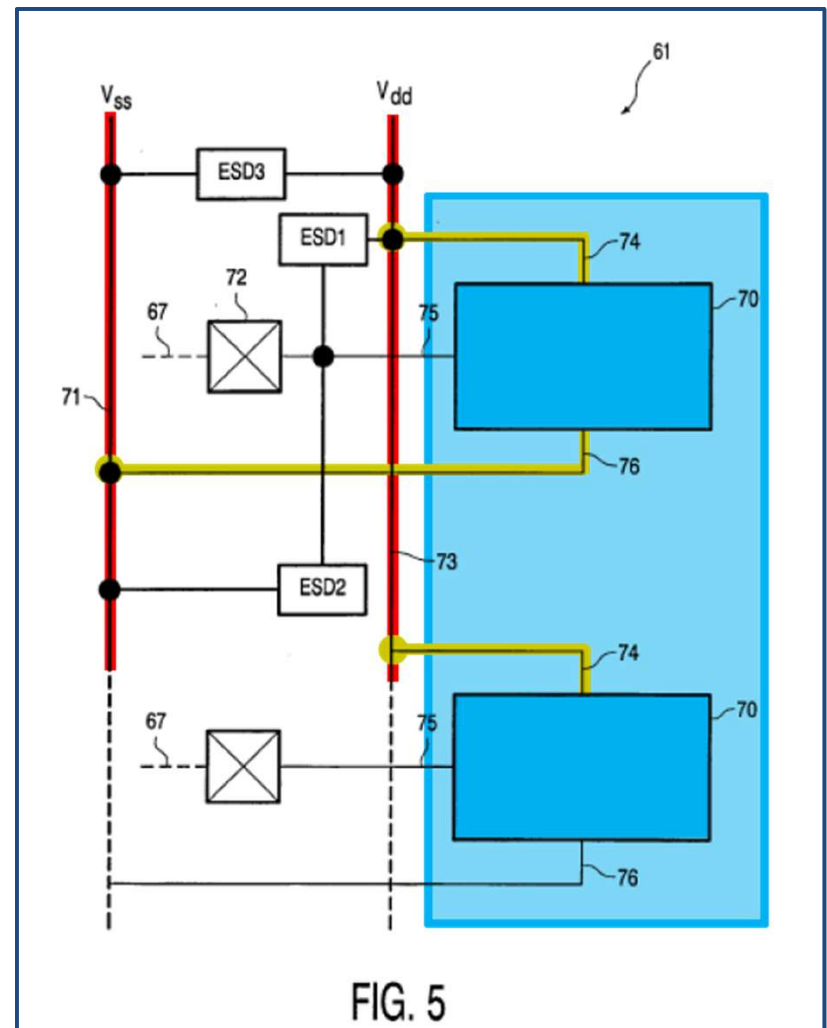
*Reiner, 8:8-10*

Integrated circuit devices quite often have areas where the output or input metal lines have to cross power supply lines. A typical example is an integrated circuit display driver 61 or 63 that is designed to drive many lines of an LCD display 60, as illustrated in Fig. 4. Such a display driver 61, 63 typically has a large number of parallel outputs. In order to keep the cost for making such display drivers in an affordable range, one

*Reiner, 9:11-15*

herein is in particular suited for such integrated circuit devices. The bump bridges allow many output devices of the integrated circuit device 61 or 62 to cross the power supply lines which provide supply voltage (e.g.,  $V_{dd}$ ) to the output devices. A schematic block diagram of a display driver 61 in accordance with the present invention is given in Fig. 5. ESD protection means can easily be integrated into such a display driver 61.

*Reiner, 9:18-22*



*Reiner, FIG. 5  
See, e.g., Petition 19-24*

# Petitioner's expert explains why *Reiner* describes protecting the scanning line driving circuit from ESD damage

104. As I explain in [4b], *Reiner* “relates to integrated circuit devices with ESD protection.” *Reiner*, 2:2-3, 4:15-16 (“It is an object of the present invention to provide a scheme that allows to add an ESD protection network to densely packed integrated circuit devices.”) (emphasis added). A “typical example is an integrated circuit display driver 61 or 63” in *Reiner*, *Reiner*, 9:12-14, 12:4-5 (emphasis added). *Reiner* generally discloses that its teachings are “well suited for integrated circuit devices operating with two or more supply voltages (e.g., Vdd, Vee and Vss)” (power supply lines). *Reiner*, 12:4-5. *Reiner* also explains that its disclosure has “advantages” of being “well suited for conducting currents occurring during ESD events” and “avoid[ing] thermal damage caused by high current during an ESD event.” *Reiner*, 12:23-25, see also *Reiner*, 8:8-15 (“The present invention is well suited for use in integrated circuit devices, such as CMOS devices for example, that comprise an electrostatic discharge device (ESD) protection.”). *Reiner* continues that, “[q]uite often integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1 (emphases added).

Murphy ¶104

105. *Reiner*'s FIG. 5 shows a “schematic block diagram of a display driver 61” where “ESD protection means can easily be integrated into such a display driver 61.” *Reiner*, 9:20-22. This statement in *Reiner* ends a paragraph that more generally discusses “integrated circuit display driver 61 or 63” and “display driver 61, 63,” thus confirming that both the source driver 61 and the gate driver 63 are “display drivers” to be protected from ESD events, *Reiner*, 9:11-22 (emphases added). Indeed, a POSITA would have understood that *Reiner* generally describes the protection of “integrated circuits,” which *Reiner* makes clear can be either gate driver 63 or source driver 61. As such, a POSITA would have understood that FIG. 5 describes source driver 61 as exemplary and that FIG. 5's teachings apply equally to gate driver 63 (scanning line driving circuit) because gate driver 63 is also a “driver display circuit.” Indeed, *Reiner*'s explanation that “[q]uite often, integrated circuit devices ... comprise an electrostatic discharge device (ESD) protection in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event” does not differentiate between the source driver 61 and the gate driver 63, thus teaching, or at least suggesting, that both integrated driver circuits would be protected in a similar manner. *Reiner*, 2:28-3:1.

Murphy ¶105  
See, e.g., Petition 24-26

# The record establishes a motivation to protect scan line driver circuits with ESD protection like *Reiner's* Fig. 5 (1/4)

111. Thus, *Reiner* explains that ESD1, ESD2, and ESD3 protect the drive circuitry at each line driver unit 70, which together form the gate driver 63 and thus the gate driver 63 is protected. *Reiner*, 10:10-15. In FIG. 5, as shown below, driver “output devices 70” are shown as ‘black box’ elements. These boxes 70 do not show the internal circuitry, and a POSITA would have recognized that the ESD protection network protects any driver circuitry in that box and that the protection provided applies equally to both source driver 61 and the gate driver 63, especially in light of *Reiner's* discussions that both drivers are “integrated circuits” that *Reiner* discloses need protecting from electrostatic damage because they contain “very sensitive circuits” that are easily damaged. See *Reiner*, 2:28-3:1, 4:15-16, 9:11-22. As such, a POSITA would have understood that *Reiner's* description of ESD protection in FIG. 5 also applies to gate driver 63 and that the ESD protection shown in FIG. 5 would have protected gate driver 63, where each of output devices 70 (together the gate driver 63) comprises the line-driving circuitry for driving each scan line 68.

Murphy ¶111

devices. Because *Reiner* teaches that a “typical example” of a protected integrated circuit “is an integrated circuit display driver 61 or 63,” a POSITA would have found it obvious to protect the gate driver 63 (scanning line driving circuit) with the same ESD protection network as the source driver 61 described in the example of FIG. 5. *Reiner*, 9:12-14, 12:4-5 (emphasis added). *Reiner* generally describes protecting integrated circuits and both gate drivers (scanning line driving circuits) and source drivers (data line driving circuits) are types of integrated circuits that are usually comprised of various circuit elements, such as transistors, that receive power and other signals, such as clock or data signals.

Murphy ¶112

See, e.g., Petition 27-30

## The record establishes a motivation to protect scan line driver circuits with ESD protection like *Reiner's* Fig. 5 (2/4)

113. As explained by *Reiner*, the transistors in these driving circuits can be MOS (metal oxide semiconductor) transistors or other types of transistors that are used to provide the driving signal for each of the gate lines (scan lines) or source lines (data lines). That is, each of the lines being driven will have its own semiconductor units (e.g., *Reiner's* output devices 70) the drive that particular line. The collection of each of the line drivers for the scan lines or data lines forms the entire driving circuit for either the gate driver 62 or the source driver 61, respectively. In my opinion, a POSITA would have recognized that the similarities in the driving circuits, such as both having transistor elements in the line driving units, and *Reiner's* warning that both driver circuits contain "very sensitive circuits" that can be "destroyed" by ESD, would have lent itself to protecting both the source driver 61 and the gate driver 63. A POSITA also would have been cognizant that *Reiner's* ESD protection network of FIG. 5 has several benefits, including being effective for "densely packed" driver circuits, protecting against both electrical and thermal ESD damage, and being compatible with manufacturing methods that have only a single metal layer (which could lower the cost of producing the driver circuits). Given these benefits (although the same motivation would apply for either or both benefit) and the similarities of the gate and source drivers themselves, a POSITA would have found it obvious to protect *Reiner's* gate driver 63 using the same type of ESD protection network described for the source driver 61 in FIG. 5.

Murphy ¶113

114. In my opinion, a POSITA would have found this obvious because it would have also protected the gate driver 63 from being damaged by ESD events that could "destroy[]" the "very sensitive circuits" of the gate driver, which could render the display unacceptable. Such damage can be either thermal or electrical and *Reiner* explains that its ESD protection would have protected against both types of damage. *Reiner*, 2:28-3:1, 12:24-25. As such, a POSITA would have been further motivated to implement *Reiner's* ESD protection network in gate driver 63 to prevent damage to any part of the circuit.

Murphy ¶114

See, e.g., Petition 27-30

# The record establishes a motivation to protect scan line driver circuits with ESD protection like *Reiner's* Fig. 5 (3/4)

70] of the integrated circuit device 30.”). A POSITA would have been motivated, as explained by *Reiner*, to “protect the circuitry” of each of the output devices of the gate driver 63 in the same way as source driver 61 to prevent the sensitive circuits from being damaged by ESD events occurring on either of the voltage lines Vss and Vdd or on the output line from the gate driver (the equivalent of output line 75 of the source driver 61). *Reiner*, 10:10-12. For example, a POSITA would have been motivated to provide ESD protection circuits for the gate driver 63 because a POSITA would have wanted to protect both driver circuits because an LCD display can be rendered unacceptably or irreparably damaged if either the gate driver (scanning line driving circuit) or the source driver (data line driving circuit) is damaged by ESD because damage to either driver prevents impairing activating parts of the screen, such as pixel rows or columns of the LCD screen.

Murphy ¶115

116. In my opinion, a POSITA would have also been motivated to protect *Reiner's* gate driver 63 with ESD protection like that shown in FIG. 5 because it “allows ... add[ing] an ESD protection network to densely packed integrated circuit devices.” *Reiner*, 4:15-16. A POSITA would have recognized that the risk of ESD damage (both electric and thermal) is heightened for densely packed integrated circuits, such as *Reiner's* gate driver 63, because they contain “very sensitive” circuit elements that would be close together and thus more of the individual driver units making up the gate driver 63 would be susceptible to ESD damage. *Reiner*, 2:28-3:1, 4:15-16.

Murphy ¶116

*See, e.g.*, Petition 30-33

# The record establishes a motivation to protect scan line driver circuits with ESD protection like *Reiner's* Fig. 5 (4/4)

117. A POSITA would have also recognized that implementing the “ESD protection network” of *Reiner's* FIG. 5 in gate driver 63 protect “each output device” of the gate driver 63 (the driver unit equivalent to output device 70 for each scan line) because it represents merely implementing the known prior art ESD protection network of *Reiner* in *Reiner's* gate driver 63 to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s]” of gate driver 63. *Reiner*, 4:15-16, 10:10-12. Similarly, a POSITA would have been motivated to implement *Reiner's* known ESD protection network to improve the similar gate driver 63 in the same way as the example shown in FIG. 5 because the ESD protection network protects the output circuit in box 70, which could be either a source driver or gate driver because they have similar configurations and both need protection from ESD events. *See Reiner*, 2:28-3:1. At a minimum, in my opinion, a POSITA would have found it obvious to try implementing *Reiner's* ESD protection network shown in FIG. 5 to protect the scan line driver units (output device) of gate driver 63 and thereby protect the gate driver 63, given *Reiner's* teaching that both source driver 61 and gate driver 63 are “integrated circuits” and contain “very sensitive circuits” that can be “destroyed when ... subjected to [an ESD] discharge event” and, therefore, need protecting. *Reiner*, 2:28-3:1, 9:12-14.

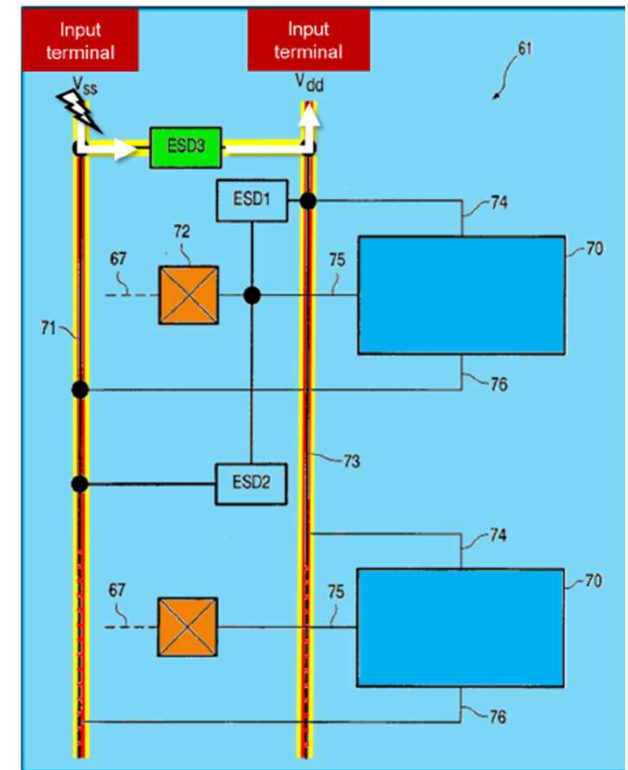
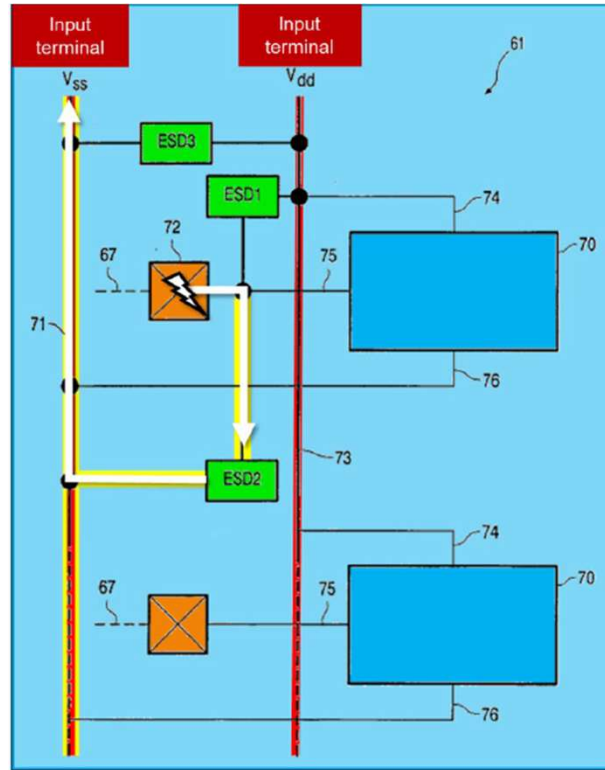
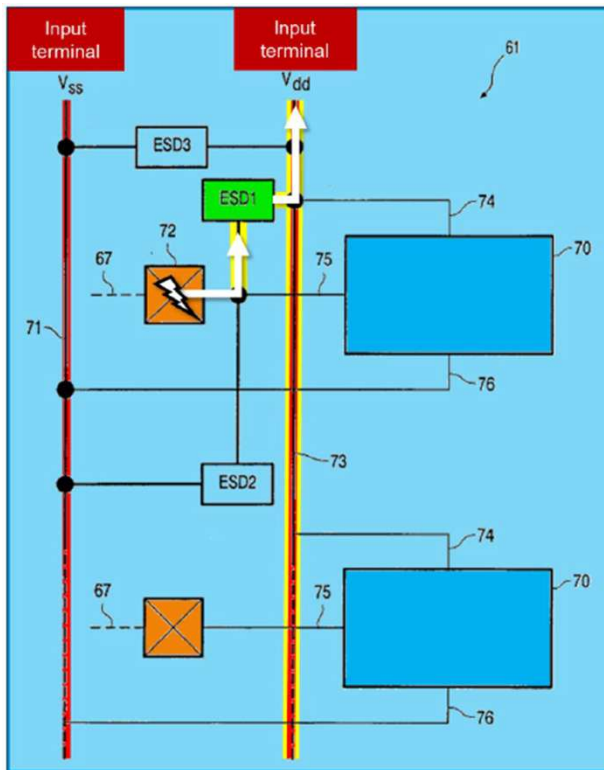
Murphy ¶117

119. A POSITA would also have been motivated to implement the ESD protection network to protect gate driver 63 to prevent damage to the sensitive line driver circuitry and “realize more densely packed integrated circuit devices” and thereby reduce the risk of damage from ESD events, and reduce fabrication costs. *Reiner*, 4:15-19, 12:16-18. A POSITA also would have recognized that because *Reiner's* gate driver 63 and source driver 61 include contact pads 72 for bonding the driver to a substrate, that static charge could also enter the circuits through the contact pads 72, and that ESD2 and ESD3 would protect the circuitry inside of the drivers (e.g., would protect each of the driver output devices 70) from static charges, in addition to protecting the drivers from static charges accumulating on the power lines Vdd and Vss.

Murphy ¶119

*See, e.g.*, Petition 30-33

# Patent Owner acknowledges that *Reiner's* ESD1, ESD2, ESD3 protect the driver circuits inside box 70



Patent Owner's Response 37-39

See, e.g., Patent Owner's Response 37-39; Pet'r Reply 16-17

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

# Patent Owner's expert's alleged "differences" between driving circuits are similarities that actually support obviousness

38. As I explain in my previous declaration, although *Reiner*'s FIG. 5 expressly labels source driver 61, a POSITA would have understood that the protection network applies equally to gate driver 63. Ex. 1003, ¶¶105, 111-120, 150, 238-242.

Murphy II ¶38

39. Dr. Schubert spends several paragraphs arguing that "differences between a source driver and a gate driver" would have precluded a POSITA from finding the claims obvious. See Schubert Declaration ¶¶63-68. I disagree with Dr. Schubert that any such differences would have rendered the claims nonobvious. Even if the differences he identifies were present, they would not have prevented a POSITA from finding it obvious to apply *Reiner*'s ESD protection network to a gate driver because they are immaterial to ESD protection. Indeed, some of Dr. Schubert's alleged "differences" actually highlight the similarities that would have made it more obvious to a POSITA.

Murphy II ¶39

40. As one example, where Dr. Schubert asserts that "*Reiner* discloses that the gate driver integrated circuit comprises individual gate drivers, not output devices 70" (Schubert Declaration ¶¶64, 65), he appears to misunderstand how gate and source drivers operate by alleging that the same general structure is somehow different. A POSITA would have known and recognized that "individual gate drivers" that "drive one whole gate line 68" describes a gate driver unit for each gate or scan line, which is the same as the individual driver units 70 shown in FIG. 5 to drive each individual line (like the individual source driver units that drive each individual source line). See *Reiner*, 9:27-28. Indeed, the '157 patent explains that this setup is conventional, as shown in FIG. 11. It was, in fact, commonplace and conventional. Because a gate driver line circuit (e.g., what would be inside box 70 in *Reiner*'s FIG. 5) is used to drive each gate line to turn it on and off, there would have been a driver unit for each line to control and time the scanning of the display. As such, Dr. Schubert's alleged "difference" actually supports applying *Reiner*'s ESD protection network in FIG. 5 to gate driver 63 because that network protects *any* circuit inside box 70 whether it has a gate driver line unit configuration or a source driver line unit configuration. See Ex. 1003, ¶111 (explaining that a POSITA would have recognized that line unit circuit 70 is a "black box," and any circuit inside would be protected by *Reiner*'s ESD protection network).

Murphy II ¶40

See, e.g., Pet'r Reply 3-8

# Patent Owner's expert acknowledges that ESD would render scanning line drivers "nonfunctional" without protection

Q        You mentioned that ESD can damage or destroy transistors. What happens if an ESD event destroys the transistors in a scanning line driving circuit?

A        If the transistors of a circuit are destroyed then the circuit becomes nonfunctional.

Schubert Tr. (Ex. 1018), 52:14-19

48. Dr. Schubert's "[f]ourth" position that "a specific ESD protection arrangement that works for source drivers would not necessarily be known to work as ESD protection for a gate driver" (Schubert Declaration ¶67 (bold emphasis omitted)) appears to tacitly acknowledge, correctly in my opinion, that ESD protections *could* work for gate drivers.<sup>6</sup> A POSITA would have understood that Reiner's ESD protection in FIG. 5 protects whatever circuit is in box 70, because it protects each of the lines connecting box 70 to the output line (e.g., gate or source line) and the power lines. By protecting all of these connections, a POSITA would have recognized that Reiner's ESD protection circuit network protects whatever is in box 70 as a "black box" because it prevents ESD from damaging the circuit, irrespective of the specific way in which the circuitry is implemented. See Ex.

Murphy II ¶48

the yard (e.g., whether it has a pool or a patio in the yard). A POSITA would have understood that both the gate drivers and source drivers within a device are composed of the same materials (e.g., CMOS), same circuit devices (e.g., transistors), similar circuit designs, same substrate, etc., and as such, the ESD protection network Reiner describes for FIG. 5 would have been expected to protect either source driver circuitry or gate driver circuitry equally. See Ex. 1003,

<sup>6</sup> I note that Dr. Schubert stops short of saying that Reiner's ESD protection circuit would not work for a gate driver. As explained above and in my previous

Murphy II ¶48

See, e.g., Pet'r Reply 3-8, 30

# Patent Owner's alleged signal operation differences are immaterial to ESD protection for scanning line driving circuits

46. Dr. Schubert's "[f]irst" position that individual gate driver units may be connected to operate as a shift register (e.g., the SP line in the '157 patent) (Schubert Declaration ¶67 (bold emphasis omitted)) is not material to protecting the driver units by ESD protection circuits coupled to the power lines for the reasons explained above.

Murphy II ¶46

42. Dr. Schubert also asserts that "a POSITA would expect to see differences between the gate driver arrangement and the source driver arrangement," for example, "that individual gate/scan line drivers are coupled to one another, to coordinate signals and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time (e.g., one would not simultaneously turn ON two horizontal rows of transistors)." Schubert Declaration ¶66. Dr. Schubert claims to identify additional differences in paragraph 67 of the Schubert Declaration. See Schubert Declaration ¶67. A POSITA would not have found that any of these differences are material to whether *Reiner* discloses or renders obvious the claims of the '157 patent. Indeed, many do not relate to the claimed structures at all, as I explain below.

Murphy II ¶42

47. Dr. Schubert's "[s]econd" and "[t]hird" positions that gate lines are driven one at a time and source lines are driven together (Schubert Declaration ¶67 (bold emphases omitted)) is also not material because that relates to the operation of the signal lines, not protection by connecting ESD protection circuits to the power lines during manufacturing when ESD is most likely to occur. Moreover, as I also explain above, this supports obviousness because each of the gate and source drivers has one driver circuit per line such that the overall structure is similar. Because *Reiner*'s ESD protection network in FIG. 5 would have been understood to protect whatever circuit is in box 70, a POSITA would have found it obvious to apply *Reiner*'s ESD protection to gate driver 63. See Ex. 1003, ¶¶103-133.

Murphy II ¶47

See, e.g., Pet'r Reply 3-8

## **Scanning Line Driver Circuit Protection Limitations:**

**Configuration of ESD protection circuits and  
a first connecting portion ([4e],[4f])**

# Petitioner's expert's Figures Ax, Bx, and Cx show all of elements [4d]-[4f]

**Scan line driving circuit**  
(blue, gate driver 63, outputs 70)

**Power supply lines**  
(red, Vdd/Vss)

**First protection circuit**  
(light green, ESD)

**Second protection circuit**  
(dark green, ESD)

**Protection circuit-to-scan driver connection** (orange)

**First connecting portion**  
(teal, scan driver-to-power supply)

**Second connecting portion**  
(pink, first protection circuit-to-power supply)

**Third connecting portion**  
(purple, second protection circuit-to-power supply)

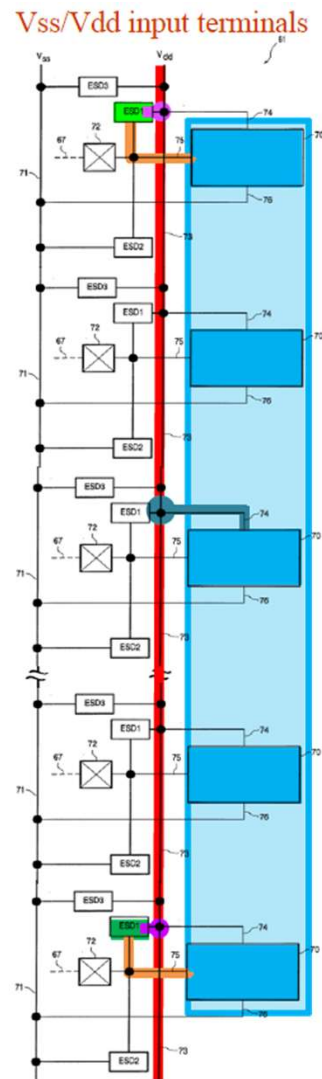


FIG. Ax

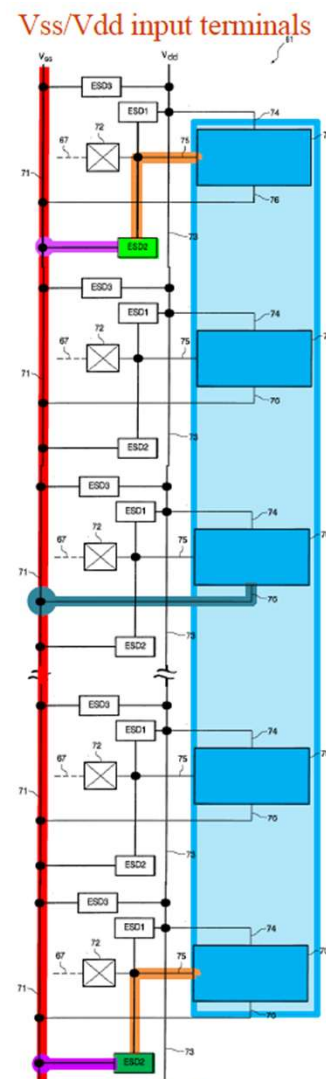


FIG. Bx

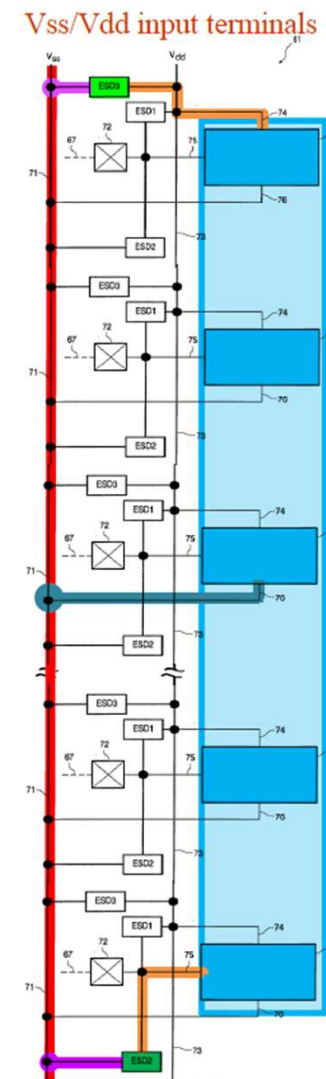


FIG. Cx

See, e.g., Murphy ¶¶106-132; Petition 25-40

## Patent Owner incorrectly requires that the first and second ESD connections be outside *all* “connecting portions,” not just the “first connecting portion”

First, as discussed in detail below regarding claim 4[e], Petitioner fails to refute Patent Owner’s correct interpretation that all scanning line driver connections must be between the two protection circuit connections. Reply, 8, 13; *see* § II.A.2, *infra*.

PO Sur-Reply 2-3

*See, e.g.,* Patent Owner’s Response 27-42; PO Sur-Reply 2-3

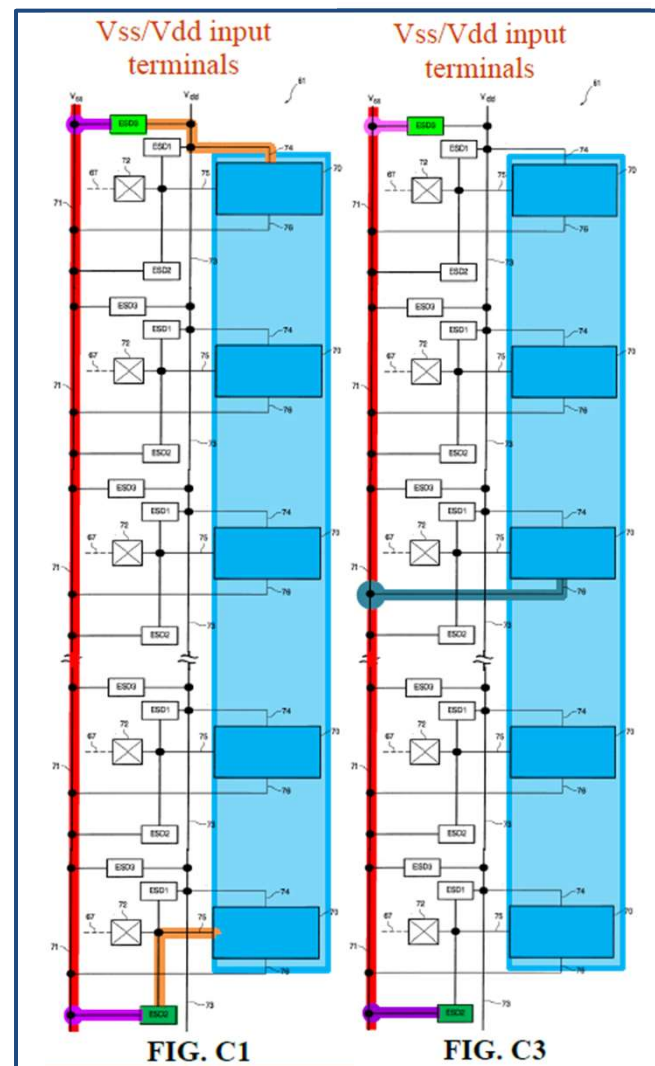
# Reiner discloses Patent Owner's construction of two ESD protection circuit connections outside all scanning line driver circuit connections (Figure Cx)

ESD3 is connected to lines Vss and Vdd between the purported input terminals and output devices 70 to protect output devices 70 from electrostatic charges that may enter integrated circuit device 61 through the Vss or Vdd input terminals and travel along the power lines and enter output device 70 via connections 74 or 76, respectively. Ex. 1005, 10:14-20; Ex. 2009 ¶82; Ex. 2008, 134:10-18. ESD3 prevents electrostatic charges (white lightning bolts) from

PO Response 38-39

110. I have also been asked to consider the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines.<sup>13</sup> As shown in FIG. C1, the first protection circuit ESD3 before the first driver unit of the gate driver 63 (closest to the input terminals) and the second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) are connected to the line driving units of the gate driver 63 “to protect the circuitry inside the devices” and also connected to the power supply line Vss on either side of the gate driver 63. See Reiner, 10:1-15.

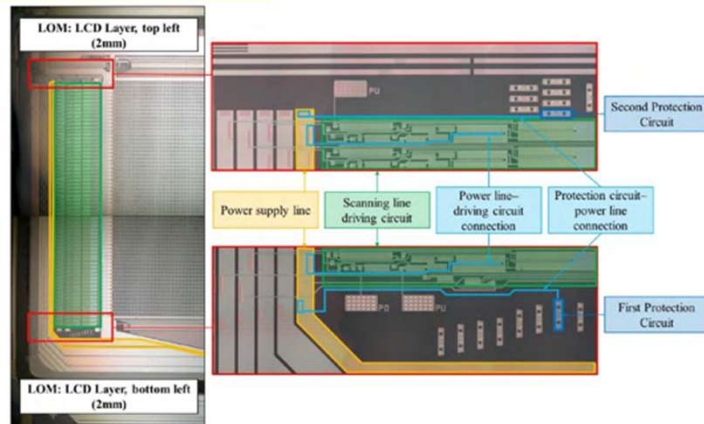
Murphy ¶110



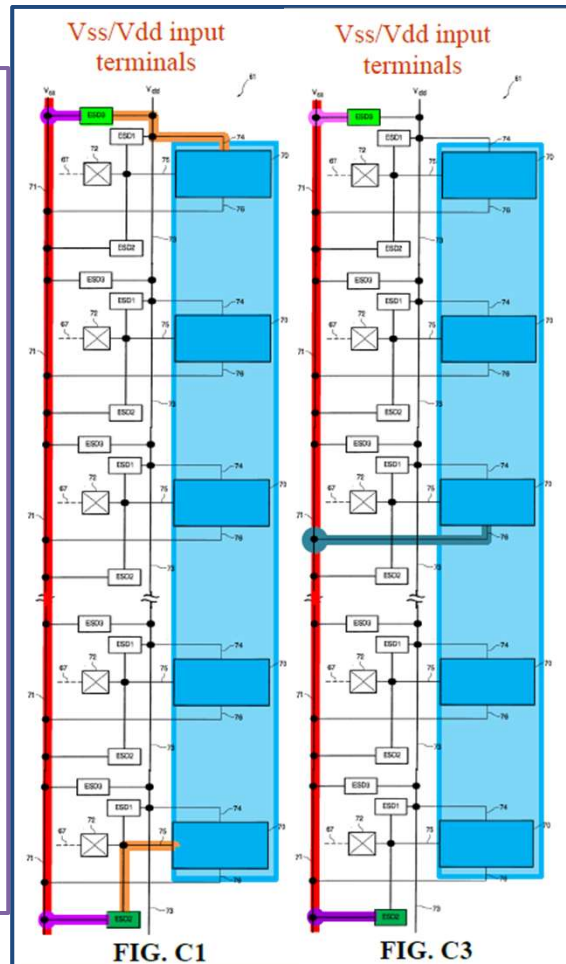
Murphy ¶¶110 (FIG. C1), 121-132 (FIG. C3)  
See, e.g., Petition 34-40; Ex. 1014 (Compl.) ¶¶142-143

# Patent Owner's alleges that the same connections as Figure Cx infringe claim 4

136. BOE display modules and panels, including, for example, the LCD panel used in the HP 21kd monitor, are display devices comprising a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line. The BOE LCD panel used in the HP 21kd monitor includes a first protective circuit and a second protective circuit, each of which is connected to the power supply line, which is connected to the scanning line driving circuit, and the protective circuits are connected to the scanning line driving circuit via the power supply line:

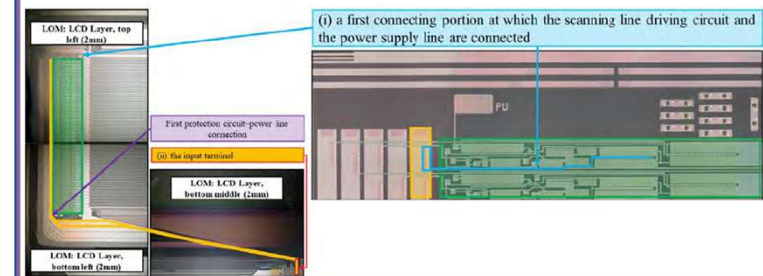


Ex. 1014, ¶136



Murphy ¶¶110 (FIG. C1), 121-132 (FIG. C3)

139. The first connecting portion is where the scanning line driving circuit and the power supply line are connected:



Ex. 1014, ¶139

See, e.g., Petition 34-40 (citing Ex. 1014, ¶¶136-144) ; Ex. 1014 (Compl.) ¶¶136, 139, 142-143

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

# Patent Owner cannot avoid its own construction



“Neither statement prohibits a petitioner from relying on a claim construction that it believes is incorrect, for example, a claim construction relied upon by patent owner in a related district court action.”

*10X Genomics, Inc. v. Bio-Rad Lab’ys, Inc.*,  
IPR2020-00088, Paper 8, at 16 (PTAB Apr. 27, 2020)

*See, e.g.*, Pet’r Reply 9-10

## The claims require only one “connecting portion” between the first and second ESD connections, not all “connecting portions”

4. A display device, comprising:

a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and

the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

10. A display device, comprising:

a circuit element included in a scanning line driving circuit;

a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;

an input terminal connected to the power supply line to supply power; and

a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element, the first protection circuit and the second protection circuit are connected to the power supply line,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and

the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

*See, e.g.,* Pet'r Reply 11-12; Ex. 1001, claims 4, 10, 18

# The specification shows a single connecting portion between two ESD protection circuit connections

FIG. 2

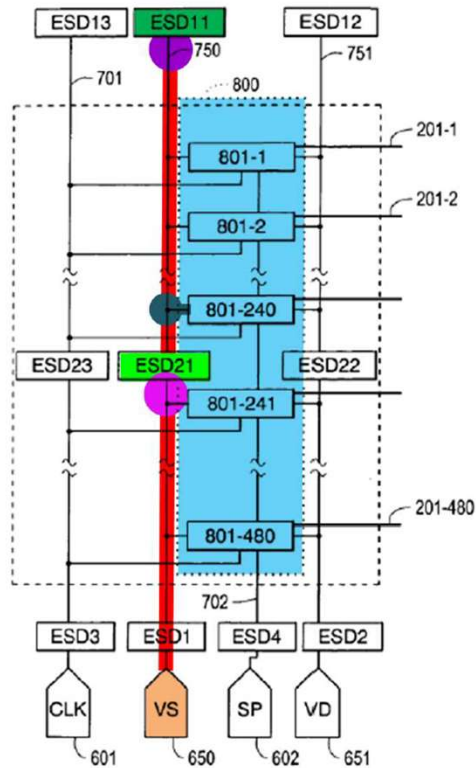


FIG. 2

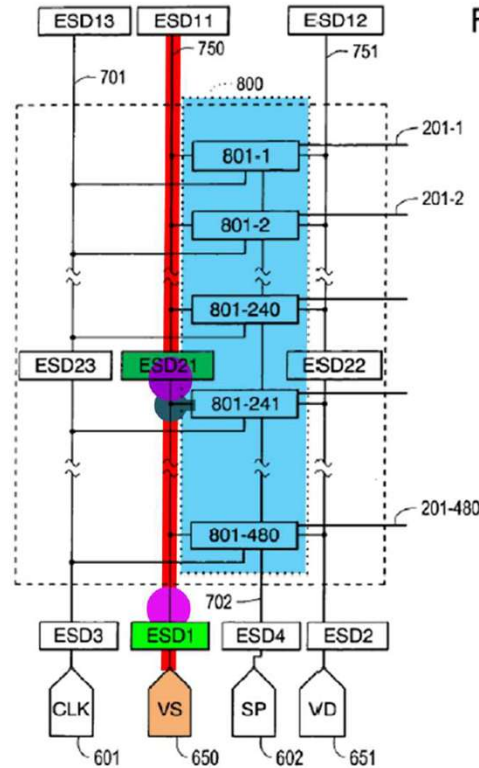
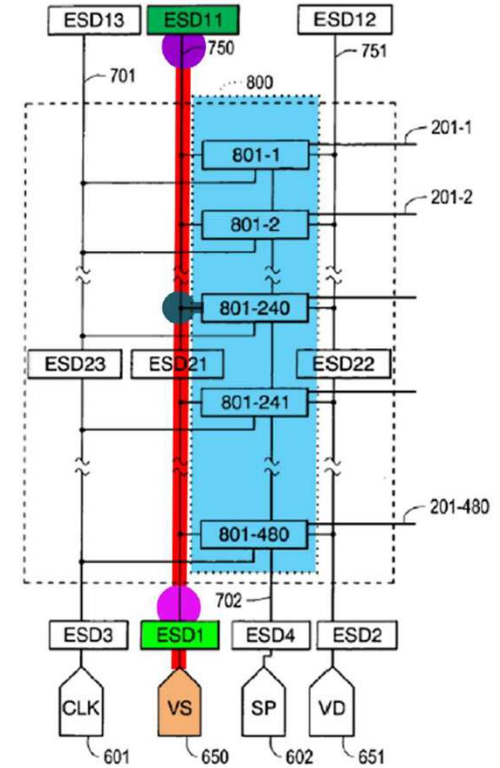


FIG. 2



First protective circuit  
Second protective circuit

First connecting portion  
Second connecting portion  
Third connecting portion

See, e.g., Murphy II ¶ 58; Pet'r Reply 12-13

## Patent Owner's requirement that “all” connecting portions be between the two ESD protection circuit connections is contrary to law



“Thus, *any* blade in between the first and third blades and with an exposure greater than that of the first blade and less than that of the third blade is a ‘second’ blade in the claimed subset of blades.”

*Gillette Co. v. Energizer Holdings, Inc.*,  
405 F.3d 1367, 1371-74 (Fed. Cir. 2005)



“[T]his court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’”

*Baldwin Graphic Sys., Inc. v. Siebert, Inc.*,  
512 F.3d 1338, 1342 (Fed. Cir. 2008)

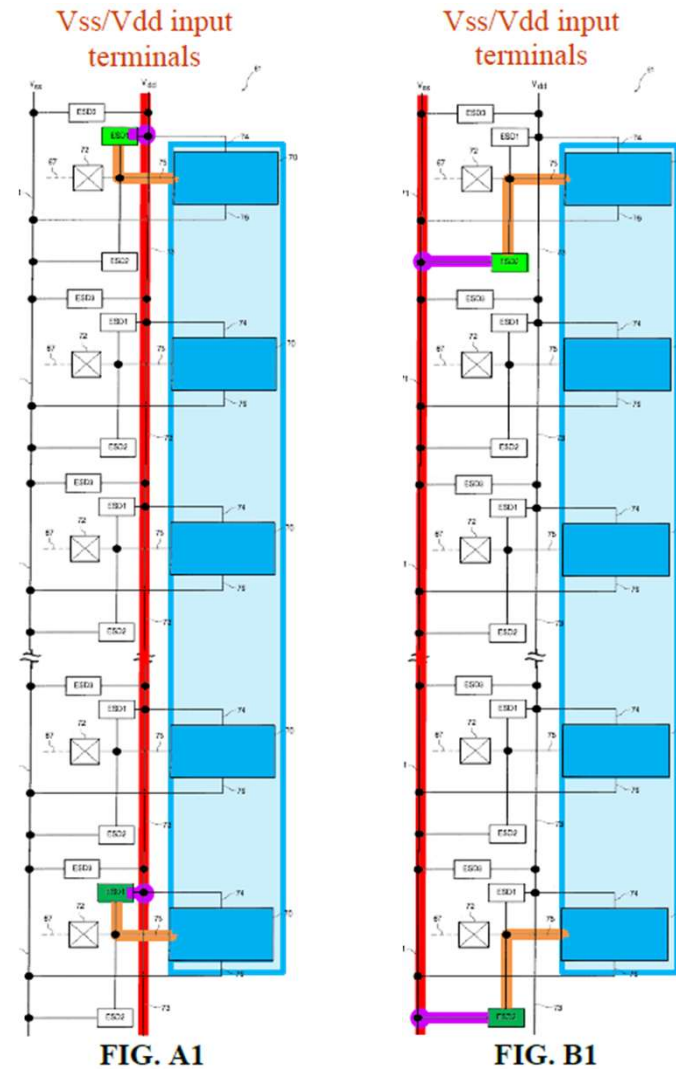
*See, e.g.*, Pet'r Reply 10-13

## Reiner discloses the two ESD protection circuits connected to the scanning line driving circuit [4d] (Figures Ax and Bx)

108. As shown in FIG. A1, the first ESD1 protection circuit at the first driver unit of gate driver 63 (closest to the input terminals) and the second ESD1 protection circuit at the last gate driver unit (farthest from the input terminals) are connected to the line driving units 70 of the gate driver 63 through output line 75 “in order to protect the circuitry inside the devices” and also connected to the power supply line Vdd. See Reiner, 10:1-15.

109. As shown in FIG. B1, the first ESD2 protection circuit at the first driver unit of gate driver 63 (closest to the input terminals) and the second ESD2 protection circuit at the last gate driver unit (farthest from the input terminals) are connected to the line driving units of the gate driver 63 through output line 75 “in order to protect the circuitry inside the devices” and also connected to the power supply line Vss. See Reiner, 10:1-15.

110. I have also been asked to consider the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines.<sup>13</sup> As shown in FIG. C1, the first protection circuit ESD3 before the first driver unit of the gate driver 63 (closest to the input terminals) and the second protection circuit ESD2 at the last gate driver unit (farthest from the input terminals) are connected to the line driving units of the gate driver 63 “to protect



Murphy ¶¶108-110

See, e.g., Petition 26-28, Murphy ¶¶103-110

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

# Reiner discloses the “first connecting portion” between the input terminals and scanning line driver connection [4e] (Figures Ax and Bx)

124. As shown above in FIG. A2, for example, the first protection circuit ESD1 at the first gate driver unit of gate driver 63 closest to the input terminals is connected to the power supply line Vdd between (i) a first connecting portion at which the gate driver 63 and the power supply line Vdd are connected at line 74 and (ii) the input terminal supplying power to the power supply line Vdd.

125. Similarly, as shown above in FIG. B2, for example, the first protection circuit ESD2 at the first gate driver unit of gate driver 63 closest to the input terminals is connected to the power supply line Vss between (i) a first connecting portion at which the gate driver 63 and the power supply line Vss are connected at line 76 and (ii) the input terminal supplying power to the power supply line Vss.

126. And, when considering the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines, as shown above in FIG. C2, for example, the first protection circuit ESD3 before the first driver unit of the gate driver 63 closest to the input terminals is connected to the power supply line Vss between (i) a first connecting portion where the gate driver 63 and the power supply line Vss are connected at line 76 and (ii) the input terminal supplying power to the power supply line Vss. Reiner, 10:1-15.

Murphy ¶¶123-126

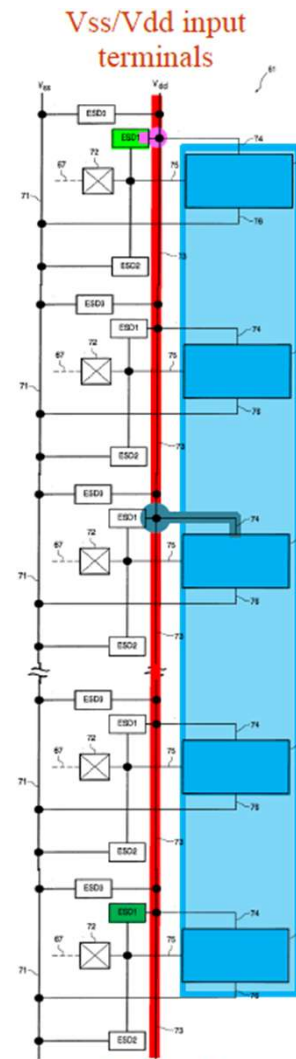


FIG. A2

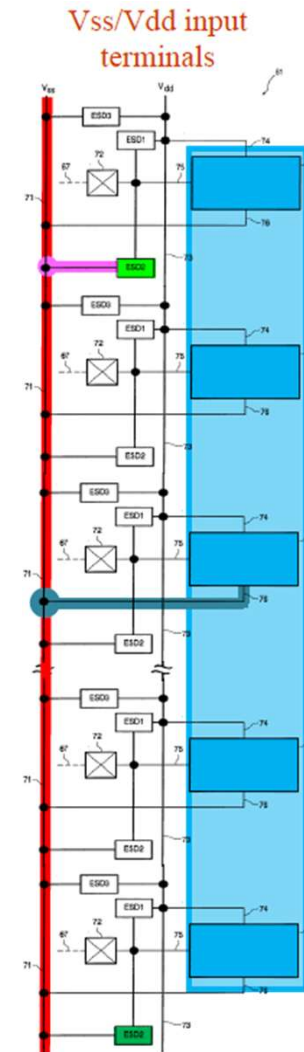


FIG. B2

See, e.g., Petition 34-36, Murphy ¶¶123-126

# Reiner discloses the “first connecting portion” between the two ESD protection circuit connections [4f] (Figures Ax and Bx)

130. As shown above in FIG. A3, for example, the gate driver 63 (scanning line driving circuit) is connected to the power supply line Vdd (such as described in [4e], FIG. A2) between (iii) a second connecting portion at which the first protection circuit ESD1 at the first gate driver unit of gate driver 63 (closest to the input terminals) and the power supply line Vdd are connected (also described in [4e], FIG. A2) and (iv) a third connecting portion at which the second protection circuit ESD1 at the last gate driver unit of gate driver 63 (farthest from the input terminals) and the power supply line Vdd are connected. See Reiner, 10:1-15.

131. Similarly, as shown above in FIG. B3, for example, the gate driver 63 (scanning line driving circuit) is connected to the power supply line Vss (such as described in [4e], FIG. B2) between (iii) a second connecting portion at which the first protection circuit ESD2 at the first gate driver unit of gate driver 63 (closest to the input terminals) and the power supply line Vss are connected (also described in [4e], FIG. B2) and (iv) a third connecting portion at which the second protection circuit ESD2 at the last gate driver unit of gate driver 63 (farthest from the input terminals) and the power supply line Vss are connected. See Reiner, 10:1-15.

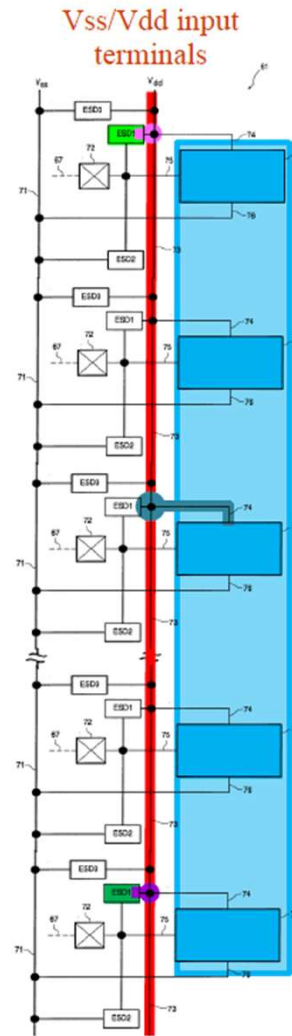


FIG. A3

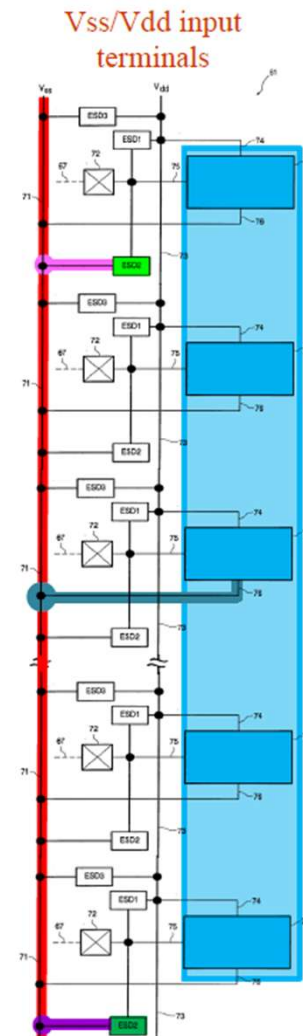


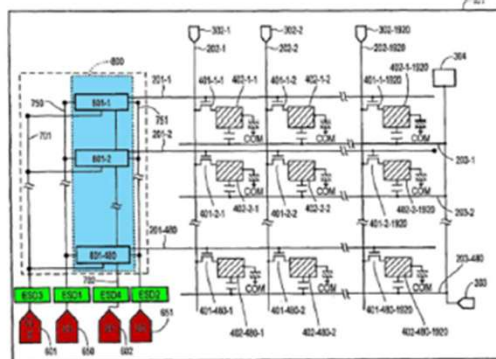
FIG. B3

Murphy ¶¶130-131

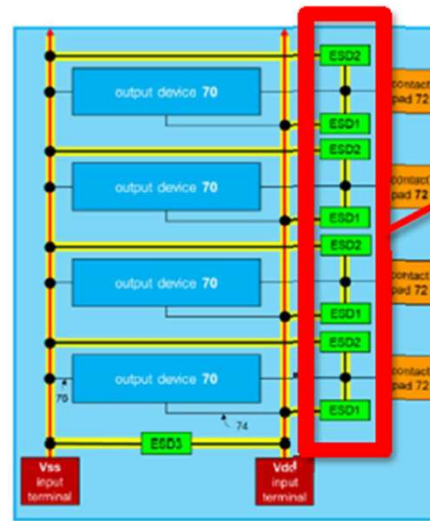
See, e.g., Petition 37-40, Murphy ¶¶129-132

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

# Reiner discloses hundreds more ESD protection circuits than the “conventional art” in the '157 Patent



Schubert Declaration ¶79 (annotating Ex. 1001, FIG. 11).



Additional ESD protection circuits not shown in '157 patent, FIG. 11

Schubert Declaration ¶80 (red text and box annotations added, other annotations in original).<sup>7</sup>

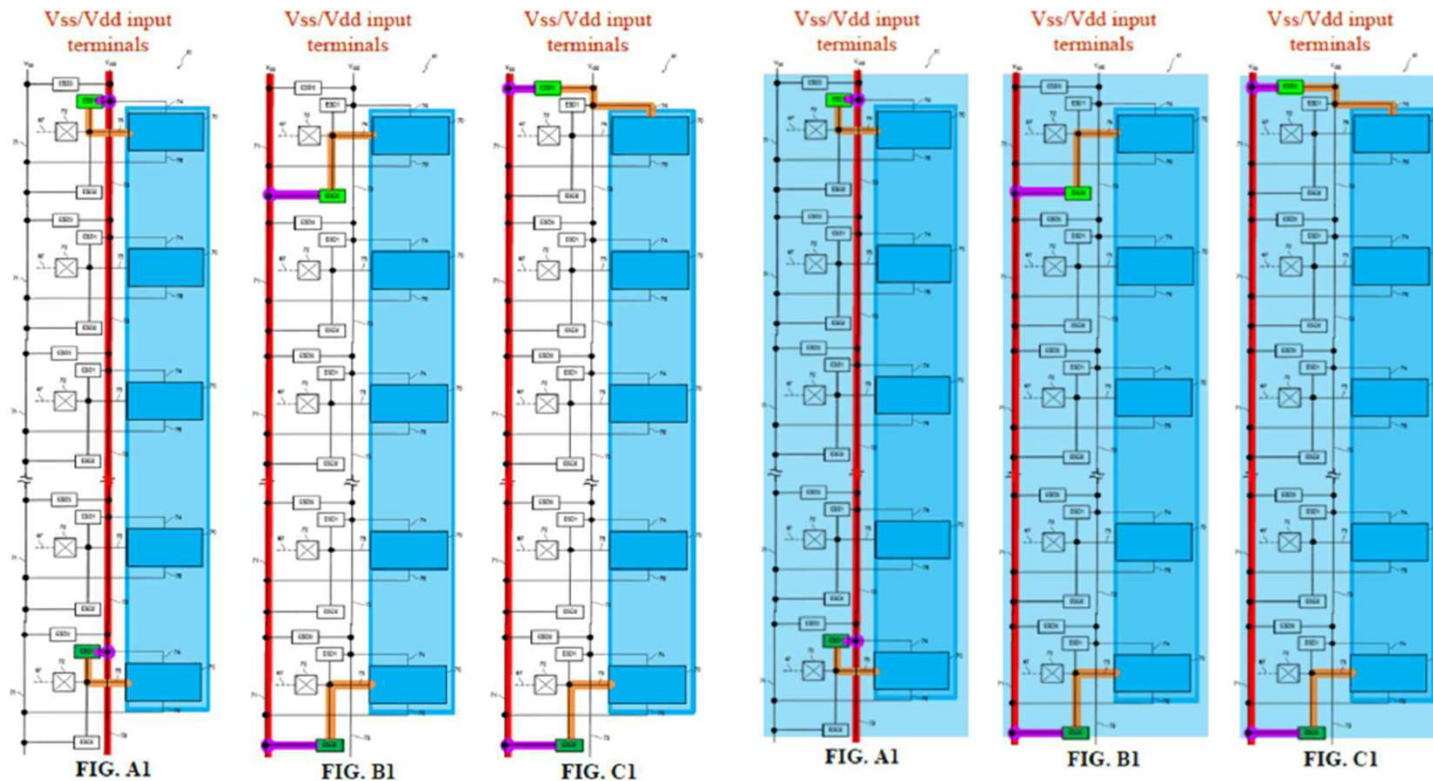
Murphy II ¶62

As Dr. Schubert’s own figure above shows, *Reiner*’s protection circuit network provides for hundreds of additional ESD protection circuits that protect the driver units far away from the input terminals—indeed all the way to the other end of the driver circuit—which is the alleged “improvement[.]” of the '157 patent. See

Murphy II ¶65

See, e.g., Patent Owner’s Response 34-36; Pet’r Reply 14-15; Murphy II ¶¶62-65

# Patent Owner's incorrect arbitrary box drawing does not change the outcome that *Reiner* discloses or renders obvious the claims



Murphy II ¶73



“Broadly speaking, ‘to’ does not exclude the word ‘in,’ as Altair wants this Court to rule.”

*Aspex Eyewear, Inc. v. Altair Eyewear, Inc.*, 818 F. Supp. 2d 348, 354 (D. Mass. 2011) (“secured to” includes secured “in” and “within”), *aff’d*, 484 F. App’x 565 (Fed. Cir. 2012)

*See, e.g.*, Pet’r Reply 17-20

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

## ***Reiner's* source driver module includes a scanning line driving circuit separate from the ESD protection**

70. I recognize that, during my deposition (Ex. 2008), Patent Owner drew an arbitrary line around the scanning line driver units (group of units 70) that also includes the ESD circuits ESD1-ESD3. Patent Owner appears to take my statements out of context. In my deposition, I was asked about a “source driver *module*,” which a POSITA would have understood is more than just the scanning line driver *circuit* itself. See, e.g., Ex. 2008, Murphy Tr., 94:22-103:16, 137:22-139:16 (emphasis added). A POSITA would have recognized that a “module” may often include more than the circuitry itself, for example, would also include the power supply lines and ESD protection circuits of *Reiner*. But the driver *circuit*, recited in the claims, is the group of circuitry in driver units 70, as I annotated in Figures Ax, Bx, and Cx of my previous declaration.

Murphy II ¶70

See, e.g., Pet'r Reply 17-18; Murphy II ¶¶68-74

## The '157 Patent discloses using a silicon chip instead of forming on an insulating substrate

Further, instead of a polysilicon transistor, an amorphous silicon thin film transistor may be used. Also, instead of a thin film transistor formed on the insulating substrate, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is formed on a crystal silicon wafer.

Ex. 1001, 11:28-33

*See, e.g.,* Pet'r Reply 24

# The Substrate Limitations (claim 8)

# Reiner's flip chip arranges the scanning line driving circuit on a substrate

33. A POSITA would have understood that these descriptions describe conventional flip-chip technology, which is also called “flip chip on glass” or “FCOG,” and is also referred to as “chip on glass” or “COG.” Flip chip refers to directly mounting the IC driver circuit (e.g., Reiner's gate driver 63 and source driver 61) on the glass substrate having the screen pixels. Ex. 1019, Kang, 1<sup>5</sup>

Murphy II ¶33; see also Murphy ¶101

carrier of the TAB tape in fine pitch interconnection. Therefore, the use of chip on glass (COG) technique is proposed for a number of products such as high pixel density and small area LCDs. In this technique, the driver IC is directly mounted on LCD panels by flip chip. Several kinds of COG bonding

Ex. 1019, Kang, 1

terminations with high resolution capabilities. Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD. FCOG and COG offer the highest density possible in packaging. Several interconnect technologies in FCOG/

Ex. 1020, Joshi, 4

technology becomes inevitable. Direct mounting of flip chip onto glass using ACA's (see Figure 1) became the topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.

Ex. 1021, Wu, 20

See, e.g., Pet'r Reply 22-25; Petition 22-23; Murphy ¶101

## Petitioner's expert explains how *Reiner* discloses or renders obvious arranging the scanning line driving circuit on a substrate, such as "flip chip"

145. For example, *Reiner* discloses that FIG. 2 shows integrated circuit 20 (e.g., source driver 61, gate driver 63), including transistors 22, arranged on substrate 21. *Reiner*, 6:18-24. Similarly, the bump bridge(s) of integrated circuit device 20 (e.g., gate drivers 61, 63) allows the integrated circuit device to be arranged on substrate 16 via an interconnection on substrate 16 (not shown). *Reiner*, 7:22-26.

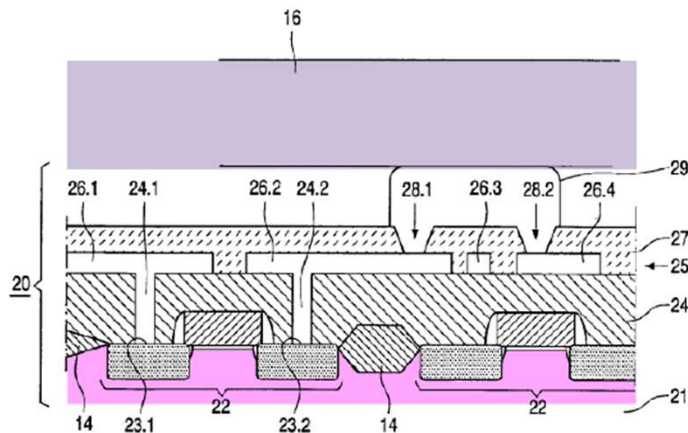


FIG. 2

Murphy ¶145

146. In my opinion, a POSITA would have recognized that substrates 21 or 16 may include, for example, the substrate on which the LCD display 60's scan/gate lines 68, source/data lines 67, and pixels are formed, such as shown in the general schematic of FIG. 4. *Reiner* explains that the driver output devices can be "connected (e.g. by means of bonding)" to their respective display lines via contact pads 72 to drive the lines, which could be patterned on the display's substrate, as shown in *Reiner*'s FIG. 4. *Reiner*, 10:1-6. Thus, *Reiner*'s gate driver 63 is arranged on a substrate to create the LCD display device described in *Reiner*, which the prior art confirms was conventional. *Takahara*, [0001], [0064], FIG. 1; *Murai*, [0001], [0017], FIG. 1; Ex. 1001, 1:57-59 ("FIG. 11 is a view illustrating a configuration of an active matrix substrate of a VGA-LCD using polysilicon TFT by the conventional art."). This known conventionality confirms the POSITA's reading of *Reiner* that the gate driver 63 would be arranged on a substrate when it is bonded at contact pad 72 to the scan lines because the scan lines, as shown in FIG. 4 and conventional in the art, are arranged on the display substrate and so the bonding together also arranges the gate driver 63 on the display substrate.

Murphy ¶146

See, e.g., Petition 44-46

## Petitioner's expert explains that *Reiner's* “flip chip” mounting had known advantages over other technologies

86. Indeed, *flip chip* technology was known to be advantageous for smaller pixel pitch sizes to create higher resolution displays, which *Reiner* itself notes and provides ESD protection for. *Reiner*, 2:7-9, 4:15-16, 12:16-18, FIG. 5; Ex. 1019, *Kang*, 1 (“[T]he use of chip on glass (COG) technique is proposed for a number of products *such as high pixel density and small area LCDs*. In this technique, the driver IC is directly mounted on LCD panels by flip chip.” (emphasis added)); Ex. 1020, *Joshi*, 4 (“Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD. *FCOG and COG offer the highest density possible in packaging*,” and “[i]n COG, the bare (unpackaged) driver ICs are mounted directly on the glass panel. Thus, COG has the potential of using the most simplified assembly process flow and as it does not involve the use of a conventional package (like TCP), it can be a low cost interconnection method.” (emphasis added)); Ex. 1021, *Wu*, 20 (“*With increasing needs for higher resolution displays, higher density interconnect technology becomes inevitable*. Direct mounting of flip chip onto glass using ACA’s (see Figure 1) became the topic of investigation for many Japanese and Korean LCD manufacturers and for Government sponsored programs.” (emphasis added)).

Murphy II ¶86

See, e.g., Pet'r Reply 24-25

## Ground 2: *Reiner and Takahara*

# **Scanning Line Driver Circuit Protection Limitations:**

## **Motivation to Protect Scanning Line Driving Circuit with ESD Protection**

## Prior art: *Takahara*

**[0066]**

The electrostatic-protection circuits 150 and 151 are formed at intermediate locations of the signal wirings 72 and 73. Here, various kinds of circuits may be utilized for the electrostatic-protection circuits 150 and 151; however, the circuit illustrated in FIG. 3, for example, utilizes protection resistors 66, and P-channel TFTs 67 and N-channel TFTs 68, which are in a push-pull layout and constitute diodes between positive power supplies VDD and negative power supplies VSS, respectively. Here, and particularly in the present embodiment, what connects the first short-circuit wiring 91 to the signal wiring 72 (or 73) is between the terminal 800 (or 801, 802) and the protection resistor 66; thereby, static electricity entering from the terminal 800 (or 801, 802) or the first short-circuit wiring 91 does not reach the data-line drive circuit 101 and the scan-line drive circuit 104 unless it passes through the protection resistor 66 and the electrostatic-protection circuit 150 (or 151). With this kind of configuration, static electricity is reliably absorbed by the electrostatic-protection circuit 150 (or 151), and the data-line drive circuit 101 and the scan-line drive circuit 104 can be reliably protected.

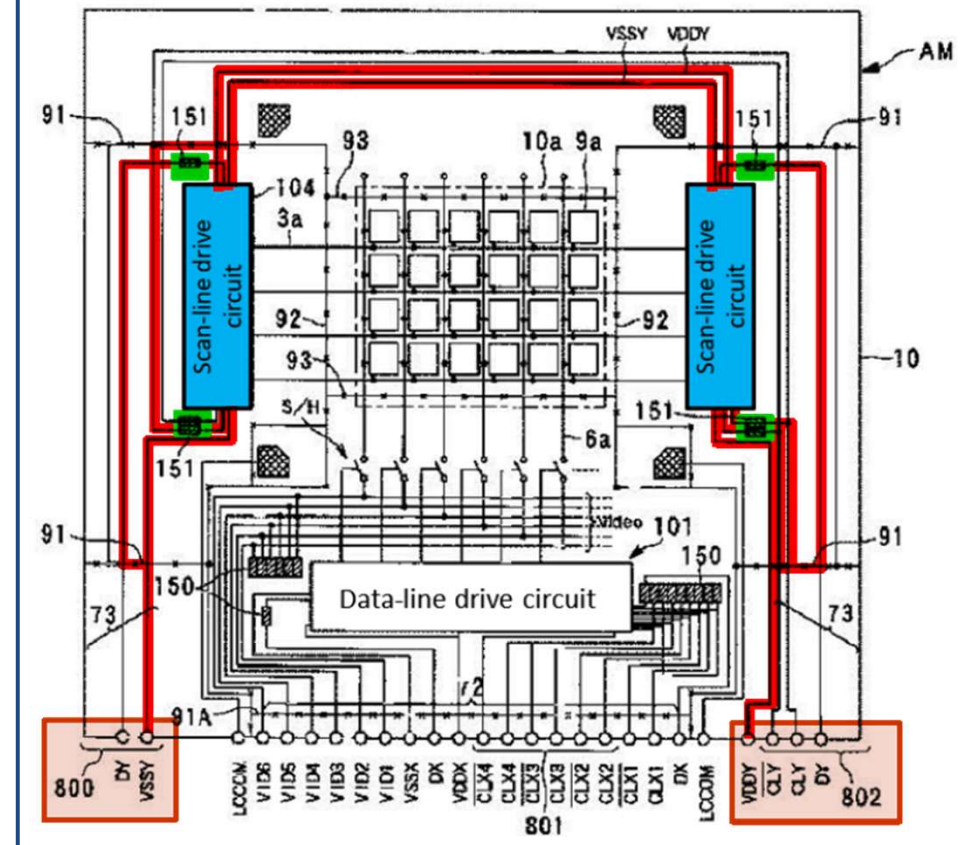
Takahara, [0066]

[0070]

In addition, after the end of the manufacturing process for the active-matrix substrate AM (that is, at shipping at the latest) the existence of these first to third short-circuit wirings 91–93 is, on the contrary, harmful to the normal operation of the device, and therefore they are cut at the locations marked with 'x' in FIG. 1 at an appropriate stage in said manufacturing process. As is described in

Takahara, [0070]

FIG. 1

Murphy ¶235 (annotating *Takahara*, FIG. 1)

*See, e.g.,* Petition 5-6, 76-78

## Petitioner's expert showed it would have been obvious to use ESD protection circuits to protect a scanning line driving circuit as in *Takahara*

236. A POSITA would have found it obvious to protect *Reiner's* gate driver 63 using ESD protection, which *Takahara* confirms, to “reliably protect[]” the “very sensitive circuits” of the driver “from being destroyed when it is subjected to a discharge event.” *Reiner*, 2:28-3:1; *Takahara*, [0066] (“the scanning line driving circuit can be reliably protected”).

Murphy ¶236

[0066], FIGS. 1, 3. A POSITA would have recognized that *Reiner's* “very sensitive circuits” of gate driver 63 are at risk from ESD damage and can be “destroyed when ... subjected to a discharge event,” for at least the reasons explained in Ground 1, claim 4. *Reiner*, 2:28-3:1. A POSITA would have been motivated to “reliably protect[]” the gate driver from ESD damage and prevent the output devices of the gate driver 63 (and thereby protect the gate driver 63) from being damaged by ESD events. For example, *Takahara* discloses that using ESD protection circuits on signal or power lines connected to the scanning line driving unit can “reliably protect[]” the scanning line driving circuit from ESD damage.

Murphy ¶237

238. A POSITA would have been motivated to “protect the circuitry” of the output devices of *Reiner's* gate driver 63 in the same way as source driver 61 to prevent them from being damaged by ESD events because *Takahara* confirms that scanning line drivers can be “reliably protected” by ESD protection circuits in the same way as data line drivers. *Reiner*, 10:10-12; *Takahara*, [0066]. A POSITA also would have been motivated to protect the gate driver 63 and its internal circuits because damage from ESD events could require costly repairs or additional complex manufacturing repair processes or render the display unfit for use. *Reiner*, 10:10-12; *Takahara*, [0066]. A POSITA would have been motivated to provide ESD protection circuits to protect *Reiner's* gate driver 63 because a POSITA would have wanted to protect both driver circuits, as taught by *Takahara*, from ESD damage that can “destroy[]” the “very sensitive circuits” inside of the drivers, which could render the LCD display unacceptably or irreparably damaged and unfit for use by ESD events at either the gate driver (scanning line driving circuit) or the source driver (data line driving circuit). *Reiner*, 2:28-3:1; *Takahara*, [0066].

Murphy ¶238

See, e.g., Petition 76-80; Murphy ¶¶236-242

## Petitioner's expert showed it would have been obvious to use *Reiner's* ESD protection circuits to protect a scanning line driving circuit as in *Takahara*

240. A POSITA would have also recognized that using the “ESD protection network” of *Reiner's* FIG. 5 to protect “each output device” of the gate driver 63 (the driver unit equivalent to output device 70 for each scan line) merely implements *Reiner's* known prior-art ESD protection network to yield the predictable result of “protect[ing] the circuitry inside the [output] device[s]” of gate driver 63, which *Takahara* confirms can be protected by ESD protection circuits and was “conventional art” as admitted by the '157 patent. *Reiner*, 4:15-16, 10:10-12; *Takahara*, [0066], FIGS. 1, 3; Ex. 1001, 1:25-2:30. Similarly, a POSITA would have been motivated to implement *Reiner's* known ESD protection technique to protect gate driver 63 in the same way as the example in FIG. 5, and *Takahara* confirms that such protection is beneficial and was conventional in the prior art. See *Reiner*, 2:28-3:1. At a minimum, a POSITA would have found it obvious to try implementing *Reiner's* ESD protection network shown in FIG. 5 to protect gate driver 63 and its many output devices, given *Reiner's* suggestion that both source driver 61 and gate driver 63 are “integrated circuits” and contain “very sensitive circuits” can be “destroyed” by electrical or thermal ESD damage when ... subjected to [an ESD] discharge event.” *Reiner*, 2:28-3:1, 9:12-14; see also *Takahara*, [0066], FIG. 1 (confirming that both scanning line driving circuits and data line driving circuits can be protected by ESD protection circuits).

Murphy ¶240

241. A POSITA also would have been motivated to implement a first and second ESD protection circuit connected to *Reiner's* gate driver 63, in the configurations described above in Ground 1, claim 4, to protect *Reiner's* gate driver 63 from ESD events both electrically and thermally, and also connected to the power supply line, such as Vss and/or Vdd, for the reasons set forth in Ground 1, claim 4. *Reiner*, 4:10-12, 9:16-22, 4:15-19, 12:15-18, claim 11.

Murphy ¶241

See, e.g., Petition 76-80; Murphy ¶¶236-242

# Takahara's short circuit wiring 91 connect VDDY/VSSY to the scanning line driving circuit 104 via ESD protection 151

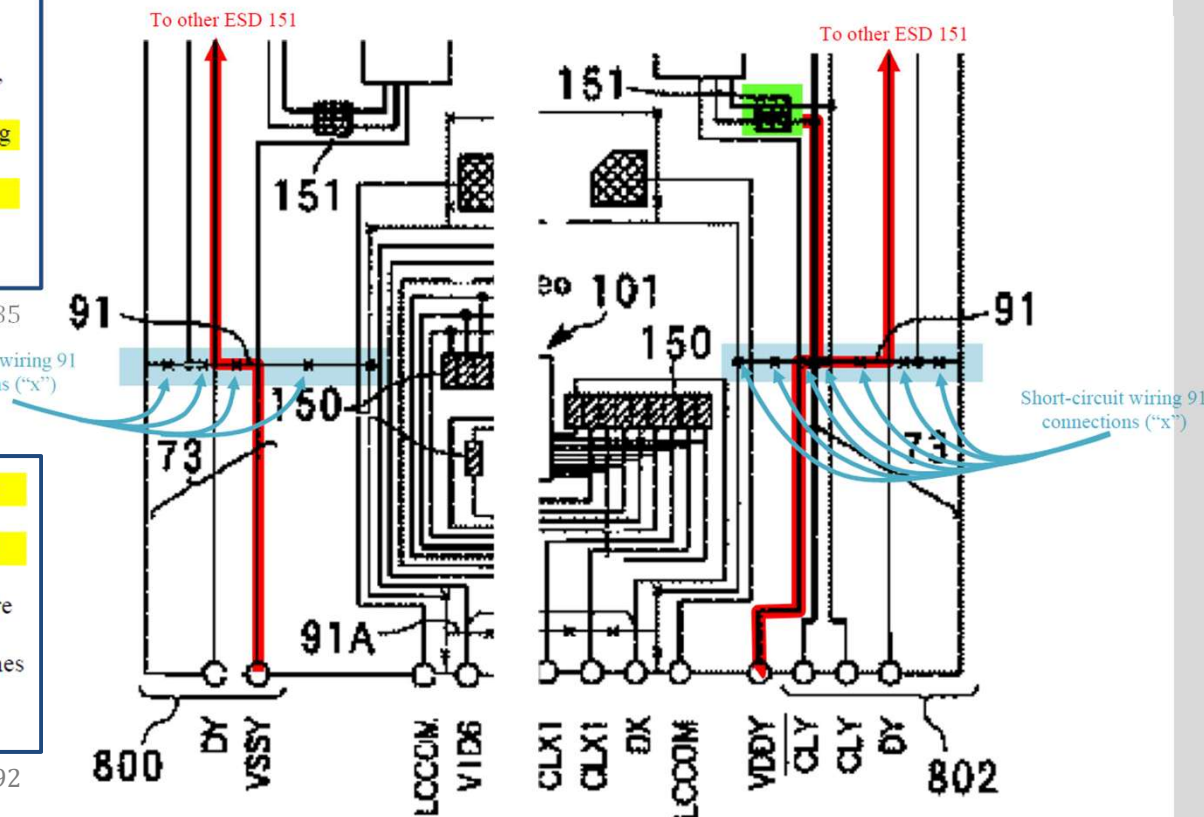
235. Takahara discloses that “[e]lectrostatic [ESD] protection circuits 150 and 151 are formed at intermediate positions of the signal lines ... 73,” which include power lines VDDY and VSSY, so that “static electricity is reliably absorbed” and “scan-line drive circuit 104 can be reliably protected.” Takahara, [0066], FIG. 1. Power lines VDDY and VSSY are shorted to the lines containing ESD protection circuits 150 and 151 that protect both ends of the scanning line driving circuit 104 by shorting lines 91. Takahara, [0070].

Murphy ¶235

Short-circuit wiring 91 connections (“x”)

Schubert Declaration ¶¶123-140. Dr. Schubert is incorrect. Takahara marks the short wirings with an “x” and clearly shows connections between the signal and power lines as shown in both FIGS. 1 and 3. I have annotated these below, where the “x” for the short-circuit wiring 91 can clearly be seen such that the power lines VDDY and VSSY are then connected to the ESD protection circuits 151.

Murphy II ¶92

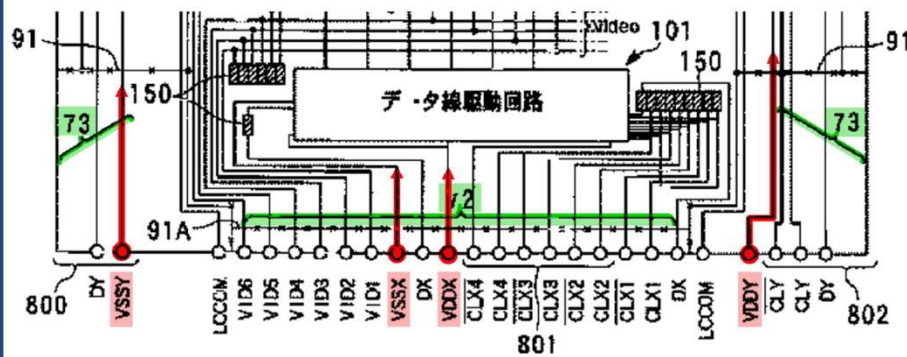


See, e.g., Petition 76-78; Pet'r Reply 26-29, 33-36

# Takahara's signal wirings 72/73 include power lines VDDY/VSSY

101. Quite the contrary to Dr. Schubert's opinions, *Takahara's* FIG. 1

shows that signal wirings VDDY, VSSY, VDDX, and VSSX (annotated red below) are encompassed by signal wirings 72, 73, shown by the brackets (green).



Murphy II ¶101

102. As shown above, *Takahara's* brackets identifying signal wirings 72,

73 (green) clearly encompass power lines VSSY, VSSX, and VDDX (red). A POSITA would have recognized that they also encompass VDDY based on the brackets' positions and directions, either overlapping or facing VDDY, VSSY, VDDX, and VSSX for consistency.

Murphy II ¶102

106. To accept Dr. Schubert's argument, a POSITA would have to *reject*

three teachings shown in (1) the brackets expressly including the power lines

VSSY, VSSX, and VDDX; (2) the bracket that is pointed towards VDDY; and

(3) *Takahara's* disclosure that the "signal wirings" are merely metal films (see

*Takahara*, [0065]). Against these multiple express teachings including the power

lines as part of the signal wirings, Dr. Schubert asks a POSITA to instead assume

that they are all incorrect and should be rejected because the single right-hand

bracket of FIG. 1 is next to and merely pointing towards power line VDDY. A

POSITA would not reject *Takahara's* multiple express disclosures based on the

position of the right-hand bracket 73 in FIG. 1 that is, in fact, pointing towards the

VDDY power line, especially when the other power lines are expressly

encompassed by the brackets and (at a minimum) strongly suggested for VDDY.<sup>13</sup>

Murphy II ¶106

See, e.g., Pet'r Reply 30-33

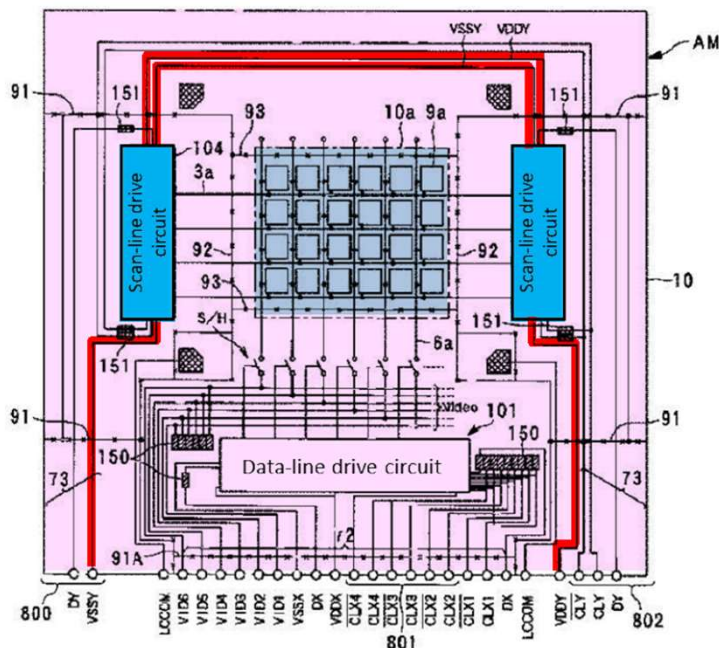
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

# The Substrate Limitations (claim 8)

# Petitioner's expert explained why a POSITA would have been motivated to arrange *Reiner's* scanning line driver on a substrate, such as in *Takahara*

244. *Takahara* discloses that a scan-line drive circuit 104 is arranged on a substrate 10 that also includes the active matrix for the LCD display. *Takahara*, [0064], FIG. 1. The scanning lines 3a and data lines 6a are formed on the substrate 10 and intersect at the active matrix pixel locations, and the scan-line drive circuit 104 and power supply lines VDDY/VSSY are located on the periphery of the substrate 10. *Takahara*, [0062], FIG. 1.

FIG. 1



Murphy ¶244

## i. Motivation

248. A POSITA would have been motivated to arrange *Reiner's* source driver 63 on a substrate to support the LCD display device of *Reiner's* FIG. 4 and provide locations for wiring and circuitry, as disclosed by *Takahara* and well known and conventional in the art. *Reiner*, for example, discloses the driver unit having a silicon substrate 21 and being bonded to the driven lines (e.g., source line or gate line) at contact pad 72. *Reiner*, 6:18-24, 10:1-6, FIGS. 4, 5. A POSITA would have been motivated to arrange *Reiner's* gate driver 63 and active matrix on a substrate and to connect the gate driver to the scan lines being drive on the substrate to provide an integrated display unit (e.g., *Reiner* FIG. 4) that can be incorporated into electronic devices as a display for a laptop computer, PDA, television, computer monitor, cellular phone screen, or other device. *Takahara*, [0064]. A POSITA also would have been motivated to arrange the gate driver on a substrate to provide external terminals to power the active matrix and the driver circuits, such as to connect to the CPU and power sources, such as an external power supply or battery of the electronic device. *Takahara*, [0064].

Murphy ¶248

See, e.g., Petition 81-89; Murphy ¶¶243-252

# Appendix

# Claim 1

1. A display device, comprising:
  - a scanning line driving circuit;
  - a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
  - an input terminal connected to the power supply line to supply power;
  - a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line;
  - a plurality of scanning line driving unit circuits included in the scanning line driving circuit, the plurality of scanning line driving unit circuits being connected to the power supply line; and
  - a third protection circuit connected to the power supply line between a first scanning line driving unit circuit of the plurality of scanning line driving unit circuits and a second scanning line driving unit circuit of the plurality of scanning line driving unit circuits, the first scanning line driving unit circuit and the second scanning line driving unit circuit being adjacent to each other,

the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

## Claims 2-3

2. The display device as set forth in claim 1, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

3. An electronic device provided with the display device as set forth in claim 1.

## Claim 4

4. A display device, comprising:  
a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and  
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

## Claim 5-7

- 5. The display device as set forth in claim 4, further comprising:
  - a scanning line driving unit circuit included in the scanning line driving circuit.
- 6. The display device as set forth in claim 4, further comprising:
  - a buffer circuit included in the scanning line driving circuit.
- 7. The display device as set forth in claim 4, further comprising:
  - a transistor included in the scanning line driving circuit.

## Claims 8-9

8. The display device as set forth in claim 4, further comprising:

- a substrate,
- the scanning line driving circuit being arranged on the substrate,
- the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,
- the first protection circuit being arranged in the first corner portion of the substrate, and
- the second protection circuit being arranged in the second corner portion of the substrate.

9. An electronic device provided with the display device as set forth in claim 4.

## Claim 10

10. A display device, comprising:  
a circuit element included in a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the circuit element, the first protection circuit and the second protection circuit are connected to the power supply line,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal, and  
the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

## Claim 11-14

11. The display device as set forth in claim 10, further comprising:

a scanning line driving unit circuit included in the scanning line driving circuit, the scanning line driving unit circuit including the circuit element.

12. The display device as set forth in claim 10, further comprising:

a buffer circuit included in the scanning line driving circuit, the buffer circuit including the circuit element.

13. The display device as set forth in claim 10, further comprising:

a transistor included in the scanning line driving circuit, the transistor being the circuit element.

14. The display device as set forth in claim 10, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

15. An electronic device provided with the display device as set forth in claim 10.

## Claim 16

16. A display device, comprising:  
a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the power supply line to protect the power supply line, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and  
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

## Claim 17

17. A display device, comprising:  
a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the power supply line to protect the scanning line driving circuit, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and  
the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.

## Claim 18

18. A display device, comprising:  
a circuit element included in a scanning line driving circuit;  
a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;  
an input terminal connected to the power supply line to supply power; and  
a first protection circuit and a second protection circuit that are connected to the power supply line to protect a part of the circuit element, the first protection circuit and the second protection circuit are connected to the scanning line drive circuit,  
the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the circuit element and the power supply line are connected and (ii) the input terminal so that the first protection circuit is disposed at a position that is on a first side of the scanning line driving circuit, and  
the circuit element being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected so that the second protection circuit is disposed at a position that is on a second side of the scanning line driving circuit.