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Paper 35
Date: December 1, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

IPR2024-00973
Patent 9,184,157 B2

Before GRACE KARAFFA OBERMANN, GEORGE R. HOSKINS, and CHRISTOPHER M. KAISER, *Administrative Patent Judges*.

HOSKINS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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I. INTRODUCTION

Petitioner BOE Technology Group Co., Ltd. filed a Petition (Paper 1, "Pet.") pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of U.S. Patent No. 9,184,157 B2 (Ex. 1001, "the '157 patent"), claims 1–18. We issued an Institution Decision (Paper 9, "Inst. Dec.") granting the petitioned review.

Patent Owner 138 East LCD Advancements Limited then filed a Patent Owner Response (Paper 17, "PO Resp."). Petitioner filed a Reply (Paper 21, "Pet. Reply"). Patent Owner filed a Sur-reply (Paper 24, "PO Sur-reply"). An oral hearing was held on October 8, 2025. *See* Paper 31 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(b)(4) and § 318(a). This Decision is a final written decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of claims 1–18 of the '157 patent. We conclude Petitioner has demonstrated the unpatentability of claims 1, 3–7, 9–13, and 15–18, but not of claims 2, 8, and 14.

II. BACKGROUND

A. Real Parties-in-Interest and Related Proceedings

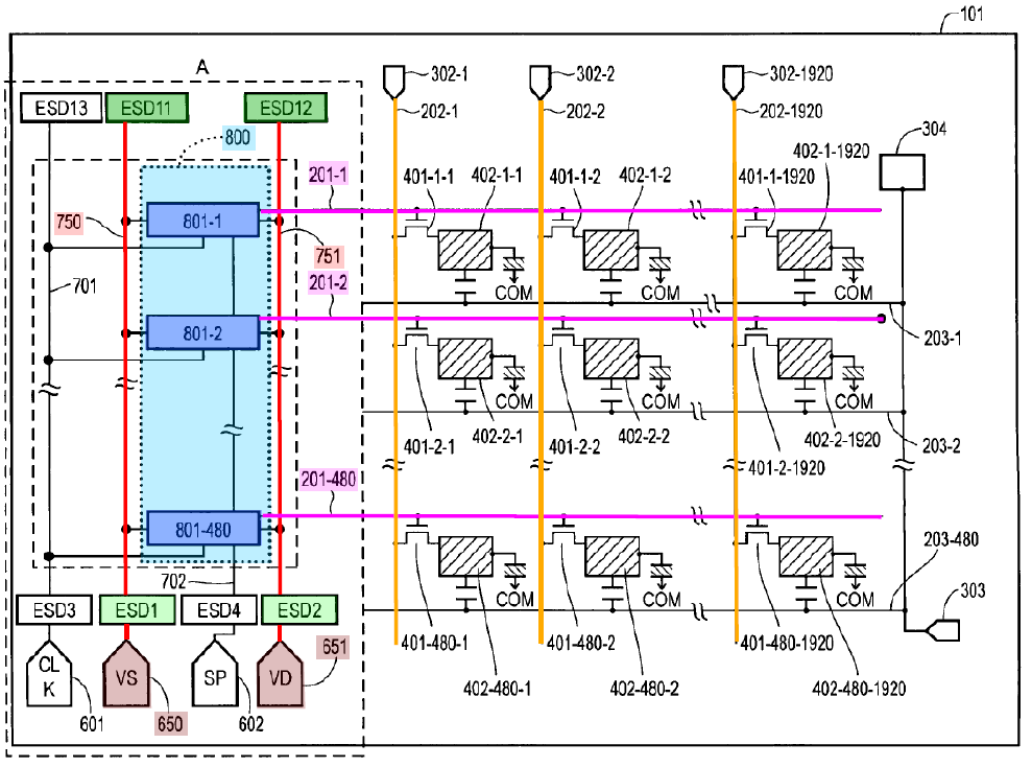
Petitioner identifies itself (BOE Technology Group Co., Ltd.) as its real party-in-interest. *See* Pet. 92. Patent Owner identifies itself (138 East LCD Advancements Limited) and Longitude Licensing Limited as its real parties-in-interest. *See* Paper 19, 1.

The parties also identify *Longitude Licensing Ltd., et al. v. BOE Tech. Group Co., Ltd.*, Case No. 2:23-cv-00515 (E.D. Tex.) ("the District Court Litigation") as a related matter. *See* Pet. 92; Paper 19, 1.

B. The '157 Patent Specification

The '157 patent is directed to a display device with a driving circuit protected from electrostatic damage (ESD) by protective circuits. *See* Ex. 1001, code (57), 1:10–20. Figure 1 of the '157 patent is reproduced below, with our color annotations added.

FIG. 1



'157 Patent, Figure 1 (Annotated in Color).

Figure 1 illustrates active matrix substrate 101 having a built-in scanning line driving circuit 800 (light blue) for supplying drive signals to scanning lines 201-1 through 201-480 (purple) in a liquid crystal display device. *See id.* at 4:30–32, 4:60–66, 5:20–23. The display region of substrate 101 also has data lines 202-1 through 202-1920 (orange) which, together with scanning lines 201 (purple), control pixel elements 401 / 402 (uncolored) to create a display. *See id.* at 4:64–5:19.

Scanning line driving circuit 800 (light blue) is composed of scanning line driving unit circuits 801-1 through 801-480 (dark blue), with one unit circuit 801 provided for each scanning line 201 (purple). *See id.* at Fig. 1, 5:20–28. Each unit circuit 801 (dark blue) is powered by low potential power source line 750 (red) and high potential power source line 751 (also red). *See id.* at Fig 1, 5:28–31. Lines 750 and 751 (red) each receive a voltage supply via respective input terminals 650 and 651 (brown). *See id.* at 5:36–43.

Protective circuits ESD1 and ESD2 (light green) are connected to a connecting line between each input terminal 650 and 651 (brown) and its associated power line 750 or 751 (red). *See id.* at 5:44–51. This "prevent[s] TFTs [thin film transistors] within the scanning line driving circuit 800 from being damaged when the static electricity or noise current is input from" terminals 650 and 651 (brown). *Id.* at 1:34, 5:51–54.

Protective circuits ESD11 and ESD12 (dark green) "are disposed at [the] far end of the opposite side" of scanning line driving circuit 800 (light blue) from input terminals 650 and 651 (brown), on each power line 750 and 751 (red), "with [the] scanning line driving circuit 800 therebetween." *Id.* at 5:55–61. "Thereby, it is possible to suppress that a unit, (for example, n=l, etc.), located far from a terminal [650 or 651 (brown)], among scanning line driving unit circuits 801-n [(dark blue)], is damaged by the static electricity during manufacturing the active matrix substrate." *Id.* at 5:61–65.

The '157 patent describes that its Figure 1 embodiment improves upon the "conventional art" illustrated in Figure 11, which is materially identical to Figure 1 except that it does not have protective circuits ESD11–ESD13 (e.g., dark green) disposed on the opposite side of scanning

line driving circuit 800 (light blue) from input terminals 650 and 651 (brown). *Id.* at 1:43–2:30, Fig. 11. Those additional protective circuits ESD11–ESD13, according to the '157 patent, can be useful when substrate 101 is formed of an insulating material such as glass rather than a conductive material such as silicon, by providing additional and more proximate mechanisms to dissipate electrostatic charges away from circuit 800 (light blue). *See id.* at 1:14–56, 2:33–57, 3:6–11. This same goal can be advanced further by adding more protective circuits between intermediate unit circuits 801 (dark blue) of scanning line driving circuit 800 (light blue). *See, e.g.*, *id.* at 7:17–47 (describing Fig. 2, including protective circuits ESD21 and ESD22 provided between intermediate unit circuits 801-240 and 801-241).

C. The '157 Patent Claims

The '157 patent includes eighteen claims, all of which are challenged here. *See* Ex. 1001, 11:43–15:3; Pet. 15. Claim 4 is illustrative (*see* Pet. 16; PO Resp. 22 & n.3), and it recites with Petitioner's labels [4pre]–[4f] added:

> 4. [4pre] A display device, comprising:
>
> [4a] a scanning line driving circuit;
>
> [4b] a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line;
>
> [4c] an input terminal connected to the power supply line to supply power; and
>
> [4d] a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line,

> [4e] the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal, and
>
> [4f] the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected.

Ex. 1001, 12:25–47; *see also* Pet. (i)–(ii) (Petitioner's labels); PO Resp. 22, 24, 27, 32 (Patent Owner utilizing Petitioner's labels).

D. Asserted Prior Art

Petitioner relies on the following two references as prior art against the '157 patent. *See* Pet. 14–15.

Name	**Reference**	**Exhibit No(s).**
Reiner	WO 03/019657 A2	1005
Takahara	JP 2003-121875 A	1006 & 1007[1]

Patent Owner does not dispute that Reiner and Takahara are prior art against all claims of the '157 patent. *See* PO Resp.

E. Asserted Grounds

Petitioner asserts the following two grounds of unpatentability. *See* Pet. 15.

[1] Exhibit 1006 is the original reference in Japanese, and Exhibit 1007 is an English translation. We cite to the latter in this Decision.

35 U.S.C. §[2]	Reference(s)	Claims Challenged
103(a)	Reiner	1–18
103(a)	Reiner, Takahara	1–18

F. Testimonial Evidence

Petitioner relies on the expert witness testimony of Patrick Murphy, Ph.D. (Exhibits 1003, 1024, and 2008). Patent Owner relies on the expert witness testimony of E. Fred Schubert, Ph.D. (Exhibits 1018 and 2009).

III. PETITIONER'S GROUNDS OF UNPATENTABILITY

A. Legal Standards

1. Petitioner's Burden

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The petitioner must prove unpatentability by a preponderance of the evidence. *See* 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

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[2] Amendments to 35 U.S.C. § 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA") took effect in March 2013. The '157 patent issued from an application filed in May 2009. *See* Ex. 1001, code (22). Therefore, we apply the pre-AIA version of § 103.

2. *Obviousness*

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, if made available in the record which has not happened here. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. *Level of Ordinary Skill in the Art*

The level of ordinary skill in the art is "a prism or lens" through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001). "This reference point prevents . . . factfinders from using their own insight or, worse yet, hindsight, to gauge obviousness." *Id.* at 1355. "The person of ordinary skill in the art is a hypothetical person who is presumed to know the relevant prior art" at the time of invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

In determining the level of ordinary skill in the art, we may consider various factors, including: "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the

technology; and (6) educational level of active workers in the field." *Best Med. Int'l, Inc. v. Elekta Inc.*, 46 F.4th 1346, 1353 (Fed. Cir. 2022).

Petitioner argues a person of ordinary skill in the art pertaining to the '157 patent "would have had at least a Bachelor's degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays," and "[a]dditional relevant work experience can compensate for less education, and *vice versa*." Pet. 15–16; Ex. 1003 ¶¶ 75–77.

Patent Owner proposes a different, three tier formulation of ordinary skill: either [1] "at least *a bachelor's degree* in electrical engineering, computer science, physics, or a similar field and *at least four years* of experience designing semiconductor display devices, including LCD displays"; or [2] *a master's degree* in the same field(s) and *at least two years* of the same experience; or [3] *a Ph.D.* in the same field(s) and *at least one year* of the same experience. PO Resp. 14–15 (emphases added); Ex. 2009 ¶¶ 19–23.

Despite this dispute, neither party leverages its ordinary skill formulation into an argument directly addressing the patentability disputes raised in this case (e.g., by objecting to the opposing expert witness's qualifications, or weighing one witness's testimony more heavily than the other's).

We adopt Patent Owner's first tier formulation of ordinary skill: at least a Bachelor's degree in electrical engineering, computer science, physics, or a similar field and at least four years of experience designing semiconductor display devices, including LCD displays. This is the same as Petitioner's formulation except it increases the requisite years of experience

from two years to four years. *See* Pet. Reply 1. We also conclude additional education can compensate for less work experience and *vice versa* (per both parties' formulations), specifically including the second and third tiers of Patent Owner's proposal. *See id.* (not objecting to Patent Owner's proposed tiers). We further note, however, that adopting Petitioner's formulation in full would not materially affect any of our analyses or determinations below.

Dr. Murphy and Dr. Schubert both have the requisite education and experience to testify from the perspective of an ordinarily skilled artisan per our formulation. *See* Pet. Reply 1; Ex. 1003 ¶¶ 6–15; Ex. 1004; Ex. 1024 ¶¶ 9–12, 15–18; Ex. 2001, Appx. A; Ex. 2009 ¶¶ 5–18; *Kyocera Senco Indus. Tools Inc. v. Int'l Trade Commission*, 22 F.4th 1369, 1375–77 (Fed. Cir. 2022) ("To offer expert testimony from the perspective of a skilled artisan in a patent case — like for claim construction, validity, or infringement — a witness must at least have ordinary skill in the art."); *Osseo Imaging, LLC v. Planmeca USA Inc.*, 116 F.4th 1335, 1340–41 (Fed. Cir. 2024) (holding expert witness may acquire the requisite ordinary skill after the time of the patent's invention).

C. Claim Construction

We interpret the '157 patent claims "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b). This "includ[es] construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." *Id.*

Petitioner argues "no terms need construction to resolve the controversy in this" IPR proceeding. Pet. 14.

"Patent Owner contends that the claims should receive their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art." PO Resp. 14. Patent Owner does not proffer any constructions for particular terms. *See id.*

We discuss the scope of several terms recited in representative claim 4 below, as part of comparing the claim with Reiner. *See infra* Section III.D.2(d)(iii) (claim 4 preamble); Section III.D.2(f)(ii) (limitation [4e], "first connecting portion"); Section III.D.2(g)(ii) (limitation [4f], "driving circuit"); Section III.D.2(i) (limitation [4d] and Petitioner's Mapping C).

Otherwise, based on the arguments and evidence presented, we determine no explicit construction is needed to resolve the parties' controversy. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Ground One — Obviousness over Reiner

In Ground One, Petitioner asserts claims 1–18 of the '157 patent are unpatentable as having been obvious over Reiner. *See* Pet. 1–10, 15, 16–71. Patent Owner disagrees. *See* PO Resp. 1–52.

For reasons that follow, we conclude Petitioner has demonstrated claims 1, 3–7, 9–13, and 15–18 are unpatentable as having been obvious over Reiner, but Petitioner has not demonstrated such unpatentability for

claims 2, 8, and 14. First we summarize Reiner's disclosure, then we consider the parties' contentions.

1. Overview of Reiner

Reiner is directed to an integrated circuit device with bump bridges. *See* Ex. 1005, code (54). Figure 2 shows a first embodiment of Reiner's invention (*see id.* at 6:18),[3] and is reproduced below with our color annotations added.

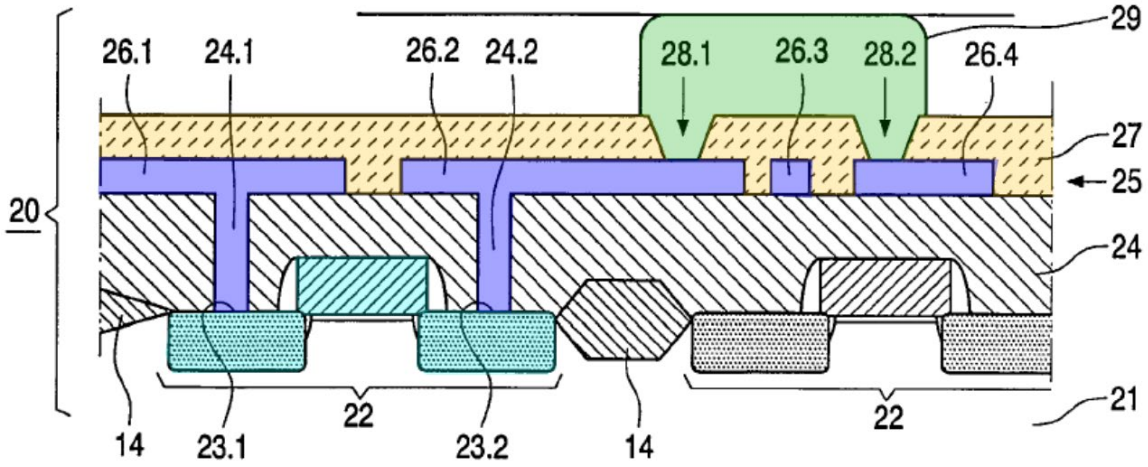


FIG. 2

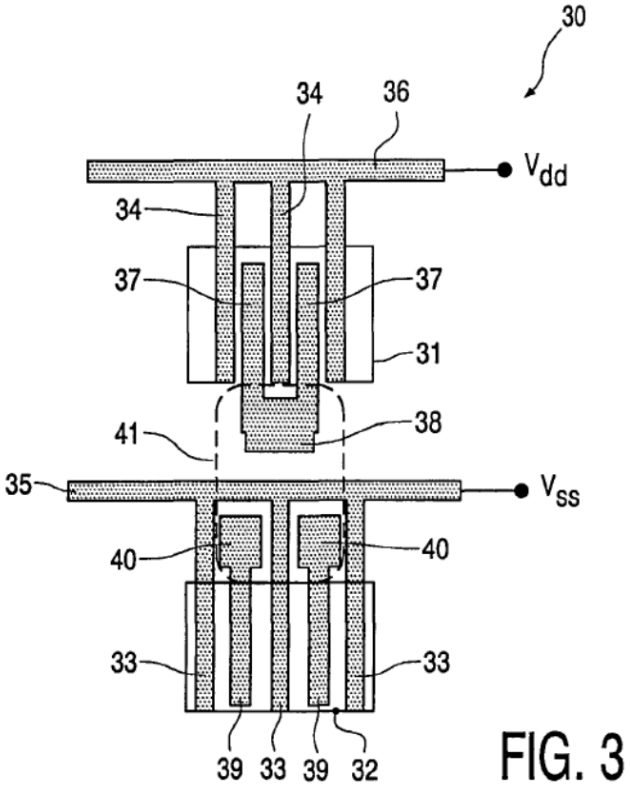
Reiner, Figure 2 (Annotated in Color).

Figure 2 illustrates integrated circuit device 20 comprising silicon substrate 21, integrated devices 22 (light blue), isolating layer 24, metallization level 25 (dark blue), passivation layer 27 (yellow), and bump bridge 29 (green). *See id.* at 6:18–31, 7:12. Bump bridge 29 electrically connects metal lines 26.2 and 26.4, while isolating that connection from metal line 26.3, "to provide for a connection to an ESD [electrostatic

[3] When citing to Exhibit 1005, we refer to the pagination added by Petitioner at the bottom left corner of each page.

discharge] device (not shown in Fig. 2)" that "prevent[s] the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event." *Id.* at 2:28–3:3, 4:12–16, 7:3–18.

Figure 3 of Reiner shows a second embodiment of Reiner's invention (*see id.* at 8:8–11, 8:18–19), and is reproduced below.



Reiner, Figure 3.

Figure 3 illustrates part of integrated circuit device 30 comprising integrated device 31 powered by supply voltage Vdd via metal lines 34 and 36, and integrated device 32 powered by supply voltage Vss via metal lines 33 and 35, wherein devices 31 and 32 are electrically connected to each other by bump bridge 41. *See id.* at 8:18–9:10. This embodiment is "well suited for" incorporating "electrostatic discharge device (ESD) protection" via bump bridge 41 connecting the two devices 31 and 32 "without making any connection to the metal line 35 (Vss)." *Id.* at 8:8–17, 8:31–9:10.

Reiner states its bump bridge technology is "particular[ly] suited" for use with "[i]ntegrated circuit devices [that] have areas where the output or input metal lines have to cross power supply lines." *Id.* at 9:11–18. One example, according to Reiner, is "an integrated circuit display driver 61 or 63 that is designed to drive many lines of an LCD display 60" as shown in Figure 4, because "[s]uch a display driver 61, 63 typically has a large number of parallel outputs." *Id.* at 9:12–15. Figure 4 is reproduced below.

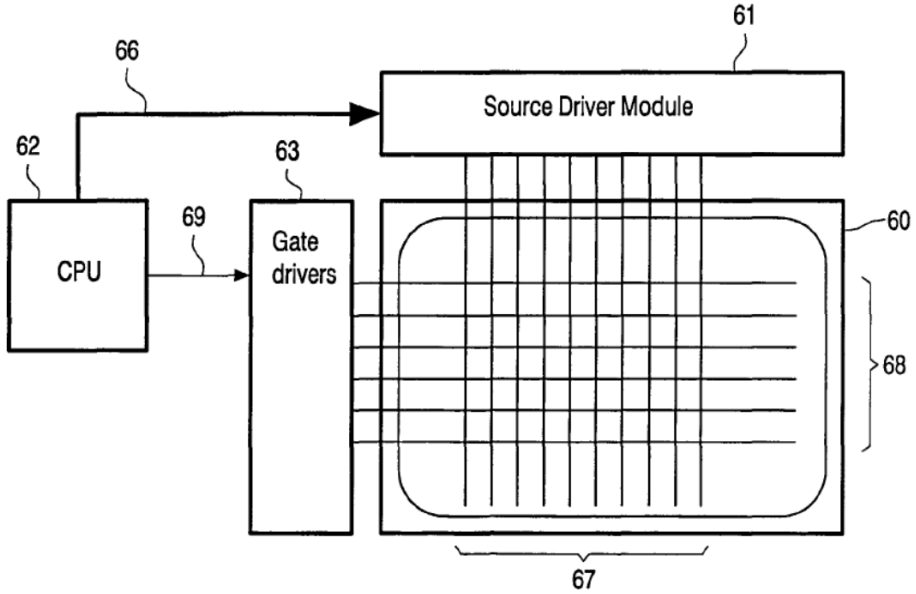


FIG. 4

Reiner, Figure 4.

Figure 4 is a schematic block diagram of an LCD display including: LCD screen 60; source driver 61 which drives source lines 67 in the display; gate driver 63 which drives gate lines 68 in the display; and CPU 62 which controls the scanning of lines 67 and 68. *See id.* at 9:23–34. "The bump bridges allow many output devices of the integrated circuit device 61 or 62

[sic '63'[4]] to cross the power supply lines which provide supply voltage (e.g., Vdd) to the output devices." *Id.* at 9:18–20.

Reiner's Figure 5 is "[a] schematic block diagram of a display driver 61" in which "ESD protection means can easily be integrated." *Id.* at 9:20–22. Figure 5 is reproduced below with our color annotations added.

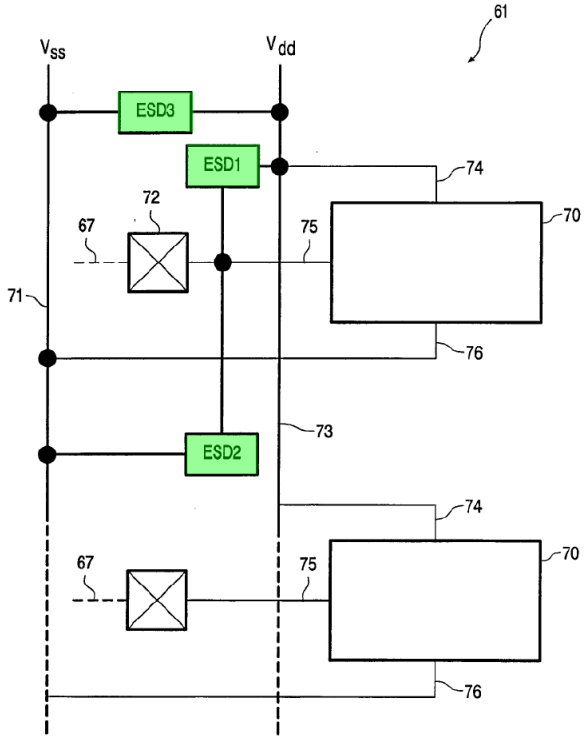


FIG. 5

Reiner, Figure 5 (Annotated in Color).

Figure 5 illustrates source driver module 61 that "comprise[s] several source drivers," and in particular has one output device 70 per each source line 67, to drive the line via output line 75 and contact pad 72. *See id.* at Figs. 4–5, 9:31–10:6 ("There is an array of several parallel output devices 70 (two such output devices are shown in Fig. 5)."). Power supply line 71 provides

[4] We agree with Petitioner's unopposed contention that Reiner's reference to "62" here is a typographical error for "63." *See* Ex. 1005, 9:11–34; Pet. 8 n.4; Ex. 1003 ¶ 56 n.5.

supply voltage Vss through connections 76 to each output device 70, and power supply line 73 provides supply voltage Vdd through connections 74 to each output device 70. *See id.* at 10:7–10. Further: "[T]hree ESD devices ESD1, ESD2, and ESD3 [(green)] are provided for each output device 70" at locations shown in Figure 5, "in order to protect the circuitry inside the devices 70" wherein "to cross some of the lines, bump bridges can be employed." *Id.* at 10:10–23, 14:33–15:21 (claims 12 and 13).

2. Claim 4

Petitioner provides arguments and evidence in support of contending claim 4 is unpatentable as having been obvious over Reiner, including testimony from Dr. Murphy. *See* Pet. 7–10, 16–40; Ex. 1003 ¶¶ 54–56, 88–133. Patent Owner opposes, as supported by testimony from Dr. Schubert. *See* PO Resp. 1–11, 15–42; Ex. 2009 ¶¶ 34–43, 48–84. For the following reasons, we conclude Petitioner has demonstrated claim 4 is unpatentable by a preponderance of the evidence.

(a) [4pre] — The Claim Preamble

The preamble of claim 4 refers to "[a] display device." Ex. 1001, 12:25. Petitioner assumes the preamble is limiting, and contends Reiner discloses a display device as the LCD display shown in Figure 4. *See* Pet. 16–17 (citing Ex. 1005, Fig. 4, 6:7, 9:24–26); Ex. 1003 ¶ 89. We conclude this contention, which Patent Owner does not oppose, is supported by a preponderance of the evidence. In particular, Reiner describes Figure 4 as illustrating "an LCD display" including LCD screen 60 and associated control circuitry. Ex. 1005, 6:7, 9:11–15, 9:23–31; Ex. 1003 ¶ 89.

(b) [4a] — A Scanning Line Driving Circuit

Limitation [4a] recites the display device comprises "a scanning line driving circuit." Ex. 1001, 12:25–26. Petitioner contends Reiner's display device correspondingly includes gate driver 63. *See* Pet. 7, 17–18 (citing Ex. 1005, Fig. 4, 9:11–14, 9:25–31); Ex. 1003 ¶¶ 90–92. We conclude this contention, which Patent Owner does not oppose, is supported by a preponderance of the evidence.

In particular, both expert witnesses testify that: (1) Reiner's *gate* driver 63 is analogous to the *scanning line* driver of Figure 1 in the '157 patent; and (2) Reiner's *source* driver 61 is analogous to the *data line* driver of Figure 1 in the '157 patent. *See* Ex. 1003 ¶ 55; Ex. 2009 ¶ 51 n.2. Therefore, we will refer hereafter to Reiner's gate/scanning driver 63 and source/data driver 61. Further, as discussed below in Sections III.D.2(g)(ii) and III.D.2(j), we find Reiner's scanning line "driving circuit" (specifically) corresponds to the group of output devices 70 in gate/scanning driver 63.

(c) [4b] — A Power Supply Line

Limitation [4b] recites the display device comprises "a power supply line connected to the scanning line driving circuit, the power supply line being one of a low potential power supply line or a high potential power supply line." Ex. 1001, 12:27–30. Petitioner contends Reiner's gate/scanning driver 63 is powered by two power supply lines, respectively conveying a low voltage Vss and a high voltage Vdd. *See* Pet. 19–21 (citing Ex. 1005, Fig. 5, 9:12–14, 9:18–22, 10:7–9, 12:4–5); Ex. 1003 ¶¶ 93–95, 97. We conclude this contention, which Patent Owner does not oppose, is supported by a preponderance of the evidence.

In particular, Reiner discloses that its integrated circuit device 30 (shown in Figure 3) is powered by low voltage power supply line Vss and high voltage power supply line Vdd, and utilizes bump bridge 41 to incorporate ESD protection that avoids a connection to line Vss. *See* Ex. 1005, Fig. 3, 8:8–9:10; *see also* Ex. 1003 ¶ 95 (testifying Vss is a low potential power supply line and Vdd is a high potential power supply line).

Reiner also discusses how its integrated circuit devices utilizing a bump bridge (including device 30 shown in Figure 3) are "particular[ly] suited" for use in *either* source/data driver 61 *or* gate/scanning driver 63. *See id.* at 9:11–20. In this way, Reiner indicates gate/scanning driver 63 is powered by low voltage power supply line Vss and high voltage power supply line Vdd.

However, we disagree with Petitioner's additional argument and Dr. Murphy's testimony that Reiner's Figure 5 "describes" — that is, expressly discloses — gate/scanning driver 63 being powered by lines Vss and Vdd. Pet. 19 (arguing limitation [4b], citing Ex. 1005, 9:18–22); *id.* at 24–25, 26 n.9, 29 (arguing limitation [4d], citing Ex. 1005, Figs. 4–5, 2:2–3, 4:15–16, 9:11–22, 10:10–15, 12:4–5); Ex. 1003 ¶¶ 94, 103–105, 107 n.12, 111. We find, as we did in the Institution Decision, that Reiner's Figure 5 is disclosed as illustrating *only* source/data driver 61. *See* PO Resp. 24 (maintaining this position after institution); Ex. 2009 ¶¶ 63–64; Inst. Dec. 32–33. The Petitioner Reply does not challenge that aspect of the Institution Decision. *See, e.g.*, Pet. Reply 3–21 (argument addressing limitations [4d]–[4f]).

Reiner does disclose, as Petitioner argues, that both of its display drivers 61 and 63 are "typical example[s]" of integrated circuit devices that

can benefit from utilizing Reiner's bump bridge technology for providing electrostatic discharge protection, due to the large number of parallel output lines that must cross power supply lines. *See* Ex. 1005, 4:15–16, 9:11–20 (describing Fig. 4), 12:4–5. However, in contrast to such disclosures that treat Reiner's display drivers 61 and 63 together as a group, Reiner's description of Figure 5 repeatedly refers *only* to Reiner's source/data driver 61. *See id.* at 9:20–10:23. Therefore, we conclude Reiner does not *disclose* that Figure 5 illustrates the structural makeup of gate/scanning driver 63. At the same time, Figure 5's illustration of source/data driver 61 being powered by lines Vss and Vdd is consistent with our finding above, based on disclosures outside of Figure 5 itself, that gate/scanning driver 63 also is powered by lines Vss and Vdd.

For the foregoing reasons, we find Reiner discloses gate/scanning driver 63 is powered by low voltage power supply line Vss and high voltage power supply line Vdd, even though this is not shown in Figure 5 because it is limited to source/data driver 61.

(d) [4c] — An Input Terminal Connected to the Power Supply Line

Limitation [4c] recites the display device comprises "an input terminal connected to the power supply line to supply power." Ex. 1001, 12:31–32.

Petitioner contends Reiner "suggests or renders obvious" limitation [4c]. Pet. 21. We discuss: (i) Petitioner's contentions for utilizing power line input terminals in Reiner; (ii) Petitioner's contentions as to where an ordinarily skilled artisan would have been led to locate the power line input terminals in Reiner; and (iii) Patent Owner's opposition concerning limitation [4c].

(i) Utilizing Power Line Input Terminals in Reiner

Petitioner asserts and Dr. Murphy testifies that a person of ordinary skill in the art "would have understood that [Reiner's] power supply lines 71, 73 would require input terminals . . . so that power can be provided from the power source to the driver units to drive the LCD display 60." Pet. 21; Ex. 1003 ¶ 98. Petitioner also asserts a person of ordinary skill in the art would have been motivated to provide such power line input terminals in Reiner with a reasonable expectation of success, "because it was conventional to do so and because there would need to be an input terminal to create a connection between the power lines Vdd/Vss of the scanning line driving circuit and the power source for the LCD display." Pet. 21–24 (citing Ex. 1001, Fig. 11, 1:54–56, 2:5–14; Ex. 1005, 7:23–25, 9:12–14, 9:18–20, 9:27–29, 10:6–10, 12:4–5; Ex. 1007, Fig. 1, ¶¶ 63, 66); Ex. 1003 ¶¶ 97, 99–102. Dr. Murphy further testifies that utilizing power line input terminals would have been known "to facilitate manufacturing" when "connect[ing] the power supply lines with the corresponding power source or with the power supply lines of the substrate on which the LCD display is arranged." Pet. 23; Ex. 1003 ¶ 101.

Patent Owner does not dispute Petitioner's foregoing contentions and expert witness testimony. *See, e.g.*, PO Resp. 22–24 (argument directed to limitation [4c]); Pet. Reply 1–2.

We conclude a preponderance of the evidence supports Petitioner's contention that a person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner's power supply lines 71-Vss and 73-Vdd, as follows.

Importantly, Reiner does not disclose any particular mechanism or structure for supplying power to its power supply lines 71-Vss and 73-Vdd. Instead, Figure 3 simply illustrates metal line 35 being connected to supply voltage Vss by a thin black line, and metal line 36 being connected to supply voltage Vdd by a thin black line. *See* Ex. 1005, Fig. 3. Reiner's accompanying written description provides no further detail as to how power is supplied to integrated circuit device 30. *See id.* at 8:18–27.

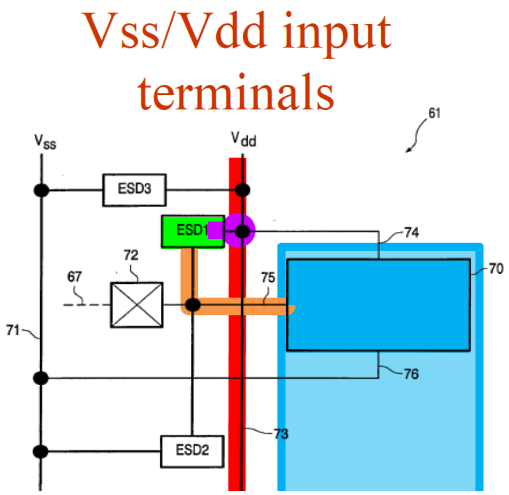
Figure 5 similarly illustrates power supply line 71 being connected to supply voltage Vss, and power supply line 73 being connected to supply voltage Vdd, without providing any further detail as to how power is supplied to line 71-Vss and line 73-Vdd. *See id.* at Fig. 5, 10:7–10.

We are persuaded by Dr. Murphy's testimony that a person of ordinary skill in the art would have been motivated to utilize input terminals to supply power to line 71-Vss and line 73-Vdd which would be required to operate Reiner's display device. *See* Ex. 1003 ¶¶ 97–102; Ex. 2009 ¶¶ 56–61 (Dr. Schubert's testimony directed to limitation [4c] assumes and does not dispute that "Reiner renders obvious input terminals to provide power to lines Vss and Vdd"). Dr. Murphy's testimony is supported by Takahara's disclosure of utilizing input terminals 800 and 802 for supplying power to power lines VSSY and VDDY which lead to scan-line drive circuits 104. *See* Ex. 1007, Fig. 1, ¶¶ 63, 66 (cited at Ex. 1003 ¶¶ 101–102).

Thus, we conclude a person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner's power supply lines 71-Vss and 73-Vdd that power gate/scanning driver 63.

(ii) Where to Locate the Power Line Input Terminals in Reiner

Petitioner further asserts and Dr. Murphy testifies that a person of ordinary skill in the art "would have recognized that the input terminals *would have been [located] above the first ESD3*" in Reiner's Figure 5, because this "was conventional in the prior art."[5] Pet. 22 (emphasis added) (citing Pet. 1–10 (§ II)); Ex. 1003 ¶ 100 (citing Ex. 1003 ¶¶ 49–56 (§ VI)). Dr. Murphy correspondingly annotates a portion of Reiner's Figure 5 to illustrate this contention, as excerpted below. *See* Pet. 28; Ex. 1003 ¶ 110.



Reiner, Figure 5 (Excerpt, Annotated at Ex. 1003 ¶ 110).

This excerpt of Reiner's Figure 5 is a schematic block diagram of source/data driver 61 as annotated by Dr. Murphy, including that the "Vss/Vdd input terminals" would be located above the ends of lines 71-Vss and 73-Vdd. This *location* aspect of Petitioner's contentions is important because, as discussed below in Section III.D.2(f), limitation [4e] specifies a

[5] As found above in Section III.D.2(c), Reiner's Figure 5 depicts source/data driver 61 *not* gate/scanning driver 63. Nonetheless, as discussed below in Section III.D.2(j), we conclude it would have been obvious to protect driver 63 with the same ESD protection network shown in Figure 5 for driver 61.

positional relationship between the power line input terminal and where the first protection circuit and the scanning line driving circuit are connected to the power supply line.

Prior to institution, Patent Owner disputed Petitioner's foregoing contentions as to where to locate the power line input terminals in Reiner. *See* Inst. Dec. 22–23. We concluded the preliminary record justified institution of review on this issue. *See id.* at 23–28.

The Patent Owner Response does not dispute Petitioner's contentions as to where to locate the power line input terminals in Reiner. *See, e.g.*, PO Resp. 22–24 (argument directed to limitation [4c]); Pet. Reply 1–2; Tr. 31:7–26. Therefore, any such argument has been waived. *See* Inst. Dec. 44 ("Any arguments not raised by Patent Owner in a timely-filed response may be deemed waived."); Paper 10, 10 ("Patent Owner is cautioned that any arguments for patentability not raised in the response may be deemed waived.").

On this record, therefore, we conclude a person of ordinary skill in the art would have recognized that the power line input terminals would have been located above the first ESD3 in Reiner's Figure 5, as shown by Dr. Murphy's annotations reproduced above, for the reasons articulated in the Institution Decision. *See* Inst. Dec. 23–28.

The Institution Decision, in part, relied on the conventional art illustrated in Figure 11 of the '157 patent, and cited then-binding Office Guidance concerning use in an IPR proceeding of admissions in the challenged patent. *See* Inst. Dec. 24–25 & n.6. Thereafter, Office Guidance changed such that "applicant admitted prior art (AAPA) . . . may not be used to supply a missing claim limitation," although AAPA "may still be used in

an IPR . . . to demonstrate the knowledge of a person having ordinary skill in the art." USPTO Memorandum, *Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews* (July 31, 2025) (available at https://www.uspto.gov/sites/default/files/documents/aapa_memo_final__signed.pdf) ("New Guidance"), at 1–2.[6]

In our present Decision, we cite the AAPA in the '157 patent as demonstrating the knowledge of a person of ordinary skill in the art (which is permitted by the New Guidance as well as the previous Guidance[7]), not as supplying a missing claim limitation (which is forbidden by the New Guidance). Specifically, we find Figure 11 of the '157 patent illustrates power line input terminals 650 and 651 connected to power lines 750 and 751 at the end of scanning line driving circuit 800 leading to the last driving unit circuit 801-480. *See* Inst. Dec. 24–25 (citing Ex. 1001, Fig. 11, 1:54–56, 1:66–2:15). Limitation [4c] at issue here, by contrast, merely recites "an input terminal connected to the power supply line to supply power" (Ex. 1001, 12:31–32) which would have been obvious over Reiner without the AAPA of the '157 patent as discussed above in Section III.D.2(d)(i).

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[6] The New Guidance is binding on petitions filed on or after September 1, 2025. *See* New Guidance, at 3. The Petition here was filed in June 2024. Nonetheless, the basis for the New Guidance is that the previous Guidance is "no longer consistent with Federal Circuit precedent." *Id.* at 2. Therefore, in an abundance of caution, we consider the New Guidance here.

[7] *See* USPTO Memorandum, *Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311* (June 9, 2022) (available at www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf), at 4.

Limitation [4e] specifies a positional relationship between the input terminal and where the first protection circuit and the scanning line driving circuit are connected to the power supply line. *See* Ex. 1001, 12:38–41. However, we do not rely on the AAPA of the '157 patent as teaching that positional relationship. *See infra* Section III.D.2(f).

Moreover, and alternatively, even if we were to disregard the AAPA of the '157 patent, we would still find the combination of Takahara (Figure 1), Murai (Figure 1), and Reiner (Figure 5) as discussed in the Institution Decision is sufficient evidence to support Petitioner's contentions of obviousness in relation to limitation [4c]. *See* Inst. Dec. 25–28.

(iii) Patent Owner's Opposition Concerning Limitation [4c]

Patent Owner argues that "even if Reiner renders obvious input terminals connected to lines Vdd and Vss," still those terminals "would be input terminals for integrated circuit driver 61" and "would *not* be input terminals for a display device" as required by claim 4. PO Resp. 22–24. In support, Patent Owner asserts and Dr. Schubert testifies that Reiner's "[d]rivers 61 and 63 are not formed on the display substrate (in Reiner, LCD display 60)," and a person of ordinary skill in the art "would understand that the display device would include *separate* power supply lines on the display substrate." *Id.* at 22–23 (citing Ex. 2008, 98:13–99:15, 104:15–105:7); Ex. 2009 ¶¶ 56–61. Further: "Nothing in Reiner suggests that lines Vss and Vdd also supply power to the LCD display 60," and a person of ordinary skill in the art "would understand that LCD display 60 may include separate input terminals for separate power supply lines, because LCD display 60 is

formed on a separate substrate." PO Resp. 23 (citing Ex. 1003 ¶ 101); Ex. 2009 ¶ 60.

We disagree, for two reasons. First, Patent Owner's argument relies on unclaimed subject matter. *See* Pet. Reply 2 n.1 ("Patent Owner's position requires the preamble be limiting, but failed to establish those requirements."). "[T]he mere fact that a structural term in the preamble is part of the claim does not mean that the preamble's statement of purpose or other description is also part of the claim," although the preamble may be limiting in some circumstances. *In re Xencor, Inc.*, 130 F.4th 1350, 1357 (Fed. Cir. 2025). Patent Owner makes no attempt to establish that the "display device" preamble of claim 4 should be limiting. Ex. 1001, 12:25; *see* PO Resp. 22–24.

Second, even if the preamble is limiting, we find Reiner renders obvious a display device that comprises a power line input terminal. Specifically, Reiner describes Figure 4 as illustrating "*a display with display drivers* [61 and 63]" and "*an LCD display with control circuitry*." Ex. 1005, 6:7, 9:23–25 (emphases added); *see* Ex. 1003 ¶ 89; Pet. Reply 3. That is, as described in Reiner, gate/scanning driver 63 is a component of the LCD display shown in Figure 4, because it drives gate lines 68 of LCD screen 60 to generate a display on the screen. *See* Ex. 1005, 9:11–34. LCD screen 60 would not operate without display drivers 61 and 63 and CPU 62. *See id.* at 9:23–10:6. We therefore find that the power line input terminals for supplying power to gate/scanning driver 63 are power line input terminals of the display device, because driver 63 is a component of the display device. *See also* Pet. Reply 2–3 (asserting Patent Owner's "argument turns on the

faulty premise that 'display device' means only the LCD pixels, not the scanning line driving circuits").

Patent Owner's arguments that the claimed power line input terminal must additionally power LCD screen 60, and be formed on the same substrate as LCD screen 60, rely on unclaimed subject matter. In those regards, claim 4 pertinently recites only "[a] display device comprising . . . an input terminal connected to the power supply line to supply power." Ex. 1001, 12:25–32.

(iv) Conclusion Concerning Limitation [4c]

We conclude a person of ordinary skill in the art would have been motivated to utilize input terminals to provide power to Reiner's power supply lines 71-Vss and 73-Vdd that power gate/scanning driver 63 of Reiner's display device, and further would have recognized that the input terminals would have been located above the first ESD3 in Reiner's Figure 5 as shown by Dr. Murphy's annotations reproduced above.

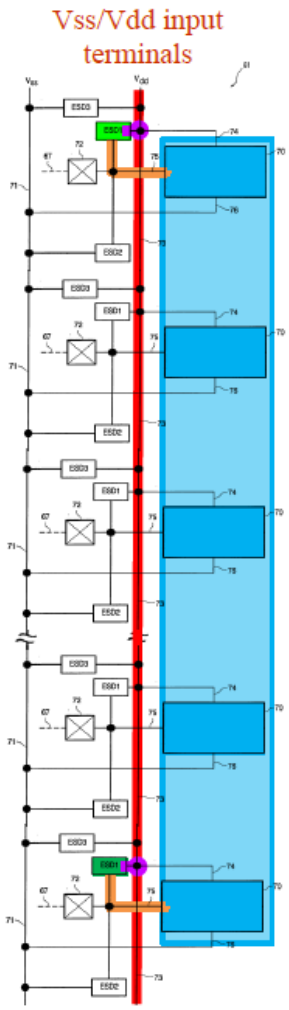
(e) [4d] — First and Second Protection Circuits

Limitation [4d] recites the display device comprises "a first protection circuit and a second protection circuit that are connected to the scanning line driving circuit to protect the scanning line driving circuit, and the first protection circuit and the second protection circuit are connected to the power supply line." Ex. 1001, 12:33–37.

Petitioner contends "Reiner discloses or renders obvious" limitation [4d]. Pet. 24. Petitioner and Dr. Murphy provide three different Mappings A, B, and C of claim 4 to Reiner's Figure 5 that each allegedly demonstrate how the illustrated display driver satisfies limitation [4d]. *See*

Pet. 24–29; Ex. 1003 ¶¶ 103–111. Petitioner also asserts and Dr. Murphy testifies that, in the event Reiner's Figure 5 is found not to illustrate Reiner's gate/scanning driver 63 specifically (as we have done above in Section III.D.2(c)), then it would have been obvious to protect driver 63 with the same ESD protection network shown in Figure 5 for source/data driver 61. *See* Pet. 29–33; Ex. 1003 ¶¶ 112–120.

We find Petitioner's Mapping A demonstrates that the display driver illustrated in Reiner's Figure 5 satisfies limitation [4d] except that it is a source/data driver rather than a gate/scanning driver. In particular, Petitioner's Figure A1, reproduced at right, illustrates Petitioner's Mapping A as it relates to limitation [4d]. *See* Pet. 24–29 (citing Ex. 1005, Fig. 5, 2:2–3, 2:28–3:1, 4:15–16, 8:8–15, 9:11–22, 10:1–17, 12:4–5, 12:23–25); Ex. 1003 ¶¶ 103–111. Figure A1 extends Reiner's Figure 5, which shows only two output devices 70 for driving two lines 67, to include at least three more devices 70 and lines 67 on the basis that a person of ordinary skill in the art would have understood there would be as many devices 70 as there are lines in Reiner's display device. *See* Pet. 26; Ex. 1003 ¶ 107. Patent Owner does not dispute this extension of Reiner's Figure 5.



Petitioner's Fig. A1.

We find the color-coded annotations in Petitioner's Figure A1 identify, per limitation [4d], a first protection circuit (light green, ESD1 at top) and a second protection circuit (dark green, ESD1 at bottom) connected to a driving circuit (light blue, via orange lines) to protect the driving circuit. *See* Ex. 1005, Fig. 5, 2:1–3, 2:28–3:1,

4:15–16, 10:1–17, 12:22–25; Pet. 27–29; Ex. 1003 ¶¶ 108, 110–111. The annotations further identify how both protection circuits are connected to the power supply line 73-Vdd (red, via purple lines). *See* Ex. 1005, Fig. 5, 9:11–22, 10:1–17; Pet. 27–28; Ex. 1003 ¶¶ 108, 110. Patent Owner does not dispute these findings. *See* PO Resp. 27–32 (argument comparing Reiner with limitations [4d] and [4e]).

Thus, we find Petitioner's Mapping A demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4d], except that it is a source/data driver rather than a gate/scanning driver as claimed. We address below how Petitioner's Mapping B demonstrates the same (in Section III.D.2(h)), and why Petitioner's Mapping C is not supported by a preponderance of the evidence (in Section III.D.2(i)). We also address Petitioner's obviousness contentions below (in Section III.D.2(j)).

(f) [4e] — First Protection Circuit's Connection to Power Supply Line

Limitation [4e] recites "the first protection circuit being connected to the power supply line between (i) a first connecting portion at which the scanning line driving circuit and the power supply line are connected and (ii) the input terminal." Ex. 1001, 12:38–41.

Petitioner contends "Reiner discloses or renders obvious" limitation [4e] per Mappings A, B, and C. Pet. 34–36; Ex. 1003 ¶¶ 121–126. Petitioner also asserts and Dr. Murphy testifies that, in the event Reiner's Figure 5 is found not to illustrate Reiner's gate/scanning driver 63 specifically (as we have done above in Section III.D.2(c)), then it would have been obvious to protect driver 63 with the same ESD protection network shown in Figure 5 for source/data driver 61. *See* Pet. 29–33

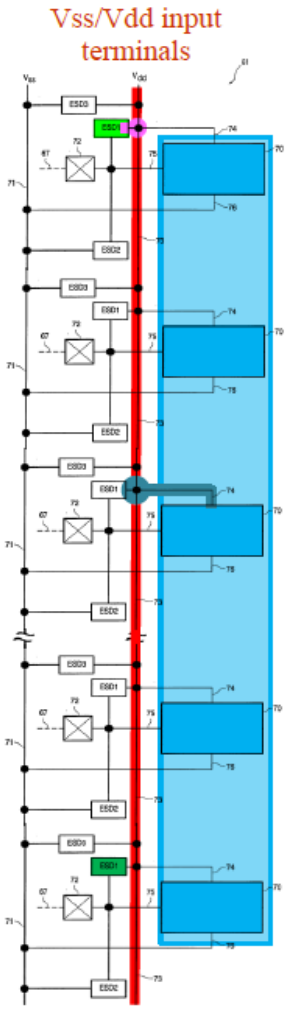
(arguing limitation [4d]), 34 (arguing limitation [4e]); Ex. 1003 ¶¶ 103–111, 122.

For the reasons that follow, we find Petitioner's Mapping A demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4e], except that it is a source/data driver rather than a gate/scanning driver as claimed. We address below how Petitioner's Mapping B demonstrates the same (in Section III.D.2(h)), and why Petitioner's Mapping C is not supported by a preponderance of the evidence (in Section III.D.2(i)). We also address Petitioner's obviousness contentions below (in Section III.D.2(j)).

(i) The Arguments

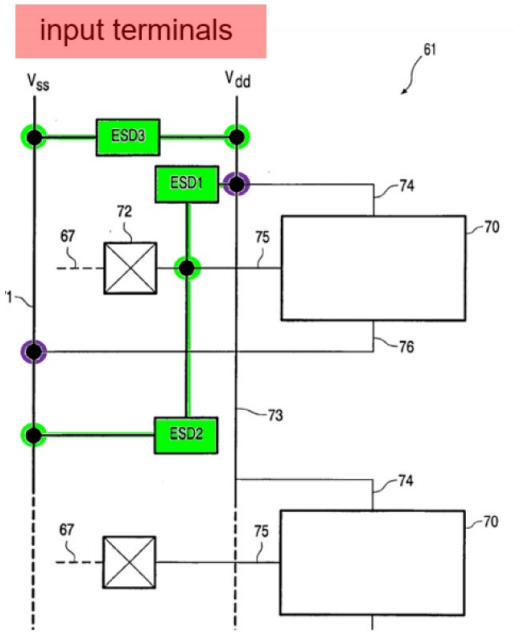
Petitioner's Figure A2, reproduced at right, illustrates Petitioner's Mapping A as it relates to limitation [4e]. *See* Pet. 34–36 (citing Ex. 1005, Fig. 5); Ex. 1003 ¶¶ 121–124. Petitioner asserts and Dr. Murphy testifies that the color-coded annotations in Figure A2 identify, per limitation [4e], a first protection circuit (light green, ESD1 at top) connected to the power supply line 73-Vdd (red, via pink line) between: (i) a first connecting portion (dark teal line 74) at which the scanning line driving circuit (light blue) and the power supply line 73-Vdd (red) are connected; and (ii) the input terminal (brown, at top). *See* Pet. 34–36; Ex. 1003 ¶¶ 121–124.

Patent Owner argues Petitioner's identified "first protection circuit" (light green, ESD1 at top) fails to satisfy the requirement of limitation [4e] of being "connected to the



Petitioner's Fig. A2.

power supply line . . . *between* the scanning line driving circuit's connection to the power supply line and the power supply line input terminal." PO Resp. 27. Instead, according to Patent Owner, the identified "ESD1 is connected to line Vdd *at the same location* at which the source driver *first connects* to line Vdd." *Id.* at 27–28 (second italics added); *see also* Ex. 2009 ¶¶ 73–74 (testifying Petitioner's identified "first protection circuit" is not "*between*, as claimed, [the] power supply line's connection to *any portion* of the scanning line driving circuit and the power supply line's input terminal" (emphasis added)). We reproduce below Patent Owner's annotations to Reiner's Figure 5 to support this argument:



Reiner, Figure 5 (Annotated at PO Resp. 28).

Reiner's Figure 5 is a schematic block diagram of source/data driver 61, which Patent Owner has annotated pertinently to identify Petitioner's alleged first protection circuit per Mapping A (ESD1, green) and where it connects (upper right purple node) to power supply line 73-Vdd (uncolored). *See* PO Resp. 28; Ex. 2009 ¶ 74. That connection point (upper right purple

node) also is where the top-most output device 70 is connected to power supply line 73-Vdd via line 74. *See* PO Resp. 28; Ex. 2009 ¶ 74; Ex. 1005, 10:7–8.

Patent Owner objects to the claim construction underlying Petitioner's Mapping A, whereby the first connecting portion "may be *any* connecting portion at which an output device 70 and line Vdd . . . are connected." PO Resp. 29; Ex. 2009 ¶¶ 71–72. Patent Owner then asserts Petitioner's dark teal line 74 in Figure A2 above cannot be the claimed first connecting portion, because it is "in the middle" of Figure A2. PO Resp. 29–30 (citing Ex. 1003 ¶ 123); Ex. 2009 ¶ 71. According to Patent Owner:

> [Petitioner's] interpretation defeats the purpose of the invention, which places a power supply line protection circuit between that power supply line's input terminal and the power supply line's connection to the scanning line driving circuit, to protect the scanning line driving circuit from charges that could enter the device through the input terminal and travel along the power supply line and damage the scanning line driving circuit.

PO Resp. 31 (citing PO Resp. 2–14 (§ II)); Ex. 2009 ¶ 72. Patent Owner concludes "limitation 4[e] understood in context with limitation 4[f] confirms that claim 4 recites a scanning line driving circuit — *the circuit, not intermediate components of the circuit* — connected between two protection circuits." PO Resp. 31 (emphasis added); Ex. 2009 ¶ 72.

Petitioner replies that Patent Owner applies an incorrect claim construction that excludes "intermediate components of the circuit" from being where the first connecting portion connects to the scanning line driving circuit. Pet. Reply 10 (quoting PO Resp 31). According to Petitioner, limitation [4e] "require[s] only 'a' single 'first connecting portion' connecting the scanning line driving circuit and power line." *Id.*

Petitioner asserts the "comprising" transition term in claim 4 "does not exclude other 'connecting portion[s]'" being part of the claimed invention, and the term "*a* first connecting portion" in limitation [4e] (emphasis added) "means 'one or more'" connecting portions. *Id.* at 11 (citations omitted). Petitioner concludes "any 'connecting portion' between the scan line driving circuit and the power line can be 'a first connecting portion,'" including the dark teal line 74 in Figure A2 above. *Id.*; Ex. 1024 ¶¶ 52–56.

Petitioner asserts its construction of independent claim 4 is confirmed by independent claim 10.[8] *See* Pet. Reply 11–12. Limitation [4e] pertinently recites "a first connecting portion at which *the scanning line driving circuit* and the power supply line are connected." Ex. 1001, 12:39–41 (emphasis added). Claim 10 more particularly recites "*a circuit element included in a scanning line driving circuit*" and "a first connecting portion at which *the circuit element* and the power supply line are connected." *Id.* at 13:6, 13:19–21 (emphases added). Petitioner asserts this confirms that the first connecting portion of either claim "need only be a connection between ***one*** scan line driver unit (e.g., one unit 801-x [in Figure 1 of the '157 patent]) and the power line, not the entire scan line driver (i.e., not all units 801-1 through 801-n)." Pet. Reply 11–12 & n.8 (citing *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001)).

Petitioner further disputes Patent Owner's assertion that the Petition's application of limitation [4e] to Reiner "defeats the purpose of the invention" (PO Resp. 31), because Mapping A instead "align[s] with various

[8] Petitioner also cites independent claim 18 (*see* Pet. Reply 11), but claim 10 is representative of the issues presented.

embodiments in the '157 patent that include additional ESD protection circuits in various combinations." Pet. Reply 12–13 (annotating Figure 2 of the '157 patent); Ex. 1024 ¶¶ 57–59.

Patent Owner replies that "Petitioner manufactures a claim construction dispute to try to save" Mapping A. PO Sur-reply 12. Patent Owner asserts "the plain claim language" of limitation [4e] "recites a first protection circuit connected to the power supply line *between* where the scanning line driving circuit is connected to the power supply line — the scanning line driving circuit *as a whole*, not a component of the scanning line driving circuit — and the input terminal." *Id.* at 14. By contrast, according to Patent Owner, Petitioner's Figure A2 above shows the alleged first connecting portion (dark teal line 74) being located "*after* the location where" the alleged first protection circuit (light green ESD1, at top) is connected to power supply line 73-Vdd. *Id.* at 13 (citing Ex. 1003 ¶¶ 110, 123).

Patent Owner asserts claim 10 supports Patent Owner's claim construction, due to claim differentiation whereby "different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope." *See id.* at 14–15 (citing *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1368–69 (Fed. Cir. 2005)). Patent Owner argues claim 10 recites the "first connecting portion" "in terms of where a circuit element — a *part* of the scanning line driving circuit — is connected to the power supply line." *Id.* Patent Owner contends limitation [4e], by contrast, recites the "first connecting portion" "in terms of where the scanning line driving circuit — not a part of the scanning line driving circuit — is connected to the power supply line." *Id.* at 15. Patent Owner

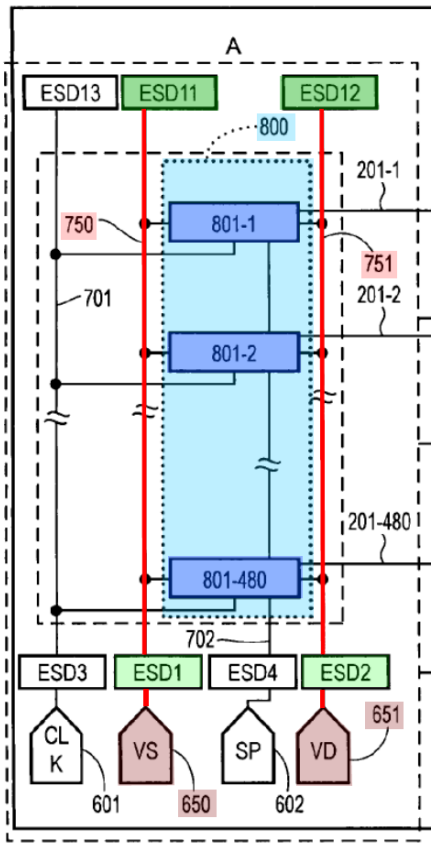
concludes this is confirmed by limitation [4f], which "recites a scanning line driving circuit — the circuit, not intermediate components of the circuit — connected between two protection circuits." *Id.*

Patent Owner further disputes Petitioner's contention that Mapping A aligns with embodiments of the '157 patent. *See id.* at 16–17. Patent Owner argues Petitioner overlooks that Figure 2 of the '157 patent illustrates "ESD protection circuits *at intermediate locations* within the scanning line driving circuit [e.g., ESD21 and ESD22] *and* protection circuits between input terminals and the scanning line driving circuit [e.g., ESD1 and ESD2]." *Id.* at 16 (citing Ex. 1001, Fig. 2, 7:25–34). Patent Owner asserts the former protection circuits do not satisfy the location requirement of limitation [4e], but the latter protections circuits do. *See id.* at 16–17.

(ii) Claim Construction Analysis and Conclusion

Limitation [4e] recites "the first protection circuit being connected to the power supply line between (i) *a first connecting portion at which the scanning line driving circuit and the power supply line are connected* and (ii) the input terminal." Ex. 1001, 12:38–41 (emphasis added).

The claim construction dispute presented here stems from the fact that there can be several "connecting portions" at which a scanning line driving circuit is connected to a power supply line. Figure 1 of the '157 patent, an excerpt of which is reproduced at right with our color annotations added, is representative of the intrinsic evidence. It illustrates scanning line driving circuit 800 (light blue) composed of 480 scanning line driving unit circuits 801-1 to 801-480 (dark blue) for supplying drive signals to scanning lines 201-1 through 201-480. *See* Ex. 1001, 4 :60–66, 5:20–28. Each unit circuit 801 (dark blue) is powered by low potential power source line 750 (red) and high potential power source line 751 (also red). *See id.* at 5:28–31. Specifically, where power source lines 750 and 751 (red) pass by each respective unit circuit 801 (dark blue), there is a "connecting portion" consisting of a horizontal offshoot (black node and line) extending to the unit circuit. *See id.* at Fig. 1.



'157 Patent, Figure 1 (Excerpt, Annotated in Color).

Per limitation [4e], ESD1 (light green) is a first protection circuit connected to power supply line 750 (red) "between" a "first" driving circuit to power line connecting portion and input terminal 650 (brown). *See id.* at Fig. 1, 5:36–51 (describing ESD1 as being "connected to . . . a connecting line between the low potential power terminal 650 and the low potential power source line 750"). Indeed, ESD1 is connected to power supply line 750 "between" *each one* of the 480 driving circuit to power line

connecting portions and power line input terminal 650. *See id.* at Fig. 1. The same is true of ESD2 (light green) with respect to power supply line 751 (red) and power line input terminal 651 (brown). *See id.*

Patent Owner argues we should construe limitation [4e] to require that the first protection circuit is connected to the power supply line between *all* of the driving circuit to power line connecting portions (on one side of the first protection circuit) and the input terminal (on the other side of the first protection circuit). *See, e.g.*, PO Resp. 27 (referring to where Reiner's "source driver *first connects* to line Vdd" (emphasis added)); Ex. 2009 ¶ 73–74 (referring to Reiner's "power supply line's connection to *any portion* of the scanning line driving circuit" (emphasis added)). We disagree, for the following reasons.

First, Patent Owner's construction is not supported by the plain language of limitation [4e]. Patent Owner's construction would replace "a first connecting portion" between the scanning line driving circuit and the power supply line (Ex. 1001, 12:39–41) with "all connecting portions." Figure 1 of the '157 patent does illustrate protection circuits ESD1 and ESD2 being connected to their respective power supply lines between all of the driving circuit to power line connecting portions and the input terminal. However, we must be careful not to read particular embodiment(s) appearing in the '157 patent specification into claim 4 if the claim language is broader than the embodiment(s). *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("particular embodiments appearing in the written description will not be used to limit claim language that has broader effect"); *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) ("[L]imitations are not to be read into the claims from

the specification."). We decline Patent Owner's proposal to do so in this case.

Second, Patent Owner argues and Dr. Schubert testifies that Petitioner's claim construction "defeats the purpose of the invention," which they characterize as "protect[ing] the scanning line driving circuit *from charges that could enter the device through the input terminal*." PO Resp. 31 (emphasis added) (citing PO Resp. 2–14 (§ II)); Ex. 2009 ¶ 72. However, they do not cite any intrinsic evidence to support this contention. *See* PO Resp. 31; Ex. 2009 ¶ 72. The cross-referenced section of the Patent Owner Response does discuss the '157 patent's description of ESD1 and ESD2 in Figure 1 as addressing the "key issue to prevent the damage when a static electricity flows through input terminals" by being "formed between input terminals and the semiconductor device forming a circuit, i.e., immediately after the input terminals." Ex. 1001, 1:23–31 (cited at PO Resp. 5).

However, claim 4 instead broadly refers only to the first protection device being "connected to the scanning line driving circuit to protect the scanning line driving circuit." Ex. 1001, 12:33–35. Claim 4 does not specify a particular location where the first protection circuit must guard against charges entering the device. *See id.* at 12:25–47. Indeed and importantly, limitation [4e] places the first protection circuit between the input terminal and *a first connecting portion* of the scanning line driving circuit, <u>not</u> the scanning line driving circuit itself. *See id.* at 12:38–41. Patent Owner could instead have written limitation [4e] to recite that the first protection circuit is located "between [the] input terminals and the [scanning line driving circuit]" (*id.* at 1:28–30) or "immediately after the input terminals" (*id.* at 1:30–31). Moreover, it would be somewhat anomalous to

construe the scope of limitation [4e] to be limited to the locations of ESD1 and ESD2 shown in Figure 1 of the '157 patent in order to achieve "the purpose of the invention" (PO Resp. 31) when ESD1 and ESD2 are taken from the admitted prior art shown in Figure 11 of the '157 patent (*see id.* at 5–6). Thus, we disagree with Patent Owner's position that limitation [4e] should be construed such that the "first connecting portion" cannot be located at "intermediate components of" the scanning line driving circuit. PO Resp. 31.

As a result, we agree with Petitioner's position that in Figure 2 of the '157 patent, the intermediate protective circuits ESD21 and ESD22 satisfy the first protection circuit requirements of limitation [4e]. That is, protective circuits ESD21 and ESD22 both are connected to their respective power supply line 750 or 751 "between" the respective connecting portions for unit circuit 801-240 and their respective input terminal 650 or 651. *See* Ex. 1001, Fig. 2, 7:17–47; Ex. 1024 ¶ 58 (first annotated version of Fig. 2, focusing on ESD21). Indeed, the '157 patent describes Figure 2 as showing how ESD21 and ESD22 "are provided *between* the unit driving circuit 801-240 at the 240th stage, which is *an intermediate stage of the driving circuit 800*, and the unit driving circuit 801-241 at the 241st stage" in order "to suppress the damage caused by static electricity in the vicinity of the intermediate stage (n=240), which is *far from both the vicinity of the terminal [650 or 651]* and the far end of the terminal." Ex. 1001, 7:30–38 (emphases added). Thus, Petitioner's construction of limitation [4e] does not defeat the purpose of the '157 patent, as Patent Owner would have it.

Third, we agree with Petitioner that claim 10 similarly supports its construction of claim 4. Claim 4 recites "a scanning line driving circuit" and

claim 10 more particularly recites "a circuit element [that is] included in a scanning line driving circuit." Ex. 1001, 12:26, 13:6; *see also id.* at 12:48–51 (claim 5 depends from claim 4 to add a "unit circuit included in the scanning line driving circuit" similar to the "circuit element" of claim 10). Claim 10 indicates one example of "a first connecting portion at which the scanning line driving circuit and the power supply line are connected" per claim 4 is a connection to a particular "circuit element" (e.g., one of the 480 unit circuits 801 in Fig. 1) of the scanning line driving circuit (e.g., circuit 800 in Fig. 1). *Id.* at 12:39–41, 13:19–21. Thus, claims 4 and 10 recite the same language ("scanning line driving circuit") rather than different language as Patent Owner would have it, and claim 10 establishes that the "first connecting portion" of claim 4 may be satisfied by connecting to any one of the circuit elements in the scanning line driving circuit.

Fourth, to the extent Patent Owner's claim construction is premised on the term "*first* connecting portion" (Ex. 1001, 12:39 (emphasis added)) being limited to the connecting portion at one *end* of the scanning line driving circuit, such as unit circuit 801-1 or 801-480 of scanning line driving circuit 800 in Figure 1, we disagree. Claim 4 as a whole recites three connecting portions: a "first" connecting portion between the power supply line and the scanning line driving circuit; a "second" connecting portion between the power supply line and the first protection circuit; and a "third" connecting portion between the power supply line and the second protection circuit. *Id.* at 12:38–47. Thus, the "first," "second," and "third" terms differentiate between different components being connected to the power supply line, rather than "first" referring to one end of the scanning line driving circuit.

Fifth, to the extent Patent Owner's construction of limitation [4e] relies on Patent Owner's arguments concerning limitation [4f], we address those arguments below in Section III.D.2(g).

In conclusion, we reject Patent Owner's claim construction of limitation [4e] that would require the first protection circuit to be connected to the power supply line between *all* of the connecting portions at which the scanning line driving circuit and the power supply line are connected (on one side of the first protection circuit) and the input terminal (on the other side of the first protection circuit). We instead construe limitation [4e] to permit the first connecting portion to be connected to an intermediate component of the scanning line driving circuit, such as (for example) one of the intermediate unit circuits 801-n of scanning line driving circuit 800 shown in Figure 1 of the '157 patent.

(iii) Comparing Reiner with Limitation [4e] Per Petitioner's Mapping A

We find the color-coded annotations in Petitioner's Figure A2, reproduced above, demonstrate how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4e], except that it is a source/data driver rather than a gate/scanning driver as claimed. That is, the illustrated display driver includes a first protection circuit (light green, ESD1 at top) connected to the power supply line 73-Vdd (red, via pink line) between: (i) a first connecting portion (dark teal line 74) at which the scanning line driving circuit (light blue) and the power supply line 73-Vdd (red) are connected; and (ii) the input terminal (brown, at top).

To the extent Patent Owner disputes these findings, Patent Owner's argument is premised on a construction of limitation [4e] that we have rejected above.

(iv) Conclusion Concerning Limitation [4e]

We conclude Petitioner's Mapping A demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4e], except that it is a source/data driver rather than a gate/scanning driver as claimed.

(g) [4f] — Driving Circuit's Connection to Power Supply Line

Limitation [4f] recites "the scanning line driving circuit being connected to the power supply line between (iii) a second connecting portion at which the first protection circuit and the power supply line are connected and (iv) a third connecting portion at which the second protection circuit and the power supply line are connected." Ex. 1001, 12:42–47.

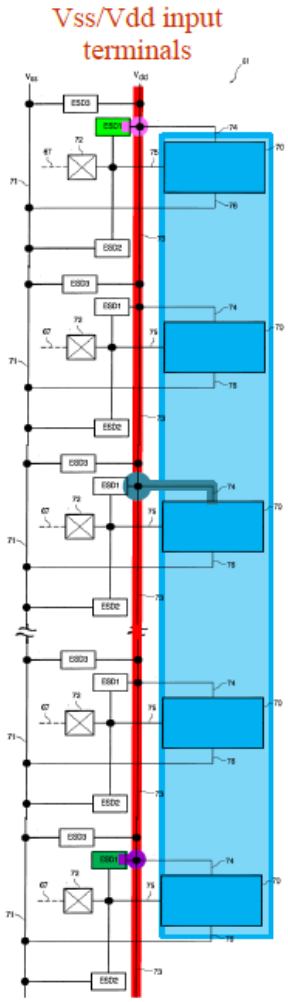
Petitioner contends "Reiner discloses or renders obvious" limitation [4f] per Mappings A, B, and C. Pet. 37–40; Ex. 1003 ¶¶ 127–132. Petitioner also asserts and Dr. Murphy testifies that, in the event Reiner's Figure 5 is found not to illustrate Reiner's gate/scanning driver 63 specifically (as we have done above in Section III.D.2(c)), then it would have been obvious to protect driver 63 with the same ESD protection network shown in Figure 5 for source/data driver 61. *See* Pet. 29–33 (arguing limitation [4d]), 37 (arguing limitation [4f]); Ex. 1003 ¶¶ 103–111, 128.

For the reasons that follow, we find Petitioner's Mapping A demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4f], except that it is a source/data driver rather than a

gate/scanning driver as claimed. We address below how Petitioner's Mapping B demonstrates the same (in Section III.D.2(h)), and why Petitioner's Mapping C is not supported by a preponderance of the evidence (in Section III.D.2(i)). We also address Petitioner's obviousness contentions below (in Section III.D.2(j)).

(i) The Arguments

Petitioner's Figure A3, reproduced at right, illustrates Petitioner's Mapping A as it relates to limitation [4f]. *See* Pet. 37–39 (citing Ex. 1005, Fig. 5); Ex. 1003 ¶¶ 127–130. Petitioner asserts and Dr. Murphy testifies that the color-coded annotations in Figure A3 identify, per limitation [4f], the driving circuit (light blue) connected to the power supply line 73-Vdd (red, via dark teal line 74) between: (iii) a second connecting portion (pink line) at which the first protection circuit (light green, ESD1 at top) and the power supply line 73-Vdd (red) are connected; and (iv) a third connecting portion (purple line) at which the second protection circuit (dark green, ESD1 at bottom) and the power supply line 73-Vdd (red) are connected. *See* Pet. 37–39; Ex. 1003 ¶¶ 127–130.



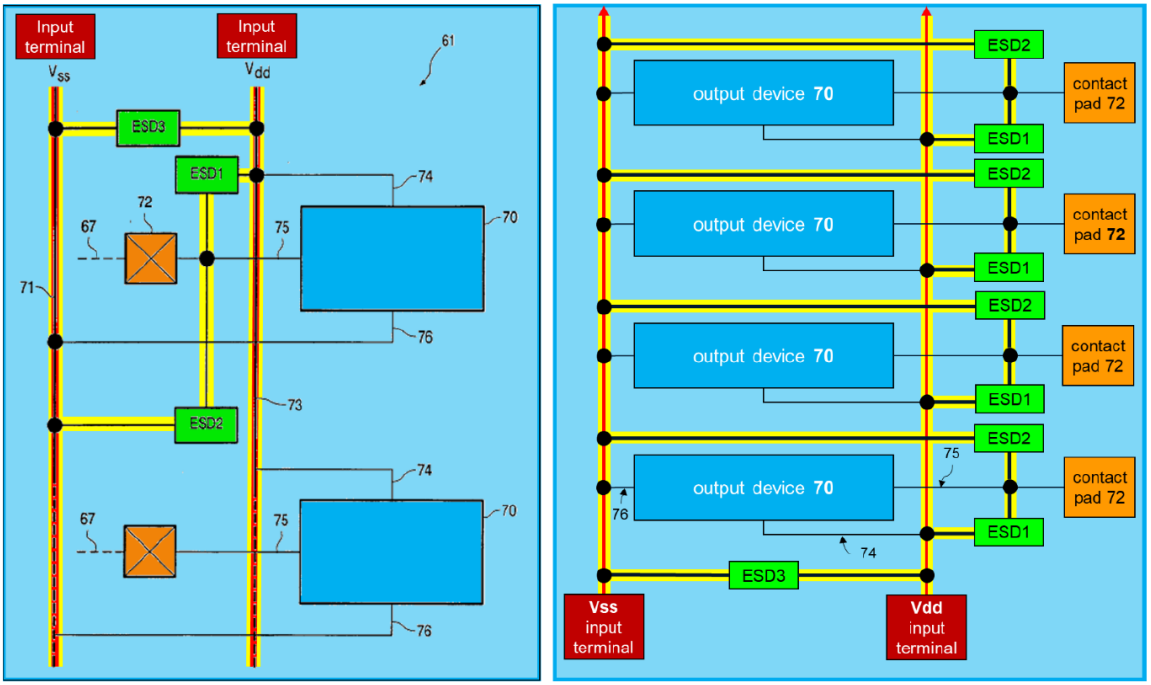
Petitioner's Fig. A3.

Patent Owner argues Reiner does not disclose a "driving circuit connect[ed] to a power supply line *between* the protection circuit connecting portions" as required by the "plain language" of limitation [4f]. PO Resp. 32–33. Instead, according to Patent Owner, "Reiner teaches an integrated circuit including an internal

ESD protection network . . . *in* an integrated circuit" and "Reiner's ESD protection network is *inside* its purported scanning line driver, to protect individual output devices 70." *Id.* (citing Ex. 2008, 139:3–10); Ex. 2009 ¶¶ 75–77.

In support, Patent Owner argues Reiner represents the conventional art described in the '157 patent, upon which claim 4 improves. *See* PO Resp. 33. That conventional art, as described by Dr. Schubert, corresponds to "ESD devices connected between each input/output (i.e., entry point into the integrated circuit, here, the Vss and Vdd input terminals and each contact pad 72) and the integrated circuit's output devices 70." PO Resp. 32, 33–34 (citing Ex. 1001, Fig. 11, 1:14–19, 1:23–28, 1:48–54, 2:25–28; Ex. 1005, Fig. 5, 3:4–8; Ex. 2008, 56:13–57:21); Ex. 2009 ¶¶ 76, 78–79.

We reproduce below Dr. Schubert's supporting illustrations:



Reiner Figure 5 (At Left, Annotated by Dr. Schubert) and Redrawing of Reiner Figure 5 (At Right) (Ex. 2009 ¶ 80).

Here, Dr. Schubert annotates Figure 5 of Reiner (at left) and a redrawing of the same figure (at right) oriented for comparison to Figure 11 of the '157 patent. *See* PO Resp. 35–36; Ex. 2009 ¶ 80. Dr. Schubert testifies that the redrawn figure at right demonstrates Reiner "teaches ESD protection between input/outputs of the source driver 61 device to protect output devices 70 of source driver 61," like the conventional art of the '157 patent. PO Resp. 35; Ex. 2009 ¶ 80. Specifically, according to Dr. Schubert: ESD1 and ESD2 (green) protect their associated output device 70 (dark blue) from electrostatic discharge entering integrated circuit device 61 (light blue) via contact pad 72 (orange); and ESD3 (green) protects all of the output devices 70 (dark blue) from electrostatic discharge entering integrated circuit device 61 (light blue) via the Vss or Vdd input terminal (dark red). *See* PO Resp. 36–40 (citing Ex. 1005, Fig. 5, 10:12–20; Ex. 2008, 107:21–108:16, 111:16–22, 122:7–9, 134:10–18); Ex. 2009 ¶¶ 80–83.

Thus, Patent Owner concludes and Dr. Schubert testifies that "each of Reiner's ESD devices . . . are *inside* integrated circuit source driver 61 [(light blue)] between access points (terminals [(dark red)] and contact pads 72 [(orange)])," and rely on low-ohmic paths (yellow) *inside* integrated circuit source driver 61 (light blue) to shunt electrostatic discharges away from output devices 70 (dark blue). PO Resp. 40 (emphasis added) (citing Ex. 1005, 3:4–8); Ex. 2009 ¶ 84. Patent Owner asserts Dr. Murphy ignores this disclosure in Reiner. *See* PO Resp. 40 (citing Ex. 2008, 119:16–19, 124:15–21, 125:1–6, 127:2–6).

Patent Owner argues limitation [4f] "recites a scanning line driving circuit connected to the power supply line *between two protection circuit connections to that power supply line*." *Id.* at 41 (citing Ex. 1001, 3:12–17).

Reiner, per Patent Owner's contrast, "does not disclose a driver that is connected to a power supply line *between protection circuits*" and instead "discloses only the prior art: an integrated circuit including internal ESD protection device[s] near each input/output terminal." PO Resp. 41; Ex. 2009 ¶ 84. This is demonstrated, in Patent Owner's view, by Petitioner's Figure A3 showing "driver 61 connected to line Vdd *at* ESD1 connecting portions (not between)." PO Resp. 41–42.

Petitioner replies that Patent Owner's argument concerning limitation [4f] "relies on the same incorrect interpretation refuted above [in relation to limitation [4e]] that all scanning line driver connections must be between the two protection circuit connections." Pet. Reply 14, 21. Petitioner also argues "Patent Owner agrees that Reiner's ESD1 and ESD2 protect the driver circuits 70 at least from electrostatic discharge entering through the signal lines," which "is all claim 4 requires." *Id.* at 16–17 (citing PO Resp. 36–39); Ex. 1024 ¶¶ 66–67.

Petitioner also disputes Patent Owner's assertion that Reiner's ESD devices are "inside integrated circuit source driver 61 between access points." Pet. Reply 17 (quoting PO Resp. 39–40). According to Petitioner, "Patent Owner misstates Dr. Murphy's testimony where he was asked about a 'driver ***module***'" which "may include more than the 'driving circuit' recited in claim 4 . . . such as the power lines and ESD1–ESD3 protection circuits" in Reiner's Figure 5. *Id.* at 17–18 (citing PO Resp. 20–21, 23, 33); Ex. 1024 ¶ 70. Petitioner asserts the claimed "driving circuit" in Reiner "is the group of driver units 70" as identified by the light blue box in Petitioner's Figures A1–A3 above. Pet. Reply 18; Ex. 1024 ¶¶ 68–69. Petitioner argues Patent Owner "engages in arbitrary line drawing to allege

[Reiner's] driver circuit also includes protection circuits ESD1–ESD3," and "regardless of where the 'box' is drawn, there is no difference in structure or operation." Pet. Reply 18–20 (citing PO Resp. 39–40; Ex. 2008, 179:5–180:17); Ex. 1024 ¶¶ 68–74.

Petitioner moreover argues that the '157 patent's conventional art has "one single ESD at the input terminal" for each power supply line, whereas Reiner has "numerous additional ESD1–ESD3 at each driver unit" along each power supply line. Pet. Reply 14–15 (citing Dr. Schubert's illustrations at Ex. 2009 ¶ 80); Ex. 1024 ¶¶ 62–65. In Petitioner's view, Patent Owner mischaracterizes the '157 patent's conventional art as protecting "access points" or "inputs/outputs," because the conventional art instead has "only one ESD protection circuit at the input terminals." Pet. Reply 12 n.9 (citing Ex. 1001, Fig. 11, 1:47–2:32); *id.* at 20–21; Ex. 1024 ¶ 65.

Patent Owner responds that "Petitioner does not dispute that Reiner does not disclose a driver that is connected to a power supply line between protection circuits" or that "Reiner discloses only the prior art: an integrated circuit including [an] internal ESD protection device near each input/output terminal." PO Sur-reply 2. According to Patent Owner, "Petitioner concedes [those] limits of Reiner's teachings and instead argues that claim 4 is broad enough to cover a layout in which protection circuits are connected *within* a scanning line driving circuit." *Id.* Patent Owner disagrees with that claim construction, as discussed above in Section III.D.2(f) in relation to limitation [4e]. *See id.* at 2–3.

Patent Owner also argues "Petitioner mischaracterizes and misunderstands Patent Owner's comparison of Reiner to the conventional art disclosed by the '157 patent." *Id.* at 3–7. For example, Patent Owner

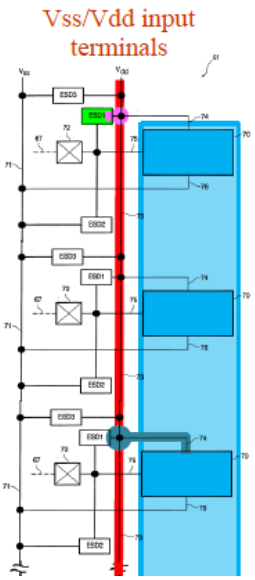
maintains that Dr. Schubert's reoriented version of Reiner's Figure 5 (reproduced above) is like Figure 11 of the '157 patent in "teach[ing] ESD protection between input/outputs of the circuitry to be protected." *Id.* at 4.

Patent Owner further argues Dr. Murphy's cross-examination testimony contradicts the alleged distinction between "module" and "driving circuit" in his Reply Declaration. *See id.* at 8 (citing Pet. Reply 17–18; Ex. 1024 ¶ 70; Ex. 2008, 83:1–85:19). This distinction also is rebutted by Reiner's express disclosure, according to Patent Owner. *See id.* (citing Ex. 1005, Fig. 5, 9:20–23).

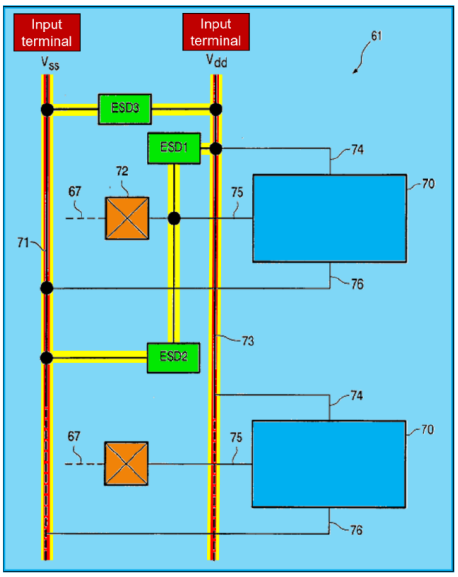
Patent Owner finally contends that, if "Reiner's ESD devices shown in Figure 5 are inside Reiner's source driver 61 integrated circuit chip" as Patent Owner contends, then the "between" requirement of limitation [4f] cannot be met regardless of Petitioner's arguments to the contrary. *Id.* at 8–9 (citing Pet. Reply 17–21).

(ii) Mapping the Claimed "Driving Circuit" to Reiner's Figure 5

As demonstrated by the summary of the parties' arguments above, a foundational dispute is whether Petitioner's mapping of the claimed "driving circuit" to Reiner's Figure 5 is supported by a preponderance of the evidence. The competing contentions are illustrated below (on the next page).



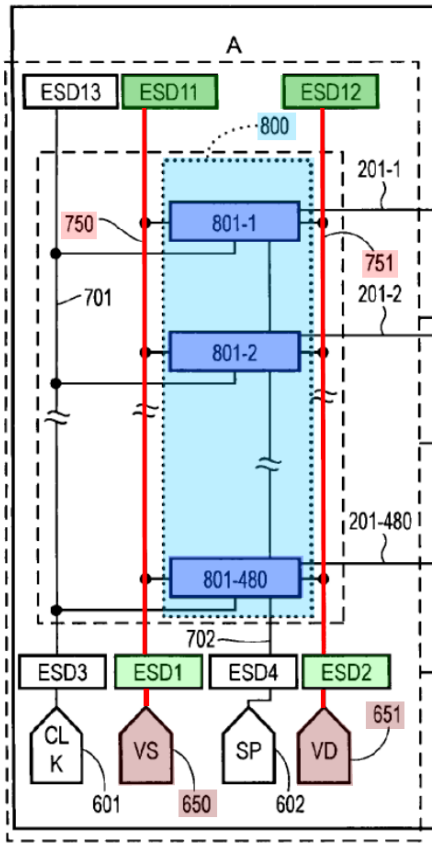
Petitioner's Contention.



Patent Owner's Contention.

Petitioner contends, as illustrated at left, that the claimed "driving circuit" (light blue box) corresponds to the group of output devices 70 (dark blue boxes). *See* Pet. 37–38; Pet. Reply 18. Patent Owner contends, as illustrated at right, that the claimed "driving circuit" must correspond to the entire "integrated circuit [of] Reiner's driver 61" (light blue box). PO Resp. 33; *see id.* at 35–36. Patent Owner particularly asserts the claimed "driving circuit" must correspond not only to the group of output devices 70 (dark blue boxes), but must also include the two power lines 71-Vss and 73-Vdd (red), the ESD devices (green), the contact pads 72 (orange), the input terminals (dark red), and the low-ohmic pathways (yellow). *See id.* at 35–41.

We conclude Petitioner's mapping is supported by a preponderance of the evidence, as follows. First, an excerpt of Figure 1 of the '157 patent is reproduced at right, with our color annotations added. The '157 patent identifies the claimed "scanning line *driving circuit* 800" as a dotted line box (light blue) surrounding the group of "*driving unit circuits* 801-1 to 801-480" (dark blue). Ex. 1001, 4:60–66, 5:20–28 (emphasis added). This is directly analogous to Petitioner's contention that the claimed "driving circuit" in Reiner's Figure 5 may correspond to the group of Reiner's output devices 70, without including the power lines 750 and 751 (red), the devices ESD1, ESD2, ESD11, and ESD12 (green), or the input terminals 650 and 651 (brown). Indeed, Patent Owner "*disputes*" Petitioner's annotations to Figure 2 of the '157 patent "showing the scanning line driving circuit as *encompassing more than the dashed-line box 800*." PO Sur-reply 9 & n.2 (emphases added); *see* Pet. Reply 18–20.



'157 Patent, Figure 1 (Excerpt, Annotated in Color).

Second, Patent Owner and Dr. Schubert do not cite any intrinsic evidence that might indicate the claimed "driving circuit" in Reiner's Figure 5 must include the power lines, the ESD devices, the contact pads, the input terminals, and the low-ohmic pathways. *See* PO Resp. 32–42; Ex. 2009 ¶¶ 75–84. Instead, their position seems to be that Reiner's display driver 61 is structured as an "integrated circuit" so the "driving circuit" of claim 4 must be mapped to the entirety of display driver 61 as shown in

Figure 5. *See, e.g.*, PO Resp. 32–33 (arguing "Reiner teaches an integrated circuit including an internal ESD protection network" and referring to "an integrated circuit like Reiner's driver 61"); *see also* Ex. 1005, 9:18–22 (referring to "integrated circuit device 61" and stating Figure 5 illustrates "a display driver 61" wherein "ESD protection means can easily be integrated into such a display driver 61").

However, even if the entirety of Reiner's Figure 5 is structured as an "integrated circuit" per Reiner's teachings, Petitioner's mapping of the claimed "driving circuit" to the group of output devices 70 in Reiner's Figure 5 is supported by the intrinsic evidence as discussed above. We discern nothing in the plain and ordinary meaning of the claim term "driving circuit" or in Reiner's disclosure that precludes Petitioner's mapping of the claimed "driving circuit" to the portion of Reiner's integrated circuit structure 61 that drives display lines 67 in LCD screen 60. *See, e.g.*, Ex. 1005, 9:23–34 (describing Fig 4), 10:1–23 (describing Fig. 5).

Third, we acknowledge that in summarizing the '157 patent specification, Patent Owner and Dr. Schubert assert "*[t]he driving circuit 'in the scope of the claims*' is a scanning line driving circuit that is 'formed by integrating polysilicon *thin film transistors [TFTs] on [an] active matrix substrate*." PO Resp. 2–3 (emphasis added) (citing Ex. 1001, Fig. 1 (active matrix substrate 101), 1:10–13, 5:20–28); Ex. 2009 ¶ 35. Patent Owner and Dr. Schubert also assert such a driving circuit "is different than" a driving circuit that "is a 'general semiconductor device' — *an integrated circuit formed on a silicon wafer*" to form "a *discrete integrated circuit chip*." PO Resp. 2–7 (emphasis added) (citing Ex. 1001, Figs. 1 and 11, 1:10–13, 1:23–39, 1:47–54, 2:20–50, 3:67–4:13, 5:20–28); Ex. 2009 ¶¶ 35–36.

However, we find nothing in the language of claim 4 or in the '157 patent specification that requires the scanning line driving circuit to be formed of thin film transistors on an active matrix substrate, or to exclude an integrated circuit formed on a silicon substrate. Claim 4 does not specify a substrate, much less a particular material or structural configuration of a substrate. *See* Ex. 1001, 12:25–47 (claim 4); Tr. 27:8–28:23 (Patent Owner's counsel agreeing that claim 4 does not recite an active matrix substrate); *see also* Ex. 1001, 12:58–62 (dependent claim 8 adds "the scanning line driving circuit being arranged on [a] substrate").

The '157 patent specification indicates the invention was inspired by the need to improve electrostatic discharge protection for large display driving circuits composed of thin film transistors formed on an active matrix substrate, but it does not reflect that the invention should be limited to such a design to the exclusion of an integrated circuit formed on a silicon substrate. *See* Ex. 1001, 1:10–13, 1:33–2:57, 4:3–13, 5:20–28. The specification in fact suggests the contrary. *See id.* at 11:29–33 ("*[I]nstead of a thin film transistor formed on the insulating substrate*, an active matrix substrate may be used, in which a pixel switching element or a driving circuit is *formed on a crystal silicon wafer*." (emphases added)); Pet. Reply 24. Thus, during oral argument, Patent Owner's counsel clarified that "[c]laim 4 might not explicitly exclude an integrated circuit" and Patent Owner's position instead is "[c]laim 4 specifically requires an arrangement . . . that *Reiner's* integrated circuit [(specifically)] cannot teach." Tr. 32:1–34:9 (emphasis added).

Fourth, Patent Owner argues Petitioner's mapping of claim 4 to Reiner *in the Petition* was that the claimed "driving circuit" is the entirety of

Reiner's display driver 61, which Petitioner then altered in the Petitioner Reply to be only the group of output devices 70 in display driver 61. *See* Tr. 33:23–35:23 ("In the petition, Petitioner says, and Dr. Murphy says, that the claimed scanning line driving circuit is 61, not the group of output devices 70."). We disagree. Petitioner's position in this proceeding has always been that the claimed "driving circuit" corresponds to the light blue box in Petitioner's Figures A1–A3, as reproduced above. *See id.* at 51:16–21.

It is true that the Petition, when discussing the claimed "scanning line driving circuit" in limitation [4a], states "Reiner discloses gate driver 63 (scanning line driving circuit)" in blue text, and then correspondingly annotates Figure 4 of Reiner to identify the "Gate drivers" 63 in blue. Pet. 17–18. However, when mapping limitations [4d]–[4f] to Figure 5 of Reiner, the Petition similarly color codes Figure 5 in light blue to identify the "driving circuit" as the group of output devices 70 in display driver 61. *See* Pet. 27–28 (Fig. A1), 34–36 (Fig. A2), 37–39 (Fig. A3). Notably, the group of output devices 70 in display driver 61 of Figure 5 are part of the box 61 shown in Figure 4 — or, per Petitioner's obviousness contentions discussed below in Section III.D.2(j), part of box 63 as colored blue earlier in the Petition. Thus, Petitioner's mapping of the "driving circuit" limitation to Reiner's disclosure has not changed.

For the foregoing reasons, we conclude Petitioner's mapping of the "driving circuit" claim term to the group of output devices 70 in Reiner's Figure 5 is supported by a preponderance of the evidence. As a result, Patent Owner's attempt to distinguish Reiner from claim 4 on the basis that

Reiner's protection circuits ESD1 are "in" or "inside" Reiner's driving circuit is unavailing.

In particular, we find the color-coded annotations in Petitioner's Figure A3, reproduced above, demonstrate how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4f], except that it is a source/data driver rather than a gate/scanning driver as claimed. That is, the illustrated display driver includes a driving circuit (light blue) connected to the power supply line 73-Vdd (red, via dark teal line 74) between: (iii) a second connecting portion (pink line) at which the first protection circuit (light green, ESD1 at top) and the power supply line 73-Vdd (red) are connected; and (iv) a third connecting portion (purple line) at which the second protection circuit (dark green, ESD1 at bottom) and the power supply line 73-Vdd (red) are connected.

(iii) Whether Reiner Corresponds to the Conventional Art of the '157 Patent

We also disagree with Patent Owner's contention and Dr. Schubert's testimony that Reiner represents the conventional art described in the '157 patent, for the following reasons.

The '157 patent specification describes conventional art having protection circuits *only* at the *input terminals* — specifically, ESD1 at power line input terminal 650, ESD2 at power line input terminal 651, ESD3 at signal line input terminal 601, and ESD4 at signal line input terminal 602. *See* Ex. 1001, Fig. 11, 1:43–2:28. For example, the '157 patent states the "conventional method used in a semiconductor on a silicon wafer is applied as it is, so that *only protective circuits for preventing the static electricity from the input terminals are built in*." *Id.* at 1:48–51 (emphasis added).

Patent Owner and Dr. Schubert do not cite any disclosure of the '157 patent that indicates the conventional art included protection circuits at any *outputs*, as they allege. *See* PO Resp. 33–36, 41; Ex. 2009 ¶¶ 78–80, 84. Thus, although Reiner's placement of protection circuit ESD3 in Figure 5 may be akin to the '157 patent's conventional art as Patent Owner alleges, Reiner's *additional* placement of protection circuits ESD1 and ESD2 near output contact pads 72 is a significant difference from the '157 patent's conventional art. *Compare* PO Resp. 35 (annotating Fig. 11 of the '157 patent), *with id.* at 36 (annotating Fig. 5 of Reiner). Indeed, Reiner states "*three* ESD devices ESD1, ESD2, and ESD3 are provided for *each output device 70*" as shown in Reiner's Figure 5 (Ex. 1005, 10:11–12 (emphases added)), which has no analogue in the '157 patent's Figure 11.[9]

Further, Petitioner's Mapping A relies on two of Reiner's protection circuits ESD1 (not ESD3) as the first and second protection circuits of claim 4. The '157 patent's conventional art has no analogue to Reiner's ESD1, as discussed above. Therefore, Petitioner's particular usage of Reiner in proposing the unpatentability of claim 4 in Mapping A does not overlap with the conventional art described in the '157 patent.

For the foregoing reasons, we are not persuaded by Patent Owner's attempt to distinguish Reiner's structure from claim 4 on the basis that Reiner represents the conventional art of the '157 patent specification upon which claim 4 was intended to improve.

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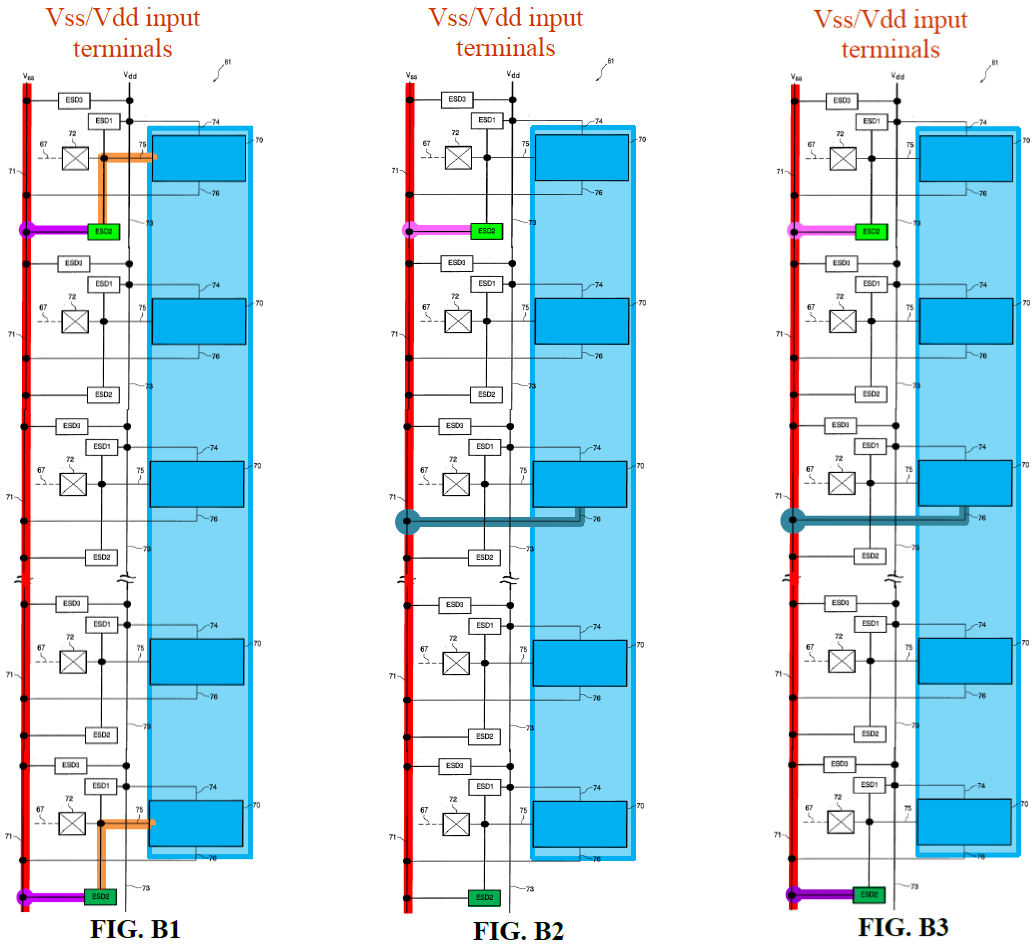
[9] This is true even if, as Patent Owner alleges, only ESD1 and ESD2 are repeated (without ESD3) throughout Reiner's display driver 61. *See* PO Resp. 36 n.4; Pet. Reply 15 n.11.

(iv) Conclusion Concerning Limitation [4f]

We conclude Petitioner's Mapping A demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitation [4f], except that it is a source/data driver rather than a gate/scanning driver as claimed.

(h) [4d] to [4f] — Petitioner's Mapping B

We find Petitioner's Mapping B demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitations [4d] to [4f], except that it is a source/data driver rather than a gate/scanning driver as claimed, in a different way than Mapping A. Petitioner's Figures B1, B2, and B3 illustrate Mapping B, and are reproduced below.



Petitioner's Figures B1, B2, and B3.

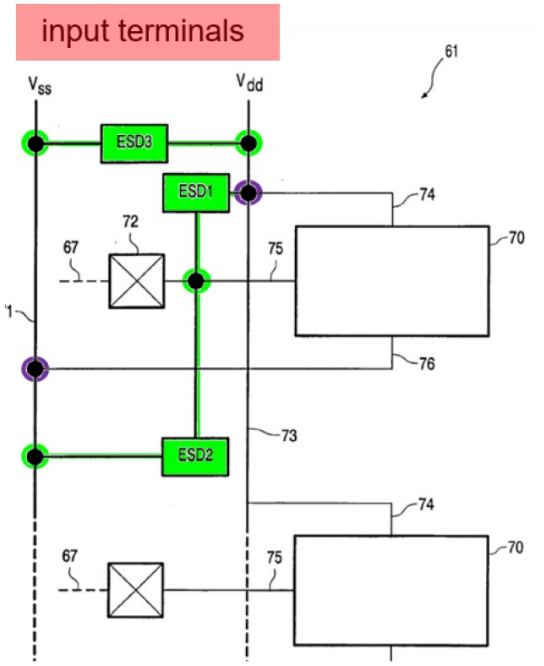
As with Petitioner's Mapping A, Petitioner's Figures B1, B2, and B3 extend Reiner's Figure 5, which shows only two output devices 70 for driving two lines 67, to include at least three more devices 70 and lines 67 on the basis that a person of ordinary skill in the art would have understood there would be as many devices 70 as there are lines in Reiner's display device. *See* Pet. 26; Ex. 1003 ¶ 107. Patent Owner does not dispute this extension of Reiner's Figure 5.

Petitioner's Figure B1, reproduced above, illustrates Mapping B as it relates to limitation [4d]. *See* Pet. 24–29 (citing Ex. 1005, Fig. 5, 2:2–3, 2:28–3:1, 4:15–16, 8:8–15, 9:11–22, 10:1–17, 12:4–5, 12:23–25); Ex. 1003 ¶¶ 103–111. We find the color-coded annotations in Figure B1 identify, per limitation [4d], a first protection circuit (light green, ESD2 at top) and a second protection circuit (dark green, ESD2 at bottom) connected to a driving circuit (light blue, via orange lines) to protect the driving circuit. *See* Ex. 1005, Fig. 5, 2:1–3, 2:28–3:1, 4:15–16, 10:1–17, 12:22–25; Pet. 27–29; Ex. 1003 ¶¶ 109, 110–111. The annotations further identify how both protection circuits are connected to the power supply line 71-Vss (red, via purple lines). *See* Ex. 1005, Fig. 5, 9:11–22, 10:1–17; Pet. 27–28; Ex. 1003 ¶¶ 109, 110. Patent Owner does not dispute these findings. *See* PO Resp. 27–32 (argument comparing Reiner with limitations [4d] and [4e]).

Petitioner's Figure B2, reproduced above, illustrates Mapping B as it relates to limitation [4e]. *See* Pet. 34–36 (citing Ex. 1005, Fig. 5); Ex. 1003 ¶¶ 121–123, 125. We find the color-coded annotations in Figure B2 identify, per limitation [4e], a first protection circuit (light green, ESD2 at top) connected to the power supply line 71-Vss (red, via pink line) between: (i) a first connecting portion (dark teal line 76) at which the scanning line

driving circuit (light blue) and the power supply line 71-Vss (red) are connected; and (ii) the input terminal (brown, at top).

Patent Owner objects that Petitioner's identified "first protection circuit" (light green, ESD2 at top) fails to satisfy the requirement of limitation [4e] of being "connected to the power supply line . . . *between* the scanning line driving circuit's connection to the power supply line and the power supply line input terminal." PO Resp. 27. Instead, according to Patent Owner, "the source driver and line Vss are connected to one another *between* the purported input terminals and ESD2's connection to line Vss." *Id.* at 28; Ex. 2009 ¶¶ 73–74 (testifying Petitioner's identified "first protection circuit" is not "*between*, as claimed, [the] power supply line's connection to *any portion* of the scanning line driving circuit and the power supply line's input terminal" (second emphasis added)). We reproduce below Patent Owner's annotations to Reiner's Figure 5 to support this argument:



Reiner, Figure 5 (Annotated at PO Resp. 28).

Reiner's Figure 5 is a schematic block diagram of source/data driver 61, which Patent Owner has annotated pertinently to identify Petitioner's alleged first protection circuit per Mapping B (ESD2, green) and where it connects (lower left green node) to power supply line 71-Vss (uncolored). *See* PO Resp. 28; Ex. 2009 ¶ 74. That connection point (lower left green node) is underneath where the top-most output device 70 is connected to power supply line 71-Vss (at lower left purple node) via line 76, rather than "between" that connection and the input terminal (red at top). *See* PO Resp. 28; Ex. 2009 ¶ 74; Ex. 1005, 10:8–9.

Patent Owner also objects to the claim construction underlying Petitioner's Mapping B, for the same reasons discussed above in Section III.D.2 in relation to Petitioner's Mapping A, but here directed to Petitioner's dark teal line 76 in Figure B2. *See* PO Resp. 29–31. The Petitioner Reply and the Patent Owner Sur-reply similarly repeat the claim construction arguments we have discussed above in relation to Petitioner's Mapping A. *See* Pet. Reply 10–13; PO Sur-reply 12–17.

We conclude Patent Owner's opposition to Petitioner's Mapping B concerning limitation [4e] is unavailing, because it is premised on a claim construction that we have rejected above in Section III.D.2(f)(ii). In short, limitation [4e] is open to the "first connecting portion" being connected to an intermediate component of the scanning line driving circuit, as dark teal line 76 in Figure B2 is.

Petitioner's Figure B3, reproduced above, illustrates Mapping B as it relates to limitation [4f]. *See* Pet. 37–39 (citing Ex. 1005, Fig. 5); Ex. 1003 ¶¶ 127–129, 131. We find the color-coded annotations in Figure B3 identify, per limitation [4f], the driving circuit (light blue) connected to the

power supply line 71-Vss (red, via dark teal line 76) between: (iii) a second connecting portion (pink line) at which the first protection circuit (light green, ESD2 at top) and the power supply line 71-Vss (red) are connected; and (iv) a third connecting portion (purple line) at which the second protection circuit (dark green, ESD2 at bottom) and the power supply line 71-Vss (red) are connected.

Patent Owner's opposition concerning limitation [4f] relies on arguments we have considered above in Section III.D.2(g) in relation to Petitioner's Mapping A. *See* PO Resp. 32–42. That opposition is unavailing for the reasons provided above in Section III.D.2(g). Additionally, Petitioner's Mapping B relies on two of Reiner's protection circuits ESD2 (not ESD3) as the first and second protection circuits of claim 4. The '157 patent's conventional art has no analogue to Reiner's ESD2, as discussed above in Section III.D.2(g). Therefore, Petitioner's particular usage of Reiner in proposing the unpatentability of claim 4 in Mapping B does not overlap with the conventional art described in the '157 patent.

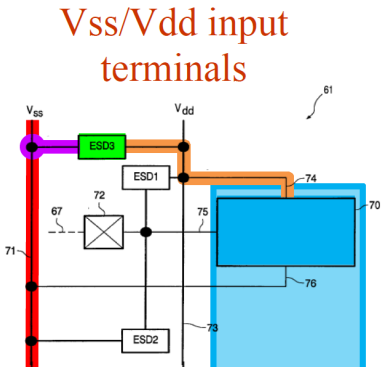
Thus, we conclude Petitioner's Mapping B demonstrates how the display driver illustrated in Reiner's Figure 5 satisfies limitations [4d] to [4f], except that it is a source/data driver rather than a gate/scanning driver as claimed.

(i) [4d] to [4f] — Petitioner's Mapping C

Petitioner's Mapping C is premised on Petitioner's assertion that, in the District Court Litigation, "Patent Owner appears to take the liberal [claim construction] view that any two circuits connected to the same

powerline are connected to each other." Pet. 27 (citing Ex. 1014[10] ¶¶ 136–144). Petitioner "disagrees" with that alleged construction, but presents Mapping C here as "assuming" and applying the alleged construction to Reiner's display driver in Figure 5. *See id.*

We reproduce below an excerpt of Petitioner's Mapping C to Reiner.



Excerpt of Petitioner's Mapping C (Pet. 27–28) to Reiner, Figure 5.

This excerpt of Mapping C includes color-coded annotations to illustrate, as pertinent here, Petitioner's assertion that Reiner discloses a first protection circuit (light green, ESD3) "connected to line driving units of gate driver 63" (orange line leading to blue boxes) through power supply line 73-Vdd (uncolored, vertical component of orange line). Pet. 27–28. Dr. Murphy's testimony concerning Mapping C indicates he was "asked to consider the situation in which ESD3 is considered to be connected to the scanning line drive circuit through the power lines," and he "express[es] no opinion on the correctness of this." Ex. 1003 ¶ 110 & n.13.

Patent Owner responds that "the Petition offers no evidence — and specifically *avoids* creating evidence — that ESD3 is 'connected to the scanning line driving circuit'" as required by limitation [4d]. PO Resp. 27.

[10] Exhibit 1014 is the Complaint filed against Petitioner in the District Court Litigation by Patent Owner's exclusive licensee. *See* Ex. 1014, 1; Paper 19, 1.

Patent Owner asserts "ESD3 is *not*, according to the Petition, connected to the scanning line driving circuit." *Id.* at 31. Patent Owner further argues "Dr. Murphy is unable to, or has refused to, opine that ESD3 is connected to the scanning line driving circuit, e.g., output device 70." *Id.* (citing Ex. 2008, 128:2–133:9).

Petitioner replies that Patent Owner's argument is "disingenuous because Patent Owner ***admits*** Petition Figures C*x* satisfy the claims if Patent Owner's construction is adopted." Pet. Reply 9 (citing PO Resp. 27, 31). Petitioner argues "Patent Owner 'cannot have it both ways' to avoid its own construction in this proceeding while asserting it in district court" and "[t]he Board regularly considers a patent owner's constructions, even when the petitioner does not subscribe to them." *Id.* at 9–10, 21 (citations omitted).

Patent Owner replies that "Patent Owner does *not* admit that Petitioner's Figures C*x* disclose all limitations of claim 4." PO Sur-reply 9. Patent Owner further maintains Dr. Murphy "has not opined that ESD3 . . . is 'connected to' the top output device 70 (the claimed 'scanning line driving circuit['])." *Id.* at 9–10 (citing Ex. 2008, 128:2–133:9). Patent Owner concludes "Petitioner has not met its burden to show the unpatentability of claim 4" per Mapping C. *Id.* at 10–11 (citing Pet. 27–28, 35–36, 38–39; Pet. Reply 9–10; Ex. 1003 ¶¶ 110, 123; Ex. 1014 ¶¶ 136–144).

We conclude Petitioner has failed to satisfy its burden to prove unpatentability applying Mapping C. *See* 35 U.S.C. § 316(c). This burden requires Petitioner to identify how the challenged claim is to be construed. *See* 37 C.F.R. § 42.104(b)(3). The Petition here does not satisfy that burden.

The Petition instead simply asserts "Patent Owner appears to take the liberal view that any two circuits connected to the same powerline are

connected to each other." Pet. 27 (citing Ex. 1014 ¶¶ 136–144). In addition to being vague ("appears to take"), this assertion is not supported by any explanation of why Petitioner believes the Complaint in the District Court Litigation is premised on the alleged construction. *See id.* Petitioner cites seven pages of factual averments from the Complaint — averments that rely heavily, but without sufficient explanation, on annotated photographs of complicated LCD circuits. *See* Ex. 1014 ¶¶ 136–144. Petitioner stops short of explaining adequately, if at all, how or why that evidence supports the challenge or, in particular, Petitioner's Mapping C. The cited evidence is neither simple nor self-explanatory. *See id.* We decline Petitioner's invitation to sift through this evidence without any guiding arguments to determine whether, or why, it supports Petitioner's contentions. In other words, the Petition is deficient from the onset for failure to show with particularity why the patent it challenges is unpatentable. *Harmonic*, 815 F.3d at 1363.

This deficiency in the Petition is exacerbated by Dr. Murphy's testimony in support of Petitioner's Mapping C. Dr. Murphy was "*asked to consider the situation in which ESD3 is considered to be* connected to the scanning line drive circuit through the power lines," and he "express[es] no opinion on the correctness of this." Ex. 1003 ¶ 110 & n.13 (emphasis added). Dr. Murphy does not address the Complaint in the District Court Litigation at all, much less explain how its photographs of complicated LCD circuits might be premised on the alleged construction that any two circuits connected to the same powerline are connected to each other. *See id.* ¶¶ 103–111. Further, under cross-examination, Dr. Murphy repeatedly refused to explain how Reiner's ESD3 might be considered to be

"connected" to output device 70. *See* Ex. 2008, 128:2–133:9 ("I don't have an opinion as to that question. Wasn't something that was developed in detail as part of my analysis for the '157 patent.").

Petitioner belatedly attempted to cure this deficiency in the Petition via Demonstrative Slide 28 during oral argument. *See* Tr. 18:12–20:21, 62:16–19; Ex. 1025, 28. As noted in our Order Setting Oral Argument: "Demonstrative exhibits cannot be used to advance arguments or introduce evidence not previously presented in the record." Paper 27, 4 (citing legal authorities). Petitioner's Demonstrative Slide 28 attempts to do exactly that. *Compare* Pet. 27 *with* Ex. 1025, 28. Petitioner cites the Petition at pages 34–40 as making the demonstrated argument, but there is no discussion there of the Complaint in the District Court Litigation. *See* Pet. 34–40; Ex. 1025, 28; Paper 27, 4 ("[I]t is strongly recommended that each demonstrative include a citation to a paper in the record, which allows the Board to easily ascertain whether a given demonstrative contains 'new' argument or evidence."). Moreover, even considering Petitioner's Demonstrative Slide 28, it still fails to explain how the photographs of complicated LCD circuits in the Complaint might justify Petitioner's Mapping C here. *See* Ex. 1025, 28.

Next, we disagree with Petitioner's assertion that Patent Owner has admitted Mapping C satisfies claim 4 if the Complaint's alleged claim construction is adopted. We discern no such admission in the Patent Owner Response, and Patent Owner disavowed any such admission in its Sur-reply and during oral argument. *See* PO Resp. 27, 31 (cited at Pet. Reply 9); PO Sur-reply 9–11; Tr. 40:21–41:13, 62:1–63:7. Patent Owner does "believe that it is correct to say that a protection circuit is connected to this

scanning line driving circuit through the power supply line" (*id.* at 63:4–5), but for all the reasons discussed above it is not clear whether or how the Complaint relies on that belief so as to support Petitioner's Mapping C by a preponderance of the evidence.

Finally, in a recent precedential decision, the USPTO Director held that when a petitioner proposes different claim constructions in an IPR petition and in District Court litigation, the petitioner must explain why the different constructions are warranted. *See Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20, at 2–5 (Squires Nov. 3, 2025). Further: "Simply noting that the petitioner is adopting a patent owner's claim construction proposals from district court . . . is not a sufficient reason." *Id.* at 5.

In the present case, Petitioner has argued in District Court that its accused products do not infringe claim 4 based on a construction of limitation [4d] that is narrower than the construction undergirding Mapping C. *See* Ex. 1026, 3–12. The Petition does not provide the explanation required by the *Revvo* decision for such alternative claim constructions. *See* Pet. 27. The Petitioner Reply does no more than simply allege Petitioner is applying Patent Owner's claim construction from the District Court litigation. *See* Pet. Reply 9–10, 21. Therefore, Petitioner's Mapping C is deficient pursuant to the *Revvo* decision.

For the foregoing reasons, we reject Mapping C as failing to satisfy Petitioner's burden to prove unpatentability.

(j) Whether Reiner Renders Obvious a Scanning Line Driving Circuit Utilizing First and Second Protection Circuits per Limitations [4d]—[4f]

As discussed above in Sections III.D.2(e)–(h), Reiner's Figure 5 discloses a display device driving circuit protected by first and second protection devices per limitations [4d]–[4f] and Mappings A and B, except the protected driving circuit is in Reiner's source/data driver 61 rather than Reiner's gate/scanning driver 63.

Petitioner contends a person of ordinary skill in the art would have been motivated to configure Reiner's gate/scanning driver 63 to include the ESD protection network structure of Figure 5. *See* Pet. 24–25, 29–33; Ex. 1003 ¶¶ 103–105, 112–120.

In support, Petitioner asserts and Dr. Murphy testifies that Reiner seeks to provide "integrated circuit devices with ESD protection" "in order to prevent the very sensitive circuits on the chip from being destroyed when it is subjected to a discharge event," wherein a "typical example is an integrated circuit display driver 61 *or 63*." Pet. 24–25, 29 (citing Ex. 1005, 2:2–3, 2:28–3:1, 4:15–16, 8:8–15, 9:12–14, 12:4–5, 12:23–25); Ex. 1003 ¶¶ 104–105, 111–112. Petitioner and Dr. Murphy cite Reiner's Figure 5 as illustrating how "ESD protection means can easily be integrated" into either one of Reiner's display drivers 61 or 63. Pet. 25 (citing Ex. 1005, 2:28–3:1, 9:11–22); Ex. 1003 ¶ 105.

Thus, according to Petitioner and Dr. Murphy, a person of ordinary skill in the art would have understood that the ESD protection network structure of Figure 5 would have "applie[d] equally to" Reiner's gate/scanning driver 63, because both drivers 61 and 63 are display device circuit drivers, and Reiner discloses how both display drivers 61 and 63 can

benefit from ESD protection thereby "teaching, or at least suggesting, that both drivers would be protected in similar fashion." Pet. 25, 29–32 (citing Ex. 1005, 2:2–3, 2:28–3:3, 4:10–19, 6:12–17, 8:30–31, 9:11–22, 10:10–17, 12:4–5, 12:16–18); Ex. 1003 ¶¶ 105, 111–119.

Petitioner and Dr. Murphy conclude a person of ordinary skill in the art would have been motivated to configure Reiner's gate/scanning driver 63 to include the ESD protection network structure of Reiner's Figure 5, with a reasonable expectation of success. *See* Pet. 30–33; Ex. 1003 ¶¶ 115–120. For example, that structure "would have protected the circuits . . . using a single metal layer [which] would have reduced the cost of fabricating gate driver 63 and made the chip less bulky." Pet. 32 (citing Ex. 1005, 4:10–12, 4:15–19, 9:16–22, 10:15–17, 12:15–18, claim 11); Ex. 1003 ¶ 118.

Patent Owner argues and Dr. Schubert testifies that Petitioner "fails to show that Reiner renders obvious applying Reiner's source driver ESD protection network to a gate driver" because "[d]ifferences between a source driver and a gate (scan line) driver would *require changes* to Reiner's ESD protection network." PO Resp. 24 (emphasis added); Ex. 2009 ¶¶ 62–68. Patent Owner asserts "[n]o evidence shows that the gate driver would include an ESD protection network identical to the source driver's network and include the same number of ESD devices connected in the same way." PO Resp. 24. Dr. Schubert testifies in support that "Dr. Murphy does not cite evidence showing that (1) the gate drivers comprise output devices 70, or (2) the gate driver is arranged like the source driver, to accommodate the same ESD layout" and, in fact, "Reiner discloses that the gate driver integrated circuit comprises individual gate drivers, not output devices 70." Ex. 2009 ¶ 65 (citing Ex. 1005, 9:20–9:31); *see* PO Resp. 24–25.

Dr. Schubert further testifies that a person of ordinary skill in the art "would know to expect changes in the layout in view of key differences between a source driver and a gate driver." Ex. 2009 ¶ 64; PO Resp. 25. Those differences include:

Gate/Scanning Driver 63	**Source/Data Driver 61**
"*individual gate/scan line drivers are coupled to one another, to coordinate signals* and ensure that no two gate/scan line drivers transmit gate signals to more than one gate/scan line at the same time"	coordinated signals are "not . . . required for source/data unit drivers because *each individual source/data driver transmits image data signals simultaneously*"
"*the individual gate line unit driving circuits are in communication with the two neighboring unit drivers* so that *the ensemble of gate line unit driving circuits can operate as a shift register*"	"the source line unit drivers are *independently operating* drivers whose *signals are independent from one another"*
"the gate line drivers provide *two-state, digital ON and OFF signals*"	"the source line drivers provide *analog image information signals*"
"the gate drivers drive, sequentially, one gate line at a time"	"the source drivers drive all data lines at all times"

Ex. 2009 ¶¶ 66–67 (emphases added); *see* PO Resp. 25–26. Dr. Schubert concludes that, due to the foregoing differences, "a specific ESD protection arrangement that works for source drivers would not necessarily be known to work as ESD protection for a gate driver," so "Reiner does not disclose or suggest that source driver 61's internal ESD layout would, or even could, apply to a gate driver." Ex. 2009 ¶¶ 67–68; *see also* PO Resp. 26 ("These

differences demand different wiring layouts, affecting the ESD protection network that Reiner provides only in the source driver context.”).

Petitioner replies that “[t]he Board already rejected similar arguments” in the Institution Decision. Pet. Reply 4 (citing Inst. Dec. 36–37). Petitioner also asserts and Dr. Murphy testifies that “Patent Owner does not identify any alleged ‘[d]ifferences’ that are material to the ’157 patent’s claims” and in fact “[m]any of Patent Owner’s ‘[d]ifferences’ actually highlight the similarities between source drivers and gate drivers that confirm obviousness.” *Id.* at 4–8; Ex. 1024 ¶¶ 36–51. As one example, Dr. Murphy testifies Reiner discloses individual gate driver circuit units in gate/scanning driver 63 for driving each gate line 68, so a person of ordinary skill in the art would have “appl[ied] Reiner’s ESD protection network in FIG. 5 to gate driver 63 because that network protects any circuit inside box 70 whether it has a gate driver line unit configuration or a source driver line unit configuration.” Ex. 1024 ¶¶ 40–41 (citing Ex. 1005, Figs. 3–5, 2:2–3, 2:28–3:8, 4:15–16, 8:8–15, 9:11–22, 9:27–28); *see* Pet. Reply 4–5 (also citing Ex. 1005, 10:1–23).

Patent Owner responds by reiterating its arguments summarized above. *See* PO Sur-reply 17–18.

We conclude Petitioner’s contentions of obviousness are supported by a preponderance of the evidence, as follows.

First, we find Reiner discloses *both* of its display drivers 61 *and* 63 would benefit from ESD protection, as Dr. Murphy testifies. That is, Reiner describes display drivers 61 and 63 as “typical example[s]” of densely packed integrated circuit devices that can benefit from utilizing Reiner’s bump bridge technology for providing ESD protection, due to the large

number of parallel output lines that must cross power supply lines. *See* Ex. 1005, 4:15–16, 8:8–17, 9:11–20 (describing Fig. 4), 12:4–7; Ex. 1003 ¶¶ 104–105, 115; Ex. 1024 ¶¶ 37–38. Dr. Schubert does not disagree with Dr. Murphy in this regard. *See* Ex. 2009 ¶¶ 62–68.

Second, we are persuaded by Dr. Murphy's testimony that the *ESD protection network structure* of Reiner's Figure 5 would be suitable for implementing in Reiner's gate/scanning driver 63 due to similarities between the two drivers. *See* Ex. 1003 ¶¶ 104–105, 111–120. One key similarity is that display drivers 61 and 63 both are composed of individual output devices, each dedicated to driving one line 67 or 68 in LCD screen 60. *See, e.g.*, Ex. 1005, 9:18–20 ("The bump bridges allow *many output devices* of the integrated circuit device 61 or 62 [sic '63'] to cross the power supply lines which provide supply voltage (e.g., Vdd) *to the output devices*." (emphasis added)); *id.* at Fig. 4 (illustrating "Gate drivers" (plural) in box 63); *id.* at 9:31–10:10 (Fig. 5 shows source/data driver 61 composed of individual output devices 70 to drive source lines 67). Thus, Dr. Murphy testifies persuasively that Reiner's gate/scanning driver 63 has output devices akin to the output devices 70 shown in Figure 5 for source/data driver 61. *See* Ex. 1003 ¶¶ 111, 113, 115, 117; Ex. 1024 ¶ 40.

Dr. Schubert agrees that "Reiner discloses that the gate driver integrated circuit comprises *individual gate drivers*," although he adds that those individual gate drivers are "not output devices 70." Ex. 2009 ¶ 65 (emphasis added, citing Ex. 1005, 9:20–9:31). We correspondingly find that the internal configuration of the individual output devices in gate/scanning driver 63 will very likely differ from the internal configuration of the

individual output devices 70 in source/data driver 61 (which are shown as black boxes in Figure 5). *See id.*; Ex. 1003 ¶¶ 111, 115, 117; Ex. 1024 ¶ 40.

Nonetheless, as pertinent here, the individual output devices in both display drivers 61 and 63 are powered by two power supply lines 71-Vss and 73-Vdd. *See supra* Section III.D.2(c) (limitation [4b]); Ex. 1005, Fig. 3, 8:8–9:20. Thus, display drivers 61 and 63 both are subject to the same design difficulty that Reiner's bump bridge technology and the associated ESD protection network are designed to overcome, namely the large number of parallel output lines that must cross power supply lines. *See* Ex. 1005, 4:15–16, 8:8–9:22, 12:4–7; *id.* at Fig. 3 (illustrating exemplary integrated circuit device 30 powered by supply voltages Vdd and Vss, with bump bridge 41 connecting contacts pads 38 and 40 while avoiding line 35-Vss), Fig. 5 (illustrating source/data driver 61 including output devices 70 with output lines 75 crossing power supply line 73-Vdd); Ex. 1003 ¶¶ 104–105, 111–113; Ex. 1024 ¶ 37. Therefore, we are persuaded by Dr. Murphy's testimony that Reiner's bump bridge technology for providing ESD protection could and would have been implemented in Reiner's gate/scanning driver 63 in the same fashion as illustrated in Figure 5 for Reiner's source/data driver module 61. *See* Ex. 1003 ¶¶ 104–105, 111–120; Ex. 1024 ¶¶ 40–41.

Third, Reiner describes the ESD protection network structure of its Figure 5 as one specific way that a display device driving circuit composed of individual drivers (whether gate/scanning output devices or source/data output devices) can be protected while utilizing only a single metal layer, avoiding the increased bulk and cost associated with two metal layers. *See* Pet. 32; Ex. 1005, 4:10–19, 9:16–22, 12:15–18; Ex. 1003 ¶¶ 118–119. This

disclosure would have led a person of ordinary skill in the art to configure Reiner's gate/scanning driver to include Figure 5's ESD protection network structure. *See* Ex. 1003 ¶¶ 118–119.

Fourth, we have considered Dr. Schubert's testimony that the ESD protection network structure of Reiner's Figure 5 would need to be changed when applied to Reiner's gate/scanning driver 63, because the individual gate drivers will be coupled to one another to coordinate their signals, whereas such coupling and coordination is not needed for the individual source drivers 70 of source/data driver module 61. *See* Ex. 2009 ¶¶ 64, 66, 67 ("**First**" and "**Second**"). However, we are persuaded by Dr. Murphy's reply testimony that "the means for such coupling (e.g., lines or other structures that Dr. Schubert suggests but fails to depict or define)" could have been implemented "within the 'black box' line driver unit 70 of Reiner's FIG. 5" as controlled by CPU 62, and would not have affected the power line ESD protection network structure of Reiner's Figure 5. Ex. 1024 ¶¶ 42–46; *see also* Ex. 1005, 9:28–32 ("The CPU 62 controls the scanning of all the gate lines 68" by providing "row timing signals (control signals) via a bus 69 to the gate driver 63"). "A person of ordinary skill is also a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 550 U.S. at 420–21.

Fifth, we have considered Dr. Schubert's testimony that the individual gate drivers in gate/scanning driver 63 will drive their respective gate/scan lines 68 in different ways than the individual source drivers 70 in source/data driver module 61 will drive their respective source/data lines 67. *See* Ex. 2009 ¶ 67 ("whereas the source line drivers provide analog image

information signals, the gate line drivers provide two-state, digital ON and OFF signals" and "the source drivers drive all data lines at all times, whereas the gate drivers drive, sequentially, one gate line at a time"). However, we conclude that such differences in the *signal outputs* of Reiner's respective display drivers 61 and 63 have little to do with the benefits of configuring the *power inputs* of the display drivers to protect the individual circuits from electrostatic discharge events, or how to do so. *See, e.g.*, Ex. 1024 ¶¶ 47–49. Thus, these signal output differences do not undercut Dr. Murphy's testimony in support of obviousness, as discussed above.

For the foregoing reasons, we conclude a preponderance of the evidence demonstrates that a person of ordinary skill in the art would have been motivated to configure Reiner's gate/scanning driver 63 to include the ESD protection network structure of Reiner's Figure 5.

(k) Conclusion as to Claim 4

We conclude Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable as having been obvious over Reiner.

3. Claim 8

Petitioner provides arguments and evidence in support of contending claim 8 (which depends from claim 4) is unpatentable as having been obvious over Reiner, including testimony from Dr. Murphy. *See* Pet. 44–50; Ex. 1003 ¶¶ 143–153. Patent Owner opposes, as supported by testimony from Dr. Schubert. *See* PO Resp. 43–47; Ex. 2009 ¶¶ 88–100. For the following reasons, we conclude Petitioner has not demonstrated claim 8 is unpatentable by a preponderance of the evidence.

Claim 8 recites:

8. The display device as set forth in claim 4, further comprising:

a substrate,

the scanning line driving circuit being arranged on the substrate,

the power supply line being formed over first and second corner portions of the substrate so as to follow a periphery of the substrate,

the first protection circuit being arranged in the first corner portion of the substrate, and

the second protection circuit being arranged in the second corner portion of the substrate.

Ex. 1001, 12:58–13:2.

Petitioner argues "Reiner discloses the display device further comprising a substrate." Pet. 44; Ex. 1003 ¶ 144. Petitioner asserts Figure 2 of Reiner includes substrates 16 and 21, as illustrated by Dr. Murphy's annotations reproduced below.

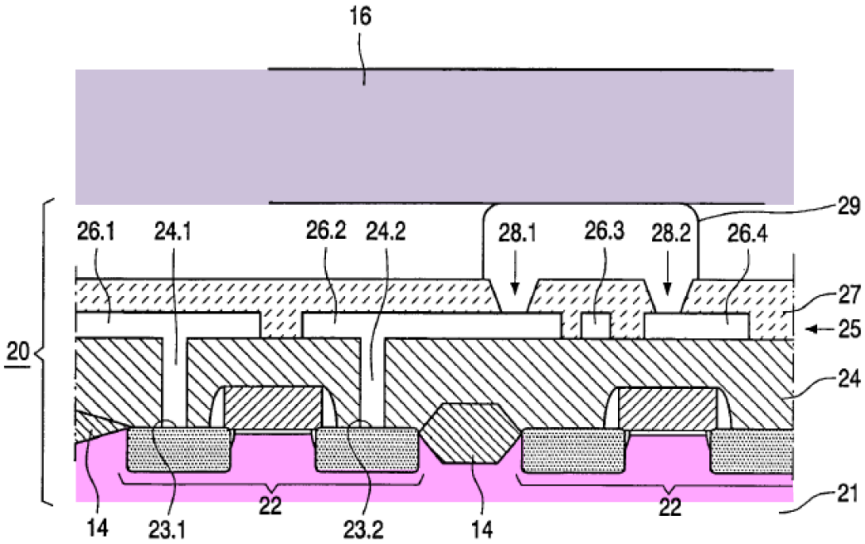


FIG. 2

Reiner, Figure 2 (Annotated at Ex. 1003 ¶ 145).

Dr. Murphy testifies Figure 2 illustrates "integrated circuit 20 (e.g., gate driver 63) . . . arranged on substrate 21" (pink). Pet. 45 (citing Ex. 1005, Fig. 2, 6:18–24, 7:22–26); Ex. 1003 ¶ 145. Dr. Murphy also cites Reiner's disclosure that "[w]hen packaging the integrated circuit device 20, it is flipped onto the substrate 16, according to the well-known flip-chip technology." Ex. 1005, 7:23–25; *see* Ex. 1003 ¶ 145. We accept, for purposes of this Decision, that Reiner's gate/scanning driver 63 includes a scanning line driving circuit arranged on substrate 16 or 21.[11]

Petitioner next asserts a person of ordinary skill in the art "would have recognized that *substrates 21 or 16 may include*, for example, the substrate on which LCD display 60's scan/gate lines 68, source/data lines 67, and pixels are formed, such as shown in" Figure 4, "which was conventional." Pet. 45–46 (emphasis added) (citing Ex. 1005, Fig. 4, 10:1–6; Ex. 1007, Fig. 1, ¶¶ 1, 64; Ex. 1010, Fig. 1, ¶¶ 1, 17; Ex. 1001, Fig. 11, 1:57–59); Ex. 1003 ¶ 146. Dr. Murphy annotates Figure 4 to illustrate this assertion, as reproduced below.

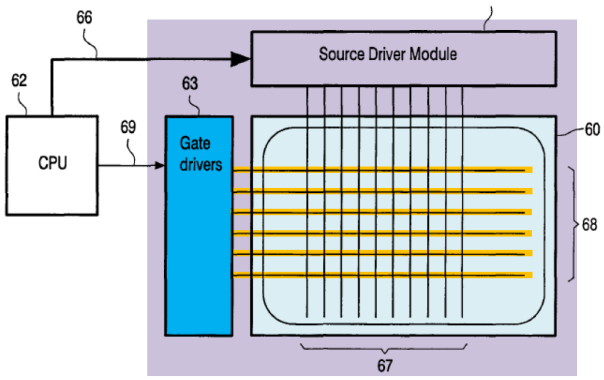


FIG. 4

Reiner, Figure 4 (Annotated at Ex. 1003 ¶ 146).

[11] Patent Owner disagrees, arguing that substrate 16 is not "a 'substrate' on which the integrated device 20, let alone gate driver 63, is 'arranged.'" PO Resp. 44–45.

Figure 4 is a schematic block diagram of an LCD display including: LCD screen 60; source driver 61 which drives source lines 67 in the display; and gate driver 63 (blue) which drives gate lines 68 (yellow) in the display. *See* Ex. 1005, 9:23–31. Dr. Murphy has added a purple box to illustrate that substrate 16 or 21 of Figure 2 may be extended to be the substrate of those components. *See* Pet. 45–47; Ex. 1003 ¶¶ 146, 148.

Based on that extension of substrate 16 or 21, Petitioner contends Reiner discloses or renders obvious the further limitations of claim 8 that the power supply line is formed over first and second corner portions of the substrate to follow a periphery of the substrate, wherein the first protection circuit is arranged in the first corner and the second protection circuit is arranged in the second corner. *See* Pet. 47–50 (citing Ex. 1005, Figs. 4 and 5, 10:1–10); Ex. 1003 ¶¶ 50–51, 149–153. Dr. Murphy illustrates this by making a new Figure D, reproduced below.

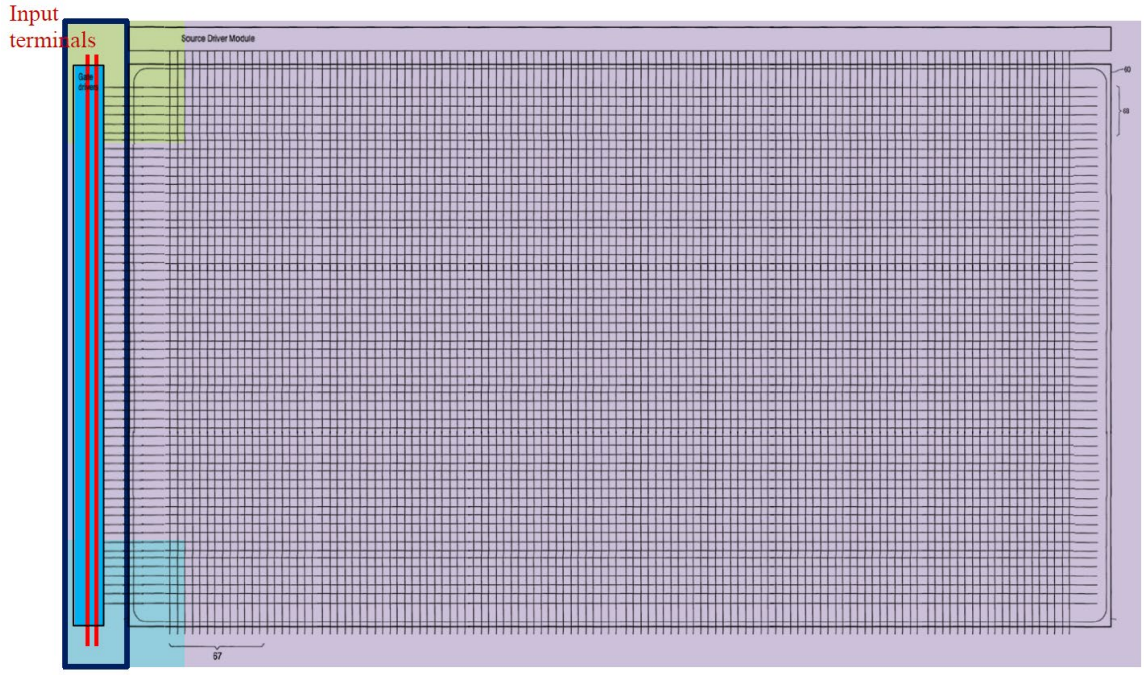


FIG. D
Dr. Murphy's Figure D (Ex. 1003 ¶ 151).

Dr. Murphy's Figure D extends Reiner's Figure 4 to include several more source/data lines 67 and gate/scan lines 68 on substrate 16 or 21 (purple), wherein gate/scanning driver 63 (blue) and its two power lines (red) are formed along one periphery of the substrate between two corners (green and aqua). *See* Pet. 47–49; Ex. 1003 ¶¶ 151–153.

Patent Owner argues Reiner does not disclose or render obvious the "substrate" recited in claim 8. *See* PO Resp. 43. Patent Owner asserts Reiner is limited to "integrated circuits having their own substrates and, separate, a display to which the integrated circuits may connect (for example, via contact pads)." *Id.* at 43–45 (citing Ex. 1005, Fig. 2, 6:18–21, 7:22–25); Ex. 2009 ¶¶ 89–92.

Patent Owner further contends Petitioner "cites no evidence disclosing a *display device* substrate on which a scanning line driving circuit is arranged," and Reiner particularly does not relate substrate 16 or 21 of integrated circuit device 20 to LCD screen 60. PO Resp. 45 (citing Pet. 45–46; Ex. 1005, 9:11–34); Ex. 2009 ¶¶ 92–93. Patent Owner asserts Dr. Murphy's annotated version of Reiner's Figure 4 and his Figure D "simply invent[] a 'substrate [(purple)] to create the LCD display device described by Reiner' upon which 'gate driver 63' would be arranged," based only on impermissible hindsight. PO Resp. 45–46 (citing Pet. 46). Patent Owner moreover argues Petitioner "fails to show that arranging Reiner's 'gate driver[s] 63' on the display substrate 'was conventional,'" because Petitioner's cited references "relate to devices with driving circuits formed on the display substrate, whereas Reiner's source driver 61 is a discrete integrated circuit chip." *Id.* at 46 (citing Pet. 46; Ex. 1007 ¶ 1; Ex. 1010 ¶ 1; Ex. 1001, 5:20–23).

Petitioner replies that "Reiner's substrate 16, onto which the drivers are flipped, is the pixel substrate at the contact pad for the source/gate lines" and "Reiner teaches connecting the drivers to the lines of the pixel substrate at contact pads 72" utilizing "'flip-chip technology' to attach the driver to substrate 16, *which describes arranging the driver on the pixel substrate*." Pet. Reply 23 (emphasis added) (citing Ex. 1003 ¶¶ 101, 145–146, 231, 251; Ex. 1005, Figs. 2–5, 7:23–25, 9:11–29, 10:1–6; Ex. 2008, 69:12–73:15, 82:8–17, 87:19–88:13, 93:9–94:1; Ex. 1019, 1; Ex. 1020, 4; Ex. 1021, 20); Ex. 1024 ¶¶ 74–87.

Petitioner also maintains that "[a]rranging the scan lines and gate drivers on a substrate was conventional in the prior art," including mounting flip chips directly on to the glass of an LCD display. Pet. Reply 23 (citing Ex. 1003 ¶ 146; Ex. 1007, Fig. 1, ¶¶ 1, 64; Ex. 1010, Fig. 1, ¶¶ 1, 17; Ex. 1001, 1:57–59). Moreover: "The purpose of Reiner's flip-chip technology is mounting the source/data and gate/scan line drivers ***on*** the LCD panel to realize higher-density integrated circuits and pixels," and "[w]hether other attachment options were available does not change that Reiner discloses, or at least renders obvious, claim 8." *Id.* at 24–25 (citing Ex. 1005, 12:15–18; Ex. 1019, 1; Ex. 1020, 4); Ex. 1024 ¶¶ 85–86.

Patent Owner responds by reiterating its arguments summarized above. *See* PO Sur-reply 18.

We conclude Petitioner has not demonstrated claim 8 is unpatentable by a preponderance of the evidence. First, the express disclosures of Reiner cited by Petitioner are limited to providing a substrate for *integrated circuit device 20* in Figure 2 (whether substrate 16 or substrate 21), which forms *gate/scanning driver 63* in Figure 4. *See* Ex. 1005, Figs. 2 and 4, 6:18–24,

7:22–26, 9:11–29, 10:1–10, 12:15–18. Petitioner does not cite any express disclosure in Reiner that substrate 16 or 21 may be extended into the other components of Reiner's display device, such as LCD screen 60 or source/data driver 61. *See id.*; Pet. 44–50; Pet. Reply 22–25. Such extension is a necessary component of Petitioner's case for unpatentability, because it is how Petitioner addresses the substrate "periphery" and "corner portion" recitations in the claim. *See* Pet. 47–50.

Indeed, Reiner describes how source/data driver 61 utilizes "*contact pads* 72" which are "*connected* (e.g. by means of *bonding*)" to source lines 67 in LCD screen 60. Ex. 1005, Fig. 5, 10:1–6 (emphases added). As Patent Owner points out, this disclosure tends to suggest Reiner's display drivers 61 and 63 are separate structures from LCD screen 60. Figure 5 similarly illustrates these components 60, 61 and 63 as separate boxes. Reiner's disclosures thereby cut against Petitioner's notion that Reiner discloses or suggests utilizing one single substrate for display drivers 61 and 63 and LCD screen 60. There is no support in Reiner's express disclosure for Dr. Murphy's purple box in his annotated version of Figure 4 (reproduced above) illustrating a common substrate for those components. *See* Ex. 1003 ¶ 146.

Petitioner contends "Reiner's substrate 16, onto which the drivers are flipped, *is* the pixel substrate" because "Reiner uses '*flip-chip technology*' to attach the driver to substrate 16, *which describes arranging the driver on the pixel substrate*." Pet. Reply 23 (emphases added). Dr. Murphy correspondingly testifies that "Reiner's 'flip-chip technology' (also called FCOG or COG) *is exactly arranging the gate and source drivers onto the pixel substrates at contact pads*, like those disclosed in Reiner," and "this is

what 'flip-chip technology' ***is***, in particular COG and FCOG." Ex. 1024 ¶¶ 75, 82–83 (citing Ex. 1019, 1; Ex. 1020, 4; Ex. 1021, 20).

However, the evidence does not support Dr. Murphy's alleged equivalence between Reiner's broadly described "well-known flip-chip technology" (Ex. 1005, 7:23–26) and the other prior art's particular uses of flip-chip technology to manufacture LCD displays having a common glass substrate for gate and source drivers and display pixels (*see* Ex. 1019, 1; Ex. 1020, 4; Ex. 1021, 20). Indeed, the other prior art references describe chip on glass technology and flip-chip technology as different concepts, not as the same concept as Dr. Murphy would have it. *See* Ex. 1019, 1 (listing "chip on glass (COG)" and "flip chip" as different index terms, and describing the "chip on glass (COG) technique" as "the driver IC is directly mounted on LCD panels by flip chip"); Ex. 1020, 4 ("Chip on glass (COG) and flip chip on glass (FCOG) are being used to mount the driver IC directly on to the glass LCD.").

Turning then to obviousness, Petitioner asserts and Dr. Murphy testifies that substrate 16 "may include" the substrate for LCD screen 60 along with gate/scanning driver 63, such that display lines 67 and 68 "could be patterned on" substrate 16. Pet. 45–46; Ex. 1003 ¶ 146. However, the fact that Reiner's display device may or could have been manufactured with a common substrate for display drivers 61 and 63 and LCD screen 60 is not a sufficient reasoning to support obviousness. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 991–92 & 993–94 (Fed. Cir. 2017); *InTouch Techs., Inc. v. VGo Commc'ns, Inc.*, 751 F.3d 1327, 1351–52 (Fed. Cir. 2014). Dr. Murphy's testimony, at best, establishes Reiner's display device could have been modified predictably to reach the claimed invention,

and does not provide a rational underpinning for why this would have been done. *See, e.g., Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention."); *InTouch*, 751 F.3d at 1348–49 ("[The expert witness's] testimony was nothing more than impermissible hindsight; she opined that all of the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references.").

Petitioner relies heavily on Reiner's disclosure that: "When packaging the integrated circuit device 20, *it is flipped* onto the substrate 16, according to *the well-known flip-chip technology*." Ex. 1005, 7:23–26 (emphasis added); *see* Pet. 45–46; Ex. 1003 ¶¶ 145–146, 148. Petitioner and Dr. Murphy combine that disclosure with other prior art references allegedly indicating it was "conventional" to utilize flip-chip technology to arrange display drivers and display lines on a common substrate in a display device. *See* Pet. 45–46; Pet. Reply 23; Ex. 1005 ¶ 146 (citing Exs. 1001, 1007, and 1010); Ex. 1024 ¶¶ 75–76, 78, 82–83, 85–87 (further citing Exs. 1019, 1020, and 1021). However, even assuming such conventionality, the fact that the cited prior art would have allowed for the claimed invention, or possibly could be combined to reach the claimed invention, is not a sufficient reasoning to support obviousness. *Personal Web*, 848 F.3d at 991–92 & 993–94 (obviousness requires "a motivation to pick out those two references and combine them to arrive at the claimed invention," and "the amount of explanation needed will vary from case to case, depending on the complexity of the matter and the issues raised in the record" (citations

omitted)); *InTouch Techs.*, 751 F.3d at 1351–52. Petitioner's argument does not proffer a sufficient motivation to combine. *See* Pet. 45–46; Pet. Reply 22–23.

For the foregoing reasons, we conclude Petitioner has not shown by a preponderance of the evidence that claim 8 is unpatentable as having been obvious over Reiner.

4. Claims 1–3, 5–7, and 9–18

Petitioner provides arguments and evidence in support of contending claims 1–3, 5–7, and 9–18 are unpatentable as having been obvious over Reiner, including supporting testimony from Dr. Murphy. *See* Pet. 40–44, 50–71; Ex. 1003 ¶¶ 134–142, 154–227.

As to claims 1, 3, 5–7, 9–13, and 15–18, Patent Owner argues for patentability based solely on arguments considered above in the context of claim 4. *See, e.g.*, PO Resp. 42–43, 47–52. Therefore, Patent Owner has waived any other argument. *See* Inst. Dec. 44; Paper 10, 10. We adopt Petitioner's arguments concerning these claims having been obvious over Reiner as our own in this Decision. *See* Pet. 40–44, 50–56, 57–70, 71; Ex. 1003 ¶¶ 134–142, 154–168, 174–221, 227. Accordingly, we conclude a preponderance of the evidence establishes these claims are unpatentable as having been obvious over Reiner.

As to claims 2 and 14, Patent Owner argues for patentability based on arguments considered above in the context of claim 8. *See* PO Resp. 48, 51–52. Petitioner likewise argues these claims together as a group. *See* Pet. 56, 71; Pet. Reply 26. Accordingly, we conclude Petitioner has not shown by a preponderance of the evidence that claims 2 and 14 are

unpatentable as having been obvious over Reiner, for the reasons expressed above in the context of claim 8.

5. Conclusion as to Ground One

We conclude Petitioner has demonstrated claims 1, 3–7, 9–13, and 15–18 are unpatentable as having been obvious over Reiner, but Petitioner has not demonstrated such unpatentability for claims 2, 8, and 14.

E. Ground Two — Obviousness over Reiner and Takahara

In Ground Two, Petitioner asserts claims 1–18 of the '157 patent are unpatentable as having been obvious over Reiner and Takahara. *See* Pet. 15, 71–89. Ground Two is premised on Ground One (obviousness over Reiner), then relies on Takahara to shore up potential deficiencies in Ground One. *See, e.g.*, Pet. 71–72, 81.

Patent Owner raises various arguments in opposition. *See* PO Resp. 52–73. After considering each of those arguments, we conclude Petitioner has demonstrated claims 1, 3–7, 9–13, and 15–18 are unpatentable as having been obvious over Reiner and Takahara, but Petitioner has not demonstrated such unpatentability for claims 2, 8, and 14.

1. Claim 4

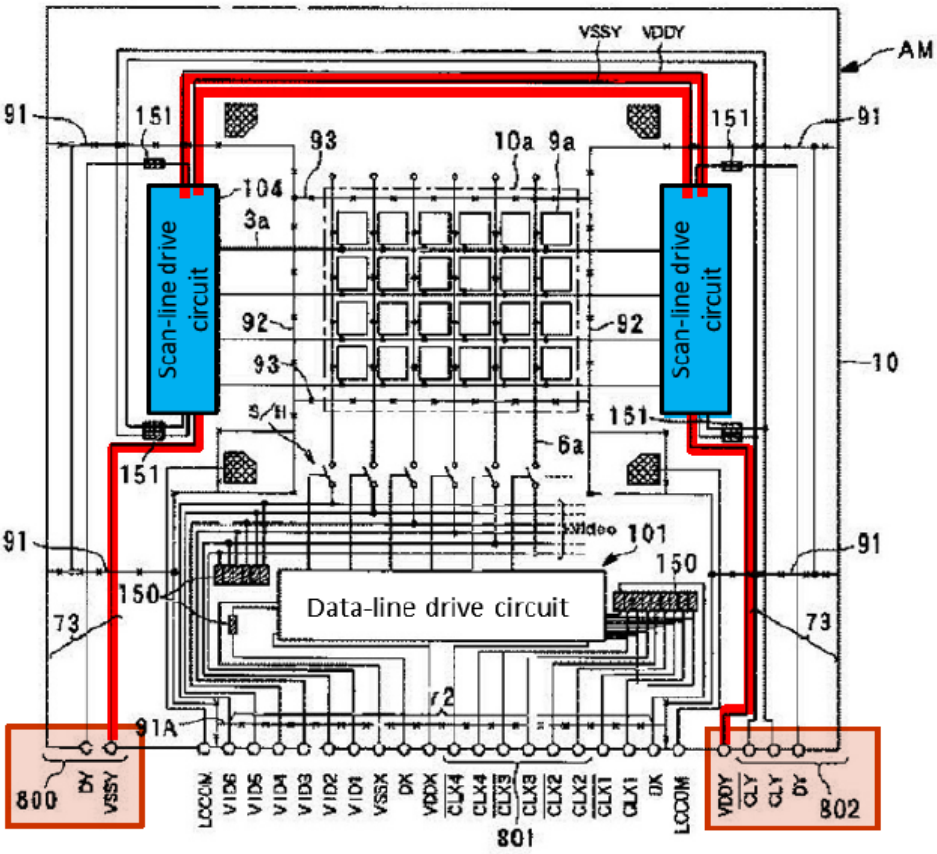
(a) [4c] — An Input Terminal Connected to the Power Supply Line

Limitation [4c] recites the display device comprises "an input terminal connected to the power supply line to supply power." Ex. 1001, 12:31–32.

If it is determined Reiner alone does not disclose or render obvious limitation [4c] in Ground One, then Petitioner contends in Ground Two that it would have been obvious to utilize power input terminals in Reiner in light

of Takahara. *See* Pet. 71–76; Ex. 1003 ¶¶ 228–235. Dr. Murphy's supporting annotations to Figure 1 of Takahara are reproduced below.

FIG. 1



Takahara, Figure 1 (Annotated at Ex. 1003 ¶ 229).

Figure 1 of Takahara is a block diagram schematically illustrating a drive circuit employed in a liquid crystal display panel. *See* Ex. 1007 ¶¶ 57–58. Petitioner cites Takahara as disclosing input terminals 800 and 802 (brown) that respectively provide power to power supply lines VSSY and VDDY (red) for driving a scanning line driving circuit 104 (blue). *See* Pet. 72–73 (citing Ex. 1007, Fig. 1, ¶¶ 63, 65); Ex. 1003 ¶ 229. Petitioner asserts a person of ordinary skill in the art would have been motivated "to provide input terminals on Reiner's power supply lines Vdd, Vss of gate driver 63, which are equivalent to VDDY and VSSY of Takahara" with a reasonable

expectation of success, in order "to supply power because the terminals would have provided a power connection from a power source to gate driver 63." Pet. 73–76 (citing Ex. 1005, 7:23–25, 9:12–14, 9:18–20, 9:27–29, 10:6–10, 12:4–5; Ex. 1007, Fig. 1, ¶¶ 63, 66; Ex. 1001, Fig. 11, 1:54–56, 2:5–14); Ex. 1003 ¶¶ 230–233.

Patent Owner argues Petitioner's combination of Reiner and Takahara does not disclose or render obvious "input terminals of a display device" per limitation [4c]. PO Resp. 52, 58. Patent Owner particularly asserts the combination "at most render[s] obvious input terminals connected to Reiner's lines Vdd and Vss, and those input terminals would be input terminals *of integrated circuit driver 61 . . . separate from the display substrate,"* relying on arguments we have addressed above in Section III.D.2(d) in connection with Ground One concerning limitation [4c]. *Id.* at 58 (emphasis added); Ex. 2009 ¶ 123.

Petitioner replies that "Patent Owner's arguments . . . fail because they relate to Reiner's disclosure, not the asserted combination that includes input terminals [from Takahara]." Pet. Reply 29 (citing Pet. 72–76; PO Resp. 58); Ex. 1024 ¶ 95.

Patent Owner responds by reiterating its arguments summarized above. *See* PO Sur-reply 20.

We conclude Petitioner's contentions are supported by a preponderance of the evidence, for essentially the same reasons provided above in Section III.D.2(d) in relation to Ground One. The addition of Takahara in Ground Two bolsters Petitioner's case, because Takahara demonstrates that it was known to utilize input terminals 800 and 802 for

power supply lines VSSY and VDDY leading to scanning line driving circuits 104. *See* Ex. 1007, Fig. 1, ¶¶ 63, 65–66.

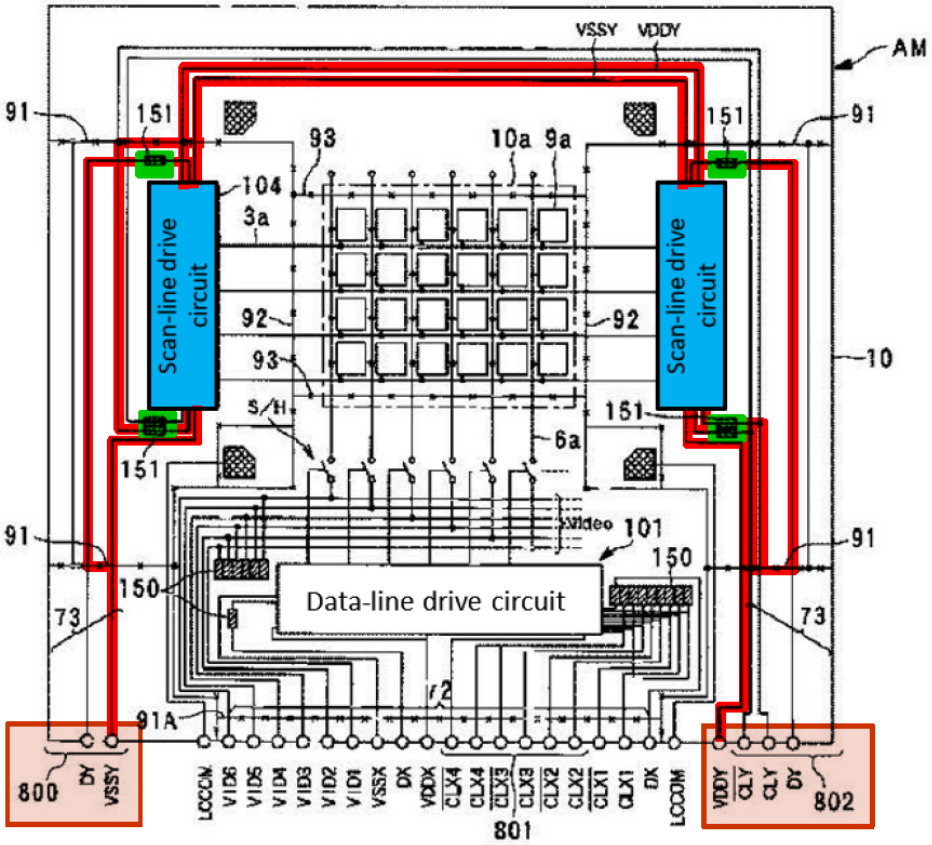
(b) [4d] to [4f] — Whether the Combination of Reiner and Takahara Renders Obvious a Scanning Line Driving Circuit Utilizing First and Second Protection Circuits

Limitations [4d]–[4f] together recite first and second protection circuits connected to the scanning line driving circuit and the power supply line in a particular positional configuration, to protect the scanning line driving circuit. *See* Ex. 1001, 12:33–47.

If it is determined Reiner alone does not show "it would have been obvious to protect the gate driver 63 (scanning line driver circuit) with ESD protection of [4d]–[4f]" in Ground One, then Petitioner contends in Ground Two that "Reiner in view of Takahara would have rendered [this] obvious." Pet. 71–72, 76; Ex. 1003 ¶ 228. In particular, Petitioner cites Takahara as additional evidence of protecting scanning line driving circuits from electrostatic discharge events. *See* Pet. 76–80; Ex. 1003 ¶¶ 234–242.

In support, Dr. Murphy annotates Figure 1 of Takahara, as reproduced below (on the next page).

FIG. 1



Takahara, Figure 1 (Annotated at Ex. 1003 ¶ 235).

Figure 1 of Takahara is a block diagram schematically illustrating a drive circuit employed in a liquid crystal display panel. *See* Ex. 1007 ¶¶ 57–58. Dr. Murphy testifies Figure 1 illustrates electrostatic protection circuits 151 (green) "' . . . formed at intermediate positions of the signal lines' 73, which include power lines VDDY, VSSY" (red), to protect scan line drive circuits 104 (blue). Pet. 76–77 (citing Ex. 1007, Fig. 1, ¶¶ 66, 70); Ex. 1003 ¶ 235. Petitioner contends and Dr. Murphy testifies that Takahara thereby "confirms" the desirability of protecting Reiner's gate/scanning driver 63 from electrostatic discharge events, supporting Petitioner's alleged motivation for a person of ordinary skill in the art to configure driver 63 to include the ESD protection network of Reiner's Figure 5. Pet. 77–80 (citing

Ex. 1005, 2:28–3:1, 4:10–19, 6:12–17, 8:30–31, 9:12–22, 10:10–12, 12:15–18, 14:27–32 (claim 11); Ex. 1007, Figs. 1 and 3, ¶¶ 63, 66; Ex. 1001, 1:25–2:30); Ex. 1003 ¶¶ 236–242.

Patent Owner firstly argues that Takahara's display device "does not close [the] gap" of Reiner's alleged failure to disclose the particular positional configuration of limitation [4f]. PO Resp. 59. In support, Patent Owner asserts Takahara's protection circuits 151 are connected only to *signal* lines not to any *power* lines, and Takahara's scanning line driving circuits 104 are not connected to their power supply lines Vss and Vdd *between* connecting portions at which two protection circuits 151 are connected to those power supply lines. *Id.* at 53–58, 59–68; Ex. 2009 ¶¶ 116–122, 124–137.

Patent Owner secondly argues there is no motivation to combine Reiner and Takahara as proposed by Petitioner. *See* PO Resp. 69; Ex. 2009 ¶¶ 138–140. In particular, according to Patent Owner, a person of ordinary skill in the art "would have no reason to modify Reiner in view of Takahara" because "Reiner provides an ESD protection network for *silicon integrated circuits*," whereas "Takahara provides protection circuits for *signal lines*," and Petitioner "cites no need to combine the teachings of Reiner and Takahara." PO Resp. 69 (emphases added); Ex. 2009 ¶ 139.

Petitioner replies that Takahara's protection circuits 151 *are* connected to *power* lines Vss and Vdd through short-circuit wiring 91 during manufacture of Takahara's display device, despite Patent Owner's arguments to the contrary. *See* Pet. Reply 26–29, 30–36; Ex. 1024 ¶¶ 91–94, 96–110.

Petitioner also asserts "the Petition relies on Takahara for the basic, conventional teaching of protecting a scanning line driver circuit from ESD damage as motivation to protect Reiner's gate/scan line driver with an ESD protection network, *like in Reiner's FIG. 5*." Pet. Reply 30 (emphasis added) (citing Pet. 76–80); *see also* Tr. 23:22–24:20 (discussing the limited nature of Petitioner's reliance on Takahara). Petitioner argues "[t]hat basic teaching is sufficient to render [claim 4] obvious," as we preliminarily determined in the Institution Decision. *Id.* (citing Inst. Dec. 42–43). Concerning motivation for the combination, Petitioner asserts "Patent Owner does not challenge any of the motivations identified in the Petition" including "Reiner's acknowledgement that driver circuits are 'very sensitive' and susceptible to being 'destroyed' by ESD" as well as "Takahara's teaching that ESD protection circuits can 'reliably protect[]' the scan line driver from ESD damage that can render it nonfunctional." *Id.* at 30, 36 (citing Pet. 77–80; Ex. 1003 ¶¶ 113–119, 237–240; Ex. 1018, 51:15–52:19); Ex. 1024 ¶¶ 97, 110–112.

Patent Owner responds by reiterating its arguments summarized above, with additional argument directed to Takahara's short-circuit wiring 91. *See* PO Sur-reply 18–21.

We conclude Petitioner's contentions are supported by a preponderance of the evidence. In particular, Takahara provides protection circuits 151 to protect scan line drive circuits 104 from electrostatic discharge events. *See* Ex. 1007, Fig. 1, ¶ 60. Thus, the addition of Takahara in Ground Two bolsters Petitioner's motivation to combine from Ground One.

Further, as discussed above in Section III.D.2, we find that the display driver illustrated in Reiner's Figure 5 satisfies limitations [4d]–[4f] per Petitioner's Mappings A and B, except that it is a source/data driver rather than a gate/scanning driver as claimed. Thus, there is no "gap" in Reiner for Takahara to fill with regard to the particular positional configuration of claim 4, as Patent Owner would have it. In particular, even if Takahara's protection circuits 151 are only on signal lines and not on power lines as Patent Owner contends, Takahara still supports Petitioner's argument by suggesting that Reiner's gate/scanning driver 63 would benefit by being protected from electrostatic discharge events.

We also determine Patent Owner's arguments attack Reiner and Takahara separately, when Petitioner's case for obviousness relies on their combined teachings. In particular, Petitioner relies on Takahara only as disclosing that ESD protection circuits may be utilized to protect a scan line drive circuit; Petitioner does not propose incorporating Takahara's ESD protection structure into Reiner's gate/scanning driver 63. *See* Pet. 76–80. Petitioner in fact proposes incorporating the ESD protection structure of Reiner's Figure 5 into Reiner's gate/scanning driver 63. *See id.* at 78–80.

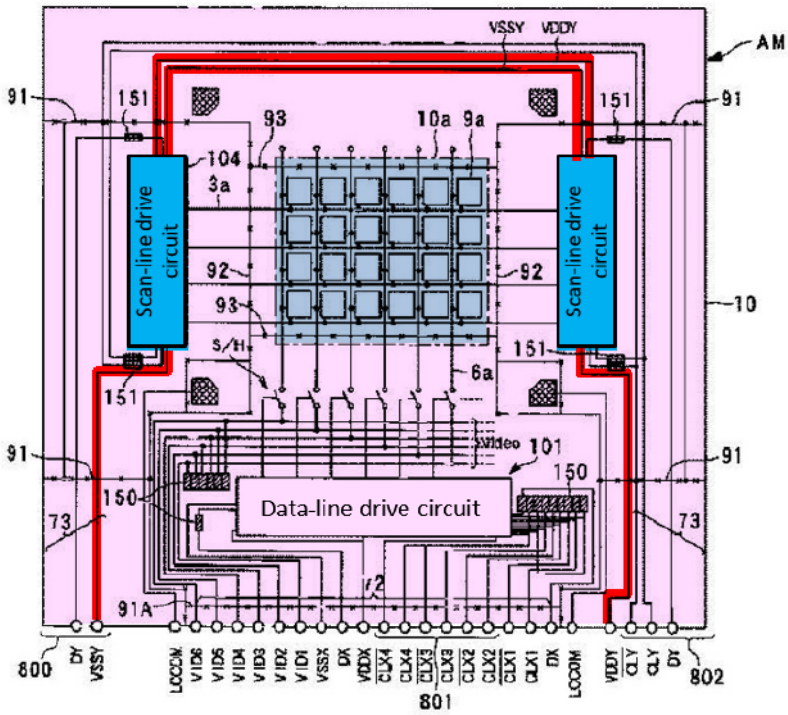
(c) Conclusion as to Claim 4

Other than Petitioner's reliance on Takahara as discussed above, Ground Two relies on Reiner as in Ground One. *See* Pet. 71–80. Therefore, we conclude Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable as having been obvious over Reiner and Takahara.

2. Claim 8

If it is determined "Reiner does not disclose or render obvious the additional limitations of claim 8" in Ground One (as we have done above in Section III.D.3), then Petitioner contends "Reiner and Takahara render them obvious." Pet. 81; Ex. 1003 ¶ 243. In support, Dr. Murphy annotates Figure 1 of Takahara, as reproduced below.

FIG. 1

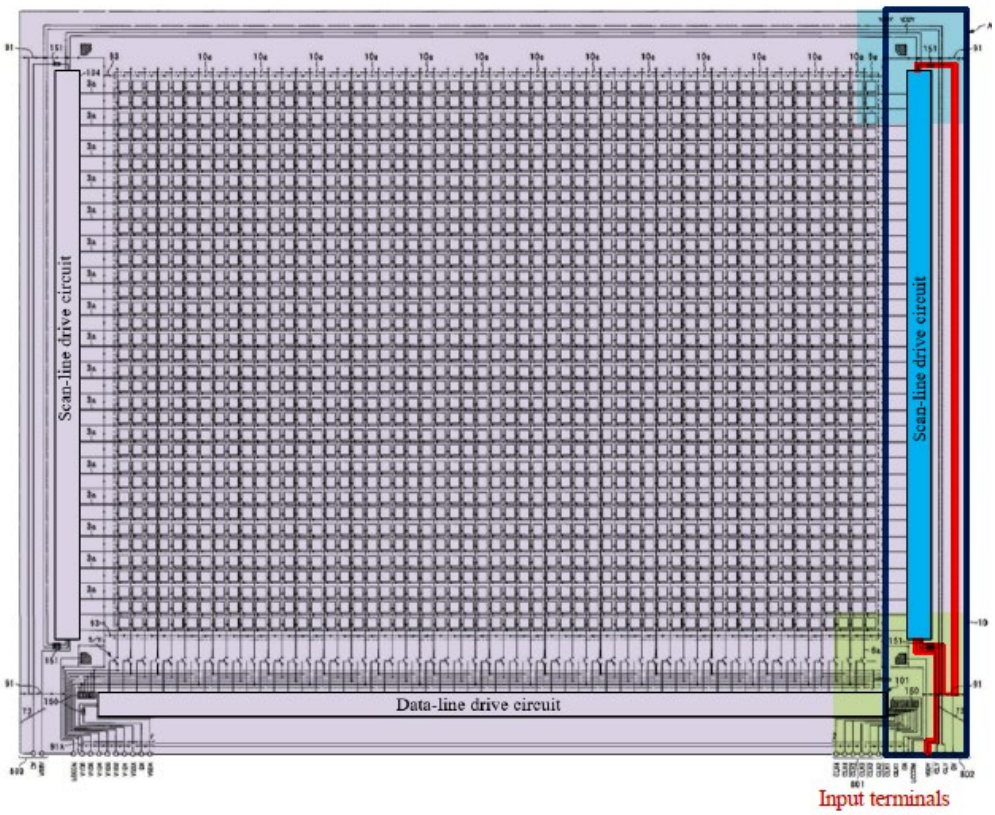


Takahara, Figure 1 (Annotated at Ex. 1003 ¶ 244).

Figure 1 of Takahara is a block diagram schematically illustrating a drive circuit employed in a liquid crystal display panel. *See* Ex. 1007 ¶¶ 57–58. Dr. Murphy testifies Figure 1 illustrates scanning line driving circuits 104 (blue) "arranged on substrate 10 [(pink)] that includes the active matrix for the LCD display" composed of scanning lines 3a and data lines 6a (teal). Pet. 81–82 (citing Ex. 1007, Fig. 1, ¶ 64); Ex. 1003 ¶ 244. Further according to Dr. Murphy, scanning line driving circuits 104 (blue) and their associated

power supply lines VDDY/VSSY (red) "are located on the periphery of substrate 10 [(pink)]." Pet. 81–82 (citing Ex. 1007, Fig. 1, ¶ 62); Ex. 1003 ¶ 244. We accordingly find that Takahara's scanning line driving circuits 104 are arranged on a common substrate 10 with scanning lines 3a and data lines 6a. *See, e.g.*, Ex. 1007, Fig. 1, ¶¶ 57–58, 62–65. Patent Owner does not dispute this finding.

Further according to Petitioner and Dr. Murphy, although Figure 1 of Takahara shows a 4x6 pixel array, a person of ordinary skill in the art "would have recognized that the active matrix typically has several hundred or more scan and data lines." Pet. 83; Ex. 1003 ¶¶ 246–247. Dr. Murphy illustrates this by making a new Figure E, reproduced below.



Dr. Murphy's Figure E (Ex. 1003 ¶ 246).

Dr. Murphy's Figure E extrapolates Takahara's Figure 1 into a larger display, with color coding to identify: substrate 10 (purple) with a lower-right corner (green) and an upper right corner (aqua); scanning line driving circuit 104 (blue); power line VDDY (red); and input terminals 801 and 802 (brown). *See* Pet. 83–85 (citing Ex. 1007, Figs. 1 and 12); Ex. 1003 ¶¶ 246–247. As described by Petitioner, "the peripheral area" in Figure E is "a small fraction of the overall substrate" such that "the ends of the scanning line drive circuits would have included the first and second protection circuits in corner portions of the substrate, as explained in Ground [One], claim 8." Pet. 83; Ex. 1003 ¶ 246.

Petitioner next argues and Dr. Murphy testifies that a person of ordinary skill in the art "would have been motivated to arrange Reiner's source driver 63 on a substrate to support Reiner's LCD display device and provide locations for wiring and circuitry, as taught by Takahara and conventional in the art," for various reasons. Pet. 85–88; Ex. 1003 ¶¶ 248–250. For the following reasons, we conclude none of those reasons is supported by a preponderance of the evidence. *See, e.g.*, PO Resp. 70 ("[E]ven though Takahara teaches forming a scanning line driving circuit on the display substrate," a person of ordinary skill in the art "would not have been motivated to form Reiner's integrated circuit drivers 61 and 63, as described and shown in Figure 5, on a display substrate.").

Petitioner initially asserts a person of ordinary skill in the art would have recognized Reiner's display "would have included a similar configuration [as Takahara's] to be placed on a substrate to support the gate/scan lines 68, the source/data lines 67, pixels, and driver circuits 61, 63" as was "well known in the art." Pet. 82–83 (citing Ex. 1010, Fig. 1,

¶¶ 17–19); Ex. 1024 ¶ 245. For reasons provided above in Section III.D.3, the evidence does not support Petitioner's assertion that Reiner discloses or suggests forming its display drivers 61 and 63 and LCD screen 60 on a common substrate.

Petitioner's first reason for combining Reiner and Takahara to include such a common substrate is that "arrang[ing] Reiner's gate driver 63 on a substrate to connect the gate driver to the scan lines being drive[n] on the substrate" would have "*provide[d] an integrated display unit that can be incorporated into electronic devices (e.g., laptop computer, PDA, television, computer monitor, cellular phone screen)*." Pet. 85–86 (emphasis added) (citing Ex. 1005, Figs. 4 and 5, 6:18–24, 10:1–6; Ex. 1007 ¶ 64); Ex. 1003 ¶ 248. However, Dr. Murphy does not explain why Reiner's display device might have been unsuitable for those display types, or why Takahara's display device might have been particularly suitable for those display types. *See* Ex. 1003 ¶ 248. Dr. Murphy cites paragraph 64 of Takahara, but he does not explain and we do not discern any rational relationship between that disclosure and the possible unsuitability of Reiner or the particular suitability of Takahara for the listed display types. *See id.*; Ex. 1007 ¶ 64. Thus, we conclude Dr. Murphy's testimony in this regard is too conclusory to be persuasive, and is not supported by a preponderance of the evidence.

Petitioner's second reason for combining Reiner and Takahara is that a person of ordinary skill in the art would have "arrange[d] the gate driver on a substrate *to provide external terminals* to power the active matrix and driver circuits and to connect to the CPU and power sources, such as an external power supply or battery." Pet. 86 (emphasis added) (citing Ex. 1007 ¶ 64); Ex. 1003 ¶ 248. However, this reasoning does not have any

rational relationship to the proposed modification of Reiner to form its display drivers 61 and 63 and LCD screen 60 on a common substrate. Dr. Murphy cites paragraph 64 of Takahara, but he does not explain and we do not discern any relationship between that disclosure and the possible unsuitability of Reiner to incorporate power terminal connections or the particular suitability of Takahara for using power terminal connections. *See* Ex. 1003 ¶ 248; Ex. 1007 ¶ 64. Thus, we conclude Dr. Murphy's testimony in this regard is too conclusory to be persuasive, and is not supported by a preponderance of the evidence.

Petitioner's third reason for combining Reiner and Takahara is "to *provide for the power supply lines feeding into Reiner's gate driver 63 to be formed on the substrate*, as shown in Takahara's FIG. 1, because Reiner teaches that the power supply lines run 'perpendicular to' the output lines (scan lines) of the driver circuits." Pet. 86–87 (emphasis added) (citing Ex. 1005, 10:7–10); Ex. 1003 ¶ 249. However, this reasoning does not have any rational relationship to the proposed modification of Reiner to form its display drivers 61 and 63 and LCD screen 60 on a common substrate. Instead, Dr. Murphy's supporting testimony assumes that such a common substrate would have been used per his previous testimony (which we have rejected above), and then explains why the power supply lines also would have been formed in the same common substrate as "the most efficient way." Ex. 1003 ¶ 249. Such efficiency does not explain why, in the first instance, a common substrate would have been used for Reiner's display drivers 61 and 63 and LCD screen 60. *See id.*

Petitioner's fourth reason for combining Reiner and Takahara is: "As explained above in Ground [Two], claim 4, a [person of ordinary skill in the

art] would have been motivated *to form Reiner's circuits directly on Takahara's glass substrate to take advantage of additional protection from ESD events and also improve manufacturing.*" Pet. 88 (emphasis added); *id.* at 88–89 (discussing reasonable expectation of success); Ex. 1003 ¶¶ 250, 252. We have reviewed Petitioner's extensive Ground Two arguments against claim 4 and Dr. Murphy's supporting testimony. *See* Pet. 71–80; Ex. 1003 ¶¶ 228–242. The only reference we found to utilizing Takahara's common glass substrate in Reiner is the argument that a person of ordinary skill in the art "would have found it obvious to form Reiner's gate driver 63 directly on the glass substrate of Takahara, thereby eliminating the need for contact pads 72" because "glass substrates could exacerbate risks of ESD that could damage the gate driver 63 and therefore would have benefitted from ESD protection provided by Reiner's protection circuits." Pet. 74–75; Ex. 1003 ¶¶ 231, 250.

That argument, however, does not provide a rational basis for utilizing Takahara's common glass substrate in Reiner. Indeed, the argument cuts against such a modification, in admitting that glass substrates exacerbate risks of ESD damage. Also, the argument is provided in support of modifying Reiner to include power input terminals per limitation [4c], which has little to do with the material or structure of substrates in the device. *See* Pet. 74–75.

Dr. Murphy's supporting testimony is premised on Reiner disclosing or suggesting that its "gate driver 63 is arranged on a substrate, similar to Takahara's active matrix substrate 10" which is glass. Ex. 1003 ¶ 231. We reject that contention for reasons provided above in Section III.D.3. Dr. Murphy's testimony further pre-supposes that the substrate is glass per

Takahara's disclosure, then concludes it would have been obvious to utilize Reiner's protection circuits ESD1–ESD3 to protect Reiner's gate driver 63, because "using glass substrates can have risks of ESD events and ESD damage because of the insulative properties" such that "the risk of ESD is heightened." Ex. 1003 ¶ 231. Dr. Murphy does not provide any reason for utilizing Takahara's common glass substrate in Reiner's display device. *See id.*

At best, Dr. Murphy's testimony establishes a person of ordinary skill in the art *could* have modified Reiner's display device to form drivers 61 and 63 and LCD screen 60 on a common substrate, as Takahara does. But that is not a sufficient reasoning to support obviousness. *See, e.g.*, *Personal Web*, 848 F.3d at 991–92 & 993–94; *InTouch*, 751 F.3d at 1348–49, 1351–52.

For the foregoing reasons, we conclude Petitioner has not shown by a preponderance of the evidence that claim 8 is unpatentable as having been obvious over Reiner and Takahara.

3. Claim 1–3, 5–7, and 9–18

Petitioner provides arguments and evidence in support of contending claims 1–3, 5–7, and 9–18 are unpatentable as having been obvious over Reiner and Takahara, including supporting testimony from Dr. Murphy. *See* Pet. 89; Ex. 1003 ¶¶ 253–256.

As to claims 1, 3, 5–7, 9–13, and 15–18, Patent Owner argues for patentability based solely on arguments considered above in the context of claim 4. *See, e.g.*, PO Resp. 70–73. Therefore, Patent Owner has waived any other argument. *See* Inst. Dec. 44; Paper 10, 10. We adopt Petitioner's

arguments concerning these claims having been obvious over Reiner and Takahara as our own in this Decision. *See* Pet. 89; Ex. 1003 ¶¶ 253–256. Accordingly, we conclude a preponderance of the evidence establishes these claims are unpatentable as having been obvious over Reiner and Takahara.

As to claims 2 and 14, Patent Owner argues for patentability based on arguments considered above in the context of claim 8. *See* PO Resp. 71, 73. Petitioner likewise argues these claims together as a group. *See* Pet. 89; Pet. Reply 37. Accordingly, we conclude Petitioner has not shown by a preponderance of the evidence that claims 2 and 14 are unpatentable as having been obvious over Reiner and Takahara, for the reasons expressed above in the context of claim 8.

4. Conclusion as to Ground Two

We conclude Petitioner has demonstrated claims 1, 3–7, 9–13, and 15–18 are unpatentable as having been obvious over Reiner and Takahara, but Petitioner has not demonstrated such unpatentability for claims 2, 8, and 14.

IV. SUMMARY OF CONCLUSIONS

In summary, we determine a preponderance of the evidence establishes claims 1, 3–7, 9–13, and 15–18 of the ’157 patent are unpatentable, but does not establish claims 2, 8, and 14 of the ’157 patent are unpatentable, as shown in the following table.[12]

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[12] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or*

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–18	103(a)	Reiner	1, 3–7, 9–13, 15–18	2, 8, 14
1–18	103(a)	Reiner, Takahara	1, 3–7, 9–13, 15–18	2, 8, 14
Overall Outcome			1, 3–7, 9–13, 15–18	2, 8, 14

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 3–7, 9–13, and 15–18 of the '157 patent have been proven by a preponderance of the evidence to be unpatentable;

FURTHER ORDERED that claims 2, 8, and 14 of the '157 patent have not been proven by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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