Fully Integrated Power Management with Switch Mode Charger

Check for Samples: TWL6030

FEATURES

- **Seven highly efficient 6-MHz buck converters**
  - **Two 0.6 to 2.1 V @ 1.6 A**
  - **Five 0.6 to 2.1 V @ 1.0 A**
- **11 General-purpose LDOs**
  - **Six 1.0 to 3.3 V @ 0.2 A with battery or preregulated supply (One can be used as a vibrator driver.)**
  - **One 1.0 to 3.3 V @ 50 mA with battery or preregulated supply**
  - **One low noise 1.0 to 3.3 V @ 50 mA with battery or preregulated supply**
  - **3.3 V @ 35 mA USB LDO**
  - **One LDO for TWL6030 internal use**
  - **One LDO for internal and external use**
- **USB OTG module**
- **Backup battery charger**
- **10-bit ADC with 17 input channels**
- **13-bit Coulomb counter with four programmable integration periods**
- **Low power consumption**
  - **5 µA in backup mode**
  - **20 µA in wait-on mode**
  - **110 µA in deep sleep, with two DCDCs active**
- **RTC with alarm wake-up mechanism**
- **SIM and MMC card detections**
- **Two digital PWM outputs**
- **Thermal monitoring**
  - **High-temperature warning**
  - **Thermal shutdown**
- **Control**
  - **Configurable power-up and power-down sequences (EPROM programmable)**
  - **Three output signals that can be included in the start-up sequence**
  - **Two I^2C™ interfaces**
  - **All resources configurable by I^2C**
- **Clock management**

  32-kHz output
- **Battery charger 1.5 A**
  - **Charger for single-cell Li-Ion and Li-Polymer battery packs**
  - **Switched mode charger with integrated power FET for up to 1.5-A current**
  - **High-accuracy voltage and current regulation**
  - **Safety timer and reset control**
  - **Thermal regulation protection**
  - **Input/output overvoltage protection**
  - **Charging indicator LED driver**
  - **Boost mode operation for USB OTG**
  - **Compliant with:**
    - **USB 2.0**
    - **OTG and EH 2.0**
    - **YD/T 1591-2006**
    - **USB battery charging 1.1 and 1.2**
    - **Japanese battery charging requirements**
- **Package 7 mm x 7 mm 187-pin nFBGA**

APPLICATIONS

- **Mobile phones and smart phones**
- **Gaming handsets**
- **Portable media players**
- **Portable navigation systems**
- **Handheld devices**
- **Tablets**

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DESCRIPTION

The TWL6030 device is an integrated power-management integrated circuit (IC) for applications powered by a rechargeable battery. The device provides seven configurable step-down converters with up to 1.6A capability for memory, processor core, I/O, auxiliary, preregulation for LDOs, etc. The device also contains 11 LDO regulators that can be supplied from a battery or a preregulated supply. Power-up/power-down controller is configurable and can support any power-up/power-down sequences (EPROM based). The real-time clock (RTC) provides a 32-kHz output buffer, second/minute/hour/day/month/year information, and alarm wake up. The TWL6030 supports 32-kHz clock generation based on a crystal oscillator. The device integrates a switched-mode charger allowing faster battery charge, higher efficiency, and less power dissipation.

The TWL6030 device generates power supplies for OMAP™ 4 processors and operates together with the TWL6040 device, which includes all audio and related detection features. For audio IC parameters, see the TWL6040 datasheet. In addition, the TWL6030 device can be used as a power management multichannel IC (PMIC) for several other processors, thanks to the programmable startup/shutdown controller and default supply voltage levels. The TWL6030 is available in an nFBGA package, 7.0 mm x 7.0 mm, with a 0.4-mm ball pitch.

Figure 1 shows the TWL6030 block diagram.

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Table 1. Part Number Differentiation

PART NUMBER	ORDERING	OMAP VERSION	PRIMARY WATCHDOG	HW CHARGER WATCHDOG	TRANSPORT MEDIA QUANTITY
TWL6030	TWL6030B107CMRR	OMAP4430	Disabled	Disabled	Tape and reel, 2500
TWL6030	TWL6030B107CMR	OMAP4430	Disabled	Disabled	Trays, 260
TWL6030	(P)TWL6030B1AECMRR	OMAP4430	Disabled	Enabled	Tape and reel, 2500
TWL6030	(P)TWL6030B1AECMR	OMAP4430	Disabled	Enabled	Trays, 260
TWL6030	(P)TWL6030B1A0CMRR	OMAP4430	Enabled	Enabled	Tape and reel, 2500
TWL6030	(P)TWL6030B1A0CMR	OMAP4430	Enabled	Enabled	Trays, 260
TWL6030	TWL6030B1A4CMRR	OMAP4460/4470	Disabled	Disabled	Tape and reel, 2500
TWL6030	TWL6030B1A4CMR	OMAP4460/4470	Disabled	Disabled	Trays, 260
TWL6030	(P)TWL6030B1AFCMRR	OMAP4460/4470	Disabled	Enabled	Tape and reel, 2500
TWL6030	(P)TWL6030B1AFCMR	OMAP4460/4470	Disabled	Enabled	Trays, 260
TWL6030	(P)TWL6030B1AACMRR	OMAP4460/4470	Enabled	Enabled	Tape and reel, 2500
TWL6030	(P)TWL6030B1AACMR	OMAP4460/4470	Enabled	Enabled	Trays, 260

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DEVICE INFORMATION

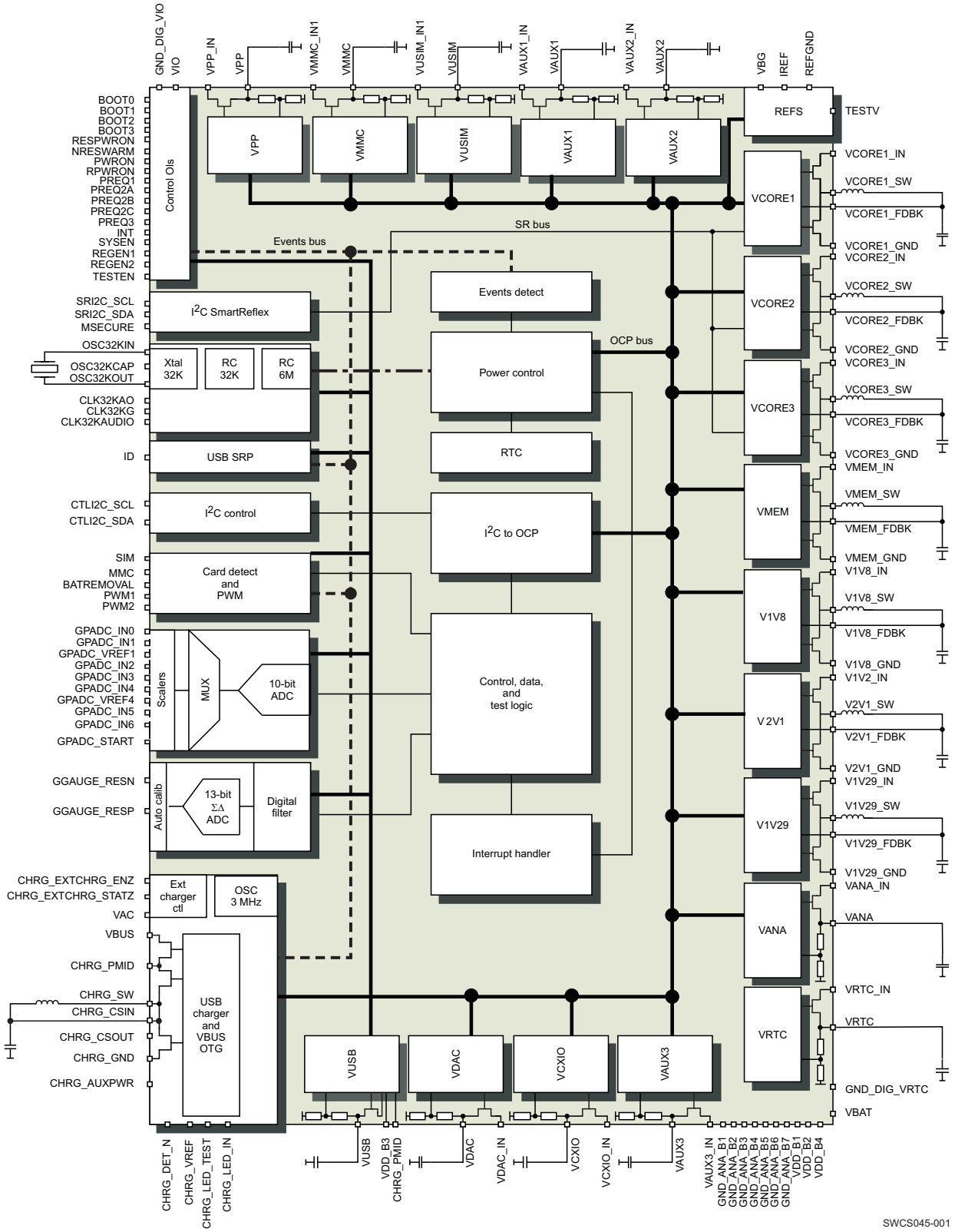

Figure 1. TWL6030 Block Diagram

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Table 2 presents the ball description of the TWL6030 device. Figure 2 shows the ball mapping from the top view.

Table 2. Ball Description

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
CHARGER						
CHRG_AUXPWR	E6	Analog	I	Switched charger auxiliary power supply, connected to the battery pack to provide power in high-impedance mode	Ground	–
CHRG_BOOT	G2	Analog	O	Switched charger boot-strapped capacitor for the high-side MOSFET gate driver	Floating	–
CHRG_CSIN	E4	Analog	I	Switched charger current-sense input	Ground	
CHRG_CSOUT	D4	Analog	I	Switched charger battery voltage/current sense input	Ground	
CHRG_DET_N	E5	Analog	I	USB charging port detection signal from USB PHY	Ground	
CHRG_EXTCHRG_EN Z	J7	Digital	O	Output control signal to an external VAC charger	Floating	
CHRG_EXTCHRG_ST ATZ	H7	Digital	I	External charger status input pin	Floating or tied to VRTC (fixed internal pullup to VRTC)	*PU 70–190 kΩ
CHRG_LED_IN	D6	Power	I	LED indicator input supply	Ground	
CHRG_LED_TEST	D5	Analog	I/O	External LED driver output/dedicated charger TEST ball	Ground or floating	
CHRG_PGND_B1	A5	Ground	I	Switched charger power ground	Ground	–
CHRG_PGND_B2	A6					
CHRG_PGND_B3	B6					
CHRG_PGND_B4	B5					
CHRG_PMID_B1	E1	Analog	O	Switched charger connection point between reverse blocking MOSFET and high-side switching MOSFET	Floating	–
CHRG_PMID_B2	F1					
CHRG_PMID_B3	E2					
CHRG_PMID_B4	F2					
CHRG_SW_B1	A3	Power	O	Switched charger internal switch to output inductor connection	Floating	–
CHRG_SW_B2	A4					
CHRG_SW_B3	B4					
CHRG_SW_B4	B3					
CHRG_VREF	F5	Analog	O	Switched charger internal bias regulator voltage	Floating	–
VAC	F4	Power		Input supply from an external VAC charger	Ground (if not used in BBS)	–
VBUS_B1	C1	Power	I/O	VBUS input voltage, USB battery charger power supply	Ground (Must be connected to VBUS if VBUS detection from PMIC is needed; for example, for USB bootupt)	–
VBUS_B2	D1					
VBUS_B3	C2					
VBUS_B4	D2					
POWER SUPPLIES						

(1) I = Input; O = Output
(2) PU/PD shows the pullup/down resistors on digital input lines. An asterisk indicates the default option.

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Table 2. Ball Description (continued)

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
GND_ANA_B1	N8	Ground	I	Analog power ground	Ground	–
GND_ANA_B2	M10					
GND_ANA_B3	E11					
GND_ANA_B4	L13					
GND_ANA_B5	D9					
GND_ANA_B6	H4					
GND_ANA_B7	G7					
GND_DIG_VIO	M8	Ground	I	VIO digital ground	Ground	–
GND_DIG_VRTC	G4	Ground	I	VRTC digital ground	Ground	–
PBKG_B11	T1	Substrate	I	Substrate ground	Ground	–
PBKG_B12	T2					
PBKG_B13	R1					
PBKG_B2	H5					
PBKG_B31	T16					
PBKG_B32	T15					
PBKG_B33	R16					
PBKG_B41	A1					
PBKG_B42	A2					
PBKG_B43	B1					
PBKG_B51	A16					
PBKG_B53	B16					
VDD_B1	N9	Power	I	Analog input voltage supply	N/A	–
VDD_B2	G13					
VDD_B3	B9					
VDD_B4	L4					
VIO	M9	Power	I	The TWL6030 device digital I/O input supply voltage (1.8 V)	N/A	–
VPROG	G10	Power	I	EPROM programming voltage	Ground	–
VBACKUP	E10	Analog	I	Backup battery input voltage	Ground (prefered) or Floating	–
VBAT	B13	Power	I	Battery voltage sense line	N/A	–
CLOCKING						
CLK32KAO	H10	Digital	O	32-kHz digital output clock always on when VIO input supply is present	Floating	–
CLK32KAUDIO	E9	Digital	O	32-kHz digital gated output clock toward the audio device	Floating	–
CLK32KG	J10	Digital	O	32-kHz digital gated output clock controlled by software	Floating	–
OSC32KCAP	E8	Analog	O	VRTC power supply external filtering cap for the 32-kHz crystal oscillator	Floating	–
OSC32KIN	A10	Analog	I	32-kHz crystal oscillator input or digital clock input	Digital clock input,analog clock input	–
OSC32KOUT	A8	Analog	O	32-kHz crystal oscillator output or floating in case of digital clock input	Floating when digital clock input, capacitor when analog clock input	–
REFERENCES						
IREF	H12	Analog	I/O	Reference current generation	N/A	–

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Table 2. Ball Description (continued)

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
REFGND_B1	A9	Ground	I	System reference ground	Ground	–
REFGND_B2	F12					
VBG	G12	Analog	O	Band gap output reference voltage	N/A	–
TESTING						
TESTEN	J8	Digital	I	Test mode enable	Ground (fixed internal pulldown to ground)	*PD 170–950 kΩ
TESTV	A15	Analog	O	Internal voltages sense line	Floating	
SYSTEM CONTROL						
CTLI2C_SCL	M4	Digital	I/O	Control I^2C serial clock (I^2C voltage level is set by an external pullup.)	N/A	PU 0.46–1.76 kΩ
CTLI2C_SDA	N4	Digital	I/O	Control I^2C serial bidirectional data (I^2C voltage level is set by an external pullup.)	N/A	PU 0.46–1.76 kΩ
INT	K10	Digital	O	Maskable interrupt output request to the host processor	Floating	–
BATREMOVAL	L12	Digital	O	Battery removal indicator	Floating	
BOOT0	H8	Digital	I	Boot ball 0 for power-up sequence selection	Ground or VRTC	
BOOT1	G8	Digital	I	Boot ball 1 for power-up sequence selection	Ground or VRTC	
BOOT2	G9	Digital	I	Boot ball 2 for power-up sequence selection	Ground or VRTC	
BOOT3	H9	Digital	I	Boot ball 3 for power-up sequence selection	Ground or VRTC	
NRESPWRON	N5	Digital	O	System reset/power on output	Floating	*PU 70–190 kΩ
NRESWARM	M5	Digital	I	Warm reset input	Floating (fixed internal pullup to VIO)	PU 170–950 kΩ
PREQ1	J9	Digital	I	Peripheral 1 power request input	Floating (use of internal PU/PD) or tied to common ground or VIO (depending on selected sensitivity)	PU/*PD 170–950 kΩ
PREQ2A	K9	Digital	I	Peripheral 2A power request input	Floating (use of internal PU/PD) or tied to common ground or VIO (depending on selected sensitivity)	PU/*PD 170–950 kΩ
PREQ2B	K8	Digital	I	Peripheral 2B power request input	Floating (use of internal PU/PD) or tied to common ground or VIO (depending on selected sensitivity)	PU/*PD 170–950 kΩ
PREQ2C	M7	Digital	I	Peripheral 2C power request input	Floating (use of internal PU/PD) or tied to common ground or VIO (depending on selected sensitivity)	PU/*PD 170–950 kΩ

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Table 2. Ball Description (continued)

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
PREQ3	N6	Digital	I	Peripheral 3 power request input	Floating (use of internal PU/PD) or tied to common ground or VIO (depending on selected sensitivity)	PU/*PD 170–950 kΩ
PWM1	M11	Digital	O		Floating	–
PWM2	M12	Digital	O	Pulse width modulation 2	Floating	–
PWRON	L5	Digital	I	External on-button switch-on event (primary input to launch system wakeup)	N/A	*PU 55–370 kΩ
REGEN1	K7	Digital	O	External regulator enable 1	Floating	–
REGEN2	J5	Digital	O	External regulator enable 2	Floating	–
RPWRON	K5	Digital	I	External remote switch-on event (secondary input to launch system wakeup)	Floating (fixed internal pull-up to VBAT)	*PU 55–370 kΩ
SYSEN	M6	Digital	O	External system enable	Floating	–
MSECURE	N2	Digital	I	Secure mode input. Allow I^2C access to secure registers.	Ground or floating	*PD 170–950 kΩ
SRI2C_SCL	M13	Digital	I/O	SmartReflex™ I^2C serial clock (I^2C voltage level is set by an external pullup.)	Internal pullup on VIO	PU 0.46–1.76 kΩ
SRI2C_SDA	N13	Analog	I/O	SmartReflex I^2C serial data (I^2C voltage set by an external pullup.)	Internal pullup on VIO	PU 0.46–1.76 kΩ
DETECTION						
ID	E12	Digital	I/O	USB connector identification signal	Floating (Internal pull-up to VUSB)	–
MMC	N11	Digital	I	MMC card insertion and extraction detection to deactivate the VMMC LDO	Internal pullup to VIO or pulldown to ground	PU/*PD 70–190 kΩ
SIM	N12	Power	I	SIM card insertion and extraction detection to deactivate the VUSIM LDO	Internal pullup to VIO or pulldown to ground	PU/*PD 70–190 kΩ
LDO REGULATORS						
VANA	B10	Power	O	Output voltage for VANA regulator	N/A	–
VANA_IN	D10	Power	I	Supply of output stage of VANA regulator	VBAT	–
VAUX1	T8	Power	O	Output voltage for VAUX1 regulator	Floating	–
VAUX1_IN	N7	Power	I	Supply of output stage of VAUX1 regulator	VBAT	–
VAUX2	T9	Power	O	Output voltage for VAUX2 regulator	Floating	–
VAUX2_IN	N10	Power	I	Supply of output stage of VAUX2 regulator	VBAT	–
VAUX3	R9	Power	O	Output voltage for VAUX3 regulator (vibrator driver output)	Floating	–
VAUX3_IN	R8	Power	I	Supply of output stage of VAUX3 regulator	VBAT	–
VCXIO	F15	Power	O	Output voltage for VCXIO regulator	Floating	–
VCXIO_IN	F13	Power	I	Supply of output stage of VCXIO regulator	VBAT	–
VDAC	G15	Power	O	Output voltage for VDAC regulator	Floating	–
VDAC_IN	H13	Power	I	Supply of output stage of VDAC regulator	VBAT	–
VMMC	J13	Power	O	Output voltage for VMMC regulator	Floating	–
VMMC_IN	J12	Power	I	Supply 1 of output stage of VMMC regulator	VBAT	–
VPP	K4	Power	O	Output voltage for VPP regulator	Floating	–
VPP_IN	J4	Power	I	Supply of output stage of VPP regulator	VBAT	–
VRTC	D7	Power	O	Output voltage for VRTC regulator	N/A	–

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Table 2. Ball Description (continued)

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
VRTC_IN	D11	Power	I	Input voltage supply for VRTC regulator	VBAT	–
VUSB	A7	Power	O	Output voltage for VUSB regulator	Floating	–
VUSIM	B8	Power	O	Output voltage for VUSIM regulator	Floating	–
VUSIM_IN	D8	Power	I	Supply 1 of output stage of VUSIM regulator	VBAT	–
MONITORING						
GGAUGE_RESN	D13	Analog	I	Sense resistor input signal negative (ground side)	Ground	–
GGAUGE_RESP	E13	Analog	I	Sense resistor input signal positive (battery negative side)	Ground	–
GPADC_IN0	D12	Analog	I/O	General-purpose analog-to-digital converter (GPADC) input 0	Ground/VRTC	–
GPADC_IN1	B11	Analog	I/O	GPADC input 1	Ground	–
GPADC_VREF1	A11	Analog	O	GPADC output reference 1	Floating	–
GPADC_IN2	B14	Analog	I	GPADC input 2	Ground	–
GPADC_IN3	A13	Analog	I	GPADC input 3	Ground	–
GPADC_IN4	B12	Analog	I/O	GPADC input 4	Ground	–
GPADC_VREF4	A12	Analog	O	GPADC output reference 4	Floating	–
GPADC_IN5	A14	Analog	I	GPADC input 5	Ground	–
GPADC_IN6	B15	Analog	I	GPADC input 6	Ground	–
GPADC_START	K12	Digital	I	Trigger hardware request to start GPADC synchronous conversion	Ground	*PD 170–950 kΩ
SMPS REGULATORS						
V1V29_FDBK	G16	Analog	I	V1V29 SMPS feedback	Ground	–
V1V29_GND_B1	H16	Ground	I	V1V29 SMPS ground	Ground	–
V1V29_GND_B2	H15					
V1V29_IN_B1	K16	Power	I	V1V29 SMPS input voltage	VBAT	–
V1V29_IN_B2	K15					
V1V29_SW_B1	J16	Power	O	V1V29 SMPS switch	Floating	–
V1V29_SW_B2	J15					
V1V8_FDBK	L15	Analog	I	V1V8 SMPS feedback	Ground	–
V1V8_GND_B1	M16	Ground	I	V1V8 SMPS ground	Ground	–
V1V8_GND_B2	L16					
V1V8_GND_B3	M15					
V1V8_IN_B1	T13	Power	I	V1V8 SMPS input voltage	VBAT	–
V1V8_IN_B2	T14					
V1V8_IN_B3	R14					
V1V8_SW_B1	N16	Power	O	V1V8 SMPS switch	Floating	–
V1V8_SW_B2	P16					
V1V8_SW_B3	P15					
V2V1_FDBK	F16	Analog	I	V2V1 SMPS feedback	Ground	–
V2V1_GND_B1	E16	Ground	I	V2V1 SMPS ground	Ground	–
V2V1_GND_B2	E15					
V2V1_IN_B1	C16	Power	I	V2V1 SMPS input voltage	VBAT	–
V2V1_IN_B2	C15					
V2V1_SW_B1	D16	Power	O	V2V1 SMPS switch	Floating	–
V2V1_SW_B2	D15					
VMEM_FDBK	R13	Analog	I	VMEM SMPS feedback	Ground	–

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Table 2. Ball Description (continued)

NAME	BALL	TYPE	I/O (1)	DESCRIPTION	CONNECTION IF NOT USED	PU/PD (2)
VMEM_GND_B1	T12	Ground	I	VMEM SMPS ground	Ground	–
VMEM_GND_B2	R12					
VMEM_IN_B1	T10	Power	I	VMEM SMPS input voltage	VBAT	–
VMEM_IN_B2	R10					
VMEM_SW_B1	T11	Power	O	VMEM SMPS switch	Floating	–
VMEM_SW_B2	R11					
VCORE1_FDBK	L2	Analog	I	VCORE1 SMPS feedback	Ground	–
VCORE1_GND_B1	M1	Ground	I	VCORE1 SMPS ground	Ground	–
VCORE1_GND_B2	L1					
VCORE1_GND_B3	M2					
VCORE1_IN_B1	T4	Power	I	VCORE1 SMPS input voltage	VBAT	–
VCORE1_IN_B2	T3					
VCORE1_IN_B3	R3					
VCORE1_SW_B1	N1	Power	O	VCORE1 SMPS switch	Floating	–
VCORE1_SW_B2	P1					
VCORE1_SW_B3	P2					
VCORE2_FDBK	R4	Analog	I	VCORE2 SMPS feedback	Ground	–
VCORE2_GND_B1	T5	Ground	I	VCORE2 SMPS ground	Ground	–
VCORE2_GND_B2	R5					
VCORE2_IN_B1	T7	Power	I	VCORE2 SMPS input voltage	VBAT	–
VCORE2_IN_B2	R7					
VCORE2_SW_B1	T6	Power	O	VCORE2 SMPS switch	Floating	–
VCORE2_SW_B2	R6					
VCORE3_FDBK	G1	Analog	I	VCORE3 SMPS feedback	Ground	–
VCORE3_GND_B1	H1	Ground	I	VCORE3 SMPS ground	Ground	–
VCORE3_GND_B2	H2					
VCORE3_IN_B1	K1	Power	I	VCORE3 SMPS input voltage	VBAT	–
VCORE3_IN_B2	K2					
VCORE3_SW_B1	J1	Power	O	VCORE3 SMPS switch	Floating	–
VCORE3_SW_B2	J2					
RESERVED PINS						
RESERVED1	N15			Reserved (tied to ground)	Ground (3)	
RESERVED2	K13			Reserved (to be left floating)	Floating (4)	
RESERVED3	B7			Reserved(to be left floating)	Floating (5)	

(3) Float is also possible
(4) Connected to VMMC_IN1 is also possible
(5) Connected to VUSIM_IN1 is also possible

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	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
T	PBKG _B31	PBKG _B32	V1V8 _IN _B2	V1V8 _IN _B1	VMEM _GND _B1	VMEM _SW _B1	VMEM _IN _B1	VAUX2	VAUX1	VCORE 2_IN _B1	VCORE 2_SW _B1	VCORE 2_GND _B1	VCORE 1_IN _B1	VCORE 1_IN _B2	PBKG _B12	PBKG _B11	T
R	PBKG _B33		V1V8 _IN _B3	VMEM _FDBK	VMEM _GND _B2	VMEM _SW _B2	VMEM _IN _B2	VAUX3	VAUX 3 _IN	VCORE 2_IN _B2	VCORE 2_SW _B2	VCORE 2_GND _B2	VCORE 2 _FDBK	VCORE 1_IN _B3		PBKG _B13	R
P	V1V8 _SW _B2	V1V8 _SW _B3													VCORE 1_SW _B3	VCORE 1_SW _B2	P
N	V1V8 _SW _B1	RESERVED 1		SR I2C _SDA	SIM	MMC	VAUX 2 _IN	VDD _B1	GND _ANA _B1	VAUX 1 _IN	PREQ3	NRESP WRON	CTL I2C _SDA		MSE CURE	VCORE 1_SW _B1	N
M	V1V8 _GND _B1	V1V8 _GND _B3		SR I2C _SCL	PWM2	PWM1	GND _ANA _B2	VIO	GND _DIG _VIO	PREQ 2C	SYSEN	NRES WARM	CTL I2C _SCL		VCORE 1_GND _B3	VCORE 1_GND _B1	M
L	V1V8 _GND _B2	V1V8 _FDBK		GND _ANA _B4	BAT RE MOVAL							PWR ON	VDD _B4		VCORE 1 _FDBK	VCORE 1_GND _B2	L
K	V1V29 _IN _B1	V1V29 _IN _B2		RESERVED 2	GPADC_ START		INT	PREQ2A	PREQ2B	REGEN 1		RPWR ON	VPP		VCORE 3_IN _B2	VCORE 3_IN _B1	K
J	V1V29 _SW _B1	V1V29 _SW _B2		VMMC	VMMC _IN		CLK 32K G	PREQ1	TEST EN	CHRG _EXT CHRG _ENZ		REGEN 2	VPP _IN		VCORE 3_SW _B2	VCORE 3_SW _B1	J
H	V1V29 _GND _B1	V1V29 _GND _B2		VDAC _IN	IREF		CLK 32K AO	BOOT3	BOOT0	CHRG _EXT CHRG_ STATZ		PBKG _B2	GND _ANA _B6		VCORE 3_GND _B2	VCORE 3_GND _B1	H
G	V1V29 _FDBK	VDAC		VDD _B2	VBG		VPROG	BOOT2	BOOT1	GND _ANA _B7			GND _DIG _VRTC		CHRG _BOOT	VCORE 3 _FDBK	G
F	V2V1 _FDBK	VCXIO		VCXIO _IN	REF GND _B2							CHRG _VREF	VAC		CHRG _PMID _B4	CHRG _PMID _B2	F
E	V2V1 _GND _B1	V2V1 _GND _B2		G GAUGE _RESP	ID	GND _ANA _B3	VBACK UP	CLK 32K AUDIO	OSC 32K CAP		CHRG _AUX PWR	CHRG_ DET_N	CHRG _CSIN		CHRG _PMID _B3	CHRG _PMID _B1	E
D	V2V1 _SW _B1	V2V1 _SW _B2		G GAUGE _RESN	GPADC _IN0	VRTC _IN	VANA _IN	GND _ANA _B5	VUSIM _IN	VRTC	CHRG _LED_IN	CHRG _LED _TEST	CHRG_ CSOUT		VBUS _B4	VBUS _B2	D
C	V2V1 _IN _B1	V2V1 _IN _B2													VBUS _B3	VBUS _B1	C
B	PBKG _B53	GPADC _IN6	GPADC _IN2	VBAT	GPADC _IN4	GPADC _IN1	VANA	VDD _B3	VUSIM	RESERVED 3	CHRG _PGND _B3	CHRG _PGND _B4	CHRG _SW _B3	CHRG _SW _B4		PBKG _B43	B
A	PBKG _B51	TESTV	GPADC _IN5	GPADC _IN3	GPADC _VREF4	GPADC _VREF1	OSC 32K IN	REF GND _B1	OSC 32K OUT	VUSB	CHRG _PGND _B2	CHRG _PGND _B1	CHRG _SW _B2	CHRG _SW _B1	PBKG _B42	PBKG _B41	A
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

SWCS045-003

Figure 2. TWL6030 Package Top View Ball Mapping

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SAMSUNG EX. 1034 - 11/101

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
All battery-related input balls (LDOs and SMPSs) and supply voltage: VBAT, VDD, _IN	–0.3	5.5	V
All battery SMPS-related input balls _FDBK	–0.3	VOUTmax + 0.3	V
Backup battery supply voltage VBACKUP	–0.3	5.5	V
I/O digital supply voltage VIO	–0.3	VIOmax + 0.3	V
Battery charger supply voltage VBUS	-0.3	20.0	V
Battery charger supply voltage VAC	–0.3	20.0	V
Battery charger CHRG_PMID	–0.3	20.0	V
Battery charger CHRG_SW, CHRG_BOOT	–0.7	20.0	V
Voltage difference between CSIN and CSOUT inputs (V_{CSIN}-V_{CSOUT})	–7	7	V
Battery charger CHRG_VREF	–0.3	6.5	V
Battery charger CHRG_DET_N	–0.3	VUSBmax + 0.3	V
All other charger analog-related input balls, such as CHRG_AUXPWR, CHRG_CSIN, CHRG_CSOUT, and CHRG_LED_IN	–0.3	5.5	V
Voltage on the USB OTG ID ball	–0.3	5.5	V
Voltage on the VRTC GPADC balls: GPADC_IN0, GPADC_IN1, and GPADC_IN4	–0.3	VRTCmax + 0.3	V
Voltage on the VANA GPADC balls: GPADC_IN2, GPADC_IN3, GPADC_IN5, and GPADC_IN6	–0.3	VANAmax + 0.3	V
Voltage on the VDD_B3 GPADC balls	–0.3	5.5	V
Voltage on the crystal oscillator OSC32KIN ball	–0.3	VRTCmax + 0.3	V
Voltage on all other analog input balls such as GGAUGE_RESN, GGAUGE_RESP	–0.3	VANAmax + 0.3	V
EPROM supply voltage VPROG	–0.3	20.0	V
Voltage on VRTC digital input balls	–0.3	VRTCmax + 0.3	V
Voltage on VIO digital input balls	–0.3	VIOmax + 0.3	V
Voltage on VBAT digital input balls	–0.3	VBAT + 0.3 ≤ 5.5	V
External buck boost supply voltage	–0.3	5.5	V
Junction temperature range	–45	150	°C
Peak output current on all other terminals than power resources	–5.0	5.0	mA

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Main battery supply voltage VBAT	2.5	3.8	4.8	V
All battery-related input balls VDD_B[1..4]	2.5	3.8	4.8	V
Preregulated LDO-related input balls _IN	1.8	3.8	4.8	V
Other LDO-related input balls _IN	2.3	3.8	4.8	V
All battery SMPS-related input balls _IN	2.5	3.8	4.8	V
All battery SMPS-related input balls _FDBK	VCOREmin	1.1	VOUTmax	V
Backup battery supply voltage VBACKUP	1.9	3.2	4.8	V
I/O digital supply voltage VIO	VIOmin	VIO	VIOmax	V
Battery charger supply voltage VBUS	0	5.0	6.7	V
Battery charger supply voltage VAC	0	5.0	10.0	V
Battery charger CHRG_PMID	0	5.0	6.0	V
Battery charger CHRG_SW, CHRG_BOOT	0	5.0	6.0	V
Battery charger CHRG_VREF	0	5.0	6.5	V
Battery charger CHRG_DET_N	0	VUSB	VUSBmax	V
All other charger analog-related input balls, such as CHRG_AUXPWR, CHRG_CSIN, CHRG_CSOUT, CHRG_LED_IN	0	3.8	4.8	V
Voltage on the USB OTG ID ball	0	VUSB	VUSBmax	V
Voltage on the VRTC GPADC balls GPADC_IN0, GPADC_IN1, and GPADC_IN4	0	VRTC	VRTCmax	V
Voltage on the VANA GPADC balls GPADC_IN2, GPADC_IN3, GPADC_IN5, and GPADC_IN6	0	VANA	VANAmax	V
Voltage on the VDD_B3 GPADC balls	0	3.8	4.8	V
Voltage on the crystal oscillator OSC32KIN ball	0	VRTC	VRTCmax	V
Voltage on all other analog input balls such as GGAUGE_RESN, GGAUGE_RESP	0	VANA	VANAmax	V
EPROM supply voltage VPROG	0	8.0	10.0	V
Voltage on VRTC digital input balls	0	VRTC	VRTCmax	V
Voltage on VIO digital input balls	0	VIO	VIOmax	V
Voltage on VBAT digital input balls	0	3.8	4.8	V
External buck boost supply voltage	MAXLDO (TDCOVmax + DV)	3.8	4.8	V
Ambient temperature range	–40	27	85	°C
Junction temperature (Tj)	–40	27	125	°C
Storage temperature range	–65	27	150	°C
Lead temperature (soldering, 10 seconds)		260		°C

ESD SPECIFICATIONS

ESD METHOD	STANDARD	LEVEL
Human body model (HBM)	EIA/JESD22-A114D	2 kV
Charge device model (CDM)	EIA/JESD22-C101C	500 V

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SAMSUNG EX. 1034 - 13/101

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switched-mode regulators						
C_I	Input capacitor		0.6	4.7	6.5	µF
C_O	Output filter capacitor		4	10	15	µF
	Filter capacitor ESR	f = [1–10] MHz	1	10	20	mΩ
L_O	Filter inductor	V1V29, V2V1, VCORE1, VCORE2, VCORE3, V1V8, VMEM	0.68	1	1.30	µH
		At inductor saturation, IDC=I_{sat}	0.30			
DCR_L	Filter inductor DC resistance		1	50	100	mΩ
	Filter inductor Q factor	>6 MHz	20			
	PMOS current limit (high side)	**V1V29, V2V1, VCORE2, VCORE3, VMEM**				mA
		ILIMIT[1:0] = 00 (no current limitation)	–	–	–	
		ILIMIT[1:0] = 01 (800 mA I_{OUTmax} mode)	1300	1620	2000	
		ILIMIT[1:0] = 1X (1000 mA I_{OUTmax} mode)	1640	2050	2520	
	PMOS current limit (high side)	**V1V8, VCORE1**				mA
		ILIMIT[1:0] = 00 (no current limitation)	–	–	–	
		ILIMIT[1:0] = 01 (1.2 A I_{OUTmax} mode)	1640	2050	2460	
		ILIMIT[1:0] = 10 (1.5 A I_{OUTmax} mode)	1920	2400	2800	
		ILIMIT[1:0] = 11 (1.6 A I_{OUTmax} mode)	2540	3100	3600	
	Input current limit under short-circuit conditions	V1V29_FDBK, V2V1_FDBK, VCORE1_FDBK, VCORE2_FDBK, VCORE3_FDBK, V1V8_FDBK, VMEM_FDBK = 0 V	10	20	30	mA
V_{INF}	Input voltage (functional)		max(V_{out}+ 0.4, 2.5)		5.5	V
V_{INP}	Input voltage (performances) V1V29, V2V1, VCORE2, VCORE3, VMEM		max(V_{out}+ MinDOV, 2.5)	3.8	4.8	V
MinDOV	Dropout voltage for performances (DOV = Vin–Vout)	**V1V29, V2V1, VCORE2, VCORE3, VMEM**				V
		I_{OUT} = 800 mA	0.65			
		I_{OUT} = 1000 mA	0.90			
		VCORE1, V1V8				
		I_{OUT} = 1200 mA	0.70			
		I_{OUT} = 1500 mA	0.90			
		I_{OUT} = 2000 mA	1.10			
I_{OUT}	Rated output current	PWM mode: V1V29, V2V1, VCORE2, VCORE3, VMEM (limitation on maximum temperature)(1)	0		800	mA
		PWM mode: VCORE1, V1V8 (limitation on maximum temperature)(2)	0		1500	
		Pulse-frequency modulation (PFM) mode: All		200		

(1) V1V29, V2V1, VCORE2, VCORE3, VMEM at I_{OUT} = 800 mA. Maximum junction temperature for VOUT ≤ 1.4 V: 125°C. Maximum junction temperature for VOUT > 1.4 V : 115°C.
(2) VCORE1, V1V8 at I_{OUT} = 1500 mA. Maximum junction temperature for VOUT ≤ 1.4 V: 125°C. Maximum junction temperature for VOUT > 1.4 V: 115°C.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OUT\ EXT}$	Extended output current	PWM mode: V1V29, V2V1, VCORE2, VCORE3, VMEM (limitation on maximum temperature) (3)(4)	0		1000	mA
		PWM mode: VCORE1, V1V8 (limitation on maximum temperature) (5)(6)	0		1600	
T_{DCOV}	Total DC output voltage accuracy	Includes voltage references, DC load/line regulations in PFM and PWM modes, process, and temperature (–1.2%/+2.4%)				
		0.6 V	0.601	0.608	0.623	V
		1.1 V	1.101	1.114	1.141	
		1.225 V	1.226	1.241	1.271	
		1.3 V	1.301	1.317	1.349	
		1.35 V	1.352	1.368	1.401	
		1.8 V	1.801	1.823	1.867	
		1.9 V	1.902	1.925	1.971	
		2.1 V	2.101	2.127	2.178	
V_{OUT}	Output voltage, programmable	Low range (EPROM dependent)	0.6		1.3	V
		High range (EPROM dependent)	0.7		1.4	
		Step size		12.5		mV
		Other selectable voltages		1.35 1.5 1.8 1.9 2.1		V
		Extended voltage range, multiplier for nominal levels (enabled by EPROM)		3.0476		
R_V	Ripple voltage	PWM mode, I_{OUT} = 0 to I_{OUTmax}		5	10	mVpp
		PFM mode, I_{OUT} = 1 mA, ΔV_{OUT} / V_{OUT}		1	2	%
DC_{LDR}	DC load regulation	PWM mode, I_{OUT} = 0 to I_{OUTmax}, ΔV_{OUT} / V_{OUT}		0.25	0.5	%
DC_{LNR}	DC line regulation	PWM mode, I_{OUT} = 0 to I_{OUTmax}, V_{IN} = V_{INPmin} to V_{INPmax} , ΔV_{OUT} / V_{OUT}		0.8	1.6	%

(3) V1V29, V2V1, VCORE2, VCORE3, VMEM at IOUT = 1000 mA. Maximum junction temperature for VOUT ≤ 1.4 V: 115°C. Maximum junction temperature for VOUT > 1.4 V: 105°C.
(4) Able to withstand this maximum current during cumulative stress time of 1900 hours.
(5) VCORE1, V1V8 at I_{OUT} = 2000 mA. Maximum junction temperature for VOUT ≤ 1.4 V: 115°C. Maximum junction temperature for VOUT > 1.4 V: 100°C.
(6) Able to withstand this maximum current during cumulative stress time of 1900 hours.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{LDR}	Transient load regulation, ΔV_{OUT} / V_{OUT}	**V1V29, V2V1, VCORE2, VCORE3, VMEM at Vout < 0.75 V**				%
		I_{OUT} = 0–150 mA, Tr/Tf = 100 ns		2	3	
		I_{OUT} = 50–250 mA, Tr/Tf = 100 ns				
		I_{OUT} = 150–400 mA, Tr/Tf = 100 ns				
		V1V29, V2V1, VCORE2, VCORE3, VMEM at Vout ≥ 0.75 V				
		I_{OUT} = 0–150 mA, Tr/Tf = 100 ns		1	1.5	
		I_{OUT} = 50–250 mA, Tr/Tf = 100 ns				
		I_{OUT} = 150–400 mA, Tr/Tf = 100 ns				
		VCORE1, V1V8 at Vout < 0.75 V				
		I_{OUT} = 0–150 mA, Tr/Tf = 100 ns		3.3	4.2	
		I_{OUT} = 50–250 mA, Tr/Tf = 100 ns				
		I_{OUT} = 350–800 mA, Tr/Tf = 100 ns				
		VCORE1, V1V8 at Vout >= 0.75 V				
		I_{OUT} = 0–150 mA, Tr/Tf = 100 ns		2.8	3.6	
		I_{OUT} = 50–250 mA, Tr/Tf = 100 ns				
		I_{OUT} = 350–800 mA, Tr/Tf = 100 ns				
T_{LNR}	Transient line regulation, ΔV_{OUT} / V_{OUT}	VIN step = ±0.6 V; Tr/Tf = 10 us; I_{OUT}=I_{OUTmax}				%
		Vout < 0.75 V		0.7	1.4	
		Vout ≥ 0.75 V		0.5	1.0	
T_{ON}	Off to on	I_{OUT} = 200 mA, V_{OUT} within accuracy limits, SMPS not frequency locked		350	500	µs
		I_{OUT} = 200 mA, V_{OUT} within accuracy limits, SMPS frequency locked		2	3	ms
T_{OFF}	On to off	I_{OUT} = 0 @ V_{OUT} down to 10% x V_{OUT}		250	500	µs
	Pulldown resistor	Off mode	3	7.5	15	Ω
	Output voltage settling time (normal mode) VCORE1, VCORE2, VCORE3	From V_{OUTMIN} = 0.6 V to V_{OUTMAX} = 1.3 V ±5%, ILOAD = $I_{LOADmax}$	50	57	65	µs
	Slew rate	From V_{OUTMIN} = 0.6 V to V_{OUTMAX} = 1.3 V ±5%, I_{LOAD} = $I_{LOADmax}$	11	12.7	14	mV/µs
	Overshoot			3	10	%
	Switching frequency		5.1	6	6.9	MHz
I_{QOFF}	Off ground current	Off mode @ 25°C		0.1	0.25	µA
		Off mode		0.2	1	
I_Q	On ground current	PFM mode, no switching		35	50	µA
		V1V29,V2V1,VCORE2,VCORE3,VMEM in PWM Mode, I_{OUT} = 0 mA, VIN = 3.8 V		8000		
		VCORE1,V1V8 in PWM mode, I_{OUT} = 0 mA, VIN = 3.8 V		12000		

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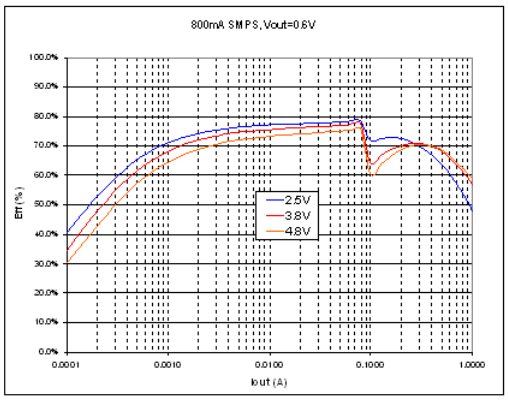

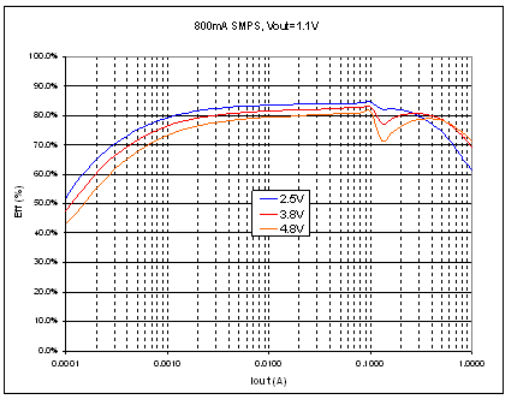

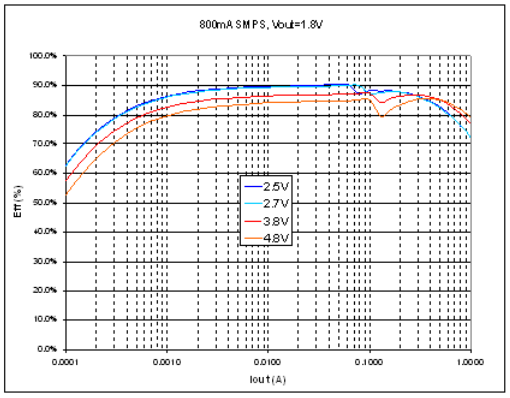

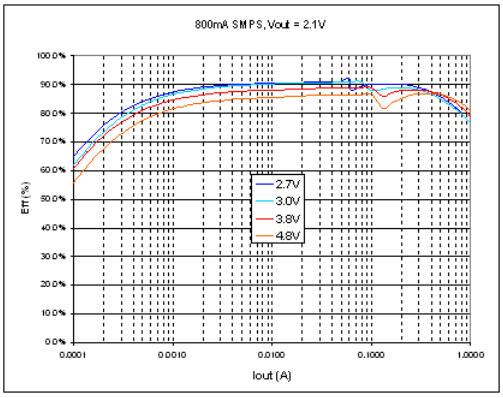

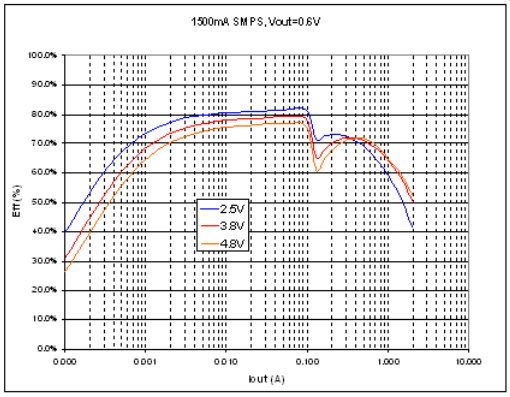

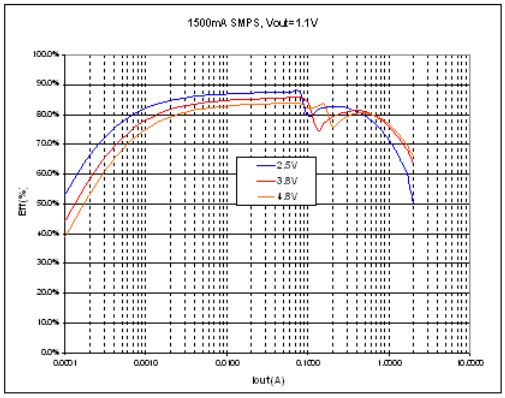

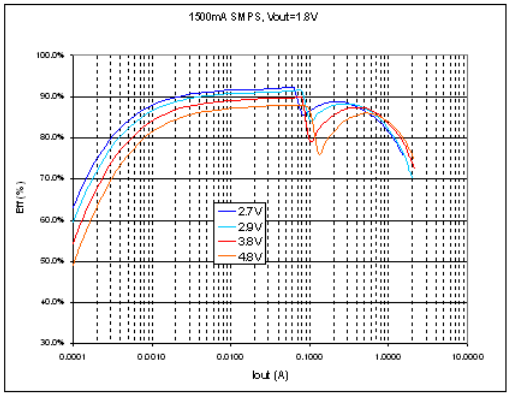

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Figure 3. 0.8 A and 1.5 A SMPS Regulator Efficiencies(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO REGULATORS						
C_{IN}	Input filtering capacitor	Connected from _IN to GND. Shared input tank capacitance (depending on platform requirements and power tree)	0.3	10		µF
		For VUSB - Connected from CHRG_PMID to GND	0.9	4.7	6.5	
C_{OUT}	Output filtering capacitor	Connected from LDO output to GND	0.6	2.2	2.7	µF
	Filtering DC capacitor ESR	< 100 kHz	20	100	600	mΩ
	Filtering AC capacitor ESR	[1–10] MHz	1	10	20	mΩ
V_{INF}	Input voltage (functional)	VRTC: VBAT during on mode	$VBAT_{min}$	3.8	5.5	V
		VRTC: VBAT during backup mode	1.9	2.1	3.1	
		VRTC: Vbackup during backup mode	1.9	3.8	5.5	
		VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VMMC, VPP, VUSIM (for V_{OUT} > 1.5 V)	$T_{DCOV} + D_V - 0.2$	$T_{DCOV} + D_V - 0.1$	5.5	
		VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VMMC, VPP, VUSIM (for V_{OUT} ≤ 1.5 V)	1.8	3.8	5.5	
		VANA	2.3	3.8	5.5	
		VUSB from VBAT	3.5	3.8	5.5	
		VUSB from CHRG_PMID	3.5	6.0	6.8	
V_{INP}	Input voltage (performance)	VRTC	$VBAT_{min}$	3.8	5.5	V
		VANA: VBAT input source supply only supported	2.3	3.8	4.8	
		VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VMMC, VPP, VUSIM (for V_{OUT} > 1.5 V)	$T_{DCOVmax} + D_V$	3.8	4.8	
		VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VMMC, VPP, VUSIM (for V_{OUT} ≤ 1.5 V)	1.8	3.8	4.8	
		VUSB: from VBAT	3.6	3.8	4.8	
		VUSB: from CHRG_PMID	4.3	5.0	5.5	

(7) Coils used:
(a) For VCORE1: MURATA LQM32PN1R0MG0 3.2x2.5x1
(b) For VCORE2: MURATA LQM2MPN1R0NG0 2x1.6x1

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{DCOV}	Total DC output voltage accuracy. Includes voltage references, DC load/line regulations, process and temperature (except VRTC)	1.0 V	–1.7%	1.018	+1.2%	V
		1.2 V		1.222		
		1.3 V		1.323		
		1.4 V		1.425		
		1.5 V		1.527		
		1.6 V		1.628		
		1.7 V		1.730		
		1.8 V		1.832		
		1.9 V		1.934		
		2.0 V		2.036		
		2.1 V		2.138		
		2.2 V		2.240		
		2.3 V		2.341		
		2.4 V		2.443		
		2.5 V		2.545		
		2.75 V		2.800		
		2.8 V		2.850		
		2.9 V		2.952		
		3.0 V		3.054		
		3.3 V		3.359		
	VRTC	1.8V	1.801	1.823	1.890	V
T_{OVA}	Total output voltage accuracy. Includes voltage references, DC load/line regulations, transient load/line regulation, process and temperature	1.0 V	–3.6%	1.018	+3.1%	V
		1.2 V		1.222		
		1.3 V		1.323		
		1.4 V		1.425		
		1.5 V		1.527		
		1.6 V		1.628		
		1.7 V		1.730		
		1.8 V		1.832		
		1.9 V		1.934		
		2.0 V		2.036		
		2.1 V		2.138		
		2.2 V		2.240		
		2.3 V		2.341		
		2.4 V		2.443		
		2.5 V		2.545		
		2.75 V		2.800		
		2.8 V		2.850		
		2.9 V		2.952		
		3.0 V		3.054		
		3.3 V		3.359		
D_V	Dropout voltage @V_{IN_MIN} = 2.3 V	VCXIO, VDAC, $I_{OUT} = I_{OUTmax}$			150	mV
		VANA, $I_{OUT} = I_{OUTmax}$			100	
		VMMC, VUSIM: I_{OUT} = 50 mA			140	
		VUSB, @$I_{OUT}=I_{OUTmax}$			200	
		VAUX1, VAUX2, VAUX3, VMMC, VPP, VRTC, VUSIM: $V_{INPmin} = T_{DCOV} + D_V$, @$I_{OUT}=I_{OUTmax}$			300	
	Dropout voltage @V_{IN_MIN} =1.8 V	VCXIO, VDAC, $I_{OUT} = I_{OUTmax}$			250	
		VAUX1, VAUX2, VAUX3, VMMC, VPP, VUSIM: $V_{INPmin} = T_{DCOV} + D_V$, @$I_{OUT}=I_{OUTmax}$			400	
I_{OUT}	Rated output current	VANA, VRTC			25	mA
		VUSB			35	
		VDAC, VPP			50	
		VAUX1, VAUX2, VAUX3, VCXIO, VMMC, VUSIM			200	
V_{OUT}	Output voltage, programmable (except VRTC and VANA)	Range	1.0		3.3	V
		Step size		100		mV
		Additional selectable voltage level		2.75		V
	Load current limitation	VANA, VDAC, VPP, VRTC, VUSB	100	250	400	mA
		VAUX1, VAUX2, VAUX3, VCXIO, VMMC, VUSIM	400	650	900	

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC_{LDR}	DC load regulation, $\Delta V_{OUT}/V_{OUT}$	I_{OUT} = 0 to I_{OUTmax}		0.25	0.5	%
DC_{LNR}	DC line regulation, $\Delta V_{OUT}/V_{OUT}$	V_{IN} = V_{INPmin} to V_{INPmax} I_{OUT} = I_{OUTmax}		0.1	0.2	%
T_{on}	Turn-on time	I_{OUT} = 0, V_{OUT} = 0.1 V up to V_{OUTmin}		100	500	µs
T_{off}	Turn-off time (except VRTC)	I_{OUT} = 0, V_{OUT} down to 10% x V_{OUT}		250	500	µs
	Pulldown resistor (except VRTC)	Off mode	40	60	80	Ω
PSRR	Power supply ripple rejection	f = 217 Hz, I_{OUT} = I_{OUTmax}	55	90		dB
		f = 50 kHz, I_{OUT} = I_{OUTmax}	35	45		
		f = 1 MHz, I_{OUT} = I_{OUTmax}	30	35		
I_{QOFF}	Off ground current	Off mode @ 25°C	0	0.05	0.15	µA
		Off mode	0	0.2	1	
I_{Q0}	On ground current	I_{OUT} = 0, (except VDAC)	12	18	23	µA
		I_{OUT} = 0, VDAC	75	150	175	
α_Q	On ground current coefficient On mode, $I_{QOUT} = I_{Q0} + \alpha_Q * I_{OUT}$	I_{OUT} < 100 µA		4		%
		100 µA < I_{OUT} < 1 mA		2		
		I_{OUT} > 1 mA		1		
T_{LDR}	Transient load regulation, $\Delta V_{OUT}/V_{OUT}$	On mode, I_{OUT} = 100 µA to $I_{OUTmax}/2$, $T_r = T_f$ = 1 µs		0.75	1.5	%
T_{LNR}	Transient line regulation, $\Delta V_{OUT}/V_{OUT}$	V_{IN} step = 600 mVpp, $T_r = T_f$ = 10 µs		0.25	0.5	%
	Noise (except VDAC)	100 < f < 10 kHz		5000	8000	nV/√Hz
		10 kHz < f < 100 kHz		1250	2500	
		100 kHz < f < 1 MHz		150	300	
		f > 1 MHz		250	500	
	Noise (VDAC)	100 < f < 5 kHz		200	400	nV/√Hz
		5 kHz < f < 400 kHz		62	125	
		400 kHz < f < 10 MHz		25	50	
VAUX3 WHEN USED AS VIBRATOR DRIVER						
C_{OUT}	Output filtering capacitor	Connected from LDO output to GND	0.6	2.2	2.7	µF
	Output regulated output range	Configurable step of 100 mV	1.0		3.3	V
	Vibrator inductive load	Connected from VAUX3 to ground	70	350	700	µH
	Vibrator load resistance		15	40	50	Ω
REFERENCE GENERATOR						
	Filtering capacitor	Connected from VBG to REFGND	30	100	150	nF
	Biasing resistor (±1%) @ 25°C	Connected from IREF to REFGND	0.990	1.000	1.010	MΩ
	Biasing resistor (±1%) temperature coefficient			25	50	ppm/°C
V_{INF}	Input voltage VINF	Functional	1.9	2.2	2.3	V
V_{INP}	Input voltage VINP	Performance	2.3	3.8	5.5	V
	Ground current		15	20	40	µA
	Start-up time			1	3	ms
CRYSTAL CHARACTERISTICS						
	Crystal frequency	@ specified load cap value		32768		Hz
	Crystal tolerance	T = 25°C	–20	0	20	ppm
	Secondary temperature coefficient		–0.04	–0.035	–0.03	$ppm/°C^2$
	Crystal series resistor	@ fundamental frequency			90	kΩ
	Operating drive level		0.1		0.5	µW
	Crystal load capacitor (according to crystal data sheet)			12.5		pF

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Shunt capacitor			1.4	2.6	pF
	Quality factor		8000		80000	
CRYSTAL OSCILLATOR EXTERNAL COMPONENTS						
	VRTC power supply external filtering cap	OSC32KCAP	0.6	1.0	2.7	µF
	Load capacitors on OSC32KIN and OSC32KOUT (parallel mode, including parasitic of PCB for external cap)	Frequency		32.768		kHz
		Duty cycle	40	50	60	%
		Rise and fall time (10–90%)		10	20	ns
		Setup time			1	ms
	Frequency accuracy (considering crystal tolerance and internal load capacitors variation)	@ 25°C, normal and high-performance (HP) modes	–30	0	30	ppm
		@ 25°C, backup mode	–80	0	80	
	Oscillator capacitor ratio: COSC32KIN/COSC32KOUT			1		
	Frequency temperature coefficient	Oscillator contribution in normal and HP modes (not including the crystal variations)		±0.5		ppm/°C
	SSB phase noise at a 1-kHz offset from the carrier	HP mode OSC_HPMODE = 1			–125	dBc/Hz
	SSB phase noise at a 100-Hz offset from the carrier	HP mode OSC_HPMODE = 1			–105	dBc/Hz
	Cycle jitter short term (peak-peak)	Normal mode OSC_HPMODE = 0			25	ns
	Period-to-period jitter, long-term 100k pulses (peak-peak)	Normal mode OSC_HPMODE = 0			120	ns
	Integrated jitter (HP mode)	20 Hz – 20 kHz flat			0.86	ns_{RMS}
		80 Hz – 20 kHz flat			0.43	
	Startup time on power on	Gm boosted during start-up phase Shunt capacitor ≤ 1.4 pF			300	ms
	Sixth harmonic mode rejection RS32/RS200	Oscillator ratio between negative resistance @ 32 kHz and negative resistance @ 200 kHz (sixth harmonic)	10			
	Ground current	Crystal mounted:				µA
		– Backup mode (@ 25°C)			1.5	
		– Normal mode: OSC_HPMODE = 0			3	
		– HP mode: OSC_HPMODE = 1			5	
		– Start-up (boost) phase			20	
		Bypass mode: OSC_BYPASS = 1			3	
	Duty cycle CLK32KAO/CLK32KG	Logic output signal	40	50	60	%
	Rise and fall time (10–20%)	CLK32KAO/CLK32KG	5	20	100	ns
32-kHz RC OSCILLATOR						
	Output frequency			32		kHz
	Output frequency accuracy	After trimming	–15	0	+15	%
	Cycle jitter (RMS)				10	%
	Output duty cycle		40	50	60	%
	Settling time				150	µs
	Active current consumption			4	8	µA
	Power-down current				30	nA
6-MHz RC OSCILLATOR						
	Output frequency			6		MHz
	Output frequency accuracy	After trimming	–10	0	+10	%
	Cycle jitter (RMS)				5	%

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output duty cycle		40	50	60	%
	Settling time				5	µs
	Active current consumption			50	100	µA
	Power-down current				50	nA
CLK32KAUDIO OUTPUT BUFFER						
	Settling time		0	25	50	µs
	Active current consumption		5	7	10	µA
	Power down current				30	nA
	High output level (VHOUT)		1.70	1.80	1.90	V
	Duty cycle degradation contribution		–2	0	2	%
	Integrated jitter contribution	20 Hz–20 kHz flat	0	25	50	ps_{RMS}
		80 Hz–20 kHz flat	0	10	20	
	External output load		5	10	50	pF
	Output delay time	Output load = 10 pF	0	15	30	ns
	Output rise/fall time	Output load = 10 pF	5	7.5	10	ns
	Output drive strength	VOL = 0.2 V	±1%		±2%	mA
		V_{OH} = VHOUT–0.2 V				
BACKUP BATTERY CHARGER						
	VBACKUP to GPADC input attenuation	VBACKUP from 2.4 to 4.5 V		0.2		V/V
	Backup battery charging current	VBACKUP = 0 to 2.6 V BB_CHG_EN = 1	350	650	900	µA
	End backup battery charging voltage: VBBCHGEND	IVBACKUP = –10 µA, BB_SEL = 00 (VBAT > 3.2 V)	2.90	3.00	3.10	V
		IVBACKUP = –10 µA, BB_SEL = 01 (VBAT > 2.7 V)	2.42	2.52	2.60	
		IVBACKUP = –10 µA, BB_SEL = 10 (VBAT > 3.35 V)	3.05	3.15	3.25	
		IVBACKUP = –10 µA, BB_SEL = 11 (VBAT > 2.5 V)	VBAT–0.3	VBAT		
		IVBACKUP = –10 µA, BB_SEL = XX (VBAT < 2.5 V)	VBAT–0.2	VBAT		
	Current consumption	BB_CHG_EN = 1, IVBACKUP = 0 µA			10	µA
	Backup battery series resistance	Capacitance = 5 to 15 mF	10		1500	Ω
		Capacitance = 100 to 2000 mF	5		15	
BATTERY CHARGER						
C_{VBUS}	VBUS capacitor (VBUS – PGND)	0 V < VBUS < 5.25 V	1.2	4.7	6.5	µF
		0 V < VBUS < 6 V	0.9	4.7	6.5	µF
		ESR (1–10 MHz)	1	10	20	mΩ
C_{PMID}	PMID capacitor (PMID – PGND)	0 V < VBUS < 5.25 V	1.2	4.7	6.5	µF
		0 V < VBUS < 6 V	0.9	4.7	6.5	
		ESR (1–10 MHz)	1	10	20	mΩ
	Output capacitor (CSOUT – PGND)	0 V < CSOUT < 4.5 V	3	10	15	µF
		ESR (1–10 MHz)			20	mΩ
	Output capacitor (CSIN – PGND)	0 V < CSIN < 4.5 V	20	100	150	nF
		ESR (100 kHz)			400	mΩ
	Bootstrap capacitor (BOOT – SW)		5	10	20	nF
		ESR (9 MHz)			200	mΩ
	Ref voltage capacitor	0 V < VREF < 6.5 V	0.7	2.2	2.86	µF
	(VREF – PGND)	ESR (1–10 MHz)			20	mΩ

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Coil (option 1), (SW – CSIN)	0 A–1.5 A	0.7	1	1.45	µH
		DCR			130	mΩ
	Coil (option 2), (SW – CSIN)	0 A–2.7 A	0.7	1	1.3	µH
		DCR			60	mΩ
	Rsense resistor (CSIN – CSOUT)		–1%	68	+1%	mΩ
	Output average current	CHRG_SW		1.5	1.545	A
I_{VBUS}	VBUS supply current control	VBUS > VBUSmin, PWM switching		10		mA
		VBUS > VBUSmin, PWM not switching			5	mA
		0°C < TJ < 85°C, HZ_MODE = 1, 32S mode			30	µA
I_{VBUS_LEAK}	Leakage current from battery to VBUS ball	0°C < TJ < 85°C, CHRG_AUXPWR = 4.2 V, high-impedance mode			5	µA
V_{OREG}	Nominal output charge voltage, programmable	20-mV steps	3.50	3.54	4.76	V
	Voltage regulation accuracy	T = 25°C	–0.5		0.5	%
		0°C < T < 125°C	–1.0		1.0	%
$I_{OCHARGE}$	Nominal output charge current, programmable		300		1500	mA
	Charge current accuracy	$I_{OCHARGE}$ < 600 mA	–5		5	%
		$I_{OCHARGE}$ ≥ 600 mA	–3		3	%
I_{TERM}	Termination charge current	I_{TERM} = 50 mA	–33		33	%
	Termination current accuracy	100 mA ≤ I_{TERM} ≤ 250 mA	–25		25	%
		300 mA ≤ I_{TERM} ≤ 400 mA	–5		5	%
	Deglitch time for charge termination	Both rising and falling, 2-mV overdrive, T_R, T_F = 100 ns	30	31	34	ms
	VAC detection	VAC_DET positive threshold	2.90	3.00	3.15	V
		Hysteresis	100	135	170	mV
	VBUS detection	VBUS_DET positive threshold	2.90	3.00	3.15	V
		Hysteresis	100	135	170	mV
	VAC/VBUS detection deglitch time		25	30	36	ms
V_{VBUS_MIN}	VBUS input voltage lower limit	Input power source detection for battery charging	3.6	3.8	4.0	V
	Deglitch time for VBUS rising above VVBUS_MIN	Rising voltage, 2-mV overdrive, T_R = 100 ns	4	5	6	ms
	Hysteresis for VVBUS_MIN	Input voltage rising	100		200	mV
	Collapse threshold	Input current is automatically reduced, programmable, 80-mV steps	4.2		4.76	V
	Analog DPM loop kick-in threshold accuracy		–2		+2	%
	Collapse comparator threshold accuracy	(Digital DPM feature)	–4		4	%
	Analog anticollapse comparator hysteresis			50		mV
	Input source dV/dt	VBUS falling from collapse threshold to V_{INmin}			2000	V/s
	Collapse debounce time	VBUS falling VBUS rising		0.0625 100		ms
	Tint detection interval	Input power source detection	1.7	2	2.6	s

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN_LIMIT}	VBUS input current limiting threshold	I_{IN_LIMIT} = 100 mA, VBAT > VBATMIN_LO	84	91	98	mA
		I_{IN_LIMIT} = 500 mA, VBAT > VBATMIN_LO	425	460	495	
	VREF internal reference voltage	VBUS > VINmin or CHRG_AUXPWR > VBATMIN, IVREF = 1 mA, CVREF = 1 µF	1.65		6.5	V
	Voltage from BOOT pin to SW pin	During charge or boost operation			6.5	V
	Recharge threshold voltage	Below VOREG	70	120	160	mV
		Deglitch time, VCOUT decreasing below threshold, T_F = 100 ns, 10 mV overdrive		130		ms
BATTERY CHARGER, BATTERY DETECTION						
	IDETECT battery detection current before charge done (sink current)	Begins after termination detected, CHRG_AUXPWR ≤ VOREG	-0.6	–0.45	-0.2	mA
	TDETECT battery detection time		215	262	335	ms
BATTERY CHARGER, SLEEP COMPARATOR						
V_{SLP}	SLEEP state entry threshold	VBUS above CHRG_AUXPWR 2.3 V ≤ CHRG_AUXPWR ≤ VOREG, VBUS falling	CHRG_AUXPWR+0.0	CHRG_AUXPWR+0.04	CHRG_AUXPWR+0.1	mV
V_{SLP_EXIT}	SLEEP state exit hysteresis	2.3 V ≤ HRG_AUXPWR ≤ VOREG	140	200	260	mV
	Deglitch time for VBUS rising above VSLP + VSLP_EXIT	Rising voltage, 2-mV overdrive, T_R = 100 ns	31	32	34	ms
BATTERY CHARGER, PWM						
	Internal top reverse blocking MOSFET on-resistance			180	250	mΩ
	Internal top N-channel switching MOSFET on-resistance	Measured from PMID to SW		120	250	mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		150	200	mΩ
f_{OSC}	Oscillator frequency		2.7	3	3.3	MHz
D_{MAX}	Maximum duty cycle			99.5		%
D_{MIN}	Minimum duty cycle		0			%
BATTERY CHARGER, BOOST MODE						
V_{BUS_B}	Boost output voltage (to pin VBUS)	2.5 V < CHRG_AUXPWR < 4.5 V		5.05		V
	Boost output voltage tolerance	Including line, load regulation	–3	0	3	%
I_{BO1}	Maximum output current for boost at USB connector level	V_{BUS_B} = 5.10 V, 2.5 V < CHRG_AUXPWR < 4.5 V	200			mA
I_{BO2}	Maximum output current for boost at PMID connector level	V_{BUS_B} = 5.10 V, 2.5 V < CHRG_AUXPWR < 4.5 V	235			mA
	IBLIMIT cycle-by-cycle current limit for boost	V_{BUS_B} = 5.10 V, 2.5 V < CHRG_AUXPWR < 4.5 V	0.5	1.0	1.5	A
V_{BUSOVP}	Overvoltage protection threshold for boost (VBUS pin)	Threshold over VBUS to turn off converter during boost	5.8	6.0	6.2	V
	Hysteresis	VBUS falling from above V_{BUSOVP}	90	125	160	mV
	Efficiency	CHRG_AUXPWR = 3.6 V, I_{BO} = 200 mA, TA = 25°C, synchronous operation	70	85		%
I_{DDQ}	Quiescent current			2.34	2.7	mA
V_{BATMAX}	Maximum battery voltage for boost (CSOUT pin)	VCSOUT rising edge during boost	4.75	4.9	5.05	V
	Hysteresis	VCSOUT falling from above V_{BATMAX}	149	200	260	mV

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATMIN}	Minimum battery voltage for boost (CHRG_AUXPWR pin)				2.5	V
	Boost output resistance at HP mode (from VBUS to PGND)	HZ_MODE = 1	165			kΩ
BATTERY CHARGER, PROTECTION						
V_{OVP_VBUS}	VBUS OVP threshold voltage	Threshold over VBUS to turn off converter during charge	6.3	6.5	6.7	V
	Hysteresis	VBUS falling from above V_{OVP_VBUS}	120	140	160	mV
V_{OVP_VBAT}	Battery OVP threshold voltage	VCSOUT threshold over VOREG to turn off charger during charge	110	117	121	%
	Hysteresis	Lower limit for VCSOUT falling from above V_{OVP_VBAT}		11		
	ILIMIT cycle-by-cycle current limit for charge(1)	BUCK_HSLIMI = 0: 2.55 A	2.10	2.55	3.30	A
		BUCK_HSLIMI = 1: 1.90 A default	1.50	1.90	2.60	
V_{BAT_SHORT}	Short-circuit voltage threshold	CHRG_AUXPWR rising (default)	2.00	2.10	2.20	V
	Hysteresis	CHRG_AUXPWR falling from above V_{BAT_SHORT}	90	100	110	mV
I_{BAT_SHORT}	Short-circuit detection current	CHRG_AUXPWR ≤ V_{BAT_SHORT}	20	30	40	mA
	VBUS input current	VBUS = 9.7 V, OVP active			4	mA
	Charger thermal shutdown	Temperature threshold, TCHRGSHTDWN		148		°C
		Hysteresis, TCHRGHYS		10		
	Thermal regulation threshold TCF			125		°C
BATTERY TEMPERATURE MEASUREMENT						
R_{BRI}	External pulldown resistor		0		130	kΩ
I_{BRI}	Current source for the detection			7.5		µA
V_{BRIRef}	Detection threshold	Threshold	1.5		1.6	V
	Offset of the comparator		–10		10	mV
	Current consumption of the comparator				10	µA
	Delay of the comparator	With >10-mV overdrive			10	µs
INDICATOR LED DRIVER						
	VBAT				4.8	V
	LED current	CH_LED_CURR[1:0] = 00		0	0	mA
		CH_LED_CURR[1:0] = 01	–15%	1	+15%	
		CH_LED_CURR[1:0] = 10	–15%	2.5	+15%	
		CH_LED_CURR[1:0] = 11	–15%	5	+15%	
	Rise and fall time for the current	Transition on PWM signal, 10–90%			5	µs
	Startup time	CH_LED_CURR[1:0] from 00 → others			20	µs
	Quiescent current	Disabled				µA
		VRTC (backup mode)			0.1	
		VRTC (wait-on/sleep/active modes)		1	2	
		VAC (@ 20 V)			70	
		CHRG_PMID (@ 5.25 V)			20	
		CHRG_PMID (@ 20 V)			70	
		CH_LED_CURR[1:0] = 01 (1 mA)			200	µA
		CH_LED_CURR[1:0] = 10 (2.5 mA)			400	
		CH_LED_CURR[1:0] = 11 (5 mA)			750	

(1) If using a charger with a current charge always lower and equal to 1.25 A, you can use a 1.5-A current rated inductor. If the current charge is higher than 1.25 A, a 2.1-A current rated inductor must be used.

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Pulldown resistance	CH_LED_CURR[1:0] = 00, can be disabled by the DIS_PULLDOWN bit	50	100	200	kΩ
	Voltage at the output for performance				3.2	V
	Voltage at the output for tolerance	CHRG_LED_TEST pin is driven externally			5.5	V
	Dropout voltage Minimum voltage between CHRG_LED_IN and CHRG_LED_TEST	1 mA	0.2			V
		2.5 mA	0.4			
		5 mA	0.6			
	VAC voltage	During operation	4.1			V
	VBUS voltage	During operation	4.0			V
	CHRG_LED_IN voltage		2.3		5.5	V
USB OTG ID EXTERNAL RESISTORS SPECIFICATIONS						
R_{ID_FLOAT}	ID pulldown, when ID pin is floating	Input spec for external ID resistor	220			kΩ
R_{ID_A}	ACA ID pulldown, TWL6030 is A-Device	Input spec for external ID resistor	119		132	kΩ
R_{ID_B}	ACA ID pulldown, TWL6030 is B-Device, but can't connect	Input spec for external ID resistor	65		72	kΩ
R_{ID_C}	ACA ID pulldown, TWL6030 is B-Device, can connect	Input spec for external ID resistor	35		39	kΩ
R_{IDGND}	ID pulldown when ID pin is grounded	Input spec for external ID resistor			1	kΩ
USB OTG PULLUP AND PULLDOWN RESISTORS						
$R_{ID_PU_100K}$	ID 100k pullup to VUSB		70	100	130	kΩ
$R_{ID_PU_220K}$	ID 220k pullup to VUSB		160	220	280	kΩ
$R_{ID_GND_DRV}$	ID 10k pulldown to ground		1	10	20	kΩ
R_{ID_LKG}	ID internal leakage without GPADC (7 V)				350	nA
R_{ID_LKG}	ID internal leakage without GPADC (2 V)				650	nA
	ID external leakage		–1.5	0	1	µA
USB OTG COMPARATORS						
V_{ID_WK}	ID wake-up comparator threshold	No hysteresis	0.300	0.650	1.150	V
$R_{ID_WK_UP}$	ID wake-up equivalent threshold resistance		10	100	220	kΩ
V_{ID_CMP1}	ID comparator 1 threshold	No hysteresis	0.150	0.200	0.250	V
V_{ID_CMP2}	ID comparator 2 threshold	No hysteresis	0.683	0.720	0.757	V
V_{ID_CMP3}	ID comparator 3 threshold	No hysteresis	1.300	1.400	1.500	V
V_{ID_CMP4}	ID comparator 4 threshold	No hysteresis	2.350	2.500	2.650	V
USB OTG CURRENT SOURCES						
$I_{ID_WK_SRC}$	ID wake-up current source	V_{ID} < 2.75 V	3.5	9	25	µA
$I_{ID_SRC_16u}$	ID current source (trimmed)	V_{ID} < 2.75 V	15.5	16	16.5	µA
$I_{ID_SRC_5u}$	ID current source	V_{ID} < 2.75 V	4.5	5	5.5	µA
USB OTG ADP COMPARATORS						
V_{ADP_PRB}	ADP probing voltage threshold	No hysteresis	0.6	0.65	0.7	V
V_{ADP_SNS}	ADP sensing voltage threshold	No hysteresis	0.20	0.40	0.55	V
V_{ADP_DSCHRG}	ADP discharge voltage				0.15	V
USB OTG ADP CURRENT SOURCES/SINKS						
VBUS_IADP_SRC	ADP source current	VBUS < 0.8 V	1.10	1.40	1.65	mA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBUS_IADP_SINK	ADP sink current	0.5 V < VBUS < 0.8 V	1.1	1.5	2	mA
		0.15 V < VBUS < 0.8 V	0.5	1.5	2	
USB OTG ADP TIMINGS						
T_ADP_SINK	ADP sink time		13	14	15	ms
TA_ADP_PRB	ADP probing period, A-device		1.25	1.75	1.85	s
TA_ADP_PRB	ADP probing period, B-device		1.9	2.0	2.6	s
T_ADP_SNS	ADP sensing time-out		3			s
USB OTG COMPARATORS						
VVBUS_WKUP_UP	VBUS wake-up comparator threshold (up)		2.90	3.00	3.15	V
VVBUS_WKUP_DWN	VBUS wake-up comparator threshold (down)		2.80	2.90	3.05	V
VVBUS_WKUP_HYS	VBUS wake-up hysteresis voltage		50	100	175	mV
VA_VBUS_VLD	A-device VBUS valid comparator threshold	No hysteresis	4.4	4.5	4.6	V
VB_SESS_VLD_UP	B-device session valid comparator threshold (up)		2.2	2.4	2.6	V
VB_SESS_VLD_DWN	B-device session valid comparator threshold (down)		2.1	2.3	2.5	V
VB_SESS_VLD_HYS	B-device session valid hysteresis voltage		20	80	140	mV
VA_SESS_VLD_UP	A-device session valid comparator threshold (up)		0.9	1.1	1.3	V
VA_SESS_VLD_DWN	A-device session valid comparator threshold (down)		0.8	1.0	1.2	V
VA_SESS_VLD_HYS	A-device session valid hysteresis voltage		10	40	70	mV
VB_SESS_END_UP	B-device session end comparator threshold (up)		0.3	0.5	0.8	V
VB_SESS_END_DWN	B-device session end comparator threshold (down)		0.2	0.4	0.7	V
VB_SESS_END_HYS	B-device session end hysteresis voltage		10	40	70	mV
VOTG_SESS_VLD_UP	OTG session valid comparator threshold (up)		2.90	3.10	3.40	V
VOTG_SESS_VLD_DWN	OTG session valid comparator threshold (down)		2.80	3.00	3.30	V
VOTG_SESS_VLD_HYS	OTG session valid hysteresis voltage		20	80	140	mV
VOTG_OVV_UP	OTG overvoltage comparator threshold (up)		6.3	6.5	6.8	V
VOTG_OVV_DWN	OTG overvoltage comparator threshold (down)		6.2	6.4	6.7	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOTG_OVV_HYS	OTG overvoltage hysteresis voltage		40	110	180	mV
GAS GAUGE						
	Current measurement range	10-mΩ sense resistor	–6.2	0	6.2	A
	Measurement accuracy after calibration Tolerance of the sense resistor not included	Includes reference, temperature, offset CG_PERIOD[1:0] = 00 CG_PERIOD[1:0] = 01 CG_PERIOD[1:0] = 10 CG_PERIOD[1:0] = 11	–Vmeas*1% –0.11 –0.28 –0.74 –2.15	0 0 0 0	Vmeas*1% +0.11 +0.28 +0.74 +2.15	mV
	Offset before autocalibration	CG_PERIOD[1:0] = 00		200		µV
		CG_PERIOD[1:0] = 01		200		
		CG_PERIOD[1:0] = 10		200		
		CG_PERIOD[1:0] = 11		450		
	Offset after autocalibration	CG_PERIOD[1:0] = 00		10	`	µV
		CG_PERIOD[1:0] = 01		10		
		CG_PERIOD[1:0] = 10		100		
		CG_PERIOD[1:0] = 11		450		
	Usable input voltage range		–62	0	62	mV
	Input clock frequency	32-kHz crystal oscillator		32.768		kHz
	Current consumption	Power on; FG_EN = 1		50	70	µA
		Power off; FG_EN = 0			0.2	
	Integration period (sample counter uses 32-kHz crystal oscillator)	00: 250 ms		250		ms
		01: 62.5 ms		62.5		
		10: 15.625 ms		15.625		
		11: 3.90625 ms		3.90625		
	External sense resistor			10		mΩ
	Integrator data size (two's complement)	CG_PERIOD[1:0] = 00		1 + 13		Bit
		CG_PERIOD[1:0] = 01		1 + 11		
		CG_PERIOD[1:0] = 10		1 + 9		
		CG_PERIOD[1:0] = 11		1 + 7		
INL	Integral nonlinearity	CG_PERIOD[1:0] = 00	-3.5	0	+3.5	LSB
		CG_PERIOD[1:0] = 01	-2.5	0	+2.5	
		CG_PERIOD[1:0] = 10	-2.0	0	+2.0	
		CG_PERIOD[1:0] = 11	-1.5	0	+1.5	
DNL	Differential nonlinearity	CG_PERIOD[1:0] = 00	-4.0	0	+4.0	LSB
		CG_PERIOD[1:0] = 01	-2.5	0	+2.5	
		CG_PERIOD[1:0] = 10	-1.5	0	+1.5	
		CG_PERIOD[1:0] = 11	-1.0	0	+1.0	
	Accumulator data size			1 + 31		Bit
	Offset data size			1 + 9		Bit
	Sample counter data size			24		Bit
GPADC						
	Current consumption	GPADC_EN = 1	750	900	1400	µA
	Off – mode current	GPADC_EN = 0			1	µA
	Running frequency F		0.85	1	1.15	MHz
	Clock period T = 1/F	Duty cycle 50/50		1		µs
	Resolution			10		Bit
	Number of external inputs			7		
	Number of internal inputs			10		

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	N = number of analog inputs to convert in one sequence		0		17	
	Turn on/off time	GPADC_EN 0 to 1 or GPADC_EN 1 to 0	0	50	100	µs
	Gain error (without scalar)		–3.5	0	3.5	%
	Offset (inputs using opamp-based scalar)	Channel 11 (ICHG)	–20	0	20	LSB
	Offset (inputs using resistive scalar)		–9	0	9	LSB
	Offset (other inputs without scalar)		–9	0	9	LSB
	Offset drift (after trimming)	Temperature and supply	–1	0	1	LSB
	Gain error drift (including reference voltage)	Temperature and supply	–0.6	0	0.2	%
	Integral nonlinearity	Best fitting	–2	0	2	LSB
	Differential nonlinearity		–2	0	2	LSB
	GPADC_IN# input impedance		100			MΩ
	Input capacitor C_{bank}			12		pF
	Maximum source input resistance RS (for all internal or external inputs)				100	kΩ
	GPADC voltage reference			1.25		V
	Input range (SAR)		0		1.25	V
	Gain error of the scalar		–1	0	1	%
	GPADC_IN0 current source	±5%		7		µA
	GPADC_IN0 additional current source	±5%		15		µA
THERMAL MONITORING						
I_{QOFF}	Off ground current (two sensors on the die, specification for one sensor)	Off mode			0.1	µA
		@ 25°C off mode			0.5	
I_{QO}	On ground current (two sensors on the die, specification for one sensor)	On mode, standard mode		7	15	µA
		On mode, GPADC measurement		25	40	
	00 (first hot-die threshold)	Rising temperature	104	117	127	°C
		Falling temperature	95	108	119	
	01 (second hot-die threshold)	Rising temperature	109	121	132	°C
		Falling temperature	99	112	123	
	10 (third hot-die threshold)	Rising temperature	113	125	136	°C
		Falling temperature	104	116	128	
	11 (fourth hot-die threshold)	Rising temperature	118	130	141	°C
		Falling temperature	108	120	132	
	Thermal shutdown	Rising temperature	136	148	160	°C
		Falling temperature	126	138	150	
SYSTEM CONTROL THRESHOLDS						
	POR rising-edge threshold		2.00	2.15	2.50	V
	POR falling-edge threshold		1.90	2.00	2.10	V
	POR hysteresis	Rising edge – falling edge	40	150	350	mV
VBATMIN_LO	Threshold of switch-off (configurable by 50-mV steps)		2.0		3.1	V
VBATMIN_HI	Threshold of switch-on (configurable by 50-mV steps)		2.5		3.55	V
CURRENT CONSUMPTION, BACKUP MODE						
	VBACKUP, supplied on VBACKUP	VBAT = 0 V VBACKUP = 3.2 V		5	8	µA
	VBAT, supplied on VBAT	VBACKUP = 0 V VBAT = 2.7 V		11	16	µA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION, WAIT-ON STATE						
		VBAT = 3.8 V		20	30	µA
CURRENT CONSUMPTION, SLEEP STATE						
	V1V8 and VMEM enabled, no load	VBACKUP = 0 V, VBAT = 3.8V VANA = 0 V, VAUX1 = 0 V, VAUX2 = 0 V, VAUX3 = 0 V, VCXIO = 0 V, VDAC = 0 V VMMC = 0 V, VPP = 0 V, VBRTC = 1.8 V, VRTC = 0V, VUSB = 0 V, VUSIM = 0 V, V1V29 = 0 V, V1V8 = 1.8 V, V2V1 = 0 V, VCORE1 = 0 V, VCORE2 = 0 V, VCORE3 = 0 V, VMEM = 0 V RC6MHZ = OFF, CLK32KG = OFF, CLK32KAUDIO = OFF VBG = ON, VBATMIN_HI = OFF, TMP = OFF, FG = OFF EPROM Features: BSI_ISOURCE = OFF, BAT_DET_EN = OFF, VMEM = 1.35 V		110		µA

The following table describes the digital input signal electrical parameters.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWRON, RPWRON						
	Low-level input voltage V_{IL}-related to VBAT/VDD		–0.3	0	0.35 × VBAT	V
	High-level input voltage V_{IH}-related to VBAT/VDD		0.65 × VBAT	VBAT	VBAT + 0.3 ≤ 5.5	V
BOOT0, BOOT1, BOOT2, BOOT3, CHRG_EXTCHRG_STATZ, GPADC_START, MMC, MSECURE, NRESWARM, OSC32KIN, PREQ1, PREQ2A, PREQ2B, PREQ2C, PREQ3, SIM, TESTEN						
	Low-level input voltage V_{IL}-related to VIO or VRTC		–0.3	0	0.35 × VR	V
	High-level input voltage V_{IH}-related to VIO or VRTC		0.65 × VR	VR	VR + 0.3	V
CTLI2C_SCL, CTLI2C_SDA, SRI2C_SCL, SRI2C_SDA						
	Low-level input voltage V_{IL}-related to VIO		–0.3	0	0.3 × VIO	V
	High-level input voltage V_{IH}-related to VIO		0.7 × VIO	VIO	VIO + 0.3	V
	Hysteresis		0.1 × VIO			V
1.2-V SPECIFIC RELATED I/Os: PREQ3(1)(2)						
	Low-level input voltage V_{IL}-related to VIO		–0.3	0	0.3 × VIO	V
	High-level input voltage V_{IH}-related to VIO		0.7 × VIO	VIO	VIO + 0.3	V

(1) PREQ3 can be programmed for two different input supplies (1.2/1.8 V) and, as such, has a configurable input threshold.
(2) Applying 1.8-V input logic on the PREQ3 ball when the 1.2-V supply mode is selected does not damage the PREQ3 input buffer. Nevertheless, because the threshold is reduced to its 1.2-V configuration, the input buffer is more sensitive to the low 1.8-V logic level.

The following table describes the digital output signal electrical parameters.

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGEN1, REGEN2						
	Low-level output voltage V_{OL}	I_{OL} = 100 µA	0	0.1 × VBAT	0.2 × VBAT	V
	High-level output voltage V_{OH}	I_{OH} = 100 µA	0.8 × VBAT	0.9 × VBAT	VBAT	V
BATREMOVAL, CLK32KAO, CLK32KG, INT, CHRG_EXTCHRG_ENZ, NRESPWRON, PWM1, PWM2, SYSEN						

(1) All output signals are guaranteed low when VRTC is not available, especially REGEN1, REGEN2, and SYSEN, all three of which control some external power resources.

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PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low-level output voltage V_{OL}-related to VIO or VRTC	I_{OL} = 2 mA	0	0.18	0.45	V
	Low-level output voltage V_{OL}-related to VIO or VRTC	I_{OL} = 100 µA	0	0.09	0.2	V
	High-level output voltage V_{OH}-related to VIO or VRTC	I_{OH} = 2 mA	VR – 0.45(2)	VR – 0.18(2)	VR	V
	High-level output voltage V_{OH}-related to VIO or VRTC	I_{OH} = 100 µA	VR – 0.2(2)	VR – 0.09(2)	VR	V
CTLI2C_SDA, SRI2C_SDA						
	Low-level output voltage V_{OL}-related to VIO	3-mA sink current	0	0.1 × VIO	0.2 × VIO	V
	Output current	V_{OL} = 0.4 V	0	1	3	mA

(2) VR replaces either VRTC or VIO.

The following table describes the digital output signal timing characteristics.

BALL NAME/OUTPUT BUFFER	LOAD (pF)	RISE/FALL TIME (ns)		
	MAX	MIN	NOM	MAX
CHRG_EXTCHRG_ENZ	35	5	10	15
INT	35	5	10	15
BATREMOVAL	35	5	10	15
NRESPWRON	35	5	10	15
PWM1	35	5	10	15
PWM2	35	5	10	15
REGEN1	35	5	15	25
REGEN2	35	5	15	25
SYSEN	35	5	10	15
VR supply output buffer	5	1		6
	20	4		11
	35	5		15
	50	8		20
VBAT supply output buffer	5	1		9
	20	3		17
	35	5		25
	50	6		34
CLK32KAO output buffer CLK32KG output buffer	5	5		15
	20	8		30
	35	10		45
	50	15		100

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OPERATION

REAL-TIME CLOCK

The RTC is driven by the 32-kHz oscillator and it provides the alarm and timekeeping functions. The RTC is supplied by the backup battery (when available) if the main battery fails and if no external power is applied.

The main functions of the RTC block are:

- Time information (seconds/minutes/hours) in binary-coded decimal (BCD) code
- Calendar information (day/month/year/day of the week) in BCD code up to year 2099
- Programmable interrupts generation. The RTC can generate two interrupts: a timer interrupts periodically (1s/1m/1h/1d period) and an alarm interrupt at a precise time of the day (alarm function). The timer interrupt can be masked during the SLEEP period to prevent the host processor from waking up.
- Oscillator frequency calibration and time correction
- Other features are:
  - Time mode switching between 12 h or 24 h at any time without disturbing the RTC (Read or write are always performed with the current mode.)
  - Shadow registers that can store time and date content and make it available and stable for reading

For security purpose, the registers related to time and calendar information are protected by restricting their write access to software running in the secure mode of the host (MSECURE). Read access is always allowed even in no secured mode.

NOTE

- IT_ALARM can generate a wake-up of the platform.
- IT_TIMER cannot generate a wake-up of the platform.

Date and Calendar Settings

All the time and calendar information are available in these dedicated registers, called TC registers. The TC registers values are written in BCD code.

1. Year data ranges from 00 to 99:
   - Leap years ≈ Years divisible by 4 (2008, 2012, etc.).
   - Common years = other years.
2. Month data ranges from 01 to 12.
3. Day value ranges from:
   - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
   - 1 to 30 when months are 4, 6, 9, 11
   - 1 to 29 when month is 2 and year is a leap year
   - 1 to 28 when month is 2 and year is a common year
4. Week value ranges from 0 to 6.
5. Hour value ranges from 00 to 23 in 24-hour mode and from 1 to 12 in AM/PM mode.
6. Minutes value ranges from 0 to 59..
7. Seconds value ranges from 0 to 59.

To modify the current time, software writes the new time into TC registers to fix the time/calendar information (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEARS_REG, and WEEKS_REG). The DBB can write into TC registers without stopping the RTC. In addition, software can stop the RTC by clearing the STOP_RTC bit of the RTC_CRTL_REG control register and check the RUN bit of the RTC_STATUS_REG status register to ensure that the RTC is frozen. Then update the TC values, and restart the RTC by setting the STOP_RTC bit.

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NOTE

The 32-kHz second primary counter is not reset when the RTC restarts with the STOP_RTC bit. Therefore, a maximum inaccuracy of 1s is stored in the RTC, depending on the instant the second primary counter is stopped.

Example: Time is 10H54M36S PM (AM/PM mode set), 2008 September 5. Previous registers values are:

Table 3. Real-Time Clock Registers Example

REGISTER	VALUE
SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x10
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x08

Rounding

The user can round to the closest minute, by setting the ROUND_30S bit of the RTC_CTRL_REG register. TC values are set to the closest minute value at the next second. ROUND_30S bit will be automatically cleared when the rounding time is performed (See calendar registers, such as SECONDS_REG, MINUTES_REG, etc., and RTC_CTRL_REG).

Example:

- If the current time is 10H59M45S, rounding changes the time to 11H00M00S.
- If the current time is 10H59M29S, rounding changes the time to 10H59M00S.

Get Time

The GET_TIME feature loads the RTC counter in shadow registers and makes the content of the shadow registers available and stable for reading. Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I^2C addresses as the calendar dynamic registers. The GET_TIME bit is a self-clearing bit. Once the copy to shadow registers is executed, it is reset to 0. If the time is read without GET_TIME, the read value comes directly from the RTC counter and software must manage the counter change during the reading. Time reading remains always at the same address, with or without using the GET_TIME feature.

Compensation Registers

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers must respect the available access period. These registers must be updated before each compensation process. For example, software can load the compensation value into these registers after each hour event, during an available access period.

Figure 4 shows compensation scheduling for the RTC.

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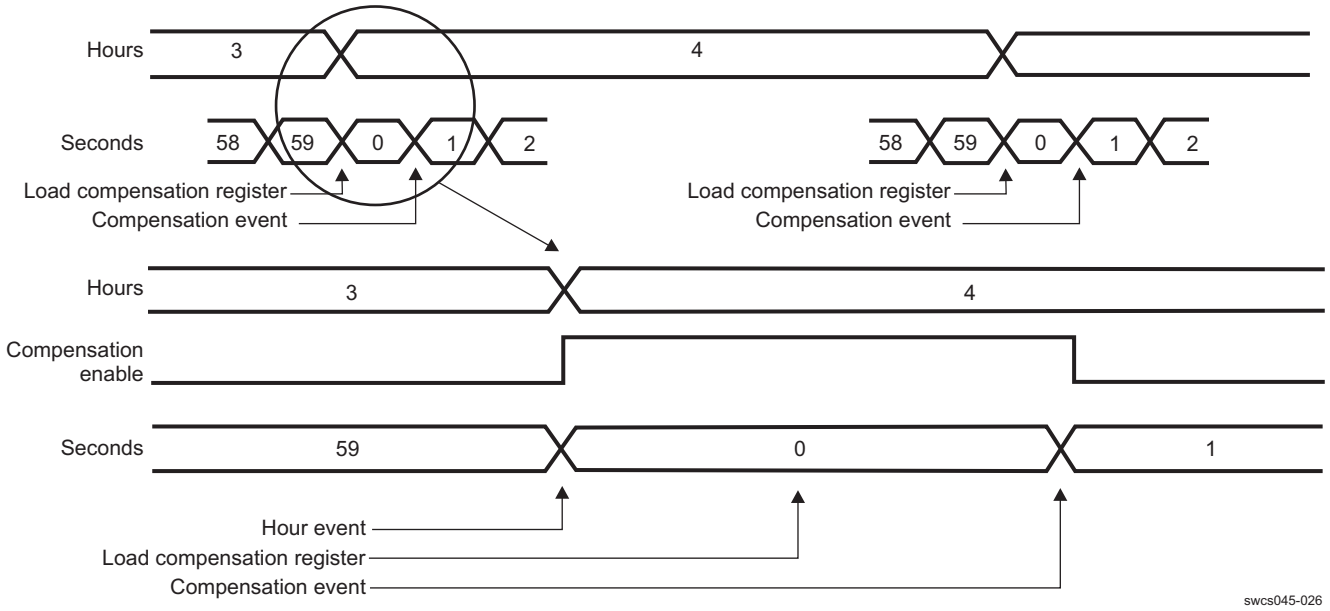

Figure 4. RTC Compensation Scheduling

To compensate for inaccuracy in the 32-kHz oscillator, it is possible to balance this drift. Software must calibrate the oscillator frequency, calculate the drift compensation versus a 1-hour period, and then load the compensation registers with the drift compensation value. If the AUTO_COMP bit in RTC_CTRL_REG is enabled, the RTC_COMP_MSB_REG/RTC_COMP_LSB_REG value (in 2's complement) is added to the RTC 32-kHz counter at each hour and 1 second. When RTC_COMP_MSB_REG/RTC_COMP_LSB_REG is added to the RTC 32-kHz counter, the duration of the current second becomes (32768 – RTC_COMP_M/LSB_REG) / 32768 seconds; therefore, it is possible to compensate the RTC with a 1/32768-s time unit accuracy by hour.

NOTE

The compensation is taken into account once written in the registers. When the TWL6030 device enters backup mode, the host IC must write the previously correct compensation value.

Interrupts

Table 4. RTC Interrupts

INTERRUPT	DESCRIPTION
RTC_ALARM	RTC alarm event: Occurs at programmed date and time.
RTC_PERIOD	RTC periodic event: Occurs at programmed period of time (each second or minute, etc.).

The RTC can generate two types of interrupts:

- Timer interrupt (RTC_PERIOD) can be generated periodically; that is, each second, minute, hour, or day (RTC_INTERRUPTS_REG EVERY[1:0] bits). This interrupt is enabled by the IT_TIMER bit of the RTC_INTERRUPTS_REG interrupts register. It is a negative edge-sensitive interrupt. The RTC_STATUS_REG[5:2] bits (1D_EVENT, 1H_EVENT, 1M_EVENT, 1S_EVENT) are updated only at each new interrupt. They present which type of events occur.
- Alarm interrupt (RTC_ALARM) can be generated when the time set into the TC alarm registers (ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, ALARM_YEARS_REG) is the same as in the TC registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG). This interrupt is then generated if the IT_ALARM bit of the RTC_INTERRUPTS_REG interrupts register is set. This interrupt is

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low-level sensitive; it indicates that an alarm interrupt occurred. This interrupt is disabled by writing 1.

NOTE

- Both alarm (RTC_ALARM) and timer (RTC_PERIOD) interrupts can occur at the same time.
- Both the primary handler and RTC IT_ALARM/IT_TIMER bits must be cleared; otherwise, they hide new interrupt events.
- Only the RTC alarm (RTC_ALARM) can wake up the TWL6030 device (see the STRT_ON_RTC bit in the PHOENIX_START_CONDITION register).

CLOCKS

The TWL6030 device is independent of any high-frequency system clock: It provides only a 32-kHz clock to the platform (see Figure 5). The oscillator can use an external crystal unit to generate the clock or use an external 32-kHz oscillator, in which case the internal oscillator module is bypassed.

To provide a high-performance, 32-kHz clock for the audio device (TWL6040), a dedicated output buffer is implemented on the CLK32KAUDIO ball. This audio buffer uses the VRTC regulator as an input supply source. The CLK32KAUDIO clock might not always be available, and its associated register configuration depends on the platform requirements.

Higher frequencies are required for the different functions of the TWL6030 device and are generated from an internal 6-MHz resistor-capacitor (RC) oscillator.

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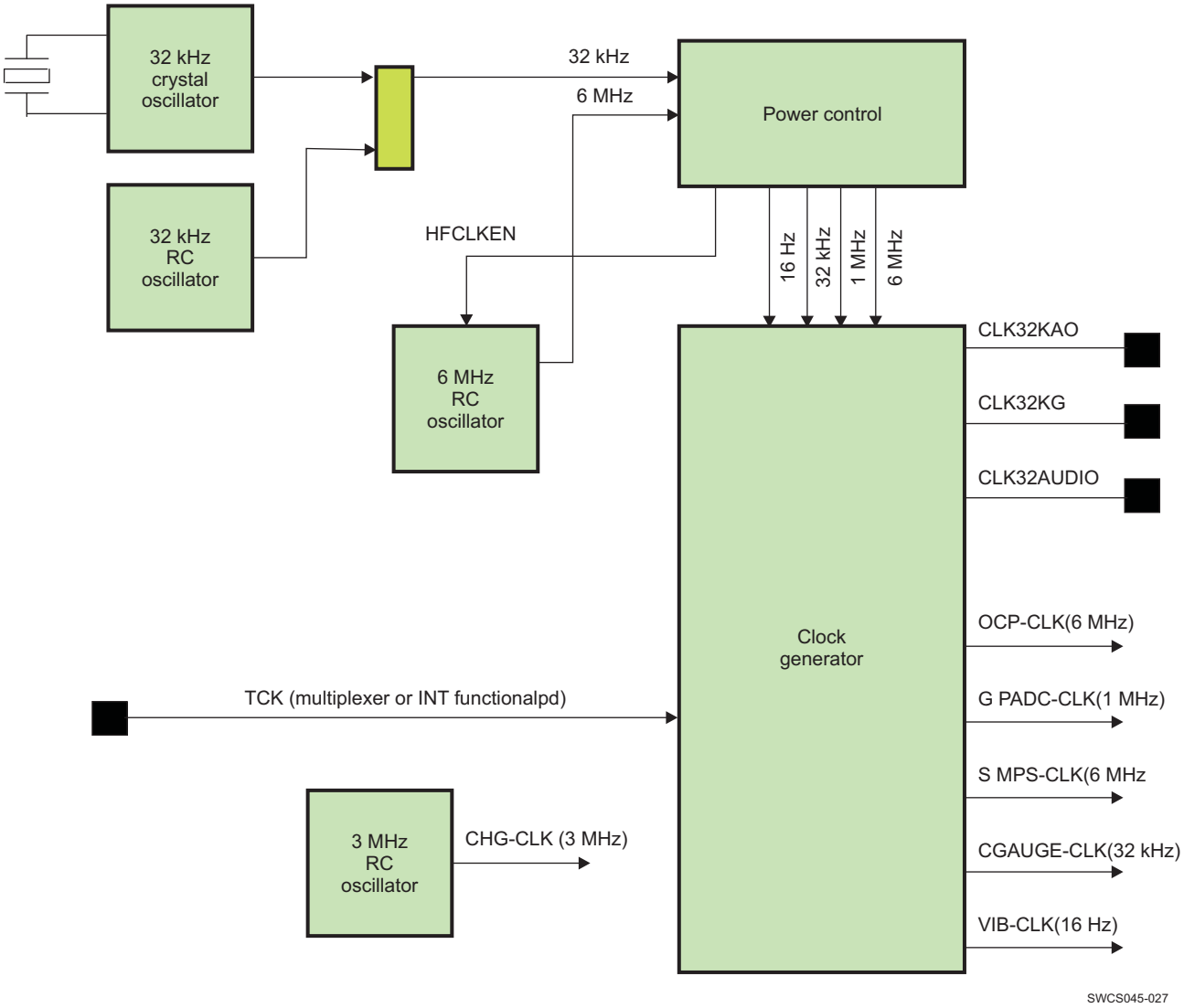

Figure 5. Clock System Functional Description

The RC 32-kHz oscillator provides the clock during the crystal oscillator start-up phase. A 250-ms timer clocked by the 32-kHz crystal clock controls the switching phase from RC to crystal oscillator. The crystal clock starts in 50 ms maximum. The total crystal oscillator start-up sequence is less than 300 ms. The crystal oscillator incorporates an analog detection mechanism of the presence of the crystal. When the crystal is not visible for a nominal period of 500 µs, the crystal oscillator is reset and the multiplexer reselects the RC 32-kHz input. The TWL6030 device is reset with a power-on reset (POR). A crystal start-up sequence phase is reinitialized as soon as the crystal is detected

The RC 6-MHz oscillator is principally required for the SMPS and OCP buses. If all TWL6030 groups are configured in sleep, the TWL6030 device enters the SLEEP state. In the SLEEP state, the RC 6-MHz oscillator is off; otherwise, the RC 6-MHz oscillator remains active. Still, if required, there is some flexibility to maintain the 6-MHz active when the TWL6030 device enters SLEEP state.

The clock generator delivers the following clocks from the RC 6-MHz oscillator:

- 6 MHz for the internal OCP bus
- 6 MHz for the seven SMPSs
- 1 MHz for the GPADC
- 32 kHz for the digital vibrator

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- 16 Hz for the analog vibrator

The clock generator delivers the following clock from the 32-kHz multiplexer output (RC32K or OSC32K): 32 kHz for the gas gauge.

NOTE

The 3-MHz charger clock is directly generated in the charger module and not from the common clock generator.

POWER RESOURCES

The power resources provided by the TWL6030 device include inductor-based SMPSs and linear LDO voltage regulators. These supply resources provide the required power to the external processor cores and external components as well as to the modules embedded in the TWL6030 device.

Short-Circuit Protection

The short-circuit current limits for all LDOs and SMPS regulators embedded in the TWL6030 device are approximately twice their respective maximum load current. For specific LDO use cases, when the output of the module is shorted to ground, the power dissipation can exceed the 1.7-W power dissipation requirement, if there is no continuous preventive action engaged.

The short-circuit protection scheme compares an LDO/SMPS output voltage to a reference voltage and detects a short circuit if the regulator voltage drops slightly below its minimum output voltage (1 V for the LDO and 0.55 V for the SMPS). A short-circuit protection scheme is included in each power resource of the TWL6030 device to ensure that, if the output of an LDO or SMPS is short-circuited, the power dissipation does not increase drastically.

All LDOs/SMPSs include this short-circuit protection that monitors the regulator output voltage and generates an interrupt when a short circuit is detected (see interrupt mapping). The VRTC regulator is the unique power resource that cannot generate an interrupt when shorted. Therefore, this regulator includes a different analog short-circuit mechanism that does not require a switch off of the regulator.

The TWL6030 device waits for the application processor to clear the short-circuit interrupt and turn off the associated power resource within the 10-ms default time. The short-circuit counter is configurable with 6 EPROM bits loaded during the power-up sequence. The possible programming range is 0–640 ms in 10-ms steps. If the interrupt is not cleared before the counter expires, the TWL6030 device switches off automatically. In parallel, the primary watchdog can shut down the device, if the watchdog expires.

In normal use conditions, when the TWL6030 device is turned off, all LDO/SMPS resources (except VRTC/VBRTC) are turned off and their corresponding short-circuit mechanisms are reset. If a short-circuit condition persists in which all power resources should normally be off, the TWL6030 device does not power up again.

SMPS Regulators

The TWL6030 device includes seven SMPSs. Three of these SMPSs have DVS capability and are SmartReflex class 3 compatible. These three SmartReflex SMPSs provide independent core voltage domains to the host processor. The four remaining SMPSs provide supply voltages for the host processor I/Os. Each SMPS is a high-frequency, synchronous, step-down DCDC converter allowing the use of low-cost chip inductors and capacitors.

Each SMPS operates at 6-MHz fixed-switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current. The PFM mode extends the battery life by reducing the quiescent current to 30 µA (typical) during light load and standby operation. For noise-sensitive applications, the required SMPS can be forced into fixed-frequency PWM mode. In shutdown mode, the current consumption is reduced to less than 1 µA.

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Each SMPS is a synchronous step-down converter operating with a 6-MHz, fixed-frequency PWM at moderate-to-heavy load currents. At light load currents, the converter operates in power-save mode with PFM. The converter uses a unique frequency locked-ring oscillating modulator to achieve best-in-class load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up, raising the output voltage until the main comparator trips. The control logic then turns off the switch.

When a SMPS is not used, the SMPS input and ground must still be provided (SMPS_IN at VBAT level). The switching node SMPS_SW can be left unconnected, but SMPS_GND and SMPS_FDBK must be tied to ground.

One key advantage of the nonlinear architecture is the absence of a traditional feedback loop. The loop response to change in VO is essentially instantaneous, which explains its extraordinary transient response. The absence of a traditional, high-gain compensated linear loop means that the regulator is inherently stable over a wide range of L and CO. Each SMPS integrates two current limits, one in the P-channel MOSFET and another in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on for at least 150 ns.

With decreasing load current, the device automatically switches into pulse-skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized, and the device runs with a minimum quiescent current and maintaining high efficiency. The converter will position the DC output voltage approximately 1 percent above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step. When in PFM mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of three pulses and goes into PFM mode when the inductor current return to a zero steady state. Because of the dynamic voltage positioning, in PFM mode the average output voltage is slightly higher than its nominal value in PWM mode. During PFM operation, the converter operates only when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into PFM mode when the output voltage exceeds the nominal output voltage.

For each SMPS, all output voltages can be selected, regardless the external devices connected to them. There is no hardware protection to prevent software from selecting an improper output voltage that would damage the related external equipments. The output voltage codes are described by the following equation.

$$\text{Nominal voltage value} = (0.6077\ \text{V} + \text{SMPS_OFFSET bit} \times 0.1013\text{V}) + (0.01266\ \text{V} \times (\text{binary value} - 00000001)) \times (\text{SMPS_MULT bit} \times 43/21 + 1) \quad (1)$$

An extended output voltage selection mode as well as an offset application can be enabled through EPROM. The extended output voltage codes with and without offset application are presented in Table 7 and in the SMPS_MULT and SMPS_OFFSET registers.

The slew rate of voltage changes is controlled using a step register. For non-SmartReflex supplies, the voltage register is used for voltage selection (for supplies having programmable output voltages). A SmartReflex command does not change the group state.

NOTE

- The OFFSET_RW and SMPS_OFFSET bit are part of the SMPS_OFFSET register.
- The MULT_RW and SMPS_MULT bit are part of the SMPS_MULT register.
- Binary code stands for the SMPS VSEL[5:0] bits.
- This formula applies to all SMPSs, instantiating the same IP, for all codes from 000001 to 111001.
- For the remaining codes, it is specified dedicated discrete output voltages:
  - 000000 sets the output voltage to 0 V.
  - 111010 to 111110 set the output voltages in the range of 1.35 – 2.1 V.
  - 111111 code is reserved and must not be used.

Table 5 lists the SMPS output voltage selection code in standard mode without offset.

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Table 5. SMPS Output Voltage Selection Code (Standard Mode Without Offset)

CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)
000000	0	010000	797.6	100000	1000.2	110000	1202.7
000001	607.7	010001	810.3	100001	1012.8	110001	1215.4
000010	620.4	010010	822.9	100010	1025.5	110010	1228.0
000011	633.0	010011	835.6	100011	1038.1	110011	1240.7
000100	645.7	010100	848.2	100100	1050.8	110100	1253.4
000101	658.3	010101	860.0	100101	1063.5	110101	1266.0
000110	671.0	010110	873.6	100110	1076.1	110110	1278.7
000111	683.7	010111	886.2	100111	1088.8	110111	1291.3
001000	696.3	011000	898.92	101000	1101.4	111000	1304.0
001001	709.0	011001	911.5	101001	1114.1	111001	1316.7
001010	721.6	011010	924.2	101010	1126.8	111010	1367.4
001011	734.3	011011	936.9	101011	1139.4	111011	1519.3
001100	747.0	011100	949.5	101100	1152.1	111100	1823.1
001101	759.6	011101	962.2	101101	1164.7	111101	1924.4
001110	772.3	011110	974.8	101110	1177.4	111110	2127.0
001111	785.0	011111	987.5	101111	1190.1	111111	Reserved

NOTE

- The VOUT values listed in this table represent nominal voltages. The total output accuracy is –4.1% (±3.8%).
- 0.600 – 1.300 V voltage steps are normally used by the SmartReflex SMPS.
- SMPS can be configured to any output selection code, without restriction.

The offset application feature can be unlocked by an EPROM bit and in this case the output voltage values are as described in Table 6:

Table 6. SMPS Output Voltage Selection Code (Standard Mode With Offset)

CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)	CODE	V_{OUT} (mV)
000000	0	010000	898.9	100000	1101.5	110000	1304.0
000001	709.0	010001	911.6	100001	1114.1	110001	1316.7
000010	721.7	010010	924.2	100010	1126.8	110010	1329.3
000011	734.3	010011	936.9	100011	1139.4	110011	1342.0
000100	747.0	010100	949.5	100100	1152.1	110100	1354.7
000101	759.6	010101	962.2	100101	1164.8	110101	1367.3
000110	772.3	010110	974.9	100110	1177.4	110110	1380.0
000111	785.0	010111	987.5	100111	1190.1	110111	1392.6
001000	797.6	011000	1000.2	101000	1202.7	111000	1405.3
001001	810.3	011001	1012.8	101001	1215.4	111001	1418.0
001010	822.9	011010	1025.5	101010	1228.1	111010	1367.4
001011	835.6	011011	1038.2	101011	1240.7	111011	1519.3
001100	848.3	011100	1050.8	101100	1253.4	111100	1823.1
001101	860.9	011101	1063.5	101101	1266.0	111101	1924.4
001110	873.6	011110	1076.1	101110	1278.7	111110	2127.0
001111	886.2	011111	1088.8	101111	1291.4	111111	Reserved

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An EPROM bit unlocks the extended output voltage feature, as listed in Table 7. In this mode, the SMPS voltage level step is 38.1 mV. Some trimming adjustments can shift those levels up or down by one or two settings, meaning ±9.5 mV or 19.05 mV. The resistor divider ratio is 21/64 versus the original configuration set (SMPS_MULT).

Table 7. SMPS Output Voltage Selection Code (Extended Mode Without Offset)

CODE	V_{OUT} (V)	CODE	V_{OUT} (V)	CODE	V_{OUT} (V)	CODE	V_{OUT} (V)
000000	0	010000	2.431	100000	3.048	110000	3.665
000001	1.852	010001	2.469	100001	3.087	110001	3.704
000010	1.891	010010	2.508	100010	3.125	110010	3.743
000011	1.929	010011	2.547	100011	3.164	110011	3.781
000100	1.968	010100	2.585	100100	3.202	110100	3.820
000101	2.006	010101	2.624	100101	3.242	110101	3.858
000110	2.045	010110	2.662	100110	3.280	110110	3.897
000111	2.084	010111	2.701	100111	3.318	110111	3.936
001000	2.122	011000	2.739	101000	3.357	111000	3.974
001001	2.161	011001	2.778	101001	3.395	111001	4.013
001010	2.199	011010	2.817	101010	3.434	111010	2.084
001011	2,238	011011	2.855	101011	3.473	111011	2.315
001100	2.276	011100	2.894	101100	3.511	111100	2.778
001101	2.315	011101	2.932	101101	3.550	111101	2.932
001110	2.354	011110	2.971	101110	3.588	111110	3.241
001111	2.392	011111	3.010	101111	3.627	111111	Reserved

NOTE

The V_{OUT} values listed in Table 8 represent nominal voltages. The total output accuracy is –4.1% (±3.8%).

Table 8. SMPS Output Voltage Selection Code (Extended Mode With Offset)

CODE	V_{OUT} (V)	CODE	V_{OUT} (V)	CODE	V_{OUT} (V)	CODE	V_{OUT} (V)
000000	0	010000	2.739	100000	3.357	110000	3.974
000001	2.161	010001	2.778	100001	3.395	110001	4.013
000010	2.199	010010	2.817	100010	3.434	110010	4.051
000011	2.238	010011	2.855	100011	3.473	110011	4.090
000100	2.277	010100	2.894	100100	3.511	110100	4.128
000101	2.315	010101	2.932	100101	3.550	110101	4.167
000110	2.354	010110	2.971	100110	3.588	110110	4.206
000111	2.392	010111	3.010	100111	3.627	110111	4.244
001000	2.431	011000	3.048	101000	3.665	111000	4.283
001001	2.469	011001	3.087	101001	3.704	111001	4.321
001010	2.508	011010	3.125	101010	3.743	111010	4.167
001011	2.547	011011	3.164	101011	3.781	111011	2.315
001100	2.585	011100	3.202	101100	3.820	111100	2.778
001101	2.624	011101	3.241	101101	3.858	111101	2.932
001110	2.662	011110	3.280	101110	3.897	111110	3.241
001111	2.701	011111	3.318	101111	3.936	111111	Reserved

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Soft Start

Each SMPS has an internal soft-start circuit that limits the inrush current during start up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter. The soft-start system progressively increases the ON-time from a minimum pulse-width of 30 ns as a function of the output voltage. This mode of operation continues for 140 µs after enable. If the output voltage does not reach its targeted value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation. The converter then operates in a current-limit mode, specifically the P-MOS current limit is set to half the nominal limit and the N-channel MOSET remains on until the inductor current is reset. After an additional 100 µs, the device ramps up to full current limit operation, providing the output voltage rises above approximately 0.7 V. Therefore, the start-up time depends primarily on the output capacitor and load current.

Inductor Selection

All step-down converters are designed to operate with an effective inductance value from 0.30 to 1.30 µH and with output capacitors from 4 to 15 µF. The output capacitor maximum value is normally used during the start-up phase, when the capacitor is still unbiased. The internal compensation is optimized to operate with an output filter of L = 1 µH and CO = 10 µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions.

The inductor value affects the following:

- Peak-to-peak ripple current
- PWM-to-PFM transition point
- Output voltage ripple
- Efficiency

The selected inductor must be rated for its DC resistance and saturation current. The ripple current of the inductor decreases with higher inductance and increases with higher VI or VO.

In high-frequency converter applications, the efficiency is mostly affected by the inductor AC resistance (quality factor) and, to a smaller extent, by the inductor DCR value. To achieve high-efficiency operation, special care must be taken to select inductors featuring a quality factor above 20 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades the transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Output Capacitor Selection

SMPS advanced fast-response voltage mode control allows the use of tiny ceramic capacitors. Ceramic capacitors, with low ESR values, provide the lowest output voltage ripple. The output capacitor requires either an X7R or an X5R dielectric.

NOTE

Aside from their wide variation in capacitance overtemperature, Y5V and Z5U dielectric capacitors become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor reactance.

At light loads, the device operates in power-save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds and propagation delays.

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Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor must prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. Although a 2.2-µF capacitor is sufficient for most applications, a 4.7-µF capacitor is recommended to improve input noise filtering.

CAUTION

Exercise caution when using ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and can be mistaken as loop instability or even damage the part. In this circumstance, additional bulk capacitance (electrolytic or tantalum) must be placed between CI and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CI.

VCORE1, VCORE2, VCORE3

The TWL6030 device includes three SMPS converters (VCORE1, VCORE2, and VCORE3) intended to provide three independent core voltage domains to the host processor. All three SMPSs are buck converters with a configurable output voltage. Default output voltage at power up is 0.95 V (EPROM settings). These three converters are SmartReflex class 3 compliant; their output voltages are independently controlled using the SmartReflex I^2C dedicated interface (SR-I2C) or control I^2C (CTL-I2C) thru registers.

VMEM

The TWL6030 device includes an SMPS buck converter VMEM dedicated to memory supply. For example, the output voltage of this SMPS can be 1.8 V, 1.35 V, or 1.2 V.

V2V1

One SMPS V2V1 is dedicated to step the battery voltage down to a preregulated voltage of either 1.8 V or 2.1 V, essentially to supply the TWL6040 (audio) device but also as an input for some LDOs (for example, VCXIO and VDAC) to improve overall platform power efficiency.

V1V29, V1V8

V1V29 operates at a fixed output voltage to supply an external modem or an RF transceiver and/or 1.2-V I/Os. V1V8 SMPS is dedicated to a 1.8-V general-purpose supply (standard I/Os, external peripheral, etc.).

When used as system 1.8-V I/Os, the TWL6030 device I/O supply (VIO ball) must be connected to V1V8.

LDO REGULATORS

All LDOs are integrated so that they can be connected to an internal preregulator, to an external buck boost SMPS, or to another preregulated voltage source.

All LDOs output voltages can be selected, regardless of the LDO input voltage level VIN. There is no hardware protection to prevent software from selecting an improper output voltage if the VIN minimum level is lower than T_{DCOV} (total DC output voltage) + D_V (dropout voltage). In such conditions, the output voltage would be lower and nearly equal to the input supply. For example, in electrical tables, only the possible input supplies, which fulfill the electrical performances in all their ranges, are mentioned at each selected output. Software must not select the 2.5-V output voltage if the VBAT supply is used as the input voltage and VBAT is lower than T_{DCOV} + D_V.

The regulator output voltage cannot be modified on the fly, from the 1.0–2.1 V voltage range to the other 2.2–3.3 V voltage range and vice versa. The regulator must be restarted in these cases.

If an LDO is not needed and not turned-on by software or a switch-on sequence, the external components can be removed. The TWL6030 device is not damaged by this configuration, and the other functions do not depend on the unmounted LDOs and continue to work.

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LDOs are controlled by I^2C access and their output voltage can be selected in a wide range of values. The following equation describes the relationship between the LDO output voltage and the register value.

Absolute voltage value = 1.0 V + 0.1 V × (binary value – 00000001) (2)

NOTE

- This formula applies to all general-purposes LDOs, for all codes from 00000001 to 00011000.
- For the remaining codes, it is specified dedicated output voltages:
  - 00000000 sets the output voltage to 0 V.
  - 00011001 to 00011110 codes are reserved.
  - 00011111 code sets the output voltages at 2.75 V.

Table 9. LDO Output Voltage Selection Code

CODE	V_{OUT}(V)	CODE	V_{OUT}(V)	CODE	V_{OUT}(V)	CODE	V_{OUT}(V)
00000000	0	00001000	1.7	00010000	2.5	00011000	3.3
00000001	1.0	00001001	1.8	00010001	2.6	00011001	Reserved
00000010	1.1	00001010	1.9	00010010	2.7	00011010	Reserved
00000011	1.2	00001011	2.0	00010011	2.8	00011011	Reserved
00000100	1.3	00001100	2.1	00010100	2.9	00011100	Reserved
00000101	1.4	00001101	2.2	00010101	3.0	00011101	Reserved
00000110	1.5	00001110	2.3	00010110	3.1	00011110	Reserved
00000111	1.6	00001111	2.4	00010111	3.2	00011111	2.75

NOTE

- Depending on the output voltage selection code selected, the core section of the LDO is supplied either by the VBAT level (associated VDD_B# ball) or by the LDO_IN input supply
- For all codes in the range of [1.0 - 2.1]V, the VBAT battery level is used to supply the LDO core section
- For all other codes, from 2.2V up to 3.3V, the LDO_IN power source is used to supply the LDO core section
- When Software disables the LDO, the regulator does not present any leakage, even if there is 0V at the LDO_IN input supply ball and the output voltage selected is ≥ 2.2V
- Disabling the LDO does not interact on the core supply switch selection, only linked to the output voltage code
- The output voltage selection, which also affects the core supply switch control, has to be programmed before the regulator turn on event
- The regulator output voltage cannot be modified on the fly, from the [1.0 - 2.1]V voltage range to the other [2.2 - 3.3]V voltage range and vice-versa. The regulator must be restarted
- TWL6030 does not prevent SW for enabling the LDO, even if the LDO_IN input supply is not present

VANA

The VANA voltage regulator is dedicated to supply the analog functions of the TWL6030 device, such as the GPADC, gas gauge, and other analog circuitry.

VANA can be enabled and disabled individually or when associated with a power group. This power resource control optimizes the overall SLEEP state current consumption. This regulator can be used at platform level to supply other applications, provided they do not generate noise to the supply line and the maximum current is less than 15 mA.

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VRTC

The VRTC regulator supplies always-on functions, such as RTC and wake-up functions. This power resource is active as soon as a valid energy source is present.

This resource has two modes:

- Normal mode when supplied from main battery and able to supply all digital part of the TWL6030
- Backup mode when supplied from either a backup battery or a main battery and able to supply only always-on parts

VRTC supplies the digital part of the TWL6030 device. In BACKUP state, the VRTC regulator is in low-power mode (VBRTC) and is supplied from a backup battery or main battery; the digital activity is reduced to the RTC parts only and maintained in retention registers of the backup domain. The rest of the digital is under reset and the clocks are gated.

In WAIT-ON state, the turn-on events and detection mechanism are also added to the previous RTC current load and still supplied on VRTC or VBRTC.

In ACTIVE state, VRTC switches automatically into ACTIVE state (inside analog backup battery IP). The reset is released and the clocks are available.

In SLEEP state, VRTC is kept active. The reset is released and only the 32-kHz clock is available. Still, to reduce power consumption, VBRTC can be used instead of VRTC.

VAUX1, VAUX2, VAUX3, VMMC, VUSIM

The VMMC LDO is a programmable linear voltage converter used to power a multimedia card (MMC) slot. On top of the normal control by the power controller, it can be turned off when card removal is detected (the VMMC_AUTO_OFF bit in the MMCCTRL register). VMMC is based on the same GPLDO architecture as the one used for the VAUX regulators.

Voltage regulator VUSIM is dedicated to supply removable USIM memory. In addition to the normal control by the power controller, it can be turned off when card removal is detected (the VSIM_AUTO_OFF bit in the SIMCTRL register).

The TWL6030 device includes three general-purpose resources (VAUX1, VAUX2, and VAUX3) to supply external peripherals, such as camera sensors, display drivers, memories (embedded multimedia cards [eMMCs]), and others. When not used as a supply, VAUX3 can deliver a PWM supply to drive a vibrator motor.

VCXIO, VDAC, VPP, VUSB

The VCXIO and VDAC regulators supply noise-sensitive functions; for example, the VCXIO supplies the PLLs and MIPI® D-PHY; and VDAC can be used to supply the video DAC. Both LDOs can be preregulated by the V2V1 SMPS.

VUSB supplies the USB PHY from the PMID node of the USB charger or from battery.

VPP supplies the host processor eFuse circuitry. The default value is 1.9 V output supply.

BACKUP BATTERY CHARGER

The TWL6030 device provides a backup mode in which a backup battery is used to power the RTC and other secure registers when no other energy source is available. The backup battery is optional and can be nonrechargeable or rechargeable. The rechargeable battery can be charged from the main battery using the backup battery charger.

The backup battery charger includes two control loops (CC/CV). A current loop limits the charging current when backup battery voltage is low and a voltage loop that gradually reduces the charging current as backup battery voltage approaches its final value. The charge current limit is fixed and the end of charge voltage is programmable.

The backup battery charger is enabled by software and the charging starts if the main battery voltage is 100 mV above backup battery voltage; charging is stopped when backup battery voltage equals either the selected end of the charge voltage level or the main battery voltage, if it is below the end of the charge level programmed. The backup battery charge cannot start if main battery voltage is lower than VBATMIN_LO. The backup battery switch controls when the system enters in backup mode (supplied by the backup battery).

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Figure 6 shows a block diagram of the backup battery charger.

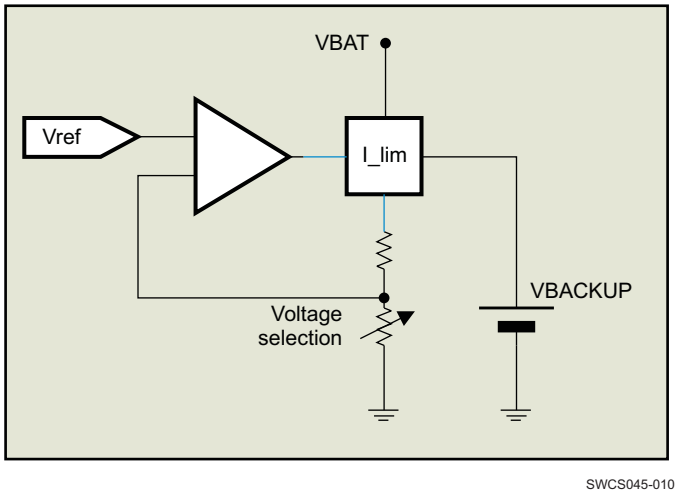

Figure 6. Block Diagram of the Backup Battery Charger

POWER MANAGEMENT

The power-management system can independently drive the power state of three different subsystems or a combination of the three. The power-management state-machine manages the state of the different resources included in the TWL6030 device depending on system activity and energy availability. It ensures the detection of external or internal triggering events that initiate a change of system power state. It controls the transition sequences required to change the system from current power state to a new power state by configuring the resources according to the desired final power state. Configuration registers are accessible through application software by the general-purpose I^2C interface (CTL-I2C). Figure 7 shows a block diagram of the power-management system.

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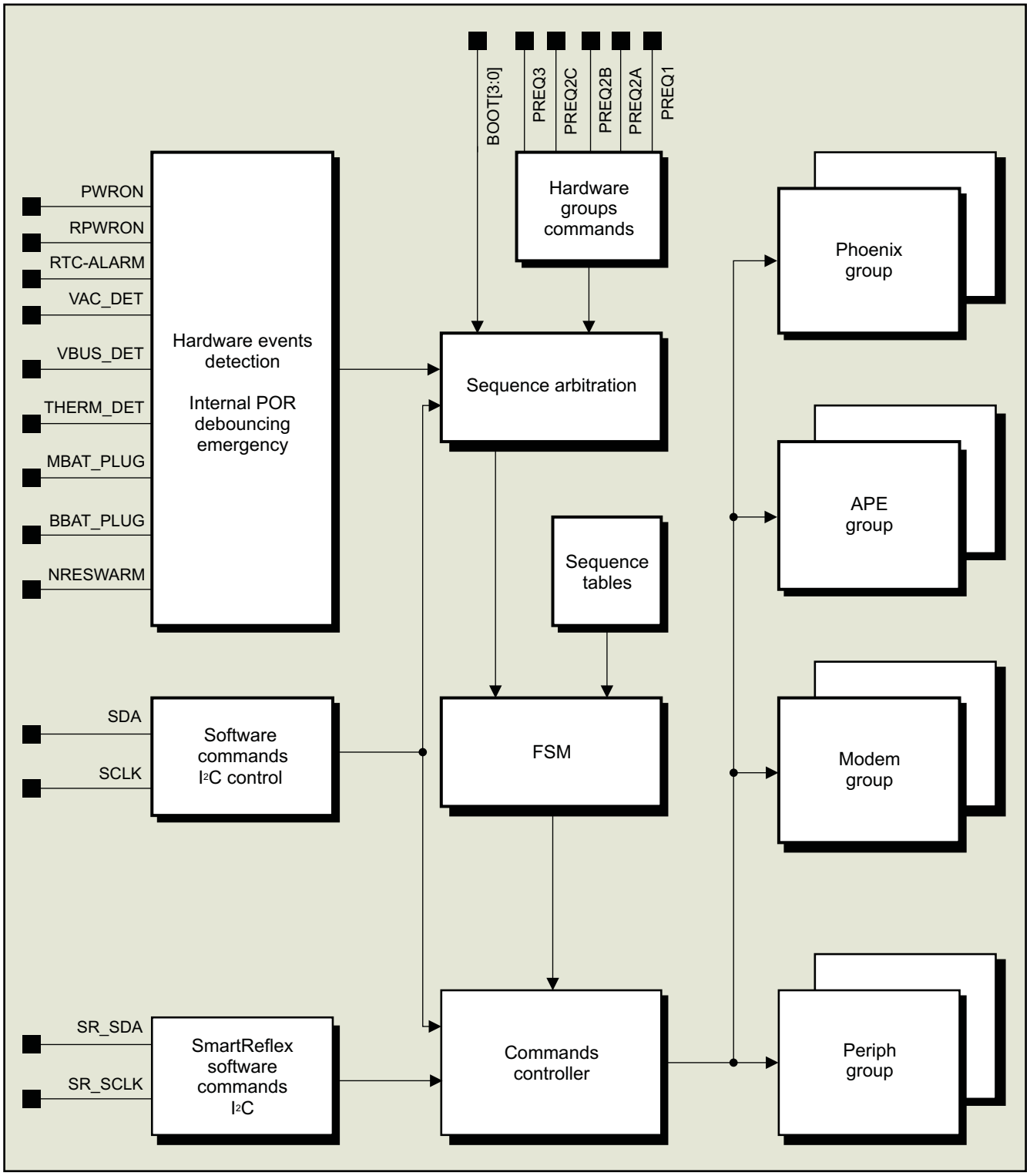

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Figure 7. Power Management Architecture

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Resources

A resource is an element that provides the requirements to a system or subsystem to operate. Typical resources are supplies, clocks, resets, references, and bias. Each resource can be addressed with its unique I^2C address or with the I^2C-shared addresses (broadcast).

Two configurable attributes can be associated to each resource:

- A subsystem group attribute (GRP) specifying to which subsystem group the resource is associated
- A resource category attribute (CAT) specifies the category of the resource among power-providers, power-references or clocks, resets, and comparators. This attribute is hard coded.

Each resource can be associated to one or more subsystems. Resource attributes can be hard coded or configurable. The state of each group to which the resource belongs is stored in the group state register. A state arbitration is made to define the current state of shared resources. The resource state versus group state can be remapped. For example, a resource can be set ON or OFF when the group state is SLEEP.

Table 10 lists the different resource operating modes.

Table 10. Resource Operating Modes

RESOURCE	MODE
Power on	OFF: Disabled
	AUTO: Enabled, adapts to load current
	FORCE: Forced to active mode
REGEN1/REGEN2/SYSEN signals	DISABLE: Logic low
	ENABLE: Logic high
SMPS regulators	OFF: Disabled
	AUTO: Enabled (PFM/PWM operation)
	FORCED PWM: Enabled, forced to operate in PWM mode
Main band gap	OFF: Disabled
	ON ACCURATE: Enabled, high on accuracy
	LOW POWER: Enabled, lower accuracy, low power
	FAST: Enabled, filtering bypassed (used only during BOOT or WAKEUP)
Comparators	OFF: Disabled
	ON: Enabled
Thermal shutdown	ACTIVE: Enabled
	OFF: Disabled
System reset	ACTIVE: NRESPWRON signal active (logic high)
	RELEASED: NRESPWRON signal inactive (logic low)
Clocks and PWM1/PWM2 drivers	DISABLE: Signal delivery is gated.
	ACTIVE: Signal is delivered.

Configuration registers are intended for resource configuration, while state registers are intended to manage the resource state transition; finally, SmartReflex registers are intended to provide dynamic voltage control through the SR-I2C. Configuration and state registers contribute to determine resource behavior. The state register defines to which state the resource must switch and the timing for the transition. The configuration register defines the resource behavior in a defined state. Although both types of registers can be accessed by the FSM and the CTL-I2C, it is preferable to reserve I^2C access to configuration registers and FSM access to state registers. SmartReflex registers are accessed exclusively through the SR-I2C in applications using SmartReflex capability.

These registers can be accessed in different ways: individual access allows the registers to be accessed through their physical address (ID), and broadcast messages are interpreted by individual resources in function of their configuration.

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Groups

Group Definition

The ensemble of resources associated with a subsystem is a group. A subsystem is an engine running a specific application in an independent way. In the TWL6030 device, four groups are defined: one for each subsystem and one for the device itself:

- Group 1: Application processor group (APP)
- Group 2: Peripherals group—connectivity devices (CON)
- Group 3: Cellular modem group (MOD)
- Group 4: Phoenix power device group

The power resources can be allocated to any of the four groups by hardware or software, depending on the resources.

NOTE

- The Phoenix power device group (group 4) includes the resources common to all other groups. Group 4 is not considered a group by itself, as are groups 1, 2, and 3, with all of the associated register bits.
- If a resource is not used, it must be unassigned from its default associated groups.
- A SLEEP-to-ACTIVE transition wakes up all assigned resources of a group.
- Modifying the default value of the CFG_TRANS register allows a specific resource of one group to act differently from the other resources of the same group.

Table 11. Groups and Resources Association

RESOURCE	GROUP1 (APP)	GROUP2 (CON)	GROUP3 (MOD)	GROUP4 (PHOENIX)
SMPS REGULATOR RESOURCES				
V1V29	Yes (software)	Yes (software)	Yes (software)	
V1V8	Yes (software)	Yes (software)	Yes (software)	
V2V1	Yes (software)	Yes (software)	Yes (software)	
VCORE1	Yes (software)	Yes (software)	Yes (software)	
VCORE2	Yes (software)	Yes (software)	Yes (software)	
VCORE3	Yes (software)	Yes (software)	Yes (software)	
VMEM	Yes (software)	Yes (software)	Yes (software)	
LDO REGULATOR RESOURCES				
VANA				Yes (hardware)
VAUX1	Yes (software)	Yes (software)	Yes (software)	
VAUX2	Yes (software)	Yes (software)	Yes (software)	
VAUX3	Yes (software)	Yes (software)	Yes (software)	
VCXIO	Yes (software)	Yes (software)	Yes (software)	
VDAC	Yes (software)	Yes (software)	Yes (software)	
VMMC	Yes (software)	Yes (software)	Yes (software)	
VPP	Yes (software)	Yes (software)	Yes (software)	
VRTC				Yes (hardware)
VUSB	Yes (software)	Yes (software)	Yes (software)	
VUSIM	Yes (software)	Yes (software)	Yes (software)	
CLOCK RESOURCES				
CLK32DAO				Yes (hardware)
CLK32KG	Yes (software)	Yes (software)	Yes (software)	
CLK32KAUDIO	Yes (software)	Yes (software)	Yes (software)	
Clock resources				

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Table 11. Groups and Resources Association (continued)

RESOURCE	GROUP1 (APP)	GROUP2 (CON)	GROUP3 (MOD)	GROUP4 (PHOENIX)
OTHER EXTERNAL CONTROLLED RESOURCES				
REGEN1	Yes (software)	Yes (software)	Yes (software)	
REGEN2	Yes (software)	Yes (software)	Yes (software)	
SYSEN	Yes (software)	Yes (software)	Yes (software)	
INTERNAL RESOURCES				
NRESPWRON				Yes (hardware)
BIAS				Yes (hardware)
RC6MHZ				Yes (hardware)
TMP				Yes (hardware)
VBATMIN_HI	Yes (software)	Yes (software)	Yes (software)	

Power States of Groups and Subsystem Groups

- NO SUPPLY state (Phoenix group only):
  - Description: The system is not powered by any energy source.
  - Condition: VUPR > VPOR
- BACKUP state (Phoenix group only):
  - Description: The system is powered only by a backup battery.
  - Activity: Minimum supply is available to maintain only the keep-alive functions in the Phoenix power device group, such as RTC and other critical data registers and no other activity in the system.
- WAIT-ON/OFF state (Phoenix group and subsystem groups):
  - Description: The system is powered by a valid energy source.
  - Activity: Minimum supply is available to maintain only the keep-alive supply for the RTC and other critical data registers. Power-management controller reset is released and the Phoenix power device group accepts and treats triggering events (WAIT-ON); all other groups are in the OFF state.
- ACTIVE state (all groups):
  - Description: The system is powered by a valid energy source.
  - Activity: The Phoenix group is ACTIVE. The resources required for the group running the application are enabled and the required power supplies are active full current capable (the other groups can remain in SLEEP or OFF state). The system reset is released.
- SLEEP state (all groups):
  - Description: The system is powered by a valid energy source. The Phoenix power device group switches to SLEEP state when all other groups are in SLEEP state.
  - Activity: Resources associated with the group are configured in low-power mode to maintain group context.

NO SUPPLY and BACKUP are global states; that is, they correspond to a unique state of the power resources. ACTIVE, WAIT-ON, and SLEEP are not global states and can be divided in substates; each substate corresponds to a different state configuration of the power resources.

Transitions from the current power state to the next power state are initiated by triggering events. Triggering events can result from user action, system activity, or a change in environmental conditions. Triggering events are enabled or disabled, depending on the triggering conditions.

Subsystem Hardware Commands

Partial-on or partial-off events coming from subsystems (ACTIVE or SLEEP) are transmitted to the TWL6030 device using hardware signals (PREQ1, PREQ2A, PREQ2B, PREQ2C, PREQ3). The FSM conveys this information to the resources of the subsystem group to set each resource in a state based on the subsystem state.

Each subsystem is associated with at least one hardware signal:

- Group 1: Application processor group (APP) → PREQ1

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- Group 2: Peripherals group—connectivity devices (CON) → Logical OR between PREQ2A, PREQ2B, and PREQ2C
- Group 3: Cellular modem group (MOD) → PREQ3

PREQ signals can be masked by register bits PREQ2A, PREQ2B, and PREQ2C sharing the same mask bit. PREQ1, PREQ2A, PREQ2B, PREQ2C, and PREQ3 are supplied on the VIO voltage domain. The default polarity of the signals is active high (group is active) and it can be selected by the register bit.

SmartReflex Software Commands

Only SMPS SmartReflex-compliant resources can be accessed by the SR-I2C. In addition to hardware commands, SmartReflex-compliant power resources receive additional commands with the SR-I2C. These commands affect the voltage setting of the SMPS, depending on the related voltage domain state. The slew rate of voltage changes is controlled with a step register. For non-SmartReflex supplies, the voltage register is used for voltage selection (for supplies having programmable output voltages). A SmartReflex command does not change the state of the group.

Boot Pins

The TWL6030 device has four input balls (Boot[3:0]) to select boot sequence executed at startup. These balls provide an indication on the following parameters to select the correct value for the supply voltages and detection thresholds:

- BOOT0: Battery chemistry (cut-off voltage)
- BOOT1: LPDDR2 (voltage/sequence)
- BOOT2: eMMC (voltage)
- BOOT3: Platform (sequence)

Table 12. BOOT[3:0]

BOOT	STATE	EFFECT
BOOT0	0	High thresholds are selected for VBATMIN_LO and VBATMIN_HI.
	1	Low thresholds are selected for VBATMIN_LO and VBATMIN_HI.
BOOT1	0	OMAP4430 PMIC: S4A LPDDR2 memories are used. VMEM supplies the LPDDR2 core at 1.35 V.
		OMAP4460/4470 PMIC: VMEM is not controlled by startup sequence.
	1	OMAP4430 PMIC: S4B LPDDR2 memories are used. VMEM supplies the LPDDR2 core at 1.2 V.
		OMAP4460/4470 PMIC: VMEM is turned ON by startup sequence. Output voltage is 1.2 V
BOOT2	0	VAUX1 is used to supply eMMC at 2.8 V.
	1	VAUX1 is used to supply eMMC at 1.8 V.
BOOT3	0	VAUX1 is disabled during power-up sequence (pulldown asserted).
	1	VAUX1 is enabled during power-up sequence (BOOT2 configuring the voltage). For example, see the OMAP4 power-up sequence.

NOTE

- OMAP4430 PMIC part numbers are TWL6030B107, TWL6030B1AE, and TWL6030B1A0.
- OMAP4460/4470 PMIC part numbers are TWL6030B1A4, TWL6030B1AF, and TWL6030B1AA.

Battery Comparator Thresholds

Three thresholds of battery voltage condition the system state transitions:

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- POR
  - Released when the energy source can supply the digital resources
  - POR threshold is the minimum voltage below which the TWL6030 device is reset.
- VBATMIN_LO
  - Threshold of hardware switch-off
  - Two values, depending on the battery technology, are stored in EPROM and selected by boot mode.
  - The comparator falling-edge threshold (VBATMIN_LO) is configurable from 2.00 to 3.100 V in 50-mV steps.
  - The equivalent comparator hysteresis range is from 150 to 500 mV.
- VBATMIN_HI
  - Threshold of switch-on
  - Checked as condition to initiate any sequence to ACTIVE state
  - Two values, depending on the battery technology, are stored in EPROM and selected by boot mode.
  - The comparator rising-edge threshold (VBATMIN_HI) is configurable from 2.50 to 3.55 V in 50-mV steps.
  - The equivalent comparator hysteresis range is from 150 to 500 mV.
  - For correct system behavior, the VBATMIN_HI threshold value must not be programmed higher than the default charging voltage. Otherwise, the TWL6030 device does not switch on after a charger plug with empty battery.

Depending on the battery technology used, the Phoenix power device must be configured appropriately with the battery chemistry BOOT pin. The corresponding EPROM bits of the main battery comparators thresholds are loaded during the Phoenix power device start-up sequence:

- The comparator rising edge threshold (VBATMIN_HI) is configurable from 2.50 to 3.550 V in 50-mV steps.
- The comparator falling edge threshold (VBATMIN_LO) is configurable from 2.00 to 3.100 V in 50-mV steps.
- The equivalent comparator hysteresis range is thus from 150 to 500 mV in 50-mV steps.

The EPROM bits stored are:

- Rising edge 16-step code for the current battery generation (6 bits)
- Rising edge 16-step code for the next battery generation (6 bits)
- Falling edge 23-step code for the current battery generation (6 bits)
- Falling edge 23-step code for the next battery generation (6 bits)

Table 13 lists the parameters for the rising edge of the VBATMIN_HI threshold.

Table 13. VBATMIN_HI Threshold

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage threshold	<001010>	2.460	2.500	2.580	V
Voltage threshold	<001011>	2.510	2.550	2.630	V
Voltage threshold	<001100>	2.560	2.600	2.680	V
Voltage threshold	<001101>	2.610	2.650	2.730	V
Voltage threshold	<001110>	2.655	2.700	2.785	V
Voltage threshold	<001111>	2.705	2.750	2.835	V
Voltage threshold	<010000>	2.755	2.800	2.885	V
Voltage threshold	<010001>	2.805	2.850	2.940	V
Voltage threshold	<010010>	2.855	2.900	2.990	V
Voltage threshold	<010011>	2.905	2.950	3.040	V
Voltage threshold	<010100>	2.955	3.000	3.090	V
Voltage threshold	<010101>	3.000	3.050	3.145	V
Voltage threshold	<010110>	3.050	3.100	3.195	V
Voltage threshold	<010111>	3.100	3.150	3.245	V
Voltage threshold	<011000>	3.150	3.200	3.300	V
Voltage threshold	<011001>	3.200	3.250	3.350	V

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Table 13. VBATMIN_HI Threshold (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage threshold	<011010>	3.250	3.300	3.400	V
Voltage threshold	<011011>	3.295	3.445	3.455	V

NOTE

- Minimum values are defined at –[1.50, 1.75]% of the nominal value.
- Maximum values are defined at +[3.00, 3.25]% of the nominal value.
- There is no hysteresis implemented between the rising and falling edges of the battery monitoring comparator.
- The default value is generally 3.200 V nominal (see the VBATMIN_HI_THRESHOLD register).
- For a correct system behavioral, the VBATMIN_HI threshold value must not be programmed above 3.350 V nominal (3.455 V maximum); otherwise the Phoenix power device will not switch on after a charger plug, battery charged up to VOREGmin = 3.465 V (3.50 V – 1%)
- It is possible to configure the VBATMIN_HI threshold with the same values as VBAT_MONITORING, if it fits the system requirements.

Table 14 lists the parameters for the falling edge of the VBATMIN_LO threshold.

Table 14. VBATMIN_LO Threshold

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage threshold	<000000>	2.265	2.300	2.370	V
Voltage threshold	<000001>	2.015	2.050	2.115	V
Voltage threshold	<000010>	2.065	2.100	2.165	V
Voltage threshold	<000011>	2.115	2.150	2.215	V
Voltage threshold	<000100>	2.165	2.200	2.270	V
Voltage threshold	<000101>	2.215	2.250	2.320	V
Voltage threshold	<000110>	2.265	2.300	2.370	V
Voltage threshold	<000111>	2.310	2.350	2.425	V
Voltage threshold	<001000>	2.360	2.400	2.475	V
Voltage threshold	<001001>	2.410	2.450	2.525	V
Voltage threshold	<001010>	2.460	2.500	2.580	V
Voltage threshold	<001011>	2.510	2.550	2.630	V
Voltage threshold	<001100>	2.560	2.600	2.680	V
Voltage threshold	<001101>	2.610	2.650	2.730	V
Voltage threshold	<001110>	2.665	2.700	2.785	V
Voltage threshold	<001111>	2.705	2.750	2.835	V
Voltage threshold	<010000>	2.755	2.800	2.885	V
Voltage threshold	<010001>	2.805	2.850	2.940	V
Voltage threshold	<010010>	2.855	2.900	2.990	V
Voltage threshold	<010011>	2.905	2.950	3.040	V
Voltage threshold	<010100>	2.955	3.000	3.090	V
Voltage threshold	<010101>	3.000	3.050	3.145	V
Voltage threshold	<010110>	3.050	3.100	3.195	V

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NOTE

- Minimum values are defined at –[1.50, 1.75]% of the nominal value.
- Maximum values are defined at +[3.00, 3.25]% of the nominal value.
- An hysteresis is implemented between the rising and falling edges, varying from 100 mV (VBAT = 2.050 V nominal) to 600 mV (VBAT = 3.100 V nominal).
- The analog IP duplicates the VBATMIN_LO default value: <000000> and <000110> selection codes are identical (2.300 V nominal).
- Because VBAT minimum level is defined as 2.3 V through the Phoenix power IC specification, all codes between <000001> and <000101> must not be used for the correct operation of the device.

Reset Signals, Reset Triggers, Reset Domains

This section describes the different reset triggers and the signals related to resets.

- **Power-on reset**: It is triggered when a low battery and a low backup battery condition occurs. This activates a POR that remains active until a valid energy source is detected. The POR release initiates the boot sequence of the TWL6030 device. A delayed version of POR is used in the charger and released during boot sequence when the resources required by the charger are available. During a POR, the TWL6030 device is in a NO SUPPLY state.
- **Warm reset (NRESWARM)**: The TWL6030 device detects a request for a warm reset on the NRESWARM ball. The effect of the warm reset is to restart the system without turning off the supplies. After a warm reset, the system is configured as it is after a first switch-on (default configuration), except that the states of all resources are unchanged and all supply voltage values can be preserved, depending on the warm reset sensitivity bit value (WR_S SMPS_CFG_VOLTAGE/LDO_CFG_VOLTAGE):
  - All resources not included in the switch-on sequence keep the state (ON or OFF) they have just before the warm reset.
  - Depending on the sensitivity bit, those resources either keep the value they had before the warm reset or are set to their default value.
  - All resources included in the start-up sequence are restarted in any case.

  During the power-on sequence, the TWL6030 device ignores the warm reset until the host processor releases it.

  Warmreset affects the POWER and CHARGER registers. Registers for other modules like the USB, FUEL GAUGE, GPADC, and PWM are not affected by warmreset
- **Software reset**: A cold reset can be initiated by software through the I^2C control interface. The effect of this software reset (the SW_RESET bit in the PHOENIX_DEV_ON register) forces the TWL6030 device to perform a switch-off sequence (go to the WAIT-ON/OFF state). This is followed by a switch-on sequence (WAIT-ON to ACTIVE).
- **Long key press**: The long key press on PWRON generates a reset, thus forcing the TWL6030 device to go into WAIT-ON/OFF state. The 10-second length is not configurable.
- **Primary watchdog reset**: The TWL6030 device includes a primary watchdog timer, which generates a reset of the system in case of a software anomaly (no response, infinite loop) (the DEVOFF_WDT bit in the PHOENIX_LAST_TURNOFF_STS register). The primary watchdog PRIMARY_WATCHDOG_CFG is programmable from 1 to 127 seconds with a default value of 32 seconds. In case the primary watchdog expires, it generates a reset forcing the TWL6030 device to go into the WAIT-ON/OFF state. The watchdog is initialized to its default value when the system is in WAIT-ON/OFF state and starts when leaving the WAIT-ON/OFF state to the ACTIVE/SLEEP states. Software cannot disable the primary watchdog, which is possible only through EPROM for testing purposes.
- **Thermal shutdown**: If the die temperature gets too high, the thermal shutdown generates a reset, forcing the TWL6030 device into the WAIT-ON/OFF state (the DEVOFF_TSHUT bit in PHOENIX_LAST_TURNOFF_STS). See also the associated thermal shutdown registers: TMP_CFG_GRP, TMP_CFG_TRANS, TMP_CFG_STATE, and TMP_CFG.
- **NRESPWRON**: The NRESPWRON output signal is the reset signal delivered to the host processor at the end of the power-on sequence. It is released when all TWL6030 supply voltages (core and I/Os) are correctly set up. In addition, the NRESPWRON signal can be gated until the 32-kHz crystal oscillator becomes stable (configured through an EPROM bit). The polarity of the NRESPWRON signal is active low.

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- **PWRON**: The PWRON ball is connected to a push button to control system power on/off. An internal pullup on the battery domain is implemented on this input. Three timers are associated with this input duration:
  - A short timer of 15 ms to confirm the key press detection. This confirmation initiates a power-on sequence or generates an interrupt, depending on the system state.
  - A long timer, programmable from 50 ms to 1.55 seconds, that measures the key press. A register bit is set if the key press duration exceeds the timer duration.
  - A very long timer of 10 seconds that causes a hardware switch-off of the system PWRON detection is performed on falling and rising edges (one interrupt line, 1 interrupt status bit). The polarity of the PWRON signal is active-low (key pressed).
- **RPWRON**: Similar to PWRON, RPWRON controls system power on/off. An internal pullup on the battery domain is implemented on this input. A short timer of 15 ms is implemented to confirm detection. Confirmation initiates either a power-on sequence or a generation of an interrupt, depending on the system state. Detection of RPWRON is performed on falling and rising edges. The polarity of RPWRON is active low (key pressed).
- **REGEN1, REGEN2**: The power-management FSM controls these output signals. These balls are activated during the power-on/off sequences. The timing of activation depends on the power sequence (EPROM). REGEN1 and REGEN2 can be used to control two different external power supplies. The polarity of these signals is active high.
- **SYSEN**: This output signal is controlled by the power-management FSM and is activated during the power-on/off sequences. The timing of activation depends on the power sequence. SYSEN can be used to control an external power supply or a slave PM device. The polarity of SYSEN is active high.

Power State-Machine

The TWL6030 FSM controls boot sequences, Phoenix group state changes, and subsystems group initialization. The power sequencing is made through broadcast commands (several resources accessed simultaneously through broadcast commands or individual access to a resource. The power sequences are stored in a hard-coded table (EPROM). The FSM reacts on events, which initiates power state transitions.

- Hardware events
  - Starting events (going into ACTIVE state)
    - Power on button (PWRON ball)
    - Remote power on (accessories) (RPWRON ball)
    - Battery plug (VBAT ball)
    - VAC detection
    - USB VBUS detection
    - USB ID detection
    - RTC alarm
  - Stopping events (going to OFF state)
    - Short PWRON key press (interrupt to host IC, which initiates switch-off)
    - Long PWRON key press (hardware switch-off)
    - Remote power on (RPWRON) (interrupt to host IC, which initiates switch-off)
    - Primary watchdog (hardware switch-off)
    - Thermal shutdown (hardware switch-off)
  - Backup events (going into NO SUPPLY or BACKUP state)
    - Removal of main and/or backup battery
    - Low main and/or backup battery
- Software events
  - Stopping events (going to OFF state)
    - Group DEVOFF instruction (all groups are OFF)
    - Software reset (SW_RESET) (going to OFF state and then restart to ACTIVE)

Internal hardware monitors the different energy sources (main and backup) and charging sources (VAC or VBUS). A set of comparators is dedicated to energy source selection to generate an uninterrupted power supply (UPR) which exists as soon as a valid energy source is present. The backup battery is considered to be a valid energy source after the first power up of the device. POR is released when UPR rises above to POR threshold

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and the voltage regulator VBRTC provide a supply for the digital control, the 32-kHz oscillators and the low-power band gap. When the main battery voltage rises above the VBATMIN_LO threshold, the digital control enables the checks of the startup events. When a startup event is detected, a final check of the battery voltage is done versus the VBATMIN_HI threshold to pursue the power-up sequence. When the system is active, the comparator is available to perform checks on battery voltage. It then compares battery voltage versus a programmable value and generates interrupts when voltage rises above and drops below the programmed threshold. The comparator can be programmed from 2.3 to 4.6 V level in 50-mV steps. Hysteresis is implemented between the rising and falling edges, varying from 100 mV (VBAT = 2.3 V) to 600 mV (VBAT = 4.6 V).

NOTE

- UPR = VBAT if: (VBAT > VBATMIN_LO) + (VBAT > VBACKUP) . (VCHARGER < VCHARGERmin)
- UPR = VBACKUP if: {[(VBAT < VBATMIN_LO) . (VBAT < VBACKUP - 0.1V)] . (VCHARGER < VCHARGERmin)} . PORZ
- UPR = VCHARGER if: (VBAT < VBATMIN_LO) . (VCHARGER > VCHARGERmin)

Figure 8 shows a block diagram of the analog power control.

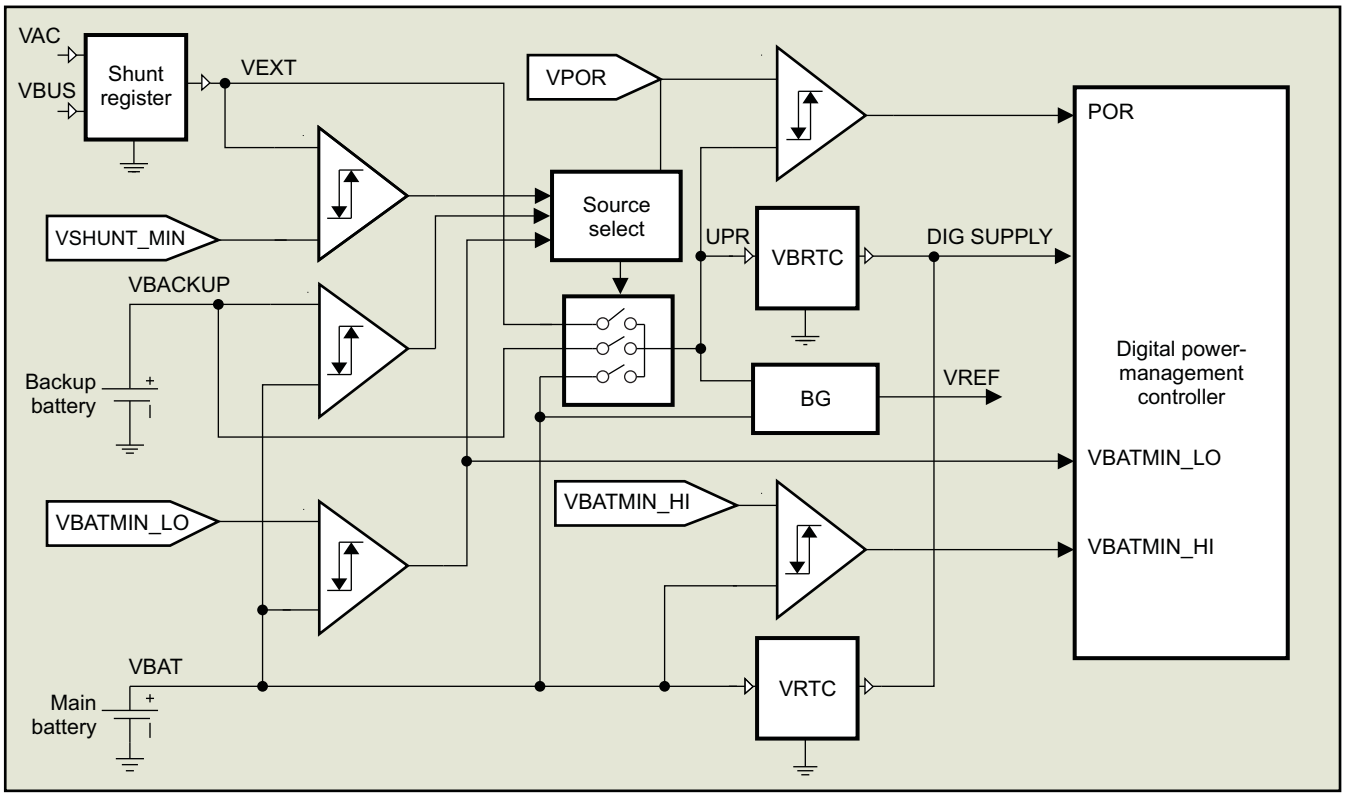

Figure 8. Block Diagram of the Analog Power Control

The boot sequence is shown in Figure 9. This monitoring validates the current state and the transitions between the states.

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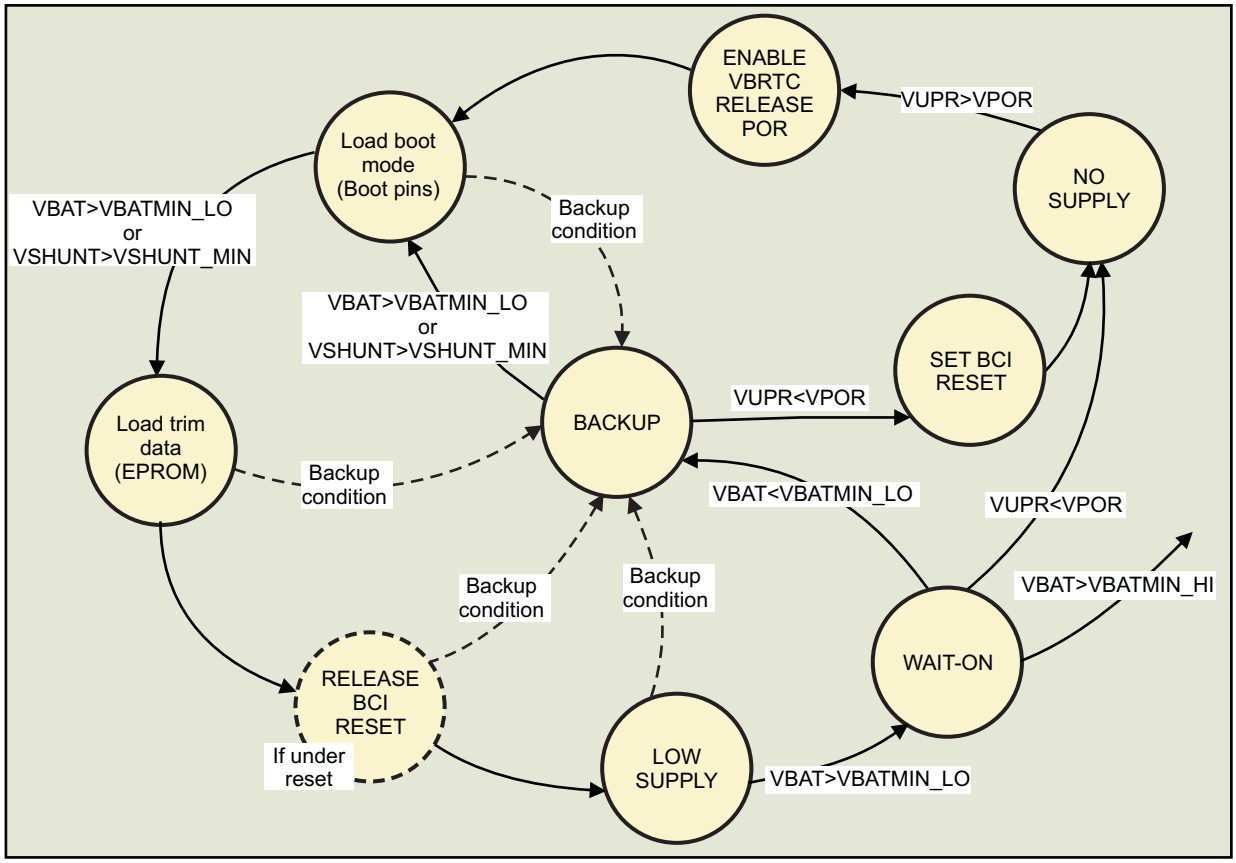

SWCS045-007

Figure 9. Boot Sequence

NOTE

- Backup condition means VBAT < VBATMIN_LO and VSHUNT < VSHUNT_MIN.
- The system is in NO SUPPLY state when VUPR < VPOR.

Figure 10 shows a diagram of the power-state transition.

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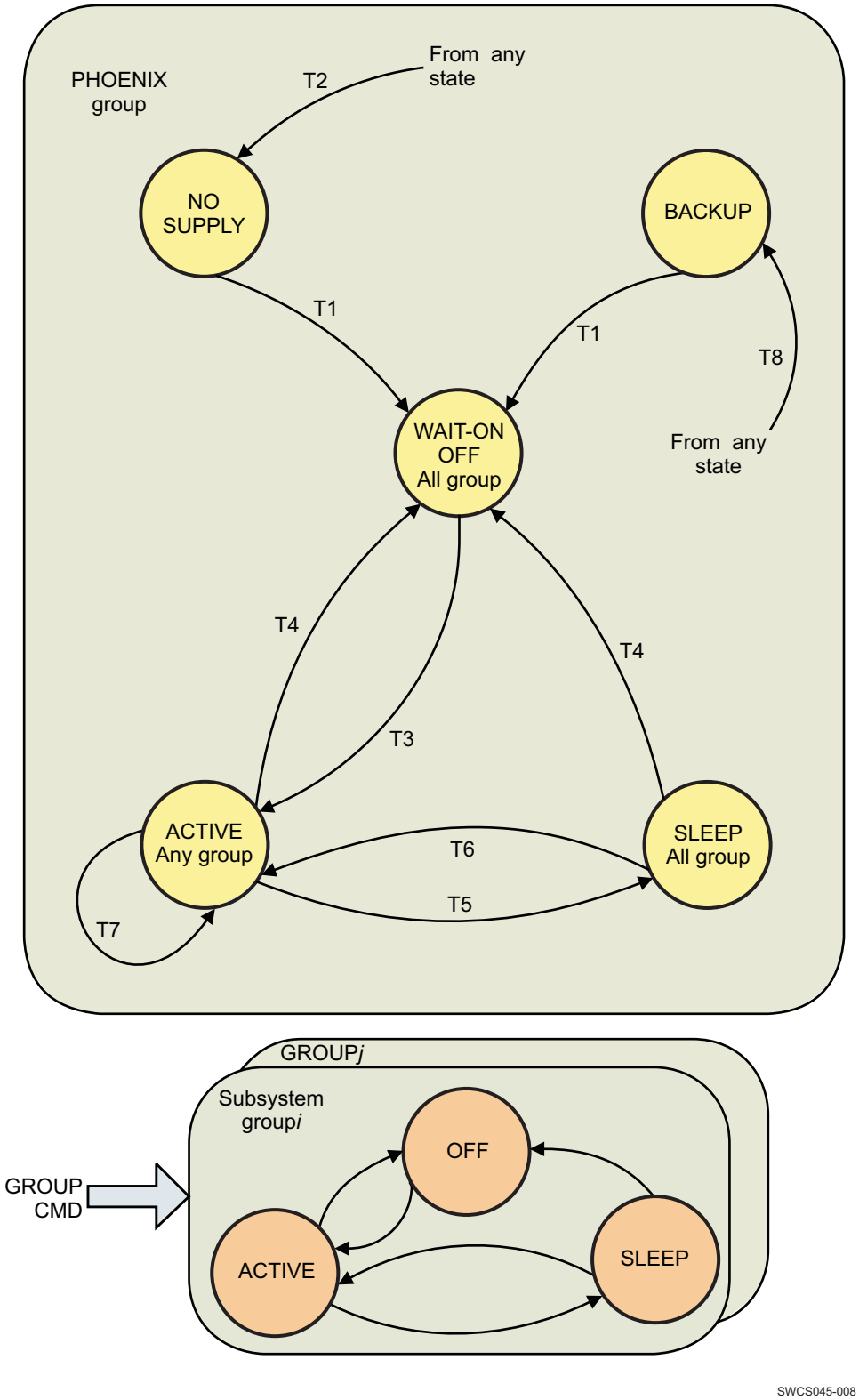

Figure 10. Power-State Transition Diagram

- Power-on transitions: T1
  - System is in NO SUPPLY or BACKUP state. Connection of a valid energy source initiates the transition to

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WAIT-ON state.
  - Triggering event: VBAT > VBATMIN_LO
    - Insertion of a charged main battery
    - Precharge is active, main battery voltage rises
  - Condition: VUPR > VPOR
- Power-off transition: T2
  - The system is in any state. Removal of all energy sources initiates a transition to NO SUPPLY state.
  - Triggering event: VUPR < VPOR
    - Main battery discharge or removal
    - Backup battery discharge or removal
    - Charger unplugged
  - Condition: No more valid energy source
- Switch-on transition: T3
  - The system is in WAIT-ON state, able to accept a hardware switch-on condition, which initiates a transition to ACTIVE state.
  - Triggering event:
    - Push button pressed and released (PWRON)
    - Charging source plug (USB or external)
    - RTC alarm
    - Accessory plug (RPWRON)
    - Insertion of a charged main battery or battery charge running (enabled by default)
    - Software reset (following transition T4)
    - USB ID plug insertion (disabled by default)
  - Condition: VBAT > VBATMIN_HI and no thermal shutdown active
- Switch-off transition: T4
  - System is powered and in ACTIVE or SLEEP state. A hardware condition may initiate a transition to reach WAIT-ON state.
  - Triggering event:
    - Group DEVOFF command (software) (if all other subsystems groups are OFF)
    - Thermal shutdown
    - Primary watchdog timer expired
    - Software reset (followed by transition T3)
    - Long key press (10 seconds) on PWRON
- Sleep-on transition: T5
  - System is powered and in ACTIVE state. A hardware condition initiates a transition to SLEEP state.
  - Triggering event: Subsystem group sleep command (hardware) (PREQ# balls)
  - Condition: All other subsystem groups are SLEEP or OFF.
- Sleep-off transition: T6
  - System is powered and in SLEEP state. A hardware condition initiates a transition to ACTIVE state.
  - Triggering event:
    - Subsystem group active command (hardware) (PREQ# balls)
    - Warm reset (reinitialization of the TWL6030 device)
- Active reset transition: T7
  - System is powered and in ACTIVE state. A hardware condition initiates a reset, system remains in ACTIVE state.
  - Triggering event: Warm reset (reinitialization of the TWL6030 device)
- Backup-on transition: T8
  - System is powered and in ACTIVE, SLEEP, or WAIT-ON state. The detection of a low main battery initiates the transition to BACKUP state.
  - Triggering event: Battery voltage < VBATMIN_LO (discharge/removal)

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– Condition: VUPR > VPOR

BATTERY CHARGING

The TWL6030 device has an integrated switch-mode charger to charge the battery from the USB connector. Figure 11 shows a block diagram of the USB charging electronics.

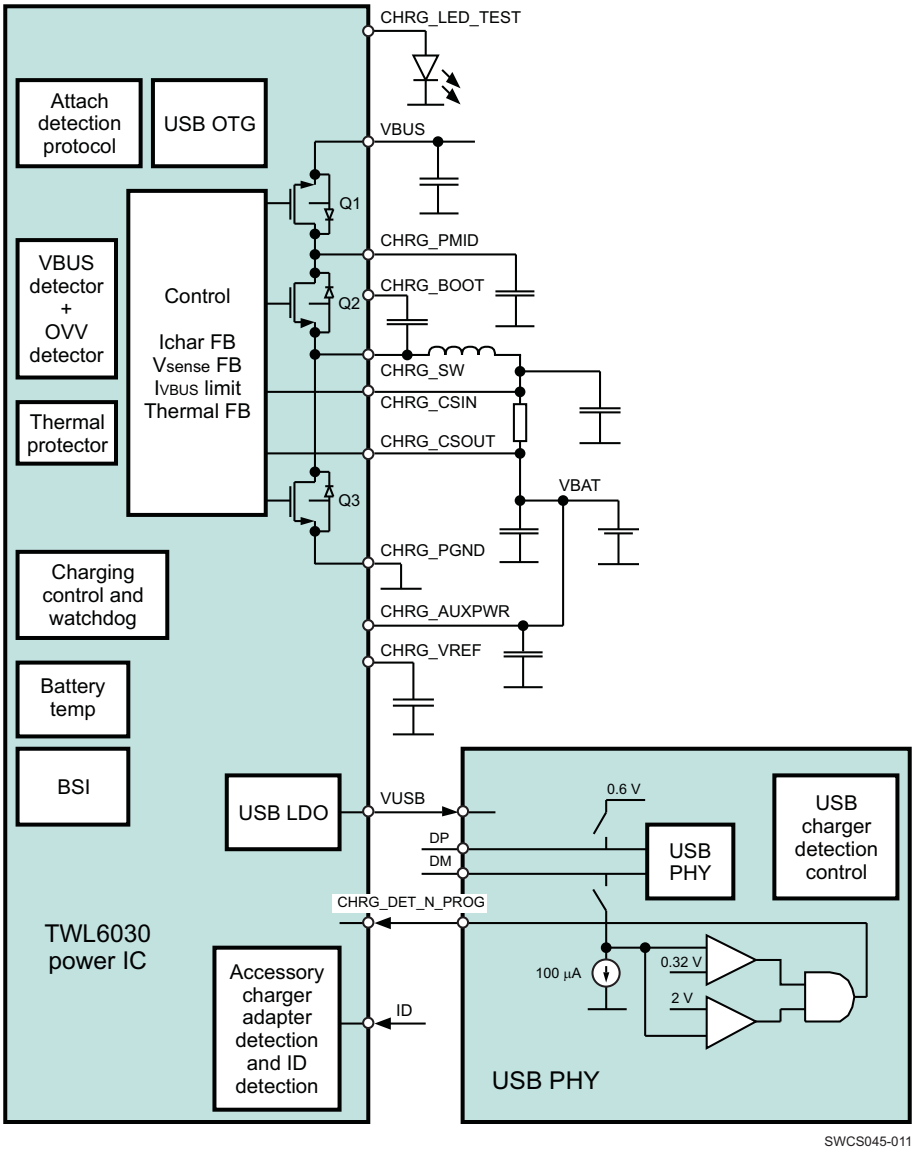

Figure 11. Block Diagram of the Battery Charger

The main features of the charger are:

- High-efficiency battery charger from the USB connector
- Interface to support external customer-specific charger and to monitor (through the CHRG_EXTCHRG_STATZ pin) the status of the external charge path (VAC)
- Built-in input current limiting
- Charging source voltage operating range: 4.0 to 6.3 V
- Integrated power FETs up to 1.5 A charging current
- Tolerate a voltage from –0.3 to 20 V on charger input related balls
- Programmable charge parameters:

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  - Input current limit
  - Fast-charge/termination current
  - Charge voltage
  - Input voltage collapse
  - Safety timer
  - Termination enable
- Synchronous fixed-frequency PWM controller operating at 3 MHz with 0% to 99.5% duty-cycle
- High-accuracy voltage and current regulation
- Automatic high-impedance mode for low power consumption
- Safety timer with reset control
- Reverse leakage protection prevents battery drainage
- Thermal regulation and protection
- I/O overvoltage protection
- Output for charging LED indicator
- Automatic charge current setting (preventing charge input from collapsing) as charge time optimization
- Boost mode operation for USB OTG supply (VBUS supply at 5 V/200 mA current)

The TWL6030 device supports a wide variety of rechargeable lithium-based battery technologies. Recent battery technologies, such as Li-SiAn and LiFePo4, present a flat discharge region in the range of 3.2–3.3 V; technologies such as LiCoO2 and LiNiMnCoO2 present a flat discharge region in the range of 3.6–3.7 V. To support the different battery chemistries effectively, the TWL6030 device has programmable VBATMIN thresholds.

The charging procedure consists of hardware-controlled preconditioning and precharging phases and software-controlled full-charging phase. The charger also performs monitoring functions:

- AC charger detection
- VBUS detection
- Battery presence detection
- VBUS overvoltage detection
- Battery overvoltage detection
- Battery end-of-charge detection
- Thermal protection
- Watchdogs

Charging Phases

Preconditioning

Preconditioning is automatically enabled as soon as the charging source is detected and operates in a constant current charging mode. During preconditioning the battery voltage is below 2.1 V (VBAT_SHORT) and the charging current is limited to 30 mA (IBAT_SHORT). In this mode, the charger uses a linear charging operation mode. This phase detects a defective (shorted) battery. As soon as the battery voltage is above 2.1 V, a precharging phase is entered automatically.

Precharge Phase (Hardware Controlled)

The precharging phase is entered when battery voltage is above 2.1 V (VBAT_SHORT) and the charging source is detected. If the charging source collapses during the precharge phase, the precharge current is automatically reduced to a value that keeps the input voltage high enough to ensure proper operation of the precharge circuitry.

The TWL6030 device supports two precharging modes:

- Slow constant current precharging for 2.1 V < VBAT < 3.54 V (VBUS current is limited to 92 mA from USB standard downstream port)
- Fast constant current precharging for 2.1 V < VBAT < 3.54 V (VBUS current is limited to 470 mA and battery charging current set to default charging current value when USB charging port detected)

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Full-Charge Phase (Software Controlled)

Full-charge can start only when the battery voltage is above VBATMIN_HI, because this phase is under the control of the host processor, and it stops when the battery voltage is below VBATMIN_LO. During this phase, the following resources are available to control the charge process.

- Charge current set point register VICHRG[3:0] (constant current mode)
- Charge voltage set point register VOREG[5:0] (constant voltage mode)
- End of charge current set point register VITERM[2:0] (minimum current when in constant voltage mode)
- Input limit current set point register CIN_LIMIT[3:0] (maximum current drawn from charging source)
- Input voltage set point register BUCK_VTH[2:0] (VBUS voltage collapsing level)
- Charge watchdog set point (programmable up to 127 s, 32 s by default)

If the charging source collapses during the full-charge phase, the full-charge current is automatically reduced to a value keeping the input voltage higher than the preset value, to ensure proper operation of the charge circuitry.

If the charging current termination is enabled, the charging is stopped if the current decreases below the preset limit during constant voltage charging. This indicates the end of the charge period.

Figure 12 shows the battery thresholds.

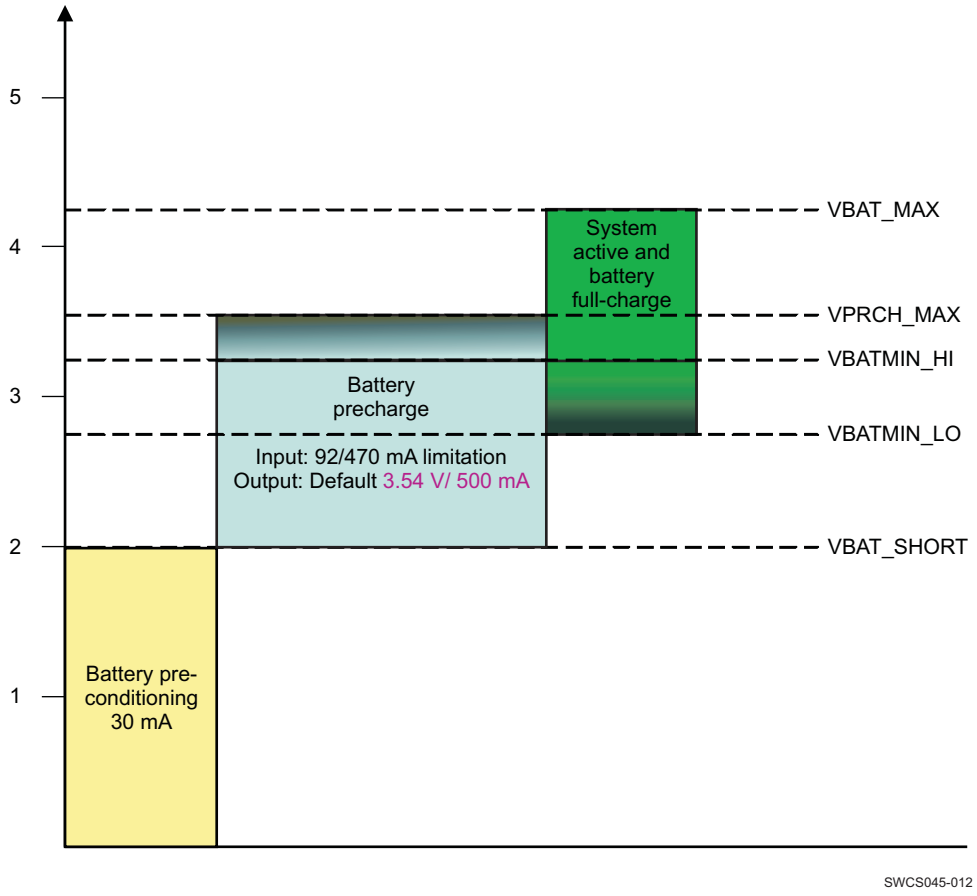

Figure 12. Battery Thresholds

Charger Controller Operation

If VAC or VBUS is detected when the battery voltage is above VPRCH_MAX, charging is enabled by the charger controller, but gated by the USB charger and VAC charger because the voltage is above the default charging

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voltage. The TWL6030 device initiates startup and indicates the reason for the startup in a register. If the battery voltage is between VBATMIN_HI and VPRCH_MAX, charging is started and the TWL6030 device initiates startup. If the battery voltage is below VBATMIN_HI, charging is started and the TWL6030 device initiates startup when the battery voltage crosses the VBATMIN_HI level. If the device is already powered on when the charger is attached, the TWL6030 device only generates an interrupt for the software.

The simplified state transitions during charging are presented in Table 15. The gating of the charging means that the charging is disabled but continues if the reason for the gating disappears. The charging termination means that the charging is stopped. To continue charging, the charger must reconnect or software must enable the charging by writing a software bit. The WD column indicates the operation of charging watchdog. The INT column indicates the generation of the interrupt, R signifying rising edge and F signifying falling edge. In addition, the interrupt generation can be masked for different reasons by register bits. The REGISTER RESET column indicates which register groups are reset.

During startup charging, the charging state-machine controls the charging until software takes control over charging by updating watchdog operation or by changing the USB charging-related current or voltage values.

The default watchdog times are selectable by EPROM bits. The watchdog time during full charge is selected by register bits.

Table 15. Simplified State Transitions During Charging

		PRECONDITIONING OR PRECHARGE NRESPWRON = 0			FULL CHARGE NRESPWRON = 1			REGISTER RESET	COMMENTS
REASON	**BIT/SIGNAL PARAMETER**		**WD**	**INT**		**WD**	**INT**		
Charger insertion	VBUS_DET VAC_DET (rising)	Charging enabled	HW mode	No	Waiting for software enable	SW mode	Yes	None	Charger insertion
Charger insertion (other one already attached)	VBUS_DET VAC_DET (rising)	Charging source selected by priority	Run	No	Charging continues from the first one	Run	Yes	None	Charger insertion, software selects the priority if NRESPWRON = 1.
VBUS charger undervoltage	POOR_SRC	Gated	Run	No	Gated	Run	R/F	None	If NRESPWRON = 0, VAC charger is enabled after 2.5 s, if attached.
VBUS charger overvoltage	VBUS_OVP	Gated	Run	No	Gated	Run	R/F	None	If NRESPWRON = 0, VAC charger is enabled after 2.5 s, if attached.
VBUS charger overtemperature	TH_SHUTD	Gated	Run	No	Gated	Run	R/F	None	
Battery invalid temperature	BAT_TEMP_ OVRANGE	Gated	Run	No	Gated	Run	R/F	None	
GPADC_IN0 line floating	BRIComp = 1	Gated	Run	No	Gated	Run	Yes (1)	None	Battery pack removal detected. If battery voltage falls below VBATMIN_LO, NRESPWRON is set to low.
Suspend bit	SUSPEND _BOOT = 1	N/A			Gated	Run	No	None	Applies to VBUS charger only
VBUS termination current triggers (enabled by bit)	VITERM [2:0] TERM = 1	Gated	Run	No	Gated	Run	Yes	None	End-of-charge indication; disabled by default by EPROM.

(1) BATREMOVAL also.

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Table 15. Simplified State Transitions During Charging (continued)

		PRECONDITIONING OR PRECHARGE NRESPWRON = 0			FULL CHARGE NRESPWRON = 1			REGISTER RESET	COMMENTS
REASON	**BIT/SIGNAL PARAMETER**		**WD**	**INT**		**WD**	**INT**		
Error in external charging	CHRG_VAC_STATZ = 1	Charging source changed after 2.5 s if the other one is available; otherwise, charging is gated by the external charger.	Run	No	Gated by external charger	Run	Yes	None	Software checks the reason and determines the operation. The error can be: - VAC overvoltage - SLEEP state - Bad adaptor - Battery overvoltage - Thermal shutdown - Timer fault - No battery
Charger removal (one charger attached)	VBUS_DET or VAC_DET (falling)	Terminated		No	Terminated		Yes	Charge group	Charger removal
Charger removal (both chargers attached, the enabled one is removed)	VBUS_DET or VAC_DET (falling)	Charging continues from the remaining charger	Run	No	Terminated		Yes	Charge group	To continue charging from the other charger, software must enable it.
Charger removal (both chargers attached, the enabled one is removed)	VBUS_DET or VAC_DET (falling)	Charging continues	Run	No	Charging continues	Run	Yes	None	
NRESPWRON falling edge	NRESPWRON (falling)	N/A			Terminated		No	All	The reasons can be: - Shutdown (software initiated) - Software reset - Battery voltage dropping below VBATMIN_LO - Primary watchdog expiration - TWL6030 thermal shutdown - Long key press
Primary watchdog expires		N/A			N/A				Sets NRESPWRON to low
32-kHz crystal oscillator stops		Terminated		No	Terminated		No	All	
Charging watchdog expires		Terminated		No	Terminated		Yes	Charge group	
Battery voltage dropping below VBATMIN_LO	VBATMIN_LO (falling)	N/A							Sets NRESPWRON to low
TWL6030 thermal shutdown	THPROT = 1	N/A							Sets NRESPWRON to low
Warm reset	NRESWARM	N/A			Terminated		No	All	Is loader software executed here? Limit register reset.
Watchdog reset	WDG_RST or WDT [6:0]	N/A			Continued	WDT[6:0]	No	None	Watchdog in software mode. Software takes control over charging.

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Table 15. Simplified State Transitions During Charging (continued)

		PRECONDITIONING OR PRECHARGE NRESPWRON = 0			FULL CHARGE NRESPWRON = 1			REGISTER RESET	COMMENTS
REASON	**BIT/SIGNAL PARAMETER**		**WD**	**INT**		**WD**	**INT**		
VBUS current/voltage setting change	VICHRG [3:0] or VOREG [5:0]	N/A			Continued	Run	No	None	Watchdog in software mode. Software takes control over charging.
Enable charging by software	EN_CHARGER = 1	N/A			Charging enabled	WDT[6:0]	No	None	
Disable charging by software	EN_CHARGER = 0	N/A			Terminated		No	Charge group	

Anticollapse Loop

The analog anticollapse loop operates so that the input voltage is monitored continuously and the charging current is set by analog loop to maintain the defined input voltage.

Battery Temperature Measurement

The battery temperature is measured using an external NTC resistor. The measurement is enabled before the charging starts and the temperature is constantly monitored during charging. If the battery temperature is outside the valid range, the charging is gated; if the temperature returns inside the valid range, the charging continues. If a battery dies, the battery temperature is monitored so that the charging does not start if the temperature is outside the valid range. The gating of the charging can be disabled with an EPROM bit if needed.

The module is enabled if VBUS or an external charger is detected. An interrupt is always generated when the battery temperature crosses the temperature limits in both directions. The interrupt generation can be masked if needed.

Figure 13 shows the battery temperature measurement circuitry.

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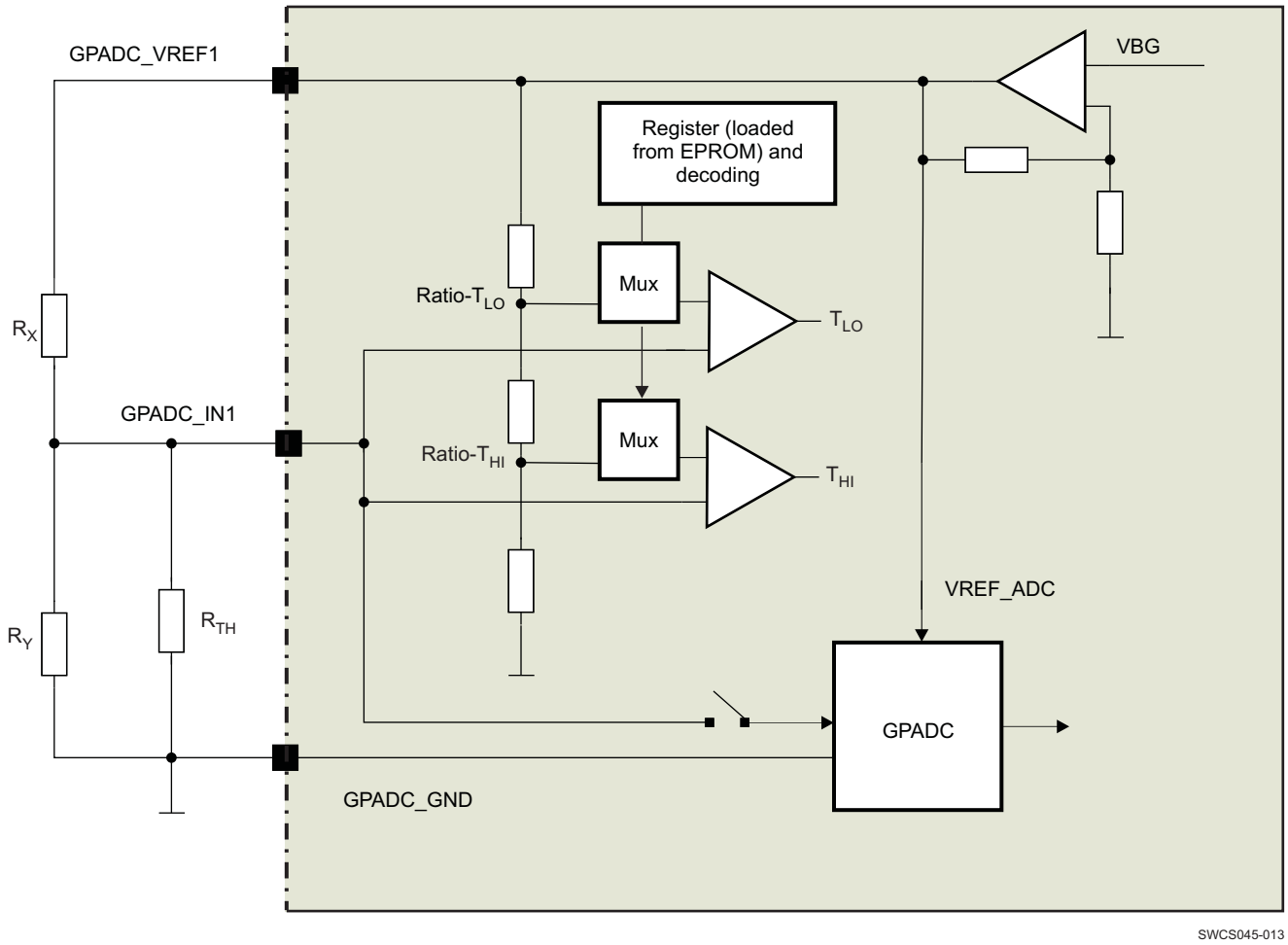

Figure 13. Battery Temperature Measurement

Because the NTC characteristic is highly nonlinear, it is combined with two resistors allowing linearization of its characteristic and making the sensitivity of the system more constant over a wide temperature range. The resulting voltage at GPADC_IN0 can be measured using the GPADC and is also monitored by two comparators that enable the charge of the battery only when the temperature is within a specified window, typically 0°C to 60°C. Resistors R_X and R_Y are used to set the desired temperature threshold levels.

Charging Watchdog

The charging watchdog time depends on the charging control mode and on the USB charger detection result. During hardware-controlled charging, the watchdog time for the USB charging port is approximately 6 minutes for the USB standard downstream port and approximately 14 minutes for a customer-specific charger. Longer values can be selected with the EPROM bit: 11 minutes instead of 6 minutes and 29 minutes instead of 14 minutes. Charger source dependency on WDG values can be enabled and disabled by EPROM. If disabled, the WDG value is always set as for the USB standard downstream port and for the customer-specific charger (longer WDG value). During software-controlled charging, software can select the watchdog time up to 127 seconds. The transition from hardware-controlled charging to software-controlled charging occurs when software updates the WDG_RST, WDT[6:0], VICHRG[3:0], or VOREG[5:0] bits. The different watchdog times are summarized in the following table.

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EPROM (CHARGING SOURCE DEPENDENCY)	CHARGING SOURCE	CHARGING CONTROL	EPROM (WDG VALUE)	WATCHDOG TIME	
				MIN	MAX
1	USB charging port	Hardware	0	5 min 4 s	5 min 36 s
1	Others	Hardware	0	13 min 13 s	14 min 15 s
1	USB charging port	Hardware	1	10 min 10 s	11 min 12 s
1	Others	Hardware	1	26 min 26 s	28 min 29 s
0		Hardware	0	13 min 13 s	14 min 15 s
0		Hardware	1	26 min 26 s	28 min 29 s
	All	Software (programmable)	X	0	127 s

Limit Registers

During full-charge phase, software sets the charging voltage and current. However, the TWL6030 device limits the current and voltage to a level that is defined in the limit registers. The limit registers in the TWL6030 device must be written just after the startup. Software must check the battery type and define the maximum charging current and voltage for the battery being used, write the limit values, and lock the limit registers with the LOCK_LIMIT register bit, so that these cannot be changed when the device is powered on. The limit values are reset during power off by the NRESPWRON signal and they must be written by software during every power up. This ensures that third-party software or a virus cannot set a charging current or voltage that is too high.

Battery Presence Detector

The TWL6030 device supports battery detection. The presence of the battery can be detected with the GPADC_IN0 input signal. The interface has two different functions:

- Detect battery removal/presence
- Measure the size of the resistor connected to the GPADC_IN0 line in the battery pack using the GPADC

Battery pack removal is detected by a comparator that monitors GPADC_IN0. The battery pack must have a pulldown resistor (R_{BRI}) and the TWL6030 device has a current source (I_{BRI}) in the line. If the battery pack is removed, GPADC_IN0 rises above the comparator threshold level, the battery removal is detected, and the TWL6030 device sends an indication to the host processor. In addition, battery charging is terminated if the battery is not present. Battery removal is detected with a comparator and a current source is supplied on the VRTC supply domain. This supply scheme allows the detection in a dead battery case configuration, because the VRTC can be supplied from the VBUS or VAC lines. The battery presence detection module is enabled during the charging and during the ACTIVE and SLEEP states.

Figure 14 shows a block diagram of the battery presence detection module.

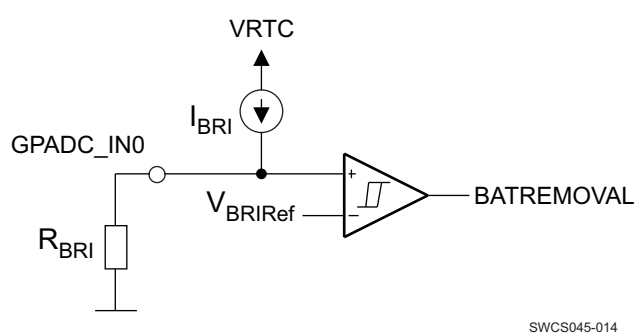

Figure 14. Battery Presence Detector

Indicator LED Driver

The TWL6030 device has an indicator LED driver that indicates charging is ongoing during hardware-controlled

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charging. During hardware-controlled charging, the LED driver is enabled only if the USB charger or external charging IC is charging the battery, and it is turned off if the battery is not charged (for example, because of charger overvoltage). The supply for the charging indicator LED driver is generated from CHRG_PMID or VAC, depending on the active charging path. The CHRG_PMID pin is used instead of the VBUS line so that the LED indicator current is included into the VBUS input current limit.

During power on, software can control the indicator LED regardless of the charging. The supply for the LED can be selected as CHRG_PMID, VAC, or CHRG_LED_IN. The current level can also be selected and the dimming function can be used. Dimming is done with a 128-Hz PWM signal, which has 255 linear steps. The LED output pin has a selectable pulldown when the module is disabled; the pulldown is enabled by default.

BOOST mode

For OTG operation, the TWL6030 device can supply VBUS (5 V) in boost mode. In this mode, the TWL6030 device delivers up to 200 mA current to the USB connector. Boost mode can be enabled through register access by writing OPA_MODE in the CHARGERUSB_CTL1 register. In VBUS supply generation mode, the TWL6030 device can detect a short circuit in the VBUS line. If a short circuit is detected, the VBUS voltage generation stops and an interrupt is generated to the host processor.

Supported Batteries

TWL6030 supports the following battery technologies:

- Li-Ion
- Li-Ion polymer
- Cobalt-Ni-Manganese
- LiCoO2
- LiNiMnCoO2
- Li-SiAn
- LiFePo4

Recent battery technology such as Li-SiAn and LiFePo4 presents a flat discharge region in the range of 3.2–3.3 V; technologies such as LiCoO2 or LiNiMnCoO2 presents a flat discharge region in the range of 3.6–3.7 V. This results in different VBATMIN thresholds, depending on the type of battery used in the system. As a consequence, the VBATMIN thresholds are programmable.

Supported Charging Sources

The following chargers are supported with the integrated switch-mode charger from the USB connector:

- Dedicated charging port
- Charging downstream port
- Charger full-filling specification YD/T 1591-2006

To configure the charger for proper operation mode depending on the charging source characteristics, the charging source type must be detected and identified. The detection of the charger attached to the USB connector is made inside the TWL6030 device by detecting a voltage greater than VINmin on charger input.

To minimize the capacitance of the data lines, the type of the charger connected to the USB connector can be identified by the USB PHY, and the information of the maximum current drawn from the charging source must be transmitted to the TWL6030 device with a dedicated signal. The TWL6030 device enables detection by delivering VUSB supply. The charger detection circuitry must deliver a CMOS level (VUSB) signal to the TWL6030 device, CHRG_DET_N, by default a high logic level indicating that USB charging port is detected. The polarity of the charger detection signal can be selected with an EPROM bit. The identification of the accessory charger adapter (ACA) occurs in the TWL6030 device.

The TWL6030 device can be interfaced with an ACA (external to the terminal) to support the charging from the USB charger and USB communication to other USB devices from the USB port. See the USB OTG section for a description of ACA detection.

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Support for External Charging IC

The TWL6030 device can be interfaced with an auxiliary stand-alone charger device to support the following use cases:

- Simultaneous battery charge from a non-USB charger (different connector) and OTG operating mode (the TWL6030 device internal USB charger used as VBUS supply)
- Charging from the sources not connected to USB connector

Figure 15 shows an example of an external charging IC supported by the TWL6030 device.

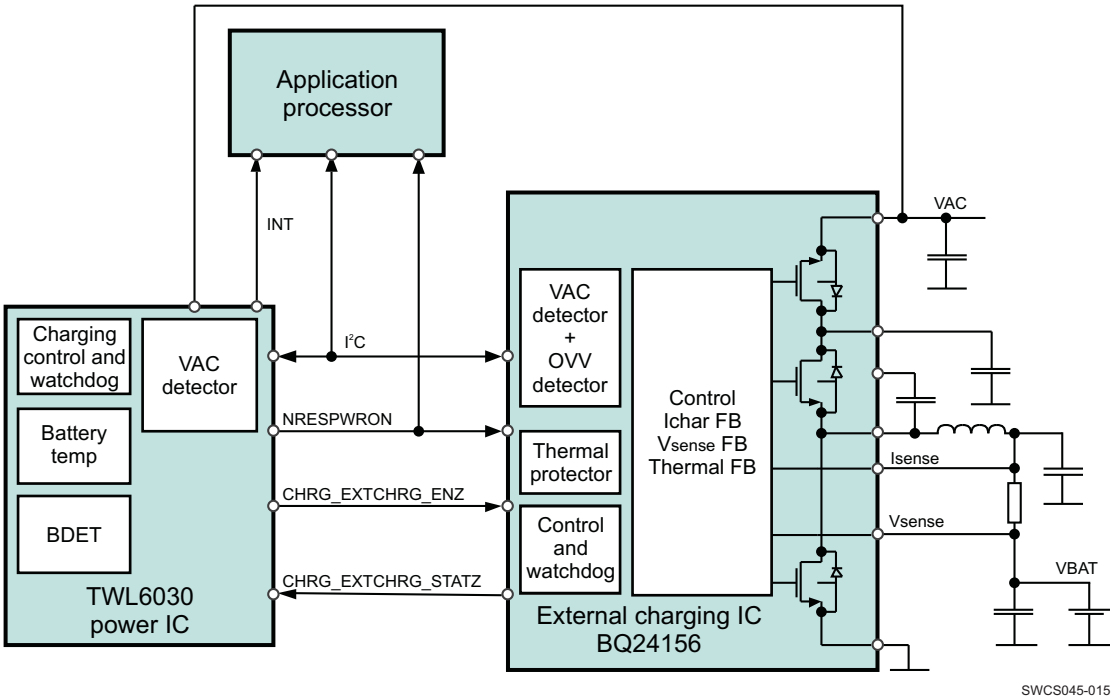

Figure 15. External Charger Interface

The external charging IC is enabled with 1.8-V CMOS level signal, CHRG_EXTCHRG_ENZ. Low logic level indicates that charging is enabled. Charging status is indicated with the CHRG_EXTCHRG_STATZ signal. The external charging IC pulls the signal down during charging.

The integrated USB charger can be associated with an external VAC (wall) charger. For that reason, VAC wall charger input is connected to the TWL6030 device to define the charge priorities:

- When the VBUS is detected and the VAC is not detected, the USB charge starts.
- When the VAC is detected and the VBUS is not detected, the external charging starts.
- When the VBUS and VAC are detected, the USB charge starts only if the CHRG_DET_N pin is set high so the USB charge has a 475-mA input current limitation.
  - When CHRG_DET_N = 0 (100-mA input current USB limitation), the VAC wall charger is expected to be better (or equivalent) and thus is chosen as the default charge path.
  - When CHRG_DET_N = 1 (500-mA input current USB limitation), the precharge associated with a USB is expected to be sufficient for battery-level quick recovery if the USB charge path is chosen.

If there is fault condition on a charger during hardware-controlled charging and the fault condition continues at least 2.5 s, the charging source is changed for lower-priority charger. The change into lower-priority charger only prevents the infinite looping between chargers. If only one charger is attached, the charger is not disabled in fault condition and if the fault condition does not disappear, the charging is terminated when the watchdog expires.

USB OTG

The TWL6030 device supports the Battery Charging Specification Revision 1.1 and both OTG 1.3 and OTG 2.0 standards. The OTG revision number is hardware predefined by an EPROM bit.

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The TWL6030 device embeds all hardware analog mechanisms associated to VBUS and ID lines. The other aspects of the OTG system, such as the OTG controller (hardware/software) or the USB data line (DP/DM) with HNP and SRP signaling, are embedded in the USB PHY, which can be either integrated into application processor or there is stand-alone USB OTG PHY. Equally, the other aspects of Battery Charging Specification Revision 1.1 relative to DP and DM pins are embedded in the USB PHY.

The TWL6030 device supports the following functions:

- OTG Revision 1.3:
  - USB VBUS detections (comparators and associated interrupts):
    - OTG A-device (VA_VBUS_VLD, VA_SESS_VLD)
    - OTG B-device (VB_SESS_VLD, VB_SESS_END)
  - OTG A-device 5-V VBUS power supply provider
  - OTG B-device USB Session Request Protocol (SRP) – VBUS pulsing method:
    - VBUS charge mode (VBUS_CHRG_VBAT, VBUS_CHRG_PMID)
    - VBUS discharge mode (VBUS_DISCHRG)
  - USB ID detections (comparators and associated interrupts):
    - OTG A-device (ID_GND)
    - OTG B-device (ID_FLOAT)
- OTG Revision 2.0:
  - USB VBUS detection (comparators and associated interrupts):
    - OTG A-device/OTG B-device (VOTG_SESS_VLD)
    - OTG A-device (VA_VBUS_VLD)
  - OTG A-device 5-V VBUS power supply provider
  - Embedded attach detection protocol (ADP) mechanism (comparators and associated interrupts):
    - OTG A-device/OTG B-device ADP probing:
      - VBUS charge mode (VBUS_IADP_SRC)
      - VBUS discharge mode (VBUS_IADP_SINK)
      - VBUS probe measurement (VADP_PRB)
    - OTG B-device ADP sensing (VADP_SNS)
  - USB ID detections (comparators and associated interrupts):
    - OTG A-device (ID_GND)
    - OTG B-device (ID_FLOAT)
- Battery Charging Specification Revision 1.1:
  - USB ID detections for ACA (comparators and associated interrupts):
    - OTG A-device (ID_GND)
    - ACA pulldown, OTG A-device (ID_A)
    - ACA pulldown, OTG B-device cannot connect (ID_B)
    - ACA pulldown, OTG B-device can connect (ID_C)
    - OTG B-device (ID_FLOAT)
  - ID ACA mechanism available in both precharge (hardware) and SLEEP/ACTIVE states (software)
- TWL6030 additional features:
  - VBUS wake-up detection (VBUS_WKUP) (maskable/rising edge)
  - VBUS overvoltage detection (always on, combined with charger IP)
  - VBUS precharge (combined with charger IP)
  - ID wake-up detection (ID_WKUP) (programmable, disabled by default)
  - ID pulldown (ID_GND_DRV), pullups (ID_PU_220K, ID_PU_100K)
  - ID current sources (ID_SRC, ID_WKUP_SRC)
  - GPADC VBUS monitoring (VBUS_MEAS)
  - GPADC ID monitoring (ID_MEAS)

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There are two types of VBUS and ID comparators, referred to throughout this section as wake-up (normally used in TWL6030 SLEEP state) and active comparators (generally activated in TWL6030 ACTIVE state). Use of these comparators is not exclusive to TWL6030 SLEEP and ACTIVE states, but can also serve in additional use cases. Indeed, the wake-up comparators target low power consumption, whereas the active comparators are intended for accurate level detection:

- The wake-up comparators operate in TWL6030 PRECHARGE, WAIT-ON, SLEEP and ACTIVE states. These comparators can wake up the device from a SLEEP state but can also switch on the device from a WAIT-ON state. VBUS wake-up comparator can also start the precharge, providing that all other precharging conditions are met.
- The active comparators operate in TWL6030 SLEEP and ACTIVE states. When operating in SLEEP state, all required power and clock resources should remain active. ID active comparators, used for ACA detection, are automatically enabled in precharge mode; VBUS active comparators remain off.

Table 16. OTG IP Features vs Register Bits/Modes/Supplies

FUNCTION/FEATURE	REGISTER/REGISTER BIT	OTG REV.	TWL6030 MODE/STATE	SUPPLIES NEEDED
Vendor ID	USB_VENDOR_ID_LSB USB_VENDOR_ID_MSB	–	ACTIVE	VRTC
Product ID	USB_PRODUCT_ID_LSB USB_PRODUCT_ID_MSB	–	ACTIVE	VRTC
SRP – Pulsing method VBUS charge on VBAT	VBUS_CHRG_VBAT	1.3	ACTIVE	VRTC VBAT
SRP – Pulsing method VBUS charge on PMID	VBUS_CHRG_PMID	1.3	ACTIVE	VRTC CHRG_PMID
SRP – Pulsing method VBUS discharge	VBUS_DISCHRG	1.3	ACTIVE	VRTC
ADP – Probing VBUS charge	VBUS_IADP_SRC	2.0	ACTIVE	VRTC VANA
ADP – Probing VBUS discharge	VBUS_IADP_SINK	2.0	ACTIVE	VRTC
VBUS detection	VBUS_ACT_COMP	1.3 2.0	SLEEP ACTIVE	VRTC VANA
VBUS wake-up detection	Always enabled if VBUS or VAC is present	–	PRECHARGE/OFF SLEEP/ACTIVE	VRTC
VBUS GPADC measurement	VBUS_MEAS	–	ACTIVE	VRTC VANA
ID 220-kΩ pullup on VUSB	ID_PU_220K	–	ACTIVE	VRTC VUSB
ID 100-kΩ pullup on VUSB	ID_PU_100K	–	ACTIVE	VRTC VUSB
ID ground drive	ID_GND_DRV		ACTIVE	VRTC
ID 16-µA source current	ID_SRC_16U	BC 1.1	PRECHARGE SLEEP/ACTIVE	VRTC VUSB
ID 5-µA source current	ID_SRC_5U	–	ACTIVE	VRTC VUSB
ID detection	ID_ACT_COMP	BC 1.1	PRECHARGE SLEEP/ACTIVE	VRTC VUSB
ID wake-up detection	ID_WK_UP_COMP	–	OFF SLEEP/ACTIVE	VRTC
ID GPADC measurement	ID_MEAS	–	ACTIVE	VRTC VANA

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NOTE

- The VBUS and ID wake-up comparators are a start event condition when the TWL6030 device is in WAIT-ON state. If VBUS wake-up enable is fixed, ID wake-up enable is configurable and disabled by default. Those comparators can also make the TWL6030 device leave SLEEP state and enter ACTIVE state. An interrupt is always sent to the host processor, but only if the masks are not applied.
- In PRECHARGE state, the VBUS wake-up comparator, the VUSB regulator, the ID comparators, and the 16-µA current source are enabled automatically by both OTG and PM state-machines. The ACA identification is required by the charger FSM for the allowed current charges whether an ACA is attached or not.
- The OTG_REV bit unlocks the respective VBUS detection features and associated electrical parameters specific to each OTG revision 1.3 and revision 2.0 (see the VBUS_ACT_COMP bit).
- For all USB OTG registers, two informative additional rows (OTG 1.3/OTG 2.0) describe if the bits have an application use for each OTG revision.
- All TWL6030 OTG registers are unlocked and operate either with a read/write (R/W) access or with a read/set/clear (R/S/C) process.
- VBUS_ACT_COMP (USB_VBUS_CTRL_SET/USB_VBUS_CTRL_CLR) is the only R/W bit that relies on the OTG_REV EPROM value. This bit enables the needed VBUS comparators, reducing the power consumption of the OTG VBUS analog section. Therefore, all deactivated comparators have their corresponding source and latch registers fixed at 0.
- For some of the analog electrical parameters that are not backward-compatible between OTG revision 1.3 and OTG revision 2.0 but also are not manageable through the OTG_REV preselection bit, it is assumed throughout this section that the OTG revision 2.0 characteristic limits supersede the OTG revision 1.3 electrical limits and, thus, OTG 2.0 is the reference.
- OTG revision 1.3 devices have just emerged on the electronic market and should be outnumbered shortly by OTG revision 2.0 devices.
- In addition, the USB-IF consortium suggests a fast-forward transition to OTG revision 2.0 to solve current incompatibilities and limitations between OTG revision 1.3 devices.
- All electrical parametric deviations from OTG revision 1.3 are explicitly highlighted through this section.
- The full list of nonbackward-compatible electrical parameters is available on the USB-IF website in the developer forum section.

ID Line

The USB Battery Charging Specification describes the operation of ACA detection. This refers to detection of external RID_A, RID_B, and RID_C resistors on ID pin. ID ground ®$_{ID_GND}$) and ID float ®$_{ID_FLOAT}$) are related to the connections of the USB OTG standard plugs. Note that when any one of the RID_A, RID_B, or RID_C resistances is presented at the ID pin, this implies that VBUS supply is provided by the ACA. Thus after wake up from VBUS or ID plug detection (due to VBUS or ID wake-up comparators controlled by ID_WK_UP_COMP, VBUS_WK_UP_COMP register bits), software can then enable the ID active comparators to correctly identify which of the different RID values is present. In addition, an interrupt is generated if the resistance on the ID ball changes.

During hardware-controlled charging, the TWL6030 device monitors if an ACA is connected and sets the corresponding VBUS input current limit.

The following pullup and pulldown resistors and current sources can be connected to the ID line:

- ID_PU_220K register bit enables an ID 220-kΩ pullup to VUSB supply.
- ID_PU_100K register bit enables an ID 100-kΩ pullup to VUSB supply.
- ID_GND_DRV register bit enables an ID 10-kΩ pulldown.
- ID_SRC_16U register bit enables an ID 16-µA current source on VUSB supply.
- ID_SRC_5U register bit enables an ID 5-µA current source on VUSB supply.
- ID_WK_UP_COMP enables an ID 9-µA current source ($I_{ID_WK_SRC}$) on VRTC supply.

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The ID wake-up comparator is used when the TWL6030 device is in WAIT-ON or SLEEP state. It allows the start up of the TWL6030 device when a USB cable A-plug is attached; that is, when a pulldown resistor to ground (ROTG_A) is present on the ID line.

Four comparators, supplied by the VUSB regulator, are implemented to evaluate the external ID resistance. Additional logic between those comparators allows the generation of five debounced interrupts (with fixed 30-ms debouncing) as shown in Figure 16.

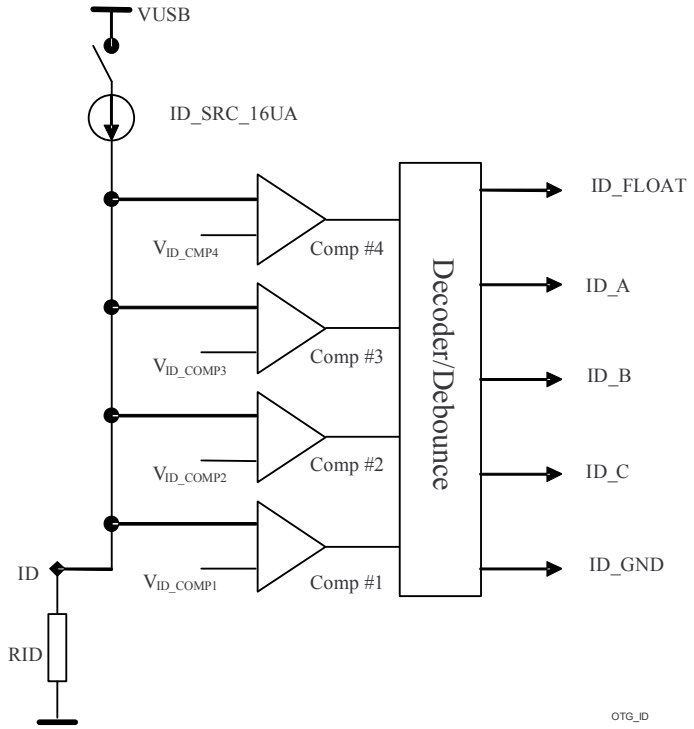

Figure 16. ID Resistance Detection

Interrupts are generated based on the conditions listed in Table 17.

Table 17. Interrupt Generation Conditions

ID PIN LEVEL	GENERATED INTERRUPT				
	ID_GND	ID_C	ID_B	ID_A	ID_FLOAT
$V_{ID} < V_{ID_CMP1}$	1	0	0	0	0
$V_{ID_CMP1} < V_{ID} < V_{ID_CMP2}$	0	1	0	0	0
$V_{ID_CMP2} < V_{ID} < V_{ID_CMP3}$	0	0	1	0	0
$V_{ID_CMP3} < V_{ID} < V_{ID_CMP4}$	0	0	0	1	0
$V_{ID} > V_{ID_CMP4}$	0	0	0	0	1

It is possible to use the GPADC to monitor the voltage on the ID line (channel 14). A 6.875-V maximum voltage on the ID line corresponds to a 1.25-V maximum dynamic at the input stage of the GPADC converter, allowing a 6.0-V maximum measurement.

VBUS Line

The VBUS wake-up comparator is used when the TWL6030 device is in PRECHARGE, WAIT-ON, SLEEP, or ACTIVE state. It allows startup of the TWL6030 device when a USB cable plug is attached; that is, when a VBUS voltage level of 3.6 V minimum is present on the VBUS line.

The VUSB regulator can be enabled or disabled by the VBUS wake-up comparator until the first I^2C write access to the VUSB resource state register (VUSB_CFG_STATE). Note that the VUSB regulator is controlled by the VBUS wake-up comparator only when the NRESPWRON signal is low.

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The ACA comparators and 16-µA current source can be enabled or disabled by the VBUS wake-up comparator until the first I^2C write access to the OTG corresponding registers. Note that ACA feature is controlled by the VBUS wake-up comparator only when NRESPWRON signal is low.

The following pullup and pulldown resistors and current sinks/sources can be connected to the VBUS line:

- VBUS_CHRG_VBAT bit enables a VBUS 2-kΩ pullup to the VBAT supply.
- VBUS_CHRG_PMID bit enables a VBUS 2-kΩ pullup to the CHRG_PMID supply.
- VBUS_DISCHRG bit enables a VBUS 10-kΩ pulldown.
- VBUS_IADP_SRC bit enables a VBUS 1.4-mA current source on the VANA supply.
- VBUS_IADP_SINK bit enables a VBUS 1.5-mA current sink.
- RA_BUS_IN resistor is present permanently and is a combination of all parallel resistor bridges implemented on VBUS in the various IPs such as backup battery, OTG, and charger.
- RVBUS_LKG represents the TWL6030 internal leakage.

Related to the OTG 1.3 revision, four comparators supplied on the VANA regulator are implemented to detect VBUS line voltage level.

In the OTG 2.0 revision, only one comparator is required for the session valid detection (VOTG_SESS_VLD) supplied also on the VANA domain. In addition the VA_VBUS_VLD comparator can be used to detect a possible VBUS short-circuit condition.

The TWL6030 device embeds the OTG 2.0 optional features related to the VBUS ADP probing and sensing, via two additional comparators supplied on VANA (VADP_PRB, and VDAP_SNS).

Seven comparators allow detection of the four OTG 1.3 and the three OTG 2.0 debounced interrupts:

- VA_VBUS_VLD (OTG 1.3/OTG 2.0) – fixed 30 ms debouncing
- VB_SESS_VLD (OTG 1.3) – fixed 30 ms debouncing
- VA_SESS_VLD (OTG 1.3) – fixed 30 ms debouncing
- VB_SESS_END (OTG 1.3) – fixed 30 ms debouncing
- VOTG_SESS_VLD (OTG 2.0) – fixed 30 ms debouncing
- VADP_PRB (OTG 2.0) – fixed 2x 30 µs debouncing
- VADP_SNS (OTG 2.0) – fixed 2x 30 µs debouncing

It is possible to use the GPADC to monitor the voltage on the VBUS line (channel 10). A 6.875-V maximum voltage on the VBUS line corresponds to a 1.25-V maximum dynamic at the input stage of the GPADC converter, allowing a 6.0-V maximum measurement. For more information, see GENERAL-PURPOSE ADC .

NOTE

- If the system switches off, VUSB stays on if VBUS is still connected.
- When NRESPWRON is released, only software accesses enable the regulator, if not previously enabled by the VBUS wake-up comparator in PRECHARGE state.
- The VUSB regulator is a dual input supply LDO. The VUSB regulator enable is independent of the overvoltage condition.
- When a VBUS overvoltage condition occurs, the CHRG_PMID input switch is automatically opened, protecting the VUSB LDO from possible overvoltage stresses.
- When neither the VBAT nor PMID input supply is selected, the VUSB LDO cannot output a proper voltage, even if its control enable is set (see the VUSB_CFG_TRANS register).
- Software should keep monitoring the VBUS overvoltage condition and turn off the VUSB regulator when necessary.
- The VBUS detection mechanism works only when VANA supply is present:
  - TWL6030 SLEEP state – VANA should remain active.
  - TWL6030 ACTIVE state – VANA is always on.
- For ADP detection, software can use the TWL6030 embedded mechanism or directly use the output of the comparators with their associated interrupts.

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ADP on VBUS Line

The ADP feature allows the device to detect when a remote device is attached or detached. The ADP detects the change in VBUS capacitance that occurs when two devices are attached or detached. The capacitance is detected by first discharging (VBUS_IADP_SINK) the VBUS line and then measuring the time it takes for VBUS to charge to a VADP_PRB voltage level with a VBUS_IADP_SRC current source. The change in the capacitance is detected by looking for a change in the T_ADP_RISE charge time. This operation is called ADP probing, which is allowed only for an A-device.

If an A-device is attached to a B-device, and both support ADP features, the A-device performs ADP probing and the B-device performs ADP sensing. During ADP sensing, the B-device searches for ADP probing activity on the VBUS line. If ADP probing activity is detected, the B-device determines that the A-device is still attached.

As shown in Figure 17, the ADP module has timing register bits (T_ADP_HIGH, T_ADP_LOW, T_ADP_RISE), control logic, a current source (VBUS_IADP_SRC), a current sink (VBUS_IADP_SINK), and two comparators: ADP probing (VADP_PRB) and ADP sensing (VADP_SNS).

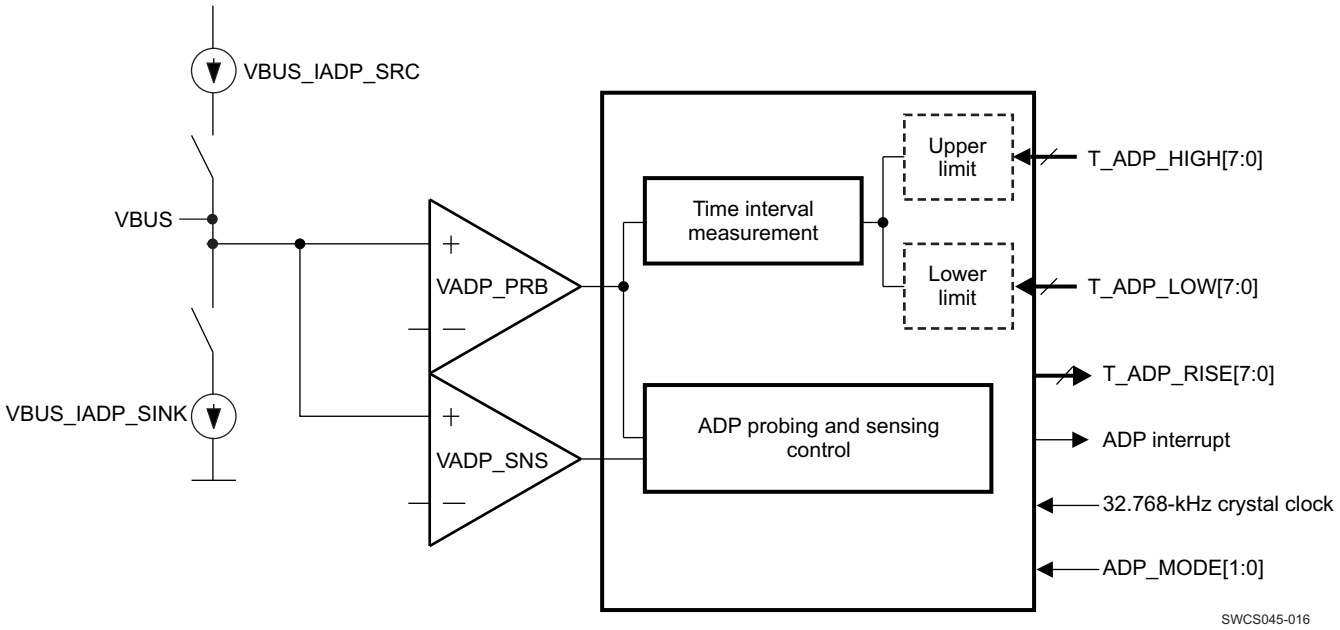

Figure 17. Attach Detection Protocol Scheme

Figure 18 shows the ADP timing diagram.

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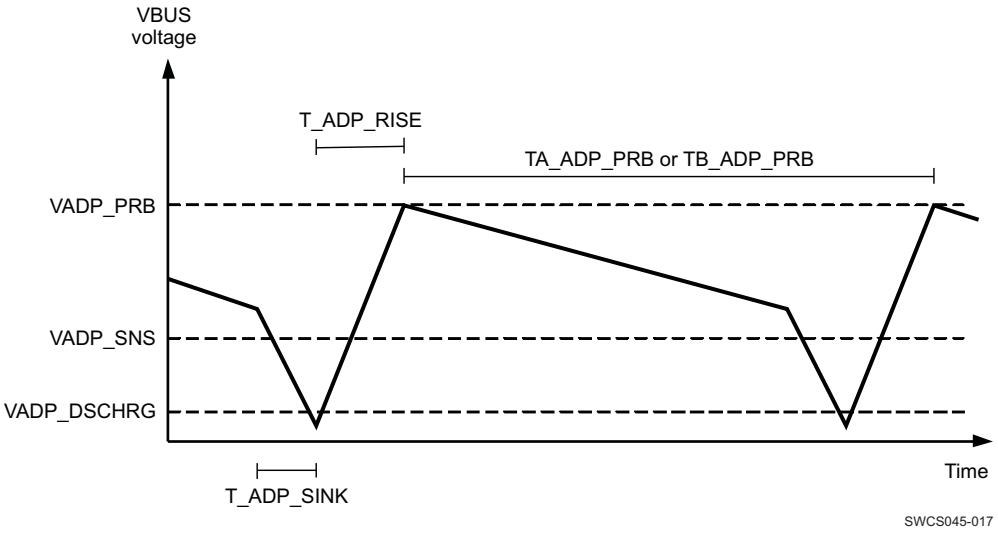

Figure 18. ADP Timing Diagram

ADP_MODE[1:0]	OPERATION
00	ADP digital module is disabled.
01	ADP digital module is enabled.
10	ADP probing mode as an A-device is enabled.

During ADP sensing mode, the VADP_SNS comparator is used. The digital module monitors the comparator output to ensure that it toggles and the time duration between the rising edge of the comparator output signal is shorter than T_ADP_SNS. If there is no new rising edge within the T_ADP_SNS period, the module generates an ADP interrupt.

Figure 19 shows the ADP sensing timing diagram.

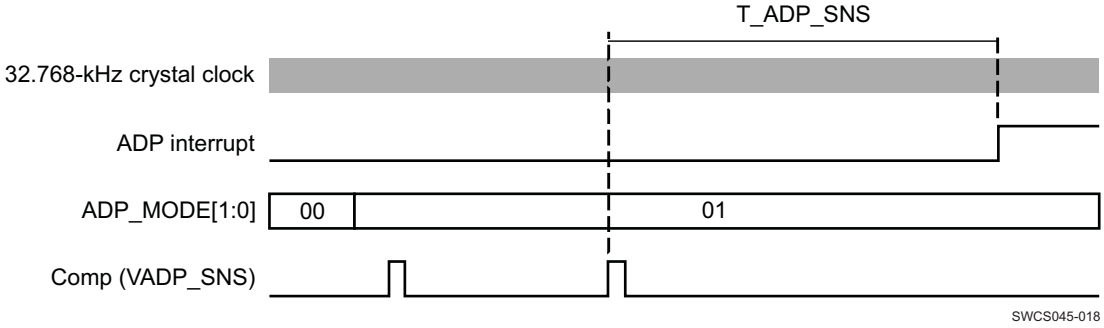

Figure 19. ADP Sensing Timing Diagram

During ADP probing, the VADP_PRB comparator is used. The time interval measurement counter is reset, the comparator is enabled and the VBUS_IADP_SINK current sink is turned on for T_ADP_SINK. The T_ADP_SINK time is long enough to discharge the VBUS voltage below VADP_DSCHG (guaranteed by design). After that, the current sink is turned off, the current source VBUS_IADP_SRC is turned on, and the time interval measurement counter starts to count 32.768-kHz crystal clock cycles. When the VBUS voltage reaches VADP_PRB or the counter value reaches 255 cycles, the current source is turned off, the time interval measurement counter is stopped, and the comparator is disabled. If the measured time interval value is lower than T_ADP_LOW[7:0] or higher than T_ADP_HIGH[7:0], an interrupt is generated. Software sets the limit values so that the operation fulfills requirements of the OTG 2.0 specification. Figure 20 shows the ADP probing timing diagram.

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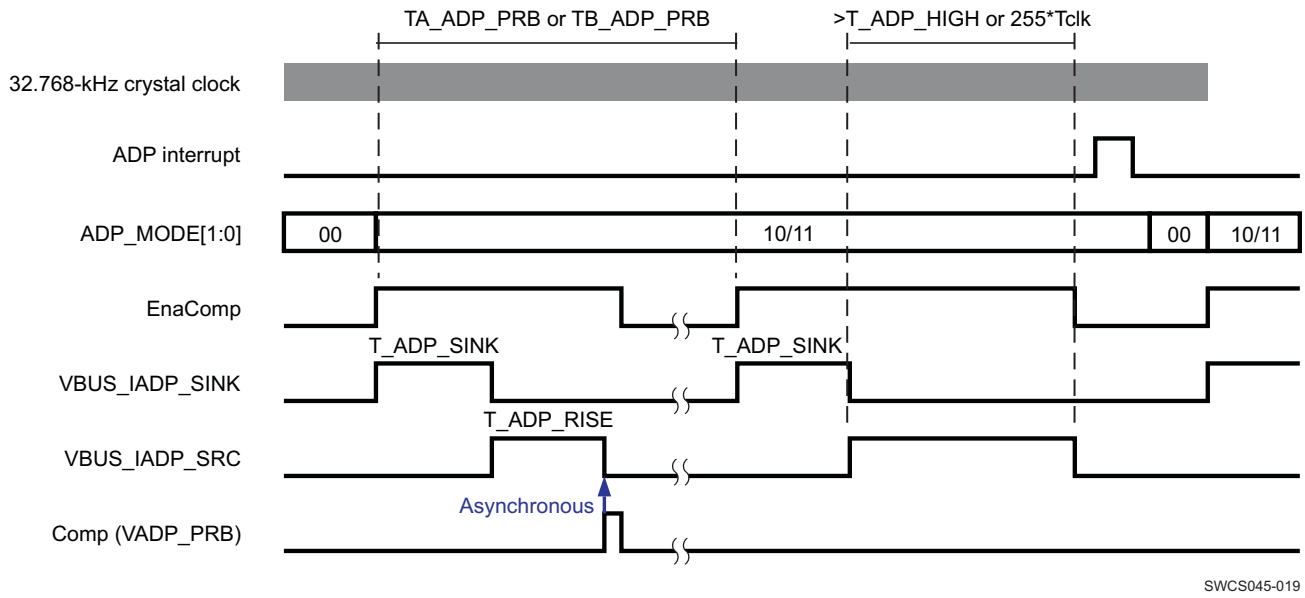

Figure 20. ADP Probing Timing Diagram

GAS GAUGE

The gas gauge, also called the current gauge, measures the current from the battery or the current into the battery. An analog-to-digital converter (ADC) (Coulomb counter) is required to measure the voltage over the external Rsense sense resistor. This resistor is connected to the negative side of the battery. The integration period of the ADC is programmable from 3.9 to 250 ms. The gas gauge works continuously, which means that the new measurement starts immediately after the previous result becomes available. The averaging and the compensation are done by the TWL6030 digital module but requires software controls.

The main features of the gas gauge are:

- Current range: ±6.2A (with 10-mΩ sense resistor)
- ADC clock frequency: 32.768 kHz
- Data size: 13 result bits + 1 sign bit, 2's complement format (with 250-ms integration period)
- Integration periods: 250 ms (default), 62.5 ms, 15.6 ms, 3.9 ms
- Battery discharging gives negative result (sign bit = 1)
- External sense resistor is needed (will be connected the negative side of battery)

Figure 21 shows a block diagram of the gas gauge.

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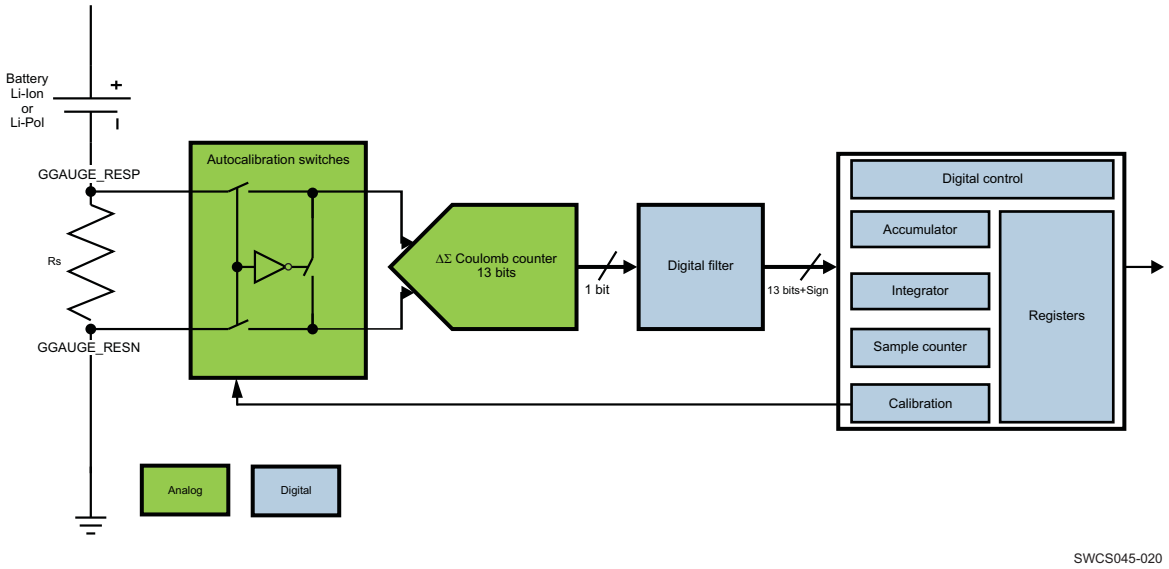

Figure 21. Gas Gauge Block Diagram

Autocalibration

Autocalibration is enabled by software. During autocalibration, the gas gauge performs eight measurements so that the inputs for the ADC are short-circuited. The result indicates the offset error of the gas gauge. The result is stored in the CC_OFFSET[9:0] register bits and the completion of the measurement procedure is indicated with the CC_AUTOCAL interrupt. Software must read the offset error result and use that to compensate the actual measurement results. The CC_CAL_EN bit self clears when the calibration completes. The gas gauge must be enabled while calibration runs. The temperature variation changes the offset error, so the recalibration is preferred during operation.

Auto-Clear and Pause

The auto-clear function is used in the sequence of changing from one integration period to another one. Before changing the integration period, the CC_PAUSE bit must be set to 1. Setting the CC_AUTOCLEAR bit to 1 clears the CC_OFFSET[9:0], CC_SAMPLE_CNTR[23:0], and CC_ACCUM[31:0] registers. The CC_AUTOCLEAR bit is self-cleared once the registers are reset.

Setting the CC_PAUSE bit to 1 keeps the analog from updating the integrator, accumulator, and sample counter registers. The integrator continues to run. If an integration period ends while the CC_PAUSE bit is 1, the value that is normally written to these registers is lost because the next integration period starts automatically.

Dithering

The FGDITHS bit is set to 1 to enable dithering in the ADC, which keeps idle tones from being generated with a DC input value. The FGDITHS bit is not affected by the CC_AUTOCLEAR bit. Use the FGDITHR bit to disable the dithering. The dithering feature status is available in the FGDITH_EN bit.

Operation with Software

Software must first set the correct integration period, enable the gas gauge, and perform the calibration to derive the offset error and use the error to make corrections to the measurement results. The gas gauge enters normal operation automatically when calibration completes. After that, software can read the sample counter and accumulator results and calculate the energy accordingly.

To record the current consumption waveform, software must set a timer of the integration period to read every integration sample result. Integration register CC_INTEG[13:0] always stores the result of the last measurement.

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GENERAL-PURPOSE ADC

The GPADC consists of a 10-bit ADC combined with a 17-input analog multiplexer. The ADC implementation consists of a successive approximation conversion. The GPADC enables the host processor to monitor a variety of analog signals using analog-to-digital conversion on the input source. After the conversion completes, the host processor reads the results of the conversion through the I^2C interface.

The GPADC supports 17 analog inputs: 7 of these inputs are available on external balls and the remaining are dedicated to internal resource monitoring. Three of the seven external inputs are associated with current sources or reference voltages allowing measurements of resistive elements (battery type and temperature or other thermal sensor). The reference voltages are available when the GPADC is enabled. The reference voltage GPADC_REF4 can be disabled by register bit.

GPADC_IN0 is associated with a current source of 7 µA. An additional 15-µA current source can be enabled by register bit. A comparator connected to this input is intended to detect the presence or absence of the battery (resistance to ground < 130 kΩ). The detection result is available at the BATREMOVAL ball.

GPADC_IN1 and GPADC_IN4 are associated with a voltage reference equal to the ADC reference and are intended to measure temperature with an NTC sensor. In addition, a detection module is connected to GPADC_IN1 to permanently monitor the temperature and gate the charge for the battery.

The monitored internal analog parameters are:

- Main battery voltage (VBAT)
- Backup battery voltage (VBKP)
- VAC/VBUS charging source voltage
- Main battery charge current (ICHG)
- Thermal monitoring mechanisms (HOTDIE1, HOTDIE2)
- USB OTG ID voltage level

The three external inputs associated to the current sources are:

- GPADC_IN0: Main battery type detection (identification resistor in battery pack)
- GPADC_IN1: Main battery temperature measurement (thermistor in battery pack)
- GPADC_IN4: Other resistive sensor

The conversion requests are initiated by the host processor, either by software through the I^2C or by hardware through a dedicated external ball GPADC_START. This last mode is useful when real-time conversion is required. An interrupt signal is generated at the end-of-sequence of the conversions.

There are two kinds of conversion requests:

- Real-time conversion request (SRT)
- Asynchronous conversion request (SW)

Real-Time Conversion Request (SRT)

The GPADC is activated when GPADC_START is asserted. When this occurs, the GPADC digital control fetches the real-time selection register to determine which channels must be sampled and converted. A sequence of conversion consists of 1 to 17 channels to convert and processes all queued, selected channels one after another, starting with channel 0 and ending with channel 16. At the end of each conversion, the GPADC writes the conversion result into the corresponding results register. An INT interrupt is generated at the end of the sequence of conversions.

If a GPADC_START real-time request occurs while a software-initiated conversion sequence is running, the ongoing software conversion is aborted, the real-time conversion sequence is started, and a new software-initiated conversion is rescheduled at the end of the GPADC_START sequence.

Asynchronous Conversion Request (SW)

Software can also require conversions asynchronously with respect to the GPADC_START ball for general-purpose use. These conversion cases are not critical in terms of start-of-conversion positioning.

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General-purpose conversions do not require a result granularity in time lower than the duration of the all-channels conversion sequences. While requiring a general-purpose conversion, there is no need to specify channels: all channels are converted. This request is active when a write access to the toggle bit SP1 in the GPADC register occurs, and an INT interrupt is generated after the conversion sequence. A GPADC_START-initiated conversion (SRT) has a higher priority than the software-initiated conversions.

If a software request occurs while a GPADC_START-initiated sequence (SRT) is running, the software request is placed on hold and the ongoing real-time sequence continues until it completes and the converted data is stored in the real-time dedicated registers. An INT interrupt is then generated and sent to the processor. The digital control executes the software request when the real-time sequence of conversions completes. An INT interrupt is then generated.

Channels description

The different ADC channels are summarized in the following table.

CH	TYPE	POWER DOMAIN	SCALER	OPERATION
0	External	VRTC	No	Battery type, resistor value
1	External	VRTC	No	Battery temperature, NTC resistor value
2	External	Special	1.875/1.25 V	Audio accessory/general purpose
3	External	VANA	No	General purpose
4	External	VANA	No	Temperature measurement/general purpose
5	External	VANA	No	General purpose
6	External	VANA	No	General purpose
7	Internal		5/1.25 V or 6.25/1.25 V	Main battery
8	Internal		6.25/1.25 V	Backup battery
9	Internal		11.25/1.25 V	External charger input
10	Internal		6.875/1.25 V	VBUS
11	Internal		1.875/1.25 V	VBUS charging current
12	Internal		No	Die temperature
13	Internal		No	Die temperature
14	Internal		6.875/1.25 V	USB ID line
15	Internal		6.25/1.25 V	Test network
16	Internal		4.75/1.25 V	Test network

NOTE

- Channel 11 scalar (ICHG) is placed in the analog charger and always enabled.
- Channel 11 operational amplifier and path switch is located in the analog GPADC and controllable with the GPADC_SCALER_EN_CH11 register bit.
- VANA must be on to avoid leakage on GP inputs 3, 4, 5, and 6.
- It is currently not possible to measure GPADC_IN2 up to 1.25 V, without enabling the scalar first (up to 1.875 V).

The following equation provides the relationship between TWL6030 IC die junction temperature and the GPADC registers read data: $T_j(°C) = (GPADC^{10CODE} – 671) \times 0.465 + 27$

with the following parameters:

- $GPADC^{10CODE}$ is the decimal code read from the GPADC register.
- 671 is the decimal code read from the GPADC register when the junction temperature is 27°C.
- 0.465 is the linear temperature – GPADC code coefficient.

Examples:

- $T_j(–40°C) = (525-671) \times 0.465 + 27 = –40.89°C$
- $T_j(+125°C) = (878-671) \times 0.465 + 27 = 123.25°C$

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VIBRATOR DRIVER AND PWM SIGNALS

Vibrator

Instead of using the VAUX3 LDO for a generic voltage supply, it can be used as a vibrator motor driver. The output voltage of this regulator is programmable, based on a nominal 4-Hz cycle. A 16-Hz input clock is received from the clock generator (32.768-kHz crystal clock resynchronized on the RC 6-MHz clock). The output voltage level is through registers and the LDO can provide up to 200 mA.

The duty cycle of the nominal 4-Hz frequency is controlled through register and can be 25%, 50%, 75%, and 100%. This vibrator driver allows a soft turn on (500 µs maximum) and turn off (2 ms maximum).

Figure 22 shows a block diagram of the vibrator motor driver.

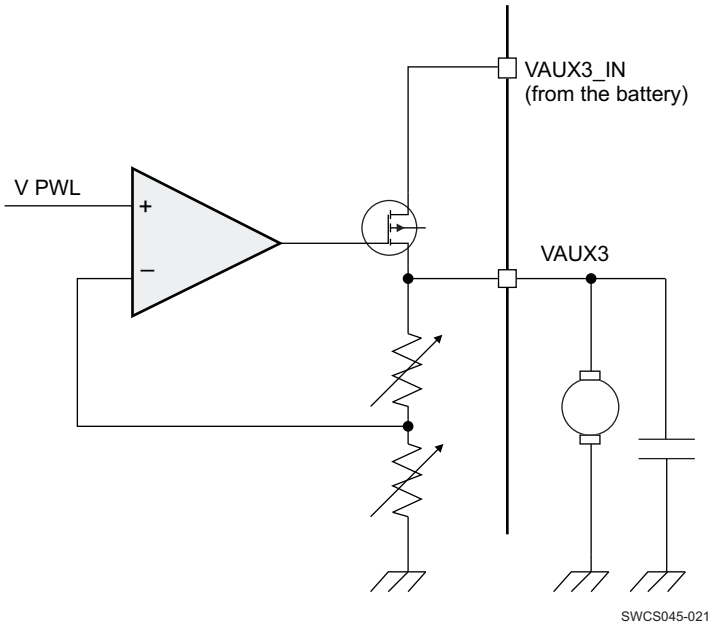

Figure 22. Block Diagram of Vibrator Motor Driver

PWMs

The PWM1 and PWM2 digital outputs provide PWM signals on the 1.8-V I/O domain. Those outputs can be active also when the system is in SLEEP state. The current drive capability of each PWM buffer is 4 mA.

Each of the PWMx ON/OFF positions is determined by the register values (PWMxON, PWMxOFF) within the range 0–127 or 0–63.

The number of clock cycles in a PWM period has two available values:

- 64 clock cycles
- 128 clock cycles

This is controlled with the PWMx_LENGTH bit in the PWMxON register.

The clock is received only when the control bit PWMxEN is set in the TOGGLE3 register. This clock enable is necessary for current saving when PWM is not used.

To get a clean OFF state (with reset on registers when PWM is disabled), first the PWMxR bit must be set and then the clock can be disabled with PWMxEN.

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NOTE

- The PWMx output signal is constantly ON by setting PWMxON[6:0] equal to PWMxOFF[6:0].
- The following conditions are prohibited:
  - PWMx_ON[6:0] > PWMx_OFF[6:0]
  - 00H ON timing setting

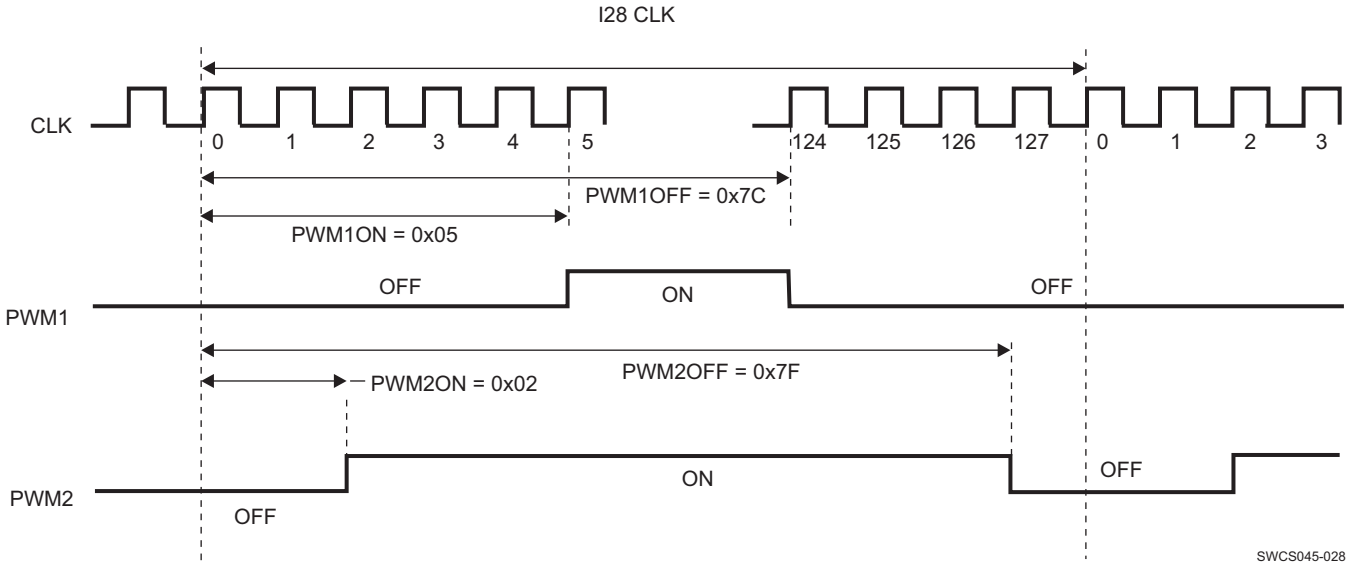

Figure 23. PWM Timings With 128 Clock Cycles Setting

When a new ON/OFF change is applied during blinking:

- If the PWM period is programmed on 64 clock cycles and changed to get 128 clock cycles, the ongoing counter goes up to 128, and the next PWM periods is 128 clock cycles.
- If the PWM period is programmed on 128 clock cycles, changed to get 64 clock cycles, and the counter is below 64, the PWM period stops at 64 clock cycles. The next periods are 64 clock cycles.
- If the PWM period is programmed on 128 clock cycles, changed to get 64 clock cycles, and the counter is above 64, the PWM period is aborted. The next periods are 64 clock cycles.

DETECTION FEATURES

The TWL6030 device supports the following detection functions:

- Detection of SIM card insertion/extraction with debouncing capability, automatic power shutdown on extraction detection (configurable)
- Detection of MMC card insertion/extraction with debouncing capability, automatic power shutdown on extraction detection (configurable)
- Detection of battery presence/removal

Cards Detection: SIM/MMC

The TWL6030 device provides the regulated supply voltage (VUSIM) for the SIM card and VMMC for the MMC card and the circuitry to detect the insertion or extraction of the SIM card or MMC card. An interrupt is generated when there is a plug/unplug detection. When the SIM card or MMC card is inserted, a mechanical contact connected to the TWL6030 device terminal SIM or MMC is tripped and after debouncing an interrupt is generated. The SIM card and MMC card presence detection logic must be active even when the system is in idle mode, and then the debouncing logic (programmable) is based on the 32-kHz low-activity clock. The signal from SIM or MMC is preprocessed depending on the detection system and on the internal pullup/pulldown

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configuration. When a card insertion is detected, the regulator VUSIM or VMMC must be enabled by software. When a card is extracted, the corresponding regulator is turned off automatically. This functionality is still configurable (enabled or disabled) by software. The SIM or MMC card plug is detected from any state of the chip (WAIT-ON, SLEEP, or ACTIVE). Both card detections are always enabled and their respective interrupt can be masked or unmasked.

Battery Removal Detection

The TWL6030 device provides the means to detect the presence or removal of the battery. The presence of the battery is detected by a comparator associated with a current source connected to the GPADC_IN0 by sensing the voltage on this ball (resistor to ground or open circuit R > 130 kΩ). The BATREMOVAL signal is activated when the presence or removal of the battery is detected. Debouncing occurs on the battery detection circuitry. This debouncing can be bypassed by a register bit (the default value is bypass). Battery detection circuitry can be enabled or disabled by a register bit. The battery detection (default configuration) can be combined with the SIM detection. Depending on the state of 2 register bits, the BATREMOVAL ball indicates the presence of the battery only, the presence of SIM only, or the presence of both SIM and battery. By default, the 2 register bits are set to indicate the battery presence only.

The polarity is defined as following:

- High level: Battery and/or SIM present
- Low level: Battery and/or SIM removed

THERMAL MONITORING

A thermal protection module monitors the temperature of the device. It generates a warning to the system when excessive power dissipation occurs and shuts down the TWL6030 device if the temperature rises to a value at which damage can occur.

Thus, there are two protection levels:

- Hot-die (HD) function, which sends an interrupt to software to close the noncritical running tasks
- Thermal shutdown (TS) function, which directly starts the TWL6030 device switch-off

The silicon technology used to build the TWL6030 device supports a maximum operating temperature of 150 °C. Regarding packaging technology, a continuous operation above 125°C would require special packaging and must be avoided to meet 100k hours lifetime.

By default, thermal protection is always enabled except in BACKUP or OFF state. It is not possible to disable it by software in the SLEEP state.

The TWL6030 device integrates two hardware detection mechanisms to monitor and alert software that the junction temperature is rising and must take action to reduce consumption. Those mechanisms are placed on two opposite sides of the chip and close to the LDOs and SMPSs. Even if there are two identical thermal feature instances on the chip, it is always considered by the specification to be unique. In addition to those HD detections, another HD feature is embedded in the charger: The charger HD is specified in BATTERY CHARGING and does not behave exactly the same way as described in Hot-Die Function.

Different thresholds are implemented. When a threshold is reached, an interrupt is issued. To avoid parasitic interrupt, debouncing is implemented within the HD detection function.

The TWL6030 device integrates a thermal shutdown mechanism to shut down the device when the junction temperature reaches a certain level to avoid irreversible die damage. The rising and falling temperature thresholds have a difference of 10°C minimum. The HD provides some interrupt mechanism and threshold registers to select the temperature interrupt level.

Hot-Die Function

The HD detector monitors the temperature of the die and provides a warning to the host processor through the interrupt system when temperature reaches a critical value. The threshold value must be set below the thermal shutdown threshold. Hysteresis is added to the HD detection to avoid the generation of multiple interrupts.

The integrated HD function provides an early warning overtemperature condition to the host PM software. This monitoring system is connected to the interrupt controller (INTC) and can send an interrupt when the temperature is higher than the programmed threshold.

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The TWL6030 device allows the programming of four junction-temperature thresholds to increase the flexibility of the system: in nominal conditions, the threshold triggering the interrupt can be set from 117°C to 130°C. The HD hysteresis is 10°C minimum in typical conditions.

When an interrupt is triggered by the power-management software, immediate action must be taken to reduce the amount of power drawn from the TWL6030 device (for example, noncritical applications must be closed).

The interrupt generation is debounced to avoid parasitic interrupt.

Thermal Shutdown

The thermal shutdown detector monitors the temperature on the die. If the junction reaches a temperature at which damage can occur, a switch-off transition is initiated and a thermal shutdown event is written into a status register.

To avoid interrupts at restart, the system cannot be restarted until the die temperature falls below the HD threshold.

The thermal shutdown monitor function is integrated to generate an immediate, unconditional TWL6030 device switch-off when an overtemperature condition exists. This function must be distinguished with the early warning provided to software by the HD monitor function.

In the TWL6030 device, the threshold (T_j rising) of the thermal shutdown is 148°C nominal. The thermal shutdown hysteresis is 10°C in typical conditions. The reset generation is debounced. The thermal shutdown function can be masked only in SLEEP state (the TMP_CFG_TRANS register) and in test mode.

CONTROL INTERFACE (I^2C , MSECURE, INTERRUPTS)

I^2C interfaces

The TWL6030 device provides two serial control interfaces: One is the general-purpose I^2C interface (CTL-I2C) for read-and-write access to the configuration registers of all system resources, and the other is the serial control interface (SR-I2C) dedicated to SmartReflex applications, such as dynamic voltage frequency scaling (DVFS) or adaptive voltage scaling (AVS).

Both control interfaces comply with the HS-I2C specification and support the following features:

- Mode: Slave only (receiver and transmitter)
- Speed
  - Standard mode (100 kbps)
  - Fast mode (400 kbps)
  - High-speed mode (limited to 2.4 Mbps maximum)
- Addressing: 7-bit mode addressing device

They do not support the following features:

- 10-bit addressing
- General call

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Single-Byte Access

A write access is initiated by a first byte that includes the address of the device (7 MSBs) and a write command (LSB), a second byte that provides the address (8 bits) of the internal register, and the third byte that represents the data to be written in the internal register.

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the address (8 bits) of the internal register
- A third byte, including again the address of the device (7 MSBs) and the read command (LSB)

The device replies by sending a fourth byte representing the content of the internal register.

Figure 24 shows a write access single-byte timing diagram.

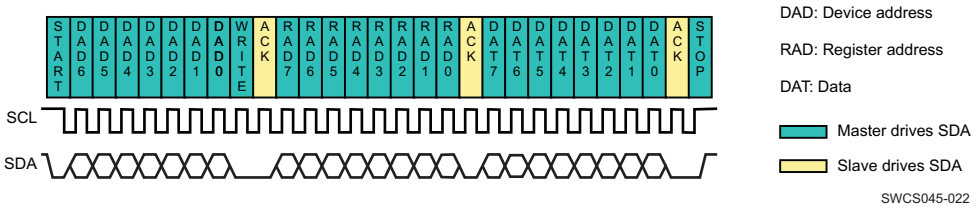

Figure 24. I²C Write Access Single Byte

Figure 25 shows a read access single-byte timing diagram.

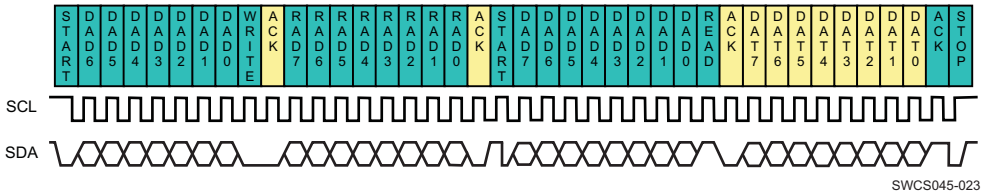

Figure 25. I²C Read Access Single Byte

Multiple-Byte Access to Several Adjacent Registers

A write access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal registers

The following N bytes represent the data to be written in the internal register, starting at the base address and incremented by one at each data byte.

Figure 26 shows a multiple-byte write access.

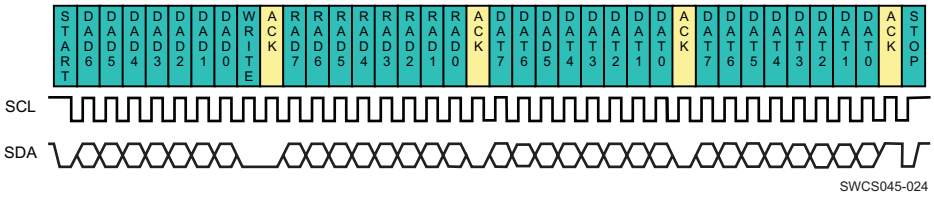

Figure 26. I²CWrite Access Multiple Bytes

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal register
- A third byte, including again the address of the device (7 MSBs) and the read command (LSB)

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The device replies by sending a fourth byte representing the content of the internal registers, starting at the base address and next consecutive ones.

Figure 27 shows a multiple-byte read access.

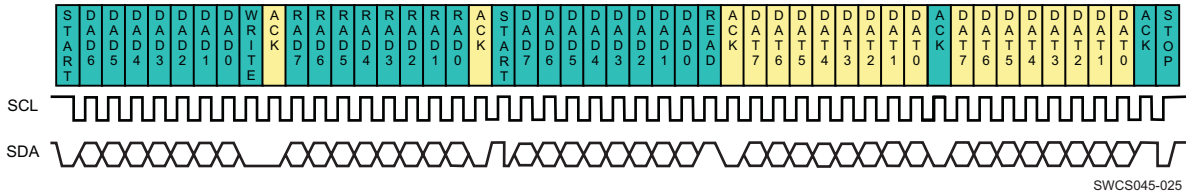

Figure 27. I²C Read Access Multiple Bytes

Secure Registers

Some registers of the TWL6030 device can be protected by restricting their access in write mode to software running in the secure mode of the host read access to protected registers. Secure access is enabled or disabled by the MSECURE control signal.

The following components or actions can be protected:

- All RTC registers
- 64 bits of general-purpose memory (8 x 8) in the backup domain named VALIDITY

The read accesses are independent to the MSECURE value.

When MSECURE is logical level 1, all read and write accesses are authorized; when MSECURE is logical level 0, only read accesses are authorized.

This security feature (MSECURE detection) is enabled and disabled by an EPROM bit.

Interrupts

The INT signal (active low) warns the host processor of any event occurring on the TWL6030 device. The host processor then pools the interrupt from the interrupt status register through I²C to identify the interrupt source. Each interrupt source can be individually masked through the interrupt mask line registers and mask status registers.

If interrupts occur while the status registers are not cleared, the status registers are not updated immediately. Instead, the interrupts are held pending in a second stage of shadow registers, waiting for all previous interrupts to be cleared first. When the interrupt line goes low again, operated just after the first set of interrupts clear, all status registers are updated with those pending interrupt sources, coming directly from the shadow registers.

To clear both interrupts and register status, a write in the status registers must be done. Each write has the same effect (interrupt line goes high and all status registers are cleared). This implies that the interrupt subroutine acquires the three status registers before acknowledging the interrupt to avoid losing any interrupt sources.

NOTE

- An interrupt associated with a function should be masked before enabling or disabling the feature; otherwise, it might generate a false interrupt directly linked to the state change of the feature and not related to an external detection event (for example, BAT_VLOW interrupt with VBATMIN_HI comparator).
- INT is always active low.
- When a TWL6030 interrupt occurs:
  - Software should first read all status registers, INT_STS_A, INT_STS_B, and INT_STS_C.
  - Execute the subroutines related to the read interrupts.
  - Clear the interrupt status of all status registers

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Table 18. Interrupt mapping

#	REG	BIT	SECTION	INTERRUPT	DESCRIPTION
00	A	0	PM	PWRON	PWRON detection: Power-on button pressed and released. Detection performed on falling and rising edges. Interrupt sent in SLEEP or ACTIVE only, not in WAIT-ON.
01	A	1	PM	RPWRON	RPWRON detection: Remote power-on signal change. Interrupt sent in SLEEP or ACTIVE only, not in WAIT-ON.
02	A	2	PM	BAT_VLOW	Battery voltage low: Battery voltage decreasing and crossing VBATMIN_HI
03	A	3	RTC	RTC_ALARM	RTC alarm event: Occurs at programmed determinate date and time
04	A	4	RTC	RTC_PERIOD	RTC periodic event: Occurs at programmed regular period of time (every second or minute)
05	A	5	Thermal monitoring and shutdown	HOT_DIE	At least one of the two embedded thermal monitoring modules detects a die temperature above the HD detection threshold.
06	A	6	SMPS/LDO	VXXX_SHORT	At least one of the following power resources has its output shorted: V1V29, V1V8, V2V1, VCORE1, VCORE2, VCORE3, VMEM, VANA, VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VPP, VUSB
07	A	7	LDO	VMMC_SHORT	VMMC power resource has its output shorted.
08	B	0	LDO	VUSIM_SHORT	VUSIM power resource has its output shorted.
09	B	1	Detection	BAT	Battery detection plug/unplug
10	B	2	Detection	SIM	SIM card plug/unplug
11	B	3	Detection	MMC	MMC card plug/unplug
12	B	4			Reserved
13	B	5	GPADC	GPADC_RT_SW1_EOC	End of conversion: Completion of a real time and a GP software 1 (SW1) conversion cycle; result available
14	B	6	GPADC	GPADC_SW2_EOC	End of conversion: Completion of a GP software 2 (SW2) conversion cycle; result available
15	B	7	Gas gauge	CC_AUTOCAL	Calibration procedure finished and the result is available in the register.
16	C	0	OTG	ID_WKUP	ID wake-up event (from WAIT-ON/SLEEP states)
17	C	1	OTG	VBUS_WKUP	VBUS wake-up event (from WAIT-ON/SLEEP states)
18	C	2	OTG	ID	ID event detection in SLEEP/ACTIVE states
19	C	3	OTG	VBUS	VBUS event detection in SLEEP/ACTIVE states
20	C	4	Charger	CHRG_CTRL	Charger controller Interrupt source can be: • Charger plug insertion and removal detection: – VAC_PLUG – VBUS_PLUG • Watchdogs 32mn / 32s interrupts: – FAULT_WDG • Battery interrupts: – BAT_REMOVED – BAT_TEMP_OVRANGE
21	C	5	Charger	EXT_CHRG	External charger fault(CHRG_EXTCHRG_STATZ)
22	C	6	Charger	INT_CHRG	Internal USB charger fault Interrupt source can be: • CHARGERUSB_FAULT • CHARGERUSB_THMREG • CHARGERUSB_STAT • CURRENT_TERM
23	C	7			Reserved

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Default boot sequences

TWL6030B107 boot sequence

This device is OMAP4430 companion chip.

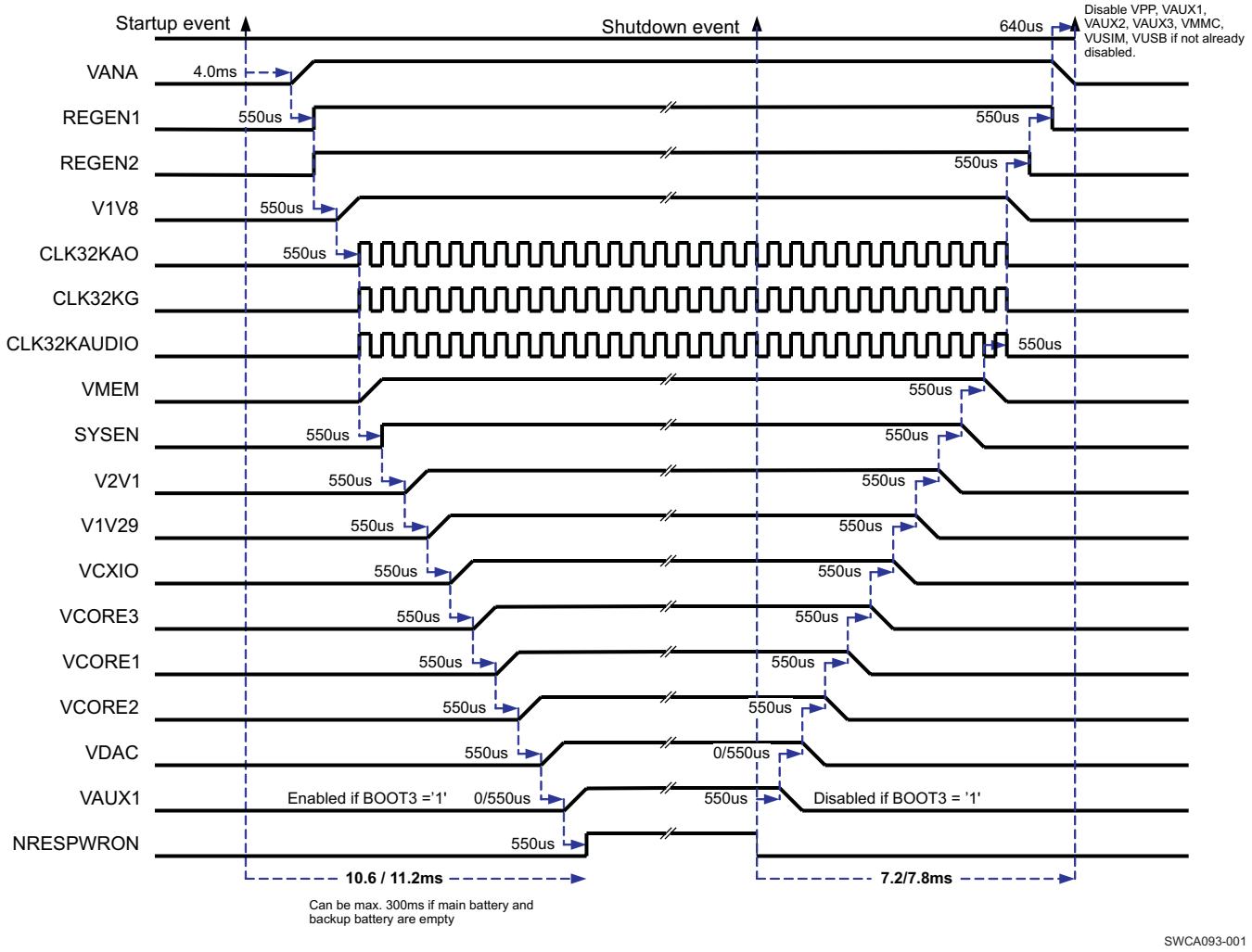

Figure 28. OMAP4430 Default Start-up and Shut-down Sequences

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TWL6030B1A4 boot sequence

This device is OMAP4460 companion chip.

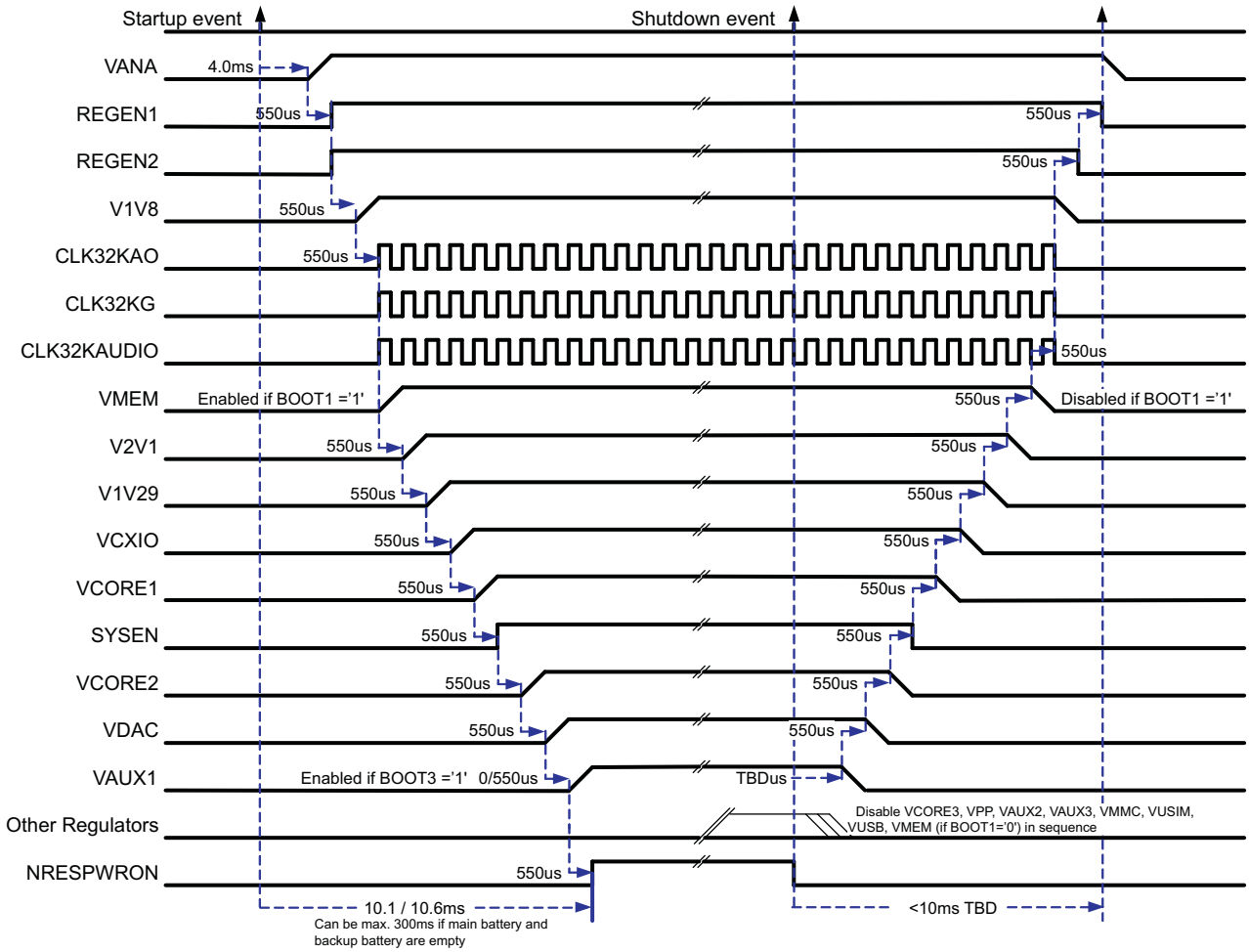

Figure 29. OMAP4460 Default Start-up and Shut-down Sequences

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RECOMMENDED EXTERNAL COMPONENTS

MODULE	COMPONENT(1)	#(2)	MANUFACTURER	PART NUMBER	VALUE	PACK(3)	SIZE (mm)
INPUT POWER SUPPLIES EXTERNAL COMPONENTS							
PM/VBAT	VDD tank capacitor(4)	1	Murata	GRM188R60J106ME84L	10 µF	603	1.6 x 0.8 x 0.8
PM/VBAT	VDD tank capacitor(4)	2	Taiyoyuden	JMK107BJ106	10 µF	603	1.6 x 0.8 x 0.8
Backup	Capacitor	1	Seiko Instruments	XH414H-IV01E	0.08 F		ø4.8, 1.4
Backup	Capacitor	2	Matsushita (MEC)	EECEP0E223AN	0.022 F		
CRYSTAL OSCILLATOR EXTERNAL COMPONENTS							
32 kHz	Crystal	1	Citizen	CM519	32.768 kHz		3.2 x 1.5 x 0.9
32 kHz	Crystal	2	Microcrystal	CC7V-T1A	32.768 kHz		
32 kHz	Crystal	3	Epson	FC135	32.768 kHz		
32 kHz	Crystal	4	NDK	NX3215SA	32.768 kHz		3.2 x 1.5 x 0.8
32 kHz	Supply decoupling	1	Murata	GRM155R61A105KE15D	1 µF	402	1 x 0.5 x 0.5
32 kHz	Supply decoupling	2	Taiyoyuden	JMK105BJ105MV-F	1 µF	402	1 x 0.5 x 0.5
32 kHz	Crystal decoupling	1	Murata	GRM1555C1H220JZ01	22 pF	402	1 x 0.5 x 0.5
32 kHz	Crystal decoupling	2	AVX	04025A120JAT2A	12 pF	402	1 x 0.5 x 0.5
BANDGAP EXTERNAL COMPONENTS							
Bandgap	Bias resistor	1	Rohm	0W06 1M 50ppm	1 MΩ	402	1 x 0.5 x 0.5
Bandgap	Bias resistor	2	Vishay		1 MΩ	603	1.6 x 0.8 x 0.8
Bandgap	Capacitor	1	Murata	GRM155R61C104K	100 nF	402	1 x 0.5 x 0.5
Bandgap	Capacitor	2	KEMET	C0402C104K8PAC	100 nF	402	1 x 0.5 x 0.5
GAS GAUGE EXTERNAL COMPONENTS							
Gas Gauge	Resistor	1	Cyntec	RL3720T-R010-FN	10 mΩ	815	
GPADC EXTERNAL COMPONENTS							
GPADC	NTC resistor	1	Murata	NCL15WB473F03RC	47 kΩ	402	1 x 0.5 x 0.5
I^2C EXTERNAL COMPONENTS							
I^2C interface	Pullup resistor	1					
SMPS EXTERNAL COMPONENTS							
SMPS	Input capacitor	1	Murata	GRM155R60J225ME15D	2.2 µF	402	1 x 0.5 x 0.5
SMPS	Input capacitor	2	Taiyoyuden	JMK105BJ225MV-F	2.2 µF	402	1 x 0.5 x 0.5
SMPS	Input capacitor	3	Murata	GRM155R60J475M	4.7 µF	402	1 x 0.5 x 0.5
SMPS	Input capacitor	4	Taiyoyuden	JMK107BJ475KA-T	4.7 µF	603	1.6 x 0.8 x 0.8
SMPS	Input capacitor	5	Murata	GRM155R60J335UE97	4.7 µF	402	1 x 0.5 x 0.5
SMPS	Output capacitor	1	Murata	GRM188R60J106ME84L	10 µF	603	1.6 x 0.8 x 0.8
SMPS	Output capacitor	2	Murata	GRM188R60J106UE82J	10 µF	603	1.6 x 0.8 x 0.8
SMPS	Ferrite bead	1	Murata	BLM18SG700TN1D	–	603	1.6 x 0.8 x 0.8
SMPS	Ferrite bead	2	Murata	BLM15PD121SN1	1300 mA	402	1 x 0.5 x 0.5
SMPS	Ferrite bead	3	Murata	BLM18KG221SN1	2200 mA	603	1.6 x 0.8 x 0.8
SMPS 0.8 A	Filter inductor (volume minimization)	1	Murata	LQM21PN1R0MC0	1 µH	805	2 x 1.25 x 0.55
SMPS 0.8 A	Filter inductor (performance maximization)	2	TDK	MLP2520S1R0M	1 µH	1008	2.5 x 2 x 1

(1) Component minimum and maximum tolerance values are provided in the electrical parameters section for each IP.
(2) The # column refers to the first (1), second (2), and third (3) source suppliers, for which the IPs are either simulated or characterized.
(3) The PACK column describes the external component package type.
(4) The VDD tank capacitors filter the VBAT/VDD_B [i] input voltage of the LDO and SMPS core architectures.

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SMPS 1.0 A, 1.2 A	Filter inductor (volume minimization)	1	Murata	LQM2MPN1R0NG0	1 µH	806	2 x 1.6 x 1
SMPS 1.2 A, 1.5 A, 2 A	Filter inductor (performance maximization)	1	Murata	LQM32PN1R0MG0	1 µH	1210	3.2 x 2.5 x 1
SMPS 1.2 A, 1.5 A, 2 A	Filter inductor (performance maximization)	2	TOKO	DFE322512C H1R0N (under development)	1 µH	1210	3.2 x 2.5 x 1.2
SMPS 1.2 A, 1.5 A, 2 A	Filter inductor (volume minimization)	3	TOKO	DFE252012C H1R0N (under development)	1 µH	1008	2.5 x 2 x 1.2
SMPS 2 A	Filter inductor (volume minimization)	1	Coilcraft	EPL2010-681MLB	0.68 µH		2 x 2 x 1
LDO EXTERNAL COMPONENTS							
LDO	Input capacitor	1	Murata	GRM155R60J105KE19D	1 µF	402	1 x 0.5 x 0.5
LDO	Input capacitor	2	Taiyoyuden	JMK105BJ105MV-F	1 µF	402	1 x 0.5 x 0.5
LDO	Input capacitor	3	KEMET	C0402C105K9PAC7867	1 µF	402	1 x 0.5 x 0.5
LDO	Output capacitor	1	Murata	GRM155R60J105KE19D	1 µF	402	1 x 0.5 x 0.5
LDO	Output capacitor	2	Taiyoyuden	JMK105BJ105MV-F	1 µF	402	1 x 0.5 x 0.5
LDO	Output capacitor	3	KEMET	C0402C105K9PAC7867	1 µF	402	1 x 0.5 x 0.5
LDO	Output capacitor	4	Murata	GRM155R60J155ME80D	2.2 µF	402	1 x 0.5 x 0.5
CHARGER EXTERNAL COMPONENTS							
Charger	Filter inductor	1	FDK	MIPS2520D1R0	1 µH	2520	
Charger	Filter inductor	2	Taiyoyuden	CKP25201R0M-T	1 µH	2520	
Charger	Filter inductor	3	Taiyoyuden	CKP2520D1R0	1 µH	2520	
Charger	Sense resistor	1	Panasonic	ERJ2BWFR068X	68 mΩ	402	1 x 0.5 x 0.5
Charger	Sense resistor	2	Rohm	UCR01	68 mΩ	402	1 x 0.5 x 0.37
Charger	Sense resistor	3	Tyco Electronics	219-908	68 mΩ	2512	
Charger	CHRG_VREF capacitor	1	KEMET	C0603C225K4PAC	2.2 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_VREF capacitor	2	Murata	GRM188R61C225UAAG	2.2 µF	603	1.6 x 0.8 x 0.8
Charger	VAC decoupling	1	Murata	GRM155R61C104K	100 nF	402	1 x 0.5 x 0.5
Charger	VAC decoupling	2	Taiyoyuden	LMK105BJ104MV-F	100 nF	402	1 x 0.5 x 0.5
Charger	VBUS decoupling	1	Murata	GRM155R60J475M	4.7 µF	402	1 x 0.5 x 0.5
Charger	VBUS decoupling	2	Taiyoyuden	JMK107BJ475KA-T	4.7 µF	603	1.6 x 0.8 x 0.8
Charger	VBUS decoupling	3	Panasonic	ECJINB1C475M	4.7 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_PMID capacitor	1	Murata	GRM155R60J475M	4.7 µF	402	1 x 0.5 x 0.5
Charger	CHRG_PMID capacitor	2	Taiyoyuden	JMK107BJ475KA-T	4.7 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_PMID capacitor	3	Panasonic	ECJINB1C475M	4.7 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_CSIN capacitor	1	Murata	GRM155R61C104K	100 nF	402	1 x 0.5 x 0.5
Charger	CHRG_CSIN capacitor	2	Taiyoyuden	LMK105BJ104MV-F	100 nF	402	1 x 0.5 x 0.5
Charger	CHRG_CSOUT	1	Murata	GRM188R60J106ME84L	10 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_CSOUT	2	Taiyoyuden	JMK107BJ106	10 µF	603	1.6 x 0.8 x 0.8
Charger	CHRG_SW capacitor	1	Murata	GRM155R61C103KA01D	10 nF	402	1 x 0.5 x 0.5
Charger	CHRG_SW capacitor	2	Taiyoyuden	TMK105BJ103MV	10 nF	402	1 x 0.5 x 0.5
Charger	CHRG_AUXPWR	1	Murata	GRM155R61A105KE15D	1 µF	402	1 x 0.5 x 0.5

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Charger	CHRG_AUXPWR	2	Taiyoyuden	JMK105BJ105MV-F	1 µF	402	1 x 0.5 x 0.5
Charger	CHRG_AUXPWR	3	KEMET	C0402C105K9PAC7867	1 µF	402	1 x 0.5 x 0.5
Charger	LED	1	Osram	LYL296	–		
Charger	LED	2	Everlight	16S-216UTD/S559/TR8	2 mA	402	1 x 0.5 x 0.35
Charger	CHRG_BOOT	1	Murata	GRM188R71H103KA01D	10 nF	603	1.6 x 0.8 x 0.8

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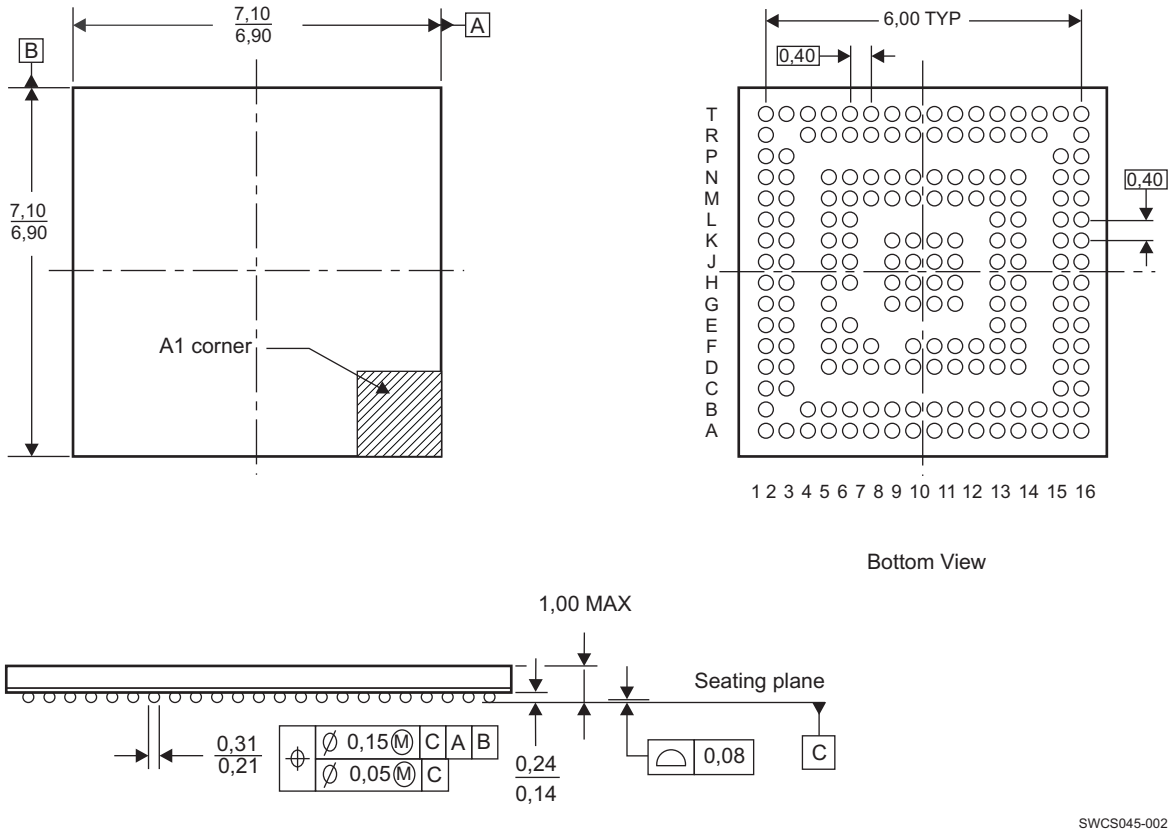
PACKAGE MATERIALS INFORMATION

PACKAGE CHARACTERISTICS

The package description of the TWL6030 PMU device is presented as follows:

PACKAGE (1)	TWL6030
Type	nFBGA
Size (mm)	7 x 7
Substrate layers	2-layer
Pitch ball array (mm)	0.4 mm
ViP (via-in-pad)	No
Array grid	16 x 16, depopulated
Number of balls	187
Thickness (mm; maximum height, including balls)	1.0 mm
Maximum power dissipation (85°C ambient temperature)	1.7 W
Others	Green, ROHS compliant

(1) Moisture Sensitivity Level Target: JEDEC MSL3 @ 260°C



The thermal resistance characteristics for the package used on the TWL6030 device is given in the following table.

PACKAGE	POWER (W)	$R_{\Theta JA}$ (°C/W)	$R_{\Theta JB}$ (°C/W)	$R_{\Theta JC}$ (°C/W)	BOARD TYPE
nFBGA, 7mm x 7mm	1.7	31	19	12	1S2P

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TAPE AND REEL INFORMATION

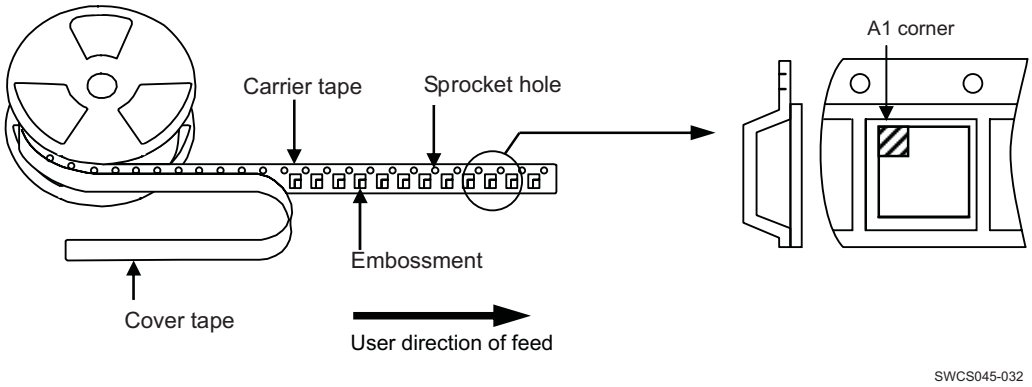

Figure 30. Tape and Reel

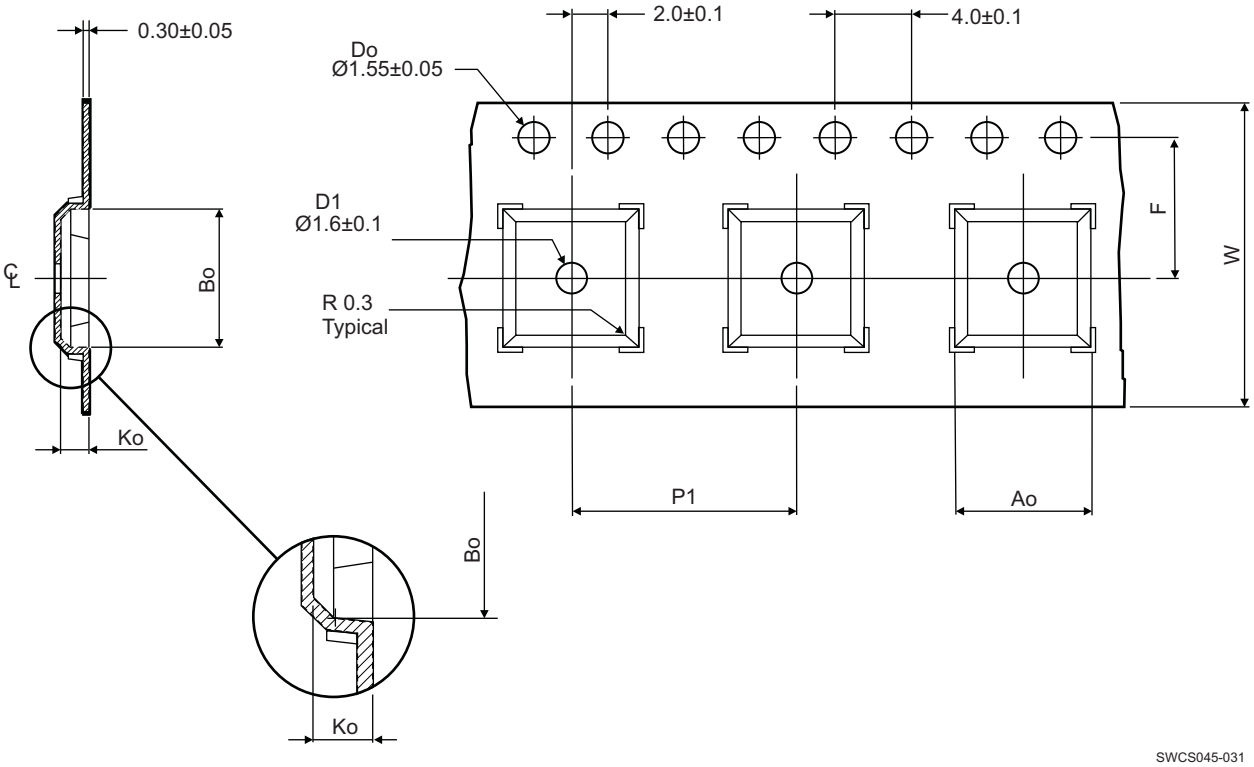

Figure 31. Tape

Table 19. Tape Dimensions

A0	B0	K0 ±0.1	F	P1	W ±0.3
7.30	7.30	1.50	7.50	12.00	16.00

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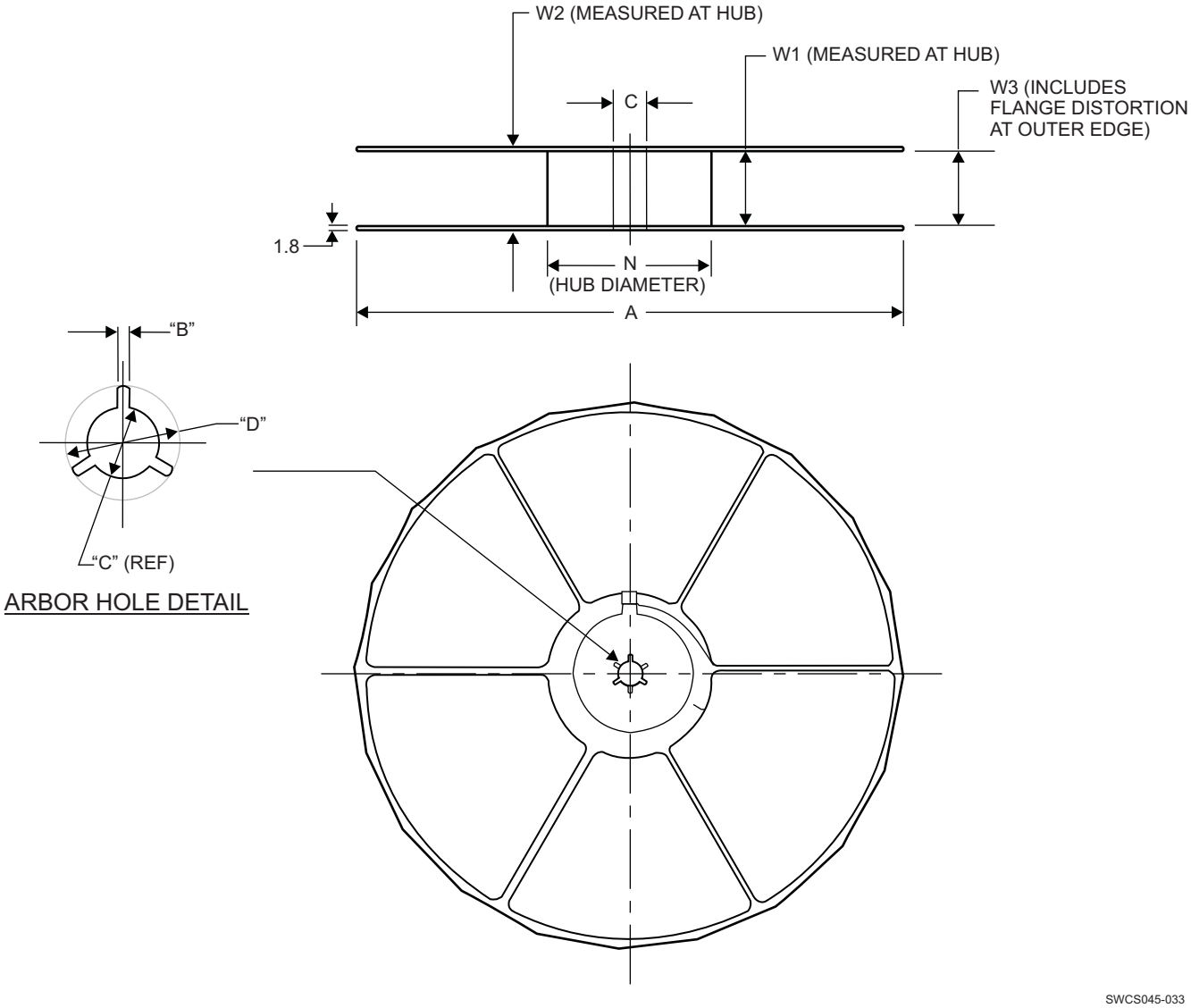

Figure 32. Reel Dimensions

Table 20. Reel Dimensions

Material type	ESD type	Tape size	Hub size	Material color	A(max)	B(±0.5)	C(±0.20)	D(min)	N	W1(+2.0/ -0.0)	W2(max)	W3(min/ max)
PS	ASD	16.0	4"	Black	330	2.0	13.0	20.8	100 ±1.0	18.4	22.4	15.9/19.4

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Revision History

The following table summarizes the *TWL6030 Data Sheet* versions.

Note: Numbering may vary from previous verisons.

Table 21. Revision History

Version	Literature Number	Date	Notes
*	SWCS045	December 2009	See (1).
A	SWCS045A	April 2011	See (2).
B	SWCS045B	June 2011	See (3).
C	SWCS045C	July2011	See (4).

(1) *TWL6030 Data Sheet*, (SWCS045) - initial release.
(2) *TWL6030 Data Sheet*, (SWCS045A):
  (a) Added Figure 1, *TWL6030 Block Diagram*, Table 2, *Ball Description*, FEATURES, and APPLICATIONS.
  (b) Updated ELECTRICAL CHARACTERISTICS, PACKAGE MATERIALS INFORMATION, and Figure 2, *TWL6030 Package Top View Ball Mapping*.
  (c) Updated RECOMMENDED EXTERNAL COMPONENTS.
  (d) Updated part numbers, Table 1, *Ordering Information*.
  (e) Rewrite of all functional blocks.
  (f) Updated figures.
(3) *TWL6030 Data Sheet*, (SWCS045B):
  (a) Updated part numbers, Table 1, *Ordering Information*.
  (b) Updated Figure 1, *TWL6030 Block Diagram*
  (c) Updated balls N15, K13, B7 name from SPARE to RESERVED.
  (d) Updated LDO REGULATORS description.
  (e) Updated Subsystem Hardware Commands description.
  (f) Updated Warmreset description.
  (g) Updated Table 12, *BOOT[3:0]*.
  (h) Updated Figure 11. Q1,Q2, and Q3 transistors name added.
  (i) Updated list of GPADC internal monitored parameters in GENERAL-PURPOSE ADC.
  (j) Updated Interrupts functionality description.
  (k) Updated Table 18, *Interrupt mapping*.
  (l) Updated ID Line, added Figure 16 and Table 17.
(4) *TWL6030 Data Sheet*, (SWCS045C):
  (a) Remove Pull down on NRESWARM in Table 2
  (b) Updated SMPS output voltage Equation 1
  (c) Added Default boot sequences section
  (d) Remove prototype mark for TWL6030B1A4 in Table 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TWL6030B107CMR	NRND	FCCSP	CMR	187	260	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	6030B107	
TWL6030B107CMRR	NRND	FCCSP	CMR	187	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	6030B107	
TWL6030B1A0CMR	NRND	FCCSP	CMR	187	260	RoHS & Green	SNAGCU	Level-3-260C-168 HR		6030B1A0	
TWL6030B1A0CMRR	NRND	FCCSP	CMR	187	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR		6030B1A0	
TWL6030B1A4CMR	NRND	FCCSP	CMR	187	260	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	6030B1A4	
TWL6030B1A4CMRR	NRND	FCCSP	CMR	187	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	6030B1A4	
TWL6030B1AACMR	NRND	FCCSP	CMR	187	260	RoHS & Green	Call TI	Level-3-260C-168 HR		6030B1AA	
TWL6030B1AACMRR	LIFEBUY	FCCSP	CMR	187	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		6030B1AA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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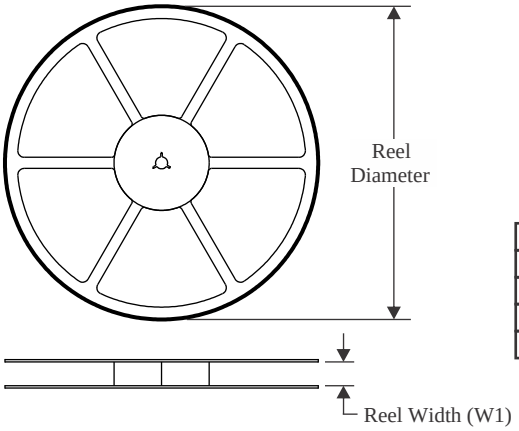
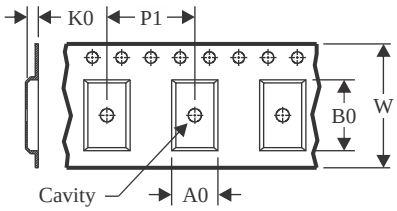
TAPE AND REEL INFORMATION

REEL DIMENSIONS

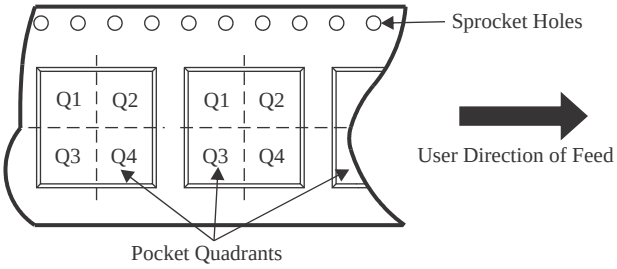


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

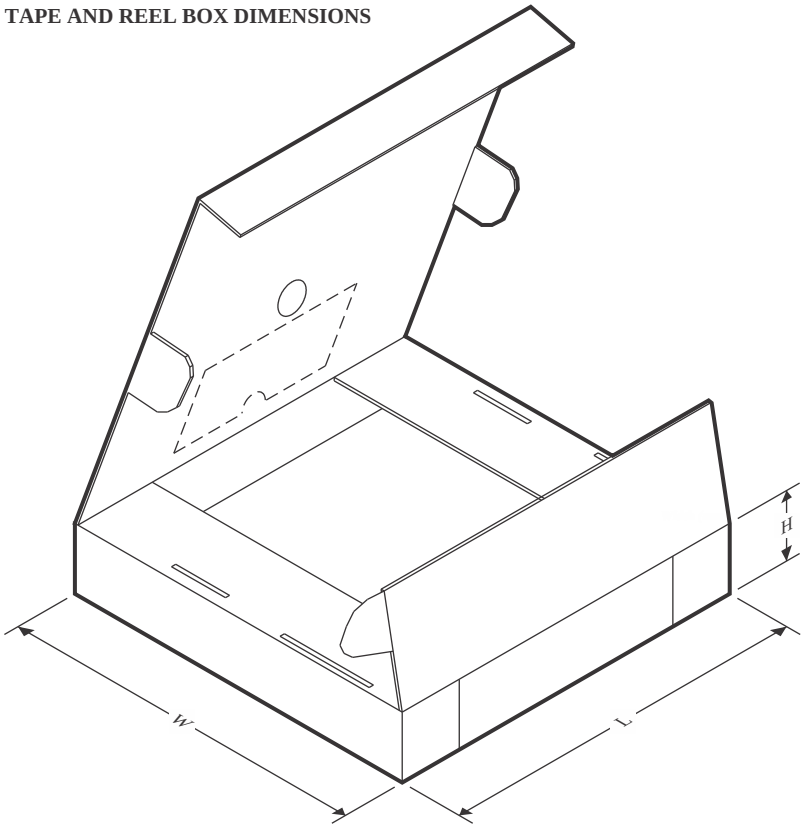
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TWL6030B107CMRR	FCCSP	CMR	187	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TWL6030B1A0CMRR	FCCSP	CMR	187	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TWL6030B1A4CMRR	FCCSP	CMR	187	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TWL6030B1AACMRR	FCCSP	CMR	187	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

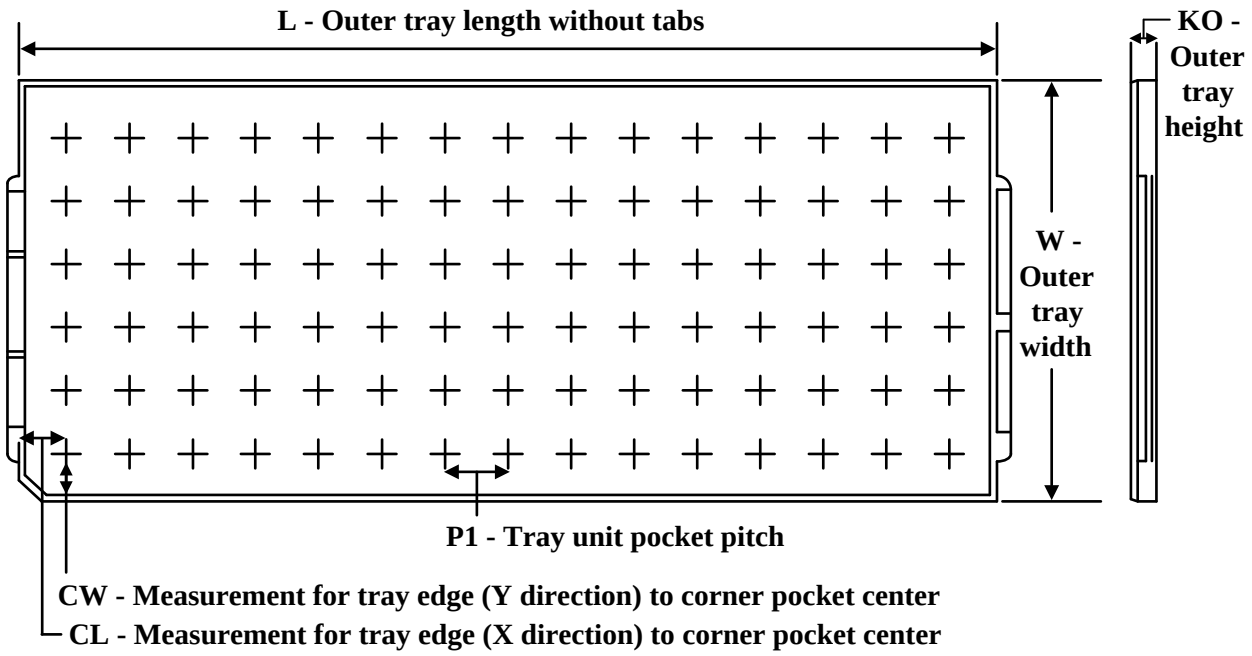
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TWL6030B107CMRR	FCCSP	CMR	187	2500	336.6	336.6	31.8
TWL6030B1A0CMRR	FCCSP	CMR	187	2500	336.6	336.6	31.8
TWL6030B1A4CMRR	FCCSP	CMR	187	2500	336.6	336.6	31.8
TWL6030B1AACMRR	FCCSP	CMR	187	2500	336.6	336.6	31.8

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TWL6030B107CMR	CMR	FCCSP	187	260	10 x 26	150	315	135.9	7620	11.8	10	10.35
TWL6030B1A0CMR	CMR	FCCSP	187	260	10 x 26	150	315	135.9	7620	11.8	10	10.35
TWL6030B1A4CMR	CMR	FCCSP	187	260	10 x 26	150	315	135.9	7620	11.8	10	10.35
TWL6030B1AACMR	CMR	FCCSP	187	260	10 x 26	150	315	135.9	7620	11.8	10	10.35

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