



Interface thermal characteristics of flip chip packages – A numerical study

Ravi Kandasamy^{a,*}, A.S. Mujumdar^b

^a ASIC Products Division, Avago Technologies Singapore, 1 Yishun Avenue 7, Singapore 768923

^b Minerals, Metals and Materials, Technology Centre and Department of Mechanical Engineering, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, Singapore

ARTICLE INFO

Article history:

Received 24 July 2007

Accepted 8 April 2008

Available online 16 April 2008

Keywords:

Interface thermal resistance

Numerical simulation

Flip chip BGA

Thermal interface Materials

Effect of voids

ABSTRACT

Flip chip ball grid array (FC-BGA) packages are commonly used for high inputs/outputs (I/O) ICs; they have been proven to provide good solutions for a variety of applications to maximize thermal and electrical performance. A fundamental limitation to such devices is the thermal resistance at the top of the package, which is characterized θ_{JC} parameter. The die-to-lid interface thermal resistance is identified as a critical issue for the thermal management of electronic packages. This paper focuses on the effect of the interface material property changes on the interface thermal resistance. The effect of package's junction to case (Theta-JC or θ_{JC}) thermal performance is investigated for bare die, flat lid and cup lid packages using a validated thermal model. Thermal performance of a cup or flat lid attached and bare die packages were investigated for different interface materials. Improved Theta-JC performance was observed for the large die as compared to the smaller die. Several parametric studies were carried out to understand the effects of interface bond line thickness (BLT), different die sizes, the average void size during assembly and thermal conductivity of interface materials on package thermal resistance.

© 2008 Elsevier Ltd. All rights reserved.

1. Introduction

Control of component temperatures and temperature gradients is essential for successful operation and reliability of electronic products [1]. The current trend of increasing heat fluxes combined with smaller dimensions leads to the development of higher local temperatures. Increasing the chip power densities to 100 W/cm² and higher is the key driving force for the need to develop highly conductive interface materials and packages with reduced bond line thicknesses. The International Technology Roadmap for Semiconductors (ITRS) predicts that this trend will continue in the future [2]. Indeed, thermal issues threaten to limit the electrical performance; hence package-level thermal management has become a primary concern for an active die. Flip chip packages are commonly used because of their improved electrical and thermal performance. These packages are primarily used in high performance microprocessors, digital signal processors, networks and data storage applications [3]. As power dissipation increases, it is essential that the packages housing the chips have highly reliable thermal and electrical characteristics to achieve optimum device performance. In high performance applications, flip chip packages are constructed using different types of materials, e.g. substrate either as laminate or ceramic with many metallization layers, lid, die and heat spreader as shown in Fig. 1.

Typically, FC-BGA packages have two different interfacial materials in the heat flow path; one is between die-to-lid (TIM I) followed by a thermal interfacial material between the lid and the heat sink (TIM II), or between the die back side and the heat sink (typically termed as TIM II). Lee [4], de Sorgo [5], and Latham [6] have discussed thermal resistances at interfaces between heat sinks and packages. These articles report primarily on their test results for the combined resistance as a function of contact pressure for various interface types. Their work involves bare die surfaces (air filled) as well as joints where the interstitial gap is filled with a material layer containing thermally conductive fillers. As noted by de Sorgo [5], these fillers include thermal greases, thermally conductive compounds, elastomers, and adhesive tapes. There are several types of interface materials in the market today [7,8] with various thermal conductivities and bond-line thicknesses, such as thermal adhesives, greases, phase change materials (PCMs) and thermal pads. Advantages of thermal pastes include low cost, ease of assembly and re-workability. Among the disadvantages of the thermal pastes are: large thermal resistance and the susceptibility for voiding and drying out [9]. The temperature drop at contact surfaces is much larger than that across the TIM due to imperfections in the wetting of the contact surfaces by the TIM [10]. Prasher et al. [11] have discussed novel models to improve the understanding of the effects of surface chemistry by particle loading and the reduced contact resistance between the interface material and the surfaces. Thermal interface materials play a major role as they account for almost 20–50% of the total thermal budget [12], i.e. they represent major thermal resistance in flip chip packages.

* Corresponding author. Tel.: +65 6215 3049; fax: +65 6215 3767.

E-mail address: ravi.kandasamy@avagotech.com (R. Kandasamy).

Nomenclature

TIM-I	thermal interface material used between die and lid	Theta-JB (θ_{JB})	package junction to board thermal resistance ($^{\circ}\text{C}/\text{W}$)
TIM-II	thermal interface material used between lids to heat sinks or dies to heat sink	Theta-JA (θ_{JA})	package junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
FC-BGA	flip chip ball grid array	Theta-CS (θ_{CS})	package case to sink thermal resistance ($^{\circ}\text{C}/\text{W}$)
I/O	inputs/outputs	Theta-SA (θ_{SA})	package sink to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
ICs	integrated circuits	T_J	junction temperature ($^{\circ}\text{C}$)
BLT	bond line thickness (μm)	T_A	ambient temperature ($^{\circ}\text{C}$)
Theta-JC (θ_{JC})	package junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)	P	power dissipation (W)

The total interfacial thermal resistances can be improved by increasing the bulk thermal conductivity of the interface material, thinning the bond line thickness, increasing the wetting or bonding of the surface, and increasing the flatness of the lid or the heat spreader. The current method of making enhancing the thermal conductivity of these attachment materials involves addition of high thermal conductive fillers such as silver particles or flakes. Some basic problems associated with this approach eliminate many of these compounds from practical application. These include poor adhesion or mechanical stiffnesses that adversely affect component reliability. Some newly developed silver-filled interfacial adhesives have high thermal conductivity but they lead to extensive voiding or have poor surface coverage. Although solder alloys have higher thermal conductivity (up to 10–20 times that of conventional TIMs), their reliability is a concern. Development and the associated challenges of new interface materials are discussed in [13–15]. La-sance [16] has identified various problems with the current test methods used commonly based on ASTM D5470 and has recommended several changes with reference to TIMs.

In this paper, we evaluate some of the major contributing factors to the thermal performance, e.g. bond line thickness, bulk thermal conductivity of the material and effect of void parameters during the assembly. Theta-JC and Theta-JB thermal performance of three different FC-CBGA packages (35 mm, 22 mm and 18 mm) using cup

lid, flat lid and no-lid configurations are investigated numerically. The Theta-JC thermal performance of a 35×35 mm CBGA package was evaluated using three different die sizes (5×5 mm, 15×15 mm and 20×20 mm) and various TIM-I materials.

2. Thermal model of package

The detailed dimensions of different flip chip package cross-sections with and without lid attached are shown in Figs. 1a–e. One side of the chip with bumps is soldered on to the substrate. The other side of the substrate is attached with a eutectic solder to the printed circuit board. Fig. 1a shows the package cross-section without lid where the die is exposed on the top surface (also called bare die or lidless package). Figs. 1b and c show a CBGA package with flat lid and cup lid. The cup and flat lids are attached to the die by a thermal interface material (TIM-I). For the cup lid package, a higher thermal conductive epoxy with weaker mechanical properties can be selected whereas for flat lids both thermal and mechanical properties have to be strong enough to hold the lid on top of the die. If a bare die is used, heat sink is directly attached to top of the die with TIM-II. The package was modeled as a series of embedded conductive cubical blocks.

A detailed thermal model of this package was created using FLOTHERM®, a commercial CFD tool [17]. This code uses the finite

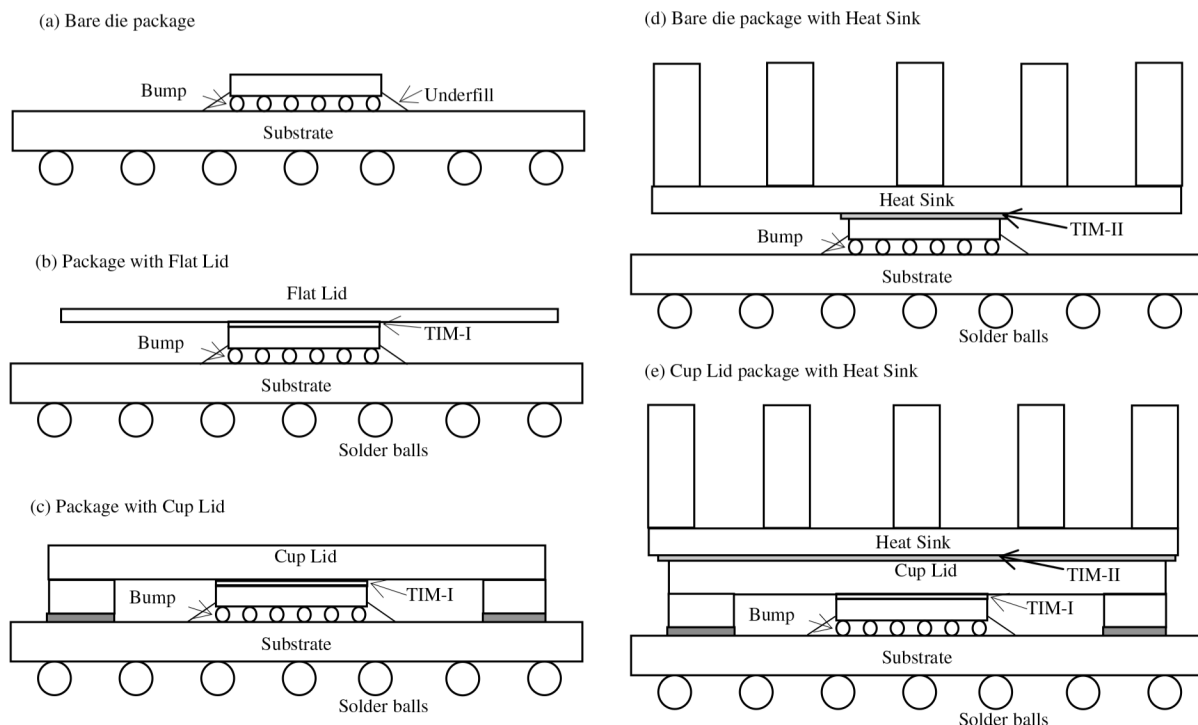


Fig. 1. Various package lid and thermal interface materials (TIM) in electronic packages modelled.

volume method for solving the conservation equations of mass, momentum and energy subject to appropriate boundary conditions. The three-dimensional governing equations are solved for steady state inside the enclosure around the package. The thermal performance of electronic packages is generally quantified in terms of their thermal resistance. Traditional metrics such as junction-to-case, junction to board and junction-to-ambient thermal resistances are used as figures of merit to compare package thermal performance.

Simulation results are reported based on three-dimensional conduction-based FLOTHERM simulation models for Theta-JC as per top cold plate test. Conduction based cooling flow channels model is used for Theta-JB as per the JEDEC standard [18]. Results from FLOPACK®, a web-based commercial package design tool (a two resistor compact model), are used to verify the 3D conduction based model results for quick assessment of the thermal performance. Figs. 2a–2c show the thermal simulation model setup for all package configurations tested.

The simulation results are compared on the basis of package junction-to-case and junction-to-board thermal resistances (θ_{JC} and θ_{JB}). The junction-to-case thermal resistance (θ_{JC}) is normally derived from a top cold plate test, in which the package is placed on a printed circuit board with all sides insulated except for the top surface. A cold plate with a specified temperature is pressed against the top surface. Hence, most of the power dissipated from the package leaves through its top surface (Fig. 2a). Subsequently, the junction-to-case thermal resistance, θ_{JC} ($^{\circ}\text{C}/\text{W}$), is calculated as

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad (1)$$

where T_J is the junction temperature, T_C is the temperature of the cold plate, which is estimated from the numerical simulations. P is the chip input power dissipation rate of the die.

Similarly, the junction-to-board resistance (θ_{JB}) is derived by placing the package in a specially constructed harness called “Ring Cold Plate” [15]. This method follows the Joint Electron Device Engineering Council (JEDEC) standard. The Ring Cold Plate (Fig. 2b) fixture consists of a standard four-layer JEDEC board inserted between two cold plates. The cold plates are in the shape of a ring. Middle parts of the ring-cold-plate are kept adiabatic so that most of the heat travels from the package through some distance within the board, and then out of the fixture through the coolant fluid in the cold plate. Subsequently, the junction-to-board thermal resistance, θ_{JB} ($^{\circ}\text{C}/\text{W}$), is from

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad (2)$$

where T_B is the board temperature, which is taken at a point on the board surface located in the middle of the longest side of the package with no more than 1 mm from the package edge. Fig. 2c shows the simplified two-resistor compact network model.

The simple conceptual package thermal network model is used Eq. (3), which links θ_{JB} and θ_{JC} thermal resistances with the die junction temperature and the ambient temperature as follows:

$$\left(\frac{T_J - T_A}{P}\right) = \theta_{JA}P = \left(\frac{P}{1/(\theta_{JC} + \theta_{CS} + \theta_{SA})}\right) + \left(\frac{P}{1/(\theta_{JB} + \theta_{BA})}\right) \quad (3)$$

Various thermal resistance values are the thermal characteristics metrics of packages used to measure the IC package thermal performance. Theta-JC is a measure of the internal thermal resistance

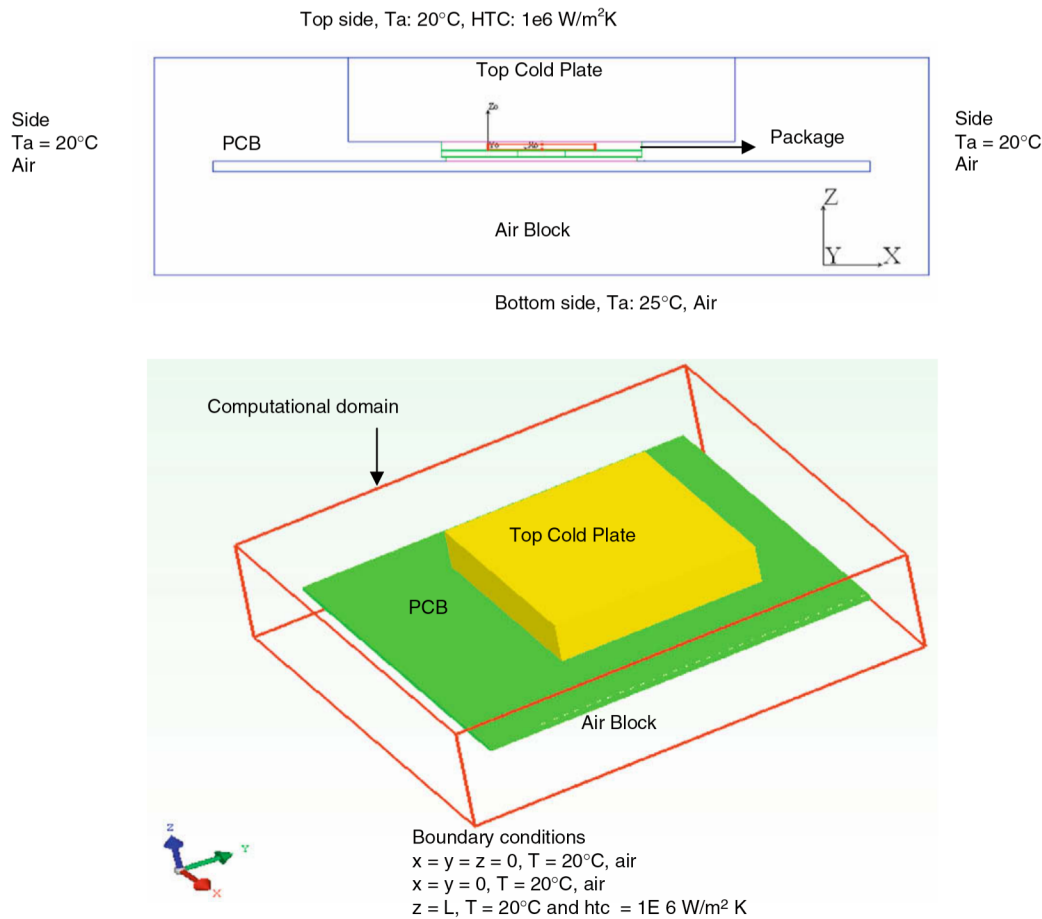


Fig. 2a. Theta-JC model: computational domain with boundary conditions.

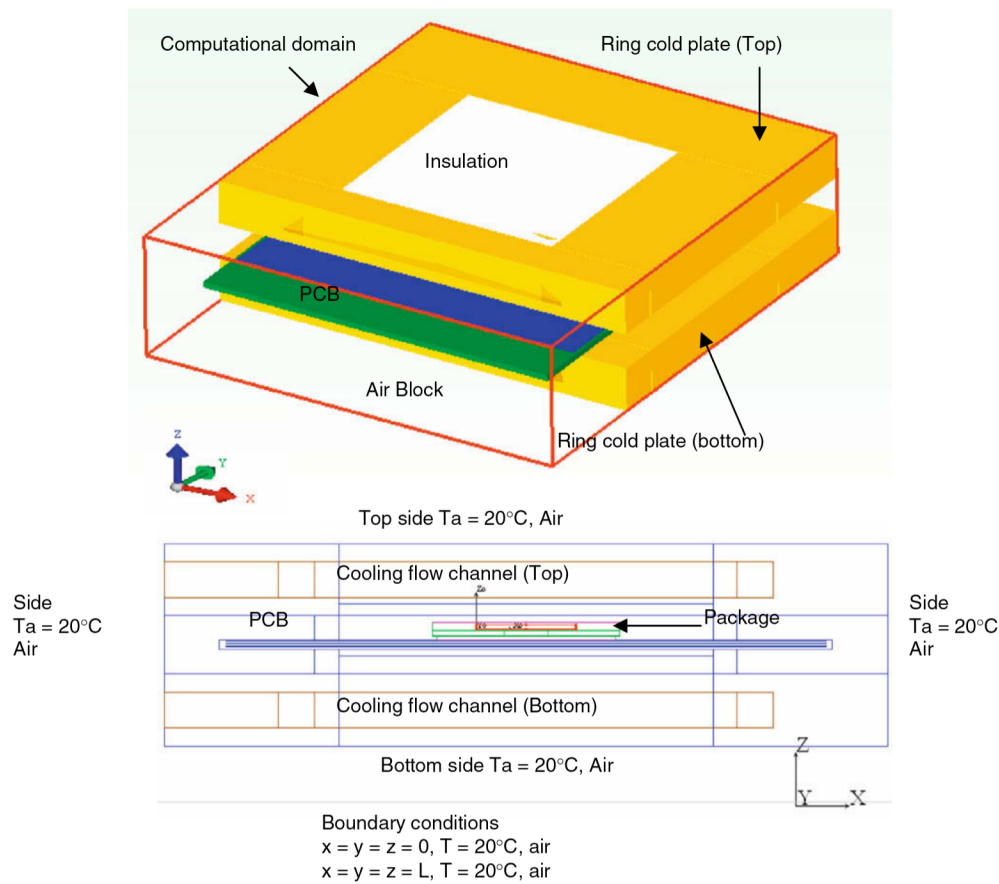


Fig. 2b. Theta-JB model: computational domain with boundary conditions.

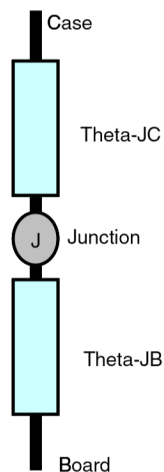


Fig. 2c. Simplified two-resistor network model.

along the major heat flow path from the die to the package top. Theta-JB is a measure of the package thermal resistance along the bottom side of heat flow path from the die to the printed circuit board through the substrate and the solder balls.

3. Numerical solution

Details of the generalized equation and the numerical method used are given in Ref. [19]. Initially, the energy equations are solved for temperature distribution inside the solution domain using boundary conditions as shown in Figs. 2a–2c. The huge and

unusual value of heat transfer coefficient is applied on the top boundary surface (as shown in Fig. 2a) to simulate a fixed temperature surface for the sake of computational convenience. The temperature distribution and flow velocities were obtained by solving the set of flow and energy equations as detailed in Ref. [20] in an environment consisting of a four-layer printed circuit board of dimensions, 102 mm × 114 mm, placed in a computational wind tunnel to compute the package power dissipation capability. The board includes all copper layers with discrete modeling for maximum accuracy. The flow inside the computational domain was assumed as turbulent with a forced convection velocity of 2.0 m/s. An algebraic turbulence model was used to describe the free stream turbulence. Wall functions were used to describe the turbulent boundary layer near solid surfaces. The total grid cell count for the detailed model simulations ranged from 300,000 cells to a million cells. Details of the velocity and boundary conditions used for simulating the flow field and the temperature field inside the solution domain are similar to those provided by Ravi and Mujumdar [20]. A grid refinement study was conducted by evaluating progressively the model results to achieve grid-independent simulation results. The model is not fully symmetric, therefore a 3D model of the problem was employed. Thermal models were created using the material properties listed in Table 1. Fig. 2d shows a pictorial representation of the potential thermal model of the voids. Equivalent volume-averaged thermal conductivity values were estimated and used as inputs for the simulations.

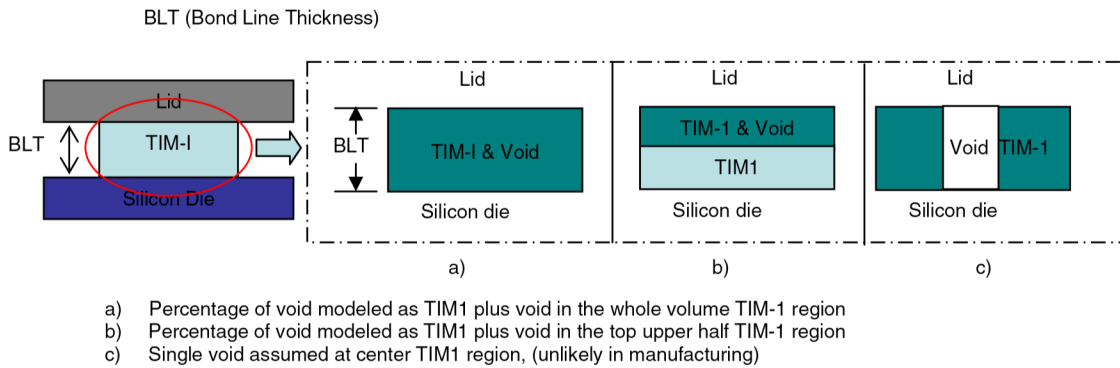
4. Results and discussion

Numerical results are presented for various thermal resistance parameters for different package and die sizes. It should be noted

Table 1

Thermal properties of various materials used

Material	Thermal conductivity (k) (W/m K)	Density (ρ) (kg/m ³)	Specific heat (C_p) (J/kg K)
Silicon (die)	$117.5 - 0.42 \times (T - 100)$	2330	700
Ceramic substrate	14.0	3690	880
Lid	170–190	3010	749
Underfill	0.67	Na	Na
C4 bump (bump)	36	10,750	142
Solder ball (high pb)	36	10,750	142
TIM-I (lid to die attach)	0.2–10.0	Na	Na
TIM-II (heat sink to lid attach or die to heat sink for lidless package)	0.2–10.0	Na	Na
Aluminum (heat sink)	180	2700	963
FR4 (PCB)	0.3	1200	880

**Fig. 2d.** Thermal model: details of TIM1 and potential void locations.

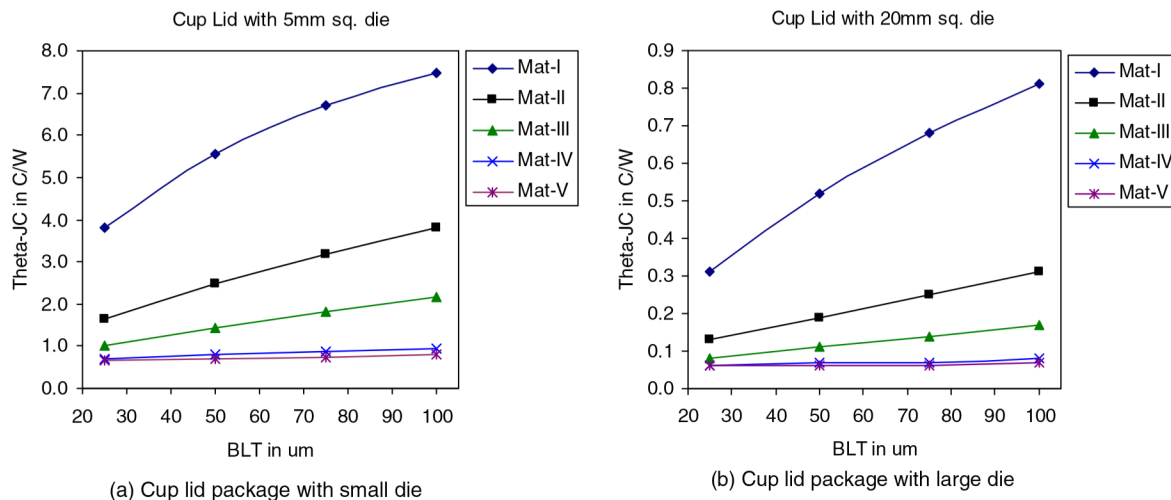
that two-resistor compact network models were also utilized to establish the thermal characteristics. A uniform heat input of 17 W was applied at the mid-plane of the die. Die junction temperature and package board or case temperature were computed at an ambient temperature of 20 °C using the detailed thermal model.

4.1. Effect of BLT, die size and TIM-I with cup lid

Fig. 3a shows variation of the interfacial thermal resistance with TIM-I bulk conductivity for different bond line thicknesses for a 35 mm package fitted with a 5 mm die for the cup lid package. The increase of thermal resistance can be seen to be more pronounced at lower TIM-1 bulk conductivity as the bond line thickness increases, as expected. The Theta-JC performance curve is

nearly flat, showing no significant effect on BLT with Mat-IV ($k = 10$ W/m K) and Mat-V ($k = 20$ W/m K). The other interfacial materials tested were, Mat-I ($k = 0.2$ W/m K), Mat-II ($k = 0.8$ W/m K) and Mat-III ($k = 2.0$ W/m K). The package interface thermal resistance decreases approximately 50% with BLT change of 100–25 μ m using Mat-I. Similar decrease is only 27% for Mat-IV while it is 17% for Mat-V.

Fig. 3b shows thermal performance plots for a large die size. By increasing the die size from 5 to 20 mm, the effective heat transfer area increases 16 times. The thermal resistance decreases 9–12 times with increased die size. The overall magnitude of Theta-JC is predicted to be 0.3–0.8 °C/W with Mat-I and it is in the range <0.1 °C/W for a highly conductive material like Mat-IV. Based on our simulation results it is clear that the thermal resistance can

**Fig. 3.** Theta-JC performance curves for various TIM-I for different BLT (35 mm, cup lid package).

be reduced by 4–12 times by selecting a suitable highly conductive material and by choosing a smaller bond line thickness especially for the small die package.

4.2. Effect of BLT, die size and TIM-I for flat lid package

Figs. 4a and b show Theta-JC performance curves for a flat lid type package of different die sizes (5 mm and 20 mm). The thermal performance predictions for different BLT's with various thermal interface materials are observed to be similar to those with the cup type lid. The thermal resistances are rather sensitive to the bond line thickness. Thermal performance is poorer and the curve becomes nearly flat as the thermal conductivity increases. The magnitude of the Theta-JC variation is lower for the larger die size. For an average BLT of 50 μm using Mat-III (2.0 W/m K), the value of Theta-JC decreases from 1.5 $^{\circ}\text{C}/\text{W}$ (with 5 mm die size) to 0.17 $^{\circ}\text{C}/\text{W}$ (with 15 mm die size) and to 0.1 $^{\circ}\text{C}/\text{W}$ (with 20 mm die size). Overall, as expected, the cup lid type package is better than the flat lid package for better thermal management.

4.3. Effects of package size and substrate conductivity

Fig. 5 compares the thermal performance of various BLT's with different materials for package body sizes of 18 mm and 35 mm for a smaller die (5 mm die). Smaller die size was chosen for this study since it is more sensitive to Theta-JC than the larger die package. As expected, Theta-JC is higher for larger package size due to better heat distribution towards the substrate as compared with a smaller package size. With a higher conductivity material using smaller die size, Theta-JC of both packages is nearly flat and indeed they overlap as seen in Fig. 5. At lower BLT, the material effect is less pronounced than that of BLT. Additional simulations were carried out by changing the thickness of the flat lid from 1.5 to 3.00 mm, but the results showed only marginal change. Changing the flat lid material from aluminum to copper also did not show any improvement in the Theta-JC thermal performance.

Lidless (package without lid attached) is seen to show significant effect on package junction-to-board thermal resistance. Fig. 6 compares the thermal performance of a 35 mm package for two different die sizes. A substrate material with a smaller number of copper layers is expected to have an effective equivalent conductivity of under 5.0 W/m K. Theta-JB performance of the package is significant for a package with smaller die and low conductivity substrate material. The value of the junction-to-board thermal resistance decreased by approximately 4–5 times with increase of die size for a poorly conductive substrate. Use of materials such as alumina ceramic as substrate ($k > 14 \text{ W/m K}$) results in better thermal performance with lower Theta-JB value for large die sizes.

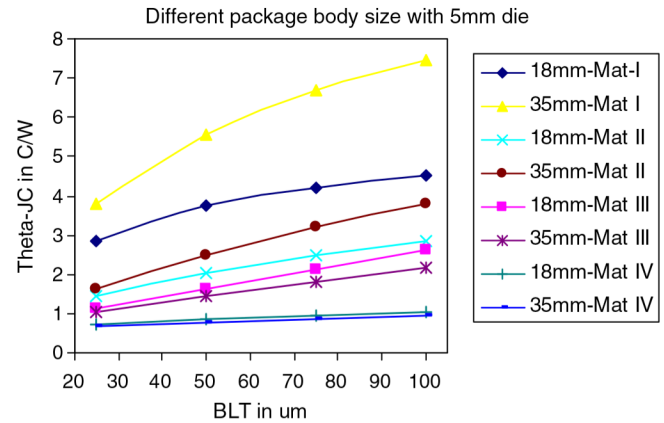


Fig. 5. Theta-JC for different TIM-I.

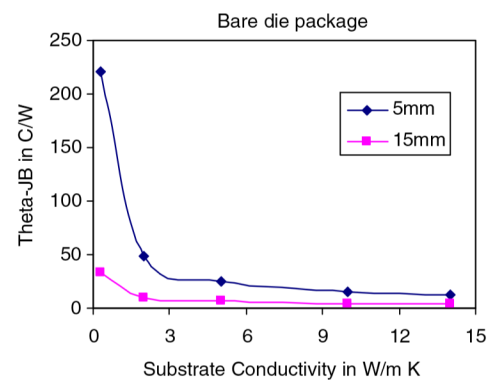


Fig. 6. Theta-JB on bare die package.

4.4. Effect of voids

Fig. 2d shows the thermal model of TIM-1 and possible voids within the TIM-1 material. In this study, the effect of voids (5–15% on volume basis) on Theta-JC performance was investigated numerically. For the simulation study, initially the voids were assumed to form in the top half region of the TIM-1 volume region (seen after curing in the assembly process). Next, uniform void distribution is assumed to occur throughout the TIM-1 volume. Another case with a single void at the centre as shown in the diagram (Fig. 2d) was also simulated. Some of the experimental samples were designed deliberately to have voids up to 15% to

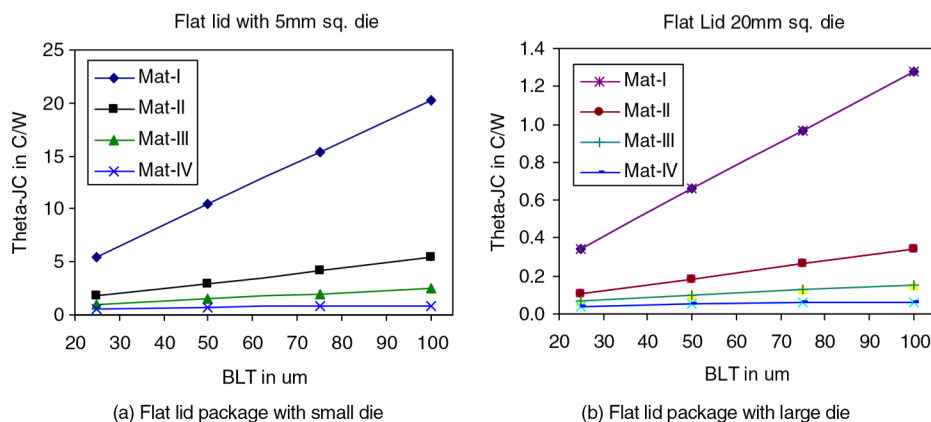


Fig. 4. Theta-JC performance curves for various TIM-I for different BLT (35 mm, flat lid package).

Table 2
Effect of TIM1 voids on thermal resistance

22 mm CBGA package, thermal resistance: Theta-JC (°C/W)				
Epoxy Thk (μm)	Flat lid used, die to lid attach conductivity: 0.4 W/m K			
	No void	5% void	10% void	15% void
<i>Void distributed across the whole volume of DA region</i>				
25	1.11	1.16	1.20	1.26
50	2.01	2.09	2.18	2.28
<i>Void distributed in the upper half of the DA region</i>				
25	1.11	1.15	1.18	1.20
50	2.01	2.05	2.10	2.15
<i>Solid single void at centre of DA region</i>				
25	1.11	1.23	1.34	1.44
50	2.01	2.18	2.33	2.47

compare the data with numerical results. A comparison of the thermal resistances at each BLT is given in Table 2. The value of the predicted Theta-JC is lower when the voids are uniformly distributed in the top half of the region as compared to cases of uniform distribution in the whole region. For the worst thermal case with a single void in the center region, the highest value of Theta-JC is obtained. The value of Theta-JC increases ~10%, ~17%, and ~23% for 5%, 10%, and 15% voids, respectively.

4.5. Effect of heat sinks and interface materials

Eliminating one of the interfaces can reduce the overall thermal resistance by a significant fraction. Package designs to protect the bare die enable wider use of bare die packaging, and eliminate one

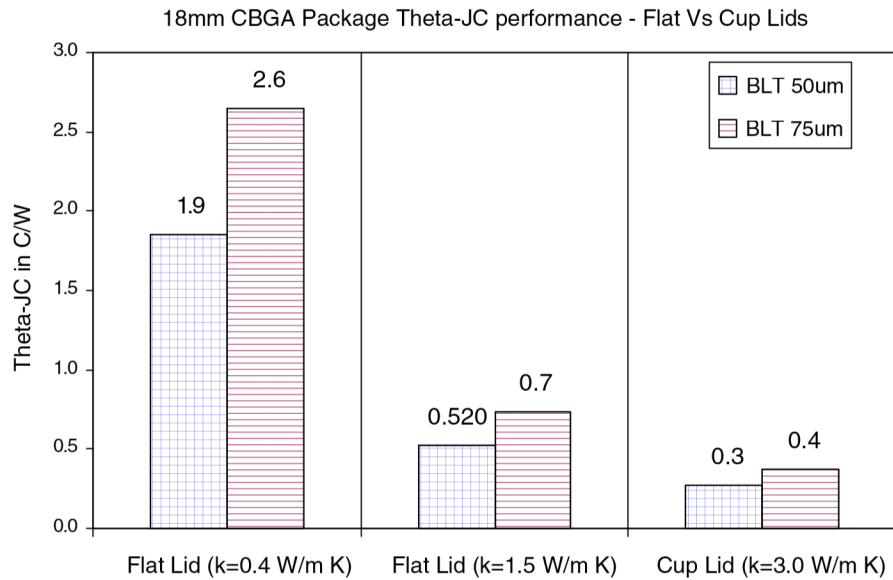


Fig. 7. Effect on package Theta-JC for different BLT over cup and flat lids.

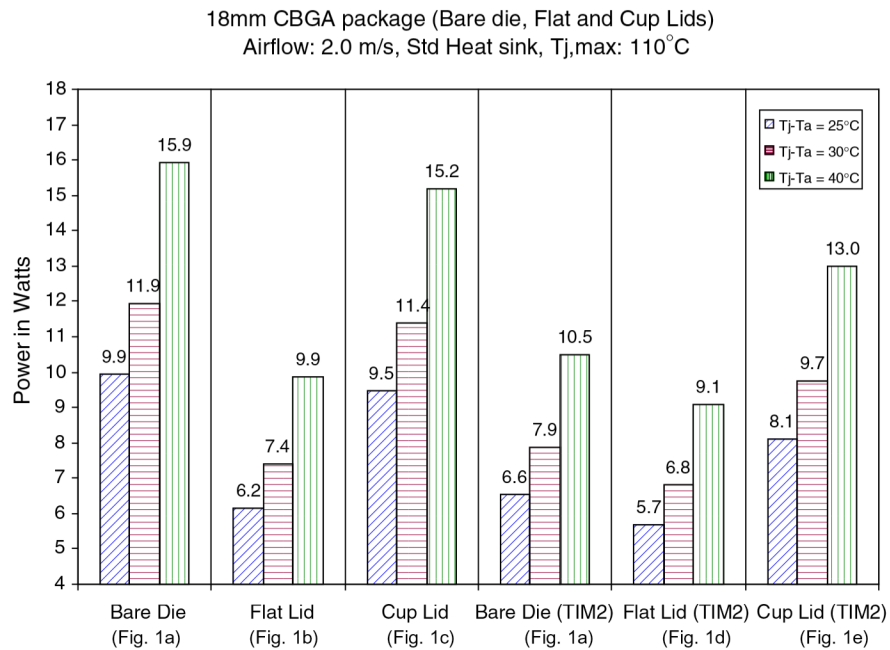


Fig. 8. Comparison of package power dissipation for various lid types with and without TIM-II material.

of the two interfaces in the heat transfer path. Lids are used not only to spread the heat but also to protect the die from mechanical damage. Lids help spread the heat from the die footprint to a larger area so that the heat sink is more efficient in dissipating heat to the environment. For a flat lid, good mechanical properties along with excellent wetting and adhesion characteristics are essential for TIM-I (some interface materials have lower thermal conductivity values of 0.4 and 1.5 W/m K). When a bare die package is used, the interface material between the die and heat sink is softer or more compliant to prevent damage during assembly. For cup lid package, TIM-I material has higher thermal conductivity and good mechanical properties.

The computed Theta-JC results are shown in Fig. 7 for 50 μm and 75 μm BLT (18 mm CBGA package for different TIM-I materials). Lower Theta-JC is achieved using the cup lid package with a smaller BLT (use of better conductive interface material is possible with cup lid). Use of bare die package can help to get rid of the first level thermal resistance. Fig. 8 shows a graph of the package power dissipation capability for the different lid choices, exploring TIM-II effects (standard heat sink at airflow of 2.0 m/s). The power dissipation results are compared to cases with and without the interface material (TIM-II) for different lid options. Among the various lid types, the highest package power dissipation is possible using bare die configuration without TIM-II interface (configuration as shown in Fig. 1a with heat sink on top). It shows that the power dissipation of the bare die package can be increased in the range between 3.3 and 6.8 W compared with other configurations (no TIM-II is an ideal case for comparison purpose, in applications to select least resistant material). Overall, the inclusion of TIM-II lowers the package power dissipation capability by about 4.4 W (bare die), 0.8 W (flat lid) and 2.2 W (cup lid), respectively. Power estimation capability of the bare die package is 60% improved (without TIM-II) and is 16% (with TIM-II) better when compared with the equivalent flat lid case. Similar power dissipation improvement is only ~5% over the cup lid when there is no interface resistance. The power dissipation of the bare die package decreases nearly 60% when using TIM-II material (configuration as seen in Fig. 1d). For cup and flat lid cases, the power dissipation rate dropped about 15%. This is due to the lid heat spreading effect from concentrated die to lid then by convection to the ambient. Selection of the right interface material is critical when the bare die with external heat sink is used in the system environment. As seen in Fig. 8, the cup lid performance is better than the bare die one if a poor conductive TIM-II material used.

5. Conclusions

This study has demonstrated that the junction-to-case thermal resistance of a flip package can be minimized in several ways by right selection of the interface material and by reducing BLT in the assembly process. Effects of different types of lids and bare

die options on thermal performance are compared. Assembly process factors such as BLT and percentage of void have appreciable effect on the thermal performance of the package. Numerical simulation provides valuable information about the package interface thermal resistances and the effect of the thermal conductivity. The package power dissipation when using a cup lid, a flat lid and a bare die packages are compared on the basis of simulation. Eliminating TIM-I interface material or using the least resistant TIM-II to attach the heat sink is an effective means of cooling for high power thermal applications with bare die packages. The die size plays a significant role in efficient thermal power dissipation of the package.

References

- [1] C. Lasance, Thermally driven reliability issues in microelectronic systems: status-quo and challenges, *Microelectronics Reliability* 43 (2003) 1969–1975.
- [2] International Technology Roadmap for Semiconductors, 2003 update, Assembly and Packaging, Semiconductor Industry Association (SIA), 2003.
- [3] G. Kromann, Thermal management of a C4/ceramic ball grid array: the motorola powerPC 603 and powerPC 604 RISC microprocessors, in: *Proceedings of 12th IEEE Semiconductor Thermal Measurement and Management Symposium*, Austin, 1996, p. 36–42.
- [4] S. Lee, How to select a heat sink, *Electronics Cooling* 1 (1) (1995).
- [5] M. de Sorgo, Thermal interface materials, *Electronics Cooling* 2 (3) (1996).
- [6] C. Latham, Thermal resistance of interface materials as a function of pressure, technical brief, *Electronics Cooling*, 1996.
- [7] D.D.L. Chung, Materials for thermal conduction, *Applied Thermal Engineering* 21 (2001) 1593–1605.
- [8] J.P. Gwinn, R.L. Webb, Performance and testing of thermal interface materials, *Microelectronics Journal* 34 (2003) 215–222.
- [9] G. Becker, C. Lee, Z. Lin, Thermal conductivity in advanced chips, *IEEE Transactions on Advanced Packaging* 14 (7) (2005) 14–16.
- [10] B.M. Guenin, Calculations for thermal interface materials, *Electronics Cooling* 9 (3) (2003) 8–9.
- [11] R.S. Prasher, P. Koning, J. Shipley, J.L. Wang, Thermal resistance of particle laden polymeric thermal interface materials, *Journal of Heat Transfer* 125 (2003) 1170–1177.
- [12] L. Maguire, M. Behnia, G. Morrison, Systematic evaluation of thermal interface materials – a case study in high power amplifier design, *Microelectronics Reliability* 45 (2005) 711–725.
- [13] V. Wakharkar, C. Matayabas, E. Lehman, R. Manipalli, M. Renavikar, S. Jayaraman, V. Lebonheur, Materials technologies for thermo-mechanical management of organic packages, *Intel Technology Journal* 9 (4) (2005).
- [14] E.C. Samson, S.V. Machiroutu, J. Chang, I. Santos, J. Hermerding, A. Dani, R. Prasher, D.W. Song, Interface material selection and a thermal management technique in second-generation platforms built on intel® Centrino™ mobile technology, *Intel Technology Journal* 9 (1) (2005).
- [15] R. Viswanath, V. Wakharkar, A. Watwe, V. Lebonheur, Thermal performance challenges from silicon to systems, *Intel Technology Journal* (2000).
- [16] C.J.M. Lasance, Problems with thermal interface material measurements: suggestions for improvements, *Electronics Cooling* 9 (4) (2003) 22–29.
- [17] FLOTHERM Reference and User Manual, Flomerics Limited, 2003.
- [18] EIA/JESD 51-8, Integrated Circuit Thermal Test Method Environmental Conditions Junction-To-Board, 1999.
- [19] Ravi Kandasamy, Suresh Subramanyam, Application of computational fluid dynamics simulation tools for thermal characterization of electronic packages, *International Journal of Numerical Methods for Heat and Fluid Flow* 15 (1) (2005) 61–72.
- [20] Ravi Kandasamy, A.S. Mujumdar, Thermal analysis of a flip chip ceramic ball grid array (CBGA) package, *Microelectronics Reliability* 48 (2) (2008) 261–273.