UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	02/20/2018	9899481	1012-1287 / 2015P51742 US	2194

57579 7590 01/31/2018

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Ralf Otremba, Kaufbeuren, GERMANY;
Infineon Technologies Austria AG, Villach, AUSTRIA;
Klaus Schiess, Allensbach, GERMANY;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57579 7590 10/06/2017
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

TITLE OF INVENTION: Electronic Component and Switch Circuit

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/08/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
RETEBO, METASEBIA T	2842	327-434000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Murphy, Bilak & Homiller, PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Infineon Technologies Austria AG

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Villach, AT

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-5650 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Mark R. Bilak, Reg. No. 47,423/ Date 2018-01-05

Typed or printed name Mark R. Bilak Registration No. 47,423

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal				
Application Number:	14997914			
Filing Date:	18-Jan-2016			
Title of Invention:	Electronic Component and Switch Circuit			
First Named Inventor/Applicant Name:	Ralf Otremba			
Filer:	Mark Ronald Bilak/Katie Kennedy			
Attorney Docket Number:	1012-1287 / 2015P51742 US			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	31423625
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Mark Ronald Bilak/Katie Kennedy
Filer Authorized By:	Mark Ronald Bilak
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	05-JAN-2018
Filing Date:	18-JAN-2016
Time Stamp:	17:16:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$960
RAM confirmation Number	010818INTEFSW00004424505650
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	1012-1287_Issue_Fee_Transmittal.pdf	201636 a0f19b6af6946e8221d4ba725a1e9ce469547b56	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30718 38a45a4bede6b3911c34a7c1a39aba2447f4005a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	232354		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

57579 7590 10/06/2017

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER
RETEBO, METASEBIA T

ART UNIT	PAPER NUMBER
2842	

DATE MAILED: 10/06/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

TITLE OF INVENTION: Electronic Component and Switch Circuit

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/08/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57579 7590 10/06/2017
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

TITLE OF INVENTION: Electronic Component and Switch Circuit

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/08/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
RETEBO, METASEBIA T	2842	327-434000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

57579 7590 10/06/2017
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER	
RETEBO, METASEBIA T	
ART UNIT	PAPER NUMBER
2842	

DATE MAILED: 10/06/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/997,914	Applicant(s) OTREMBA ET AL.	
	Examiner METASEBIA RETEBO	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/19/2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-4,6 and 8-19*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/M. R./	/LINCOLN DONOVAN/
Examiner, Art Unit 2842	Supervisory Patent Examiner, Art Unit 2842

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

1. Claims 1-4, 6, 8, 10-19 are allowable. Claim 9, previously withdrawn from consideration as a result of a restriction requirement, hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because all claims previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, the restriction requirement as set forth in the Office action mailed on 1/26/2017 is hereby withdrawn. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See In re Ziegler, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations of an electronic component, comprising: a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode; a die pad; and a first lead, a second lead and a third lead, wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality, **wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor**

transistor device is coupled to the die pad, wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

Regarding claims 2-4, 6 and 8-11, these claims are allowed since they depend on claim 1.

Regarding claim 12, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations of a switch circuit, comprising: a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead, the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provides a source sensing functionality; and a second transistor device, wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device, **wherein the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad, wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.**

Regarding claims 13-18, these claims are allowed since they depend on claim 12.

Regarding claim 19, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations of an electronic component, comprising: a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and a housing, wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad, wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces, **wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based**

transistor device is coupled to the die pad, wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to METASEBIA RETEBO whose telephone number is (571)272-9299. The examiner can normally be reached on Monday - Friday 7:30am to 5:00pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. R. /
Examiner, Art Unit 2842
/LINCOLN DONOVAN/
Supervisory Patent Examiner, Art Unit 2842

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14997914	OTREMBA ET AL.
	Examiner	Art Unit
	METASEBIA RETEBO	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/2003	6/16/2017	MR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
327	434	6/16/2017	MR

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text search. (see search history)	9/29/2017	MR
Inventor and Assignee search EAST and PALM	6/16/2017	MR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
327	434	9/29/2017	MR
H01L29	2003	9/29/2017	MR
H01L29	1608	9/29/2017	MR
H01L29	7801	9/29/2017	MR
H03K17	687	9/29/2017	MR

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14997914	OTREMBA ET AL.
	Examiner	**Art Unit**
	METASEBIA RETEBO	2842

CPC						
Symbol					**Type**	**Version**
H01L		29	/	2003	F	2013-01-01
H01L		29	/	7801	I	2013-01-01
H01L		29	/	1608	I	2013-01-01
H03K		17	/	687	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

/METASEBIA RETEBO/ Examiner.Art Unit 2842	09/29/2017	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/LINCOLN DONOVAN/ Supervisory Patent Examiner.Art Unit 2842	09/30/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14997914	OTREMBA ET AL.
	Examiner	**Art Unit**
	METASEBIA RETEBO	2842

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
327	434	H	0	3	K	17 / 687 (2006.0)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

/METASEBIA RETEBO/ Examiner.Art Unit 2842 (Assistant Examiner)	09/29/2017 (Date)	**Total Claims Allowed:** 17	
/LINCOLN DONOVAN/ Supervisory Patent Examiner.Art Unit 2842 (Primary Examiner)	09/30/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14997914	OTREMBA ET AL.
	Examiner	**Art Unit**
	METASEBIA RETEBO	2842

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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2	2	16	18												
3	3	17	19												
4	4		20												
	5														
5	6														
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11	13														
12	14														
13	15														
14	16														

/METASEBIA RETEBO/ Examiner.Art Unit 2842	09/29/2017	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/LINCOLN DONOVAN/ Supervisory Patent Examiner.Art Unit 2842	09/30/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"20090212284".pn.	US-PGPUB; USPAT	OR	ON	2017/09/29 09:57
L2	4276	lateral near transistor	US-PGPUB; USPAT	OR	ON	2017/09/29 09:59
L13	1025	327/434.ccls.	US-PGPUB; USPAT	OR	ON	2017/09/29 11:30
L14	9	L13 and (lateral near transistor)	US-PGPUB; USPAT	OR	ON	2017/09/29 11:30
S1	429	(("INFINEON") near3 ("TECHNOLOGIES") near3 ("AUSTRIA") near3 ("AG")).AANM.	USPAT	OR	ON	2017/06/14 10:53
S2	1	("20130299878").PN.	US-PGPUB; USPAT	OR	ON	2017/06/14 11:31
S3	395	(("OTREMBA") near3 ("Ralf")).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/14 11:31
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S6	8	("7250641" | "7838097" | "20110049580" | "20110101466" | "20120022332" | "20120223322" | "20140252577" | "20150116025").pn.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/14 14:48
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S9	111	(("SCHIESS") near3 ("Klaus")).INV.	US-PGPUB; USPAT;	OR	ON	2017/06/14 17:31

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S19	110	(semiconductor near transistor) same block$4 near voltage	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 14:28
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S23	1025	327/434.ccls.	US-PGPUB; USPAT	OR	ON	2017/06/16 19:41
S24	7893	H01L29/2003.cpc.	US-PGPUB; USPAT	OR	ON	2017/06/16 19:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	729	327/434.ccls.	USPAT	OR	ON	2017/09/29 10:01
L4	21	l3 and "L2"	USPAT	OR	ON	2017/09/29 10:02
L5	3453	H01L29/2003.cpc.	USPAT	OR	ON	2017/09/29 10:03
L6	99	L5 and "L2"	USPAT	OR	ON	2017/09/29 10:05
L7	2474	H01L29/1608.cpc.	USPAT	OR	ON	2017/09/29 10:51
L8	78	L7 and "L2"	USPAT	OR	ON	2017/09/29 10:53
L9	366	H01L29/7801.cpc.	USPAT	OR	ON	2017/09/29 11:24
L10	809	H03K17/687.cpc.	USPAT	OR	ON	2017/09/29 11:27
L11	3844	"L2" and "S23"	USPAT	OR	ON	2017/09/29 11:29

9/29/2017 11:31:04 AM
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/997,914	Filing Date 01/18/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/19/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
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	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
EMORY LANE

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: **Otremba**	)	
	)	
Serial No.: **14/997,914**	)	PATENT PENDING
	)	
Filed: **January 18, 2016**	)	Examiner: **RETEBO, METASEBIA T**
	)	
For: **Electronic Component and Switch Circuit**	)	Group Art Unit: **2842**
	)	
Docket No: **1012-1287 / 2015P51742 US**	)	Confirmation No.: **2194**
	)	
	)	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Applicant submits this paper in response to the Office Action mailed June 23, 2017 and requests favorable reconsideration in light of the following remarks and/or amendments. No fees should be required for entry of this response, but the Commissioner is hereby authorized to charge any required fees to Deposit Account No. 50-5650.

AMENDMENTS TO THE DRAWINGS

Please replace drawing sheets 1/13 - 13/13 with replacement drawing sheets 1/8 - 8/8 submitted herewith.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An electronic component, comprising:

a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;

a die pad; and

a first lead, a second lead and a third lead,

wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,

wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,

wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

2. (Original) The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.

3. (Original) The electronic component of claim 1, wherein the compound semiconductor

transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

4. (Original) The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

5. (Cancelled).

6. (Original) The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.

7. (Cancelled).

8. (Original) The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.

9. (Withdrawn) The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

10. (Original) The electronic component of claim 4, wherein the second current electrode is

coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

11. (Original) The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

12. (Currently Amended) A switch circuit, comprising:

a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead, the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provides a source sensing functionality; and

a second transistor device,

wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device,

wherein the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad,

wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

13. (Original) The switch circuit of claim 12, wherein a drain of the first transistor device and

a source of the second transistor device are coupled to a common die pad.

14. (Original) The switch circuit of claim 12, wherein the first transistor device is housed in a package comprising a first die pad coupled to a drain of the first transistor device and the second transistor device is housed in a package comprising a second die pad coupled to a source of the second transistor device.

15. (Original) The switch circuit of claim 14, wherein the first die pad and the second die pad are mounted on a common conductive layer.

16. (Original) The switch circuit of claim 12, wherein a first contact clip is coupled to one of a source and a drain of the first transistor device and a second contact clip is coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.

17. (Original) The switch circuit of claim 16, wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.

18. (Original) The switch circuit of claim 12, wherein a source of the first transistor device is coupled to a source of the second transistor device.

19. (Currently Amended) An electronic component, comprising:

a Group III nitride-based transistor device having a blocking voltage capability of at least

400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

a housing,

wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

20. (Cancelled).

REMARKS

The June 23, 2017 Office Action has been carefully studied and considered. Claims 1-20 were pending, of which claim 9 was withdrawn from consideration, and claims 1-8 and 10-20 were rejected. Applicant respectfully submits that all pending claims are allowable over the references cited in the Office Action at least for the following reasons.

Claim Amendments

Claim 1 is amended to include the features of claims 5 and 7. Claims 12 and 19 are amended in a similar manner. Claims 5, 7 and 20 are cancelled. No new matter is added by way of these amendments, and entry is respectfully requested.

Drawings Objections

The drawings objections should be moot in view of the replacement drawings submitted herein, and withdrawal of the drawings objections is respectfully requested.

§102/§103 Rejections

Independent claim 1 is rejected under 35 USC 102 (a) (1) as being anticipated by the reference Otremba '284 (US 2009/022284). Independent claims 1, 12 and 19 are rejected under 35 USC 103(a) in view of Otremba '313 (US2015/0115313) and Lui (US 2011/0049580). Applicant respectfully submits that all claims presented herein are patentable over the cited references for at least for the following reasons.

§102 Rejection

Claim 1 is amended to include features from pending claims 5 and 7, and now recites the features of "wherein the first transistor device is a **lateral transistor device** and a drain or a

source of the first transistor device is coupled to the die pad". Otremba '284 fails to anticipate at least these features of amended claim 1.

In rejecting prior claim 1 over Otremba '284, the Office points to Otremba '284's FIGS. 1-9 as anticipating prior claim 1. However, Otremba '284 fails to teach at least the feature of a **lateral transistor device** as recited in amended claim 1. Otremba '284 teaches a **vertical** transistor which includes current electrodes on opposing surfaces, see the electrodes 12 and 14 in figure 5C, for example. Further, paragraph [0015] describes the vertical structure of the semiconductor chips taught by Otremba '284. However, Otremba '284 **does not teach a lateral** transistor device.

Otremba '284 fails to anticipate claim 1 for at least these reasons. Claim 1 and all claims depending therefrom are patentable over Otremba '284 at least for these reasons.

§103 Rejections

Amended claim 1 recites, *inter alia,* the following:

> wherein the first lead, the second lead and the **third lead** are s**paced at a distance from the die pad**, …
> wherein the **control electrode** is coupled to the **first** lead, the **first current electrode** is coupled to the **die pad**, the **second current electrode** is coupled to the **second lead** and the **third lead** is coupled to the compound semiconductor transistor device and provides a **source sensing functionality**,
> wherein the first transistor device is a **lateral transistor device** and a drain or a source of the first transistor device is coupled to the die pad**,**
> wherein the **first current electrode** is **coupled to the die pad** by a **plurality of bond wires or a contact clip**.

The combination of Otremba '313 and Lui fails to render obvious at least the above-highlighted features of amended claim 1. In rejecting prior claim 1 over the cited references, the Office equates Otremba '313's lead 66 to the claimed first lead coupled to the claimed control electrode, its lead 67 to the claimed second lead coupled to the claimed second electrode, its lead

64 (which extends from its die pad 42) to the claimed **third lead**, and its drain electrode 50 (which is mounted on and electrically coupled to the die pad 42; see paragraph [0035]) to the claimed first current electrode. The Office acknowledges that Otremba '313 "**does not teach the third lead is spaced at a distance from the die pad**" (see Office Action, p. 5, first para.), and points to Lui as disclosing this feature. The Office further alleges that it would have been obvious to modify Otremba '313 in view of Lui. Applicant respectfully disagrees for at least the following reasons.

Firstly, Otremba '313's **lead 64 does not provide source sensing functionality** as indicated in the Office Action (see Office Action, p. 5, first para.). Indeed, Otremba '313 states that its lead 64 represents a **drain lead** (see paragraph [0041]); however, Otremba '313 states nothing regarding drain lead 64 providing a sensing function. Secondly, Otremba '313 **does not disclose a lateral transistor device**. Indeed, contrary to what the Office states at the bottom of page 5 of the Office Action in its rejection of prior claim 5 (prior claim 5 previously recited a "lateral transistor device", the feature now forming part of amended claim 1), Otremba '313's paragraphs [0012], [0024] and [0040] state nothing regarding a lateral transistor device; instead, the cited paragraphs use the term "lateral" to refer to the lateral **direction** (as opposed to the vertical direction; see para. [0012], for example). In stark contrast, as is well-known in the semiconductor arts, a lateral transistor device is a bipolar transistor in which **current flows across the base** in the **direction parallel to the wafer surface**; in contrast to conventional

vertical bipolar transistor in which current across the base flows in the direction normal to the surface.[1]

Importantly, neither Lui nor Otremba '313 teaches or otherwise renders obvious a **package for a lateral transistor** which includes **three leads configured as recited in claim 1**, **each** of the three leads being **spaced at a distance** from the die pad with one of the leads (*i.e.* the claimed third lead) providing a source sensing functionality, the package further including a first current electrode **coupled to the die pad** by a plurality of **bond wires or a contact clip**. Otremba '313 discloses a package with a bidirectional switch with **two vertical transistors** mounted and electrically coupled **to two separate portions of a die pad** by the **drain electrodes**. The upwardly facing source electrodes are coupled by the clip 45 to provide the bidirectional switch. Lui, on the other hand, discloses a **cascode arrangement** that **does not include a source sensing function**. Accordingly, there is further no motivation for the person of ordinary skill in the art to **replace** the **vertical** transistor as taught by Otremba '313 with a **lateral** transistor as claimed because as the **circuit arrangement** taught by Otremba '313 would no longer be operational as the circuit arrangement depends on the **drain electrode located on the rear side of the transistor being electrically connected to the die pad**.

The combination of the cited references fails to render amended claim 1 obvious for at least these reasons. Claim 1 and all claims depending therefrom are patentable over the cited

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[1] See definition of "lateral transistor" at http://www.semi1source.com/glossary/default.asp?searchterm=lateral+transistor.

reference at least for these reasons. For analogous reasons, claims 12 and 19 and all claims depending therefrom too are patentable over the cited references.

Withdrawal of all claim rejections is respectfully requested.

Conclusion

The present application should be in condition for allowance in view of the amendments and remarks made herein. Action to such effect is respectfully requested. The Examiner is encouraged to contact the undersigned at (919)-948-3390 if any outstanding matters can be readily addressed by a phone call.

Respectfully submitted,
Murphy, Bilak & Homiller, PLLC

Dated: September 19, 2017

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Registration No.: 73,024

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FIG 1A

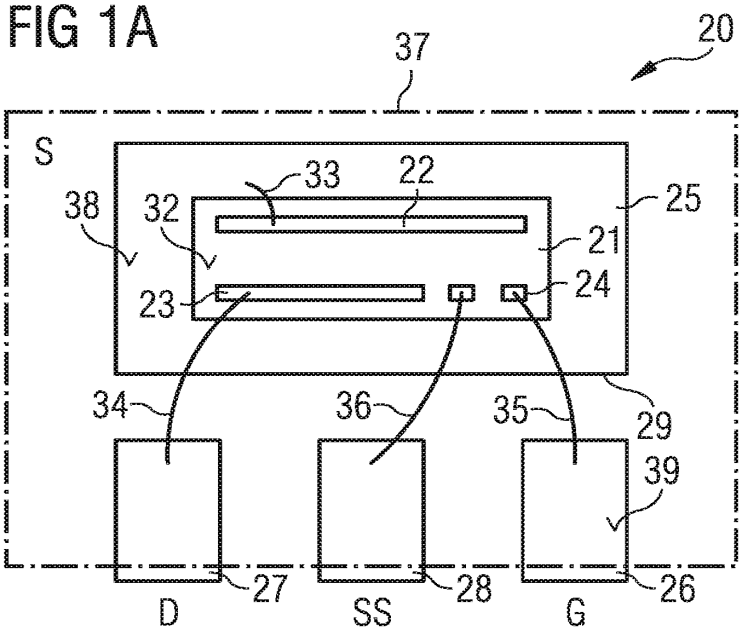

FIG 1B

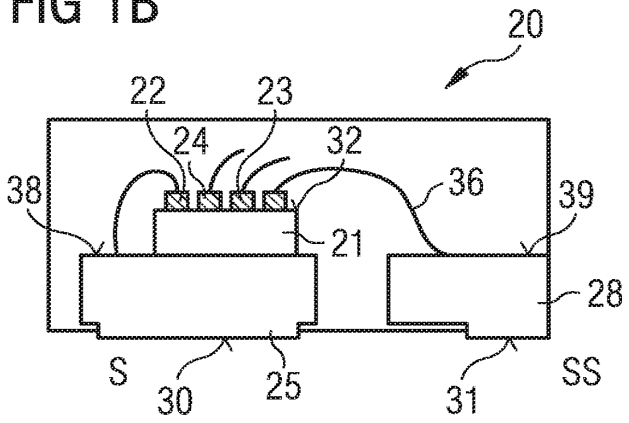

FIG 2

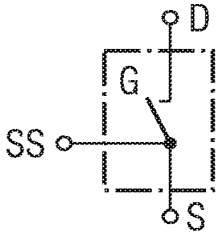

FIG 3

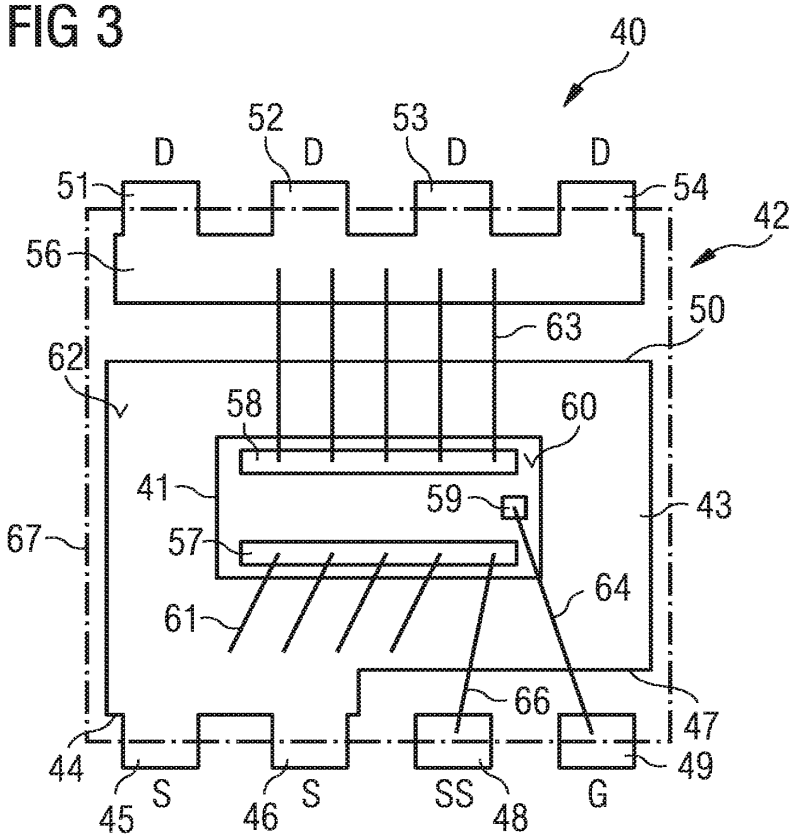
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FIG 4

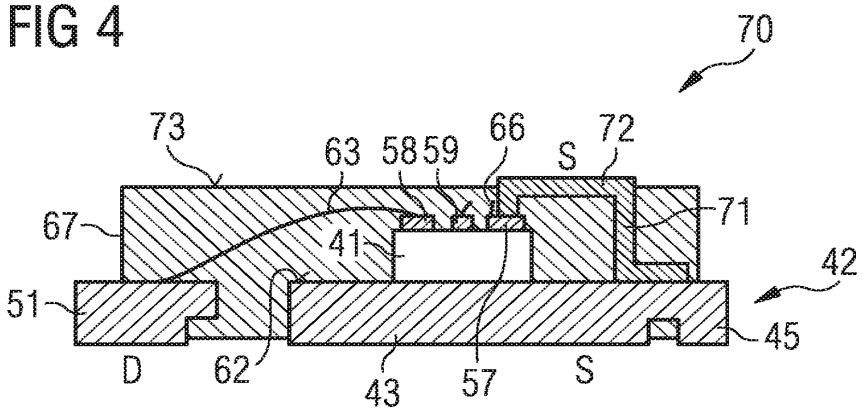
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FIG 5

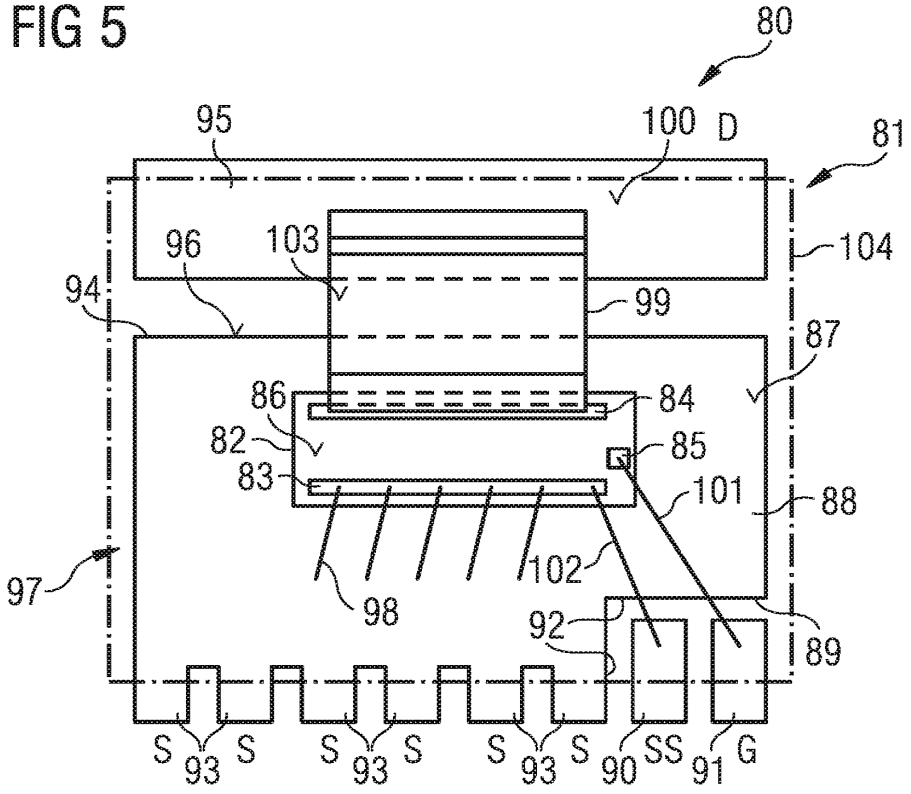
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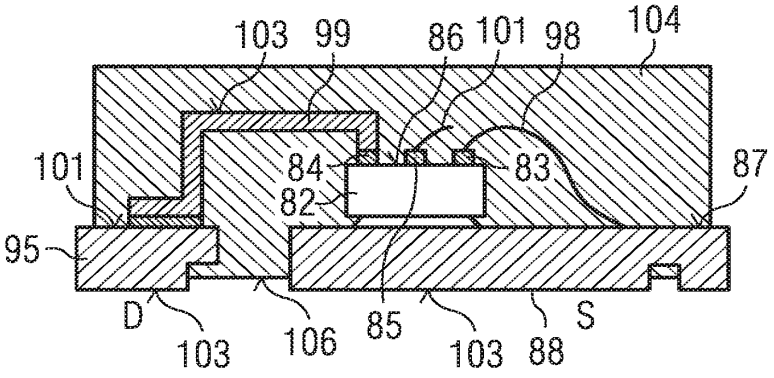
FIG 6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Replacement Sheet 4/8

FIG 7

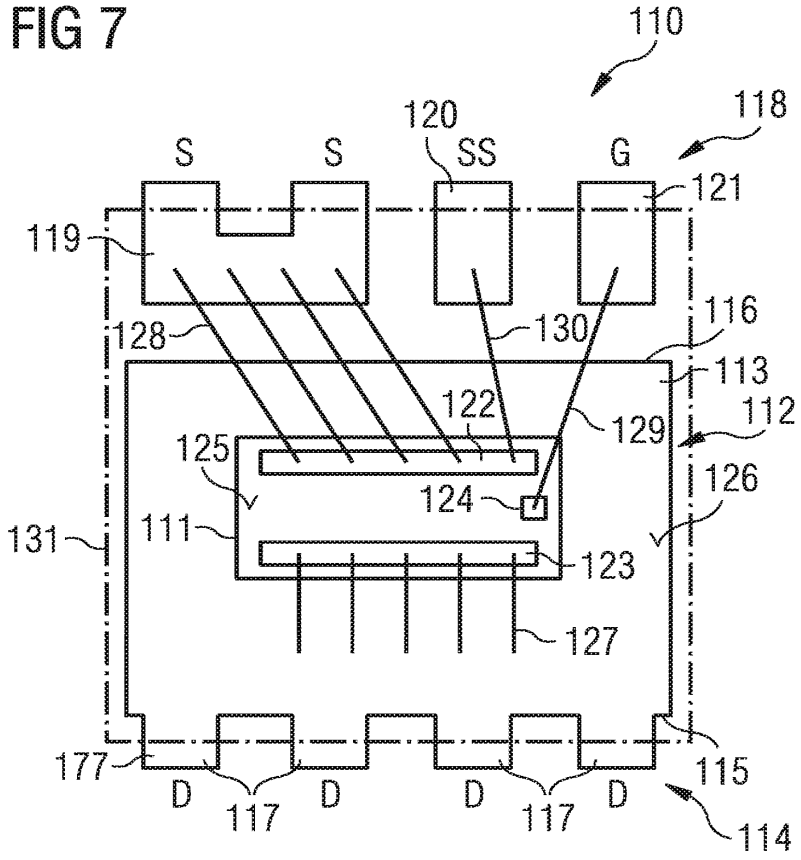
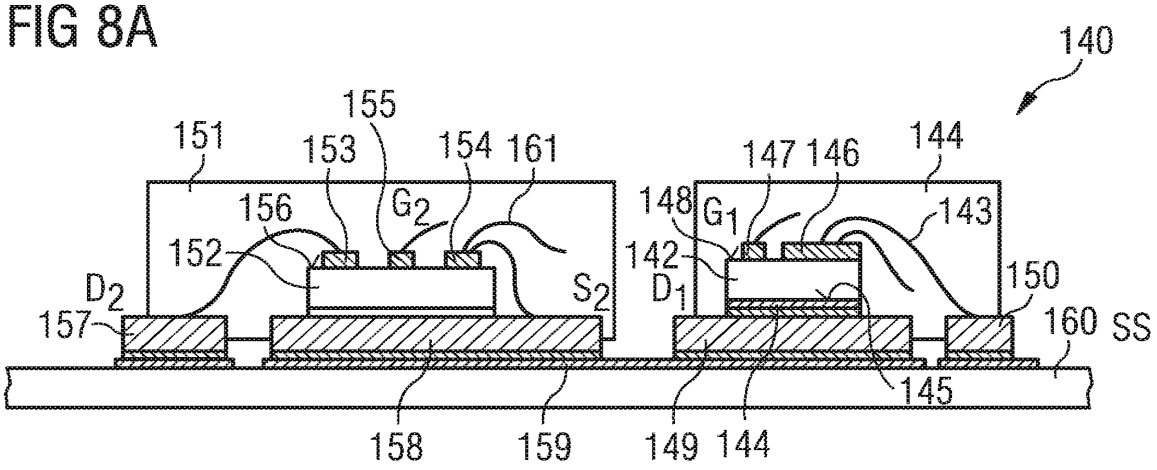


FIG 8A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G_2
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G_1
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S_2
D_1
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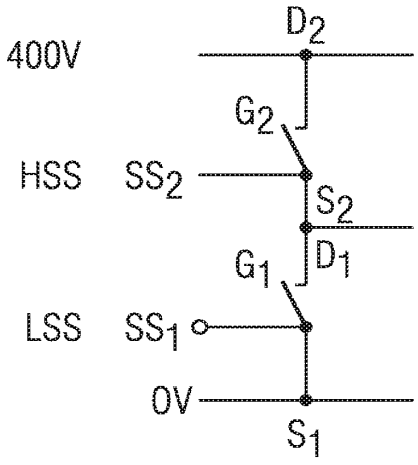
144

FIG 8B


D_2
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G_2
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SS_2
S_2
G_1
D_1
LSS
SS_1
0V
S_1

Replacement Sheet 6/8

FIG 9

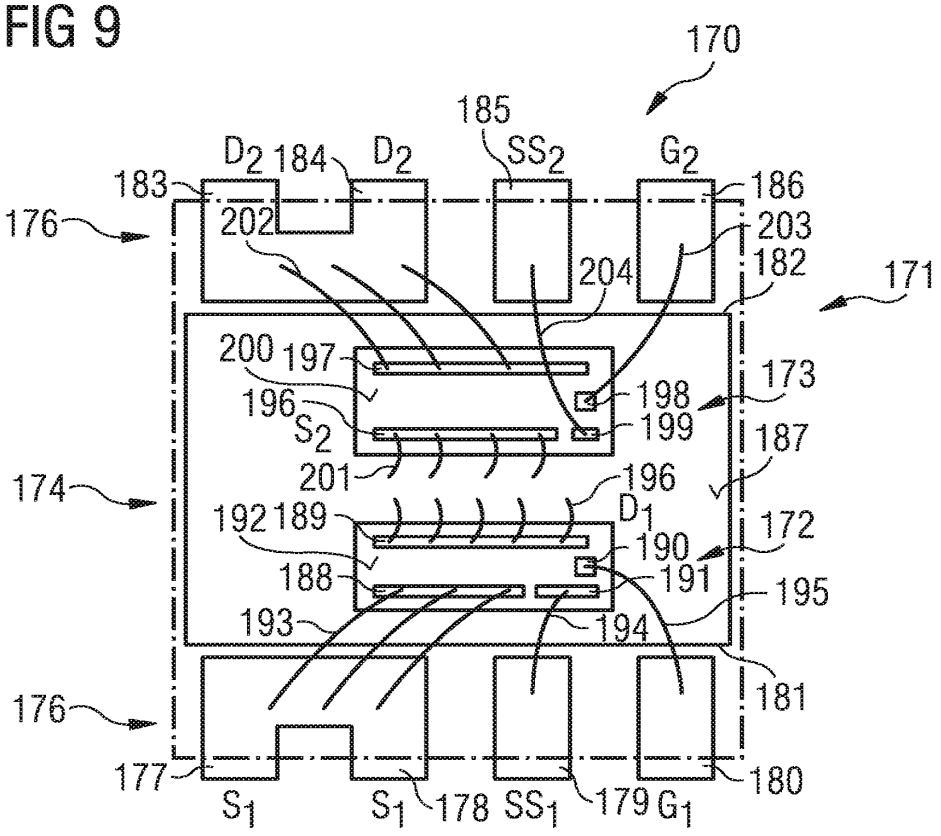


FIG 10A

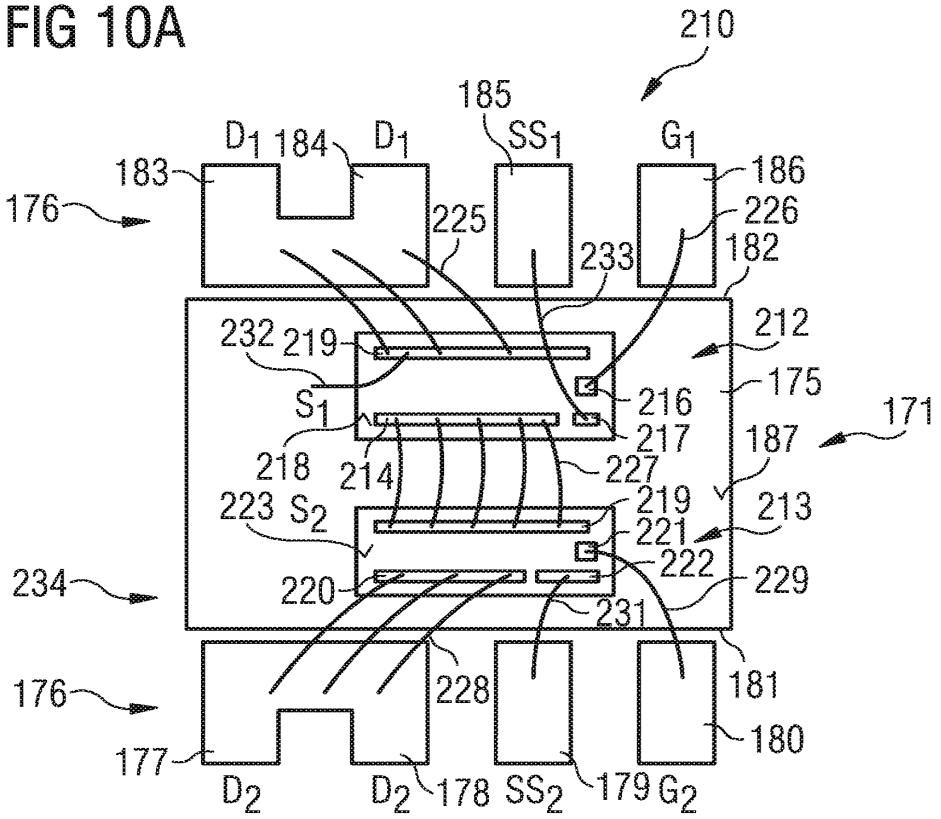
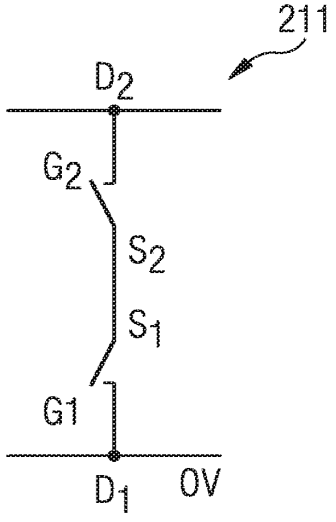


FIG 10B



Replacement Sheet 8/8

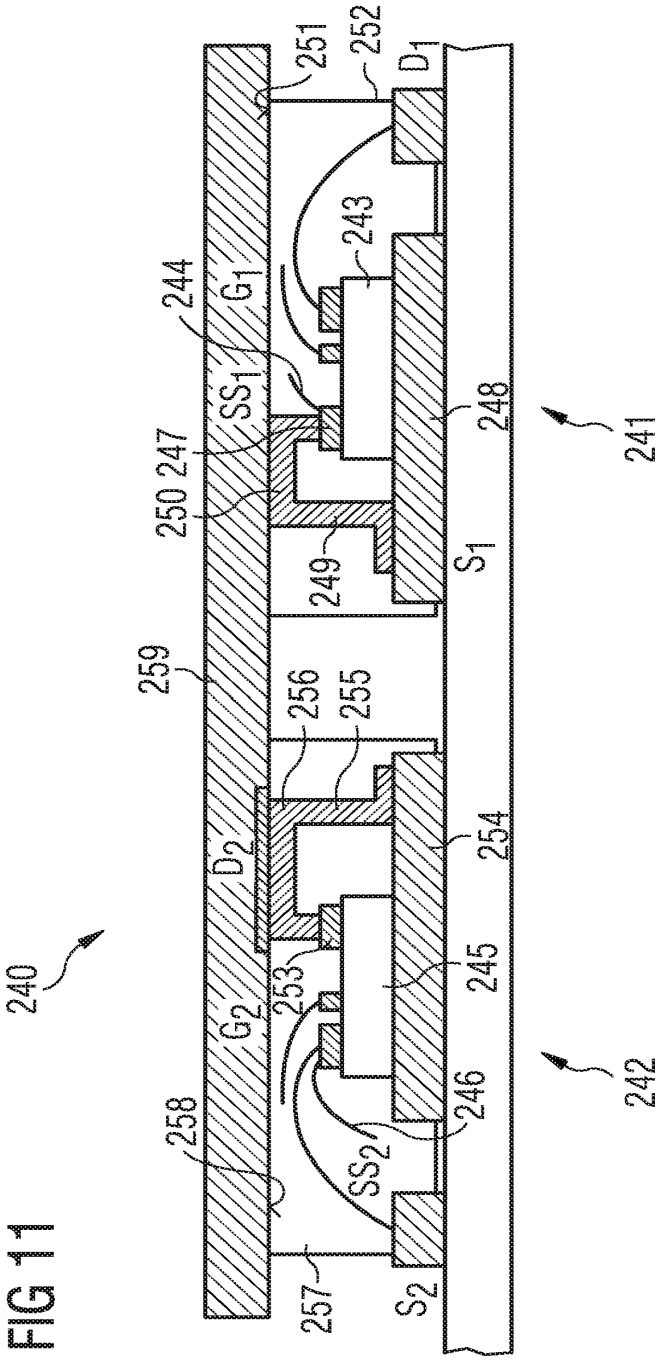


FIG 11

Electronic Acknowledgement Receipt	
EFS ID:	30403105
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Parthiban A. Mathavan/Lindsey Shaw
Filer Authorized By:	Parthiban A. Mathavan
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	19-SEP-2017
Filing Date:	18-JAN-2016
Time Stamp:	10:34:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	1012-1287_Response_to_Office_Action_of_2017-06-23.pdf	60410 a1032632e9014e8010804b60d6614d2d2974e872	no	12

Warnings:

Information:					
2	Drawings-only black and white line drawings	1012-1287_Replacement_Drawings.pdf	684375 a6dc683d29b49e1bae94b201b527c72f380657a3	no	8
Warnings:					
Information:					
			Total Files Size (in bytes):	744785	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US

CONFIRMATION NO. 2194

57579
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

PUBLICATION NOTICE

OC000000092912749

Title: Electronic Component and Switch Circuit

Publication No.US-2017-0207306-A1
Publication Date:07/20/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

57579 7590 06/23/2017

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER
RETEBO, METASEBIA T

ART UNIT	PAPER NUMBER
2842	

NOTIFICATION DATE	DELIVERY MODE
06/23/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

official@mbhiplaw.com

Office Action Summary	Application No. 14/997,914	Applicant(s) OTREMBA ET AL.	
	Examiner METASEBIA RETEBO	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/20/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) *9* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-8 and 10-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/18/2016* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

1. Applicant's election without traverse of Species II, shown in figure 3, reading on claims 1-8 and 10-20 in the reply filed on 03/20/2017 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(k) because the scale to which the drawing is made not large enough to show the mechanism without crowding.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of 35 U.S.C. 112(f):

> (f) Element in Claim for a Combination. – An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

The following is a quotation of pre-AIA 35 U.S.C. 112, sixth paragraph:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

Use of the word "means" (or "step for") in a claim with functional language creates a rebuttable presumption that the claim element is to be treated in accordance with 35 U.S.C. 112(f) (pre-AIA 35

U.S.C. 112, sixth paragraph). The presumption that 35 U.S.C. 112(f) (pre-AIA 35 U.S.C. 112, sixth paragraph) is invoked is rebutted when the function is recited with sufficient structure, material, or acts within the claim itself to entirely perform the recited function.

Absence of the word "means" (or "step for") in a claim creates a rebuttable presumption that the claim element **is not** to be treated in accordance with 35 U.S.C. 112(f) (pre-AIA 35 U.S.C. 112, sixth paragraph). The presumption that 35 U.S.C. 112(f) (pre-AIA 35 U.S.C. 112, sixth paragraph) is not invoked is rebutted when the claim element recites function but fails to recite sufficiently definite structure, material or acts to perform that function.

Claim elements in this application that use the word "means" (or "step for") are presumed to invoke 35 U.S.C. 112(f) except as otherwise indicated in an Office action. Similarly, claim elements that do not use the word "means" (or "step for") are presumed not to invoke 35 U.S.C. 112(f) except as otherwise indicated in an Office action.

Claim 20 is presumed to invoke 35 U.S.C. 112(f) (pre-AIA 35 U.S.C. 112, sixth paragraph) except as otherwise indicated in an Office action.

Claim Rejections - 35 USC § 102

4. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

6. *Claim 1 is rejected under 35 U.S.C. 102(a) (1) as being anticipated by Otremba et al. (US Pub. No. 2009/0212284 and Otremba hereinafter)*

Regarding claim 1, *Otremba* discloses an apparatus [see figures 1-9]; comprising: a compound semiconductor transistor device comprising a first current electrode [12], a second current electrode [14] and a control electrode [11]; a die pad [22]; and a first lead [16], a second lead [17] and a third lead [18], wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad [par. 25], wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality [par. 47].

Claim Rejections - 35 USC § 103

7. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

8. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

9. *Claims 1-6, 8 and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otremba et al. Otremba et al. (US Pub. No. 2015/0115313 and Otremba hereinafter) in view of Lui et al (US 2011/0049580 and Lui hereinafter)*

Regarding claim 1, *Otremba* discloses an apparatus [see figures 1-5]; comprising: a compound semiconductor transistor device [40, fig. 4] comprising a first current electrode [50, fig. 4], a second current electrode [46, fig. 4] and a control electrode [49, fig. 4]; a die pad [42, fig. 4]; and a first lead [66, fig. 4], a second lead [67, fig. 4] and a third lead [64, fig. 4], wherein the first lead and the second lead are

spaced at a distance from the die pad [see fig. 4], wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad [*drain electrode 50 is positioned on the lower surface 51 of the first transistor 41 and is mounted on, and electrically coupled to an upper surface 52 of the first die pad 42, par. 35*], the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality [third lead 64 coupled to 40]. *Otremba does not teach* the third lead is spaced at a distance from the die pad.

However, Lui teaches [see fig. 2A and 2B] leads 30b, 30c and 30d are spaced at a distance from the semiconductor die. In view of such teaching, it would have been obvious to one of ordinary skill in the art before the effective filling date of the claimed invention to *Otremba* semiconductor device to provide a lead space at a distance from semiconductor die pads to utilize well known capable option, since it has been held to be within the general skill of a worker in the art to select a known package on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 227 F.2d 197, 125 USPQ416 (CCPA 1960).

Regarding claim 2, Otremba in view of Lui discloses an apparatus [see figures 1-5]; wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device [par. 23].

Regarding claim 3, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz [par. 14-15].

Regarding claim 4, *Otremba in view of Lui* discloses an apparatus [see figures 1-5], further comprising a housing [60, fig. 4], wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

Regarding claim 5, *Otremba in view of Lui* discloses an apparatus [see figures 1-5], wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad [par. 12, 24, 40].

Regarding claim 6, *Otremba in view of Lui* discloses an apparatus [see figures 1-5], wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad [par. 12].

Regarding claim 8, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip [73, fig. 4].

Regarding claim 10, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing [73, fig. 4].

Regarding claim 12, *Otremba* discloses an apparatus [see figures 1-5], comprising: a first transistor device [41] comprising a compound semiconductor, a first current electrode [50, fig. 4], a second current electrode [46, fig. 4] and a control electrode [49, fig. 4], a die pad [42, fig. 4], a first lead [66, fig. 4], a second lead [67, fig. 4], and a third lead [64, fig. 4], the first lead and the second lead lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad [*drain electrode 50 is positioned on the lower surface 51 of the first transistor 41 and is mounted on, and electrically coupled to an upper surface 52 of the first die pad 42, par. 35*] , the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provides a source sensing functionality [par. 20,27, 30, 44]; and a second transistor device [43, fig. 4], wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device [par. 24-27]]. *Otremba does not teach* the third lead is spaced at a distance from the die pad.

However, Lui teaches [see fig. 2A and 2B] leads 30b, 30c and 30d are spaced at a distance from the semiconductor die. In view of such teaching, it would have been obvious to one of ordinary skill in the art before the effective filling date of the claimed invention to *Otremba* semiconductor device to provide a lead space at a distance from semiconductor die pads to utilize well known capable option, since it has been held to be within the general skill of a worker in the art to select a known package on the basis of its

suitability for the intended use as a matter of obvious design choice. In re Leshin, 227 F.2d 197, 125 USPQ416 (CCPA 1960).

Regarding claim 13, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein a drain of the first transistor device and a source of the second transistor device are coupled to a common die pad.

Regarding claim 14, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the first transistor device is housed in a package comprising a first die pad [42, fig. 4] coupled to a drain of the first transistor device [50, fig. 4] and the second transistor device is housed in a package comprising a second die pad [44, fig. 4] coupled to a source [47, fig. 4] of the second transistor device.

Regarding claim 15, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the first die pad and the second die pad are mounted on a common conductive layer.

Regarding claim 16, *Otremba* discloses an apparatus [see figures 1-5], wherein a first contact clip [73] is coupled to one of a source and a drain of the first transistor device and a second contact clip [74] is coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.

Regarding claim 17, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.

Regarding claim 18, Otremba in view of Lui discloses an apparatus [see figures 1-5], wherein a source of the first transistor device is coupled to a source of the second transistor device [the conductive connector 45 is provided, in the form of a clip which extends between the source electrode 46 of the first transistor 41 and the source electrode 47 of the second transistor 43, par. 39].

Regarding claim 19 recites the corresponding claim limitations in claims 1-4, therefore is rejected for the same reasoning as stated above.

10. *Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over* Otremba et al. in view of Lui et al.

With respect to claim 7, Otremba in view of Lui teaches all the features with respect to claim 1 as outlined above. *Otremba* does not explicitly teach wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

It would have been obvious to one having ordinary skill in the art at the time the invention was to utilize plurality of bond wires or a contact clip to couple the first current electrode is coupled to the die pad. A person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. KSR Int'l Co v. Teleflex Inc

With respect to claim 11, *Otremba* teaches all the features with respect to claim 1 as outlined above. *Otremba* does not explicitly teach, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to *Otremba* semiconductor device package, since it has been held to be within the general skill of a worker in the art to select a known package on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 227 F.2d 197, 125 USPQ416 (CCPA 1960).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to METASEBIA RETEBO whose telephone number is (571)272-9299. The examiner can normally be reached on Monday - Friday 7:30am to 5:00pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. R. /
Examiner, Art Unit 2842
/LINCOLN DONOVAN/
Supervisory Patent Examiner, Art Unit 2842

Notice of References Cited	Application/Control No. 14/997,914	Applicant(s)/Patent Under Reexamination OTREMBA ET AL.	
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*	B	US-2009/0212284 A1	08-2009	Otremba; Ralf	H01L23/4952	257/48
*	C	US-2011/0049580 A1	03-2011	Lui; Sik	H01L23/49575	257/262
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	323	(("LEE") near3 ("Teck")).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 10:56
L2	4	1 and block$4 near voltage	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 10:58
L3	19	("20060033122" | "20060237825" | "20070166877" | "20070216390" | "20080054422" | "20080304305" | "20090058500" | "20090218676" | "20100213510" | "20110221008" | "20120121304" | "20120161304" | "20120262828" | "20130107583" | "6020636" | "7227198" | "7605570" | "8039954" | "8723238").PN. OR ("9263563").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 11:00
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L5	7	("7042730" | "7095099" | "20040004272" | "5616955" | "20050280998" | "6933593" | "6995467").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 14:00
L9	26	("20020050635" | "20020125550" | "20040232538" | "20050056914" | "20050218498" | "20060118927" | "20060145319" | "20060186525" | "20060202319" | "20070181989" | "6166434" | "6271056" | "6927483" | "6943455" | "7271470").PN. OR ("7800208").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 14:24
L10	110	(semiconductor near transistor) same block$4 near voltage	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 14:28
L11	3	(semiconductor near transistor) same block$4 near voltage.clm.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/16 14:33
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S5	3	("20050269674" | "20090212284" | "20130235636").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/14 11:47
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S7	17	("20080017907" | "5396085" | "6144093" | "7800217" | "20030098462" | "6593622" | "6900537" | "7443014" | "7939857" | "6404050" | "7825435" | "7348612" | "7745930" | "7501670" | "7569870" | "7547964" | "6768146").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/14 16:44
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S9	111	(("SCHIESS") near3 ("Klaus")).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/14 17:31
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S11	1	"9373566".pn.	US-	OR	ON	2017/06/15

			PGPUB; USPAT			16:37
S12	6	("20060017174" | "20070215996" | "20120299119" | "6066515" | "6404041" | "8044523").PN. OR ("9373566").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/15 16:37

EAST Search History (Interference)

<This search history is empty>

6/16/2017 7:45:08 PM
C:\Users\mretebo\Documents\EAST\Workspaces\14997914-1.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Field

Substitute for PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	14/997,914
Filing Date	Jan 18, 2016
First Named Inventor	Ralf Otremba
Art Unit	2842
Examiner Name	DONOVAN, LINCOLN D
Attorney Docket Number	1012-1287 / 2015P51742 US

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code [1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7250641	B2	2007-07-31	Saito, Wataru et al.	
		7838097	B2	2010-11-23	Hayashida, Naoki et al.	

U.S. PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code [1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		20110049580	A1	2011-03-03	Lui, Sik et al.	
		20110101466	A1	2011- 05-05	Wu, Yifeng	
		20120022332	A1	2012-01-26	De Domenico, Andrea	
		20120223322	A1	2012-09-06	Lin, Heny et al.	
		20140252577	A1	2014-09-11	Otremba, Ralf et al.	Corresponds to DE102014102910 cited below
		20150116025	A1	2015-04-30	Ralf, Otremba et al.	

FOREIGN PATENT DOCUMENTS

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.T.R/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Field

Substitute for PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14/997,914
	Filing Date	Jan 18, 2016
	First Named Inventor	Ralf Otremba
	Art Unit	2842
	Examiner Name	DONOVAN, LINCOLN D
	Attorney Docket Number	1012-1287 / 2015P51742 US

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T[5]
		102014102910	DE	A1	2014-09-11	Infineon Technologies Austria AG	Corresponds to US20140252577 cited above	

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EXAMINER SIGNATURE

Examiner Signature	/METASEBIA T RETEBO/	Date Considered	06/16/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
[4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.T.R/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Field

Substitute for PTO/SB/08a (01-10)
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	Art Unit	2842
	Examiner Name	DONOVAN, LINCOLN D
	Attorney Docket Number	1012-1287 / 2015P51742 US

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e) (1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e) (2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark R. Bilak, Reg. No. 47,423/	Date (YYYY-MM-DD)	2016-08-03
Name/Print	Mark R. Bilak	Registration Number	47,423

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.T.R/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14997914	OTREMBA ET AL.
	Examiner	Art Unit
	METASEBIA RETEBO	2842

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/2003	6/16/2017	MR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
327	434	6/16/2017	MR

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text search. (see search history)	6/16/2017	MR
Inventor and Assignee search EAST and PALM	6/16/2017	MR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 2194

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/997,914	01/18/2016	327	2842	1012-1287 / 2015P51742 US

APPLICANTS
Infineon Technologies Austria AG, Villach, AUSTRIA;

INVENTORS
Ralf Otremba, Kaufbeuren, GERMANY;
Klaus Schiess, Allensbach, GERMANY;

** **CONTINUING DATA** **********

** **FOREIGN APPLICATIONS** **********

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
01/29/2016

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
❑ Yes ☑ No	❑ Yes ☑ No	/METASEBIA T RETEBO/ Examiner's Signature	❑ Met after Allowance MR Initials	GERMANY	13	20	4

ADDRESS

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518
UNITED STATES

TITLE

Electronic Component and Switch Circuit

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
2020	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Otremba	)	
Serial No.: 14/997,914	)	PATENT PENDING
Filed: January 18, 2016	)	Examiner: RETEBO, METASEBIA T
For: Electronic Component and Switch Circuit	)	Group Art Unit: 2842
Docket No: 1012-1287 / 2015P51742 US	)	Confirmation No.: 2194

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

In response to the Restriction Requirement mailed January 26, 2017, Applicant elects Species II of Figure 3 (claims 1-8 and 10-20) without traverse.

In the Office Action, the Examiner requires Applicant to elect one of the following Species:

Species I: the embodiment of Figure 1;
Species II: the embodiment of Figure 3;
Species III: the embodiment of Figure 4; and
Species IV: the embodiment of Figure 7.

The bond wires recited in claims 7 and 8 are illustrated in Figure 3 (and Figure 7). Claim 9 is illustrated in Figure 4. Claim 6 is illustrated in Figure 8a, which is not mentioned in the Restriction Requirement. The contact clip of claim 8 is illustrated in Figures 5 and 6, which are also not mentioned in the Restriction Requirement. The embodiments with two transistors of

claims 12-18 are illustrated in Figures 8-11, which are not mentioned in the Restriction Requirement. As such, claims 1-8 and 10-20 should be examined.

No fees should be required for entry of this response. However, if any fees are required, please charge them to Murphy, Bilak & Homiller, PLLC, Deposit Account No. 50-5650.

Respectfully submitted,
Murphy, Bilak & Homiller, PLLC

/Mark R. Bilak, Reg. No. 47,423/

Dated: March 20, 2017

Mark R. Bilak
Registration No.: 47,423

1255 Crescent Green, Suite 200
Cary, NC 27518
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Facsimile: (919) 948-3357

Electronic Acknowledgement Receipt	
EFS ID:	28675244
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Mark Ronald Bilak/Meredith Lilley
Filer Authorized By:	Mark Ronald Bilak
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	20-MAR-2017
Filing Date:	18-JAN-2016
Time Stamp:	12:59:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	1012-1287_Response_to_Restriction_Requirement_of_2017-01-26.pdf	17149 7509e78108e647cc475b54e52736f7a129a576c2	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	17149

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US	2194

57579 7590 01/26/2017

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER
RETEBO, METASEBIA T

ART UNIT	PAPER NUMBER
2842	

NOTIFICATION DATE	DELIVERY MODE
01/26/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

official@mbhiplaw.com

Office Action Summary	Application No. 14/997,914	Applicant(s) OTREMBA ET AL.	
	Examiner METASEBIA RETEBO	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *2* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/18/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species:

   a) Species I: The embodiment of Figure 1 regarding a device having an electronic component 20 includes a compound semiconductor transistor device 21 which includes a first current electrode 22, a second current electrode 23 and a control electrode 24. The electronic component 20 further includes a die pad 25, a first lead 26, a second lead 27 and a third lead 28. The first lead 26, the second lead 27 and the third lead 28 are spaced apart from the die pad 25. The first lead, 26, the second lead 27, and the third lead 28 are arranged adjacent and spaced apart from a single side face 29 of the die pad 25. The control electrode 24 is coupled to the first lead 26, the first current electrode 22 is coupled to the die pad 25, the second current electrode 23 is coupled to the second lead 27 and the third lead 28 is coupled to the compound semiconductor transistor device 21 and provides a source sense functionality.

   b) Species II: The embodiment of Figure 3 regarding a device having an electronic component 40 includes a compound semiconductor transistor device 41 which, in this particular embodiment, is a Group III-nitride based High Electron Mobility Transistor (HEMT). The electronic component 40 includes a package 42 having a ThinPak 8x8 package outline. The package 42 includes a die pad 43 having an L-shaped form which extends on one side face 44 to provide two substantially parallel leads 45, 46 and forms a cutaway 47 in which two further leads 48, 49 are arranged. The further leads 48, 49 are spaced apart at a distance form the side face 44 of the die pad 43 and are arranged in a row adjacent the lead 46. On the opposing side 50 of die pad 43, the package 42 includes four leads 51, 52, 53, 54 which are electrically coupled by a bar 56 extending substantially parallel and spaced apart form the side face 50 of the die pad 43.

The lower surfaces of the leads are 45, 46, 48, 49, 51, 52, 53, 54 arranged at two opposing sides of the electronic component 40 and provide surface mountable contact pads. The lower surface of the die pad 43 is substantially parallel with the lower surfaces of the leads and also provides a surface mountable contact pad for the electronic component 40.

c) Species III: The embodiment of Figure 4 regarding a device having an electronic component 70, therefore, includes a die pad 43, and leads arranged adjacent two opposing sides of the die pad 43 of which a drain lead 51 and the source lead 45 which extends from the die pad 43. The electronic component 70 also includes a HEMT 41 which is mounted on the upper surface 62 of the die pad 43. The drain pad 58 is electrically coupled to the lead 51 by bond wires 63. The gate pad 59 is electrically coupled to a gate lead and a source sense functionality is provided by a bond wire 66 extending to a further lead. The gate lead and the further lead are spaced apart from the die pad 43. The electronic component 70 differs from the electronic component 40 of the second embodiment in the form and arrangement of the electrical connection between the source pad 57 of the transistor device 41 and the die pad 43.

d) Species IV: The embodiment of Figure 7 regarding a device having an electronic component 110 includes a compound semiconductor device 111 and a leadframe 112 including a die pad 113 and a plurality of leads 114 arranged on two opposing sides 115, 116 of the die pad 113. Four leads 117 extend from the die pad 113 on the first side 115 and a further four leads 118 are arranged adjacent and spaced apart from the opposing side 116 of the die pad 113. Two of the four leads 118 are coupled together by a connector strip 119. Two leads 120, 121 are arranged adjacent the connector strip 119 such that the four leads 118 are arranged in a row and substantially parallel to one another.

The species are independent or distinct because of the reasons listed above. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species** or grouping of patentably indistinct species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or

identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to METASEBIA RETEBO whose telephone number is (571)272-9299. The examiner can normally be reached on Monday - Friday 7:30am to 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. R. /
Examiner, Art Unit 2842
/LINCOLN DONOVAN/
Supervisory Patent Examiner, Art Unit 2842

Substitute for PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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	Art Unit	2842
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	Attorney Docket Number	1012-1287 / 2015P51742 US

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code [1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7250641	B2	2007-07-31	Saito, Wataru et al.	
		7838097	B2	2010-11-23	Hayashida, Naoki et al.	

U.S. PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code [1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		20110101466	A1	2011- 05-05	Wu, Yifeng	
		20120022332	A1	2012-01-26	De Domenico, Andrea	
		20120223322	A1	2012-09-06	Lin, Heny et al.	
		20140252577	A1	2014-09-11	Otremba, Ralf et al.	Corresponds to DE102014102910 cited below
		20150116025	A1	2015-04-30	Ralf, Otremba et al.	

FOREIGN PATENT DOCUMENTS

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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	Application Number	14/997,914
	Filing Date	Jan 18, 2016
	First Named Inventor	Ralf Otremba
	Art Unit	2842
	Examiner Name	DONOVAN, LINCOLN D
	Attorney Docket Number	1012-1287 / 2015P51742 US

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T[5]
		102014102910	DE	A1	2014-09-11	Infineon Technologies Austria AG	Corresponds to US20140252577 cited above	

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
[4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

Substitute for PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14/997,914
	Filing Date	Jan 18, 2016
	First Named Inventor	Ralf Otremba
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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e) (1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e) (2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark R. Bilak, Reg. No. 47,423/	Date (YYYY-MM-DD)	2016-08-03
Name/Print	Mark R. Bilak	Registration Number	47,423

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Espacenet

Bibliographic data: DE102014102910 (A1) — 2014-09-11

Chipträgerstruktur, Chipgehäuse und Verfahren zu deren Herstellung

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Applicant(s): INFINEON TECHNOLOGIES AUSTRIA [AT] + (INFINEON TECHNOLOGIES AUSTRIA AG)

Classification: - international: ***H01L21/50; H01L23/13; H01L23/31; H01L23/495***
- cooperative: **H01L21/561**; **H01L23/4334**; **H01L23/49562**; **H01L23/49575**; **H01L23/49861**; **H01L24/19**; **H01L24/20**; **H01L24/89**; **H01L24/97**; H01L2224/24137; H01L2224/48091; H01L2224/48247; H01L2224/49111; H01L2924/07802; H01L2924/1305; H01L2924/13055; H01L2924/1306; H01L2924/13062; H01L2924/13091; H01L2924/181; Y10T29/49002 more

Application number: DE201410102910 20140305

Priority number(s): US201313784923 20130305

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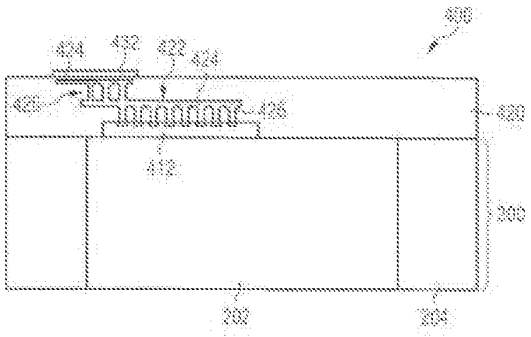
Abstract of DE102014102910 (A1)

Verschiedene Ausführungsformen stellen eine Chipträgerstruktur (200) bereit. Die Chipträgerstruktur (200) kann einen strukturierten metallischen Chipträger (202); ein Einkapselungsmaterial (204), das die Struktur (200) zumindest teilweise ausfallt; wobei die Hauptoberflächen des metallischen Chipträgers (202) frei von Einkapselungsmaterial (204) sind, umfassen.



(19) Deutsches Patent- und Markenamt

(10) **DE 10 2014 102 910 A1** 2014.09.11

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H01L 23/495 (2006.01)
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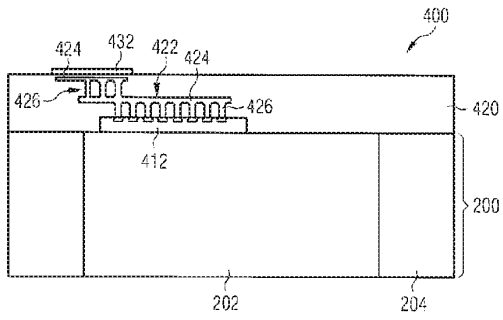
Prüfungsantrag gemäß § 44 PatG ist gestellt.

Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

(54) Bezeichnung: **Chipträgerstruktur, Chipgehäuse und Verfahren zu deren Herstellung**

(57) Zusammenfassung: Verschiedene Ausführungsformen stellen eine Chipträgerstruktur (200) bereit. Die Chipträgerstruktur (200) kann einen strukturierten metallischen Chipträger (202); ein Einkapselungsmaterial (204), das die Struktur (200) zumindest teilweise ausfallt; wobei die Hauptoberflächen des metallischen Chipträgers (202) frei von Einkapselungsmaterial (204) sind, umfassen.



Beschreibung

[0001] Verschiedene Ausführungsformen betreffen allgemein eine Chipträgerstruktur, ein Chipgehäuse, ein Verfahren zur Herstellung einer Chipträgerstruktur und ein Verfahren zur Herstellung eines Chipgehäuses.

[0002] Leistungshalbleiterchips können in eine Elektronikeinheit integriert werden, z. B. in ein Gehäuse für Durchsteckmontage (THP) oder eine Vorrichtung für Oberflächenmontage (SMD).

[0003] Gegenwärtig können Standardleistungsgehäuse, z. B. TO218, TO220, TO247, TO251, für Leistungshalbleiterchips (z. B. Hochvolt-(HV)-Halbleiterchips) in Leistungsanwendungen, z. B. für Hochspannungsanwendungen größer als 200 V, eingesetzt werden.

[0004] Doch können diese Standardleistungsgehäuse aufgrund der Gehäuseinduktivitäten [nH] bei den in der Zukunft wachsenden Anforderungen an die Stromstärke [A] zu beträchtlichen Schaltverlusten (Pswitch [W]) führen.

[0005] **Fig.** 1 zeigt Simulationsergebnisse **100** der Abhängigkeit von Schaltverlusten von der Source-Pin-Induktivität auf einen 45 mOhm J-FET (Junction Gate Field Effect Transistor).

[0006] Wie in **Fig.** 1 dargestellt, erhöhen sich mit steigender Stromstärke die Schaltverluste bei verschiedenen für einen 45 mOhm J-FET verwendeten Gehäusen TO247, TO220, ThinPAK 8 × 8 und Blade HV. Ebenso ist dargestellt, dass die Schaltverluste bei verschiedenen Gehäusen TO247, TO 220, ThinPAK und Blade HV bei gleicher Stromstärke abnehmen, wobei das Gehäuse TO247 die höchsten Schaltverluste zeigt und das Blade HV-Gehäuse die geringsten Schaltverluste aufweist. Entsprechend lassen sich mit einem optimierten Gehäuse, z. B. den Gehäusen Blade HV und ThinPAK 8 × 8, im Vergleich zu den Gehäusen TO220 und TO247 geringere Schaltverluste erreichen.

[0007] Verschiedene Ausführungsformen stellen eine Chipträgerstruktur bereit. Die Chipträgerstruktur kann einen strukturierten metallischen Chipträger; ein Einkapselungsmaterial, das die Struktur zumindest teilweise ausfüllt; wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial sind, umfassen.

[0008] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger einen Anschlusskamm umfassen.

[0009] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0010] In verschiedenen Ausführungsformen kann die Einkapselungsstruktur ein Laminat umfassen.

[0011] In verschiedenen Ausführungsformen kann der Chip frei von Einkapselungsmaterial sein, das die Struktur zumindest teilweise ausfüllt.

[0012] Nach verschiedenen Ausführungsformen kann das Verfahren weiterhin einen Klebstoff zwischen dem Chip und dem strukturierten metallischen Chipträger bilden, um den Chip an den strukturierten metallischen Chipträger anzukleben. Bei dem Klebstoff kann es sich um einen isolierenden Klebstoff oder einen elektrisch leitenden Klebstoff handeln.

[0013] Verschiedene Ausführungsformen des oben beschriebenen Chipgehäuses gelten analog für das Verfahren zur Herstellung eines Chipgehäuses.

[0014] Verschiedene Ausführungsformen stellen eine Chipträgerstruktur bereit. Die Chipträgerstruktur kann einen strukturierten metallischen Chipträger; ein Einkapselungsmaterial, das die Struktur zumindest teilweise ausfüllt; wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial sind, umfassen.

[0015] Der strukturierte metallische Chipträger kann einen Anschlusskamm umfassen. Der Anschlusskamm kann aus einem Metall oder einer Metalllegierung gefertigt sein, die z. B. einen Werkstoff umfasst, der aus der Gruppe bestehend aus: Kupfer (Cu), Eisen-Nickel (FeNi), Stahl und dergleichen ausgewählt ist. Der metallische Chipträger kann eine Mehrzahl von Teilen oder Blöcken umfassen, wobei die mehreren Teile oder Blöcke durch das Isoliermaterial voneinander isoliert sind.

[0016] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial Pressmasse oder ein vergleichbares Material umfassen. Das Einkapselungsmaterial kann eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0017] In verschiedenen Ausführungsformen kann die Chipträgerstruktur als Leistungs-Chipträgerstruktur für das Tragen eines oder mehrerer Leistungs-Chips darauf ausgestaltet sein.

[0018] In verschiedenen Ausführungsformen kann die Chipträgerstruktur weiterhin eine an eine der Hauptoberflächen des metallischen Chipträgers angebrachte Folie umfassen. Die Folie kann zur Kühlung oder Trennung verwendet werden.

[0019] Verschiedene Ausführungsformen stellen ein Chipgehäuse bereit. Das Chipgehäuse kann eine

Chipträgerstruktur umfassen. Die Chipträgerstruktur kann einen strukturierten metallischen Chipträger und ein Einkapselungsmaterial, das die Struktur zumindest teilweise ausfüllt; wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial sind, umfassen. Das Chipgehäuse kann weiterhin einen über der Chipträgerstruktur angeordneten Chip und eine über dem Chip gebildete Einkapselungsstruktur umfassen, wobei die Einkapselungsstruktur eine elektrisch leitende Umverteilungsstruktur umfassen kann. Das Chipgehäuse kann mindestens ein über der Einkapselungsstruktur gebildetes Kontaktpad umfassen, wobei das zumindest eine Kontaktpad über die elektrisch leitende Umverteilungsstruktur elektrisch an den Chip gekoppelt ist.

[0020] Der strukturierte metallische Chipträger kann einen Anschlusskamm umfassen. Das Einkapselungsmaterial kann eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen. In verschiedenen Ausführungsformen kann die Chipträgerstruktur als Leistungs-Chipträgerstruktur für das Tragen eines oder mehrerer Leistungs-Chips darauf ausgestaltet sein.

[0021] In verschiedenen Ausführungsformen kann das Chipgehäuse weiterhin einen Klebstoff zwischen dem Chip und dem strukturierten metallischen Chipträger umfassen, um den Chip an den strukturierten metallischen Chipträger anzukleben. In verschiedenen Ausführungsformen kann es sich bei dem Klebstoff um einen isolierenden Klebstoff handeln; in diesem Fall kann die Chipträgerstruktur als Kühlstruktur verwendet werden. In verschiedenen Ausführungsformen kann der Klebstoff ein elektrisch leitender Klebstoff sein; in diesem Fall kann die Chipträgerstruktur zum elektrischen Verbinden des Anschlusskontakts des Chips mit dem strukturierten metallischen Chipträger verwendet werden.

[0022] In verschiedenen Ausführungsformen kann der Chip frei von Einkapselungsmaterial sein, das die Struktur zumindest teilweise ausfüllt. In verschiedenen Ausführungsformen kann das Einkapselungsmaterial, z. B. die Vergussmasse, lediglich den strukturierten metallischen Chipträger umgeben oder kann zusätzlich den Klebstoff für das Die-Bonden des Chips an die Chipträgerstruktur umgeben.

[0023] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger als eine Leistungs-Chipträgerstruktur ausgestaltet sein. Zum Beispiel kann ein Leistungs-Chip an dem strukturierten metallischen Chipträger angebracht sein. Der Leistungs-Chip kann einen Leistungsdiodenchip und/oder einen Leistungstransistorchip (z. B. einen Leistungs-MOSFET (Metalloxidhalbleiterfeldeffekttransistor), einen JFET (Sperrschichtfeldeffekttransistor), einen IGBT (Bipolartransistor mit isoliertem Gate), einen Leistungsbipolartransistor oder dergleichen umfassen.

[0024] In verschiedenen Ausführungsformen kann die über dem Chip gebildete Einkapselungsstruktur ein Laminat umfassen. Das Laminat kann Polymermaterial mit Glasfasern umfassen.

[0025] In verschiedenen Ausführungsformen kann die elektrisch leitende Umverteilungsstruktur eine oder mehrere elektrisch leitende Schichten (auch als Umverteilungsschichten bezeichnet) und Kontaktlöcher für die elektrische Kopplung einer oder mehrerer elektrisch leitender Schichten mit dem Chip und für die elektrische Kopplung einer oder mehrerer elektrisch leitender Schichten miteinander umfassen.

[0026] Verschiedene Ausführungsformen stellen ein Verfahren zur Herstellung einer Chipträgerstruktur bereit. Das Verfahren kann das Strukturieren eines metallischen Chipträgers; das zumindest teilweise Ausfüllen der Struktur mit Einkapselungsmaterial umfassen; wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial bleiben.

[0027] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger einen Anschlusskamm umfassen.

[0028] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0029] Verschiedene Ausführungsformen stellen ein Verfahren zur Herstellung eines Chipgehäuses bereit. Das Verfahren kann das Herstellen einer Chipträgerstruktur umfassen; wozu das Strukturieren eines metallischen Chipträgers; das zumindest teilweise Ausfüllen der Struktur mit Einkapselungsmaterial gehören kann; wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial bleiben. Das Verfahren kann weiterhin das Anordnen eines Chips über der Chipträgerstruktur; das Bilden einer Einkapselungsstruktur über dem Chip, wobei die Einkapselungsstruktur eine elektrisch leitende Umverteilungsstruktur ist; und das Bilden mindestens ein Kontaktpad über der Einkapselungsstruktur zur elektrischen Kopplung des zumindest einen Kontaktpads über die elektrisch leitende Umverteilungsstruktur an den Chip umfassen.

[0030] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger einen Anschlusskamm umfassen.

[0031] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0032] In verschiedenen Ausführungsformen kann die Einkapselungsstruktur ein Laminat umfassen.

[0033] In verschiedenen Ausführungsformen kann der Chip frei von Einkapselungsmaterial sein, das die Struktur zumindest teilweise ausfüllt.

[0034] Nach verschiedenen Ausführungsformen kann das Verfahren weiterhin einen Klebstoff zwischen dem Chip und dem strukturierten metallischen Chipträger bilden, um den Chip an den strukturierten metallischen Chipträger anzukleben. Bei dem Klebstoff kann es sich um einen isolierenden Klebstoff oder einen elektrisch leitenden Klebstoff handeln.

[0035] In den Zeichnungen verweisen gleiche Bezugszeichen in den unterschiedlichen Ansichten generell auf die gleichen Teile. Die Zeichnungen sind nicht unbedingt maßstabgerecht, stattdessen wird der Schwerpunkt generell auf die Darstellung der Grundprinzipien der Erfindung gelegt. In der folgenden Beschreibung werden verschiedene Ausführungsformen der Erfindung unter Bezugnahme auf die folgenden Zeichnungen beschrieben, worin:

[0036] **Fig.** 1 Simulationsergebnisse der Abhängigkeit von Schaltverlusten von der Source-Pin-Induktivität auf einem 45 mOhm Sperrschicht-Feldeffekttransistor zeigt.

[0037] **Fig.** 2 eine Chipträgerstruktur gemäß verschiedenen Ausführungsformen zeigt;

[0038] **Fig.** 3 eine Chipträgerstruktur gemäß verschiedenen Ausführungsformen zeigt;

[0039] **Fig.** 4 ein Chipgehäuse gemäß verschiedenen Ausführungsformen zeigt;

[0040] **Fig.** 5A und **Fig.** 5B ein Chipgehäuse gemäß verschiedenen Ausführungsformen zeigen;

[0041] **Fig.** 6 ein Chipgehäuse gemäß verschiedenen Ausführungsformen zeigt;

[0042] **Fig.** 7A ein Gehäuse gemäß verschiedenen Ausführungsformen zeigt; und **Fig.** 7B eine Chipanordnung gemäß verschiedenen Ausführungsformen zeigt;

[0043] **Fig.** 8 eine Kaskadenschaltung gemäß verschiedenen Ausführungsformen zeigt;

[0044] **Fig.** 9 ein Gehäuse gemäß verschiedenen Ausführungsformen zeigt;

[0045] **Fig.** 10 ein Ablaufdiagramm zeigt, das ein Verfahren für die Herstellung einer Chipträgerstruktur gemäß verschiedenen Ausführungsformen darstellt; und

[0046] **Fig.** 11 ein Ablaufdiagramm zeigt, das ein Verfahren für die Herstellung eines Chipgehäuses gemäß verschiedenen Ausführungsformen darstellt.

[0047] In der folgenden ausführlichen Beschreibung wird auf die begleitenden Zeichnungen Bezug genommen, in denen einige bestimmte Details und Ausführungsbeispiele für die Erfindung beispielhaft dargestellt werden.

[0048] Das Wort „beispielhaft" wird hier in der Bedeutung „als Beispiel, Ausprägung oder zur Veranschaulichung dienend" verwendet. Eine hierin „beispielhaft" beschriebene Ausführungsform oder Konstruktion ist nicht unbedingt als bevorzugt oder vorteilhaft gegenüber anderen Ausführungsformen oder Konstruktionen auszulegen.

[0049] Das Wort „über", das in Bezug auf ein aufgedampftes Material „über" einer Seite oder Oberfläche verwendet wird, kann hierin bedeuten, dass das aufgedampfte Material „direkt auf", z. B. in direktem Kontakt mit der jeweiligen Seite oder Oberfläche gebildet wird. Das Wort „über", das in Bezug auf ein aufgedampftes Material „über" einer Seite oder Oberfläche verwendet wird, kann hierin bedeuten, dass das aufgedampfte Material „indirekt auf der jeweiligen Seite oder Oberfläche gebildet wird, wobei eine oder mehrere Schichten zwischen der jeweiligen Seite oder Oberfläche und dem aufgedampften Material angeordnet sind.

[0050] Verschiedene Ausführungsformen bieten eine Chipträgerstruktur mit guter elektrischer und thermischer Leistung, die zur Ausführung eines hochvoltfähigen Gehäuses (z. B. > 200 V) verwendet werden kann. Verschiedene Ausführungsformen bieten auch ein hochvoltfähiges eingebettetes Gehäuse (z. B. > 200 V) für Leistungshalbleiter.

[0051] **Fig.** 2 zeigt eine Chipträgerstruktur **200** gemäß verschiedenen Ausführungsformen.

[0052] Die Chipträgerstruktur **200** kann einen strukturierten metallischen Chipträger **202** (der vor der Einkapselung vorstrukturiert worden sein kann); Einkapselungsmaterial **204**, das die Struktur **200** zumindest teilweise ausfüllt; wobei die Hauptoberflächen (z. B. die Oberseite und die Unterseite) des metallischen Chipträgers **202** frei von Einkapselungsmaterial **204** sind, umfassen.

[0053] Der strukturierte metallische Chipträger **202** kann einen Anschlusskamm umfassen. Der Anschlusskamm kann aus einem Metall oder einer Metalllegierung gefertigt sein, die z. B. einen Werkstoff umfasst, der aus der Gruppe bestehend aus: Kupfer (Cu), Eisen-Nickel (FeNi), Stahl und dergleichen ausgewählt ist.

[0054] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial **204** Pressmasse oder ein vergleichbares Material umfassen. Das Einkapselungsmaterial **204** kann eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0055] In verschiedenen Ausführungsformen kann die Chipträgerstruktur **200** als Leistungs-Chipträgerstruktur für das Tragen eines oder mehrerer Leistungs-Chips darauf ausgestaltet sein.

[0056] **Fig.** 3 zeigt eine Chipträgerstruktur **300** gemäß verschiedenen Ausführungsformen.

[0057] Ähnlich wie bei der Chipträgerstruktur **200** von **Fig.** 2 kann die Chipträgerstruktur **300** einen strukturierten metallischen Chipträger **302** (der vor der Einkapselung vorstrukturiert worden sein kann) ; Einkapselungsmaterial **304**, das die Struktur **300** zumindest teilweise ausfüllt; wobei die Hauptoberflächen (z. B. die Oberseite und die Unterseite) des metallischen Chipträgers **302** frei von Einkapselungsmaterial **304** sind, umfassen. Verschiedene in Bezug auf die Chipträgerstruktur **200** beschriebene Ausführungsformen sind analog für die Chipträgerstruktur **300** gültig.

[0058] In verschiedenen Ausführungsformen von **Fig.** 3 kann der metallische Chipträger **302** eine Mehrzahl von Teilen oder Blöcken **306** umfassen. Zum Beispiel kann es sich bei der Mehrzahl von Teilen **306** um eine Mehrzahl von Anschlusskammteilen handeln. Diese Anschlusskammteile **306** können als Metallblöcke bezeichnet werden.

[0059] In verschiedenen Ausführungsformen kann die Chipträgerstruktur **300** weiterhin eine an eine der Hauptoberflächen des metallischen Chipträgers **302** angebrachte Folie **308** umfassen. Die Folie **308** kann zur Kühlung oder Trennung verwendet werden.

[0060] Gemäß verschiedenen Ausführungsformen von **Fig.** 2 und **Fig.** 3 oben ist eine Chipträgerstruktur mit einem Einkapselungsmaterial versehen, das die Struktur zumindest teilweise ausfüllt. In verschiedenen Ausführungsformen kann eine solche Chipträgerstruktur auch als vorgeformter Anschlusskamm bezeichnet werden.

[0061] Die Chipträgerstruktur kann für Leistungskomponenten wie Transistoren mit hoher Elektronenbeweglichkeit (High Electron Mobility Transistors; HEMT), z. B. GaN-(Galliumnitrid)-HEMT, SiC-(Siliciumcarbid)-HEMT oder Hochspannungs-Si-(Silicium) -HEMT; oder Niederspannungs-MOSFET (p-Kanal oder n-Kanal) (z. B. kleiner als 200 V), z. B. einen SFET (Silicium-Feldeffekttransistor) verwendet werden.

[0062] Die Chipträgerstruktur kann für Multi-Chip-Module, die z. B. eine durch mehrere Chips gebildete Halbbrückenschaltung oder Kaskadenschaltung umfassen, verwendet werden.

[0063] Die Chipträgerstruktur kann für ein Standard-Chipgehäuse oder ein eingebettetes Chipgehäuse verwendet werden.

[0064] Die Chipträgerstruktur gemäß verschiedenen Ausführungsformen ermöglicht die Realisierung eines hochvoltfähigen eingebetteten Gehäuses (z. B. > 200 V), denn die dafür erforderliche elektrische (z. B. Kriechstrecke) und thermische Leistung (z. B. Wärmekapazität) zusätzlich zur Anforderung einer niedrigen Induktivität kann unabhängig vom Einbettungsprozess in die Chipträgerstruktur eingebaut werden. Mit der Chipträgerstruktur verschiedener Ausführungsformen kann eine Kriechstrecke im Bereich von etwa 1 mm bis zu etwa 10 mm (z. B. im Bereich von etwa 3 mm bis zu etwa 8 mm, z. B. im Bereich von etwa 4 mm bis zu etwa 6 mm) erreicht werden. Der Einbettungsprozess wird auf die Chipträgerstruktur verschiedener Ausführungsformen angewendet, um ein Chipgehäuse verschiedener Ausführungsformen zu bilden, und gestattet Integrationsfähigkeit zusätzlich zur gewünschten niedrigen Induktivität (z. B. < 1 nH).

[0065] **Fig.** 4 zeigt ein Chipgehäuse **400** gemäß verschiedenen Ausführungsformen.

[0066] Das Chipgehäuse **400** kann eine Chipträgerstruktur **200** wie in **Fig.** 2 dargestellt umfassen. Die Chipträgerstruktur **200** kann einen strukturierten metallischen Chipträger **202**; ein Einkapselungsmaterial **204**, das die Struktur zumindest teilweise ausfüllt; wobei die Hauptoberflächen des metallischen Chipträgers **202** frei von Einkapselungsmaterial **204** sind, umfassen.

[0067] Verschiedene in der Chipträgerstruktur **200** von **Fig.** 2 oben beschriebene Ausführungsformen sind analog für das Chipgehäuse **400** gültig.

[0068] Der strukturierte metallische Chipträger **202** kann einen Anschlusskamm umfassen. Das Einkapselungsmaterial **204** kann eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen. In verschiedenen Ausführungsformen kann die Chipträgerstruktur **200** als Leistungs-Chipträgerstruktur für das Tragen eines oder mehrerer Leistungs-Chips darauf ausgestaltet sein.

[0069] Das Chipgehäuse **400** kann weiterhin einen über der Chipträgerstruktur **200** angeordneten Chip **412** und eine über dem Chip **412** gebildete Einkapselungsstruktur **420** umfassen, wobei die Einkapselungsstruktur **420** eine elektrisch leitende Umverteilungsstruktur **422** umfassen kann. Mindestens ein

Kontaktpad **432** kann über der Einkapselungsstruktur **420** gebildet werden, wobei das zumindest eine Kontaktpad **432** über die elektrisch leitende Umverteilungsstruktur **422** elektrisch an den Chip **412** gekoppelt ist.

[0070] In verschiedenen Ausführungsformen kann das Chipgehäuse **400** zwischen dem Chip **412** und dem strukturierten metallischen Chipträger **202** Klebstoff (in **Fig.** 4 nicht dargestellt) aufweisen, um den Chip **412** an den strukturierten metallischen Chipträger **202** anzukleben. In verschiedenen Ausführungsformen kann es sich bei dem Klebstoff um einen isolierenden Klebstoff handeln; in diesem Fall kann die Chipträgerstruktur **200** als Kühlstruktur verwendet werden. In verschiedenen Ausführungsformen kann der Klebstoff ein elektrisch leitender Klebstoff sein; in diesem Fall kann die Chipträgerstruktur **200** zum elektrischen Verbinden des Anschlusskontakts des Chips **412** mit dem strukturierten metallischen Chipträger **202** verwendet werden.

[0071] In verschiedenen Ausführungsformen kann der Chip **412** frei von Einkapselungsmaterial **204** sein, das die Chipträgerstruktur **200** zumindest teilweise ausfüllt. Das Einkapselungsmaterial **204**, z. B. die Vergussmasse, kann lediglich den strukturierten metallischen Chipträger **202** umgeben oder kann zusätzlich den Klebstoff für das Die-Bonden des Chips **412** an die Chipträgerstruktur **200** umgeben.

[0072] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger **202** als Leistungs-Chipträgerstruktur ausgestaltet sein. Zum Beispiel kann ein Leistungs-Chip **412** an dem strukturierten metallischen Chipträger **202** angebracht werden. Der Leistungs-Chip **412** kann einen Leistungsdiodenchip und/oder einen Leistungstransistorchip (z. B. einen Leistungs-MOSFET (Metalloxidhalbleiterfeldeffekttransistor), einen JFET (Sperrschichtfeldeffekttransistor), einen IGBT (Bipolartransistor mit isoliertem Gate), einen Leistungsbipolartransistor oder dergleichen umfassen).

[0073] In verschiedenen Ausführungsformen kann die über dem Chip **412** gebildete Einkapselungsstruktur **420** ein Laminat umfassen. Das Laminat kann Polymermaterial mit Glasfasern umfassen.

[0074] In verschiedenen Ausführungsformen kann die elektrisch leitende Umverteilungsstruktur **422** eine oder mehrere elektrisch leitende Schichten **424** (auch als Umverteilungsschichten bezeichnet) und Kontaktlöcher **426** für die elektrische Kopplung einer oder mehrerer elektrisch leitender Schichten **424** mit dem Chip **412** und für die elektrische Kupplung einer oder mehrerer elektrisch leitender Schichten **424** miteinander umfassen. Zum Beispiel zeigen die Ausführungsformen von **Fig.** 4 eine elektrisch leitende Umverteilungsstruktur **422** mit zwei Umverteilungsschichten **424**, doch kann die elektrisch leitende Umverteilungsstruktur **422** in verschiedenen anderen Ausführungsformen eine andere Anzahl (z. B. eine, drei, vier, ...) an Umverteilungsschichten umfassen.

[0075] **Fig.** 5A zeigt ein Chipgehäuse **500** gemäß verschiedenen Ausführungsformen.

[0076] In verschiedenen Ausführungsformen von **Fig.** 5A umfasst das Chipgehäuse **500** verschiedene Komponenten des in **Fig.** 4 dargestellten Chipgehäuses **400** und zusätzlich einen weiteren über der Chipträgerstruktur **200** angeordneten Chip **512** sowie eine weitere in der Einkapselungsstruktur **420** enthaltene elektrisch leitende Umverteilungsstruktur **522**. In verschiedenen Ausführungsformen kann das Chipgehäuse **500** eine Mehrzahl von Chips (z. B. drei, vier, fünf, ...) umfassen.

[0077] Das Chipgehäuse **500** kann somit ein Multi-Chip-Gehäuse bilden, wobei der Chip **412** und der weitere Chip **512** elektrisch miteinander gekoppelt sein können, z. B. durch den strukturierten metallischen Chipträger **202** und/oder die elektrisch leitenden Umverteilungsstrukturen **422**, **522**. In verschiedenen Ausführungsformen können die Chips **412**, **512** zur Bildung verschiedener Schaltungen, z. B. einer Halbbrückenschaltung, einer Kaskadenschaltung oder dergleichen, elektrisch miteinander gekoppelt sein.

[0078] In verschiedenen Ausführungsformen kann die Summe der Abmessungen A, B, C etwa 2,7 mm betragen, wobei A die Länge des Einkapselungsmaterials **204**, B die Höhe des Chipgehäuses **500** und C den Abstand zwischen den elektrisch leitenden Umverteilungsstrukturen **422** und der Kante des Chipgehäuses **500** darstellt.

[0079] **Fig.** 5B zeigt ein Chipgehäuse **550** gemäß verschiedenen Ausführungsformen.

[0080] Das Chipgehäuse **550** enthält das Chipgehäuse **500** von **Fig.** 5A und kann weiterhin auf einer Hauptoberfläche der Chipträgerstruktur **200** gegenüber den Chips **412**, **512** eine Folie **508** aufweisen. Die Folie **508** kann zu Kühlzwecken verwendet werden.

[0081] Die Chipgehäuse **500**, **550** sind kopfüber dargestellt und können so weiterhin auf einer Platine montiert werden, beispielsweise mittels Oberflächenmontagetechnik (Surface-Mounted Device; SMD).

[0082] **Fig.** 6 zeigt ein Chipgehäuse **600** gemäß verschiedenen Ausführungsformen.

[0083] In verschiedenen Ausführungsformen von **Fig.** 6 kann das Chipgehäuse **600** eine Chipträgerstruktur wie in **Fig.** 3 umfassen, einschließlich ei-

nes strukturierten metallischen Chipträgers **302** und Einkapselungsmaterials **304**, das die Struktur zumindest teilweise ausfüllt; wobei die Hauptoberflächen (z. B. die Oberseite und die Unterseite) des metallischen Chipträgers **302** frei von Einkapselungsmaterial **304** sind. Der metallische Chipträger **302** kann einem Mehrzahl von Teilen oder Blöcken **306**, z. B. eine Mehrzahl von Anschlusskammteilen (auch als Metallblöcke bezeichnet) umfassen.

[0084] Ähnlich dem Chipgehäuse **500** von **Fig.** 5A kann das Chipgehäuse **600** einen Chip **412** und einen weiteren über der Chipträgerstruktur, z. B. über einem Teil **306** des metallischen Chipträgers **302**, angeordneten Chip **512** umfassen. Eine Einkapselungsstruktur **420** kann über den Chips **412**, **512** gebildet sein, wobei die Einkapselungsstruktur **420** eine elektrisch leitende Umverteilungsstruktur **422**, **522**, die elektrisch an die Chips **412**, **512** gekoppelt ist, umfassen kann. Verschiedene in Bezug auf das Chipgehäuse **500** beschriebene Ausführungsformen sind analog für das Chipgehäuse **600** gültig.

[0085] Das Chipgehäuse **600** kann weiterhin zusätzliche, über einem anderen Teil **306** des metallischen Chipträgers **302** angeordnete Chips **612**, **614** umfassen, wobei die Chips **612**, **614** elektrisch mit der elektrisch leitenden Umverteilungsstruktur **522** gekoppelt sind.

[0086] In dieser Ausführungsformen sind die Chips **612**, **614** durch eine Schicht **616** aus Isoliermaterial, z. B. isolierendem Klebstoff, an dem Teil **306** des metallischen Chipträgers **302** angebracht. In diesem Fall können die Chips **612**, **614** vom metallischen Chipträger **302** elektrisch getrennt sein und kann der metallische Chipträger **302** als Kühlstruktur für die Chips **612**, **614** dienen.

[0087] In verschiedenen Ausführungsformen können die Chips **612**, **614** einen Logik-Chip, z. B. einen Treiber-Chip, umfassen. Der Logik-Chip kann mindestens einen Logikbaustein aus der Gruppe bestehend aus einem ASIC (Application Specific Integrated Circuit), einem Treiber, einer Steuerung, einem Sensor umfassen. Die Chips **412**, **512** können einen Leistungs-Chip, z. B. einen Leistungsdioden- und/oder einen Leistungstransistor-Chip umfassen. Die Logik-Chips **612**, **614** können zur Steuerung der Leistungs-Chips **412**, **512** verwendet werden.

[0088] **Fig.** 7A zeigt ein Gehäuse **700** gemäß verschiedenen Ausführungsformen.

[0089] Das Gehäuse **700** kann Mehrzahl von Chipgehäusen **550** wie in **Fig.** 5 dargestellt umfassen, die über der Chipträgerstruktur **300** aus **Fig.** 3 einschließlich einer Folie **308** ausgebildet sind.

[0090] In verschiedenen Ausführungsformen kann ein entsprechendes Paar der Chips **412**, **512** über einem entsprechenden Teil **306** des strukturierten metallischen Chipträgers angeordnet sein. In verschiedenen Ausführungsformen kann der Chip **416** ein HEMT, zum Beispiel ein GaN-HEMT oder ein SiC-HEMT oder ein Hochspannungs-Si-HEMT sein. Bei dem Chip **512** kann es sich um einen Niederspannungs-MOSFET (p-Kanal oder n-Kanal) (z. B. kleiner als 200 V) wie zum Beispiel einen SFET handeln.

[0091] Die elektrisch leitende Umverteilungsstruktur **422**, **522** kann eine oder mehrere Umverteilungsschichten umfassen, die zum Erreichen der gewünschten Kriechanforderungen beitragen können. Zum Beispiel kann in dem Chipgehäuse nach verschiedenen Ausführungsformen ein Kriechabstand D von 2,7 mm erreicht werden.

[0092] Es versteht sich, dass es sich bei den Chips **412**, **512** um verschiedene Arten der oben beschriebenen Leistungstransistoren handeln kann. In einer beispielhaften Ausführungsform kann der Chip **412** ein GaN-HEMT und der Chip **512** ein SFET sein.

[0093] Der GaN-HEMT-Chip **412** kann so angeordnet sein, dass seine Quellenelektrode zum Teil **306** des metallischen Chipträgers weist, und der SFET-Chip **512** kann so angeordnet sein, dass seine Drain-Elektrode zum Teil **306** des metallischen Chipträgers weist. Die Quellenelektrode des GaN-HEMT-Chips **412** und die Drain-Elektrode des SFET-Chips **512** können durch das Teil **306** des metallischen Chipträgers elektrisch miteinander verbunden sein.

[0094] In verschiedenen Ausführungsformen kann der GaN-HEMT-Chip **412** so angeordnet sein, dass seine Gate-Elektrode zur elektrisch leitenden Umverteilungsstruktur **422** weist und mit dieser elektrisch gekoppelt ist, und der SFET-Chip **512** kann so angeordnet sein, dass seine Quellenelektrode zur elektrisch leitenden Umverteilungsstruktur **522** weist und mit dieser elektrisch gekoppelt ist. Die Gate-Elektrode des GaN-HEMT-Chips **412** kann elektrisch mit der Quellenelektrode des SFET-Chips **512** gekoppelt sein, z. B. durch die elektrisch leitende Umverteilungsstruktur **422**, **522**, wobei der Knotenpunkt zwischen der Gate-Elektrode des GaN-HEMT-Chips **412** und der Quellenelektrode des SFET-Chips **512** bei Bezugszeichen **710** dargestellt ist.

[0095] Entsprechend können der GaN-HEMT-Chip **412** und der SFET-Chip **512** in dieser Anordnung eine in **Fig.** 8 dargestellte Kaskadenschaltung **800** bilden, die im Folgenden beschrieben wird.

[0096] Obwohl die Chips **412**, **512** in **Fig.** 6 und **Fig.** 7A auf dem gleichen Teil **306** des metallischen Chipträgers dargestellt sind, kann ein einzelnes Teil **306** einen oder mehrere Anschlusskammteile für die

elektrische Kopplung zwischen den Chips **412**, **512** durch den metallischen Chipträger umfassen.

[0097] **Fig.** 7B zeigt eine Chipanordnung **750**, die gemäß verschiedenen Ausführungsformen dem im Gehäuse **700** von **Fig.** 7A enthaltenen Chipgehäuse **500** entspricht.

[0098] Wie in **Fig.** 7B dargestellt, kann ein einzelnes Teil **306** der Chipträgerstruktur **300** ein erstes Anschlusskammteil **702** und ein zweites Anschlusskammteil **704** umfassen. Der GaN-HEMT-Chip **412** kann über dem ersten Anschlusskammteil **702** und der SFET-Chip **512** kann über dem zweiten Anschlusskammteil **704** angeordnet sein. Nach verschiedenen Ausführungsformen kann die Quellenelektrode des GaN-HEMT-Chips **412** zum ersten Anschlusskammteil **702** und die Drain-Elektrode des SFET-Chips **512** zum zweiten Anschlusskammteil **704** weisen. In verschiedenen Ausführungsformen kann die Quellenelektrode des GaN-HEMT-Chips **412** elektrisch mit dem zweiten Anschlusskammteil **704** gekoppelt sein, so dass er mit der Drain-Elektrode des SFET-Chips **512** elektrisch gekoppelt ist.

[0099] In verschiedenen Ausführungsformen kann ein einzelnes Teil **306** der Chipträgerstruktur **300** eine unterschiedliche Anzahl an Anschlusskammteilen umfassen, was von der Anordnung der Chips **412**, **512** abhängt.

[0100] Die verschiedenen Ausführungsformen von **Fig.** 7B können in gleicher Weise auf die Strukturen von **Fig.** 2 bis **Fig.** 4, **Fig.** 5A, **Fig.** 5B, **Fig.** 6, **Fig.** 7A oben angewendet werden.

[0101] In den unter Bezugnahme auf **Fig.** 7A und **Fig.** 7B oben dargestellten Ausführungsformen kann der GaN-Chip **412** ein Hochspannungs-HEMT-Schalter (z. B. größer als 200 V) und der SFET-Chip **512** ein Niederspannungs-Leistungs-MOSFET (z. B. kleiner als 200 V) sein. Der GaN-HEMT **412** ist eine selbstleitende Vorrichtung (Normally On) und wird mit Einführung des Niederspannungs-SFET **512** zu einem selbstsperrenden Transistor (Normally Off). Eine solche GaN-SFET-Anordnung entspricht der Kaskadenschaltung **800** in **Fig.** 8. Das Chipgehäuse **700** kann für einen Normally-Off-GaN geeignet sein.

[0102] Die Kaskadenschaltung **800** kann einen Niederspannung-SFET **512** in Source-Schaltungskonfiguration und einen Hochspannungs-GaN-HEMT **412** in Gate-Schaltungskonfiguration umfassen. Die daraus resultierende 3-Tor-Schaltung kann als Schalter fungieren. Die Drain-Elektrode des GaN-HEMT **412** definiert das 600 V-Verhalten der Kaskadenschaltung **800**.

[0103] Die Chips **412**, **512** können auch anders verbunden sein und so statt der Kaskadenschaltung **800** von **Fig.** 8 andere Arten von Schaltungen bilden.

[0104] **Fig.** 9 zeigt ein Diagramm, in dem das Gehäuse **700** von **Fig.** 7A zur Bildung einzelner Chipgehäuse, z. B. entsprechender Chipgehäuse **550** von **Fig.** 5B, vereinzelt werden kann.

[0105] Die Vereinzelung kann durch standardmäßiges Durchsägen vor allem des Einkapselungsmaterials **304** der Chipträgerstruktur **300** erfolgen. Zum Beispiel kann das Einkapselungsmaterial **304**, z. B. die Form, eine Dicke von 1000–1500 µm haben und eine Harztrennscheibe mit einer Breite von 100 µm für den Sägeprozess verwendet werden.

[0106] Wie oben beschrieben kann die Chipträgerstruktur **200**, **300** in den obigen verschiedenen Ausführungsformen als Basis für ein Chipgehäuse, z. B. ein eingebettetes Chipgehäuse, dienen. Einer oder mehrere Chips können mit der Chipträgerstruktur **200**, **300** verbunden sein, z. B. durch Kleben, Löten, Sintern usw.; und sie können über die elektrisch leitende Umverteilungsstruktur galvanisch umverteilt oder neu verdrahtet werden, so dass sie z. B. das Gehäuse **700** von **Fig.** 7A bilden. Nach der galvanischen Umverteilung oder Neuverdrahtung kann das Gehäuse **700** zur Bildung einzelner Chipgehäuse, z. B. der oben beschriebenen Chipgehäuse **400**, **500**, **550**, **600** vereinzelt werden. Die einzelnen Chipgehäuse können weiterhin auf eine Platine montiert werden, z. B. mittels SMD-Montage.

[0107] Die Chipträgerstruktur verschiedener Ausführungsformen bietet eine optimierte (dicke) Wärmekapazität und kann die gewünschten Kriechanforderungen erfüllen.

[0108] Das Chipgehäuse gemäß verschiedenen Ausführungsformen kombiniert das Vorvergießen (d. h. das Einkapselungsmaterial der Chipträgerstruktur, z. B. die Vergussmasse) mit dem Einbetten (d. h. die Einkapselungsstruktur über dem Chip, z. B. das Laminat) und erreicht eine niedrige Induktivität, einen niedrigen Drain-Source-Einschaltwiderstand ($R_{DS(on)}$), eine optimierte Wärmekapazität und kann Hochvolt-Kriechanforderungen erfüllen.

[0109] **Fig.** 10 zeigt ein Ablaufdiagramm **1000**, das ein Verfahren für die Herstellung einer Chipträgerstruktur gemäß verschiedenen Ausführungsformen darstellt.

[0110] Bei **1002** kann ein metallischer Chipträger der Chipträgerstruktur strukturiert werden.

[0111] Bei **1004** kann die Chipträgerstruktur zumindest teilweise mit Einkapselungsmaterial ausgefüllt werden, wobei die Hauptoberflächen des metalli-

schen Chipträgers frei von Einkapselungsmaterial bleiben.

[0112] In verschiedenen Ausführungsformen kann der strukturierte metallische Chipträger einen Anschlusskamm umfassen.

[0113] In verschiedenen Ausführungsformen kann das Einkapselungsmaterial eine Vergussmasse wie gefülltes Epoxidharz, z. B. mit SiO gefülltes Epoxidharz, umfassen.

[0114] Verschiedene Ausführungsformen der oben beschriebenen Chipträgerstruktur gelten analog für das Verfahren zur Herstellung einer Chipträgerstruktur.

[0115] **Fig.** 11 zeigt ein Ablaufdiagramm **1100**, das ein Verfahren für die Herstellung eines Chipgehäuses gemäß verschiedenen Ausführungsformen darstellt.

[0116] Bei **1102** kann ein metallischer Chipträger einer Chipträgerstruktur strukturiert werden.

[0117] Bei **1104** kann die Chipträgerstruktur zumindest teilweise mit Einkapselungsmaterial ausgefüllt werden, wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial bleiben.

[0118] Bei **1106** kann ein Chip über der Chipträgerstruktur angeordnet werden.

[0119] Bei **1108** kann eine Einkapselungsstruktur über dem Chip gebildet werden, wobei die Einkapselungsstruktur eine elektrisch leitende Umverteilungsstruktur umfassen kann.

[0120] Bei **1110** kann mindestens ein Kontaktpad über der Einkapselungsstruktur gebildet werden, um das zumindest eine Kontaktpad über die elektrisch leitende Umverteilungsstruktur elektrisch an den Chip zu koppeln.

[0121] Während die Erfindung insbesondere unter Bezugnahme auf bestimmte Ausführungsformen dargestellt und beschrieben wurde, sollte dem Fachmann klar sein, dass verschiedene Änderungen an Form und Details vorgenommen werden können, ohne vom Geist und Umfang der Erfindung, wie sie in den angefügten Ansprüchen definiert ist, abzuweichen. Der Umfang der Erfindung wird somit durch die angefügten Ansprüche angegeben, wobei sämtliche Änderungen im Sinne und innerhalb des Gleichwertigkeitsbereichs der Ansprüche darin eingeschlossen sein sollen.

Patentansprüche

1. Chipträgerstruktur (**200**), aufweisend:
einen strukturierten metallischen Chipträger (**202**);
Einkapselungsmaterial (**204**), das die Struktur (**200**) zumindest teilweise ausfüllt;
wobei die Hauptoberflächen des metallischen Chipträgers (**202**) frei von dem Einkapselungsmaterial (**204**) sind.

2. Chipträgerstruktur (**200**) nach Anspruch 1, wobei der strukturierte metallische Chipträger (**202**) einen Anschlusskamm aufweist.

3. Chipträgerstruktur (**200**) nach Anspruch 1 oder 2, wobei das Einkapselungsmaterial (**204**) Vergussmasse umfasst.

4. Chipträgerstruktur (**200**) nach einem der Ansprüche 1 bis 3, die als eine Leistungs-Chipträgerstruktur (**200**) ausgestaltet ist.

5. Chipgehäuse (**400**), aufweisend:
eine Chipträgerstruktur (**200**), aufweisend:
einen strukturierten metallischen Chipträger (**202**);
Einkapselungsmaterial (**204**), das die Struktur (**200**) zumindest teilweise ausfüllt;
wobei die Hauptoberflächen des metallischen Chipträgers (**202**) frei von dem Einkapselungsmaterial (**204**) sind;
einen über der Chipträgerstruktur (**200**) angeordneten Chip (**412**); und
eine über dem Chip (**412**) gebildete Einkapselungsstruktur (**420**), wobei die Einkapselungsstruktur (**420**) eine elektrisch leitende Umverteilungsstruktur aufweist;
mindestens ein über der Einkapselungsstruktur (**420**) gebildetes Kontaktpad (**432**);
wobei das mindestens eine Kontaktpad (**432**) über die elektrisch leitende Umverteilungsstruktur elektrisch an den Chip (**412**) gekoppelt ist.

6. Chipgehäuse (**400**) nach Anspruch 5, wobei der strukturierte metallische Chipträger (**202**) einen Anschlusskamm aufweist.

7. Chipgehäuse (**400**) nach Anspruch 5 oder 6,
wobei das Einkapselungsmaterial (**204**) Vergussmasse und/oder
wobei die Einkapselungsstruktur (**420**) ein Laminat umfasst.

8. Chipgehäuse (**400**) nach einem der Ansprüche 5 bis 7, wobei der Chip (**412**) frei von dem Einkapselungsmaterial (**204**) ist, das die Struktur zumindest teilweise ausfüllt.

9. Chipgehäuse (**400**) nach einem der Ansprüche 5 bis 8, weiterhin aufweisend:
Klebstoff zwischen dem Chip (**412**) und dem strukturierten metallischen Chipträger (**202**), um den Chip (**412**) an den strukturierten metallischen Chipträger (**202**) anzukleben;

wobei vorzugsweise der Klebstoff ein isolierender Klebstoff oder ein elektrisch leitender Klebstoff ist.

10. Chipgehäuse (**400**) nach einem der Ansprüche 5 bis 9, wobei der strukturierte metallische Chipträger (**202**) als eine Leistungs-Chipträgerstruktur (**200**) ausgestaltet ist.

11. Verfahren zur Herstellung einer Chipträgerstruktur (**200**), das folgende Schritte aufweist:
Strukturieren eines metallischen Chipträgers (**202**);
zumindest teilweises Ausfüllen der Struktur mit einem Einkapselungsmaterial (**204**);
wobei die Hauptoberflächen des metallischen Chipträgers (**202**) frei von dem Einkapselungsmaterial (**204**) bleiben.

12. Verfahren nach Anspruch 11, wobei der strukturierte metallische Chipträger (**202**) einen Anschlusskamm aufweist.

13. Verfahren nach Anspruch 11 oder 12, wobei das Einkapselungsmaterial (**204**) Vergussmasse (z. B. gefülltes Epoxidharz, Füllstoff: z. B. SiO) umfasst.

14. Verfahren zur Herstellung eines Chipgehäuses (**400**), das folgende Schritte aufweist: Herstellen einer Chipträgerstruktur (**200**), umfassend:
Strukturieren eines metallischen Chipträgers (**202**);
zumindest teilweises Ausfüllen der Struktur mit einem Einkapselungsmaterial (**204**);
wobei die Hauptoberflächen des metallischen Chipträgers (**202**) frei von dem Einkapselungsmaterial (**204**) bleiben;
Anordnen eines Chips (**412**) über der Chipträgerstruktur (**200**);
Bilden einer Einkapselungsstruktur (**420**) über dem Chip (**412**), wobei die Einkapselungsstruktur (**420**) eine elektrisch leitende Umverteilungsstruktur umfasst;
Bilden mindestens eines Kontaktpads (**432**) über der Einkapselungsstruktur (**420**), um das zumindest eine Kontaktpad (**432**) über die elektrisch leitende Umverteilungsstruktur elektrisch an den Chip (**412**) zu koppeln.

15. Verfahren nach Anspruch 14, wobei der strukturierte metallische Chipträger (**202**) einen Anschlusskamm aufweist.

16. Verfahren nach Anspruch 14 oder 15,
wobei das Einkapselungsmaterial (**204**) Vergussmasse umfasst; und/oder
wobei die Einkapselungsstruktur (**420**) ein Laminat umfasst.

17. Verfahren nach einem der Ansprüche 14 bis 16, wobei der Chip (**412**) frei von dem Einkapselungsmaterial (**204**) ist, das die Struktur zumindest teilweise ausfüllt.

18. Verfahren nach einen der Ansprüche 14 bis 17, weiterhin aufweisend:
das Bilden von Klebstoff zwischen dem Chip (**412**) und dem strukturierten metallischen Chipträger (**202**), um den Chip (**412**) an den strukturierten metallischen Chipträger (**202**) anzukleben;
wobei vorzugsweise der Klebstoff ein isolierender Klebstoff oder ein elektrisch leitender Klebstoff ist.

Es folgen 9 Seiten Zeichnungen

Anhängende Zeichnungen

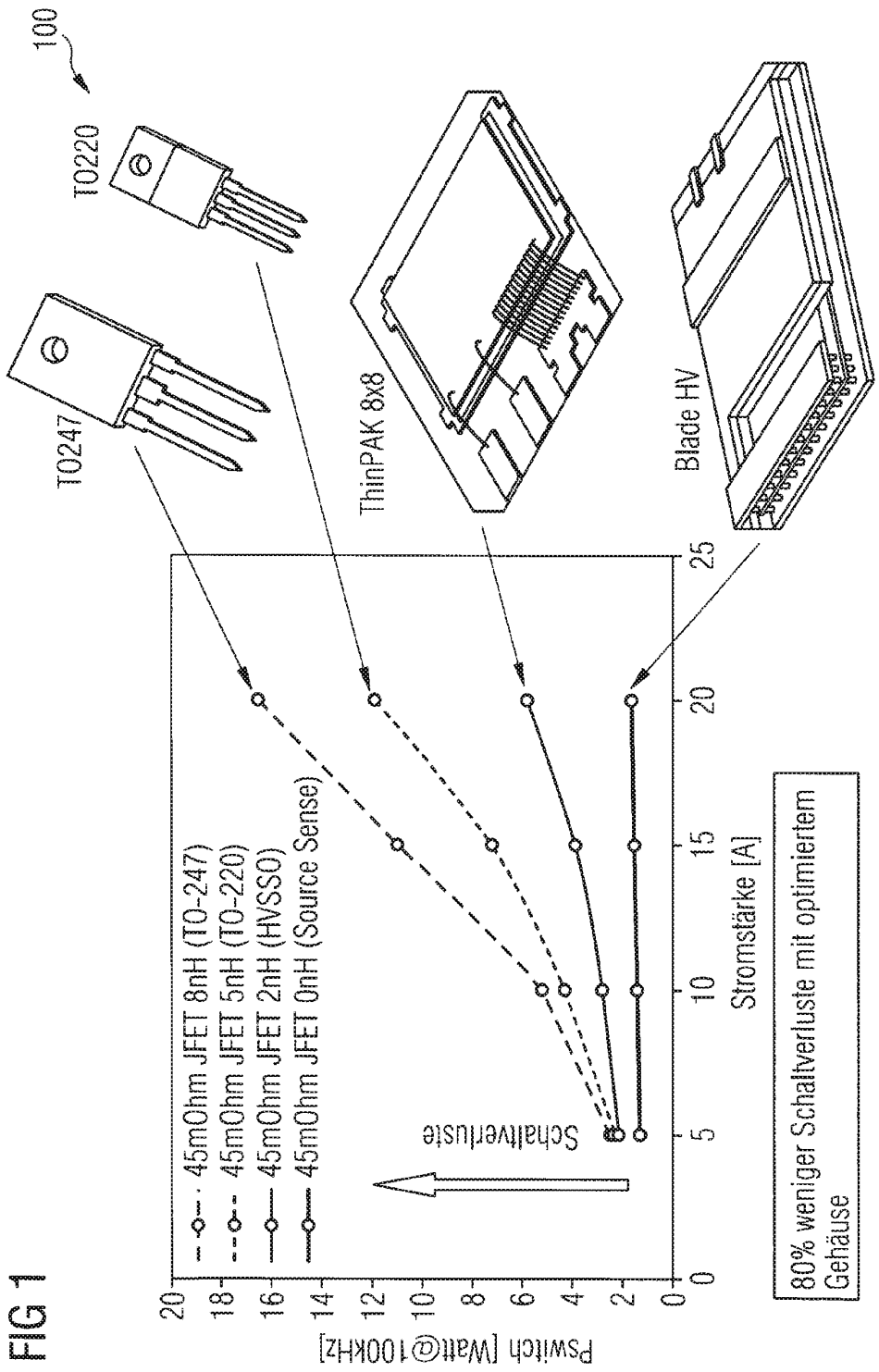


FIG 1

FIG 2

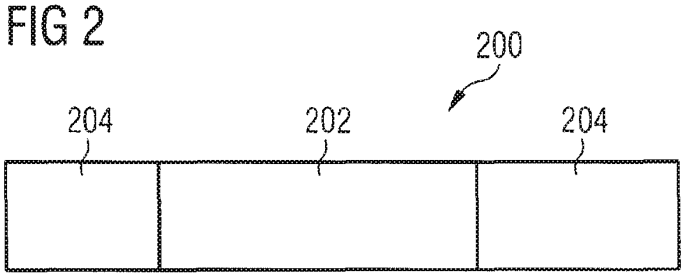


FIG 3

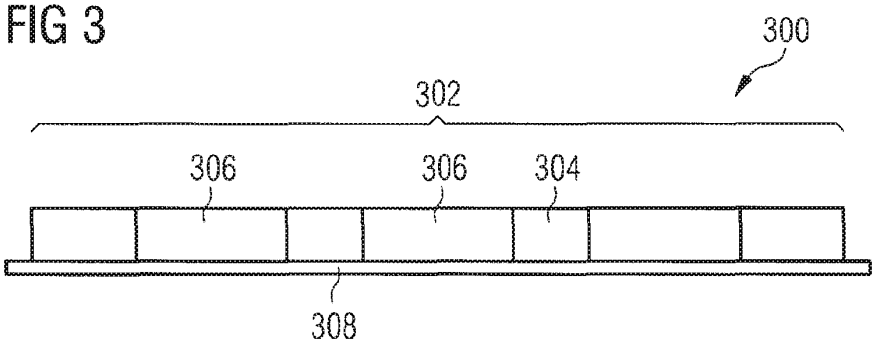


FIG 4

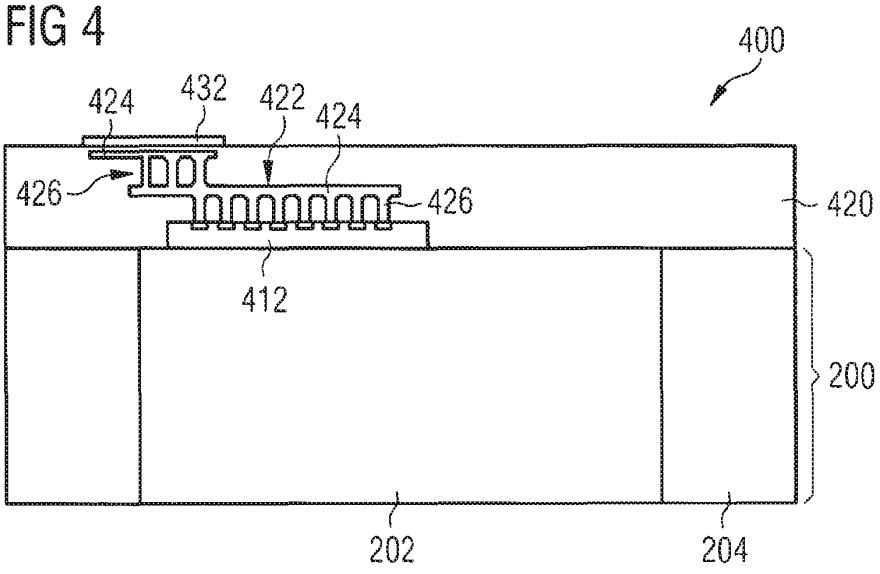


FIG 5A

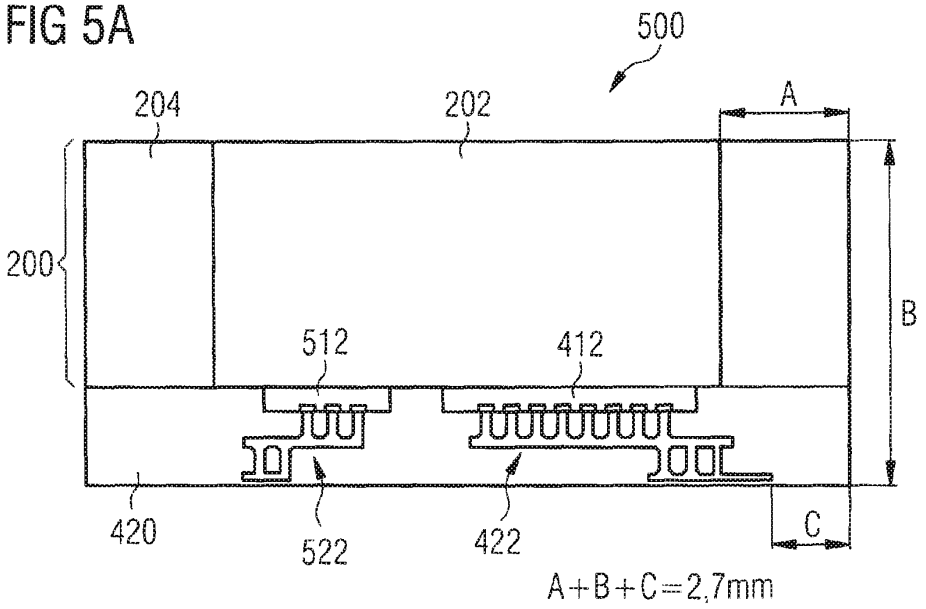
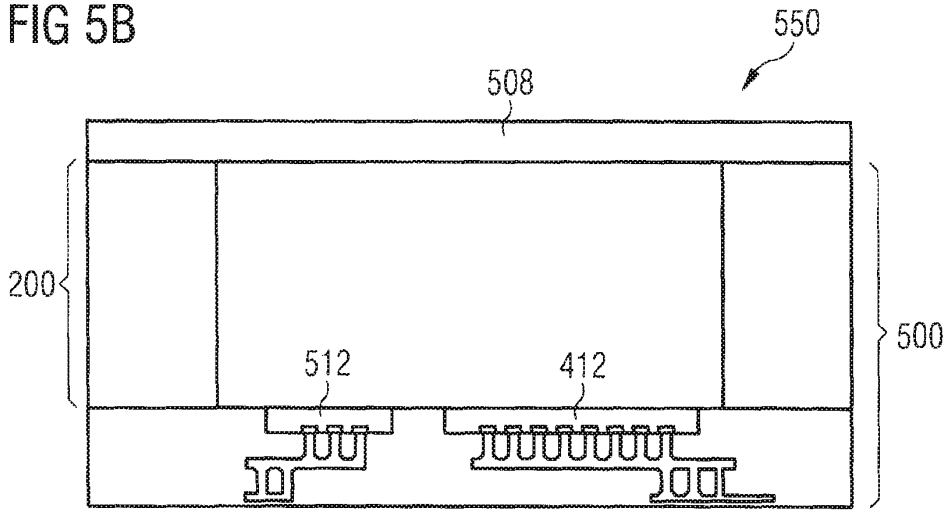

500
204
202
A
200
B
512
412
420
522
422
C
A+B+C=2,7mm

FIG 5B


550
508
200
500
512
412

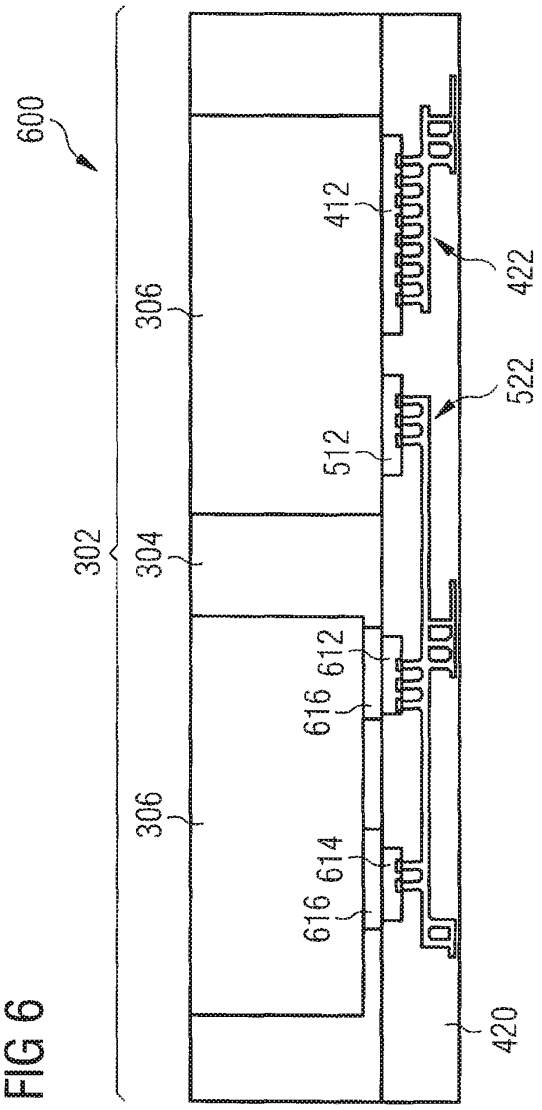


FIG 6

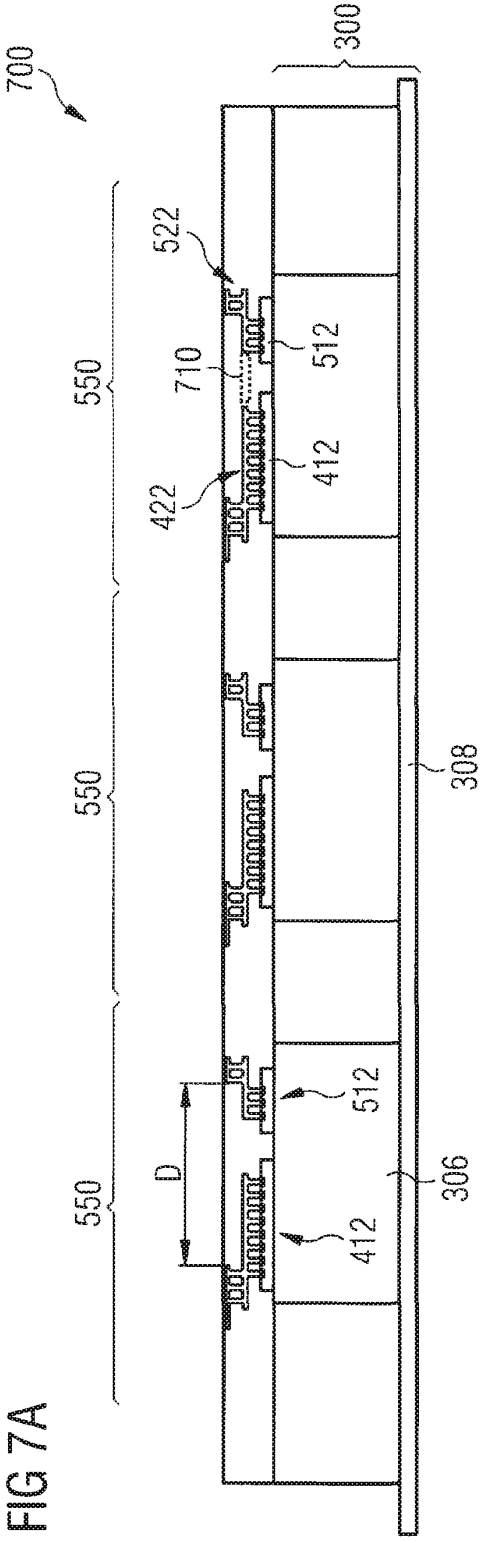


FIG 7A

FIG 7B

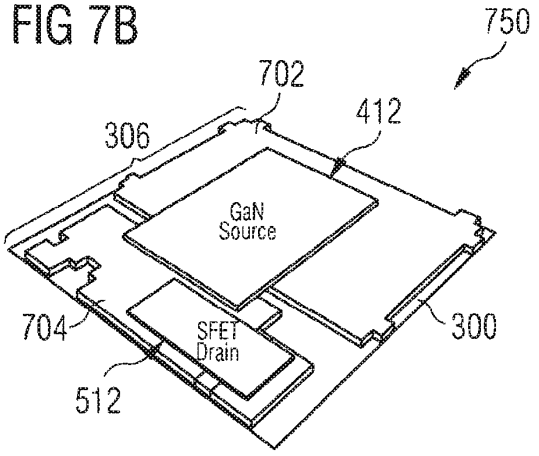
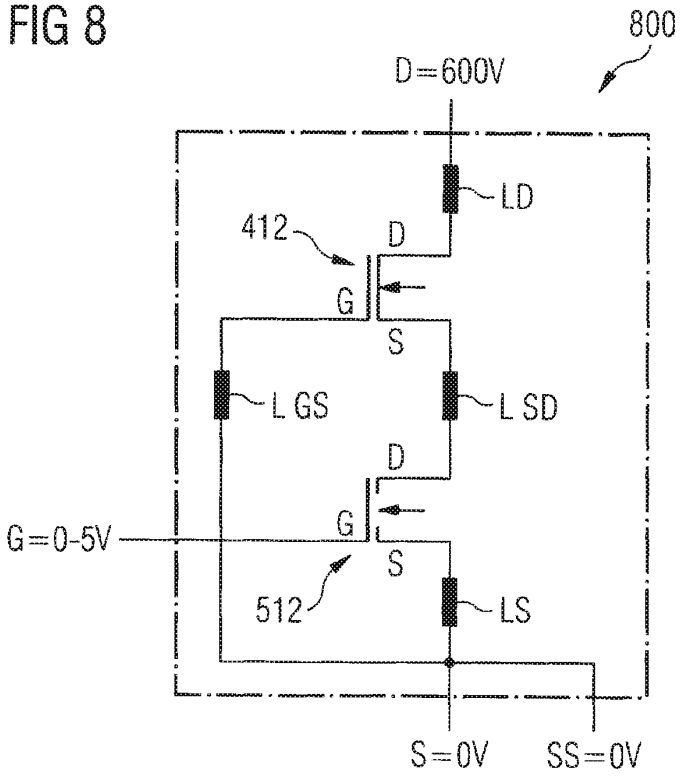

750
702
412
306
GaN
Source
704
SFET
Drain
300
512

FIG 8


800
D=600V
LD
412
D
G
S
L GS
L SD
D
G
G=0-5V
S
512
LS
S=0V
SS=0V

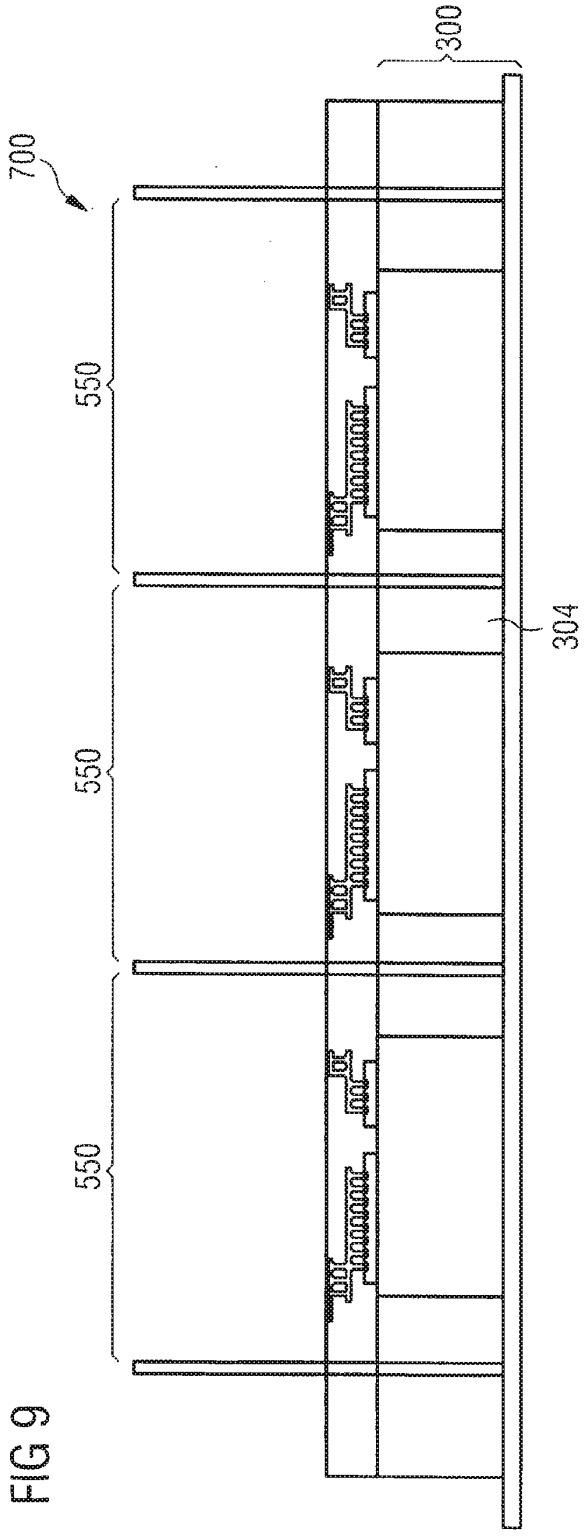


FIG 9

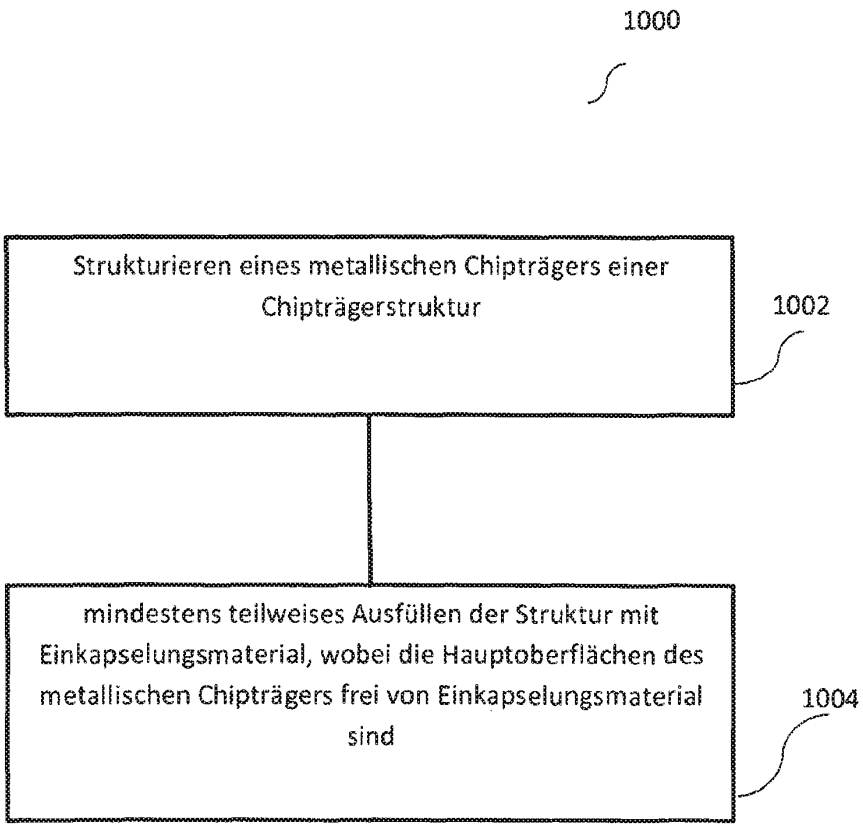

1000
Strukturieren eines metallischen Chipträgers einer Chipträgerstruktur
1002
mindestens teilweises Ausfüllen der Struktur mit Einkapselungsmaterial, wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial sind
1004

FIG. 10

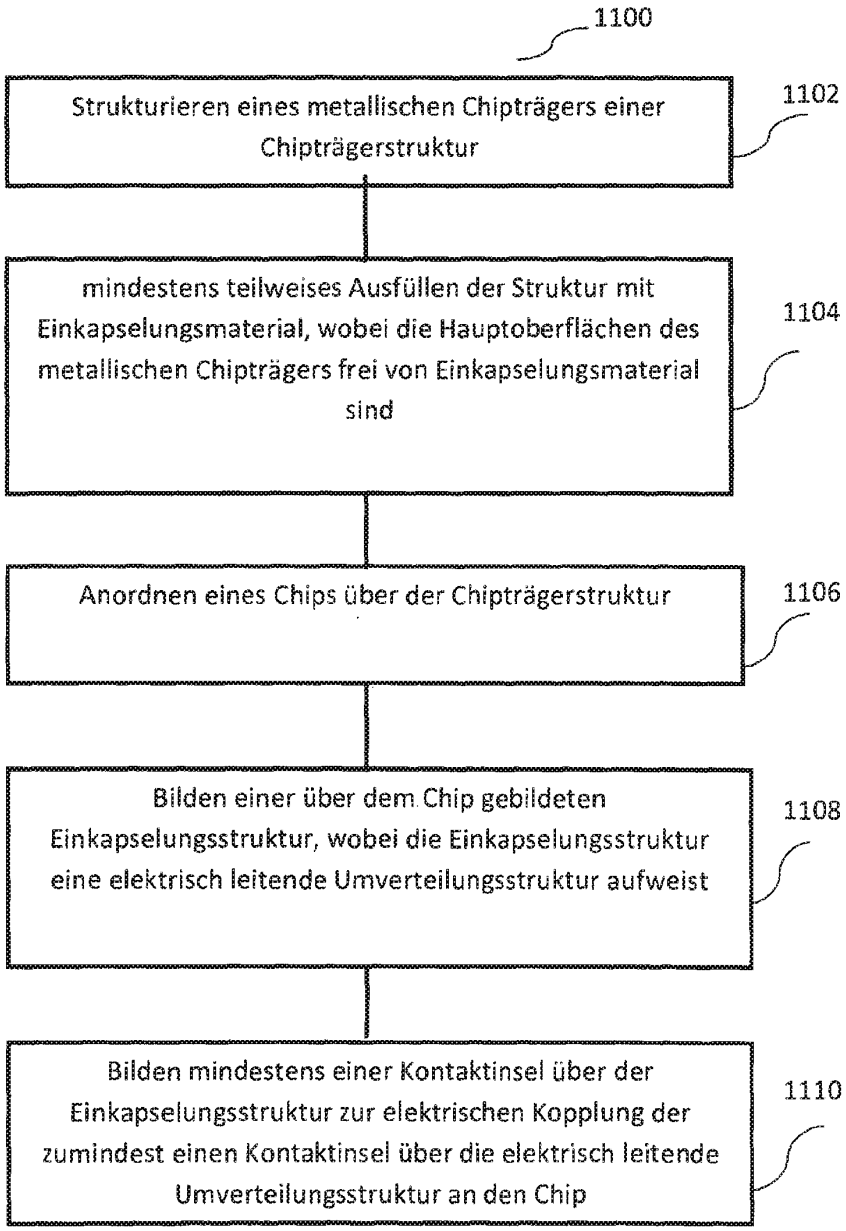

1100
Strukturieren eines metallischen Chipträgers einer Chipträgerstruktur
1102
mindestens teilweises Ausfüllen der Struktur mit Einkapselungsmaterial, wobei die Hauptoberflächen des metallischen Chipträgers frei von Einkapselungsmaterial sind
1104
Anordnen eines Chips über der Chipträgerstruktur
1106
Bilden einer über dem Chip gebildeten Einkapselungsstruktur, wobei die Einkapselungsstruktur eine elektrisch leitende Umverteilungsstruktur aufweist
1108
Bilden mindestens einer Kontaktinsel über der Einkapselungsstruktur zur elektrischen Kopplung der zumindest einen Kontaktinsel über die elektrisch leitende Umverteilungsstruktur an den Chip
1110

FIG. 11

Electronic Acknowledgement Receipt

EFS ID:	26539373
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Mark Ronald Bilak/Lindsey Shaw
Filer Authorized By:	Mark Ronald Bilak
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	03-AUG-2016
Filing Date:	18-JAN-2016
Time Stamp:	17:14:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	1012-1287_IDS_Transmittal.pdf	17956 ca14f0c0ab3c1d7421c87cd25def8c6e99b884fa	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	1012-1287_IDS.pdf	38647 7dca268d63fc63f84a380b6800a56fb29032045d	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	DE102014102910_A1.pdf	2526049 b5157219c008ed41b883f36c8c42147f8dcf2322	no	20
Warnings:					
Information:					
		Total Files Size (in bytes):	2582652		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: **Otremba**	)	
Serial No.: **14/997,914**	)	PATENT PENDING
Filed: **Jan 18, 2016**	)	Examiner: **DONOVAN, LINCOLN D**
For: **Electronic Component and Switch Circuit**	)	Group Art Unit: **2842**
Attorney's Docket No: **1012-1287 / 2015P51742 US**	)	Confirmation No.: **2194**

MS AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. 1.56, counsel wishes to make of record the attached items of information for the Examiner's consideration in connection with this application. Also enclosed is Form PTO/SB/08a for the Examiner's convenience in making such consideration of record. Inclusion herein of any particular item of information is not to be construed as an admission that same is prior art.

The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account 50-5650.

Respectfully submitted,
Murphy, Bilak & Homiller, PLLC

/Mark R. Bilak, Reg. No. 47,423/

Dated: August 3, 2016

Mark R. Bilak
Registration No.: 47,423

1255 Crescent Green, Suite 200
Cary, NC 27518

Telephone: (919) 948-3390
Facsimile: (919) 948-3357

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/997,914	01/18/2016	Ralf Otremba	1012-1287 / 2015P51742 US

CONFIRMATION NO. 2194

57579
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

POA ACCEPTANCE LETTER

OC000000080592643

Date Mailed: 02/16/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/04/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/snguyen/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/997,914
Filing Date	01-18-2016
First Named Inventor	Ralf Otremba
Title	Electronic Component and Switch Circuit
Art Unit	2811
Examiner Name	TBD
Attorney Docket Number	1012-1287 / 2015P51742 US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Mark R. Bilak, Reg. No. 47,423/	Date (Optional)	
Name	Mark R. Bilak	Registration Number	47,423
Title (if Applicant is a juristic entity)	Patent Practitioner		
Applicant Name (if Applicant is a juristic entity)	Infineon Technologies Austria AG		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 57579

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Infineon Technologies Austria AG

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Gudrun Voelker/ /Iris Druckenbrod/	Date (Optional)	23 Apr. 2014
Name	Gudrun Voelker Iris Druckenbrod		
Title	Head of IP Administration Manager IP Administration		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	24818181
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Mark Ronald Bilak/Lindsey Shaw
Filer Authorized By:	Mark Ronald Bilak
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	04-FEB-2016
Filing Date:	18-JAN-2016
Time Stamp:	10:57:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA.pdf	157180 04a95490b5ccdb1977d5d25d3fd77d4840b4bed7	no	1
Warnings:					
Information:					

2	Power of Attorney	AustriaAG.pdf	480657 fd6120de8f94f1808666bb33d45e912ad63dfc50	no	1

Warnings:	
Information:	
Total Files Size (in bytes):	637837

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/997,914

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 420 =	420
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2020

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/997,914	01/18/2016	2811	2020	1012-1287 / 2015P51742 US	20	4

CONFIRMATION NO. 2194

57579
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

FILING RECEIPT

OC000000080227279

Date Mailed: 02/03/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Ralf Otremba, Kaufbeuren, GERMANY;
Klaus Schiess, Allensbach, GERMANY;

Applicant(s)

Infineon Technologies Austria AG, Villach, AUSTRIA;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/29/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/997,914**

Projected Publication Date: 07/20/2017

Non-Publication Request: No

Early Publication Request: No
Title

Electronic Component and Switch Circuit

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ralf		Otremba	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Country of Residence [i]
Kaufbeuren	DE

Mailing Address of Inventor:

Address 1	Peter-Dorfler-Strasse 11
Address 2	
City	Kaufbeuren
State/Province	
Postal Code	87600
Country [i]	DE

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Klaus		Schiess	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Country of Residence [i]
Allensbach	DE

Mailing Address of Inventor:

Address 1	Silvaner Weg 19
Address 2	
City	Allensbach
State/Province	
Postal Code	78476
Country [i]	DE

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	57579		
Email Address	official@mbhiplaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	Electronic Component and Switch Circuit		
Attorney Docket Number	1012-1287 / 2015P51742 US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	57579		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Infineon Technologies Austria AG		
Mailing Address Information For Applicant:			
Address 1	Siemensstrasse 2		
Address 2			
City	Villach	**State/Province**	
Country	AT	Postal Code	9500
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Mark R. Bilak, Reg. No. 47,423/			Date (YYYY-MM-DD)	2016-01-18
First Name	Mark	Last Name	Bilak	Registration Number	47423

Additional Signature may be generated within this form by selecting the Add button. Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1012-1287 / 2015P51742 US
	Application Number	
Title of Invention	Electronic Component and Switch Circuit	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ELECTRONIC COMPONENT AND SWITCH CIRCUIT

BACKGROUND

[0001] An electronic component may include one or more semiconductor devices in a package. The package includes internal electrical connections from the semiconductor device to a substrate or a leadframe which includes outer contacts. The outer contacts are used to mount the electronic component on a redistribution board, such as a printed circuit board. The package may include a housing which covers the semiconductor device and the internal electrical connections. The housing may include a plastic material, such as epoxy resin, and may be formed by a mold process, such as injection molding.

[0002] To date, transistors used in power electronic applications have typically been fabricated with silicon (Si) semiconductor materials. Common transistor devices for power applications include Si CoolMOS®, Si Power MOSFETs, and Si Insulated Gate Bipolar Transistors (IGBTs). More recently, compound semiconductor devices such as silicon carbide (SiC) power devices and Group III-N semiconductor devices, such as gallium nitride (GaN) devices, have been considered. These devices are now emerging as attractive candidates to carry large currents, support high voltages and to provide very low on-resistance and fast switching times. The high voltages and fast switching times of such devices result in additional challenges for package development.

SUMMARY

[0003] In an embodiment, an electronic component includes a compound semiconductor transistor device having a first current electrode, a second current electrode and a control

electrode, a die pad, a first lead, a second lead and a third lead. The first lead, the second lead and the third lead are spaced at a distance from the die pad. The control electrode is coupled to the first lead, the first current electrode is coupled to the die pad and the second current electrode is coupled to the second lead. The third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality.

[0004] In an embodiment, a switch circuit includes a first transistor device and a second transistor device. The first transistor device includes a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead. The second lead and the third lead are spaced at a distance from the die pad. The control electrode is coupled to the first lead, the first current electrode is coupled to the die pad and the second current electrode is coupled to the second lead. The third lead is coupled to the transistor device and provides a source sensing functionality. The first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device.

[0005] In an embodiment, an electronic component includes a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz and a housing. The Group III nitride-based transistor device includes a first current electrode, a second current electrode and a control electrode. The control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality. The first lead, the

second lead and the third lead are spaced at a distance from the die pad and lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces.

[0006] In an embodiment, an electronic component includes means for coupling a control electrode of a compound semiconductor transistor device to a first lead, means for coupling a first current electrode of the compound semiconductor transistor device to a die pad, means for coupling a second current electrode of the compound semiconductor transistor device to a second lead and means for providing source sensing at a third lead.

[0007] Those skilled in the art will recognize additional features and advantages upon reading the following detailed description, and upon viewing the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts. The features of the various illustrated embodiments can be combined unless they exclude each other. Exemplary embodiments are depicted in the drawings and are detailed in the description which follows.

[0009] Fig. 1a illustrates a plan view of an electronic component according to a first embodiment.

[0010] Fig. 1b illustrates a cross-sectional view of the electronic component according to the first embodiment.

[0011] Fig. 2 illustrates a circuit diagram of a transistor with source sense functionality.

[0012] Fig. 3 illustrates a plan view of an electronic component according to a second embodiment.

[0013] Fig. 4 illustrates a cross-sectional view of an electronic component according to a third embodiment.

[0014] Fig. 5 illustrates a plan view of an electronic component according to a fourth embodiment.

[0015] Fig. 6 illustrates a cross-sectional view of the electronic component according to the fourth embodiment.

[0016] Fig. 7 illustrates a plan view of an electronic component according to a fifth embodiment.

[0017] Fig. 8a illustrates a cross-sectional view of a switch circuit including a compound semiconductor device and source sense functionality.

[0018] Fig. 8b illustrates a circuit diagram of a half-bridge circuit.

[0019] Fig. 9 illustrates a plan view of an electronic component including a switch circuit with two compound semiconductor transistor devices and a source sensing functionality.

[0020] Fig. 10a illustrates a plan view of electronic component including a bidirectional switch with source sense functionality.

[0021] Fig. 10b illustrates a circuit diagram of a bidirectional switch with source sense functionality.

[0022] Fig. 11 illustrates a cross-sectional view of a switch circuit including two compound semiconductor transistor devices with source sense functionality and topside cooling.

DETAILED DESCRIPTION

[0023] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top", "bottom", "front", "back", "leading", "trailing", etc., is used with reference to the orientation of the figure(s) being described. Because components of the embodiments can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, thereof, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0024] A number of exemplary embodiments will be explained below. In this case, identical structural features are identified by identical or similar reference symbols in the figures. In the context of the present description, "lateral" or "lateral direction" should be understood to mean a direction or extent that runs generally parallel to the lateral extent of a semiconductor material or semiconductor carrier. The lateral direction thus extends generally parallel to these surfaces or sides. In contrast thereto, the term

"vertical" or "vertical direction" is understood to mean a direction that runs generally perpendicular to these surfaces or sides and thus to the lateral direction. The vertical direction therefore runs in the thickness direction of the semiconductor material or semiconductor carrier.

[0025] As employed in this specification, when an element such as a layer, region or substrate is referred to as being “on” or extending “onto” another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element, there are no intervening elements present.

[0026] As employed in this specification, when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

[0027] As used herein, a "high-voltage device", such as a high-voltage depletion-mode transistor, is an electronic device which is optimized for high-voltage switching applications. That is, when the transistor is off, it is capable of blocking a high voltage of 400 V or higher, about 600 V or higher, or about 1200 V or higher, and when the transistor is on, it has a sufficiently low on-resistance (RON) for the application in which it is used, i.e., it experiences sufficiently low conduction loss when a substantial current passes through the device. A high-voltage device can at least be capable of blocking a voltage equal to the high-voltage supply or the maximum voltage in the circuit for which it is used. A high-voltage device may be capable of

blocking 400 V, 600 V, 1200 V, or other suitable blocking voltage required by the application.

[0028] As used herein, a "low-voltage device", such as a low-voltage enhancement-mode transistor, is an electronic device which is capable of blocking low voltages, such as between 0 V and V_{low}, but is not capable of blocking voltages higher than V_{low}. V_{low} may be about 10 V, about 20 V, about 30 V, about 40 V, or between about 5 V and 50 V, such as between about 10 V and 30 V.

[0029] As used herein, the phrase "Group III-Nitride" refers to a compound semiconductor that includes nitrogen (N) and at least one Group III element, including aluminum (Al), gallium (Ga), indium (In), and boron (B), and including but not limited to any of its alloys, such as aluminum gallium nitride ($Al_xGa_{(1-x)}N$), indium gallium nitride ($In_yGa_{(1-y)}N$), aluminum indium gallium nitride ($Al_xIn_yGa_{(1-x-y)}N$), gallium arsenide phosphide nitride ($GaAs_aP_bN_{(1-a-b)}$), and aluminum indium gallium arsenide phosphide nitride ($Al_xIn_yGa_{(1-x-y)}As_aPbN_{(1-a-b)}$), for example. Aluminum gallium nitride and AlGaN refers to an alloy described by the formula $Al_xGa_{(1-x)}N$, where $0 < x < 1$.

[0030] Fig. 1a illustrates a plan view and Fig. 1b a cross-sectional view of an electronic component 20 according to a first embodiment. Fig. 2 illustrates a circuit diagram of the electronic component 20.

[0031] The electronic component 20 includes a compound semiconductor transistor device 21 which includes a first current electrode 22, a second current electrode 23 and a control electrode 24. The electronic component 20 further includes a die pad 25, a first lead 26, a second lead 27 and a third lead 28. The first lead 26, the second lead 27 and the third lead 28 are spaced apart from the die pad 25. In the

electronic component 20 according to the first embodiment, the first lead, 26, the second lead 27, and the third lead 28 are arranged adjacent and spaced apart from a single side face 29 of the die pad 25. However, the arrangement of the leads with respect to the die pad may differ. For example, more than three leads may be provided and one or more of the leads may be arranged on adjacent two or more side faces of die pad 25.

[0032] As can be seen in the cross-sectional view of Fig. 1b, the die pad 25 has lower surface 30 which is substantially coplanar with the lower surfaces 31 of the leads 26, 27, 28. These lower surfaces 30, 31 provide the outer contact surfaces of the electronic component 20 and are surface mountable so that the electronic component 20 is a surface mountable device (SMD). The upper surface 38 of the die pad 25 and the upper surfaces 39 of the leads 26, 27, 28 are substantially coplanar. The die pad 25, first lead 25, second lead 27 and third lead 39 may include a metal such as copper.

[0033] The compound semiconductor transistor device 21 is a lateral device which has a lateral drift path. A first current electrode 22, second current electrode 23 and the control electrode 24 are arranged on an upper surface 32 of the compound semiconductor transistor device 21.

[0034] The control electrode 24 is coupled to the first lead 26, the first current electrode 22 is coupled to the die pad 25, the second current electrode 23 is coupled to the second lead 27 and the third lead 28 is coupled to the compound semiconductor transistor device 21 and provides a source sense functionality.

[0035] In the embodiment illustrated in Figs 1a and 1b, the first current electrode 22 is the source electrode of the compound semiconductor device 21 and is electrically coupled

to the die pad 25 by a conductive connector 33. The conductive connector 33 may the provided by one or more bond wires or a contact clip. In this embodiment, the die pad 25 is coupled to source so that the lower surface 30 of the die pad 25 provides a source contact for the electronic component 20. The second current electrode 23 is the drain electrode of the compound semiconductor transistor device 21 which is coupled to the second lead 27 by a conductive connector 34 which may include one or more bond wires or a contact clip. The control electrode 24 is a gate electrode which is coupled to the first lead 26 by a conductive connector 35 such as a bond wire.

[0036] In order to provide a source sensing functionality for the electronic component 20, a further electrical connection is made between the third lead 28 and source of the compound semiconductor transistor device 21, for example by a bond wire 36, electrically coupling the third lead 28 to source of compound semiconductor transistor device 21. The first lead 26 coupled to the gate electrode and the third lead 28 providing a source since functionality may be arranged adjacent one another and may be arranged on the same or on the opposing side of the die pad 25 to the lead 27 coupled to the drain electrode.

[0037] The electronic component 20 may include a housing 37 which encapsulates the side faces and upper surfaces of the die pad 25, the leads 26, 27, 28 and the electrical connections 33, 34, 35, 36 between the transistor device 21 and the upper surface 38 of the die pad 25 and upper surface 39 of the leads 26, 27, 28. The housing 37 may include an epoxy resin, for example. The lower surfaces 30, 31 of the die pad 25 and leads 26, 27, 28 are exposed from the housing 37 and provide contact areas or contact pads for providing an electrical connection to the compound semiconductor transistor device 21 within the housing 37. In some embodiments, a

portion of the leads 26, 27, 28 and die pad 25 may be exposed in the side faces of the housing 37. The electronic component 20 provides a compound semiconductor transistor device 21 in a package suitable for use in surface mount technology (SMT).

[0038] The compound semiconductor transistor device 21 may include a blocking voltage capability of at least 400 V and, in some embodiments, at least 650 V, and switching frequency capability of at least 100 kHz.

[0039] The compound semiconductor device 21 may be an enhancement-mode device. An enhancement mode device has a positive threshold voltage which means that it cannot conduct current at zero gate voltage and is normally off.

[0040] In the drawings the leads providing the nodes of the circuit are designated with source (S), drain (D), gate (G) and source sense (SS).

[0041] Fig. 2 illustrates a circuit diagram of the circuit which is provided by the electronic component 20. The circuit includes four nodes; source (S), drain (D), gate (G) and source sense (SS). The source sense node (SS) is coupled directly to the source (S) of the transistor.

[0042] In some gate driving arrangements, high switching speeds of a transistor device can result in a voltage drop across a parasitic source inductance which is sufficiently high to counteract the driving voltage which may result in increased energy loss. The parasitic source inductance is excluded from the driver circuitry by the use of the separate connection to the source provided.

[0043] The additional electrical connection between the source 22 of the transistor device 21 and the lead 28, which is

separate from the connection between the source pad 22 and the die pad 25, provides the compound semiconductor device 21 and electronic component 20 with a source sense functionality which may be used as a reference voltage by gate driver circuitry to exclude the parasitic source inductance from the driver circuit.

[0044] In some embodiments, such as that illustrated in Fig. 1, the compound semiconductor transistor device 21 is a lateral device which has a lateral drift path. In a lateral device, the first current electrode 22, the second current electrode 23 and the control electrode 24 are arranged on the upper surface 32 of the compound semiconductor transistor device 21. The compound semiconductor transistor device 21 may include a compound semiconductor such as a Group III nitride-based transistor device which may be a High Electron Mobility Transistor (HEMT).

[0045] In some embodiments, the compound semiconductor device 21 may a vertical device having a vertical drift path, in which case one of the current electrodes is arranged on lower surface of the body of the compound semiconductor transistor device and the other current electrode and control electrode are arranged on the opposing surface of the compound semiconductor transistor device. An example of a compound semiconductor transistor device having a vertical drift path is silicon carbide-based compound semiconductor transistor device.

[0046] In embodiments in which the compound semiconductor transistor device 21 includes a vertical device, a first current electrode and the control electrode are arranged on a first surface and the second current electrode is arranged on the opposing surface. In these embodiments, the second current

electrode, typically the drain, is coupled to the die pad by mounting the second current electrode onto the die pad.

[0047] If the compound semiconductor transistor device 21 is a lateral device, either one of the two current electrodes, for a HEMT source or drain, is electrically coupled to the die pad 25 by an additional connector extending between current electrode on the upper surface of the transistor device and the die pad 25.

[0048] In embodiments, in which the first current electrode, such as the source, is coupled to the die pad, the second current electrode, such as the drain, is electrically coupled to at least one lead arranged adjacent and spaced apart from the die pad. However, in other embodiments, the second current electrode, such as drain, is electrically coupled to the die pad by a connector such as one or more bond wires or a contact clip and the source is electrically coupled to a lead which is arranged adjacent and spaced apart from the die pad.

[0049] The electronic component may conform to a JEDEC package outline and, in some embodiments, conforms to a TO leadless (TOLL) package outline or ThinPak 8 x 8 package outline. Thus, a compound semiconductor transistor device may be accommodated within a standard package and include a source sense functionality. Furthermore, a lateral transistor device, such as a gallium nitride-based HEMT may be provided with a JEDEC package outline, in particular a TO leadless (TOLL) package outline or a ThinPak 8 x 8 package outline with a source sense functionality. Consequently, a lateral transistor device may be used in place of a vertical transistor device such as a CoolMOS® silicon-based transistor device as both types of device can be provided with the same package outline.

[0050] The selection of the current electrode which is electrically coupled to the die pad may be carried out depending on the position of the electronic component in an application such as a switch circuit. For example, if the electronic component is to provide the low side switch of a half bridge circuit, the drain electrode may be coupled to the die pad, whereas if the electronic component is to provide the high side switch of a half bridge circuit, the source electrode may be coupled to the die pad. This combination enables the two die pads to be mounted on, and electrically coupled to, a common conductive trace and form the output node of the half bridge circuit.

[0051] In some embodiments, a half-bridge circuit may be provided by a single electronic component including two transistor devices and a source sense functionality by mounting both transistor devices on a single die pad and coupling the drain of the transistor device providing low side switch and the source of the transistor device providing the high side switch to the die pad.

[0052] In embodiments in which a contact clip is used to coupled one of the current electrodes is coupled to the die pad or a lead, the entire contact clip may be encapsulated by the housing or a portion, such as the upper surface, may be exposed from the encapsulation material and form a portion of the upper surface of the electronic component. The exposed region of the contacts clip may be used as cooling surface on to which an additional heat dissipation device such as a heat sink may be mounted. This exposed region of the contact clip may be used to provide top side cooling for the electronic component.

[0053] The electronic component according to one any one of these embodiments may be used as part of a switch circuit

including two transistor devices. Each transistor device has a current path and the current path of the first transistor device may be coupled serially or antiserially with the current path of the second transistor device.

[0054] For example, if the switch circuit is a half bridge circuit or a cascode, the current path of the first transistor device is coupled in series with the current path of the second transistor device. If both transistor devices include a High Electron Mobility Transistor (HEMT), the drain of the first transistor device is coupled with source of the second transistor device so that the current paths are coupled serially.

[0055] If the switch circuit is a bidirectional switch, the current path of the first transistor device is coupled antiserially with the current path of the second transistor device. If both transistor devices include a High Electron Mobility Transistor (HEMT), the source of the first transistor device is coupled to source of the second transistor device so that the current paths are coupled antiserially.

[0056] Fig. 3 illustrates a plan view of an electronic component 40 according to a second embodiment. The electronic component 40 includes a compound semiconductor transistor device 41 which, in this particular embodiment, is a Group III-nitride based High Electron Mobility Transistor (HEMT). The electronic component 40 includes a package 42 having a ThinPak 8 x 8 package outline.

[0057] The package 42 includes a die pad 43 having an L-shaped form which extends on one side face 44 to provide two substantially parallel leads 45, 46 and forms a cutaway 47 in which two further leads 48, 49 are arranged. The further leads 48, 49 are spaced apart at a distance form the side face 44 of

the die pad 43 and are arranged in a row adjacent the lead 46. On the opposing side 50 of die pad 43, the package 42 includes four leads 51, 52, 53, 54 which are electrically coupled by a bar 56 extending substantially parallel and spaced apart form the side face 50 of the die pad 43. The lower surfaces of the leads are 45, 46, 48, 49, 51, 52, 53, 54 arranged at two opposing sides of the electronic component 40 and provide surface mountable contact pads. The lower surface of the die pad 43 is substantially parallel with the lower surfaces of the leads and also provides a surface mountable contact pad for the electronic component 40.

[0058] The compound semiconductor transistor device 41 includes a Group III nitride-based HEMT which is a lateral transistor device. The HEMT 41 includes a source pad 57, a drain pad 58 and a gate pad 59 arranged on its upper surface 60. The source pad 57 is electrically coupled to the die pad 43 and the leads 45, 46 by a plurality of bond wires 61 extending between the source pad 57 and the upper surface 62 of the die pad 43. The drain pad 58 is electrically coupled to the bar 56 and four leads 51, 52, 53, 54 arranged on the opposing side 50 of the die pad 43 by a plurality of bond wires 63. The gate pad 59 is electrically coupled to the lead 49 arranged adjacent the side face 44 of the die pad 43 by the board wire 64. The electronic component 40 includes a source sense functionality on lead 48 which is arranged between the source leads 45, 46 and the gate lead 49.

[0059] The lead 48 is electrically coupled to source of the compound semiconductor device 41 by an additional electrical connection 66 extending between the lead 48 and source, which is separate and spaced apart from the leads 45, 46 coupled to the die pad 43 which is coupled to source.

[0060] This additional electrical connection 66 to the source of the transistor device 41 has a smaller inductance than the electrical connection provided by the bond wires 61 between the source pad 57 and the leads 45, 46. Thus the lead 48 provides the compound semiconductor device 21 with a source sense functionality which may be used by a driver chip as a reference voltage which is free from a parasitic source inductance.

[0061] The electronic component 40 also includes a housing material, such as an epoxy resin, which is indicated schematically in Fig. 3 by the dashed line 67. The housing material covers the upper surfaces of the die pad 43, the leads, the transistor device 41 and the bond wires 61, 63, 64 and 66. In this embodiment, the upper surface of the electronic component 40 is formed by the material of the housing.

[0062] Fig. 4 illustrates a cross-sectional view of an electronic component 70 according to a third embodiment. The electronic component 70 includes a HEMT 41 arranged in a package 42 having a ThinPak 8 x 8 package outline as in the second embodiment.

[0063] The electronic component 70, therefore, includes a die pad 43, and leads arranged adjacent two opposing sides of the die pad 43 of which a drain lead 51 and the source lead 45 which extends from the die pad 43 can be seen in the cross-sectional view of Fig. 4. The electronic component 70 also includes a HEMT 41 which is mounted on the upper surface 62 of the die pad 43. As in the embodiment illustrated in Fig. 3, the drain pad 58 is electrically coupled to the lead 51 by bond wires 63. The gate pad 59 is electrically coupled to a gate lead and a source sense functionality is provided by a bond wire 66 extending to a further lead. The gate lead and

the further lead are spaced apart from the die pad 43 and cannot be seen in the cross-sectional view of Fig. 4.

[0064] The electronic component 70 differs from the electronic component 40 of the second embodiment in the form and arrangement of the electrical connection between the source pad 57 of the transistor device 41 and the die pad 43. In the electronic component 70 according to the third embodiment, the electrical connection is provided by a contact clip 71 which extends from the source pad 57 on the upper surface 60 of the HEMT 41 and the upper surface 62 of the die pad 43.

[0065] The contact clip 71 is provided by a metallic plate which is bent into an arched form having planar portions at the two distal ends. A first distal end is mounted on, and electrically coupled to, the upper surface 62 of the die pad 45 and a second distal end is mounted on, and electrically coupled to the source pad 57. In this embodiment, an uppermost portion 72 of the arch of the contact clip 71 is exposed in the upper surface 73 of the housing 67. Thus the exposed surface 72 of the contact clip 71 may be used for topside cooling. In other embodiments, the upper surface 73 of the contact clip 71 may be encapsulated by, and positioned within, the housing 67.

[0066] The connection between the drain pad 51 and bar 56 which is coupled to the leads 51, 52, 53, 54 may also be provided by a contact clip in place of the plurality of bond wires. A contact clip for the drain pad may also be embedded entirely within or partially exposed from the housing.

[0067] Fig. 5 illustrates a plan view and Fig. 6 a cross-sectional view of an electronic component 80 according to a fourth embodiment. The electronic component 80 includes a package 81 which, in this embodiment, conforms to a TO

leadless (TOLL) package outline and a compound semiconductor transistor device 82. In this particular embodiment, the compound semiconductor transistor device 82 is a lateral device including a source pad 83, a drain pad 84 and a gate pad 85 on its upper surface 86. The lower surface of the compound semiconductor transistor device 82 is mounted on the upper surface 87 of a die pad 88.

[0068] The die pad 88 is substantially rectangular with a cutaway region 89 in one corner. Two leads 90, 91 are arranged in this cutaway region which are spaced apart from side faces 92 of the die pad 88 forming the cutaway portion 89. The die pad 88 extends into six protruding portions 93 providing leads having a width substantially the same as the width of the leads 90, 91 which are arranged adjacent and substantially coplanar with the leads 90, 91. On the opposing side 94 of the die pad 88, the electronic component 80 includes a lead 95 having an elongate strip type shape which is spaced apart from the side face 96 of the die pad 88 and which has a length which is substantially the same as the long side of the rectangular die pad 88. The leads 90, 91, 95 and die pad 88 form part of a leadframe 97 of the electronic component 80. The leadframe 97 may include a metal such as copper. The leads 90, 91, 95 and die pad 88 may have substantially the same thickness so that the upper surfaces and lower surfaces are substantially coplanar.

[0069] The compound semiconductor transistor device 82 is mounted on the upper surface 87 of the die pad 88. The source pad 83 is electrically coupled to the die pad 88 and the leads 93 by a plurality of bond wires 98 extending between the source pad 83 and the upper surface 87 of the die pad 88. The drain pad 84 is electrically coupled to the elongate lead 95 on the opposing side 94 of the die pad 88 by a contact clip 99.

[0070] The contact clip 99 has the form of a metallic plate which is bent into an arched form having planar portions at the two distal ends. A first distal end is mounted on, and electrically coupled to, the drain pad 84 and a second distal end is mounted on, and electrically coupled to, the upper surface 100 of the elongate lead 95.

[0071] The gate pad 85 is electrically coupled to the lead 91 by a bond wire 101. The electronic component 80 has a source sense functionality which is accessible by the lead 90. The source sense lead 90 is arranged between the gate lead 91 and the protruding regions of the die pad 88 forming the source leads 93. The source sense lead (SS) 90 is electrically coupled to the source pad 83 by a bond wire 102.

[0072] The electronic component 80 also includes a plastic housing compound 104 in which the upper surface 87 of the die pad 88 and upper surfaces of the leads 90, 91, 96, the compound semiconductor transistor device 82 and the bond wires 98, 101, 102 are embedded. In a cross-sectional view of Fig. 5, it can be seen that in this particular embodiment, the contact clip 99 electrically coupling the drain pad 84 to the lead 95 is embedded within the plastic compound 104.

[0073] The lower surfaces 105 of the die pad 88, leads 90, 91, 95 and protruding portions 93 of the die pad 88 remain free of the plastic housing compound 104 and provide outer contact surfaces of the electronic component 80. The lower surfaces 105 are substantially coplanar with the lower surface 106 of the plastic housing compound 104. The plastic housing compound 104 also extends over side faces 92, 95, 106 of the die pad 88 and leads 90, 91, 96.

[0074] In some embodiments, the upper surface 103 of the contact clip 99 remains uncovered by the plastic housing composition 104 and forms a portion of the upper surface of the electronic component 80. In these embodiments, the electronic component 80 includes metallic portions on two opposing surfaces. The exposed metallic portion of contact clip may be used as an electrical connection, but may also be used to assist cooling of the compound semiconductor transistor device 82 and the electronic component 80 since heat can be more effectively dissipated from the exposed metallic portions than from the plastic housing composition 104. To assist cooling of electronic component 80, a further heatsink or cooling mechanism may be mounted on be exposed portion of the contact clip.

[0075] Fig. 7 illustrates a plan view of an electronic component 110 according to a fifth embodiment. The electronic component 110 includes a compound semiconductor device 111 and a leadframe 112 including a die pad 113 and a plurality of leads 114 arranged on two opposing sides 115, 116 of the die pad 113. Four leads 117 extend from the die pad 113 on the first side 115 and a further four leads 118 are arranged adjacent and spaced apart from the opposing side 116 of the die pad 113. Two of the four leads 118 are coupled together by a connector strip 119. Two leads 120, 121 are arranged adjacent the connector strip 119 such that the four leads 118 are arranged in a row and substantially parallel to one another.

[0076] The compound semiconductor device 111 is a transistor device which, in this embodiment, is a lateral transistor device having a source pad 122, a drain pad 123 and a gate pad 124 on its upper surface 125. The compound semiconductor device 111 is mounted on the upper surface 126 of the die pad 113.

[0077] In this embodiment, the drain pad 123 is electrically coupled to the die pad 113 by a plurality of bond wires 127. The source pad 122 is electrically coupled to the connector strip 119 by a plurality of bond wires 128 and the gate pad 124 is electrically coupled to the lead 121 by a bond wire 129. The electronic component 111 also includes a source sense function on the lead 120 which is arranged between the gate lead 121 and the connector strip 119. The source sense lead 120 is electrically coupled to source of the lateral transistor device by the bond wire 130. The source sense lead functionality is provided by a connection separate from the connection between the source pad 122 and the connector strip 119.

[0078] The die pad 113 and the leads 117, 118 include copper and have substantially the same thickness such that the upper surfaces of the die pad 113 and the leads 117, 118 are substantially coplanar and the lower surfaces of the leads 117, 118 and the die pad 113 are substantially coplanar. The electronic component 110 further includes a plastic housing composition indicated with the dashed line 131. The plastic housing composition covers the upper surfaces of the die pad 113 and leads 117, 118, the compound semiconductor device 111 and the bond wires 127, 128, 129, 130 and leaves the lower surfaces of the die pad 113 and leads 117, 118 exposed from the plastic composition. In some embodiments, the distal ends of the leads may also be exposed from the plastic housing composition in the side faces of the plastic housing composition.

[0079] In the case of a vertical transistor device such as a SiC-based transistor device, the device includes a current electrode on two opposing major surfaces. Therefore, one of the current electrodes, typically the drain, is mounted on

and, electrically coupled to, the die pad by the mounting connection. An additional electrical connector such as a bond wire or a contact clip is not required for this connection. The second current electrode, typically the source, is arranged on the upper surface and is electrically coupled to a lead spaced apart from the die pad by an additional electrical connector such as one or more bond wires or a contact clip.

[0080] In case of a lateral transistor device, either one of the current electrodes, that is either the source or the drain may be electrically coupled to the die pad using an additional connector extending from the upper surface of the transistor device to the upper surface of the die pad. This additional electrical connector may be provided by one or more bond wires, a contact clip or a metallic ribbon for example. In some embodiments, the additional electrical connector is embedded within the housing of the electronic component and is electrically accessible only by the lower surface of the die pad. In other embodiments, particularly for embodiments in which the electrical connector includes a contact clip, a portion of the contact clip may be exposed from the housing and provide a surface which may be electrically coupled to an external circuit or may be coupled to an additional heat sink and used for topside cooling.

[0081] In some embodiments, both current electrodes, that is both source and drain, may be coupled to the leadframe using a contact clip. The bond wire electrically coupling the gate to the gate electrode and the bond wire providing the source of function may have smaller diameter and/or different composition than that of any bond wires used to electrically couple the current electrode to a lead or a die pad.

[0082] The electronic component according to any one of the embodiments described herein includes a compound semiconductor

transistor device housed within a SMD package and includes a source sense functionality. One or more of these components may be used in a variety of applications such as a switch circuit or subcircuit of a switch circuit. Examples of switch circuits include half bridge configurations, cascode configurations or bidirectional switch. In these switch circuits, the first transistor device has a current path coupled in series with a current path of the second transistor device.

[0083] Fig. 8a illustrates a cross-sectional view of a switch circuit 140 including an electronic component 141 with a compound semiconductor transistor device 142 and a source sense functionality 143. A circuit diagram of the switch circuit is illustrated in Fig. 8b.

[0084] The switch circuit 140 is a half bridge circuit in which the electronic component 141 includes a silicon carbide-based transistor device 141 which forms the Low Side Switch (LSS) of the half bridge circuit. As discussed above, silicon carbide-based transistor devices are vertical transistor devices and include current electrodes on two opposing major surfaces. As is illustrated in Fig. 8a, the drain electrode 144 is arranged on the lower surface 145 and the source electrode 146 and gate electrode 147 are arranged on the upper surface 148. The drain electrode 144 is mounted on, and electrically coupled to, a die pad 149 (D1) of the electronic component 140. The gate electrode 147 and the source electrode 146 are electrically coupled to two separate leads (S1) (G1) not visible in the schematic cross-sectional view of Fig. 8a . The electronic component 141 includes a source sense functionality 143 provided by an additional electrical connection between the source 146 and a lead 150 (SS) which is separate from the source connection.

[0085] The half bridge circuit includes a second electronic component 151 providing the High Side Switch (HSS). In this embodiment, the electronic component 151 includes a compound semiconductor transistor device 152 in the form of a gallium nitride-based lateral transistor device having a drain pad 153, a source pad 154 and a gate pad 155 on the upper surface 156 of the compound semiconductor transistor device 152. The drain pad 153 is electrically coupled to a lead 157 (D2) spaced apart from a die pad 158. The source pad 154 is electrically coupled to the die pad 158 (S2) and the gate 155 is electrically coupled to lead (G2) which is not visible in the cross-sectional view Fig. 8a and which is arranged adjacent and spaced apart from the die pad 158. The half bridge circuit is formed by mounting die pad 158 of the electronic component 151 and the die pad 149 of the electronic component 141 on a common conductive trace 159 to electrically couple the drain pad 144 of the transistor device 141 to the source pad 156 of the second transistor device 151 and, therefore, the drain D1 of the Low Side Switch to the source (S2) of the High Side Switch. The conductive trace 159 may be part of a redistribution board 160.

[0086] The second transistor device 151 may also include a source sense functionality 161, but providing a second connection to the source pad 154 which is separate from the connection between the source pad 154 and the die pad 158.

[0087] In some embodiments, the Low Side Switch of the half bridge circuit may be provided by a silicon-based transistor device. In some embodiments, both of the Low Side Switch and the High Side Switch of the half bridge circuit may be provided by compound semiconductor devices and, in some embodiments, by gallium nitride-based transistor devices.

[0088] The semiconductor material of the transistor device for the low side switch may be selected depending on the duty cycle. If the duty cycle is around 50%/50% between the High Side Switch and the Low Side Switch, a gallium nitride-based transistor device may be used for the Low Side Switch. For a duty cycle of 90%/10%, a silicon-based, silicon carbide-based or gallium nitride-based transistor device may be used for the Low Side Switch. At ratios of grater than 2 : 1, a gallium nitride-based transistor device is typically used.

[0089] In some embodiments, a switch circuit may be provided by single electronic component.

[0090] Fig. 9 illustrates a plan view of an electronic component 170 providing a switch circuit 171 including two compound semiconductor transistor devices 172, 173. The switch circuit 171 is a half bridge circuit.

[0091] The electronic component 170 includes a leadframe 174 including a die pad 175 and a plurality of leads 176 arranged on two opposing sides of the die pad 175. The electronic component 170 includes eight contact surfaces provided by lower surfaces of the plurality of leads 176 and a contact surface provided by the lower surface of the die pad 175.

[0092] Four leads 177 178, 179 and 180 are arranged adjacent and spaced apart from a first side 181 of the die pad 175. Two leads 177, 178 are coupled together by a connector strip. The leadframe 171 includes a similar arrangement on the opposing side 182 of the die pad 175 and includes four leads 183, 184 185 186 arranged adjacent and spaced part from the side 182 of the die pad 175. Two of the leads 183, 184 are coupled together by a connector strip.

[0093] The two transistor devices 172, 173 are mounted on an upper surface 187 of the die pad 175. In this embodiment, the first transistor device 172 provides the Low Side Switch and the second semiconductor device 173 the High Side Switch of the half bridge circuit. The transistor devices 172, 173 may be Group III nitride based High Electron Mobility Transistors, for example.

[0094] The first transistor device 172 includes a source pad 188, a drain pad 189, a gate pad 190 and a source sensing pad 191 arranged on its upper surface 192. The source pad 188 is electrically coupled to the leads 177, 178 by one or more bond wires 193. The source sensing pad 191 is electrically coupled to the lead 179 by a bond wire 194 and the gate pad 190 is electrically coupled to the outermost lead 186 on first side 181 of the die pad 175 by the bond wire 195. The drain pad 189 is electrically coupled to the die pad 175 by a plurality of bond wires 196.

[0095] The second compound semiconductor transistor device 173 also includes a source pad 196, a drain pad 197, a gate pad 198 and a source sensing pad 199 on its upper surface 200. The drain pad 197 is electrically coupled to the leads 183, 184 by a plurality of bond wires 202. The gate pad 198 is electrically coupled to the outermost lead 186 by a bond wire 203 and the source pad 199 is electrically coupled to the lead 185 by bond wire 204. The source pad 196 is electrically coupled to the die pad 175 and, therefore, to the drain of the first compound semiconductor transistor device 172 by a plurality of bond wires 201.

[0096] The electronic component 170 provides a switch circuit having a half bridge configuration in which a source sense function is provided for both the first compound semiconductor transistor device 172 providing the Low Side Switch of the

half bridge circuit and for the second compound semiconductor device 173 providing High Side Switch of the half bridge circuit. The electrical connection between the drain of the Low Side Switch and source of the High Side Switch is provided by the die pad 175 on which both transistor devices 172, 173 are mounted and to which the drain pad 189 of the first transistor device 172 and the source pad 196 of the second transistor device 173 are electrically coupled by their respective plurality of bond wires 196, 201.

[0097] The electrical connections are not limited to bond wires and one or more of the pluralities of bond wires may be replaced by a contact clip, for example. The electronic component 170 provides outer contact surfaces arranged substantially underneath the lead frame 171 and the housing. The position of the housing is indicated by a dashed line in Fig. 9. The electronic component 170 provides a surface mount device (SMD) including a half bridge circuit provided by two compound semiconductor transistor devices 172, 173 and a source sense function 179, 185 for both the Low Side Switch and the High Side Switch of the half bridge circuit. The node of the half bridge circuit may be electrically accessed by the contact surface provided by the lower surface of the die pad 175.

[0098] The footprint of the electronic component 170 may conform to a ThinPak 8 x 8 package footprint.

[0099] Fig. 10a illustrates a plan view of an electronic component 210 providing a bidirectional switch circuit 211 including two compound semiconductor transistor devices 212, 213 and a lead frame 171. Fig. 10b illustrates a circuit diagram of the bidirectional switch circuit 211.

[0100] The leadframe 171 has the same configuration as that illustrated in Fig. 9 and includes a die pad 175 and leads 177, 178, 179, 180 arranged adjacent and spaced apart from the first side 181 of the die pad 175 and leads 183, 184, 185, 186 arranged adjacent and spaced apart from the opposing side 182 of the die pad 175. The compound semiconductor devices 212, 213 each include a Group III nitride-based High Electron Mobility Transistor. The first compound semiconductor transistor device 212 includes a source pad 214, a drain pad 215, a gate pad 216 and a source sense pad 217 arranged on its upper surface 218. The second compound semiconductor transistor device 213 also includes a source pad 219, a drain pad 220, a gate pad 221 and a source sense pad 222 on its upper surface 223.

[0101] A bidirectional switch circuit is formed by electrically coupling the drain pad 215 of the first compound semiconductor transistor device 212 to leads 183, 184 (D1) by a plurality of bond wires 225, the gate pad 216 to lead 186 (G1) by bond wire 226, the source pad 214 (S1) of the first compound semiconductor transistor device 212 to the source pad 219 (S2) of the second compound semiconductor transistor device 213 by a plurality of bond wires 227. The drain pad 220 of the second compound semiconductor transistor device 213 is electrically coupled to leads 177, 178 (D2) by a plurality of bond wires 228 and the gate pad 221 is coupled to the lead 180 (G2) by bond wire 229. The drain pad 215 of the first compound semiconductor transistor device 212 is electrically coupled to that die pad 175 (D1) by one or more bond wires 232. The lower surfaces of the leads 177, 178, 179, 180, 183, 184, 185, 186 and die pad 175 provides contact surfaces for the electronic component 210.

[0102] A source sense functionality is provided for each of the compound semiconductor transistor devices 212, 213 of the

bidirectional switch 211. The lead 185 (SS1) is electrically coupled to source of the first compound semiconductor transistor device 212 by bond wire 233. The lead 179 (SS2) is electrically coupled to source of the second compound semiconductor transistor device 213 by the bond wire 231. The source sense leads 179, 185 are arranged between the respective drain lead 183, 184; 177; 178 and gate lead 188; 186. The electronic component 210 may have a footprint 234 conforming to a ThinPak 8 x 8 footprint.

[0103] Fig. 11 illustrates a cross-sectional view of a switch circuit 240 including two electronic components 241, 242 coupled to provide a half bridge circuit. The first electronic component 241 includes a compound semiconductor transistor device 243 with a source sense function 244. The first electronic component 241 provides the Low Side Switch of the half bridge circuit. The electronic component 242 also includes a second compound semiconductor transistor device 245 including a source sense function 246. The second component semiconductor device 245 provides the High Side Switch of the half bridge circuit. The switch circuit 240 includes topside cooling of both the source S1 of the first electronic component 241 providing the Low Side Switch of the half bridge circuit and the drain D2 of the second electronic component 243 providing the High Side Switch 241.

[0104] The first compound semiconductor device 243 and the second compound semiconductor device 245 are lateral transistor devices with a source pad, drain pad, gate pad on their upper surface. The first compound semiconductor device 243 and the second compound semiconductor device 245 may be gallium nitride-based High Electron Mobility devices.

[0105] The source 247 of the first compound semiconductor device 243 is electrically coupled to the die pad 248 of the

electronic component 202 by contact clip 249 which has a portion 250 which is exposed in an upper surface 251 of the electronic component housing 252 of the electronic component 242. The drain 253 of the second compound semiconductor transistor device 245 providing the High Side Switch is electrically coupled to die pad 254 of the second electronic component 241 by a contact clip 255 which has a portion 256 exposed from the housing 257 in the upper surface 258 of the housing 257.

[0106] These exposed portions 250, 256 of the contact clips 249, 255, respectively, may be used to provide topside cooling of the of the half bridge circuit using a common heat dissipator 259 which may be mounted on the upper surfaces of the electronic components 241, 242 and thermally coupled to the exposed portions of the contact clips.

[0107] The half bridge circuit may be formed by electric coupling the drain D1 of the Low Side Switch to the source S2 of the High Side Switch using conductive traces of the rewiring substrate on which the electronic components 241, 242 mounted.

[0108] A compound semiconductor transistor device, such as a lateral gallium nitride-based HEMT, may be arranged in a package having a SMD outline and the package include a source sense functionality. One of the current electrodes, i.e. the source or the drain, of the lateral transistor device is coupled to the die pad and a source sense connection is provided by a second connection from the source to a lead spaced apart from the die pad which is separate from the connection providing the source node of the lateral transistor device. The transistor device may have a blocking voltage capability of at least 400V and a switching frequency

capability of at least 100 kHz. The package may conform to a standard SMD package outline or footprint.

[0109] Spatially relative terms such as "under", "below", "lower", "over", "upper" and the like are used for ease of description to explain the positioning of one element relative to a second element. These terms are intended to encompass different orientations of the device in addition to different orientations than those depicted in the figures. Further, terms such as "first", "second", and the like, are also used to describe various elements, regions, sections, etc. and are also not intended to be limiting. Like terms refer to like elements throughout the description.

[0110] As used herein, the terms "having", "containing", "including", "comprising" and the like are open ended terms that indicate the presence of stated elements or features, but do not preclude additional elements or features. The articles "a", "an" and "the" are intended to include the plural as well as the singular, unless the context clearly indicates otherwise. It is to be understood that the features of the various embodiments described herein may be combined with each other, unless specifically noted otherwise.

[0111] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

CLAIMS

What is claimed is:

1. An electronic component, comprising:

a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;

a die pad; and

a first lead, a second lead and a third lead,

wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality.

2. The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.

3. The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

4. The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

5. The electronic component of claim 1, wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad.

6. The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.

7. The electronic component of claim 1, wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

8. The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.

9. The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

10. The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

11. The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

12. A switch circuit, comprising:

a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead, the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provides a source sensing functionality; and

a second transistor device,

wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device.

13. The switch circuit of claim 12, wherein a drain of the first transistor device and a source of the second transistor device are coupled to a common die pad.

14. The switch circuit of claim 12, wherein the first transistor device is housed in a package comprising a first die pad coupled to a drain of the first transistor device and the second transistor device is housed in a package comprising a second die pad coupled to a source of the second transistor device.

15. The switch circuit of claim 14, wherein the first die pad and the second die pad are mounted on a common conductive layer.

16. The switch circuit of claim 12, wherein a first contact clip is coupled to one of a source and a drain of the first transistor device and a second contact clip is

coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.

17. The switch circuit of claim 16, wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.

18. The switch circuit of claim 12, wherein a source of the first transistor device is coupled to a source of the second transistor device.

19. An electronic component, comprising:

a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

a housing,

wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces.

20. An electronic component, comprising:

means for coupling a control electrode of a compound semiconductor transistor device to a first lead;

means for coupling a first current electrode of the compound semiconductor transistor device to a die pad;

means for coupling a second current electrode of the compound semiconductor transistor device to a second lead; and

means for providing source sensing at a third lead.

ABSTRACT

In an embodiment, an electronic component includes a compound semiconductor transistor device having a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead and a third lead. The first lead, the second lead and the third lead are spaced at a distance from the die pad. The control electrode is coupled to the first lead, the first current electrode is coupled to the die pad and the second current electrode is coupled to the second lead. The third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality.

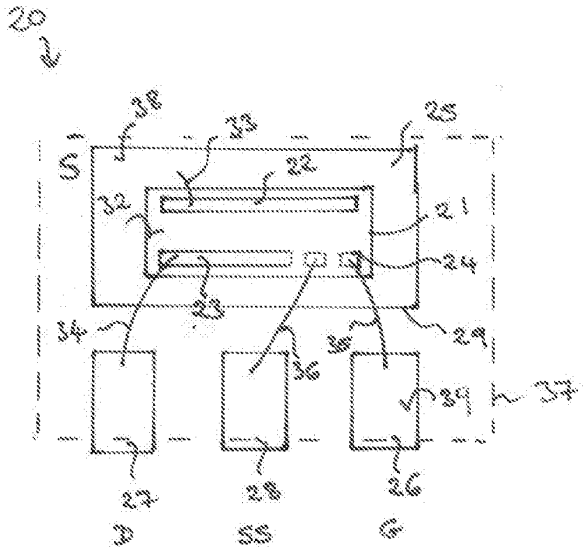

Fig 1a

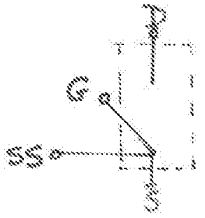

Fig 2

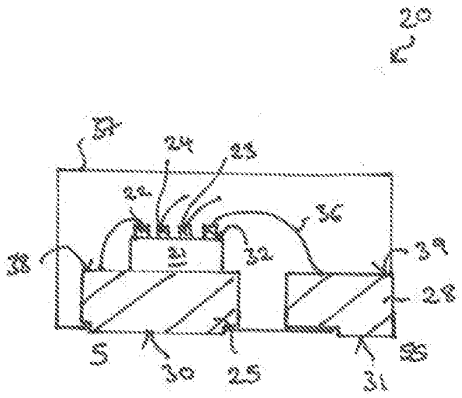

Fig 16

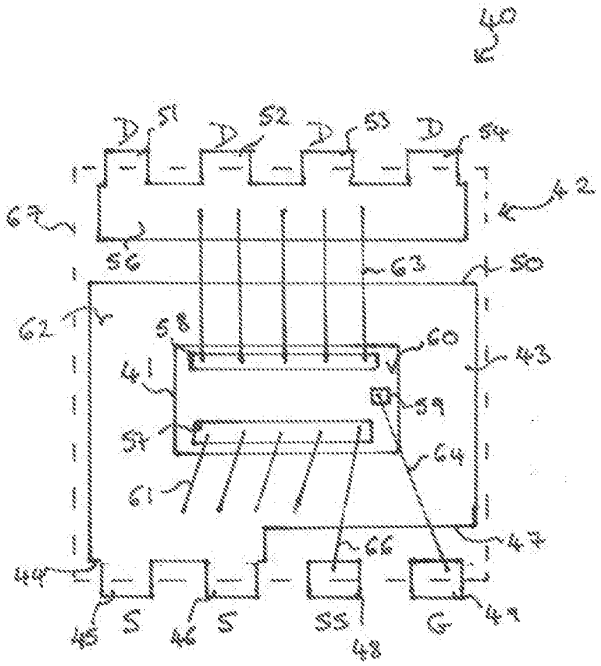
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Fig 3.

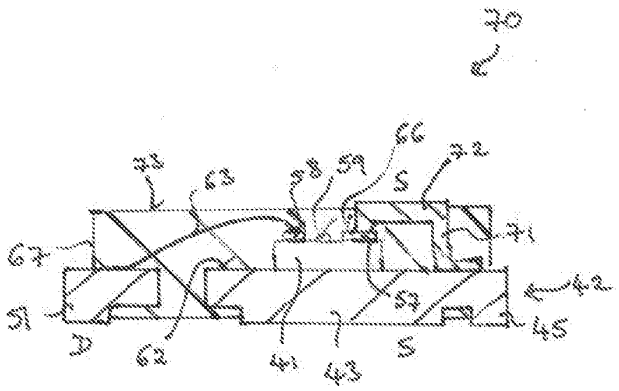

Fig. 4

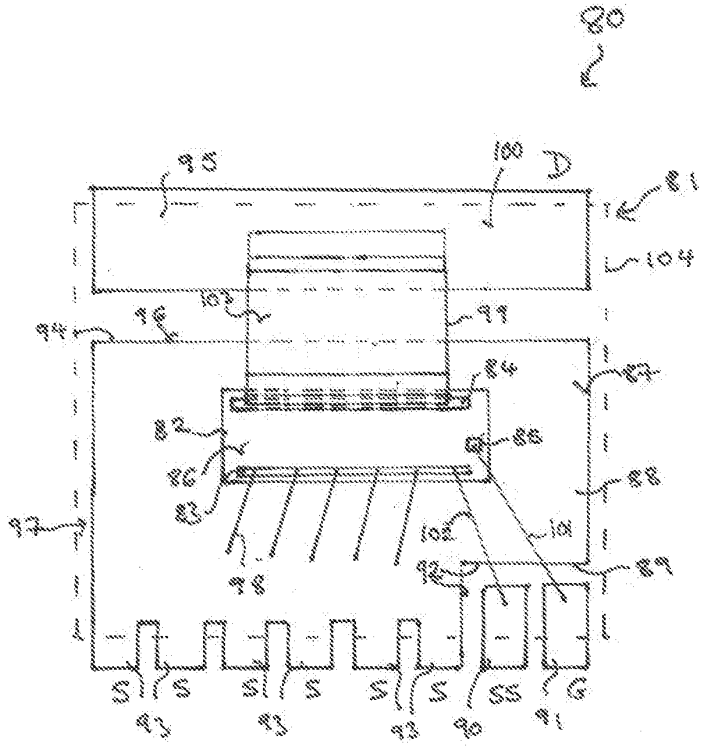
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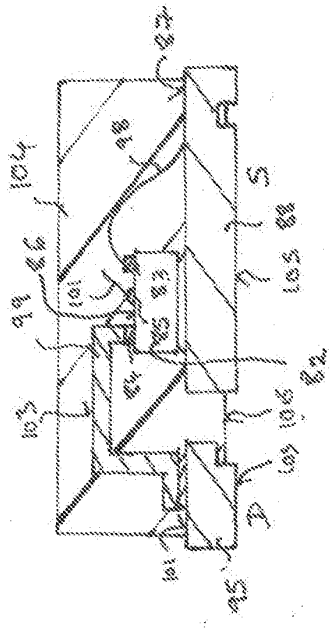
Fig 5



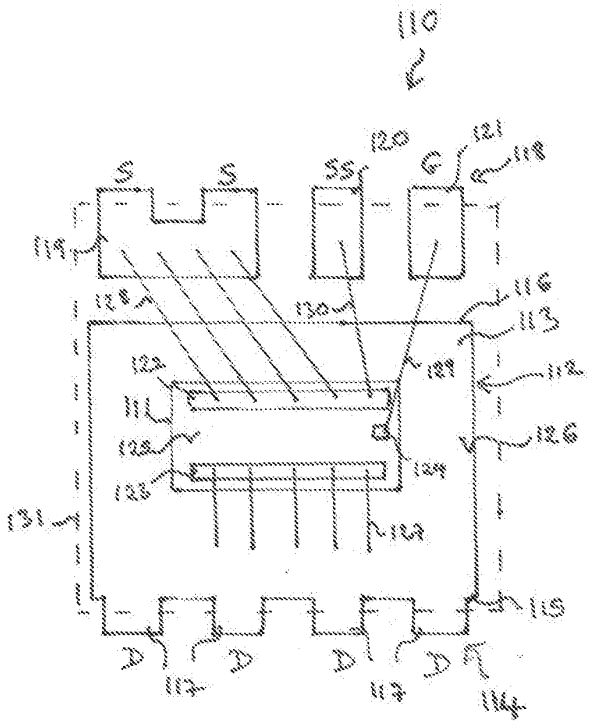

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Fig 7

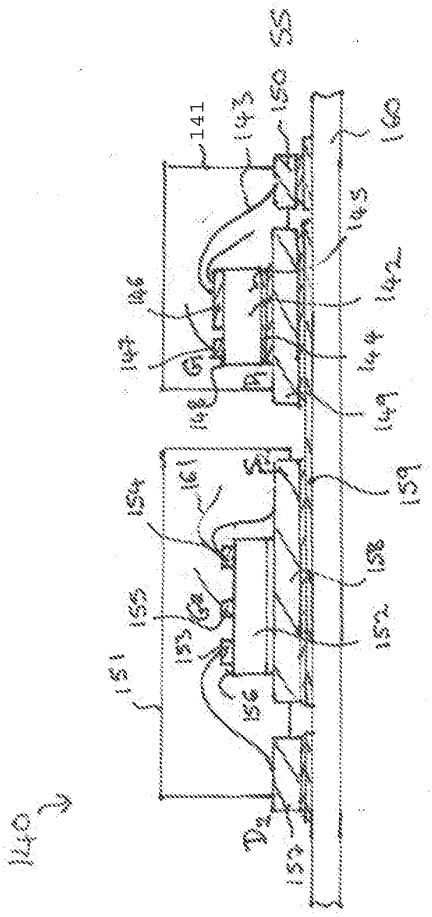
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Fig. 6a

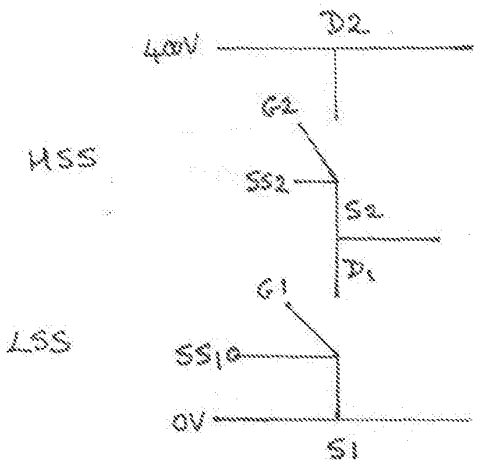

Fig. 8b.

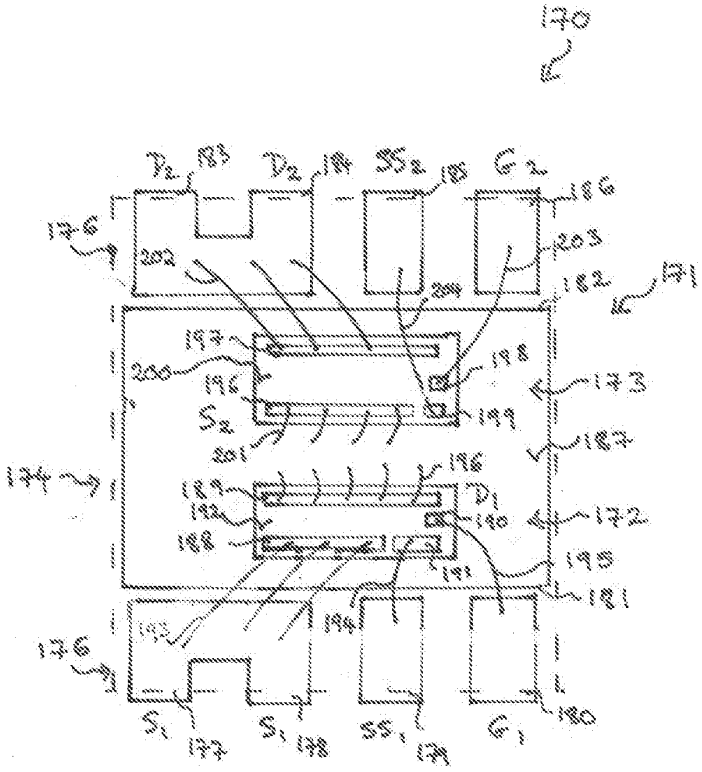
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Fig. 9

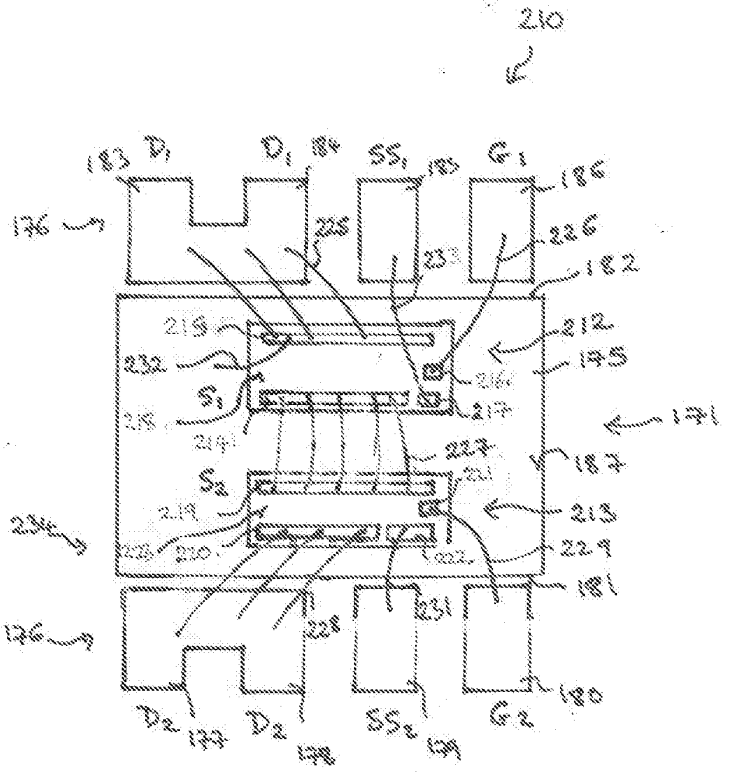

Fig 10a

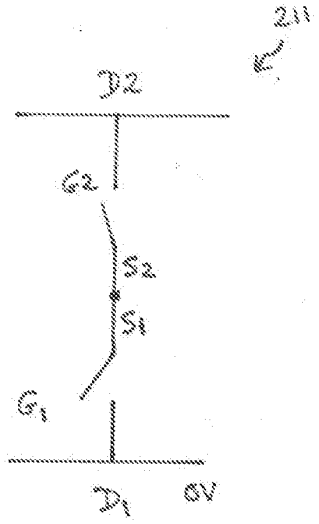

Fig 10b

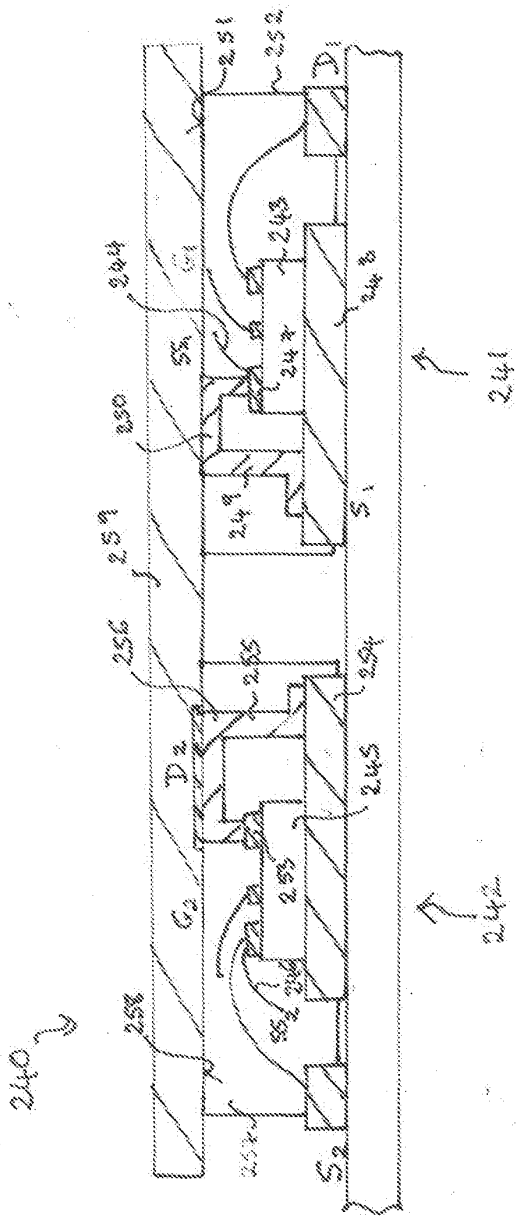
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Fig. 11

DECLARATION AND ASSIGNMENT FOR PATENT AND DESIGN APPLICATIONS

UNITED STATES PATENT RIGHTS, OR
UNITED STATES PLUS ALL FOREIGN PATENT RIGHTS

Electronic Component and Switch Circuit

As a below named inventor (hereinafter designated as the undersigned), I hereby declare that:

This declaration is directed to the application attached hereto. If the application is not attached hereto, the application is as identified by the attorney docket number as set forth above and/or the following:

United States Application Number or PCT International Appln. No. _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

WHEREAS, the undersigned has invented certain at least one claim in the application identified.

WHEREAS, Infineon Technologies Austria AG

of Siemensstrasse 2, 9500 Villach, Austria

its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America and

☒ in any foreign countries.

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, the undersigned has (have) sold, assigned and transferred, and by these considerations does (do) sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America, its territories, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America, its territories, dependencies and possessions, and if the box above is designated, in any and all foreign countries; and to any and all divisions, reissues, continuations, conversions and extensions of all of the above for the full term or terms for which the same may be granted.

The undersigned agrees to execute all papers necessary in connection with this application and any continuing, divisional, conversion or reissue applications thereof or any other proceedings before the United States Patent and Trademark Office and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agrees to execute all papers and documents and to perform any act which may be necessary in connection with claims or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agrees to perform all affirmative acts which may be necessary to obtain a grant of (a) valid United States of America patent(s) and any foreign patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorizes and requests the Patent and Trademark Office Officials in the United States of America and in any foreign countries to issue any and all Letters Patent(s) resulting from said application or any continuing, divisional conversion or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby covenants that he has the full right to convey the entire interest herein assigned, and that he has not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grants the Assignee's legal representatives the power to insert, before or after this document has been executed by the undersigned, any information to identify the instant patent application which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

The undersigned hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment.

The undersigned hereby acknowledges that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

In witness whereof, executed by the undersigned on the date opposite the undersigned name.

Full Name of Inventor: **Klaus Schiess**

Apr. 2016
Date

Inventor Signature

Full Name of Inventor: **Ralf Otremba**

15 04 2016
Date

Inventor Signature

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:	Electronic Component and Switch Circuit			
First Named Inventor/Applicant Name:	Ralf Otremba			
Filer:	Mark Ronald Bilak/Katie Kennedy			
Attorney Docket Number:	1012-1287 / 2015P51742 US			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Independent claims in excess of 3	1201	1	420	420
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		2020

Electronic Acknowledgement Receipt	
EFS ID:	24649745
Application Number:	14997914
International Application Number:	
Confirmation Number:	2194
Title of Invention:	Electronic Component and Switch Circuit
First Named Inventor/Applicant Name:	Ralf Otremba
Customer Number:	57579
Filer:	Mark Ronald Bilak/Katie Kennedy
Filer Authorized By:	Mark Ronald Bilak
Attorney Docket Number:	1012-1287 / 2015P51742 US
Receipt Date:	18-JAN-2016
Filing Date:	
Time Stamp:	17:41:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2020
RAM confirmation Number	12994
Deposit Account	505650
Authorized User	BILAK, MARK R
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	1012-1287_ADS.pdf	1822843 a9208aa5bf1616b1de92e9402a1df63d8dc251be	no	8
Warnings:					
Information:					
2		1012-1287_Application.pdf	1163741 f14cbfb72eff9cfcd2fbfee46d65a68b60335582	yes	50

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	31
	Claims	32	36
	Abstract	37	37
	Drawings-only black and white line drawings	38	50

Warnings:					
Information:					
3	Oath or Declaration filed	1012-1287_Declaration_and_Assignment.pdf	987494 cc1edcbdb48c7d3796dd483b5dafb2893680e1d0	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	36619 5e9a827f32d9fe50257bf37aed13706393f808b0	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4010697		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3699983

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
KLAUS SCHIESS	01/18/2016
RALF OTREMBA	01/15/2016

RECEIVING PARTY DATA

Name:	INFINEON TECHNOLOGIES AUSTRIA AG
Street Address:	SIEMENSSTRASSE 2
City:	VILLACH
State/Country:	AUSTRIA
Postal Code:	9500

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14997914

CORRESPONDENCE DATA

Fax Number: (919)948-3357

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 919-948-3390
Email: official@mbhiplaw.com
Correspondent Name: MURPHY, BILAK & HOMILLER/INFINEON TECHNO
Address Line 1: 1255 CRESCENT GREEN
Address Line 2: SUITE 200
Address Line 4: CARY, NORTH CAROLINA 27518

ATTORNEY DOCKET NUMBER:	1012-1287 / 2015P51742 US
NAME OF SUBMITTER:	MARK R. BILAK
SIGNATURE:	/Mark R. Bilak, Reg. No. 47,423/
DATE SIGNED:	01/18/2016
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2
source=1012-1287_Declaration_and_Assignment#page1.tif
source=1012-1287_Declaration_and_Assignment#page2.tif

DECLARATION AND ASSIGNMENT FOR PATENT AND DESIGN APPLICATIONS

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UNITED STATES PLUS ALL FOREIGN PATENT RIGHTS

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In witness whereof, executed by the undersigned on the date opposite the undersigned name.

Full Name of Inventor: **Klaus Schiess**

10. 01. 2016
Date

Inventor Signature

Full Name of Inventor: **Ralf Otremba**

15.01.2016
Date

Inventor Signature