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SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC (RD)
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SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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DocCode – APPENDIX

SCORE Placeholder Sheet for IFW Content

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- Appendix

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SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE

TECHNICAL FIELD

[0001] The present invention relates, in general, to electronics and, more particularly, to semiconductor structures thereof, and methods of forming semiconductor devices.

BACKGROUND

[0002] In the past, semiconductor manufacturers have used a combination of silicon semiconductor materials and III-N semiconductor materials to manufacture cascoded devices, such as a normally-on III-N depletion mode HEMT cascoded with a silicon device. Using this combination of materials helps achieve a normally-off state using a III-N depletion mode device that is normally-on. In cascoded devices configured as switches, the silicon device often operates in avalanche mode due to high leakage currents of the III-N device operating under a high drain bias. In the avalanche operating mode, the gate of the III-N device is under a large stress in which the absolute gate to source voltage exceeds the devices pinch-off voltage. Hard stress conditions such as operating the silicon device in the avalanche mode degrades device reliability, lowers the breakdown voltage, and increases leakage currents. Cascoded semiconductor devices have been described in U.S. Patent Application Publication Number 2013/0088280 A1 by Rakesh K. Lai et al. and published on April 11, 2013.

[0003] After manufacturing cascoded devices from different semiconductor substrate materials, semiconductor component manufacturers typically protect the silicon device and the depletion mode devices in separate packages and connect the devices in the separate packages together via leadframe leads to form a cascode device. A drawback with this approach is that increasing the number of packages increases the cost of a cascoded semiconductor component and degrades the performance of the cascoded devices because of increased parasitics such as parasitic capacitance and parasitic inductance.

[0004] Accordingly, it would be advantageous to have a cascoded semiconductor device and a method for manufacturing the cascoded semiconductor

device. It would be of further advantage for the structure and method to be cost efficient to implement.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures, in which like reference characters designate like elements and in which:

[0006] FIG. 1 is a perspective view of a semiconductor component in a cascode configuration in accordance with an embodiment of the present invention;

[0007] FIG. 2 is a cross-sectional view of the semiconductor component of FIG. 1 taken along section line 2-2 of FIG. 1;

[0008] FIG. 3 is a bottom view of the semiconductor component of FIGs. 1 and 2;

[0009] FIG. 4 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00010] FIG. 5 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00011] FIG. 6 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00012] FIG. 7 is a cross-sectional view of the semiconductor component of FIG. 6 taken along section line 7-7 of FIG. 6;

[00013] FIG. 8 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00014] FIG. 9 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00015] FIG. 10 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00016] FIG. 11 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention;

[00017] FIG. 12 is a cross-sectional view of the semiconductor component of FIG. 11 taken along section line 12-12 of FIG. 11; and

[00018] FIG. 13 is a perspective view of a semiconductor component in a cascode configuration in accordance with another embodiment of the present invention.

[00019] For simplicity and clarity of illustration, elements in the figures are not necessarily to scale, and the same reference characters in different figures denote the same elements. Additionally, descriptions and details of well-known steps and elements are omitted for simplicity of the description. As used herein current carrying electrode means an element of a device that carries current through the device such as a source or a drain of an MOS transistor or an emitter or a collector of a bipolar transistor or a cathode or anode of a diode, and a control electrode means an element of the device that controls current flow through the device such as a gate of an MOS transistor or a base of a bipolar transistor. Although the devices are explained herein as certain n-channel or p-channel devices, or certain n-type or p-type doped regions, a person of ordinary skill in the art will appreciate that complementary devices are also possible in accordance with embodiments of the present invention. It will be appreciated by those skilled in the art that the words during, while, and when as used herein are not exact terms that mean an action takes place instantly upon an initiating action but that there may be some small but reasonable delay, such as a propagation delay, between the reaction that is initiated by the initial action. The use of the words approximately, about, or substantially means that a value of an element has a parameter that is expected to be very close to a stated value or position. However, as is well known in the art there are always minor variances that prevent the values or positions from being exactly as stated. It is well established in the art that variances of up to about ten per cent (10%) (and up to twenty per cent (20%) for semiconductor doping concentrations) are regarded as reasonable variances from the ideal goal of exactly as described.

DETAILED DESCRIPTION

[00020] FIG. 1 is a perspective view of a semiconductor component 10 in accordance with an embodiment of the present invention and FIG. 2 is a cross-sectional view of semiconductor component 10 taken along section line 2-2 of FIG. 1. FIGs. 1 and 2 are described together. What is shown in FIGs. 1 and 2 are a molded device support structure 12 having a top surface 14 and a bottom surface 16. Molded support structure 12 includes a device receiving area 18, a device receiving area 20, and a bond pad 22 at top surface 14 and a contact 24 at bottom surface 16. Device receiving areas

18 and 20 may be referred to as device receiving structures. Device receiving area 18 is configured for receiving a compound semiconductor device such as, for example, a III-nitride device whereas device receiving area 20 is configured for receiving a silicon semiconductor device. In accordance with an embodiment, device receiving area 18, device receiving area 20, and bond pad 22 are substantially coplanar with surface 14. Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 12. Molded support structure 12 may be formed by placing an electrically conductive strip in a mold having a mold cavity and injecting a mold compound into the mold cavity. The electrically conductive strip may include pads or plates 18 and 20 that serve as device receiving areas, an interconnect structure 21 that includes bond pad 22 integrally formed with contact 24 through a conductor 25, and a plurality of leadframe leads such as, for example, leadframe leads 26, 28, and 30. After injecting the mold compound into the cavities, the electrically conductive strip may be singulated into a plurality of molded support structures 12. Suitable materials for the electrically conductive strips include copper, aluminum, or the like. As mentioned, molded support structure 12 is illustrated and described as a single element; however, it may be a portion singulated from a leadframe strip encapsulated in a mold compound.

[00021] A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically insulating die attach material 42. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. It should be noted that semiconductor device 48 is not limited to being a field effect transistor. For example, semiconductor device 48 may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited

to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.

[00022] A semiconductor chip 60 is bonded to surface 20A of device receiving area 20 using die attach material 42. In accordance with an embodiment, semiconductor chip 60 is a silicon chip having opposing major surfaces 64 and 66, wherein semiconductor chip 60 includes a vertical field effect semiconductor device having a drain contact 75 formed on or from surface 64, a source contact 72 formed on or from a portion of surface 66, and a gate contact 74 formed on or from another portion of surface 66. Drain contact 75 is bonded to surface 20A of device receiving area 20 through die attach material 42. It should be noted that semiconductor device 60 is not limited to being a vertical field effect transistor or a field effect transistor. For example, the semiconductor device may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. By way of example, semiconductor chip 60 is a silicon semiconductor chip, i.e., the substrate material of silicon semiconductor chip 40 comprises silicon. A silicon semiconductor material may be referred to as silicon based semiconductor material, a silicon semiconductor material, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 60, semiconductor chip 60 may be referred to as a semiconductor device.

[00023] Drain contact 50 of semiconductor device 40 is electrically connected to bond pad 22 through bond wires 76, source contact 52 of semiconductor device 40 is electrically connected to device receiving area 20 through bond wires 78, gate contact 54 of semiconductor device 40 is electrically connected to source contact 72 through a bond wire 80, and gate contact 55 of semiconductor device 40 is electrically connected to leadframe lead 30 through a bond wire 82. Gate contact 74 of semiconductor device 60 is electrically connected to leadframe lead 26 through a bond wire 84, source contact 72 is connected to surface leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, and drain contact 75 is electrically connected to surface 20A of device receiving area 20 through electrically conductive die attach material 42.

It should be noted that gate contact 54 is electrically conducted to gate contact 55 through a metallization system (not shown). Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment semiconductor devices 40 and 60 are electrically connected to device receiving areas 18 and 20, respectively through electrically conductive die attach material 42.

[00024] As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40 and 60, and bond wires 76, 78, 80, 82, 84, 86, and 88 and portions of molded support structure 12 may be encapsulated in a protection material 90 such as, for example a mold compound. It should be noted that leadframe lead 26 serves as a gate leadframe lead or a gate lead, leadframe lead 28 serves as a Kelvin leadframe lead or a Kelvin lead, leadframe lead 30 servers as a source leadframe lead or a source lead, and contact 24 serves as a drain contact.

[00025] Thus, semiconductor component 10 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are not formed over active regions of semiconductor device 40.

[00026] FIG. 3 is a bottom view of semiconductor component 10 in accordance with an embodiment of the present invention. FIG. 3 further illustrates contact 24 and leadframe leads 26, 28, and 30.

[00027] FIG. 4 is a perspective view of a semiconductor component 100 in accordance with another embodiment of the present invention. Semiconductor component 100 is similar to semiconductor component 10 except that bond wires 76 have been replaced by an electrically conductive clip 102, bond wires 78 have been replaced by an electrically conductive clip 104, and bond wires 88 have been replaced by an electrically conductive clip 106. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, have been described with reference to FIGs. 1 and 2. Thus, semiconductor component 100 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are not formed over active regions of semiconductor device 40.

[00028] As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40 and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 may be encapsulated in a protection material such as, for example a mold compound.

[00029] FIG. 5 is a perspective view of a semiconductor component 120 in accordance with another embodiment of the present invention. Semiconductor component 120 is similar to semiconductor component 10 except that semiconductor component 120 includes bond wires 122 connecting source electrode 72 with surface 18A of device receiving area 18. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, has been described with reference to FIGs. 1 and 2. Bond wires 122 electrically connect source electrode 72, hence the source, of semiconductor device 60 to the body of semiconductor material of semiconductor device 40 through die receiving area 18 and die attach material 42. Thus, semiconductor component 120 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is grounded and bond pads are not formed over active regions of semiconductor device 40.

[00030] As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40 and 60, and bond wires 76, 78, 80, 82, 84, 86, and 88 and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound.

[00031] FIG. 6 is a perspective view of a semiconductor component 130 in accordance with another embodiment of the present invention. FIG. 7 is a cross-sectional view of semiconductor component 130 taken along section line 7-7 of FIG. 6. FIGs. 6 and 7 are described together. What is shown in FIGs. 6 and 7 are a molded device support structure 132 having a top surface 134 and a bottom surface 136. Molded support structure 132 includes a device receiving area 138, a bond pad 140 at top surface 134, and a contact 142 at bottom surface 136. In accordance with an embodiment, bond pads 138 and 140 are coplanar with surface 134. Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 132. Device receiving area 138 may be referred to as a device receiving structure. Molded support structure 132 may be formed by placing an electrically conductive strip in a mold having a mold cavity and injecting a mold compound into the mold cavity. The electrically conductive strip may include a pad or plate 138 having a contact region 140, wherein pad or plate 138 serves as a device receiving area, and a plurality of leadframe leads such as, for example, leadframe leads 26, 28, and 30. After injecting the mold compound into the cavities, the electrically conductive strip may be singulated into a plurality of molded support structures 132. Suitable materials for the electrically

conductive strips include copper, aluminum, or the like. As mentioned, molded support structure 132 is illustrated and described as a single element; however, it may be a portion singulated from a leadframe strip encapsulated in a mold compound.

[00032] A semiconductor chip 40 is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. Thus, surface 44 of semiconductor chip 40 is bonded to surface 138A of device receiving area 138 through die attach material 42. It should be noted that semiconductor device 40 is not limited to being a field effect transistor. For example, semiconductor device 40 may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. As discussed above, in accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device.

[00033] Drain contact 50 of semiconductor device 40 is electrically connected to surface 138A of device receiving area 138 through bond wires 76, source contact 52 of semiconductor device 40 is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact 54 of semiconductor device 40 is electrically connected to leadframe lead 26 through bond wire 84, gate contact 55 is electrically connected to leadframe lead 30 through a bond wire 82, and bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 85. In accordance with the embodiment of FIG. 6, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50 of semiconductor device 40 is electrically connected to surface 138A of device receiving area 138. Thus, semiconductor component 130 includes a III-N cascode switch in which the substrate of the III-N semiconductor

material is electrically floating and bond pads are not formed over active regions of semiconductor device 40.

[00034] As those skilled in the art are aware, device receiving area 138, semiconductor chip 40, and bond wires 76, 82, 84, 86, and 88 and portions of molded support structure 132 are typically encapsulated in a protection material such as, for example a mold compound.

[00035] FIG. 8 is a perspective view of a semiconductor component 140 in accordance with another embodiment of the present invention. Semiconductor component 140 is similar to semiconductor component 130 except that semiconductor component 140 includes bond pad 141 and a bond wire 142, wherein bond wire 142 connects device receiving area 138 with leadframe lead 30 and a bond pad 141 is connected to drain contact 50 through bond wires 76, unlike semiconductor component 130 in which bond wires 76 connect drain contact 50 with device receiving area 138. Bond pad 141 is spaced apart from device receiving area 138. It should be noted that gate leadframe lead 26 is electrically connected to gate electrode 54 via bond wire 84 and to bond pad 140 through bond wire 85. It should be further noted that mounting semiconductor chip 40 to device receiving area 138 has been described with reference to FIGs. 6 and 7. Bond wire 142 electrically connects the substrate of semiconductor chip 40 to source electrode 52 of semiconductor device 40 through leadframe lead 30, hence the source, of semiconductor device 40 is electrically connected to the body of or semiconductor material of semiconductor device 40. Thus, semiconductor component 140 includes a discrete III-N field effect transistor in which the substrate of the III-N semiconductor material is grounded and bond pads are not formed over active regions of semiconductor device 40.

[00036] As those skilled in the art are aware, device receiving area 138, semiconductor chip 40, and bond wires 76, 82, 84, 85, 86, and 88 and portions of molded support structure 132 are typically encapsulated in a protection material such as, for example a mold compound.

[00037] FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has

been replaced by a drain contact 50A which extends over a portion of an active area of III-N of semiconductor device 40A and source contact 52 has been replaced by a source contact 52A which extends over another portion of the active area of III-N of semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGs. 1 and 2. Thus, semiconductor component 150 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.

[00038] As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound.

[00039] FIG. 10 is a perspective view of a semiconductor component 160 in accordance with another embodiment of the present invention. Semiconductor component 160 is similar to semiconductor component 120 described with reference to FIG. 5 except that drain contact 50 has been replaced by a drain contact 50B which extends over a portion of an active area of III-N of semiconductor device 40B, source contact 52 has been replaced by a source contact 52B which extends over another portion of the active area of III-N of semiconductor device 40B, and gate contacts 54 and 55 have been replaced by a gate contact 54B which extends over another portion of the active area of III-N semiconductor device 40B, bond wire 80 has been replaced by bond wires 80B, and bond wire 82 is not present in the embodiment of FIG. 10. Similarly, a reference character B has been appended to reference character 40 to distinguish a semiconductor chip having bond pads over active areas from a semiconductor chip without bond pads over active areas. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGs. 1 and 2. Thus, semiconductor component 160 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically grounded and bond pads are formed over active regions of semiconductor device 40B.

[00040] As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40B and 60, and bond wires 76, 78, 80B, 84, 86, 88, and 122, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound.

[00041] FIG. 11 is a perspective view of a semiconductor component 170 in accordance with another embodiment of the present invention. FIG. 12 is a cross-sectional view of semiconductor component 170 taken along section line 12-12 of FIG. 11. FIGs. 11 and 12 are described together. What is shown in FIGs. 11 and 12 are a molded device support structure 132 that includes device receiving area 138 and bond pad 140, and leadframe leads 26, 28, and 30. Molded device support structure 132 has been described with reference to FIGs. 6 and 7.

[00042] A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.

[00043] Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact 54B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N

semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.

[00044] FIG. 13 is a perspective view of a semiconductor component 180 in accordance with another embodiment of the present invention. Semiconductor component 180 is similar to semiconductor component 170 except that semiconductor component 180 includes a bond wire 182 connecting leadframe lead 30 with surface 138A of device receiving area 138. Bond wire 182 electrically connects source electrode 52B, hence the source of semiconductor device 40B, to the substrate of the semiconductor material of semiconductor device 40B. Thus, semiconductor component 180 includes a III-N cascode switch in which the substrate of the III-N semiconductor device is grounded and bond pads are formed over active regions of semiconductor device 40.

[00045] Although certain preferred embodiments and methods have been disclosed herein, it will be apparent from the foregoing disclosure to those skilled in the art that variations and modifications of such embodiments and methods may be made without departing from the spirit and scope of the invention. It is intended that the invention shall be limited only to the extent required by the appended claims and the rules and principles of applicable law.

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor component having at least first and second terminals, comprising:

a support having first and second sides and a plurality of leads, the first side of the support having a first device receiving structure and a first interconnect structure and the second side of the support having second interconnect structure;

a first semiconductor device mounted to the first device receiving structure, the first semiconductor device having a control terminal and first and second current carrying terminals and configured from a III-N semiconductor material;

a first electrical interconnect coupled between the control terminal of the first semiconductor device and a first lead of the plurality of leads;

a second electrical interconnect coupled between the first current carrying terminal of the first semiconductor device and a second lead of the plurality of leads; and

a third electrical interconnect coupled between the second current carrying terminal of the first semiconductor device and one of the first device receiving structure or the first interconnect structure.

2. The semiconductor component of claim 1, wherein the first semiconductor device is a gallium nitride semiconductor device.

3. The semiconductor component of claim 1, wherein the first semiconductor device is a first field effect transistor having a control electrode and first and second current carrying electrodes, the control electrode of the first field effect transistor serving as the control terminal, the first current carrying electrode of the first field effect transistor serving as the first current carrying terminal, and the second current carrying electrode of the first transistor serving as the second current carrying terminal.

4. The semiconductor component of claim 1, further including a fourth electrical interconnect coupled between the first current carrying terminal of the first semiconductor device and a third lead of the plurality of leads.

5. The semiconductor component of claim 4, wherein the first electrical interconnect is a bond wire, the second electrical interconnect is a bond wire, and the third electrical interconnect is a bond wire.

6. The semiconductor component of claim 4, further including a fifth electrical interconnect coupled between the first lead and the first interconnect structure and a sixth electrical interconnect coupled between the first interconnect structure and the control terminal of the first semiconductor device.

7. The semiconductor component of claim 6, further including a seventh electrical interconnect coupled between the semiconductor component receiving structure and the third lead of the plurality of leads.

8. The semiconductor component of claim 4, further including a fifth electrical interconnect coupled between the semiconductor component receiving structure and the third lead of the plurality of leads.

9. The semiconductor component of claim 4, wherein the support further includes a second interconnect structure, and wherein the third electrical interconnect is coupled between the second current carrying terminal of the first semiconductor device and the first interconnect structure.

10. The semiconductor component of claim 9, further including a fifth electrical interconnect coupled between the semiconductor component receiving structure and the third lead of the plurality of leads.

11. A semiconductor component, comprising:

a support having first and second sides and a plurality of leads, the first side of the support having a first device receiving structure, a second device receiving structure, and a first interconnect structure and the second side of the support having second interconnect structure;

a first semiconductor device mounted to the first device receiving structure, the first semiconductor device having a control terminal and first and second current carrying terminals and configured from a III-N semiconductor material;

a second semiconductor device mounted to the second device receiving structure, the second semiconductor device having a control terminal and first and second current carrying terminals;

a first electrical interconnect coupled between the control terminal of the second semiconductor device and a first lead of the plurality of leads;

a second electrical interconnect coupled between the first current carrying terminal of the second semiconductor device and a second lead of the plurality of leads;

a third electrical interconnect coupled between the second current carrying terminal of the second semiconductor device and a first current carrying terminal of the first semiconductor device;

a fourth electrical interconnect coupled between the second current carrying terminal of the first semiconductor device and the first interconnect structure; and

a fifth electrical interconnect coupled between the control terminal of the first semiconductor device and the first current carrying terminal of the second semiconductor device.

12. The semiconductor component of claim 11, further including a sixth electrical interconnect coupled between the first current carrying terminal of the second semiconductor device and the first device receiving structure.

13. The semiconductor component of claim 12, further including a seventh electrical interconnect coupled between the first current carrying terminal of the second semiconductor device and a third lead of the plurality of leads.

14. The semiconductor component of claim 11, further including a sixth electrical interconnect coupled between the first current carrying terminal of the second semiconductor device and a third lead of the plurality of leads.

15. The semiconductor component of claim 14, wherein the third electrical interconnect, the fourth electrical interconnect, and the sixth electrical interconnect are clips or bond wires.

16. The semiconductor component of claim 11, wherein the first current carrying terminal and the second current carrying terminal of the first semiconductor device are configured to be over active areas of the semiconductor device.

17. The semiconductor component of claim 11, wherein the support comprises a mold compound having first and second surfaces that are opposite to each other and a third surface that is perpendicular to the first and second surfaces, and wherein the plurality of leads extend from the first surface, the first device receiving structure is a first electrically conductive material embedded in the mold compound, the first device receiving structure is a second electrically conductive material embedded in the mold compound, and the first interconnect structure is a third electrically conductive material embedded in the mold compound.

18. The semiconductor component of claim 17, wherein the electrically conductive material of the first device receiving structure extends through the mold compound from the first surface to the second surface of the mold compound.

19. The semiconductor component of claim 11, wherein the second semiconductor device is a silicon based semiconductor device.

20. A method for manufacturing a semiconductor component, comprising:

forming a support having first and second sides and second sides that are parallel to each other and a third side that is perpendicular to the first side and the second side, wherein the support has a plurality of leads extending from the third side and a device receiving structure extending from the first side into the support;

mounting a first semiconductor device to the first device receiving structure, the first semiconductor device having a control terminal and first and second current carrying terminals and configured from a III-N semiconductor material;

electrically coupling the control terminal of the first semiconductor device to a first lead of the plurality of leads;

electrically coupling first current carrying terminal of the first semiconductor device to a second lead of the plurality of leads; and

electrically coupling the second current carrying terminal of the first semiconductor device to one of the first device receiving structure or the first interconnect structure.

ABSTRACT

In accordance with an embodiment, a semiconductor component includes a support having a side in which a device receiving structure and an interconnect structure are formed and a side from which a plurality of leads extends. A semiconductor device having a control terminal and first and second current carrying terminals and configured from a III-N semiconductor material is mounted to the device receiving structure. The control terminal of the first electrical interconnect is coupled to a first lead by a first electrical interconnect. A second electrical interconnect is coupled between the first current carrying terminal of the semiconductor device and a second lead. The second current carrying terminal of the first semiconductor device is coupled to the device receiving structure or to the interconnect structure.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chun-Li		Liu	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Scottsdale	State/Province	AZ	Country of Residence i	US

Mailing Address of Inventor:

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Postal Code	85008	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ali		Salih	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

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Mailing Address of Inventor:

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Postal Code	85008	Country i	US

Inventor 3 Remove

Legal Name

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	Mingjiao		Liu	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

City	Gilbert	State/Province	AZ	Country of Residence i	US

Mailing Address of Inventor:

Address 1	c/o ON Semiconductor, 5005 E. McDowell Rd.		
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City	Phoenix	**State/Province**	AZ
Postal Code	85008	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	132192		
Email Address	patents@onsemi.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE		
Attorney Docket Number	ONS01639	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	7	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

Customer Number	132192

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

○ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Semiconductor Components Industries, LLC

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

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Address 2	MD A700		
City	Phoenix	**State/Province**	AZ
Country i	US	Postal Code	85008
Phone Number	602-244-6648	Fax Number	602-244-3169
Email Address	patents@onsemi.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

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Assignee 1

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Organization Name	Semiconductor Components Industries, LLC

Mailing Address Information:			
Address 1	5005 E. McDowell Road		
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City	Phoenix	**State/Province**	AZ
Country i	US	Postal Code	85008
Phone Number	602-244-6648	Fax Number	602-244-3169
Email Address	patents@onsemi.com		

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Signature:

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Signature	/Rennie William Dover/	Date (YYYY-MM-DD)	2015-07-20

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ONS01639
	Application Number	
Title of Invention	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	

First Name	Rennie	Last Name	Dover	Registration Number	36503
Additional Signature may be generated within this form by selecting the Add button.				Add	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

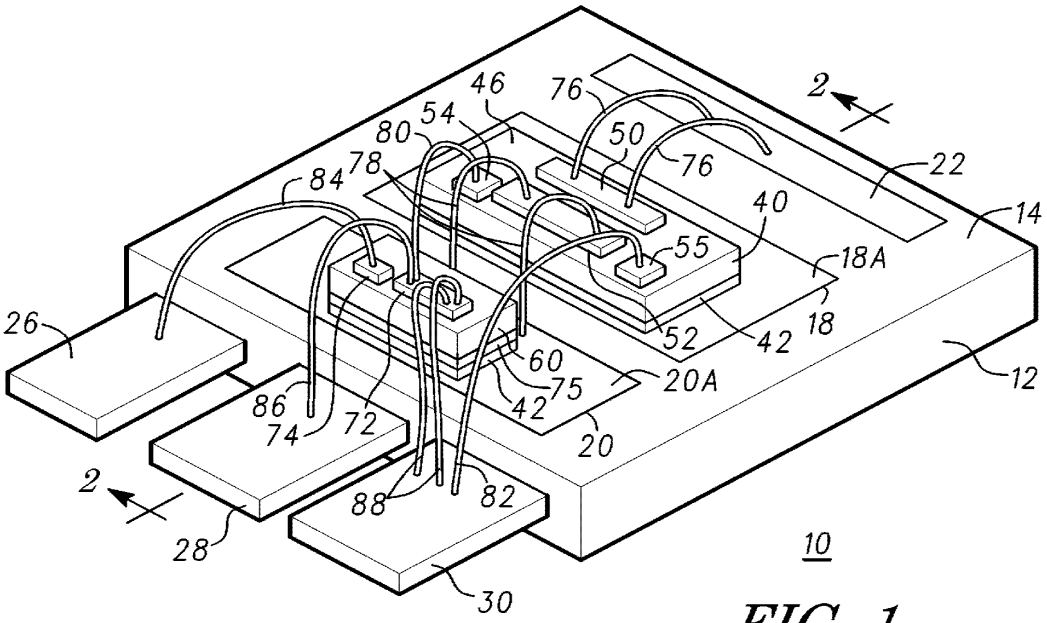
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FIG. 1

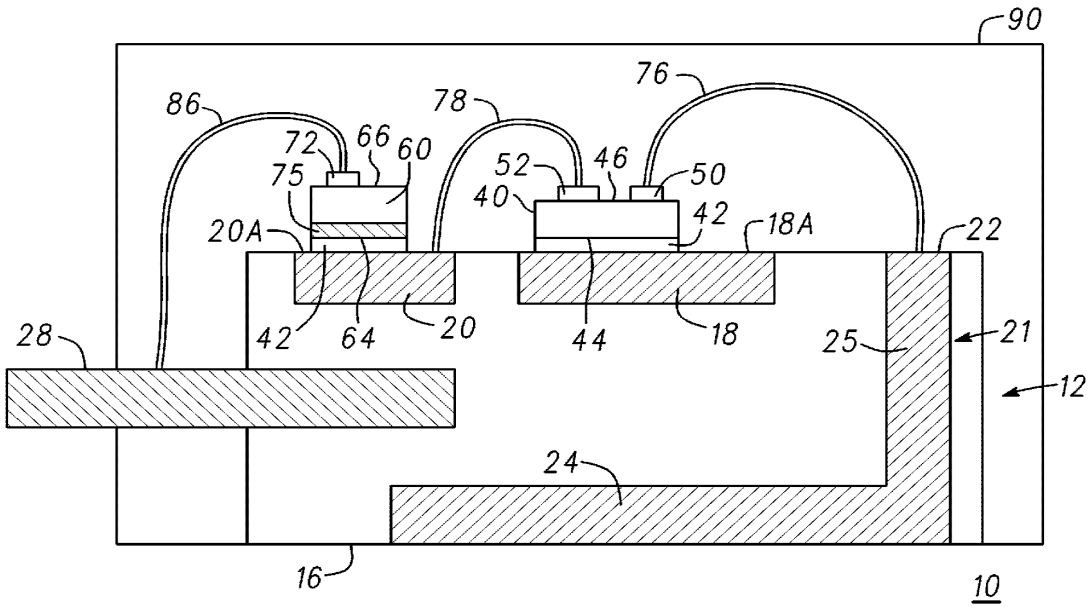
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FIG. 2

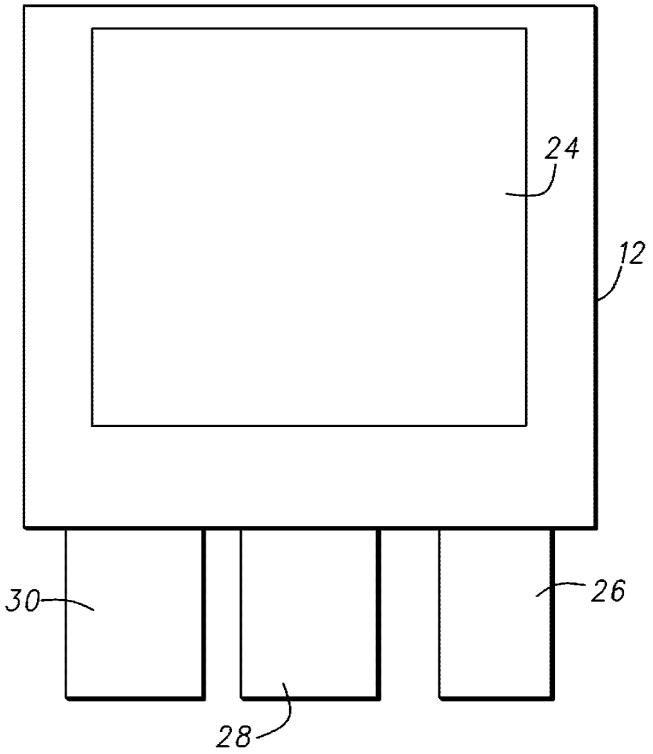

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FIG. 3

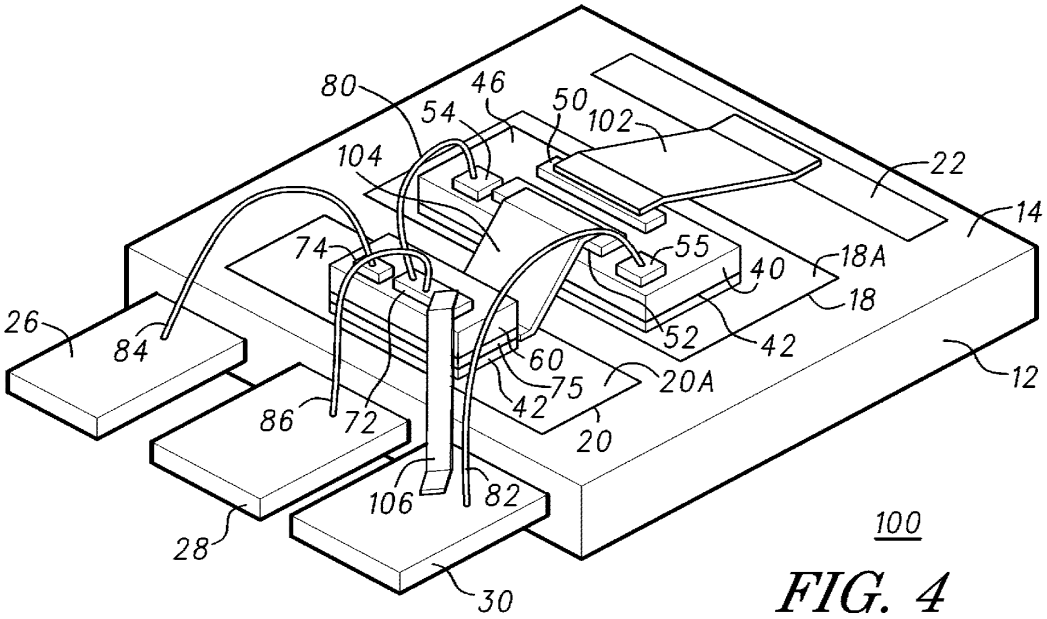

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FIG. 4

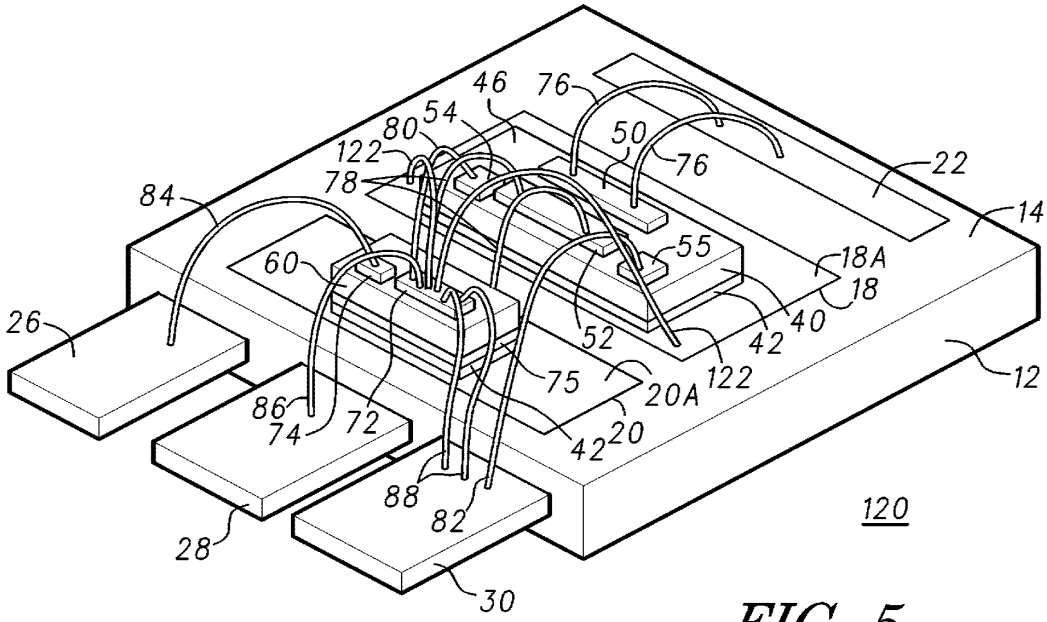
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FIG. 5

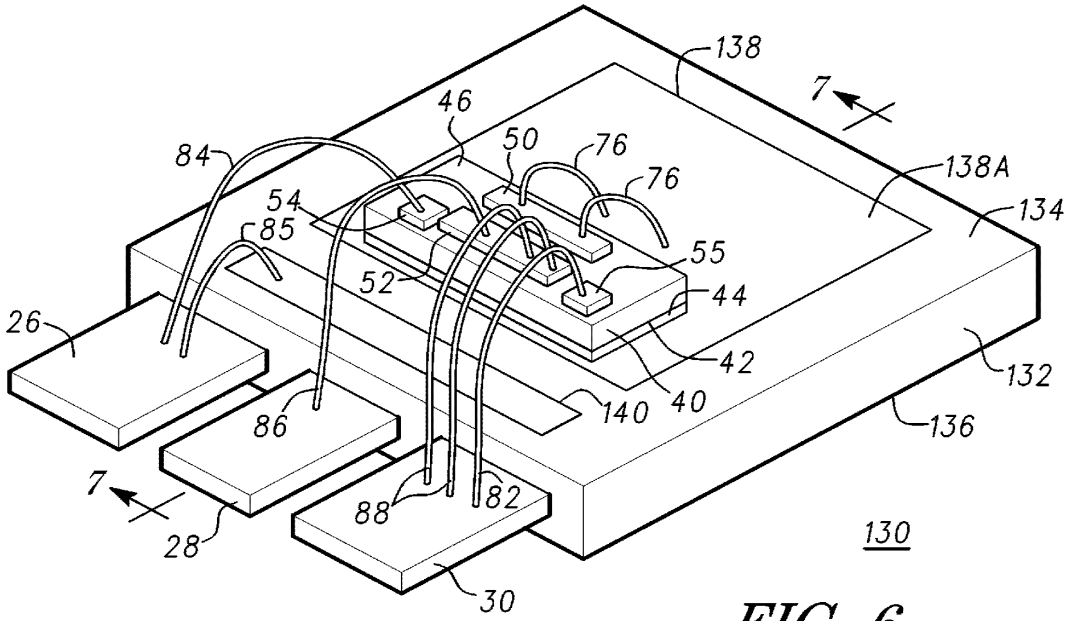
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FIG. 6

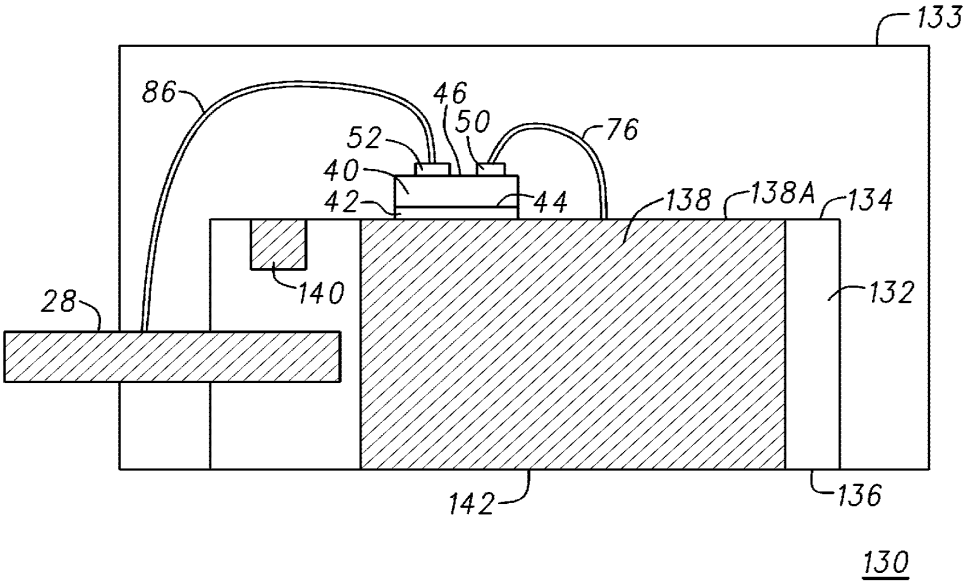
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FIG. 7

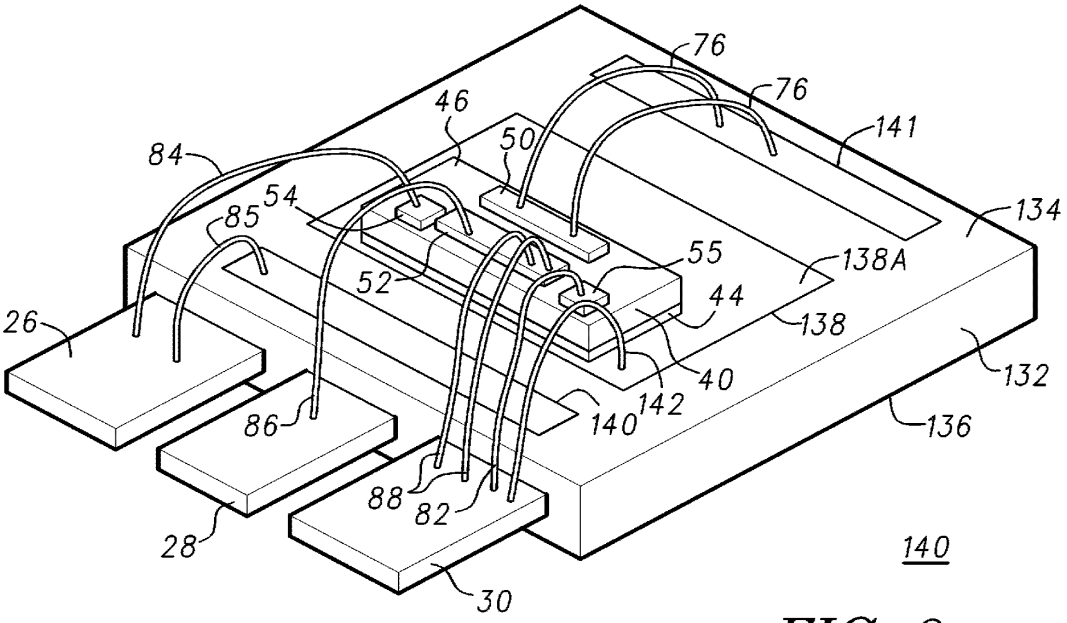
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FIG. 8

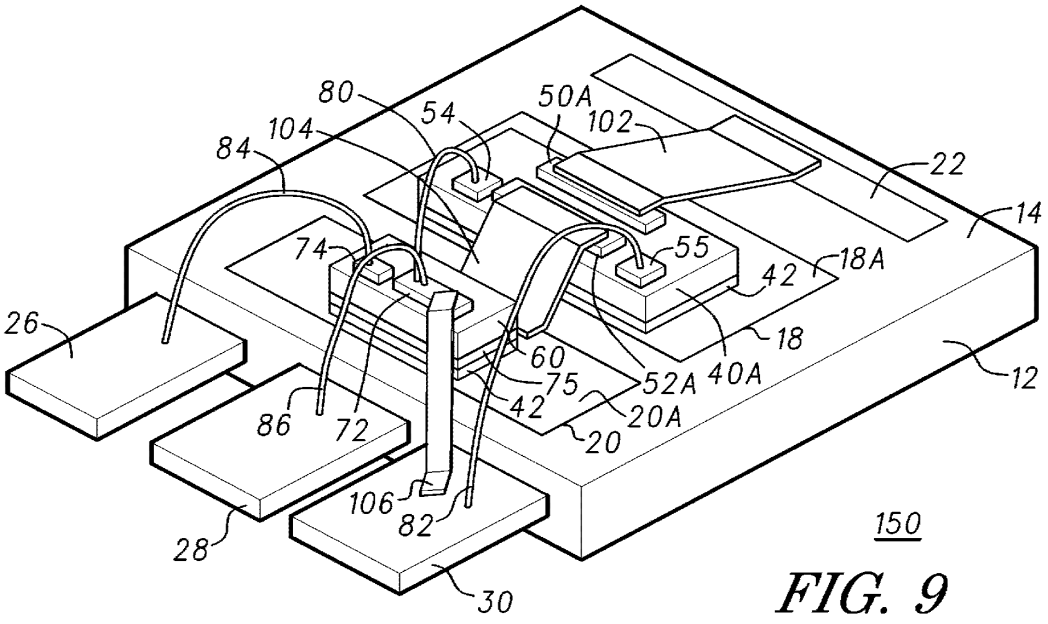
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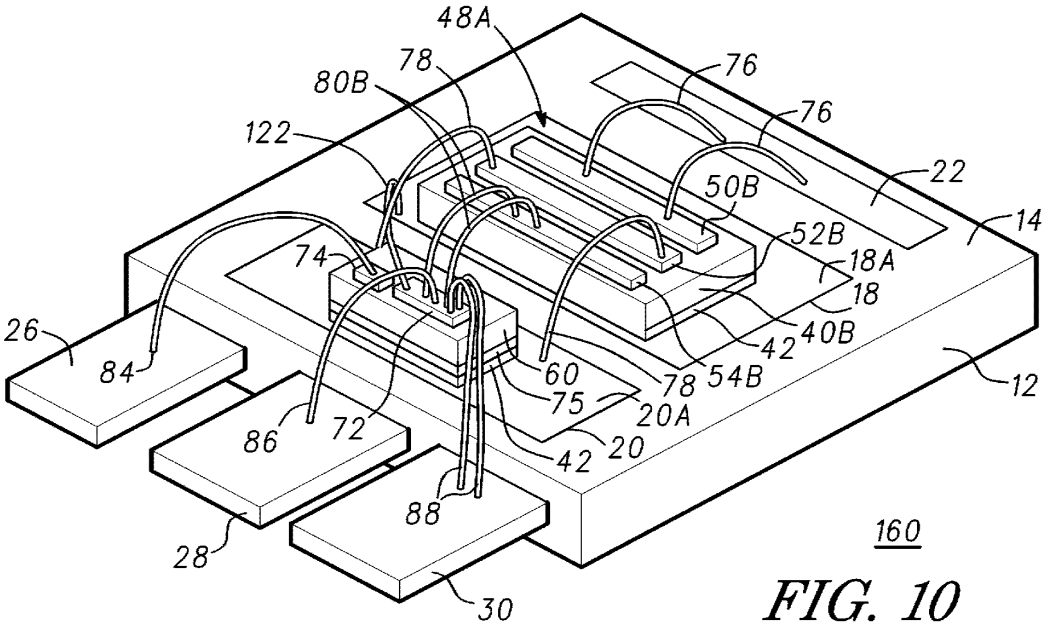
FIG. 9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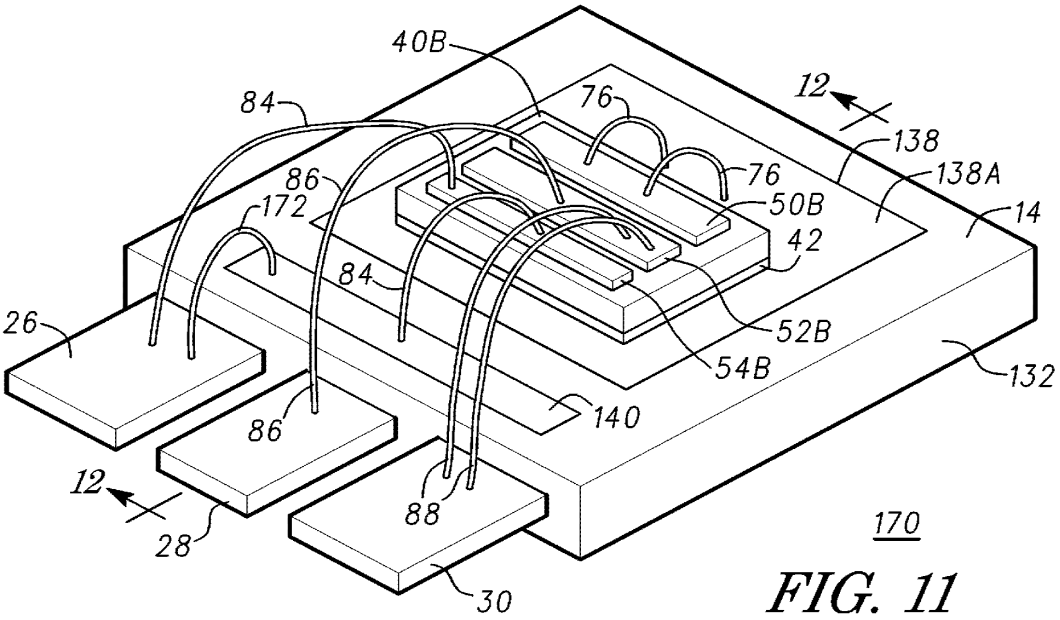
84
60
78
54B
12
75
20A
86
72
42
20
88
28
30
160

FIG. 10


40B
84
76
12
138
138A
14
86
172
76
50B
42
84
26
52B
54B
132
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140
12
88
28
30
170

FIG. 11

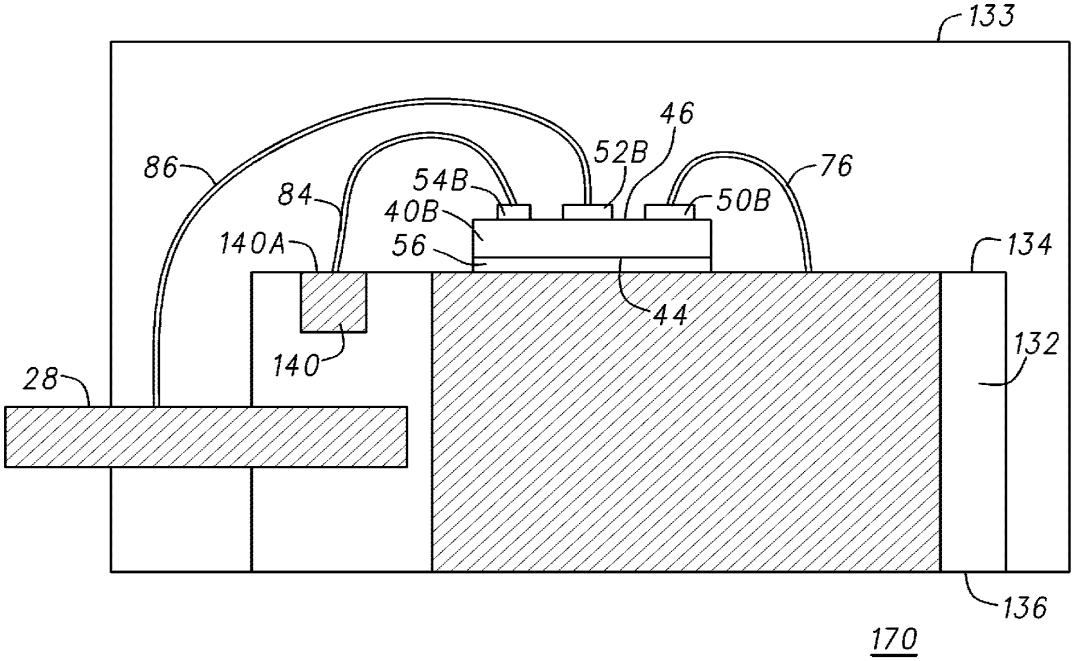

133
46
86
52B
76
84
54B
50B
40B
140A
56
134
44
132
140
28
136
170

FIG. 12

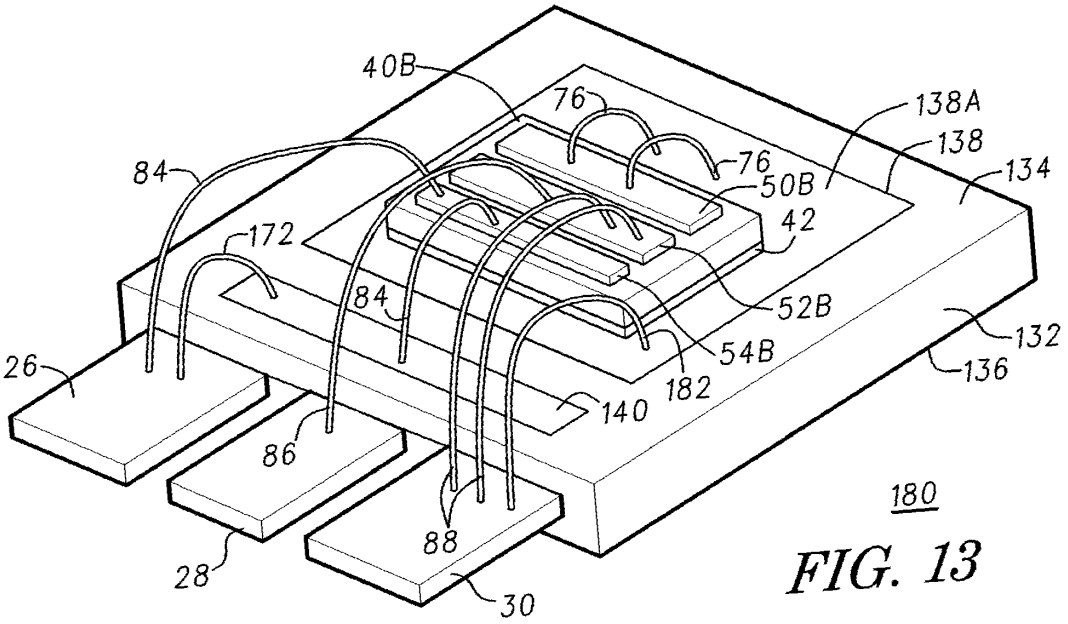

40B
76
138A
138
134
84
76
50B
42
172
84
52B
132
54B
26
182
136
140
86
180
88
28
30

FIG. 13

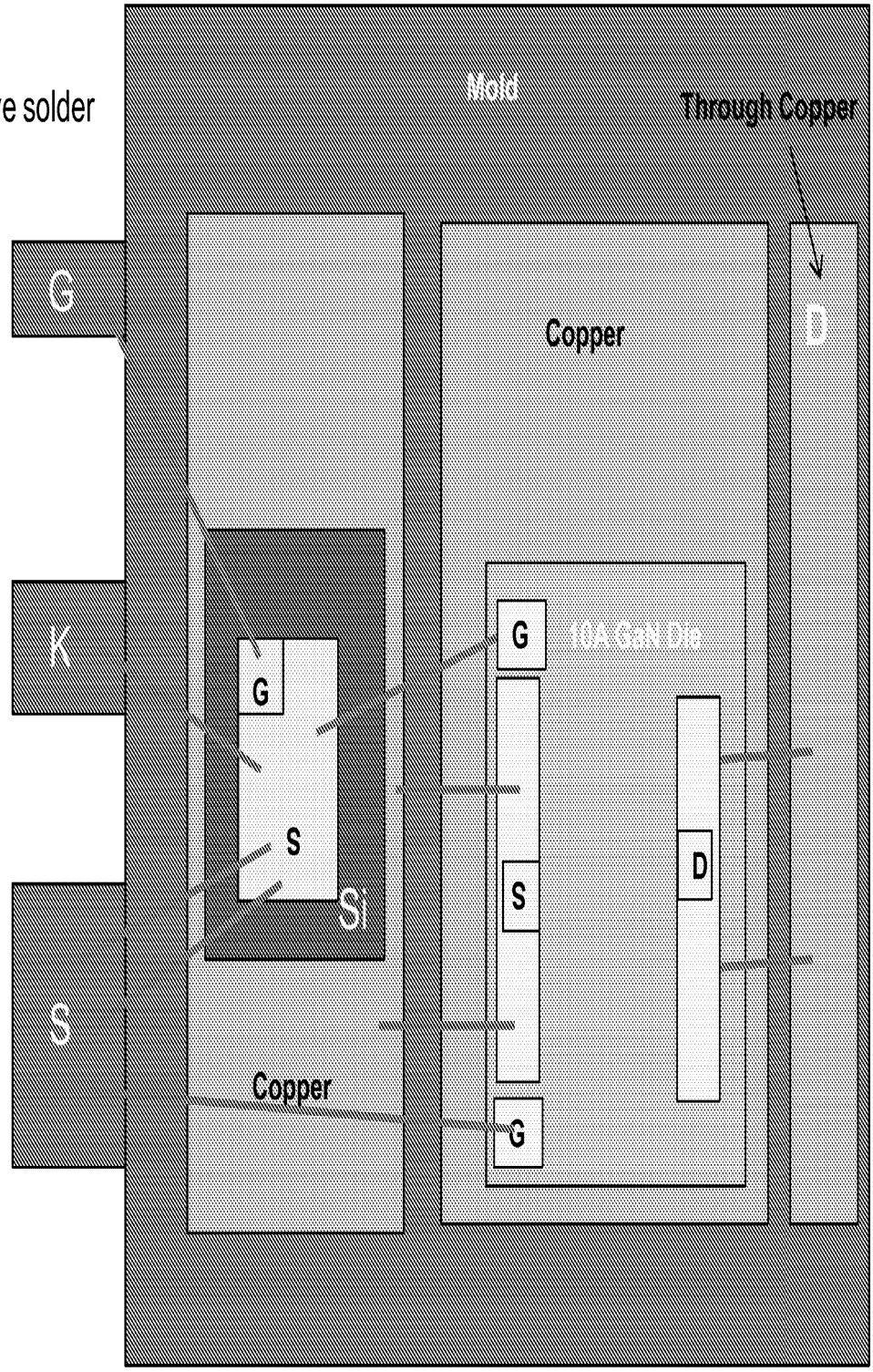
Effective heat dissipation with Cu plates, bond over active (BOA) designs, designed for cascode switch and discrete GaN devices, all the wire bonds along the power path can be replaced by clip bonds, and floating and grounding GaN substrate designs.

Die by Die Cascode/Diescrete GaN Switch: 8x8 PQFN Package: Wire Bonding w/o BOA

BOA is bond over active

GaN Cascode Switch (GaN substrate floating)

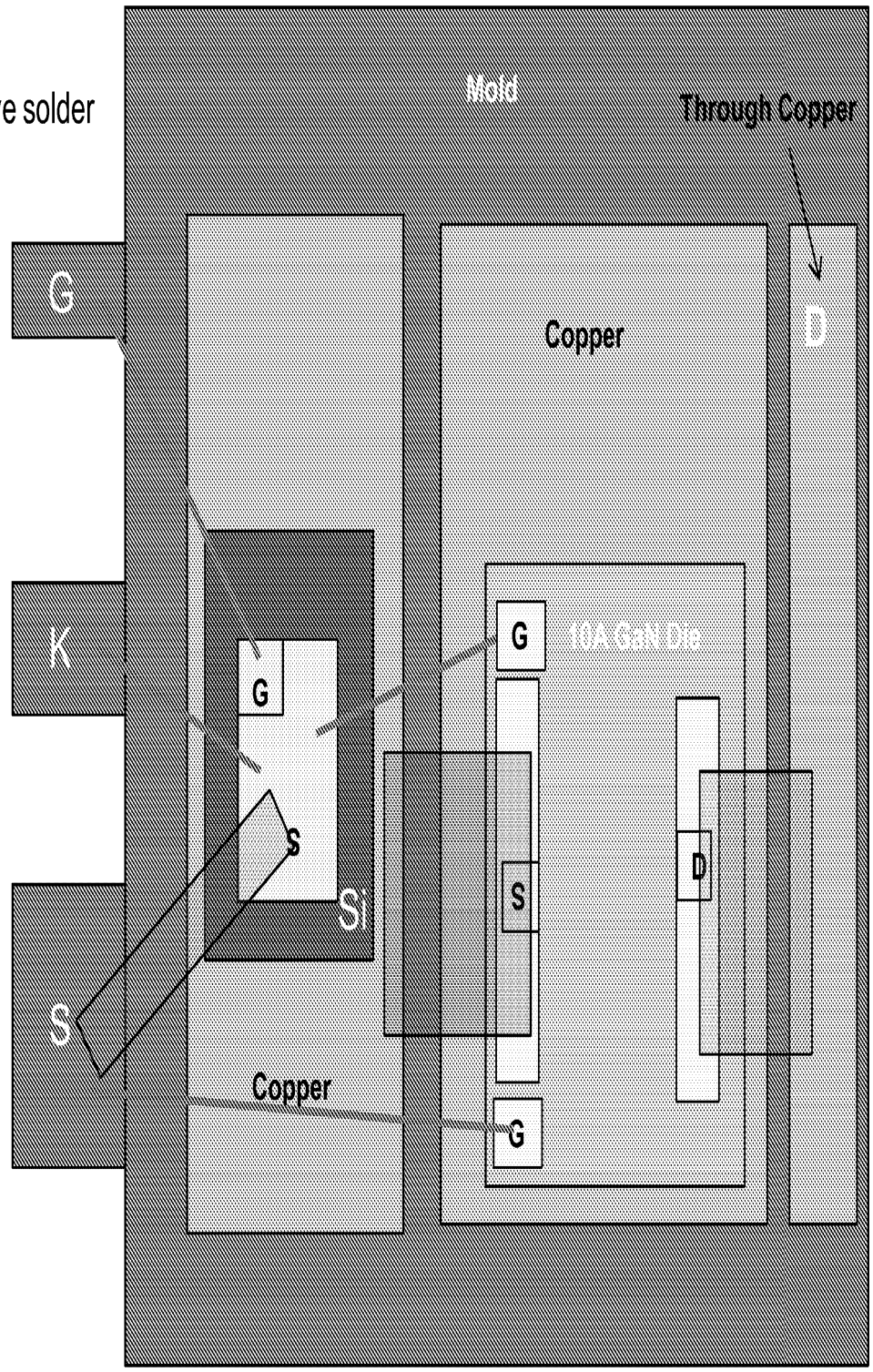
Si FET attach: conductive solder
GaN HEMT attach: non-conductive solder



GaN Cascode Switch (GaN substrate floating)

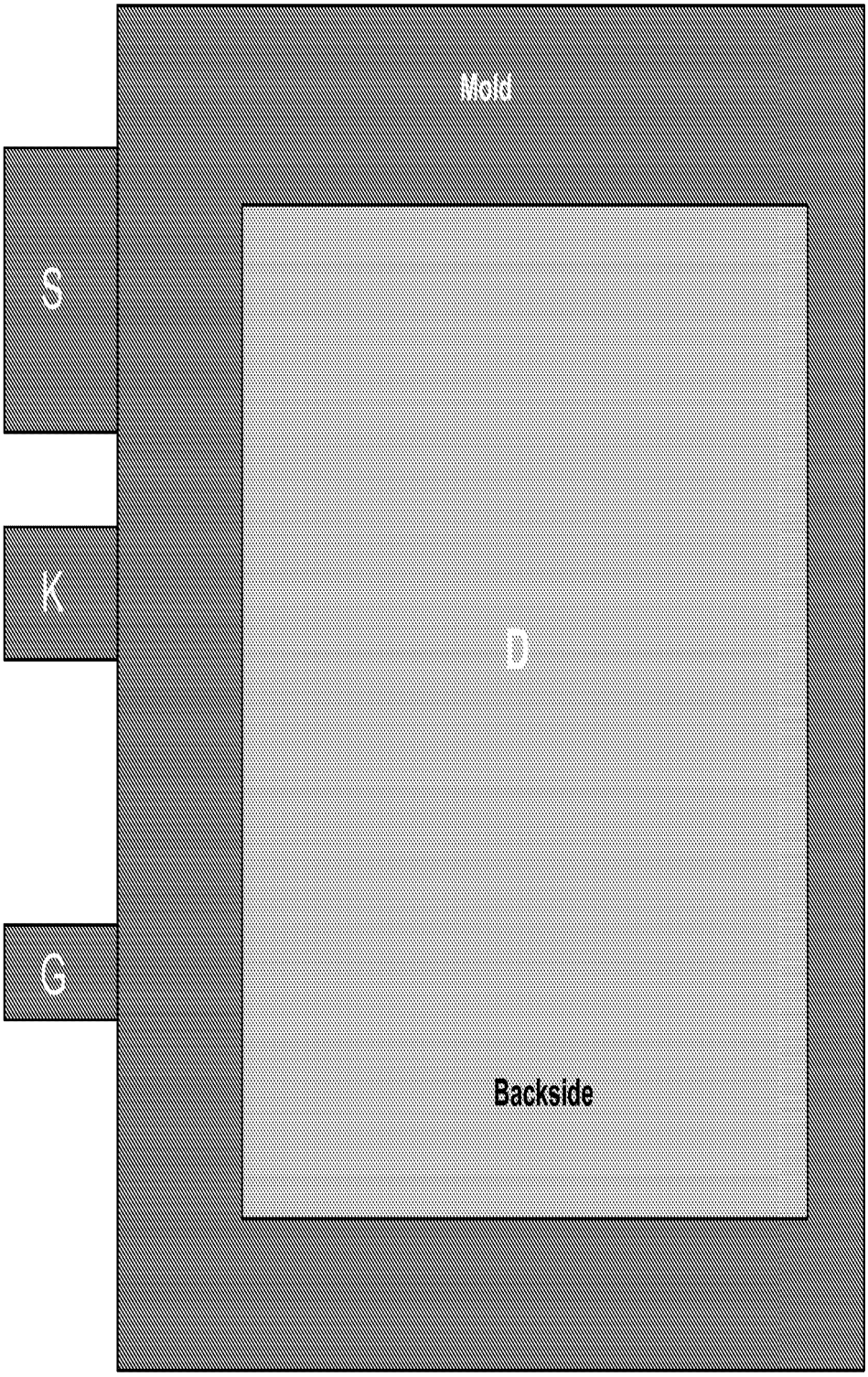
Si FET attach: conductive solder
GaN HEMT attach: non-conductive solder

Clip bonding



GaN Cascode Switch (GaN substrate floating)

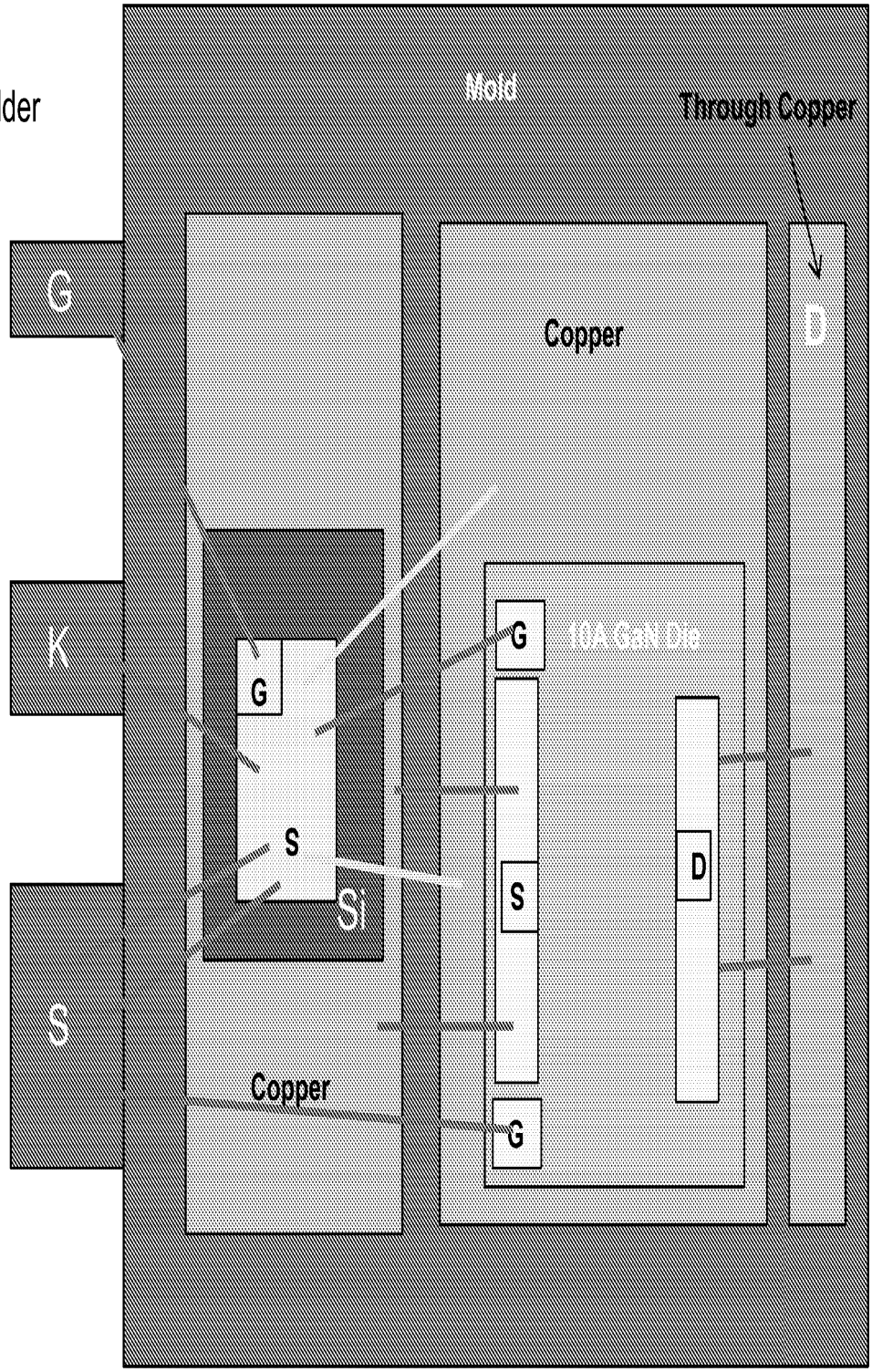
Backside View



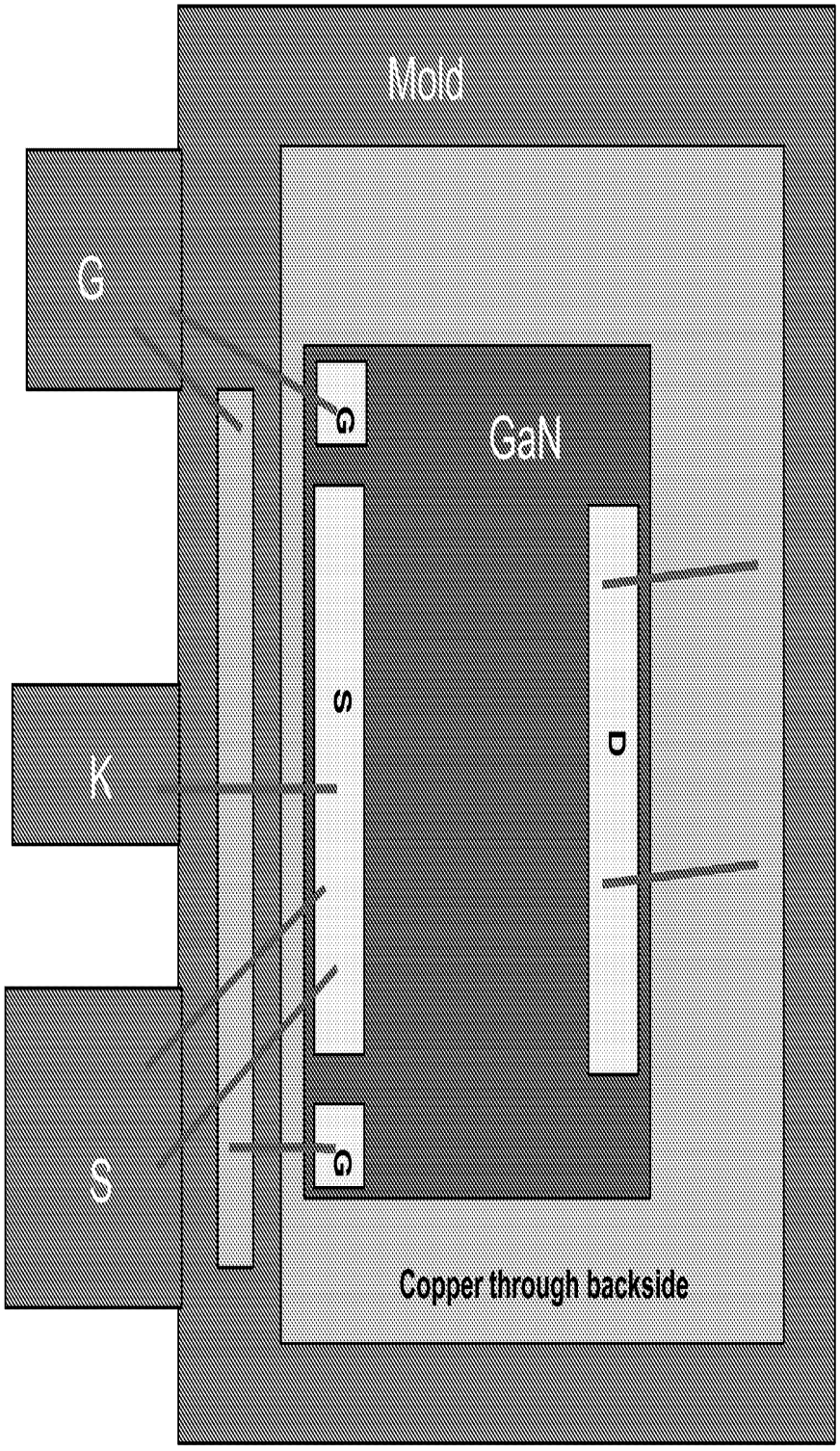
GaN Cascode Switch (GaN substrate grounded)

Si FET attach: conductive solder
GaN HEMT attach: conductive solder

GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source



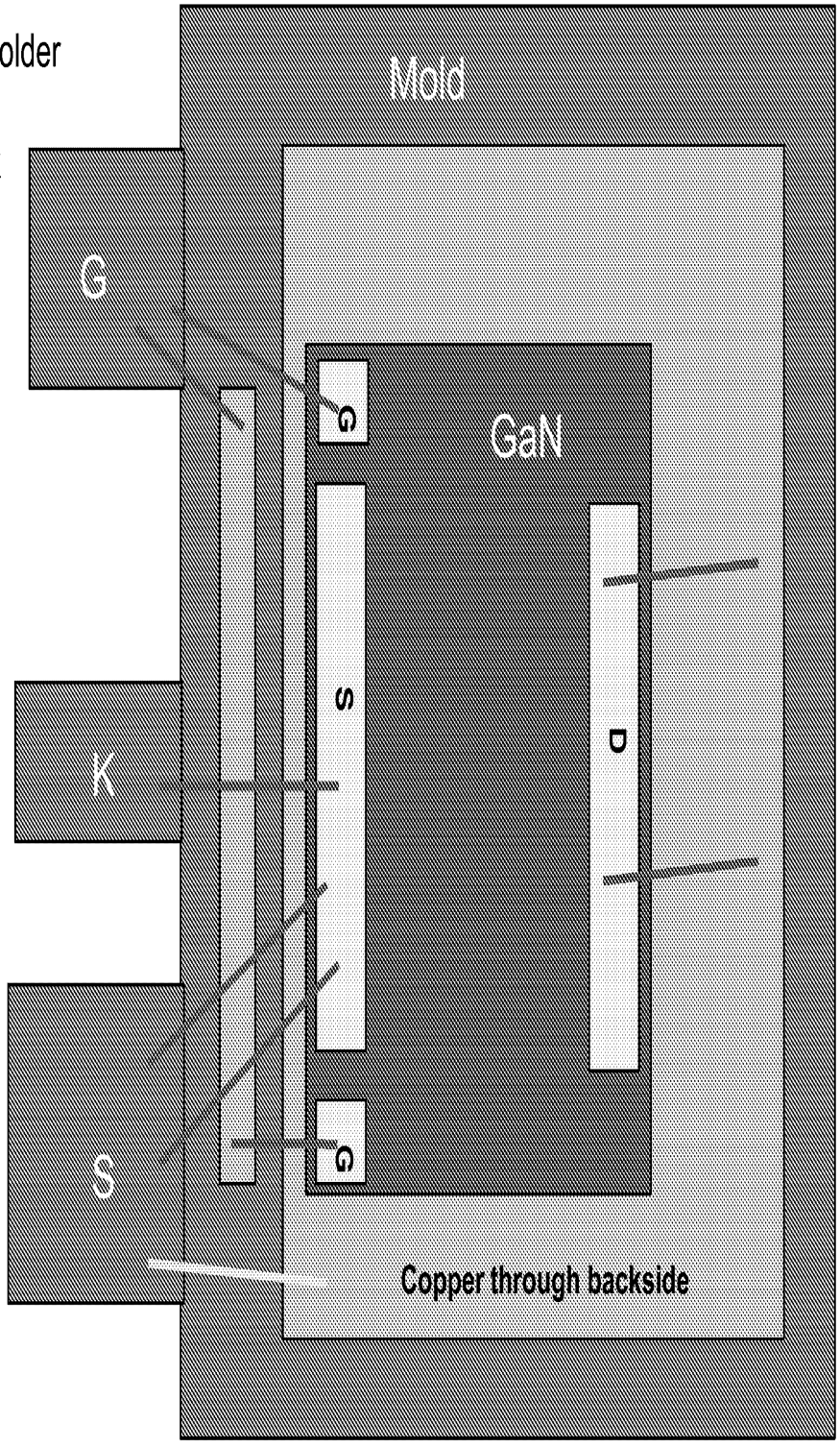
GaN Discrete PQFN (GaN substrate floating)



GaN Discrete PQFN (GaN substrate grounded)

GaN HEMT attach: conductive solder

GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source

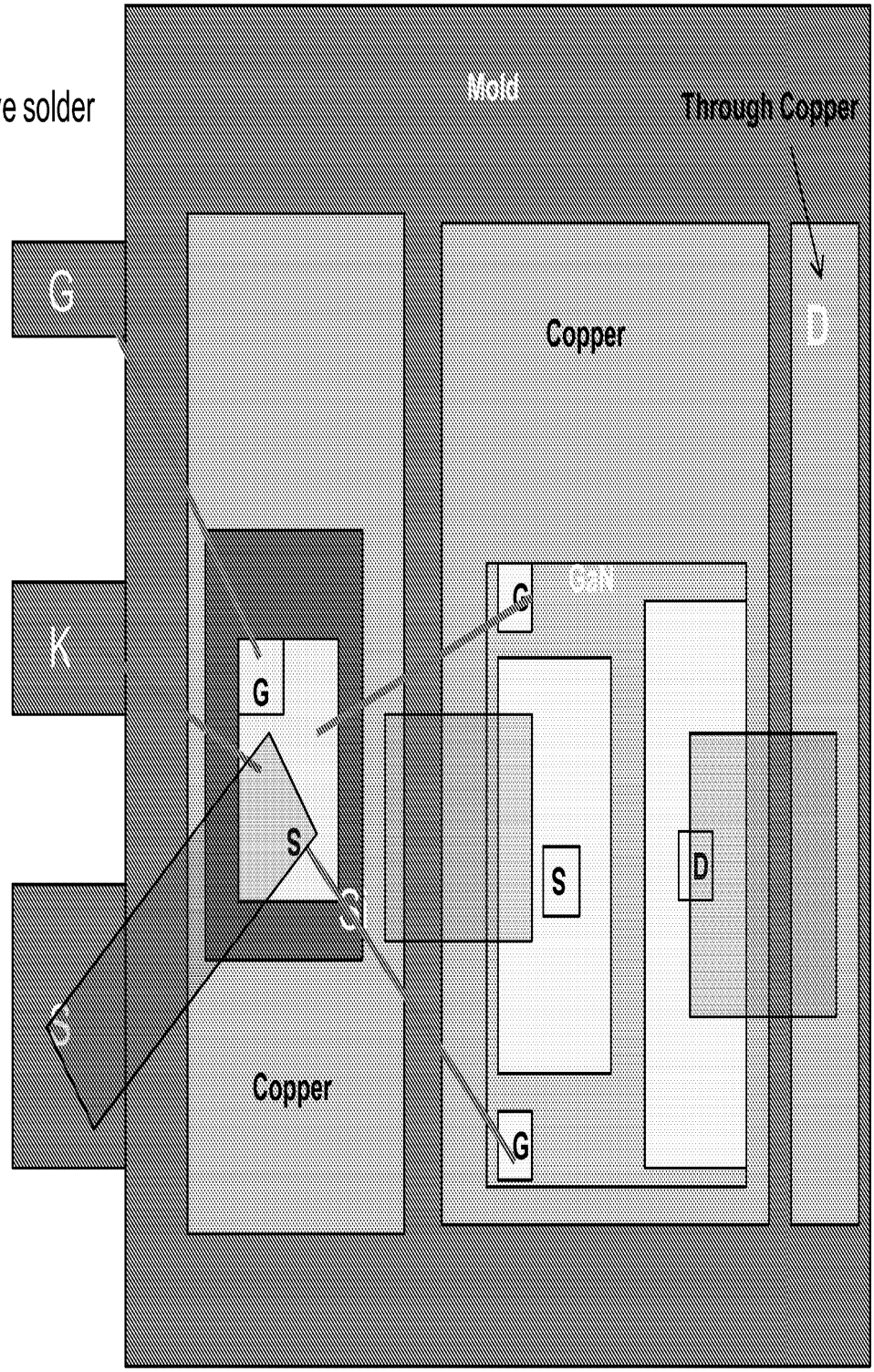


Die by Die Cascode/Diescrete GaN Switch: 8x8 PQFN Package: Wire Bonding w BOA

GaN Cascode Switch in 8x8 PQFN (GaN substrate floating)

Si FET attach: conductive solder
GaN HEMT attach: non-conductive solder

Clip bonding + BOA



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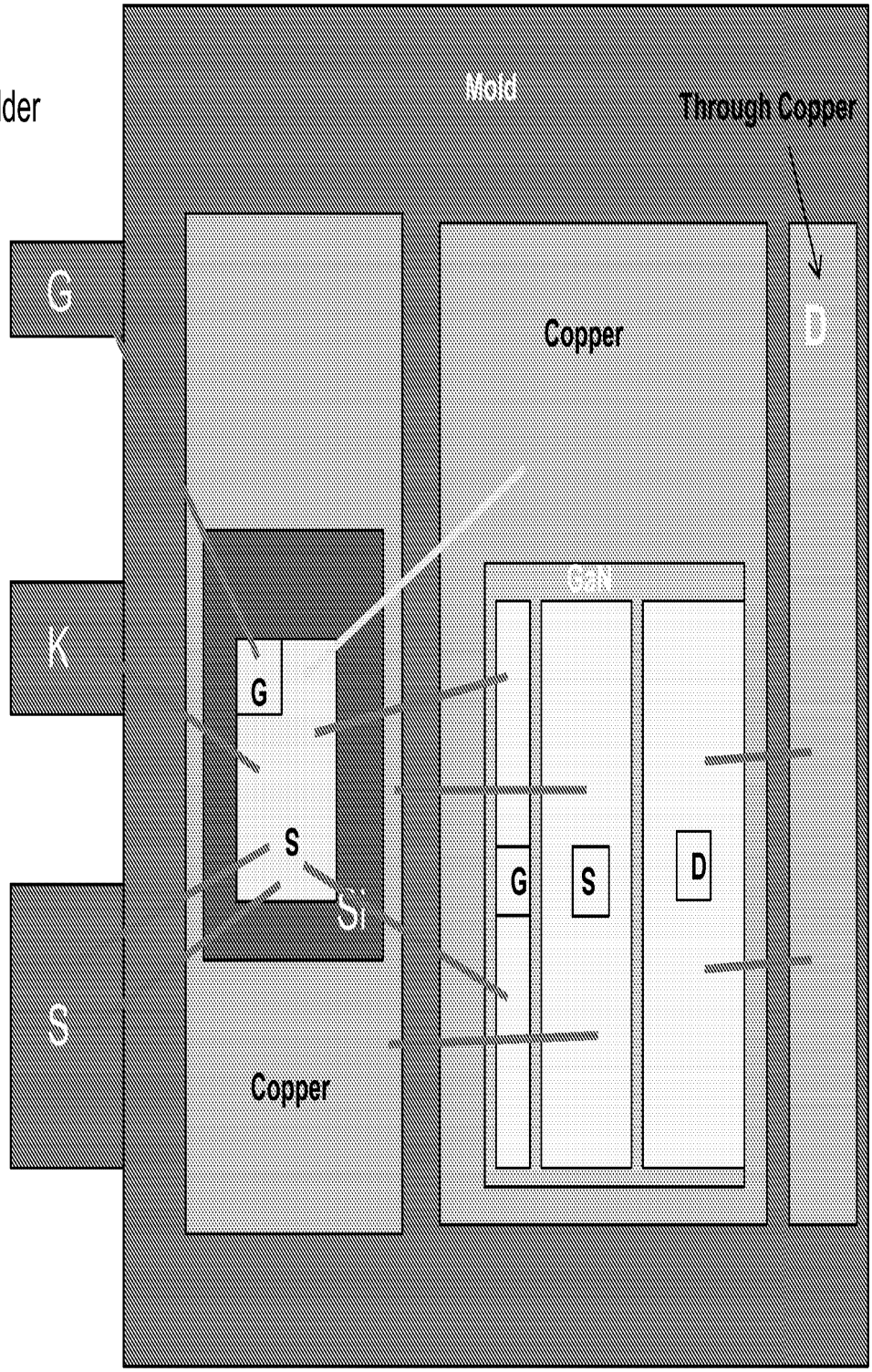
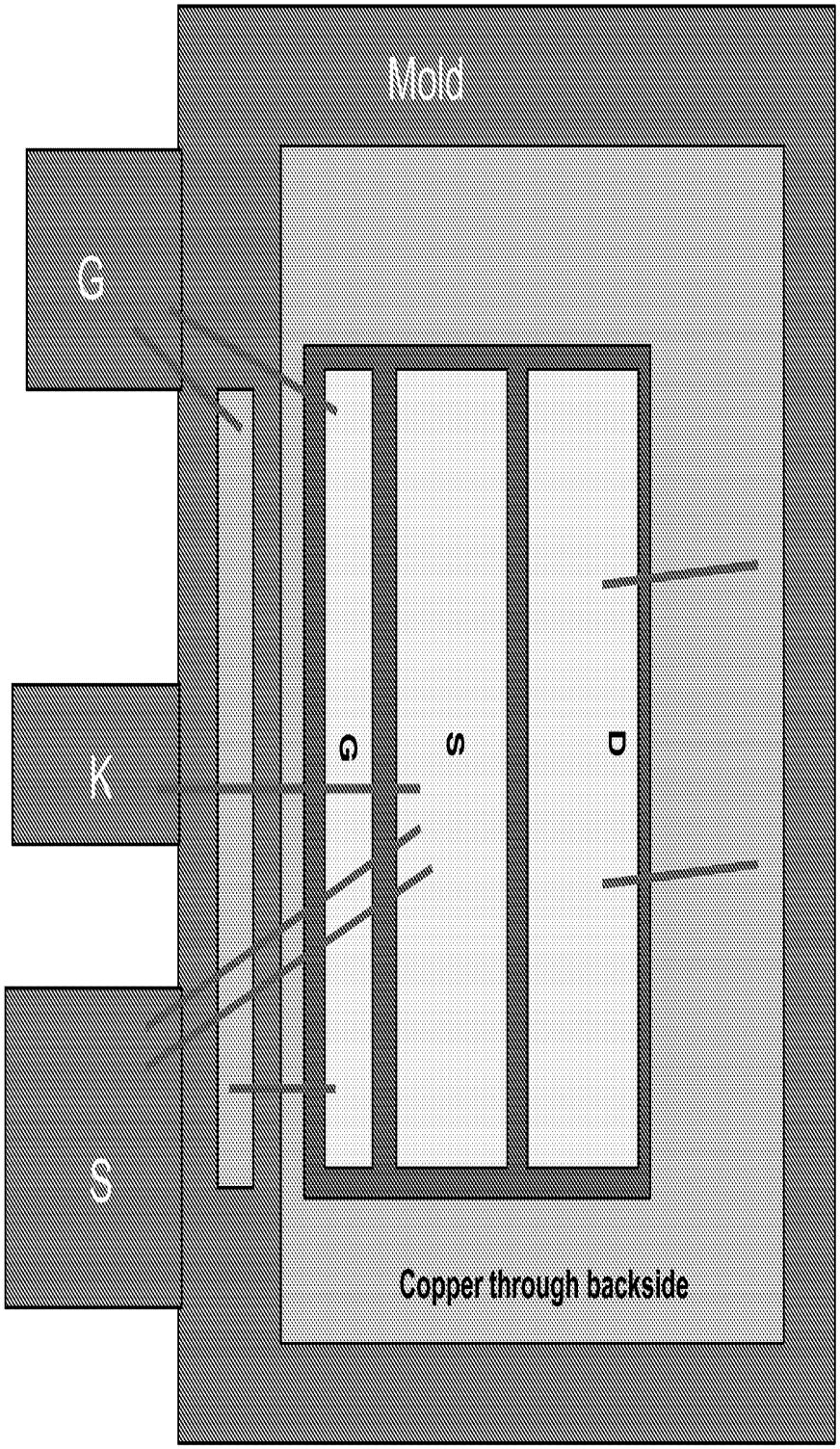


GaN Discrete (GaN substrate floating)



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Si FET attach: conductive solder
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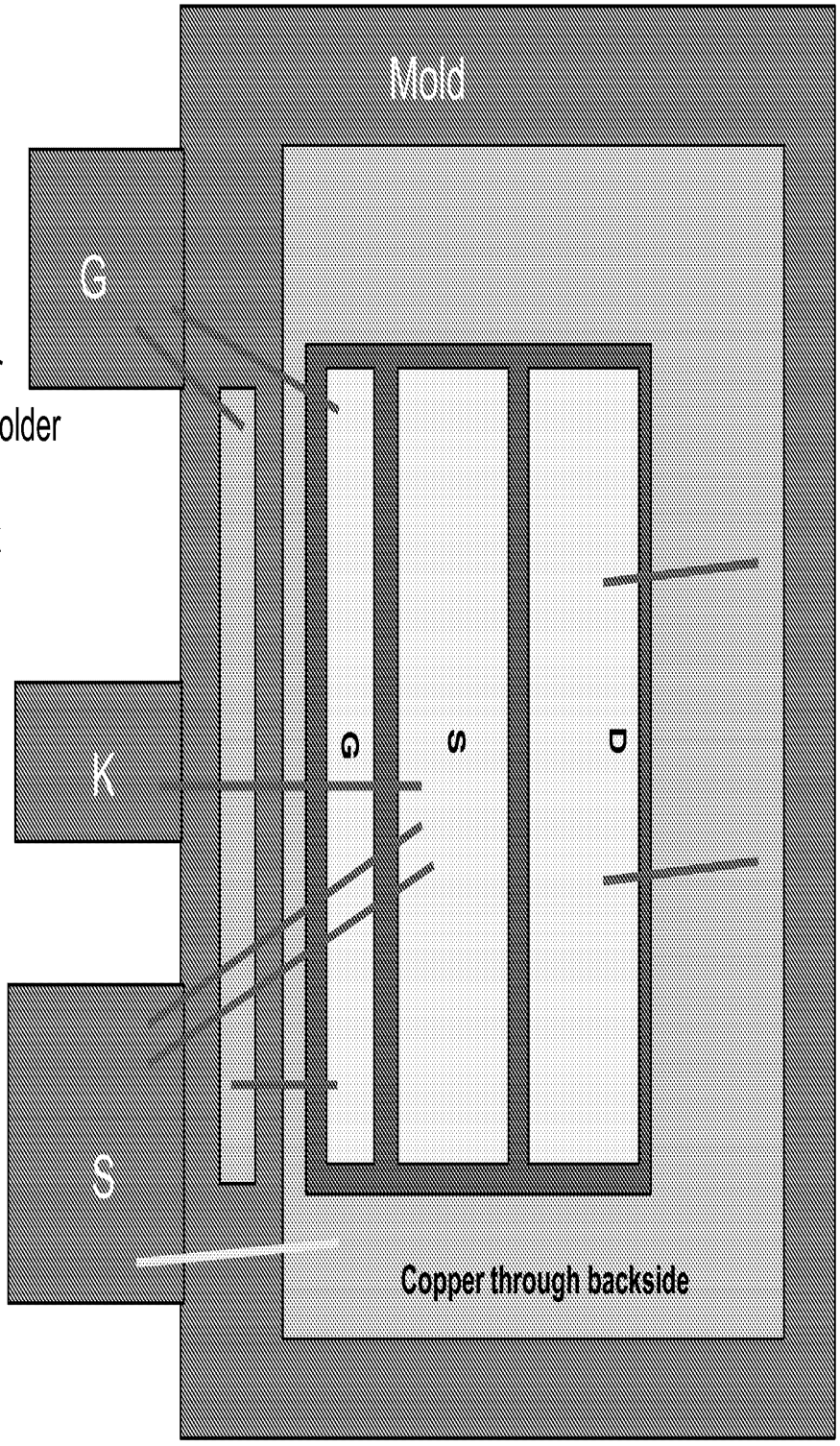
GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source



• For effective heat dissipation and electrical isolation, Cu plates hosting GaN and Si devices are placed and arranged in molding or ceramics onto nxm PQFN leadless package.
• A GaN device and a Si device are placed and arranged on top of the Cu plates where the source of GaN device is electrically connected to the drain of Si device by wire bonding, clip bonding, or other means to form a cascode configuration for switch and rectifier.
• GaN device may have a bond over active design to form a cascode configuration for switch and rectifier.
• The GaN device substrate can be electrically connected to the source pin of the cascode configuration for switch and rectifier, and thus grounding the GaN device substrate. Otherwise, the GaN substrate is floating.
• A single GaN device can be packaged into nxm PQFN with a Cu bar for connecting gate for high frequency performance.

Effective heat dissipation with Cu plates, bond over active (BOA) designs, designed for cascode switch and discrete GaN devices, all the wire bonds along the power path can be replaced by clip bonds, and floating and grounding GaN substrate designs.

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BOA is bond over active

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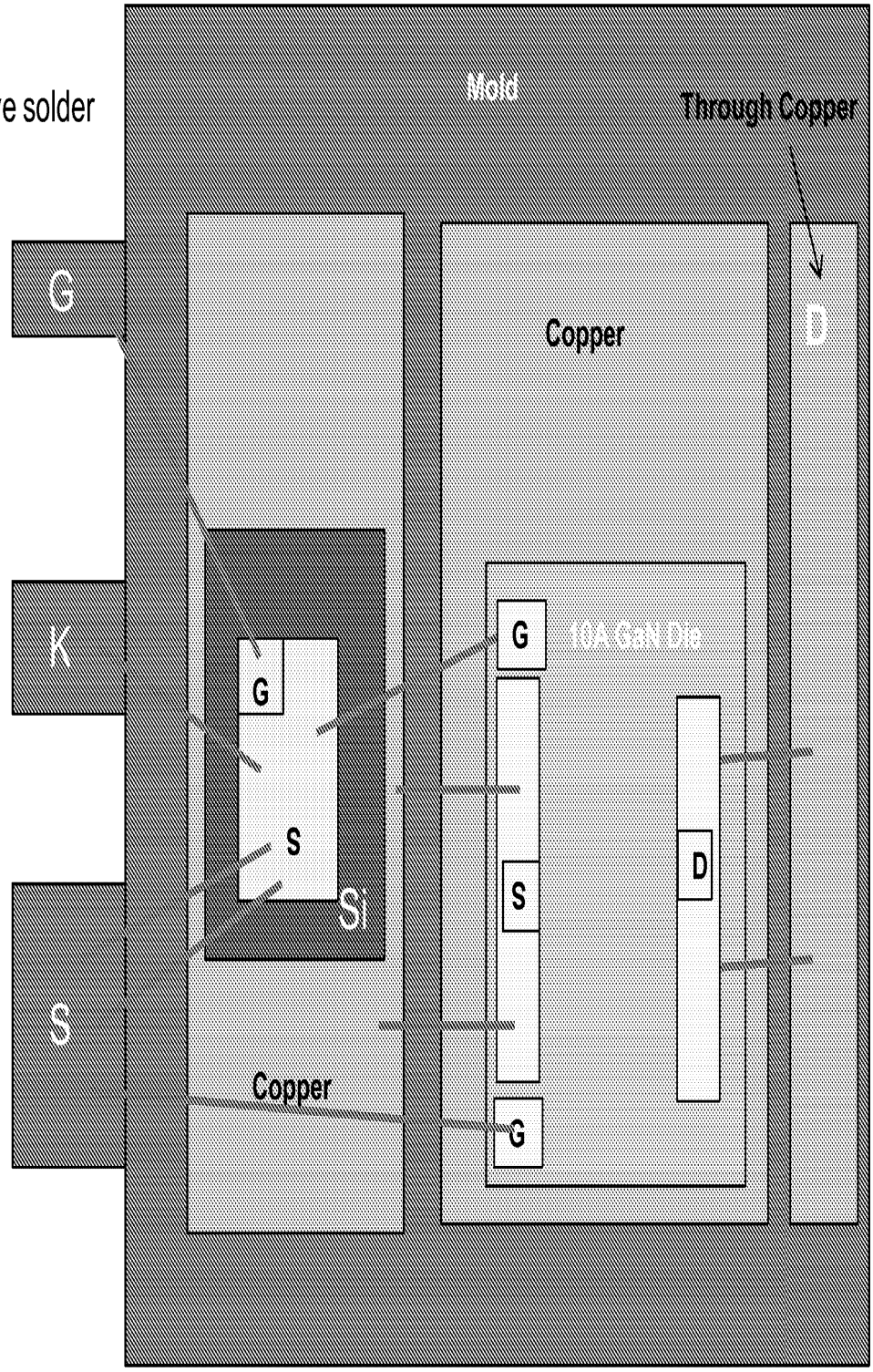

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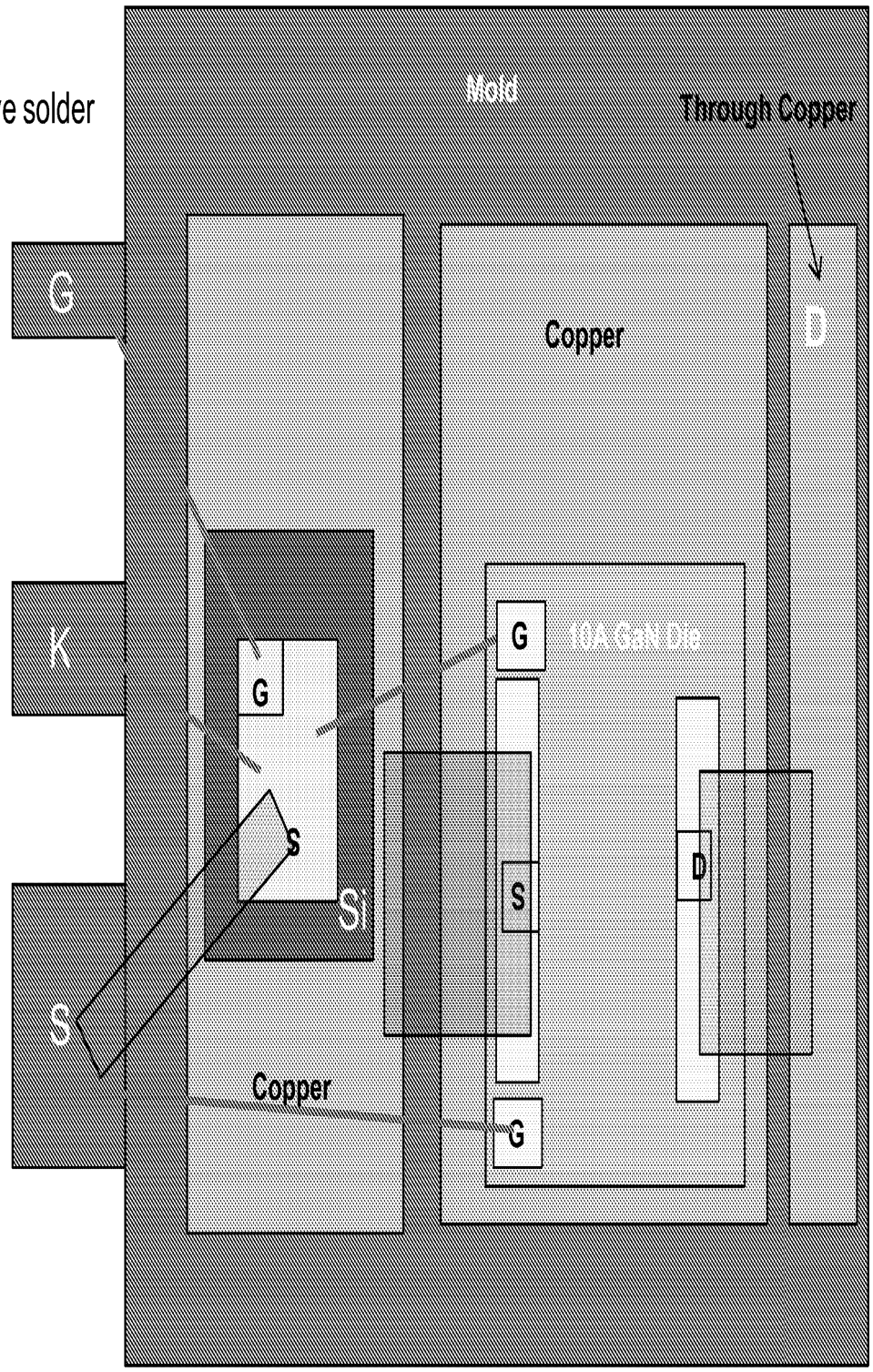
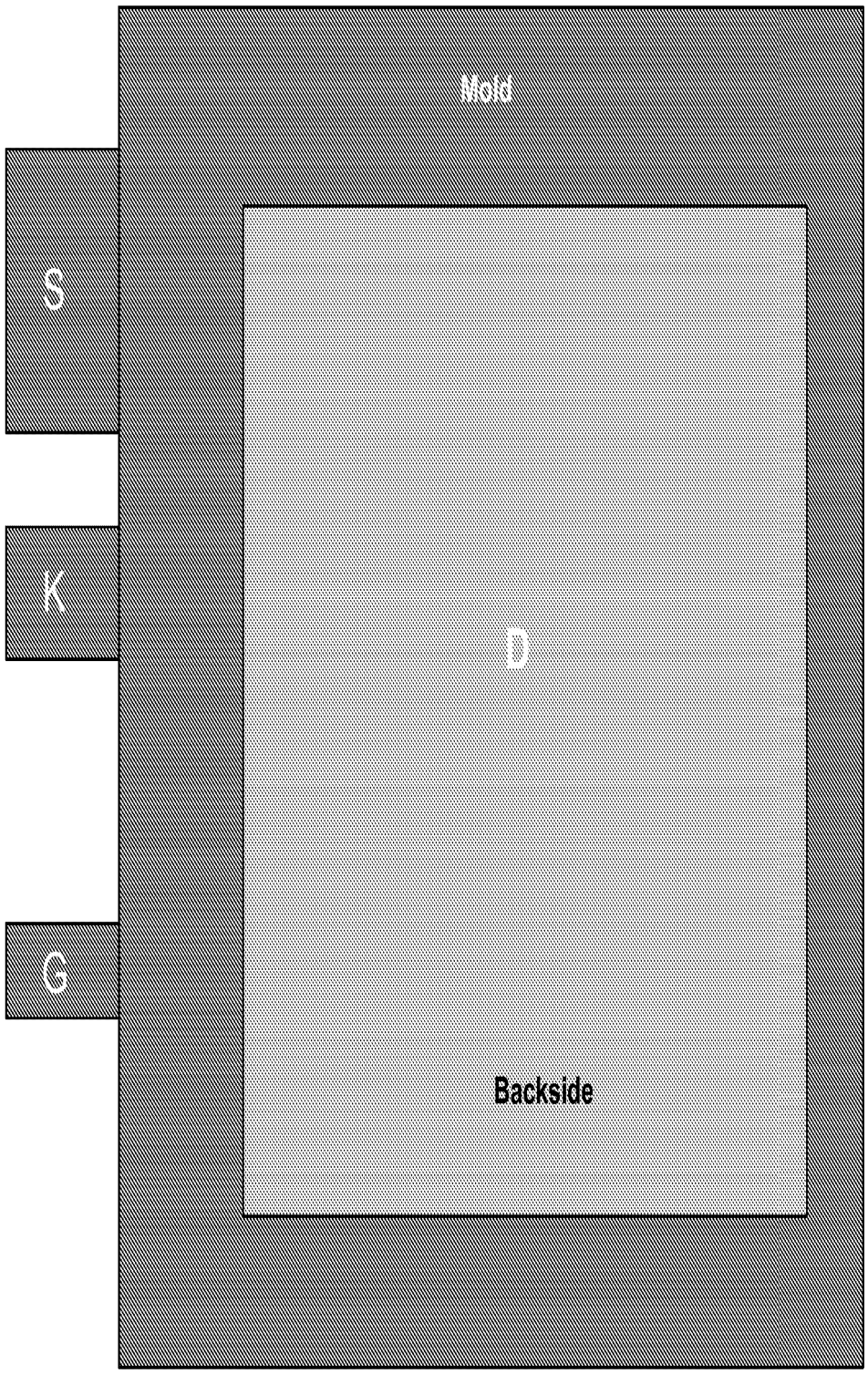
Clip bonding



GaN Cascode Switch (GaN substrate floating)

Backside View



GaN Cascode Switch (GaN substrate grounded)

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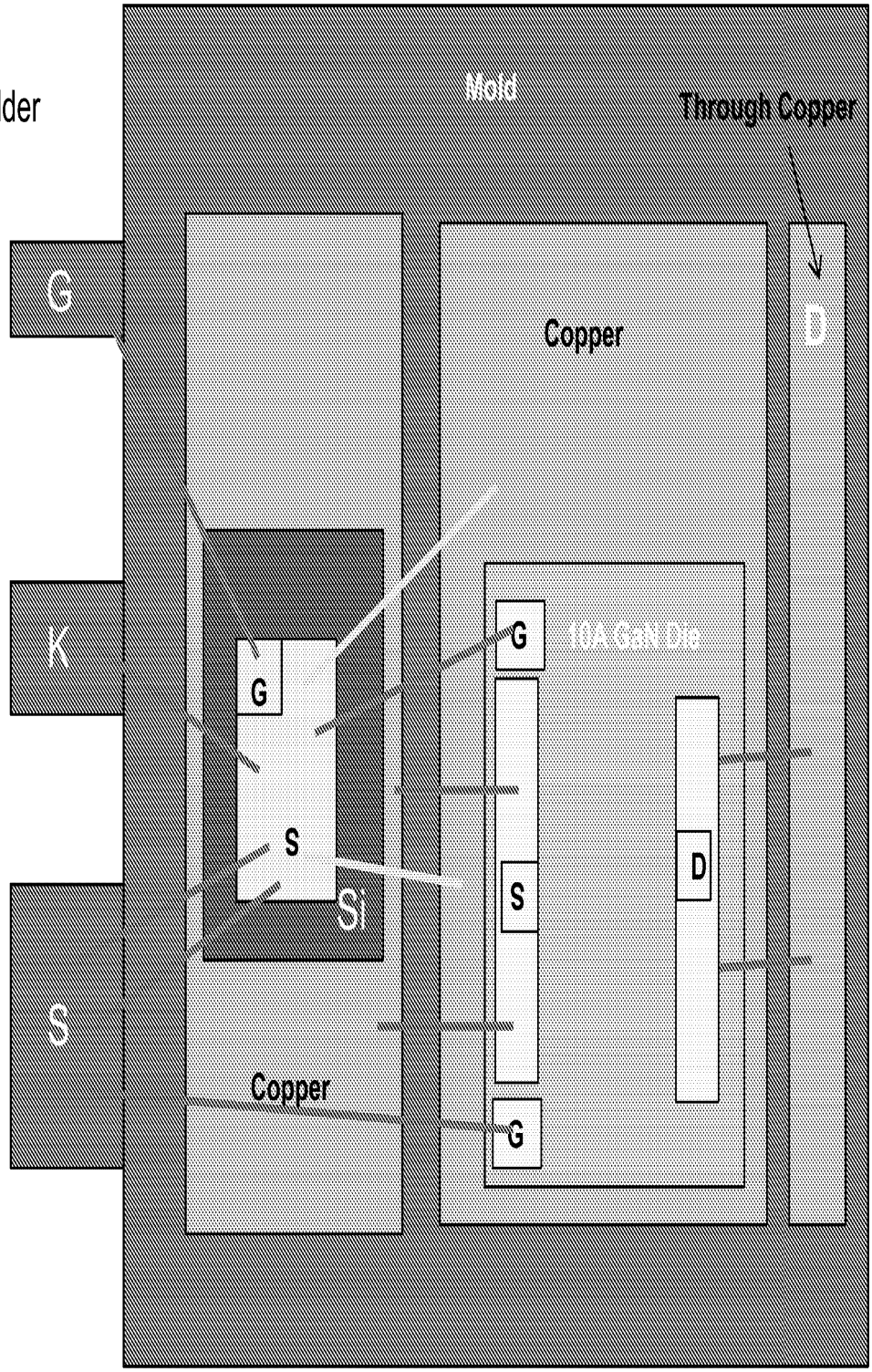
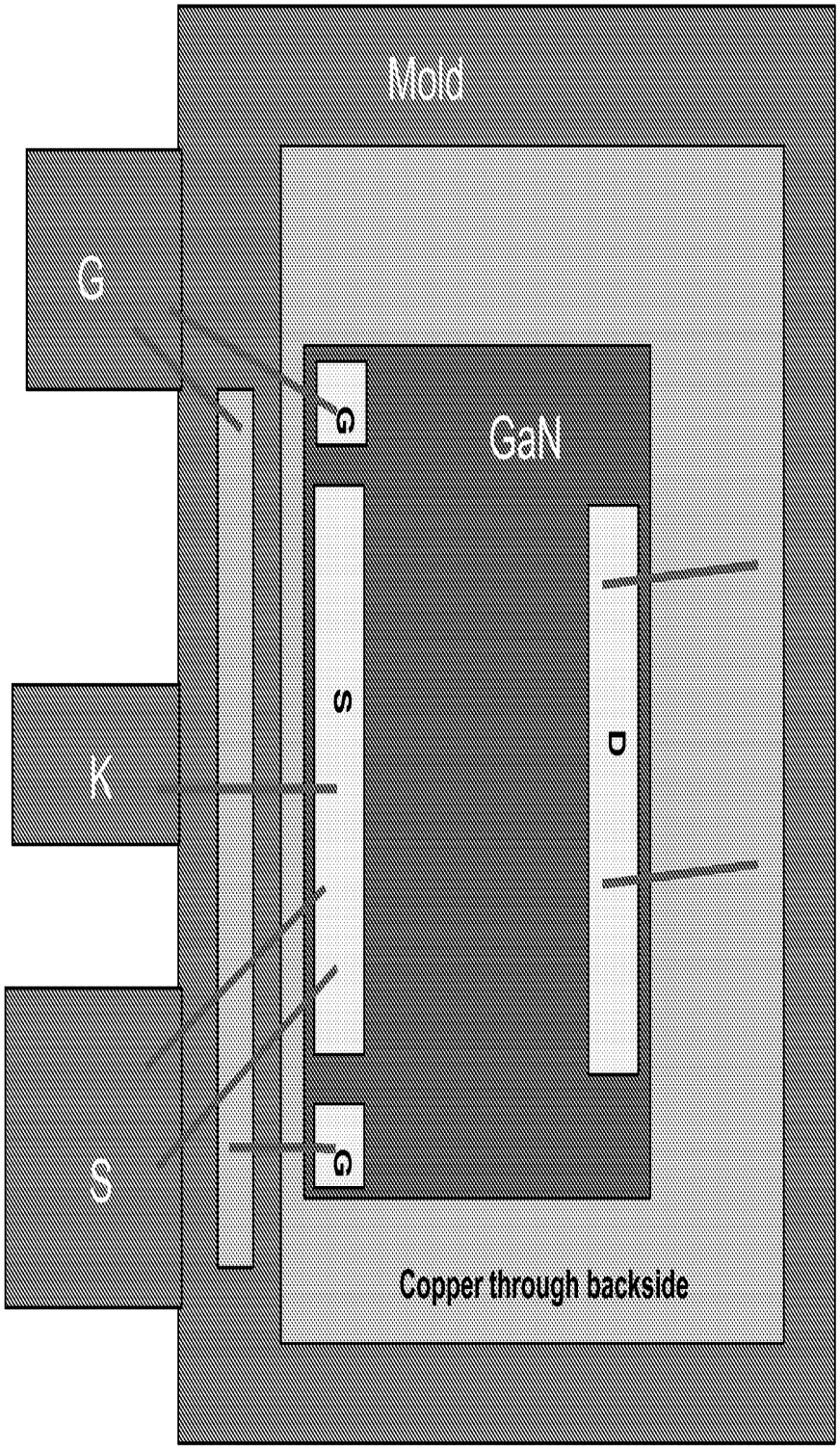
GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source



GaN Discrete PQFN (GaN substrate floating)



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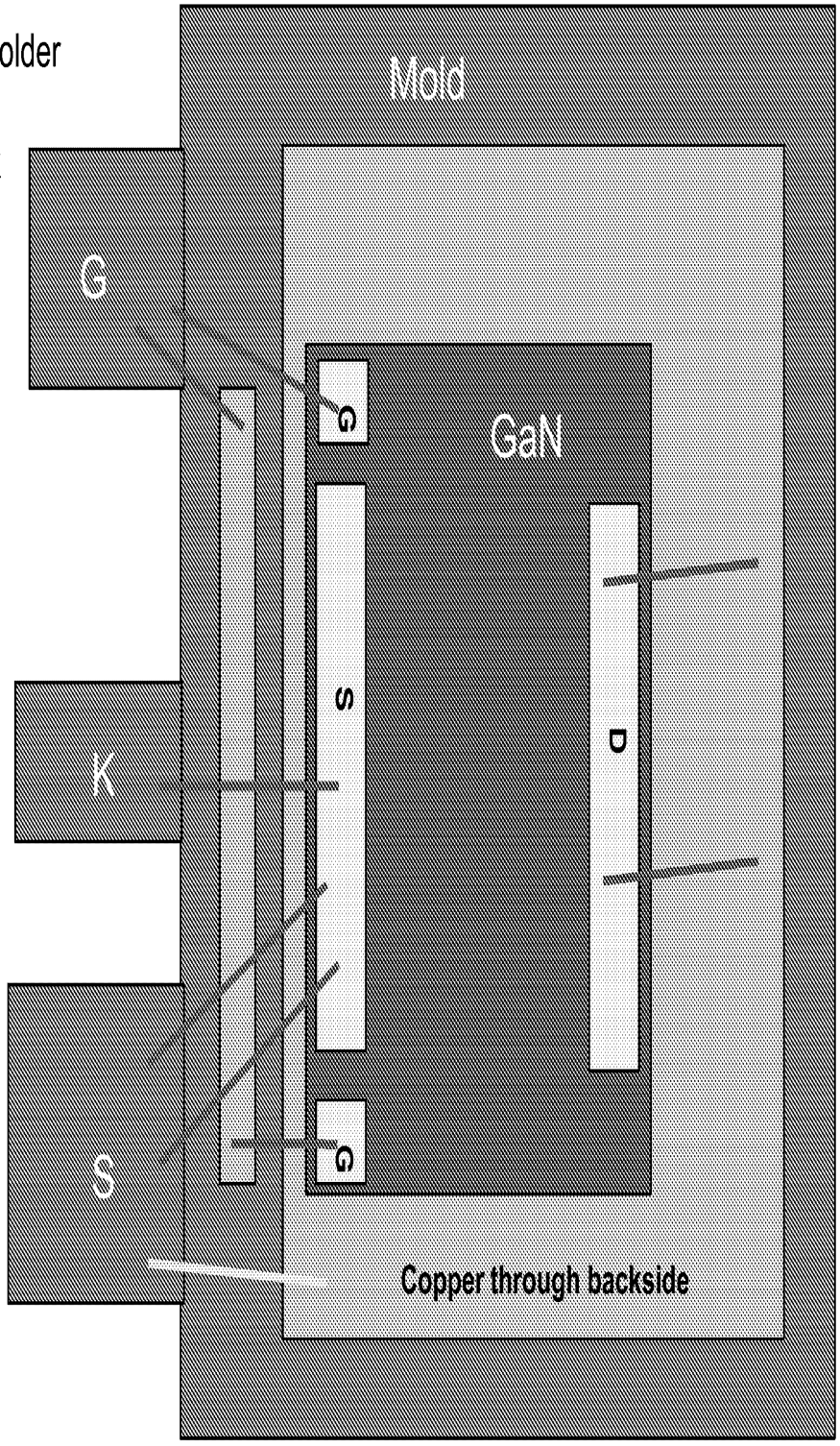
GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source



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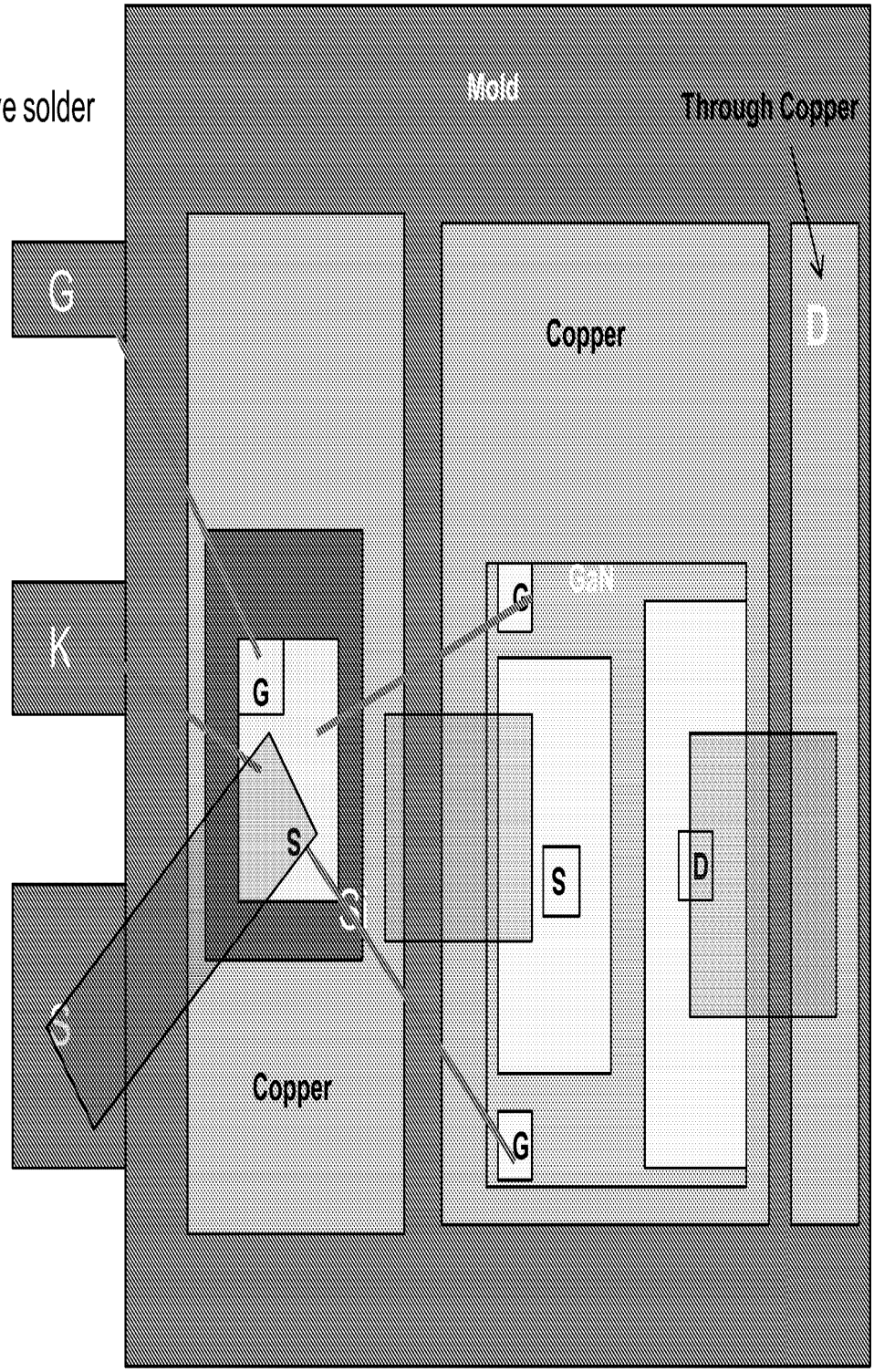
Clip bonding + BOA



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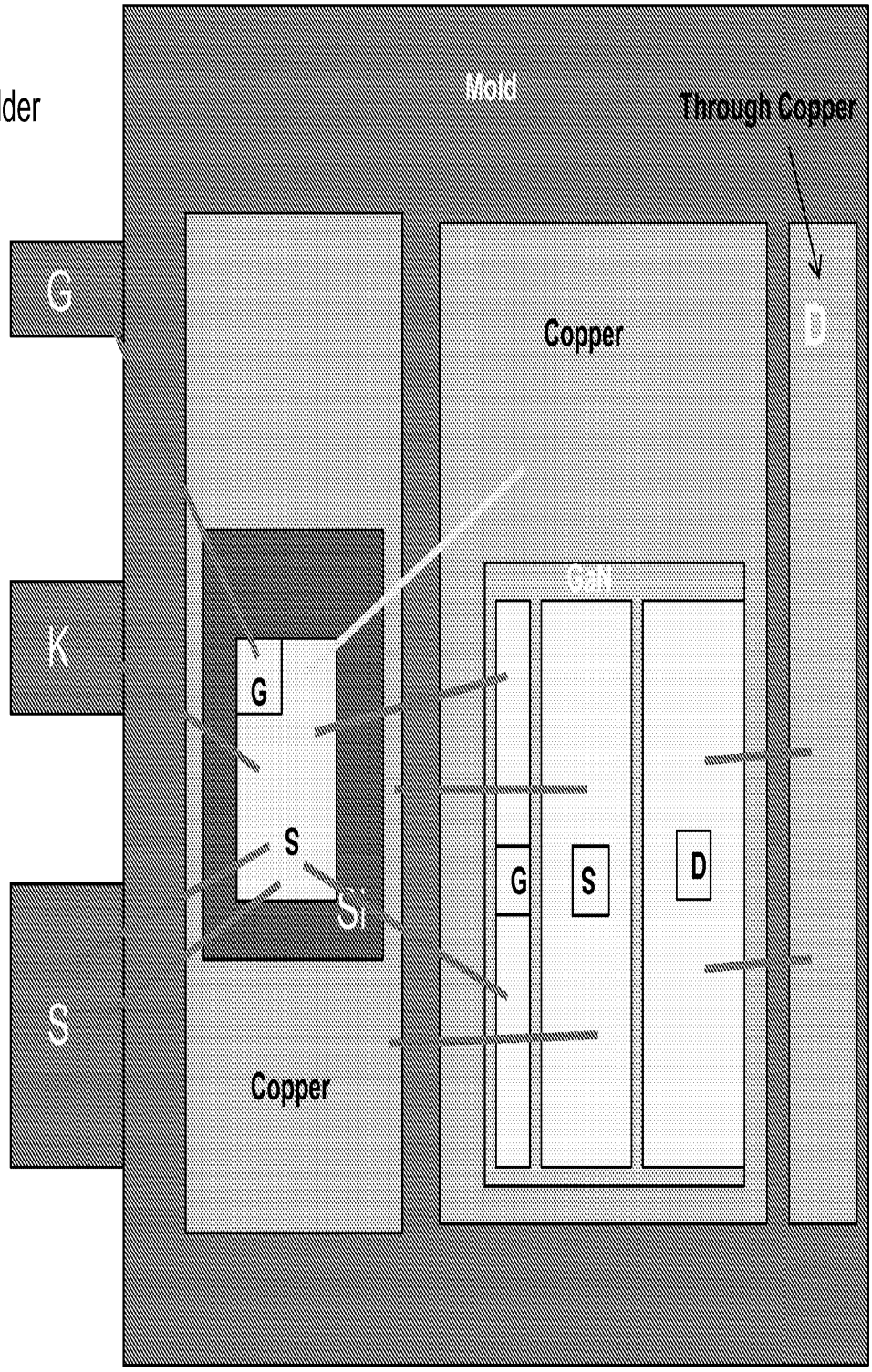

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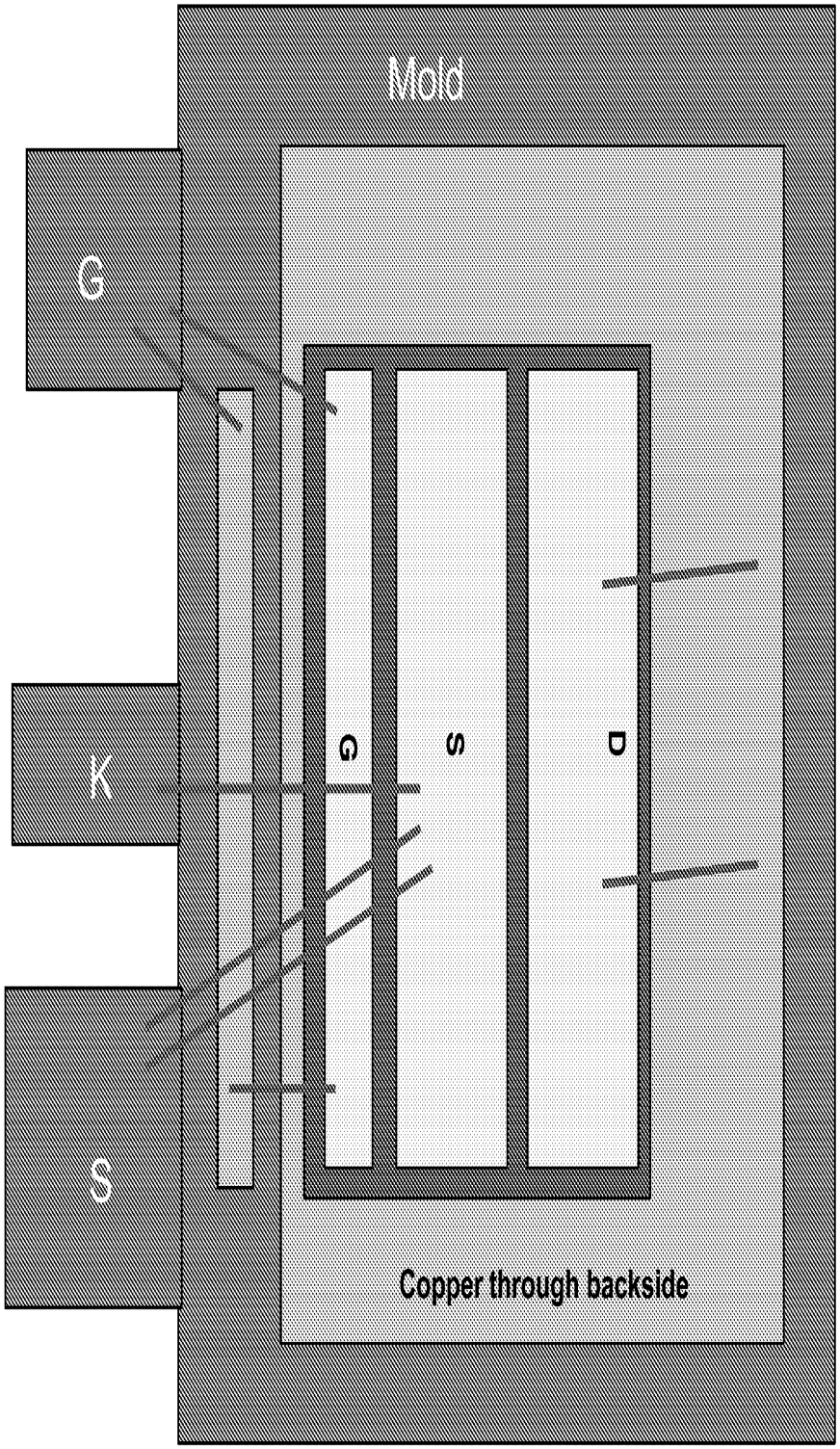

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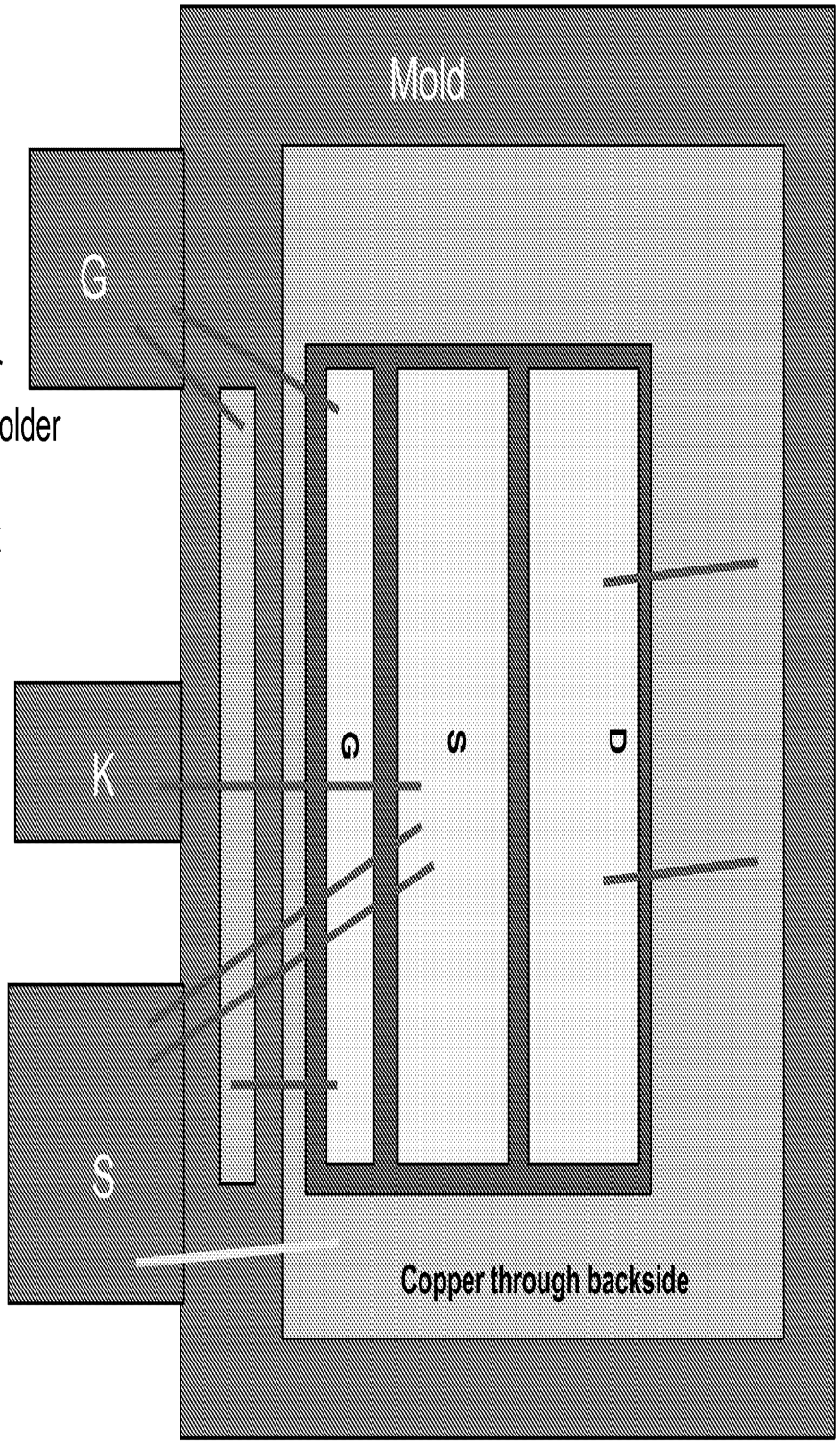
GaN HEMT: back-grinded, back solderable metal, connect GaN substrate to the source



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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE
First Named Inventor/Applicant Name:	Chun-Li Liu
Filer:	Daniel Joseph Anderson/Kelly Nelson
Attorney Docket Number:	ONS01639

Filed as Large Entity

Filing Fees for Provisional

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional Application Filing	1005	1	260	260
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**260**

Electronic Acknowledgement Receipt	
EFS ID:	23015568
Application Number:	62196629
International Application Number:	
Confirmation Number:	5988
Title of Invention:	SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE
First Named Inventor/Applicant Name:	Chun-Li Liu
Customer Number:	132192
Filer:	Daniel Joseph Anderson
Filer Authorized By:	
Attorney Docket Number:	ONS01639
Receipt Date:	24-JUL-2015
Filing Date:	
Time Stamp:	15:55:34
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$260
RAM confirmation Number	2434
Deposit Account	501086
Authorized User	KELLY, NELSON
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ONS01639_Application_Prov.pdf	88583 0ed4f5cf8b30faa7c69de9144cb4ba8f637a10fa	yes	18
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	12	
	Claims		13	17	
	Abstract		18	18	
Warnings:					
Information:					
2	Application Data Sheet	ONS01639_ADS.pdf	1505347 a08e488e6e3ad7c960c118828458bca023de2d93	no	7
Warnings:					
Information:					
3	Drawings-only black and white line drawings	ONS01639_Drawings_prov.pdf	426468 c084d6b108a45a230a083e4a27a670cd48e0c372	no	7
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4	Appendix to the Specification	ONS01639_Appendix_Prov.pdf	166102 5cf1cf83d17d7d337ae2e002c7fb0987209da5df	no	14
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5	Drawings-other than black and white line drawings	ONS01639_Appendix2_Prov.pdf	152818 373e5613d03b680ca097230a57ca5a7c0e6f918e	no	14
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6	Fee Worksheet (SB06)	fee-info.pdf	29735 f2194100b5692887ffca4668a15d4fff3b001b26	no	2

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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