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B. Murari
F. Bertotti
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(Eds.)

Smart Power ICs



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Contributions by

Andreini A., Borghi M. R., Botti E., Cognetti C., Contiero C.
Diazzì C., Fichtner W., Galbiati P., Gariboldi R., Kobayashi E.
Lonzi L., Maggioni M., Morelli M., Mukherjee S., Piccoli M.
Poletto V., Pedrazzini G., Rossi D., Speroni F., Stefani F., Storti S.
Sugawara Y., Tihanyi J.

With 480 Figures



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Editors:

Dr. Bruno Murari
SGS-Thomson Microelectronics
Via Tolomeo, 1
20010 Cornaredo (MI)
Italy

Dr. Franco Bertotti
SGS-Thomson Microelectronics
Via Tolomeo, 1
20010 Cornaredo (MI)
Italy

Dr.-Ing. Giovanni A. Vignola
Via Don Luigi Sturzo, 15
20093 Cologno Monzese (MI)
Italy

Series Editor:

Dr. Kiyoo Itoh
Hitachi Ltd., Central Research Laboratory
1-280 Higashi-Koigakubo
Kokubunji-shi
Tokyo 185-8601
Japan

Professor Takayasu Sakurai
Center for Collaborative Research
University of Tokyo
7-22-1 Roppongi, Minato-ku,
Tokyo 106-8558
Japan

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BCD Technology for Smart Power ICs

A. Andreini · C. Contiero · P. Galbiati

1.1

Introduction

The name BCD has been created in the mid-eighties to classify that family of mixed processes that allow to integrate into a single chip Bipolar, CMOS and DMOS transistors, forming a new power IC class called SMART POWER ICs [1–7].

Up till the mid-eighties Power ICs were realised using pure bipolar technologies previously developed together with their main application field, the audio amplifier market segment.

For the analog function required in these applications, the bipolar transistors were the best choice due to their amplification and matching properties.

The other major application field was the motor control one where the needed logic functions were implemented by bipolar I^2L structures.

With the growing requests of logic functions the bipolar I^2L approach resulted limited due to their design complexity, their high power consumption and their limited shrinkability with the lithography.

As these limits were not present in the CMOS components, at least at low frequency operation, to increase the smartness in the Power ICs it appeared evident that the only way was to make available CMOS in the place of I^2L .

During the Bipolar IC evolution the power that had to be supplied to the load increased, too. This increase reached the limit fixed by the allowed power dissipation and by the admitted consumptions.

The DMOS power transistor permitted to overcome all these limitations because it has no driving DC current requirement and it efficiently works in fast switching conditions.

The previous topics have been realized with the idea to merge the discrete DMOS technology, rising in the first eighties, with the junction-isolation bipolar technology used for many years to construct Power Integrated Circuits.

The realisation of this idea led to the birth of the Multipower-BCD [8].

1.2

Smart Power Technology Classification

Several different technological approaches to smart power have been explored, but all such technologies share the same basic concept of merging different

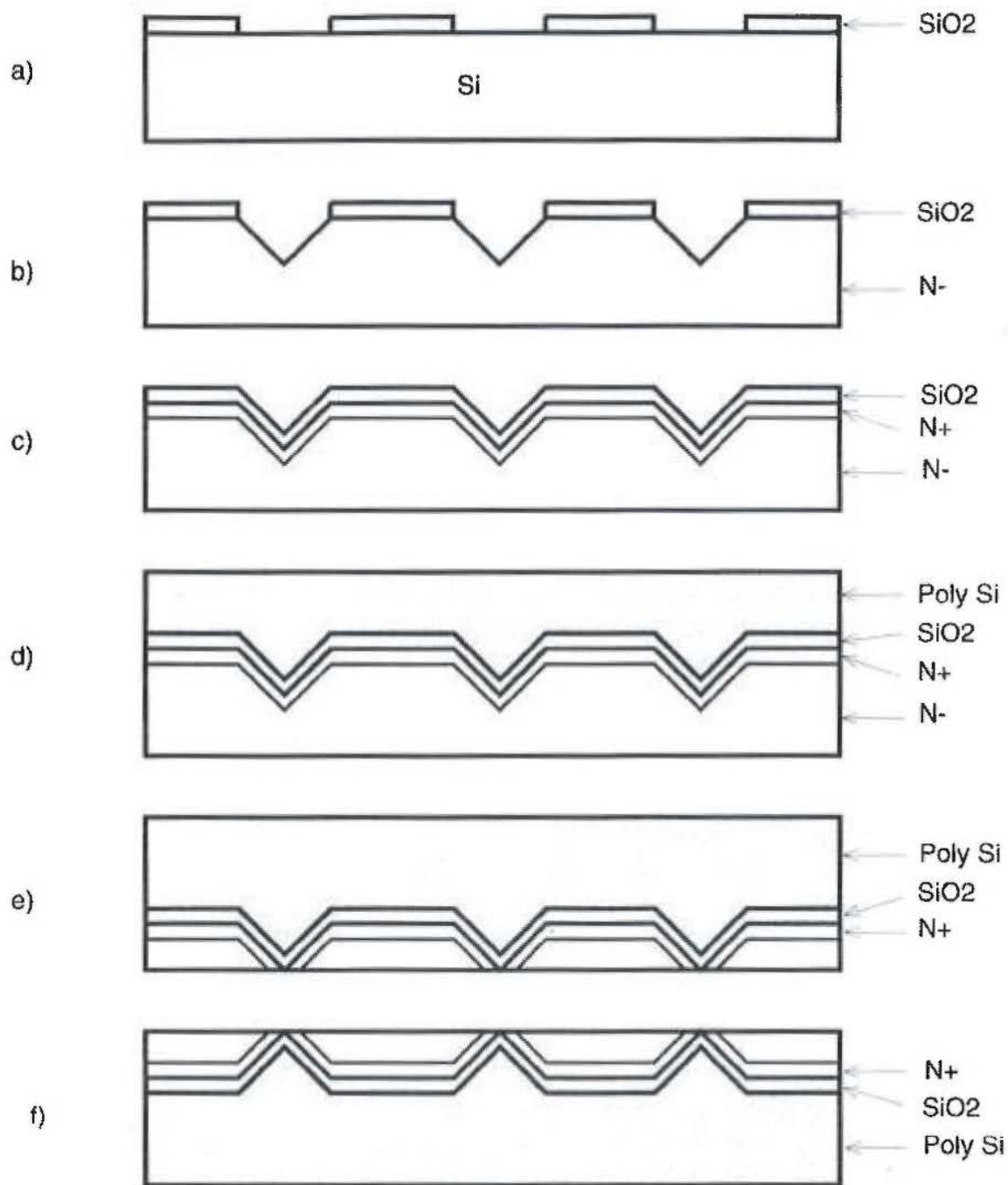


Fig. 1.1 Conventional Dielectric Isolation manufacturing process

structures into the same chip, taking advantage of the similarities in processing techniques.

Smart power technologies share many characteristics and may be conveniently classified according to the isolation technique (dielectric, self or junction isolation), by the power device structure (DMOS, bipolar, IGBT or SCR) and by the position of the drain/collector contact (on the surface or the back of the die).

1.2.1

Isolation Techniques

Dielectric Isolation (DI)

Dielectric isolation allows the realisation of silicon islands completely surrounded by oxide with advantages such as the low parasitic capacitance of components to substrate, the absence of leakage current and a reduction in the size of high voltage components. However, this method requires a more complex and costly manufacturing process (Fig. 1.1).

Moreover, since oxide is a poor conductor of heat it limits the integration of power devices.

Alongside the conventional construction methods developed more than 25 years ago [9], new techniques are being studied, such as Silicon Direct Bonding [10], lateral epitaxial growth over oxide [11] with different recrystallization techniques, and SIMOX [12–13]. These new techniques, however, are still at an experimental stage and will still require a little time before they are established. In addition, with these techniques it is difficult to realise vertical structures, even though a few examples have been reported [14–15].

Today the most promising DI approach is based on the SOI (Silicon On Insulator) substrate obtained by the Silicon Direct Bonding technique with isolation plugs realised by trench etches (Fig. 1.2) [16].

Self-Isolation

Self-isolation is used when the integrated devices do not need to be completely isolated because some terminals are shared.

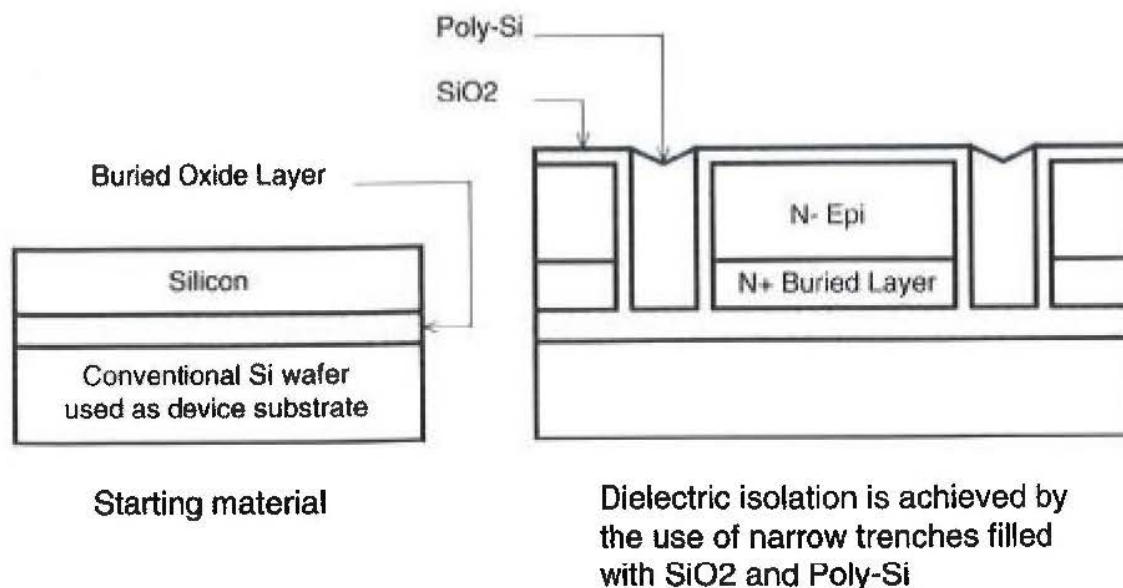


Fig. 1.2 Dielectric Isolation approach using Silicon Direct Bonding technique plus narrow trenches filled with SiO₂ and polysilicon

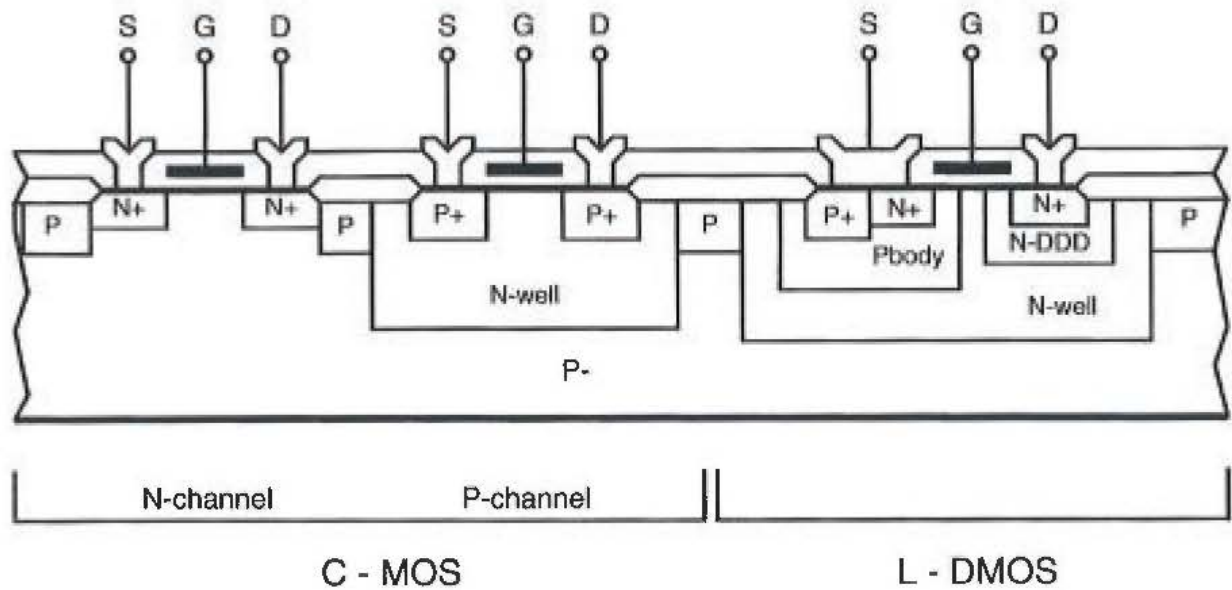


Fig. 1.3 Self isolation approach on P-type substrate: this example allows to integrate CMOS and Lateral DMOS components with drain contact on top chip surface and limited source follower capability

Discrete Power DMOS + Isolation Tub

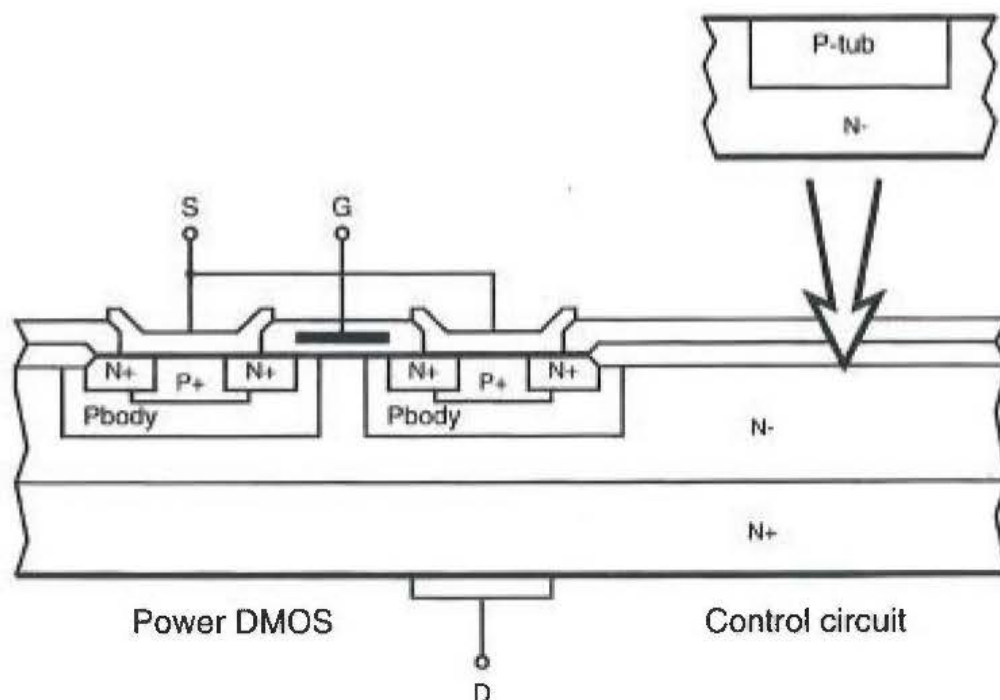


Fig. 1.4 Self isolation approach on N^-/N^+ substrate: this example allows to integrate NMOS and Vertical DMOS components with drain contact placed on the back side of the die

In this case the process is very simple and generally consists of a basic flowchart, for example CMOS or DMOS, to which a few extra steps are added to integrate additional structures. On the other side, this technique is not very flexible and is more susceptible to parasitic effects connected with biasing and supply.

Self-isolation lends itself to the integration both of high voltage and of high current devices. In high voltage devices the most common approach is carried out with the drain/collector contact on the top of the chip (Fig. 1.3). Typical applications are display drivers [17] and PWM controllers [18]. In high current devices the drain/collector contact is usually positioned on the rear of the chip (Fig. 1.4) [19].

Junction Isolation

With the junction-isolation technique the separation of the silicon islands where the various components are integrated is obtained through reverse-biased junctions realised by diffusing P regions through the entire depth of the N-type epitaxial layer grown on a P-type substrate (Fig. 1.5a). This technique is the most widely used because it offers the best compromise between cost and versatility. With various methodologies it is possible to extend the applicability of this technique to both lateral and vertical structures, high voltage and high current. With the up and down isolation approach (Fig. 1.5b), it is straightforward to produce integrated 250 V vertical DMOS devices [20–21] and the feasibility of devices up to 450 V has been demonstrated [22]. Voltages up to 1200 V have been reached applying the REDuced SURface Field (RESURF) technique [23] to lateral DMOS devices [24]. Higher currents are obtained in junction isolation processes where the power device is integrated following the vertical scheme [19, 25, 26].

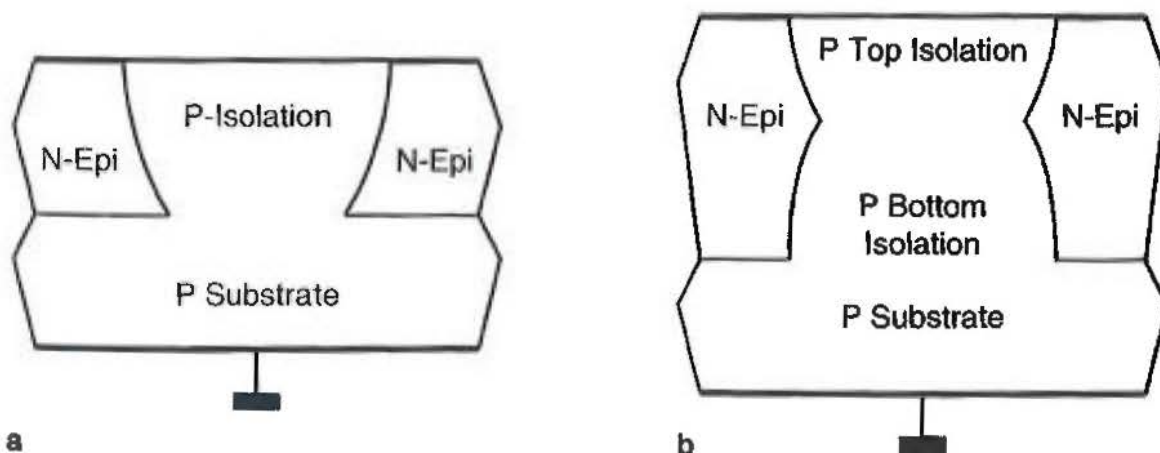


Fig. 1.5 Junction Isolation approach: a down P diffusion in thin epitaxial layer; b up and down P diffusion in thick epitaxial layer

Table 1.1 Comparison of MOS and Bipolar power transistors

MOS	BIPOLARS
Main differences	
– <i>Majority carrier device</i> no charge storage effects high switching speed drift current – <i>Voltage driven</i> high input impedance no dc driving current consumption simple drive circuitry – <i>Negative temperature coefficient of drain current for V_{GS} slightly higher than V_{TH}</i> no thermal runaway no second breakdown limitation – <i>Low transconductance</i> – <i>Drain current is proportional to channel perimeter over length ratio</i>	– <i>Minority carrier device</i> charge stored in the base and collector low switching speed diffusion current – <i>Current driven</i> low input impedance dc driving current consumption complex drive circuitry – <i>Positive temperature coefficient of collector current</i> thermal runaway effect susceptible to second breakdown – <i>High transconductance</i> – <i>Collector current is proportional to emitter area</i>

1.2.2

Integrated Power Structures

The most common power device used in a Smart Power Integrated Circuit is the DMOS [27] transistor for the well-known advantages that it offers compared to bipolar transistors (Table 1.1).

Several kinds of new power devices like IGBTs [28], IEGTs [29], ESTs [30], MCTs [31], just to mention the major ones, have been developed to compete with the performances of DMOS in high voltage and high current applications, but all these approaches are only aimed at market niches. Besides, as these are SCRs or thyristor-based structures, to overcome the problems coming from the current injection into the substrate, that can be a limiting factor to make them suitable as power elements in an integrated circuit, more recently the majority of these developments have been realised on SOI substrates.

Vertical & Horizontal Structures

As far as the geometry of power device integration is concerned, the positioning of the drain/collector contact on the surface or the rear of the chip is determined not only by the technology [25] but also by the needs of the application.

In a vertical structure the current flows through the device from the top to the bottom, across the substrate and the die attach area to the package itself (Fig. 1.6). This scheme, with the substrate above ground potential, is like that of

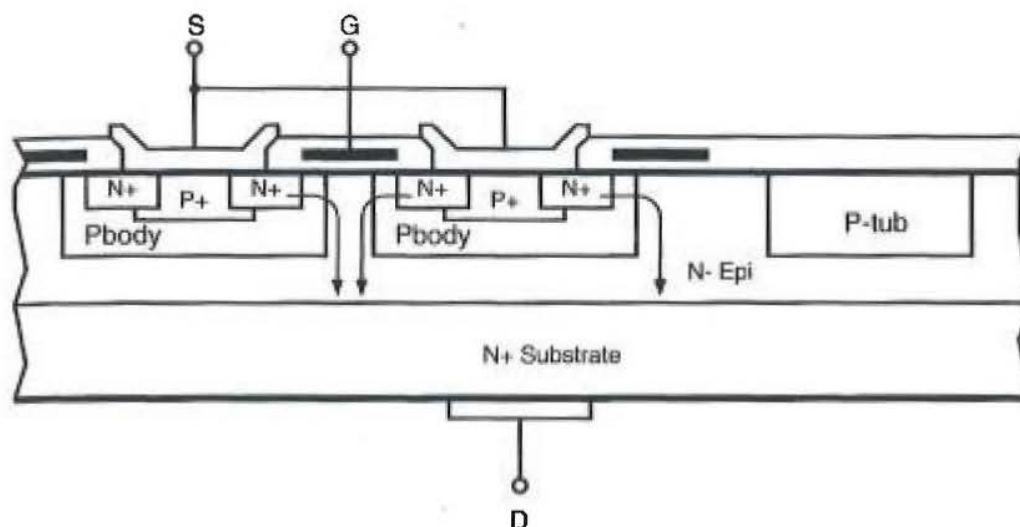


Fig. 1.6 Current flow in a Vertical structure

discrete power devices with the addition of an isolated structure containing the control circuitry. The vertical structure allows very high current densities but there is the limitation that in one chip it is only possible to integrate one power transistor, or several with the collectors or drains shared.

In a horizontal structure the current enters and leaves the chip through the upper surface of the chip. In this case, too, an isolated structure can be added that contains the control circuitry. This structure is derived from that adopted in standard power integrated circuits where the substrate is simply a mechanical support and a heat conductor. In the horizontal structure several variations can be distinguished on the basis of the current and voltage required.

Low Voltage High Current

Using DMOS as the power element the best structure in terms of specific ON-resistance is the lateral structure for voltage operation of few tens of volts (Fig. 1.7a).

High Voltage Low Current

The horizontal lateral structure that exploits the RESURF technique to reduce the surface electric field, is the most suitable for applications above 250–300 V (Fig. 1.7b).

In the junction-isolation approach this solution is generally limited to electrical configurations where the source floating capability is limited to few tens of volts.

This limitation can be overcome using a SOI approach.

Medium Voltage Medium Current

In mixed horizontal/vertical structures the current flow is vertical in the power device structure but the current is brought to the surface through buried layers

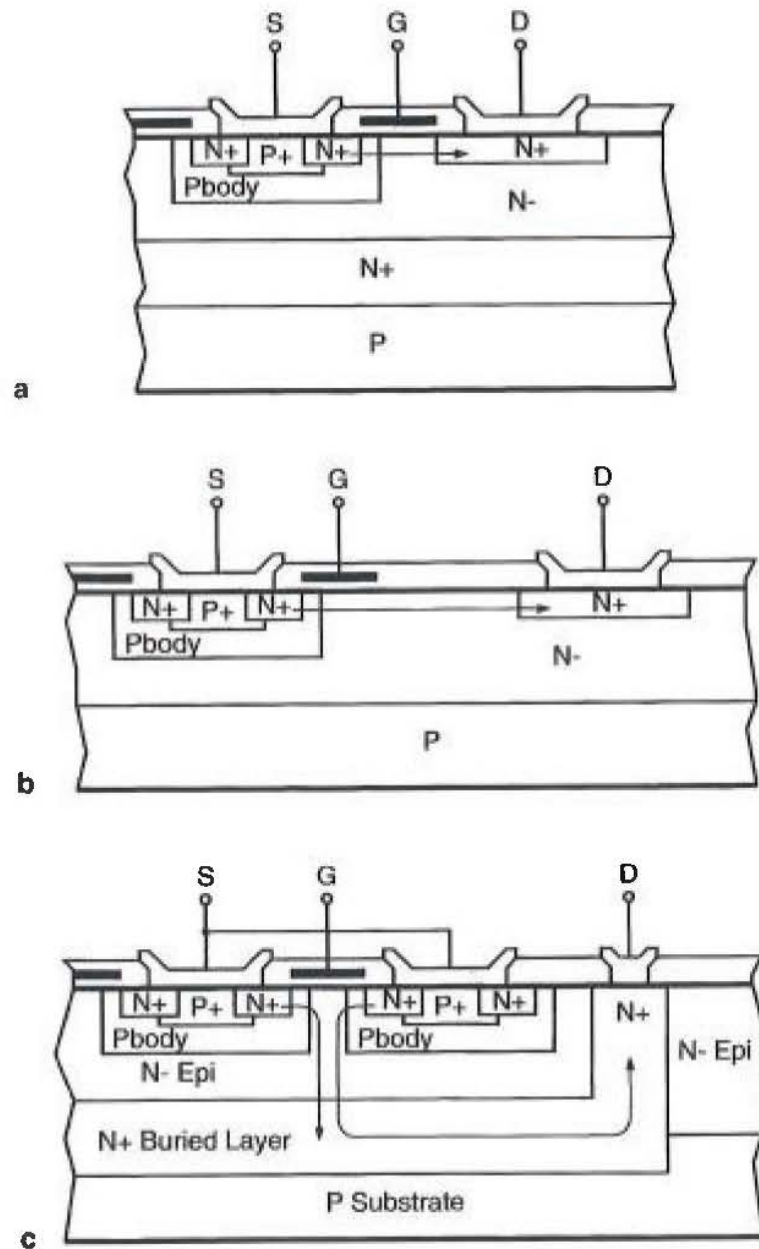


Fig. 1.7 Current flows in Horizontal structures

and sinkers (Fig. 1.7c). This approach allows the integration of any number of power devices connected in any way; in addition it offers medium currents and high voltages.

1.3 Multipower-BCD

The name Multipower originates from the possibility to integrate into one chip any number of DMOS power transistors interconnected in any way thanks to the use of the junction-isolation approach. Thus it becomes possible to integrate

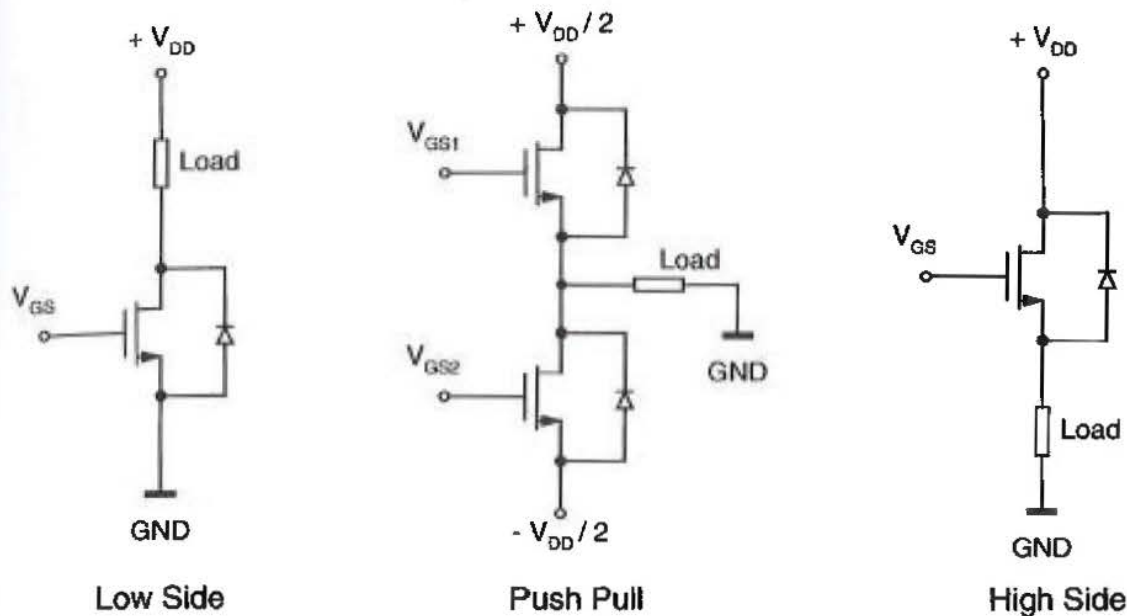


Fig. 1.8 Flexibility in the output stages

High-Side Drivers, Low-Side Drivers, Half bridges, full H-bridges and even multiple bridges (Fig. 1.8).

This feature distinguishes Multipower-BCD from the other Power IC family centred on a single power DMOS transistor, built like a discrete component, with the addition of control circuits.

This difference in flexibility makes Multipower-BCD usable in a broader application field than the other family named "Smart Discrete" that is dealt with in Chapter 3.

1.4

BCD History and Evolution

In Fig. 1.9 the genesis and evolution of the whole BCD process family are shown.

The given dates refer to the availability of the first working silicon.

The BCD process evolution has developed not only in the voltage direction (from 16 to 700 V), but also towards the reduction of the minimum lithography that is today scaled down to 0.6 μm in BCD-V.

In fact, another important advantage of the BCD is the dramatic increase of complexity induced in the Power ICs. This has been possible because in the BCD technology the power component is an MOS transistor where the current density depends on the geometrical ratio W/L (channel width/channel length) that can be improved simply by reducing the line width. Differently, in the power bipolar components the current density depends on the emitter area and therefore progress in microlithography does not bring any appreciable improvement in density.

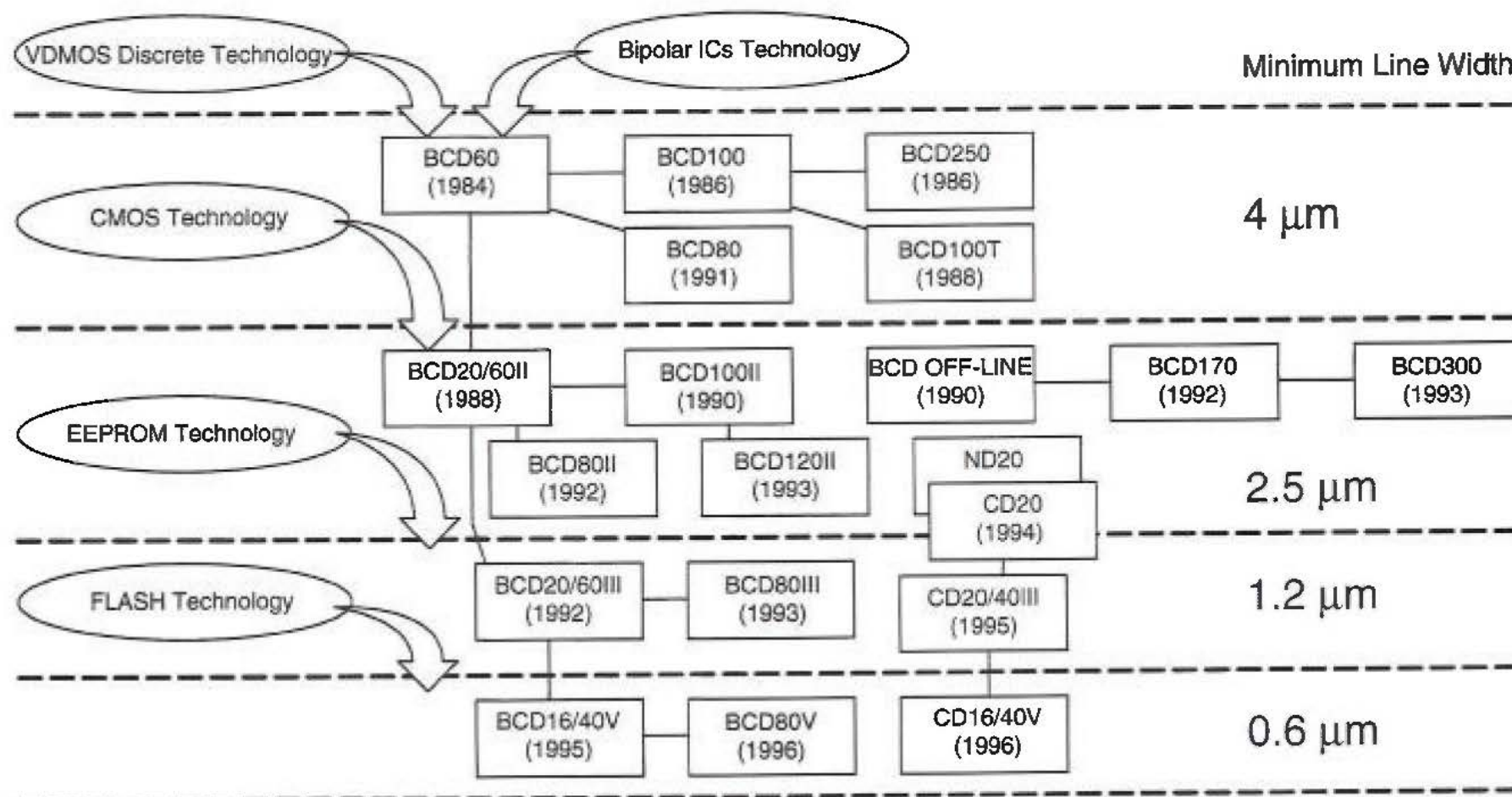


Fig. 1.9 Genesis and evolution of the BCD process family

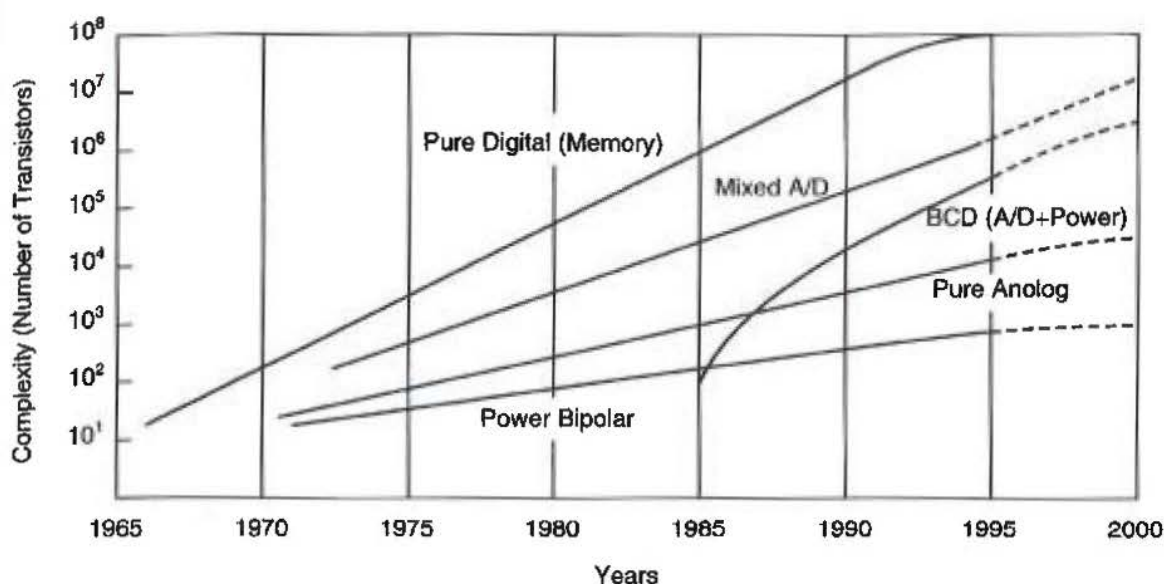


Fig. 1.10 Integrable transistor number versus time for different technology families

Combining the MOS compatibility of the BCD process with the gain obtained by moving from analog to digital signal processing, gives a complexity curve for BCD that is almost as steep as the digital memory curve (Fig. 1.10) and much steeper than the one for bipolar Power ICs.

1.4.1

First Generation (BCD-I)

The architecture of the first generation BCD process was based on the silicon gate self-aligned Vertical DMOS structure (VDMOS). Bipolar and CMOS components were added to this by applying the same doping profiles and polysilicon layer in a standard junction-isolation technology (Fig. 1.11); 4 μm was the minimum lithography used and 60 V, 100 V, 250 V were the maximum operating voltage classes developed.

The first commercially available product appeared in 1985 and it was a general purpose H-bridge motor driver IC designed in BCD60 process (Fig. 1.12) [32].

This IC demonstrated immediately the advantage of DMOS in this application because the DIP package version delivered 1.5 A continuous output current (the DMOS ON-resistance is 0.3 Ω) outperforming a similar bipolar bridge in a more expensive power package.

Products developed subsequently integrated more complex control circuits, such as a complete 10 A switch-mode regulator [33] or a stepper motor controller/driver.

However, the complexity of these circuits was limited not by the technology but because the full exploitation of the capability of the technology had to wait until system designers began to change their approach to partitioning.

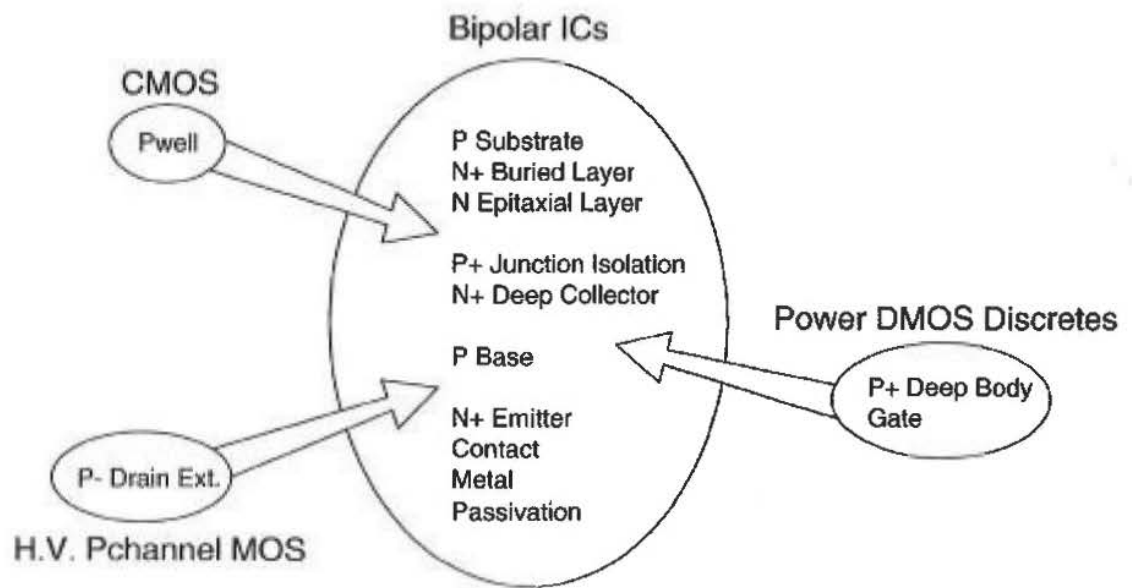


Fig. 1.11 Process architecture of First BCD generation

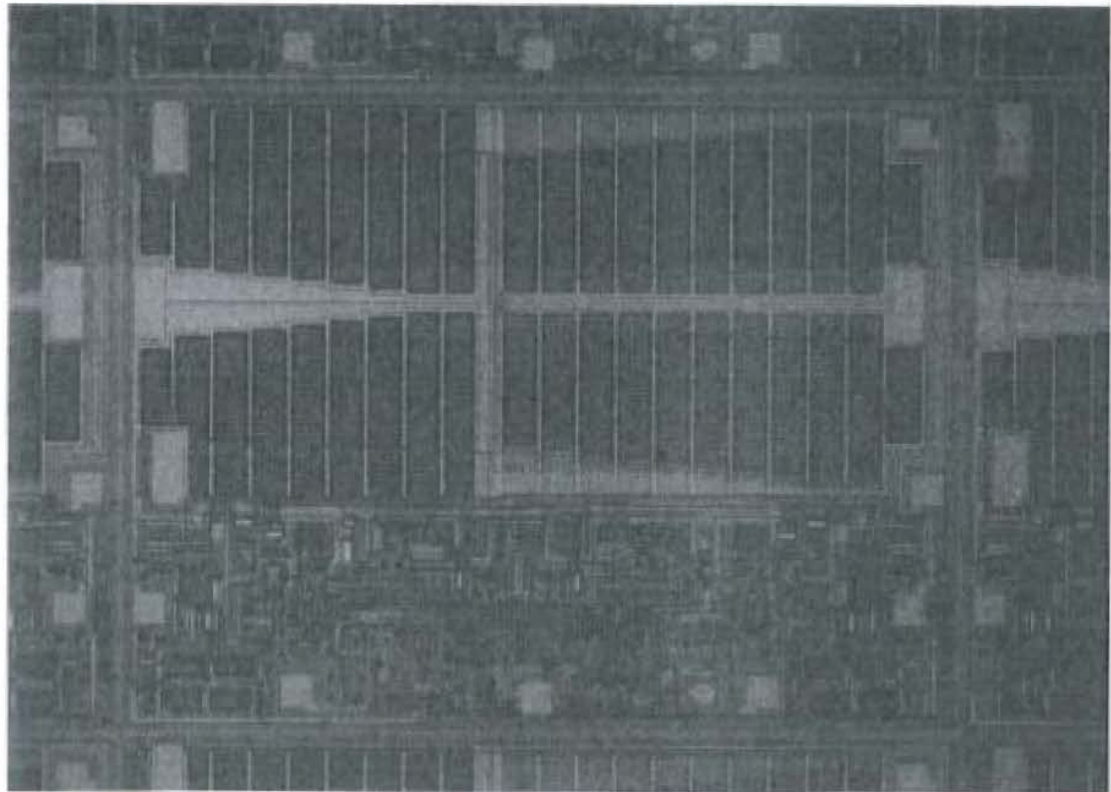


Fig. 1.12 Chip photograph of the first commercial BCD product: an H-bridge motor driver

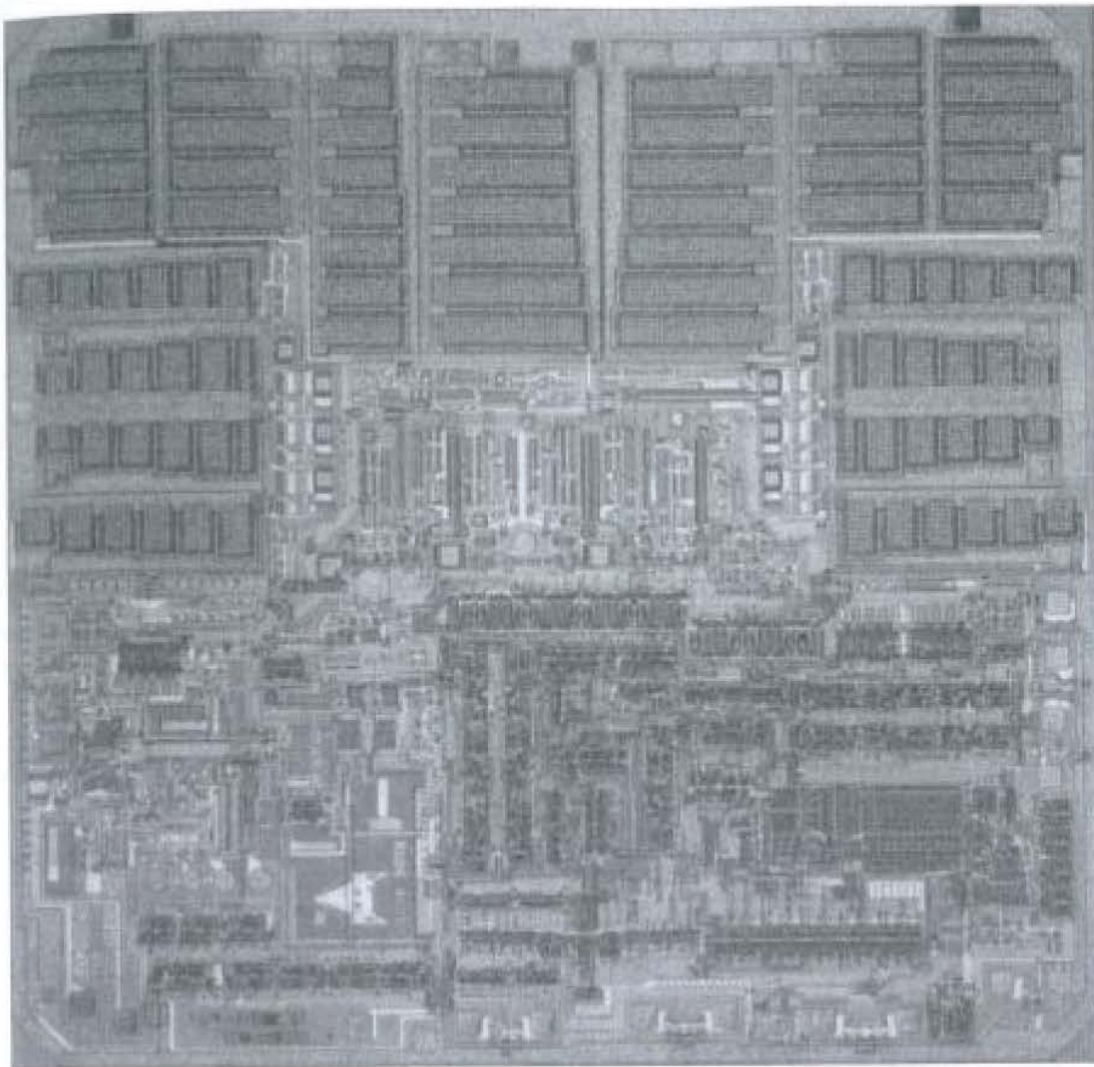


Fig. 1.13 Photograph of a single chip solution for electronic typewriter including three motor drivers and a solenoid driver

This was demonstrated in 1988 when a single chip power system was produced for a typewriter application (Fig. 1.13) [34].

Though this type of solution was possible using the first BCD process, the die size necessary for such levels of complexity made it too costly for many applications.

Therefore to make chips of this complexity truly cost effective it was essential to shrink the technology from the original $4\text{ }\mu\text{m}$ of the first generation to $2.5\text{ }\mu\text{m}$ of the second generation.

1.4.2

Second Generation (BCD-II)

In this new generation the core of the process was centred on CMOS to improve circuit design complexity (Fig. 1.14).

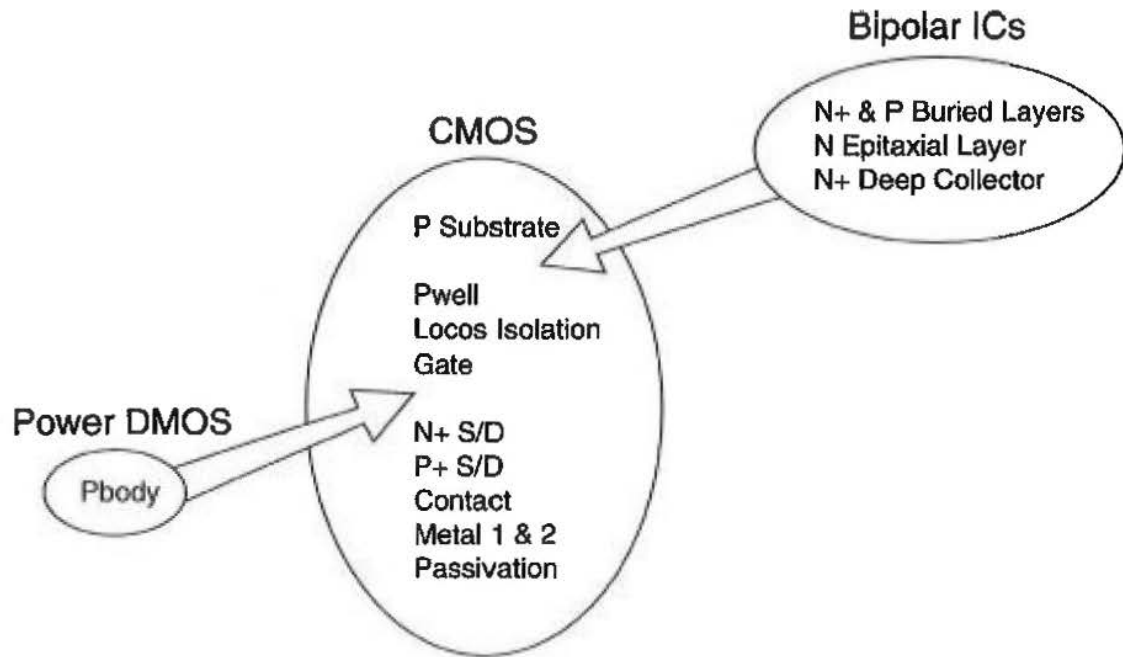


Fig. 1.14 Process architecture of Second BCD generation

This evolution approximately doubled both the signal section component density and the power section current density.

The availability of the second generation has widened the application fields and therefore many versions have been developed where the power devices are rated at 16 V, 20 V, 30 V, 40 V, 60 V, 80 V, 100 V and 120 V.

One of the first examples of a BCD-II product is the one shown in Fig. 1.15 which integrates into a single chip all the circuits needed to control and drive both the spindle motor (a three-phase brushless DC motor) and the head positioner (a “voice coil” actuator) in a hard disk drive. This chip includes 12 power DMOS transistors plus about 10 000 other transistors, though even this is still a long way from the limit of the technology.

To cover applications that require to be supplied directly from the mains, like the lamp ballast, in the second generation a version named BCD OFF-LINE has been developed, where the DMOS transistors are able to withstand reverse voltages as high as 700 V exploiting the RESURF approach. Similar to the other second generation BCD processes, also the BCD OFF-LINE architecture is based on a CMOS process [35].

An additional polysilicon level is introduced to build up the high voltage components and a twin-well structure is used (Fig. 1.16).

From this technology, designed primarily for industrial and off-line applications, it is possible to derive versions operating at lower voltages (170 V–300 V) that, with some additional structures, will also find applications in the display driving fields.

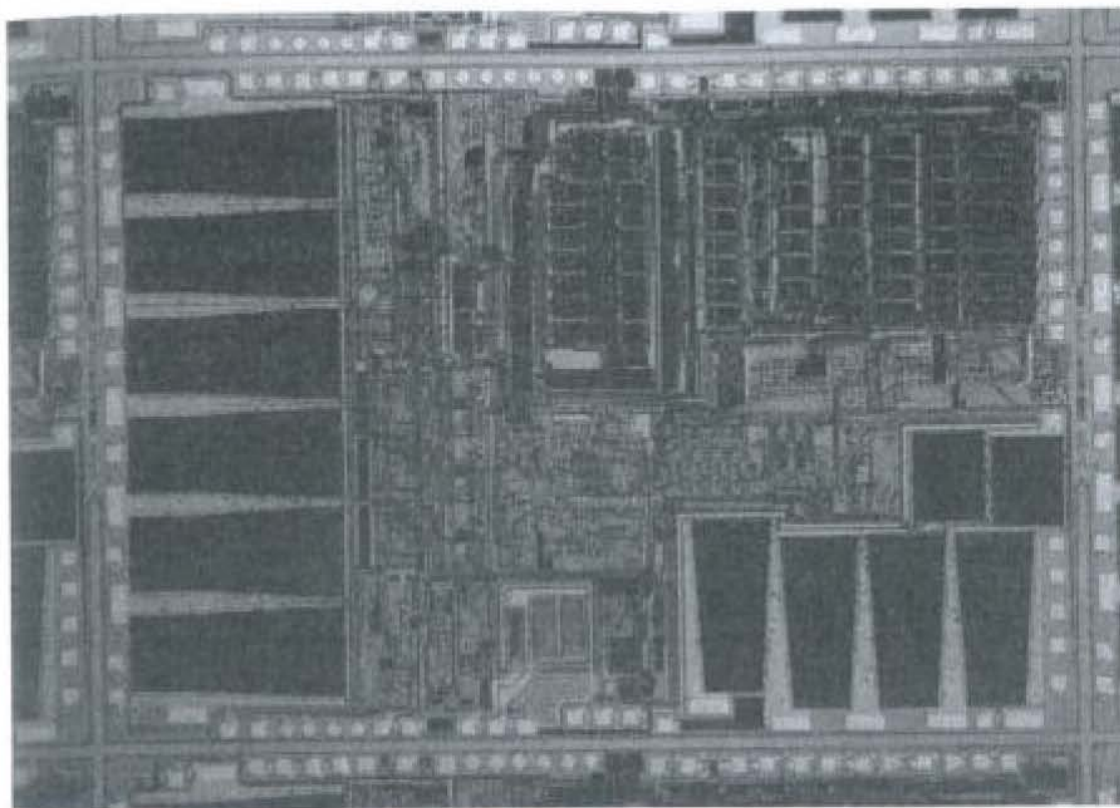


Fig. 1.15 Photograph of a single chip combo circuit for hard disk drive applications realised in BCD-II

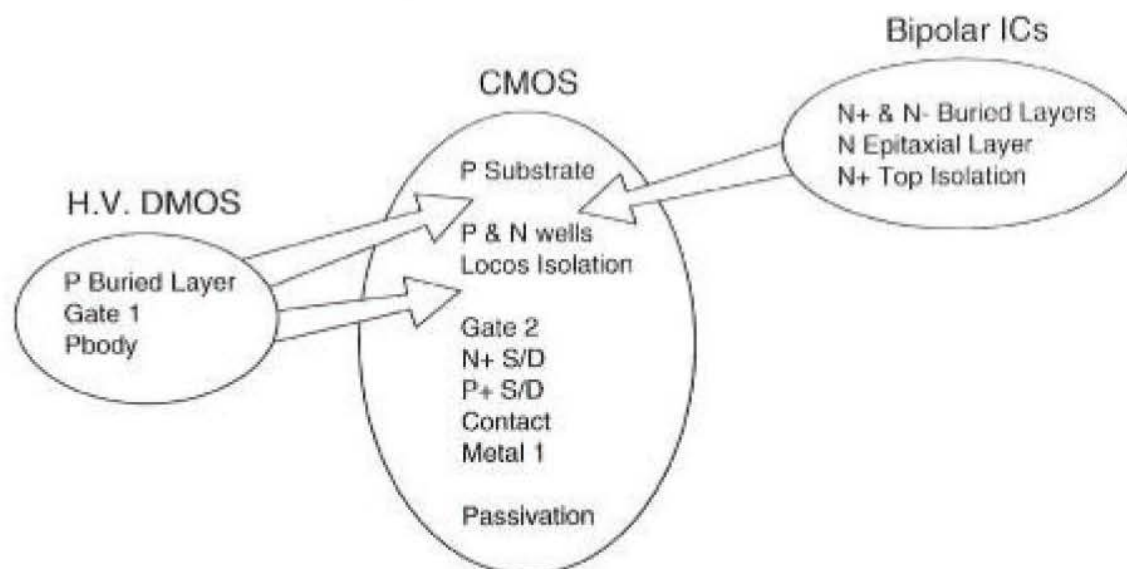


Fig. 1.16 Process architecture of BCD OFF-LINE for high voltage applications

1.4.3

System Oriented Generations

With the appearance, in the early nineties, of the third generation at $1.2\ \mu\text{m}$ (BCD-III) where non-volatile memories (EPROM and EEPROM) are integrable too, the complexity level reached in the BCD processes has allowed to generate a new complete class of Power ICs, named “System Oriented” [36].

This name comes from the capability of these circuits to integrate into a single monolithic solution entire systems, previously realised with more chips made with single-function technologies, like pure CMOS, bipolars and non-volatile memories.

In applications where space is limited this approach is very useful because it reduces complex systems to a minimum number of chips, just one in some cases. The trend towards portable equipment brings a need for space reduction but at the same time reduces power requirements, encouraging the move to solutions of this type.

The architecture of the third generation is based on the concept of modularity where additional process blocks for optional structures and components can be added to a basic process flow-chart without creating any disturbance. The core of the process is based on a twin-well CMOS technology used to produce micro-processors, memories, gate arrays and other logic devices (Fig. 1.17) [37].

Moreover to reconcile the conflicting demands of packing density and current capacity there are three levels of metallization: two for high density

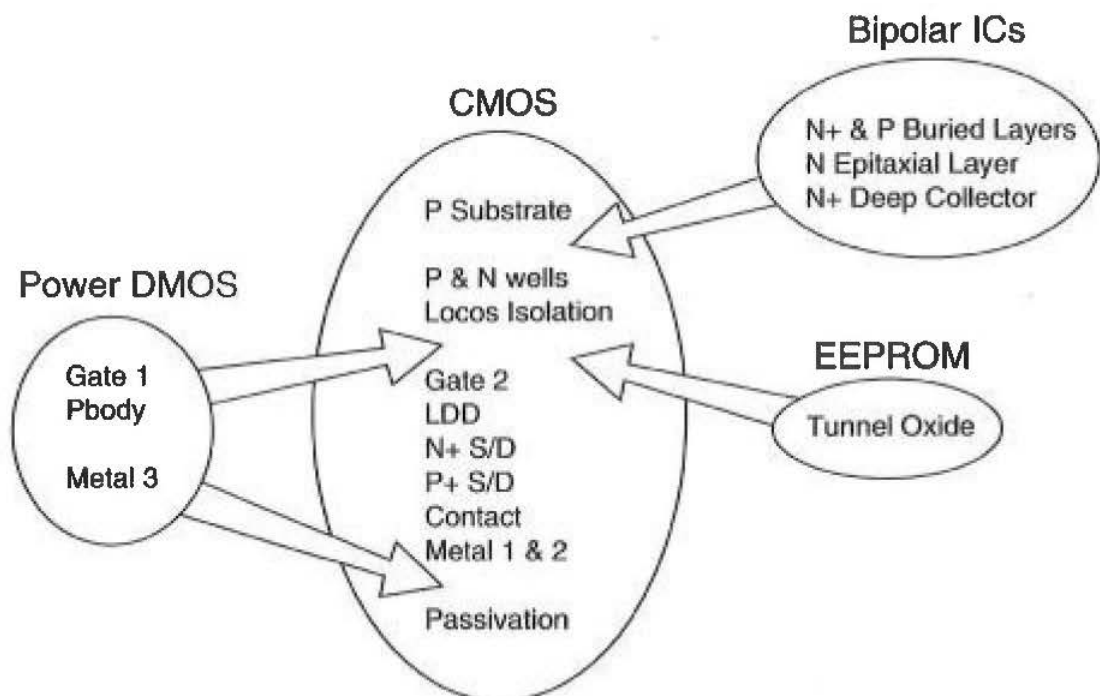


Fig. 1.17 Process architecture of Third BCD generation

interconnections in the signal section and a thicker layer for low resistance connections in the power sections.

With respect to the previous generation the current density in power devices is doubled and the density in signal components is almost tripled.

The third generation BCD is the first real example that allows designers to take advantage of existing CMOS libraries and even to include standard micro-computer cores and EEPROM memories to realize "Software programmable Smart Power" chips (SSP = Super Smart Power).

An interesting example of a complete system realised in a single chip solution using BCD-III is the Super Smart Battery Charger, that is a monolithic PWM current controller driving a 60 V, 0.1 Ω VDMOS with embedded a standard ST6 (8 bit) microcontroller with 2 Kbytes of internal EPROM and 64 bytes of internal RAM (see Chapter 11).

In the mid 90s, a 0.6 μm generation (BCD-V) has been introduced giving the possibility to integrate Flash memories, too.

At this level of lithography much more complex circuits will become feasible integrating other micro and DSP cores widening the field of application for system oriented technologies.

In automotive, for example, they can be used to make single-chip smart switches for multiplex wiring systems. They can also be used in the computer field to make hard disk drives, in telecom to produce a one-chip cellular phone, in home automation to make a one-chip network node, in cameras to control all the motors and display functions, in industrial control and in many other fields. Other possible applications include medical implants, display drivers, flat-panel displays and even one-chip products with built-in sensors.

1.5

Process Architecture and Device Technology

In this section, the major steps involved in the BCD process construction are comprehensively listed and described to reach a complete understanding of the process architectures and of the function of each step putting them in relation with the integrable components.

In all BCD processes the construction sequence starts from a $\langle 100 \rangle$ P-type substrate whose doping level is chosen according to the maximum required voltage capability.

The key processing steps are

- N^+ buried layers Antimony or Arsenic doped are implanted to create low resistive paths for collector or drain current, to avoid punch-through limitation of floating P regions towards the P substrate and to kill the gain of the parasitic vertical PNP with the P substrate acting as a collector.
- N buried layers Phosphorous doped are added in high voltage processes both to increase the breakdown voltage of N^+ buried layers versus substrate and to implement source follower capability in RESURF type high voltage devices.

- P buried layers are introduced with isolation function: a "seed" of dopant is implanted before epitaxial growth and in subsequent thermal treatments this diffuses upwards to meet a downward diffusion from the surface. This approach is followed to save silicon area. In fact, a simple diffusion of a single-junction isolating layer from the top would require prolonged thermal treatments and consequently a larger lateral diffusion (Fig. 1.5 b).
The same P buried layer can be used as buried anode of a diode featuring very low current losses towards the substrate because the gain of the parasitic substrate PNP associated to this diode is almost negligible (Fig. 1.18).
In the RESURF approach P buried layers are introduced and dimensioned mainly to work together with the substrate in sustaining high reverse voltages (Fig. 1.19).
- The N epitaxial layer grown at this step, is dimensioned to obtain the best trade-off between maximum (close to ideal) breakdown voltage and minimum epitaxial bulk resistance contribution to ON-resistance when VDMOS is used as a power component. In BCD processes in which VDMOS is not implemented the epitaxial layer is only added to allow the formation of buried layers and the doping level is determined mostly by implanted N- and P-well regions.
- The junction-isolation structure is completed by the introduction of the top isolation. In the first BCD generation this is a heavily doped layer obtained by a solid source as in the traditional junction-isolation bipolar Power ICs and the P-well regions to realize NMOS transistors for CMOS circuits are introduced by ion implantation at a specific step before the top isolation deposition.

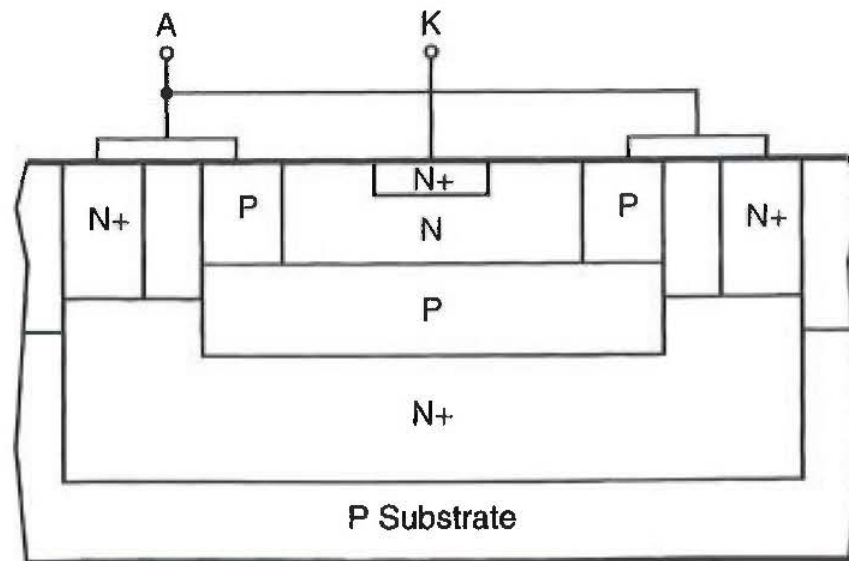
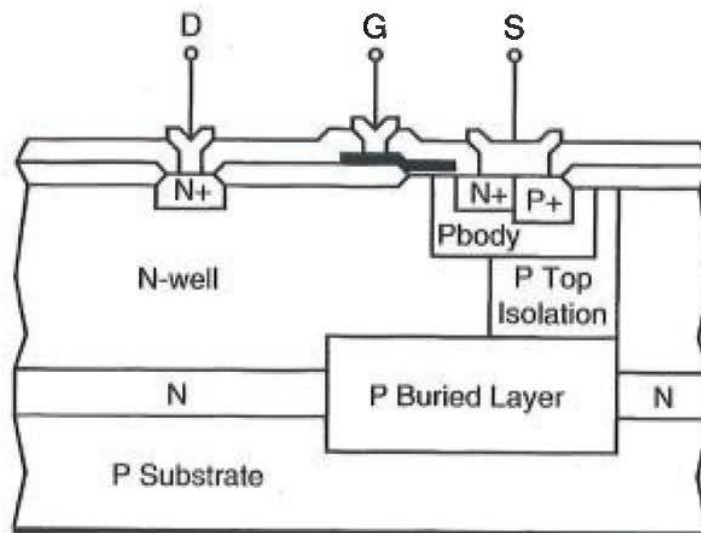


Fig. 1.18 Cross-section of a Low Leakage Diode (LLD) structure with P buried layer used as buried anode



H. V. LDMOS

Fig. 1.19 Cross-section of RESURF type high voltage Lateral DMOS with P buried layer working as electric field shaping structure by enhancing depletion layer near source region

From the second generation onwards the top isolation function is realized by the P-well itself saving one mask and heavy process steps.

A separated step is still adopted in thick epi-layer processes and when power LIGBT (Lateral IGBT) devices are implemented.

- N-well regions are inserted when high density CMOS circuits are obtainable like in the third BCD generation at 1.2 μm .
N-well regions are also introduced in high voltage RESURF type processes to better control the total charge in the drift regions of the RESURF acting structures (Fig. 1.19).
- Highly doped sinker plugs are realized by a Phosphorous deposition to contact the N^+ buried layer in order to bring up the current to the die surface in the vertical power devices. In the thick epi BCD processes, these sinker plugs are used in conjunction with buried sinker plugs to limit the area occupancy due to large side diffusions (Fig. 1.20).
- Highly doped P layers are implanted to form contact regions, lateral PNP emitter and collector and in the CMOS N-channel FET as a channel stopper on the P-well surface (BCD-I). The same layer is used also in the body of the DMOS component to contact the body itself and to reduce the value of the pinched resistance under the N^+ source region, that is, the base resistance of the parasitic intrinsic bipolar NPN transistor. As a consequence, the parasitic bipolar latch-back limit increases, making the DMOS more robust.

The position of this step at this point in the process flow is peculiar to the first generation, while from the second generation on it has been moved to the

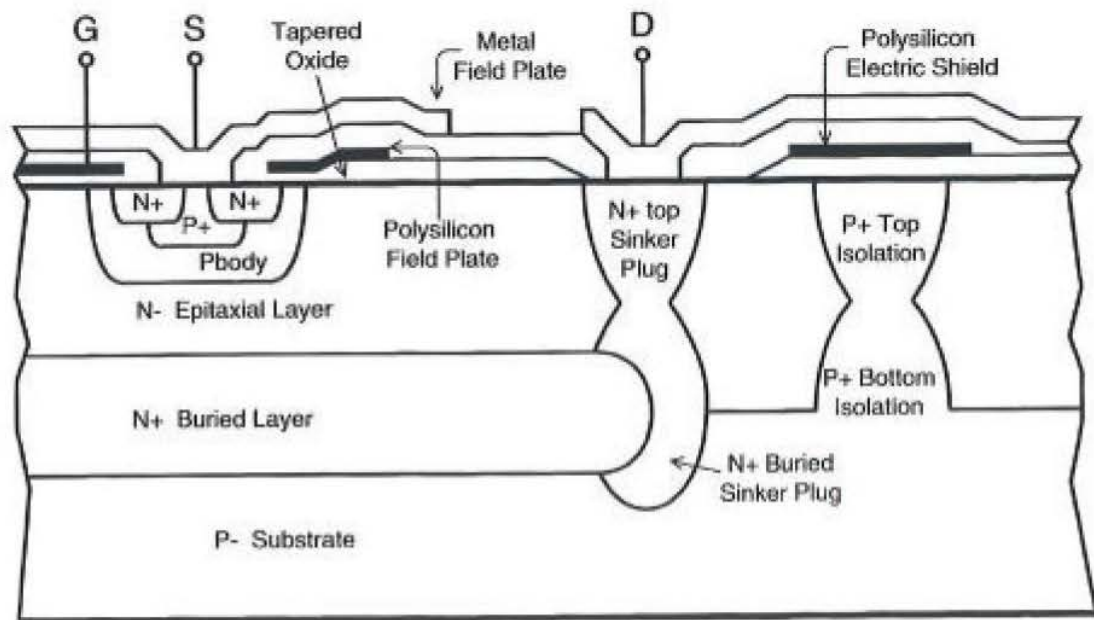


Fig. 1.20 Cross-section of high voltage Vertical DMOS in thick epitaxial layer in which deep drain contact to N⁺ buried layer is obtained via an up-and-down scheme for N⁺ sinker diffusion to reduce the area occupancy

final part of the process flow, like in a pure CMOS process architecture to make source/drain regions for PMOS, in order to increase the CMOS density.

In this way, once obtained the platform to allocate the different integrable components, the BCD process flow continues with more specific construction steps aiming at the realization of the active part of the components and at the achievement of their performances.

- The active areas are defined in different ways depending on the process generation.

In BCD-I, that is centred on the DMOS component, a thick oxide (field oxide) is patterned and etched after a high dose, low energy implant to obtain tapered oxide profiles with a very low angle. The slope of this oxide step is very important to realize high efficiency polysilicon field plates used to withstand the voltage in DMOS structures (Fig. 1.20). Furthermore, the smoothed oxide edge improves the metal step coverage even with very thick oxides.

To encounter the requests of much denser CMOS logic, starting from BCD-II, the LOCOS technique has been adopted (Fig. 1.21 a). This technique is based on the selective growth of a thick oxide (field oxide) on a silicon surface masked by a patterned silicon nitride.

The nitride protects the underlying silicon from oxidizing, while allowing a thermal SiO₂ layer to grow on the exposed silicon: as a result the field oxide is semi-recessed under the starting surface. Therefore, the width of the base of the field oxide step defining the active area regions is reduced with respect to the tapered approach where this step is obtained by a prolonged wet etch.

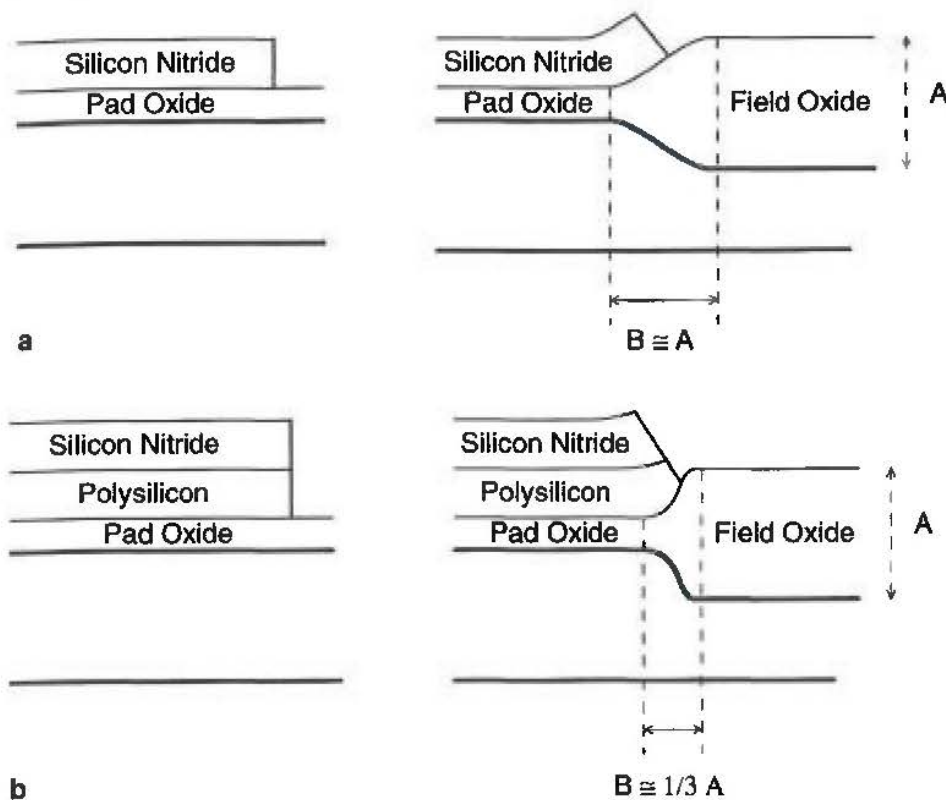


Fig. 1.21 Field oxide isolation techniques: a LOCOS; b Poly-Buffered LOCOS (PBL). The PBL technique allows to reduce the “bird beak” length compared to standard LOCOS

With the migration of the minimum lithography to values lower than $0.8 \mu\text{m}$ (BCD-V), the Poly-Buffered LOCOS (PBL) technique is used to further increase the transistor density (Fig. 1.21 b).

- With the introduction of the LOCOS technique to form the component active areas in the BCD processes, it is also possible to obtain self-aligned channel stoppers on the CMOS body regions. These channel stoppers are formed by N- and P-type regions, named N field and P field, implanted before the field oxide growth and are masked by the nitride left to inhibit the surface oxidation. Therefore, these layers can be positioned only under the thick oxide and never inside an active area (Fig. 1.22 a). The result is the increase of the surface concentration of P well, N well, N epi and consequently of the parasitic threshold voltage of polysilicon gate on field oxide.

The P-field layer is also used as a drain extension in the P-channel MOS transistor to increase its voltage capability up the maximum value requested by the process rating (Fig. 1.22 b).

- The gate oxide is grown inside the active area and it is used in all the MOS components. The required CMOS transistor density of the third generation BCD process forces to reduce the gate-oxide thickness to values not compatible with the high voltage performances needed in the vertical DMOS and high voltage P-channel MOS (H.V. PMOS) transistors. In BCD-III there-

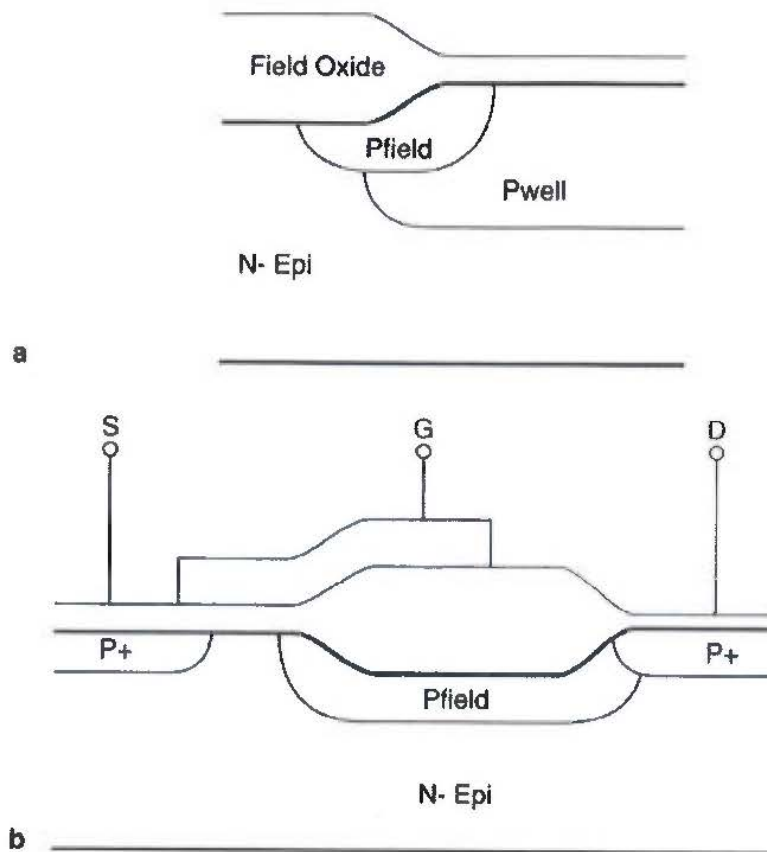


Fig. 1.22 P-field layer main functions: a self-aligned channel stopper to increase parasitic threshold voltage on P-well regions; b drain extension region in high voltage P-channel MOSFETs

fore there is a first oxidation step used as gate-oxide growth for DMOS and H.V. PMOS transistors only, while the gate-oxide growth for the CMOS components is shifted after the first polysilicon layer deposition and DMOS body diffusion step. In this case, a second polysilicon layer is also added and N^+ and P^+ source and drain implants are following. This approach has been adopted also in the BCD OFF-LINE version due to the very high voltage target for the DMOS components.

- At this point optional implants can be added to the process flow to adjust the MOS threshold voltages.
- The first polysilicon gate electrode, deposited and N doped at this step, is also used as field plate, channel stopper and as an interconnection level.

According to the modular approach, that is peculiar to the more advanced BCD process generations, additional steps can be inserted in the process flow before the polysilicon deposition in order to implement the EPROM an EEPROM cells.

- The control gate is constructed by a dedicated high dose N implant performed after the removal of the nitride layer used to define the active areas.

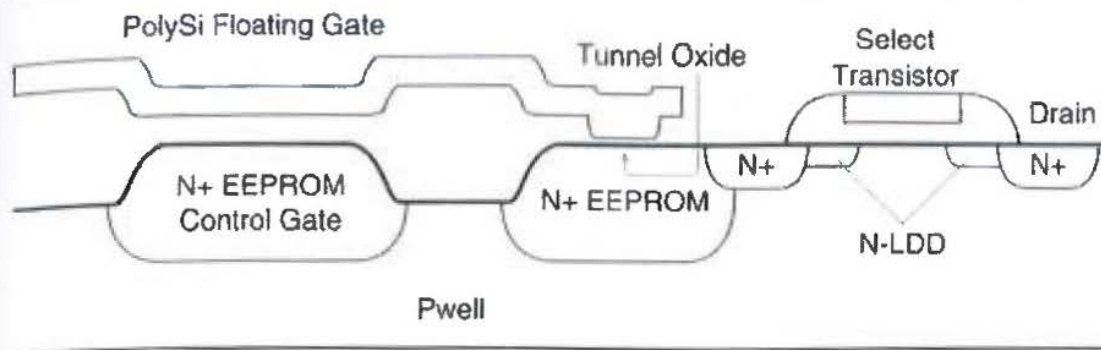


Fig. 1.23 Cross-section of a single-Poly structure EEPROM cell

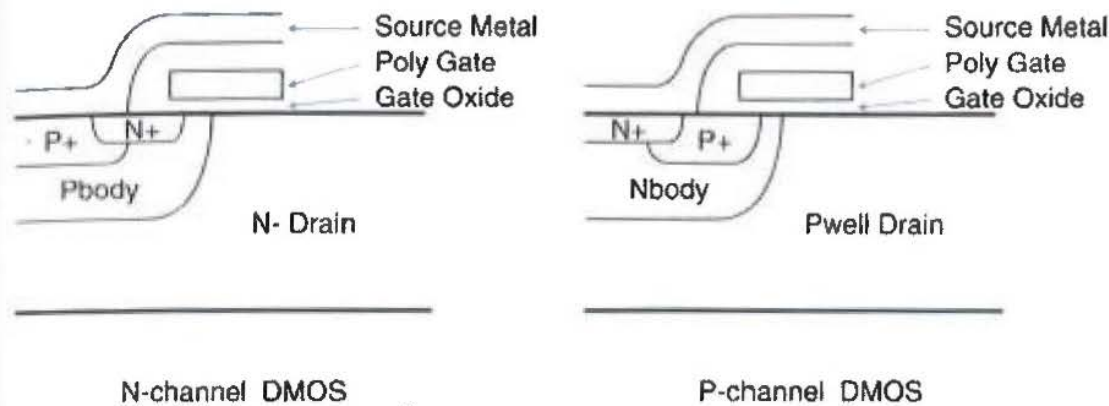


Fig. 1.24 N-channel and P-channel DMOS structure cross-sections

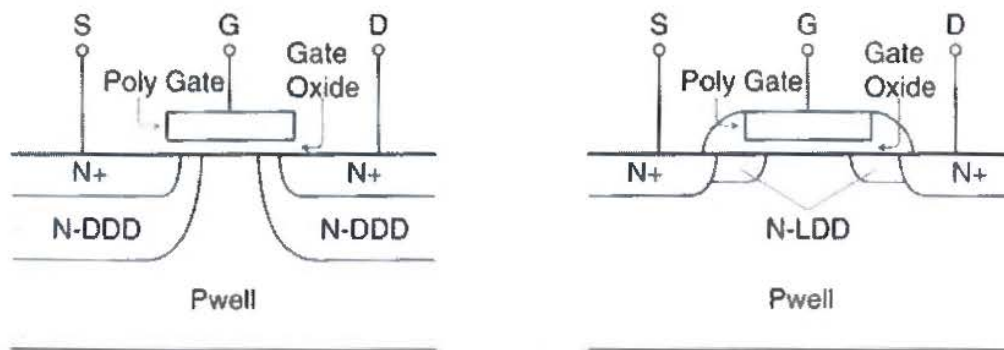


Fig. 1.25 Cross-section of DDD and LDD NMOS structures. The DDD or LDD layers are introduced to improve NMOS ruggedness against hot electron degradation

- In the EEPROM structure an extra mask is used to strip off the gate oxide from the areas where the tunnel oxide must be grown (Fig. 1.23).
- Self-aligned N and P implants are performed and diffused to form the double-diffused channel regions of P-channel and N-channel DMOS transistors (Fig. 1.24).

The process parameters of these DMOS body implant and diffusion steps are key factors in the trade-off between the off-state breakdown and the on-state

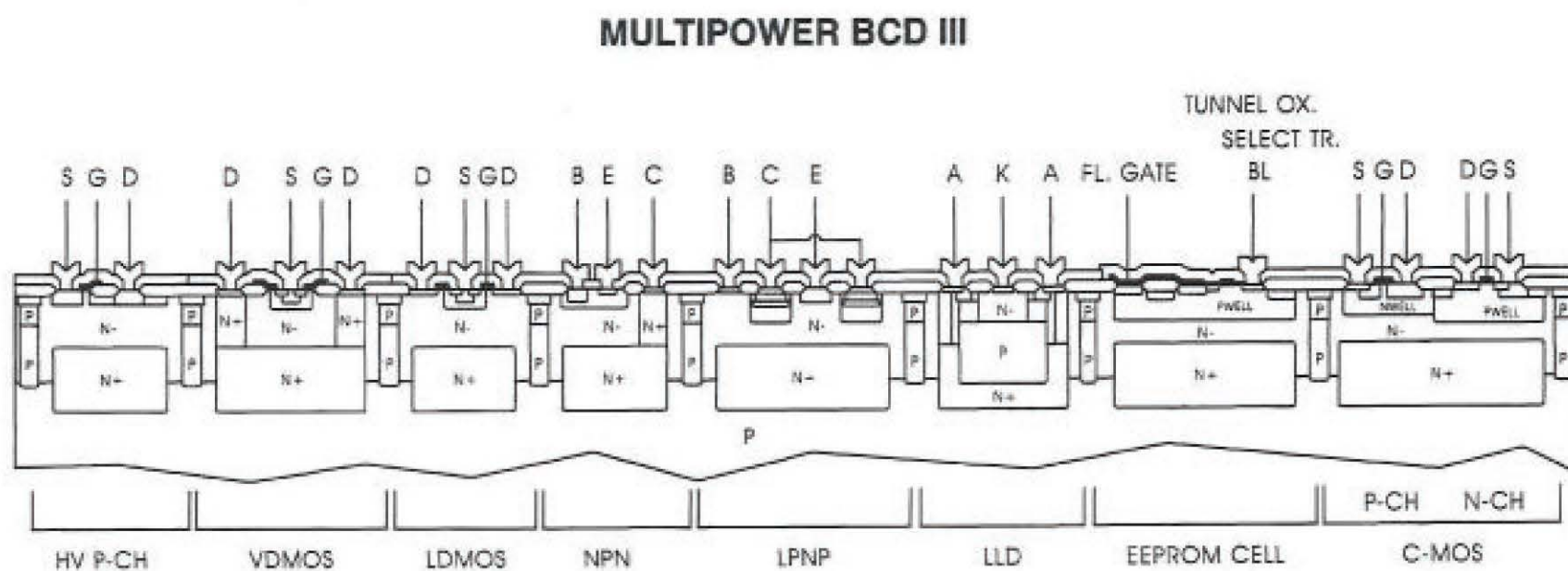


Fig. 1.26 Cross-section of BCD-III process through first metal deposition

performance that must be stated in the high voltage power DMOS components. The P-body layer has a wide use as the base of NPN transistors and as P-channel MOS source and drain regions.

- Standard DDD (Double Doped Drain) and LDD (Lightly Doped Drain) implant and spacer formation steps are carried out to build up source and drain extension regions of N-channel and P-channel MOS transistors to be used in high performance CMOS structures (Fig. 1.25).

In the same way, the availability of the spacer technique gives benefit in increasing the drain to source maximum voltage capability of compact Lateral DMOS (LDMOS) components.

- After the N^+ and P^+ implants used to form source, drain and contact regions, a standard Boron Phosphorous Silicon Glass (BPSG) layer is deposited and the whole structure is provided with the conventional next contact opening step and with the first thin metal deposition.
- The following adopted metallization scheme strongly depends on the BCD process generation and can be distinguished in two major families: the single level, double thickness metal process and the multiple level, multiple thickness metal process. The former, used in the first and partially in the second generations, is obtained stacking a second thick metal on the first metal layer to increase the overall metal thickness in order to obtain a low resistance path for the current to be handled in the power sections and to improve the ruggedness against electromigration phenomena.

The latter has been imported in the BCD processes to make the CMOS part compatible also in the interconnection scheme with pure CMOS processes.

In this way, the portability of complex logic circuits is guaranteed and the advantage of the VLSI design can be fully exploited.

Anyway, this scheme has been adapted to the Smart Power IC requirements, dimensioning the last metal level thickness in order to be used in the power components.

As an example of the BCD process architecture, in Fig. 1.26 the BCD-III cross-section is shown, with the main integrable components.

1.6

Integrable Devices: DMOS Transistors

Both bipolar and DMOS power transistors are widely used in Smart Power ICs. The choice of the power elements for application in switching conditions is based, in addition to the physical comparisons given in Table 1, on the efficiency in silicon area consumption as shown in Fig. 1.27.

For high voltage applications (i.e. > 100 V) the DMOS is better than the bipolar even in processes with a relatively large minimum lithography ($4\text{ }\mu\text{m}$). The DMOS advantage is due to the fact that its drain-to-source breakdown voltage fixes the device voltage capability that is determined by reaching the critical electric field at the body/drain junction.

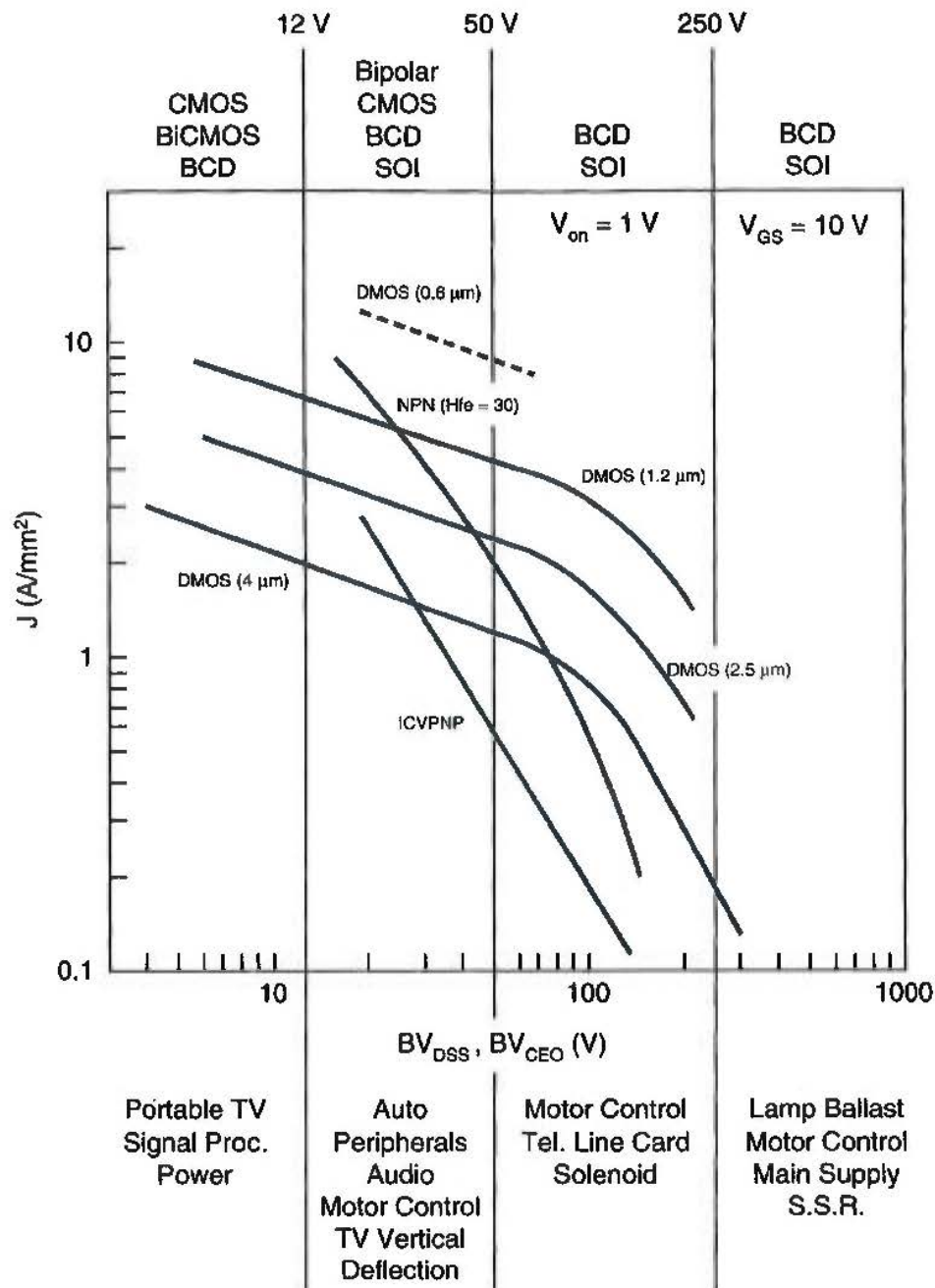


Fig. 1.27 Comparison between power bipolar and power DMOS transistors in terms of current density versus voltage capability for different process generations

In the bipolar device the transistor current gain lowers the breakdown voltage of the base/collector junction. Therefore to guarantee the same blocking voltage capability the bipolar transistor needs a thicker and more resistive epitaxial layer that penalizes its on-state performance.

Moving on to reduced minimum lithography, the DMOS transistor has taken advantage both in vertical configuration and particularly if realized in lateral arrangement. As a consequence, the breakeven point is shifted down to 20 V.

In this section, after a brief description of the DMOS structure, the optimization of its ON-resistance, that is the key parameter for the DMOS transistor operating in switching applications, will be deeply treated together with the other two parameters V_{th} and BV_{dss} that are fundamental in the device construction design.

Furthermore, the DMOS performances in the saturation region will be analyzed, too, as this component is becoming of interest also for the realisation of amplification stages in audio and telecom application fields.

DMOS structure

In the DMOS device, the channel region is obtained by the difference in lateral diffusion of two different impurity profiles introduced through the same opening in the polysilicon layer. The obtainable DMOS channel length is therefore very short and it does not depend on lithography accuracy.

Two different ways to build up the device exist depending on the drain position that determines the current flow direction.

In the vertical approach the power DMOS device consists of a number of transistors with parallel source and gate electrodes integrated into a single isolated area with a common drain. The integration of this component requires bringing the drain contact to the surface via a N^+ buried layer and a N^+ sinker diffusion.

In this case, the current flows through the sinker to the buried layer and then up to the surface (Fig. 1.7c).

On the contrary, in the lateral approach the drain, positioned in front of each source, forces the current to flow horizontally (Fig. 1.7a, 1.7b).

1.6.1

Off-State Performance

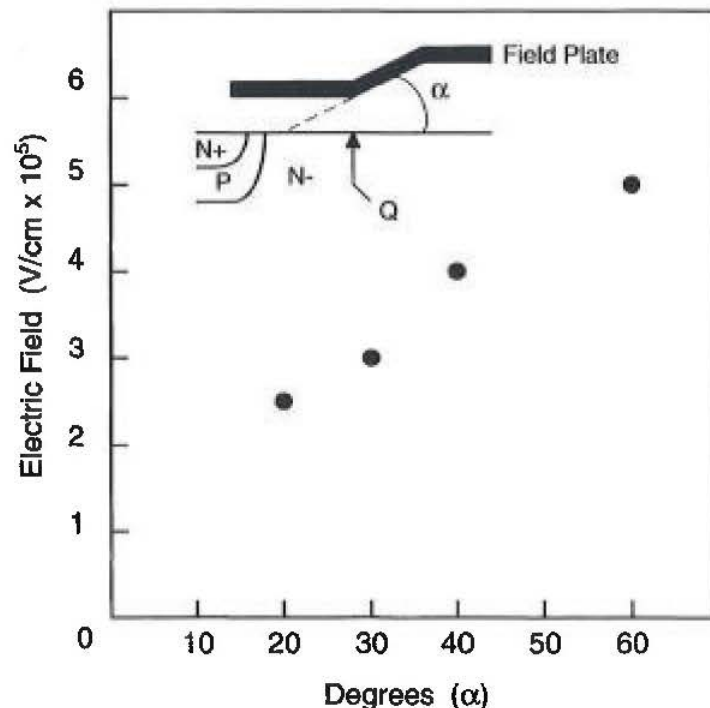
To obtain the best trade-off between maximum (close to ideal) breakdown voltage and minimum epitaxial bulk resistance, in the vertical DMOS design considerations and investigations concentrate in the edge termination structure of the P body/N epitaxial junction.

In almost all BCD process generations an efficient and reliable solution consists of a polysilicon field plate overlaying the gate and field oxides forming a standard biplanar structure [38]. The best dimensioning of the polysilicon field plate is determined using a bi-dimensional device simulator. This operation allows to highlight the high electric field critical points of this solution and it allows to fix the proper epi-layer thickness and resistivity specification to achieve the best trade-off between the minimum contribution on the on-state resistance and the required breakdown voltage.

One of the most critical points of the biplanar structure is the transition region between the thin gate oxide and the thick field oxide as pointed out in Fig. 1.28.

In this figure, the case of the first generation vertical DMOS edge termination is depicted showing the influence of the level angle of the transition region on

Fig. 1.28 Electric field at point Q versus the level angle of the filed oxide with a constant applied voltage



the surface electric field under that point. In fact, the electric field arising in that point when the angle is wide, causes electron injection into the oxide giving lowered and walking-out breakdown voltage values. The use of the LOCOS technique to define the active areas, from the second BCD process generation onwards, allows to reduce the electric field in the above mentioned critical region by adding a floating P-type ring, self-aligned to the active area. This layer helps to make a more uniform voltage partitioning (Fig. 1.29).

This ring can be formed by the P-field diffusion, already used in CMOS to increase the parasitic threshold voltage of polysilicon interconnections on field oxide over the P well, without requiring any additional mask and any extra ion implantation step.

To integrate the 250 V vertical DMOS device a triplanar structure must be adopted: it is realized extending the source metal beyond the polysilicon field plate edge over a third oxide level with an increased thickness (Fig. 1.20). The third field plate level serves to reduce the surface electric field at the edge of the polysilicon field plate that, otherwise, limits the component voltage capability.

In the vertical DMOS component the breakdown voltage condition can also occur between the inside cells. In this region, the spacing between two neighbouring cells plays a fundamental role in fixing the maximum electric field value as is shown in fig. 1.30. When the spacing becomes too large, the positive combined effect of the adjacent P-body depletion layers and of the gate field plate disappears. Each cell works like an individual P body/epi junction protected by a planar polysilicon field plate placed on a thin gate oxide. This is a less efficient structure than the biplanar one.

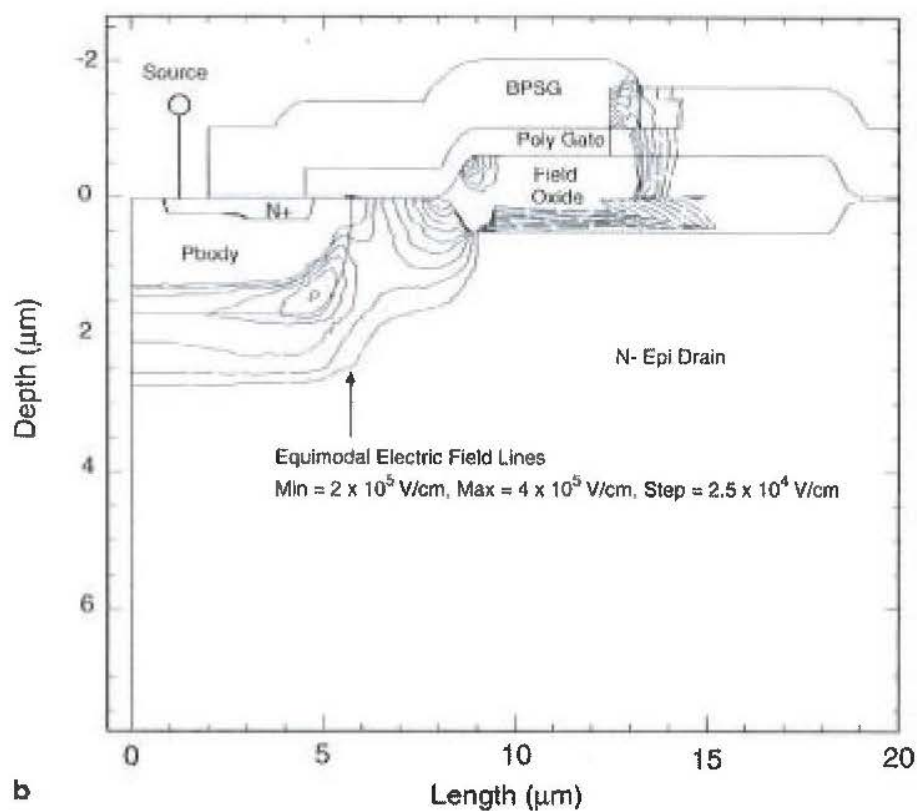
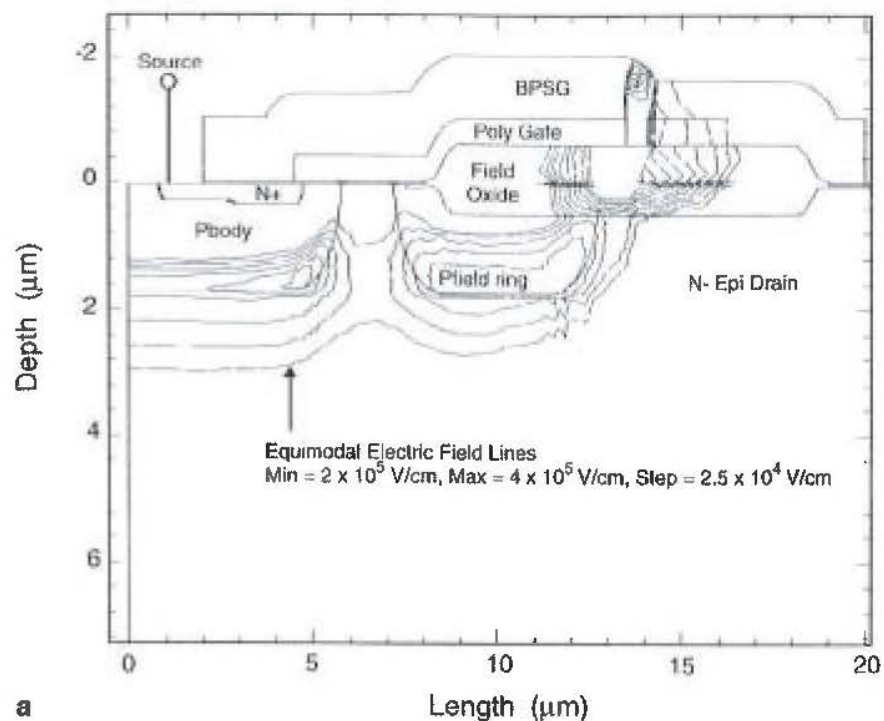


Fig. 1.29 Cross-section of VDMOS edge termination using LOCOS showing equimodal electric field lines. A self-aligned P-field floating ring (structure a) avoids the arising of a high electric field at the transition point between gate oxide and field oxide, present instead in the structure b) without P-field ring

Fig. 1.30 Electric field at the inside cells as a function of the cell spacing in the case of 250 V BCD Vertical DMOS

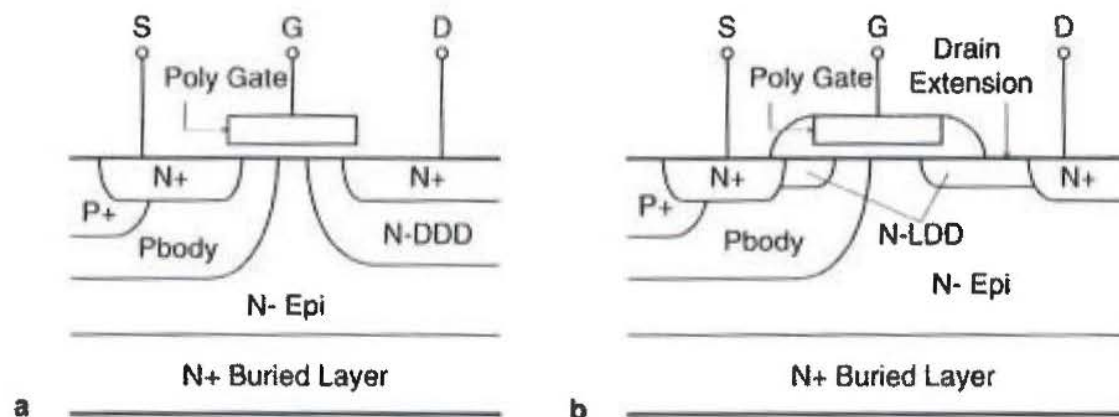
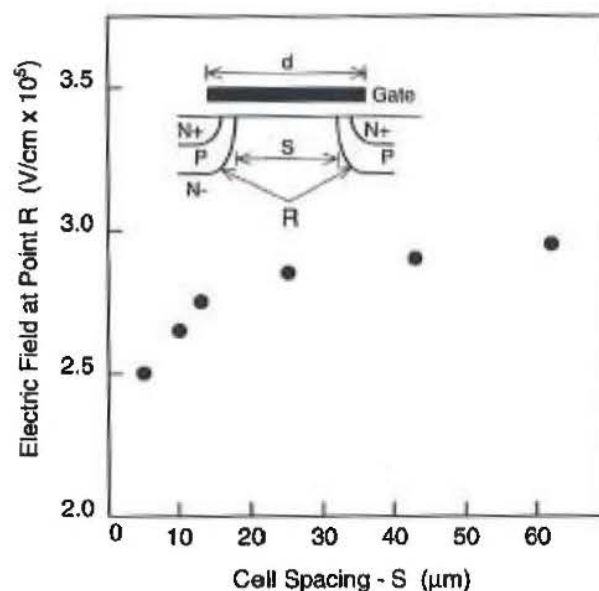


Fig. 1.31 Cross-sections of low voltage (from 16 V to about 30 V) Lateral DMOS using (a) N⁻ DDD or (b) N⁻ LDD layers in the drain region to reduce high electric field across the gate oxide

For very high off-state breakdown voltage values (> 250–300 V) the vertical structure is not suitable because it would require an epi layer so thick to become unpractical to create isolated islands by using the standard up and down junction isolation plugs.

To overcome this limitation, a completely different approach is followed: the RESURF principle (see Chapter 2). Exploiting this technique a lateral DMOS component can be placed in a thin epitaxial layer, withstanding voltages as high as 700 V.

When the lateral DMOS structure is used for low voltage applications, if drain and source are diffused in the same active area opening, the breakdown is typically located at the drain edge under the polysilicon gate. To reduce the electric field at that critical point, an extended drain structure is realized using different ingredients (DDD, LDD) depending on the BCD process generation, as shown in Fig. 1.31.

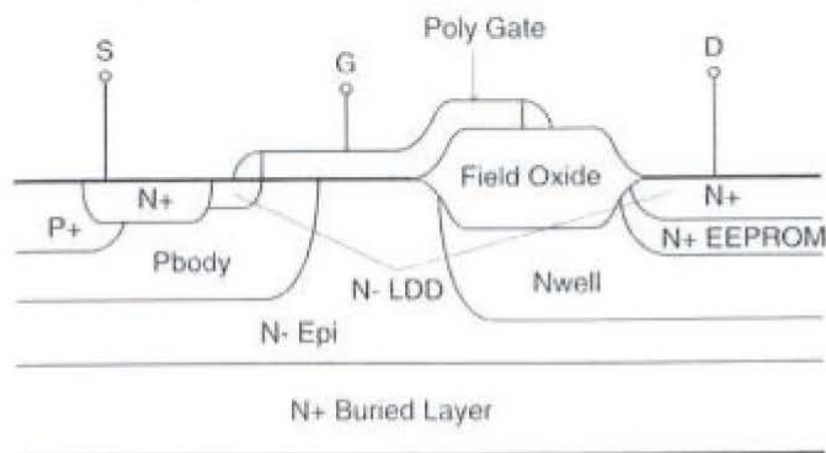


Fig. 1.32 Cross-section of medium voltage Lateral DMOS. The example shown is the 40 V device from BCD-III

With the reduction of the minimum lithography and of the LOCOS minimum size, a different lateral DMOS structure can be adopted that merges the advantages of the biplanar polysilicon field plate to improve the off-state voltage capability with the advantage of the lateral structure with respect to the vertical one for the on-state characteristics (Fig. 1.32).

1.6.2

Threshold Voltage

The value of the threshold voltage is mainly related to the thickness of the gate oxide and to the peak concentration of the laterally diffused body in the region included between source and drain.

The doping profile of the body region is multifunctional in an integrated circuit and consequently many trade-offs must be satisfied. Also when used in the DMOS transistor, the P body layer characteristics must match with conflicting requirements:

- the DMOS channel length must be as short as possible and its threshold voltage must be reasonably low;
- the channel punch-through voltage must be higher than the maximum voltage capability,

Table 1.2 DMOS channel lengths and threshold voltages through different BCD generations

BCD GENERATIONS	CHANNEL LENGTH (μm)	THRESHOLD VOLTAGE (V)
BCD-I	1.50	3.0
BCD-II	1.25	2.1
BCD-III	1.00	1.7
BCD-V	0.5	1.2

- the gain of the parasitic NPN, intrinsic to the DMOS structure, must be kept as low as possible in order to increase the DMOS ruggedness.

Table 1.2 gives the scaling of channel length and threshold voltage for DMOS components in different BCD generations.

1.6.3

ON-Resistance

Vertical DMOS Transistor

The layout of an integrated vertical DMOS device consists of alternated source and drain fingers where the source fingers consist of arrays of elementary cells.

The R_{ON} is strictly dependent on the topological layout that is shape and size (packing density) of the unit source cell and cell arrangement used to fill the silicon surface.

In the Multipower-BCD the source cells are square-shaped and they are positioned on a square matrix: it has been shown in different works [39, 40] that this is one of the most efficient ways to maximize the channel width/area ratio.

The corners of the square cell are rounded or smoothed in order to avoid excessively high electric fields close to the MOS channel area when high drain to source voltages are applied. In the integrated vertical DMOS transistor the position of the drain electrode on the top must be also considered in the R_{ON} computation because it adds an extra contribution with respect to the case of the discrete device, that depends on the N^+ buried layer drift region, the N^+ sinker contact region and the layout choice for drain and source interdigitation.

The layout configuration is identified using the following mathematical model that provides the product $R_{ON} \times \text{Area}$ as a function of the physical and geometrical parameters involved in the structure (Fig. 1.33):

$$R_{ON} \times \text{Area} = \left\{ \frac{R_c}{N} + \frac{1}{12} \times R_{bl} \times N + \frac{1}{2} \times R_{bl} \times \frac{2Y}{l} + \frac{R_{sk}}{l \times X_{sk}} \right\} \times l \times (N \times l + X_{sk} + 2Y) \quad (1.1)$$

where:

- R_c is the ON-resistance of the DMOS cell and consists of four different components:
 - R_{ch} is the channel resistance,
 - R_{acc} is the accumulation layer resistance,
 - R_{JFET} is the parasitic JFET ON resistance,
 - R_{epi} is the epitaxial layer drift resistance.

The expression used for R_c relates to the well-known model of the DMOS structure [39].

- R_{bl} is the N^+ buried layer sheet resistance;
- R_{sk} is the N^+ sinker resistance per unit area;

- l is the cell pitch = $X_{\text{cell}} + d$, where X_{cell} is the DMOS cell window and d is the spacing between two DMOS cells;
- X_{sk} is the N^+ sinker window width;
- N is the number of cells between two sinker drain contacts;
- Y is the distance between the edge of the sinker window and half spacing of the last cell (this value includes the extension of the junction edge termination region).

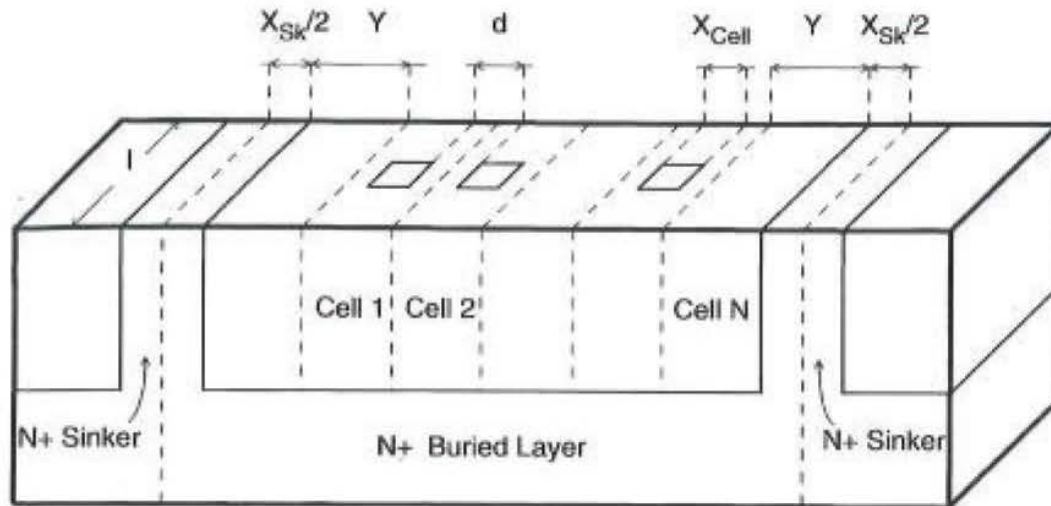


Fig. 1.33 Model for the $R_{\text{on}} \times \text{Area}$ calculation of the vertical DMOS

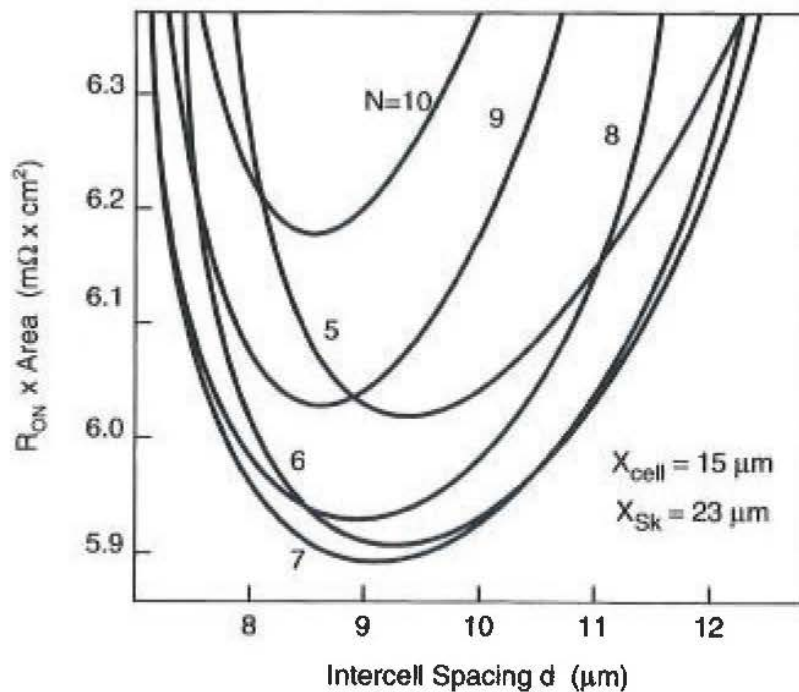


Fig. 1.34 $R_{\text{on}} \times \text{Area}$ versus intercell spacing d (parameter N : number of cells between two drain sinker contacts)

Varying the parameters X_{cell} , d , N and X_{sk} it is possible to fix the geometrical configuration that minimizes the $R_{\text{ON}} \times \text{Area}$ product that provides a measure of the efficiency of the DMOS design.

In Fig. 1.34, the $R_{\text{ON}} \times \text{Area}$ functional dependence on the intercell spacing d can be observed having as a parameter the number of cells N between two drain sinker contacts. In the reported case, that refers to the first BCD generation, the minimum value is obtained at a value of d in the range from 9 to 10 μm and at $N = 7$ [8].

This model takes into account only the silicon contributions to the ON-resistance.

With the reduction of the minimum lithography in the BCD process generations, the silicon $R_{\text{ON}} \times \text{Area}$ decreases and the metal contribution can no longer be neglected.

A new model is therefore developed that represents the DMOS device by a resistive network in which the silicon and metallization resistances are connected together in a complex way related to the power layout arrangement [41]. The equivalent resistive network for each array and for the whole device are shown in Figs. 1.35 and 1.36.

Using these models it is possible to evaluate, for a given power layout, the relative weight of the different ON-resistance terms and to identify how much they are affected by the process and layout parameters [42].

In the high voltage case (250 V), the epitaxial layer thickness and resistivity are the only parameters that influence the ON-resistance for a wide range of device size.

Lowering the voltage range (60 V and 100 V) the metal and the MOS channel contributions become comparable to the epitaxial layer term.

Evolving towards finer lithography generations and therefore increasing the DMOS channel perimeter density, the silicon contribution to the total ON-resistance reduces to levels that make the metal interconnection series resistance

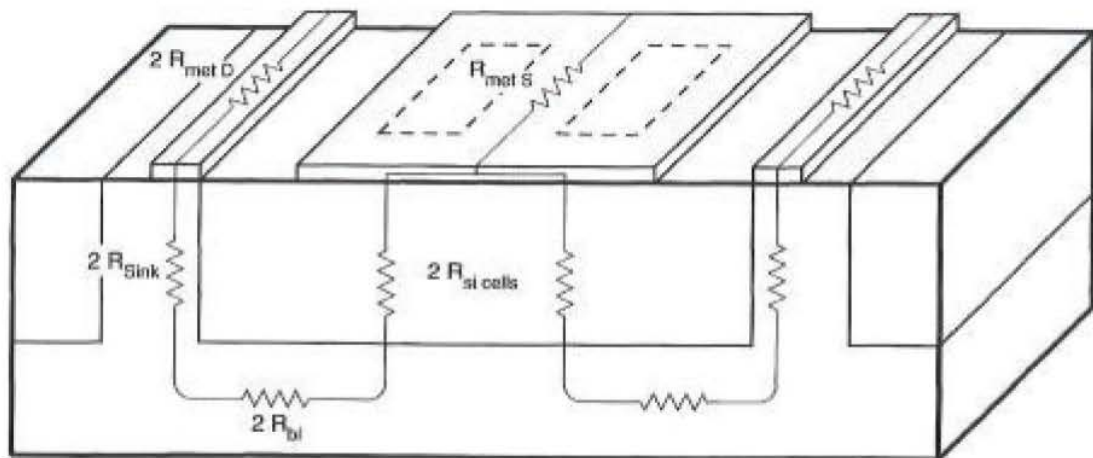


Fig. 1.35 Equivalent resistive network for a VDMOS basic finger element showing a simplified case of two cells

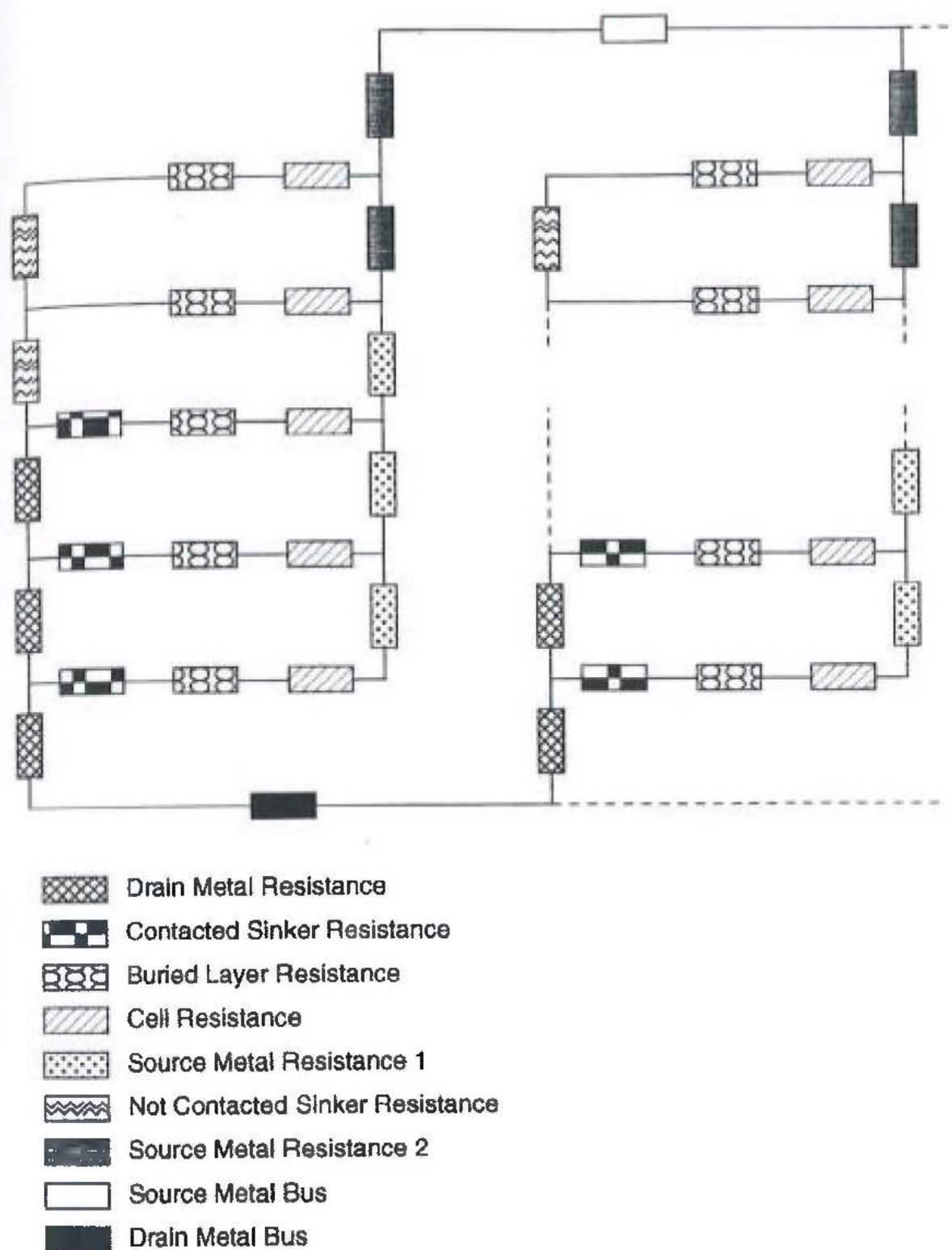
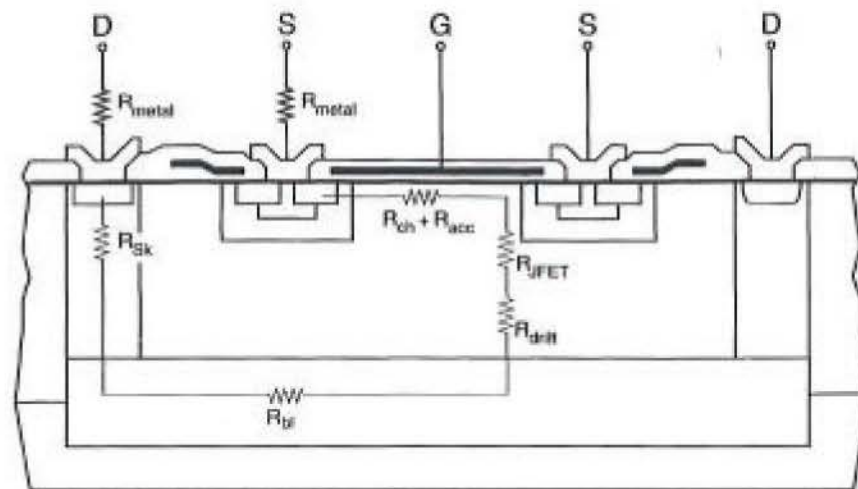


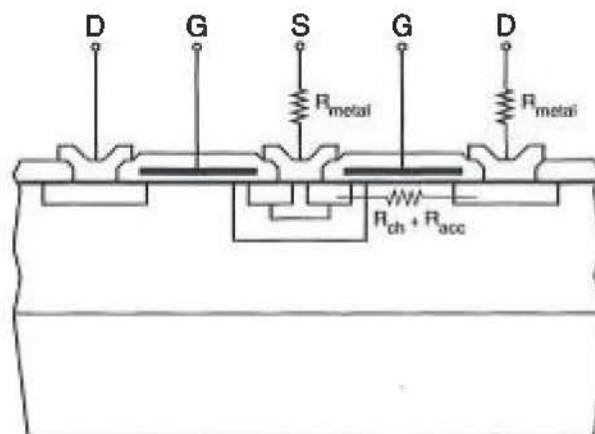
Fig. 1.36 Equivalent resistive network of an integrated VDMOS power device



Vertical DMOS

- High voltage capability
- Low ON resistance

$$R_{ON} = R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{bl} + R_{sk} + R_{metal}$$



Lateral DMOS

- Low voltage capability
- Very low ON resistance

$$R_{ON} = R_{ch} + R_{acc} + R_{metal}$$

Fig. 1.37 Contributions to the total ON-resistance in vertical and lateral DMOS transistors

relevant. The metal term reduces adopting a multiple thickness and multiple level metal process instead of a double thickness single level one used in the first BCD generation.

Lateral DMOS Transistor

As far as the power LDMOS is concerned, the R_{ON} contributions are those due the MOS channel, accumulation region, drain drift region and metal layer.

The relative weight of the drain drift region depends on the maximum reverse voltage that must be sustained by the component: it varies from a negligible value to about 90 % ranging from 20 V to 700 V.

In low voltage applications the lateral DMOS is advantageous compared to the vertical component because of the absence of different silicon contributions to the total ON-resistance (Fig. 1.37).

In this case, the percent contribution introduced by the metal interconnections becomes more relevant and therefore it becomes mandatory to introduce a multi-level metal technology in order to optimize the source and drain metallization layout scheme.

For example, in the third BCD process generation a 1 mm^2 N-channel power LDMOS device performs R_{ON} equal to 0.25, 0.12, 0.08 Ω if one, two or three metal levels are respectively used.

Fig. 1.38 shows the specific ON-resistance versus the drain-to-source breakdown voltage for the different BCD process generations.

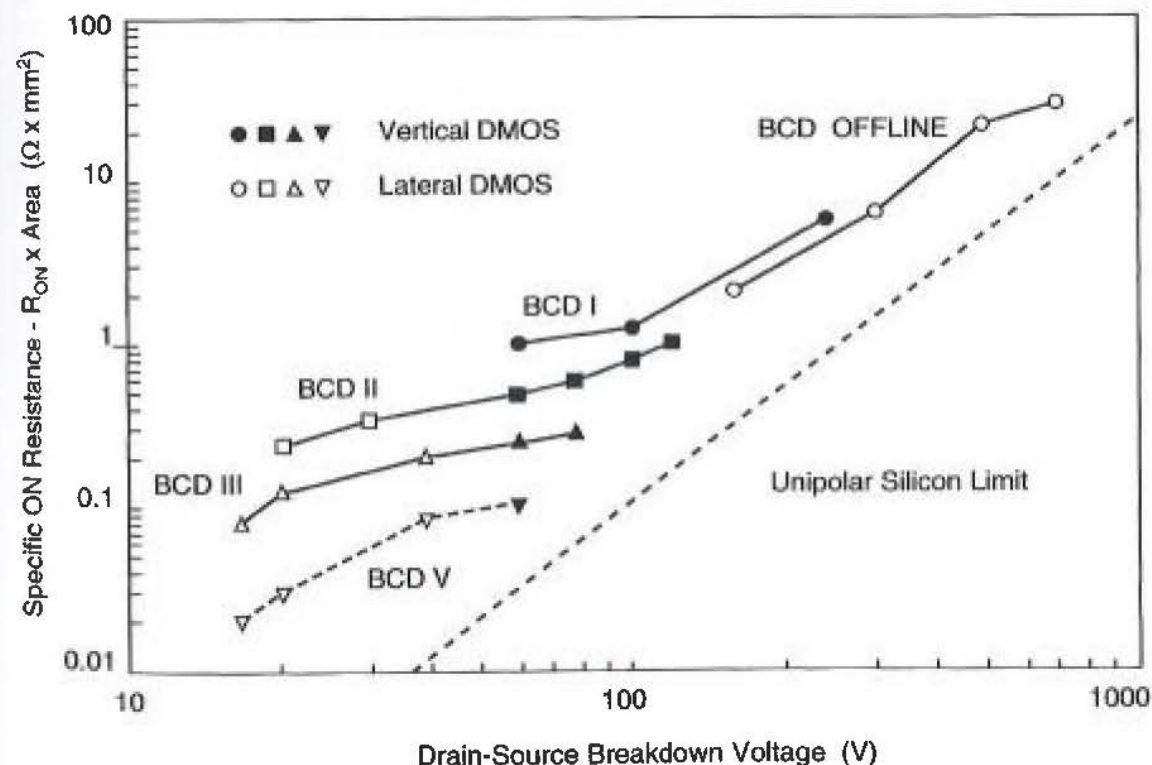


Fig. 1.38 Specific ON-resistance versus drain to source breakdown voltage for different BCD process generation

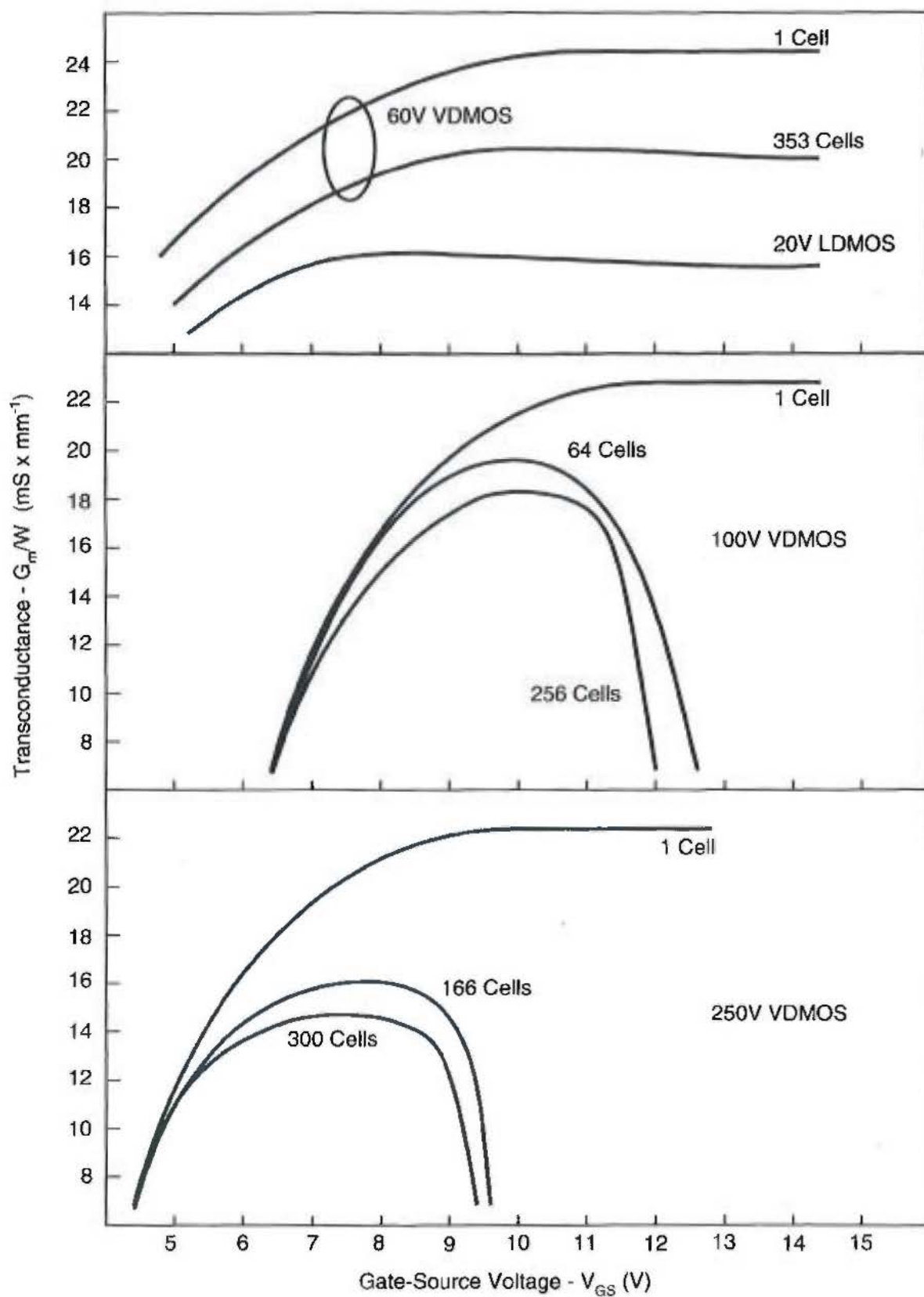


Fig. 1.39 Transconductance versus gate-to-source voltage for vertical and lateral DMOS in different voltage classes of BCD-I

1.6.4

Transconductance

The behaviour of transconductance versus gate-source voltage is reported in Fig. 1.39 for the Vertical DMOS transistor in three different processes.

The maximum transconductance value is limited by thermal effects while the quasi saturation effect explains the drop at high gate voltages. The quasi-saturation effect is caused by the carrier velocity saturation in the drift region between the P-body cells because of the high electric field, the low impurity concentration in the drift layer and the narrow cell spacing that acts as a channel of a parasitic JFET [43].

In the lateral DMOS device the quasi-saturation effect is not present because the alternated drain and source layout avoids the JFET formation and the transconductance is only temperature limited (Fig. 1.39).

1.7

Other Integrable Devices

1.7.1

High Voltage P-channel MOS (H.V. PMOS) Transistor

To satisfy the driving requirements of the high voltage DMOS device when used in high-side driver configuration, it is necessary to have a component of inverse polarity sustaining a supply voltage exceeding the DMOS maximum voltage by a value equal to its driving voltage.

The high voltage capability is achieved by an extended drain lateral structure realized by a properly doped region that allows the depletion region to spread mainly into the lightly doped drain instead of into the channel region. The drain extension also gives less Early effect. Its extension length and doping level control the maximum electric field at the drain but, at the same time, introduce a series resistance into the device.

This layer is obtained by a specific Boron implant step, in the first generation BCD processes (Fig. 1.40), while from the second generation onwards, the P-field

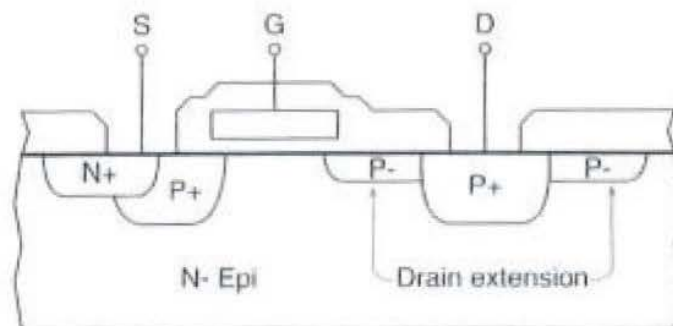


Fig. 1.40 High Voltage P-channel MOS transistor cross-section in BCD-I

layer used in the CMOS structure to increase the parasitic threshold voltage value, has such a doping level as not to require a specific processing step to get the drain extension function (Fig. 1.22 b).

1.7.2

Bipolar Transistors

To obtain bipolar transistors no extra doping layers are required because the elements used to realize CMOS and DMOS structures can be combined in different ways to build up lateral PNPs with different base width and two kinds of NPN structures.

The electrical characteristics of the lateral PNP transistors are connected to the epitaxial layer resistivity and to the spacing between emitter and collector.

In BCD-I, the emitter and collector regions are realized simultaneously with the highly doped P layer used as body contact in the DMOS cells (Fig. 1.41 a). In BCD-II and BCD-III the LOCOS field oxide scheme and the shallower P⁺ junction depth, force to introduce into the collector region both the P-body and the P-well layers that, having higher junction depths, improve the efficiency in collecting the holes injected by the emitter (Fig. 1.41 b).

The BV_{CEO} capability is related to the base width and to the collector construction.

When full voltage capability is needed, the same technique used in the high voltage P-channel MOS transistor can be implemented to increase the base to collector breakdown voltage.

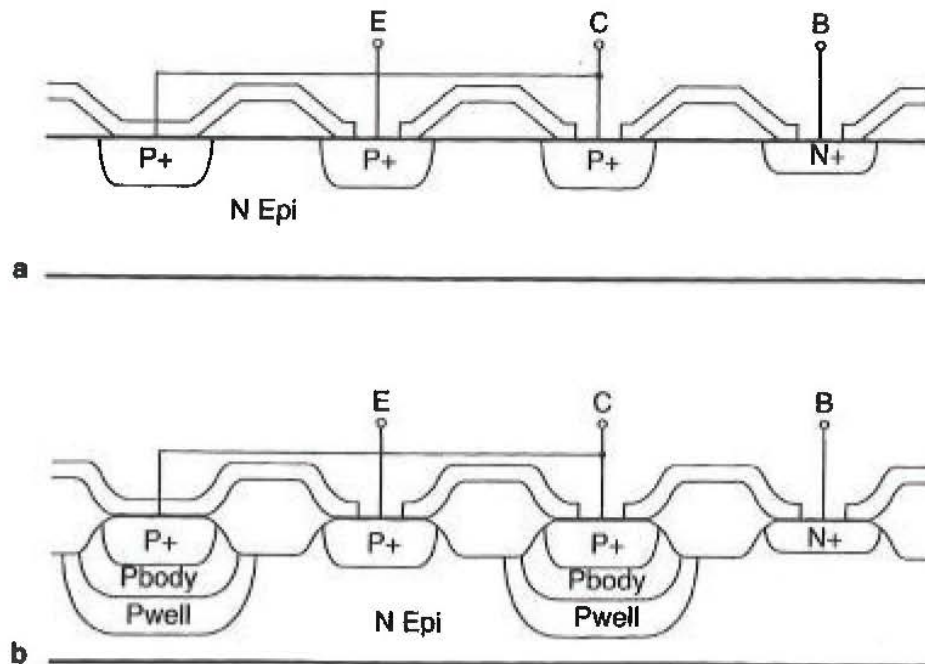
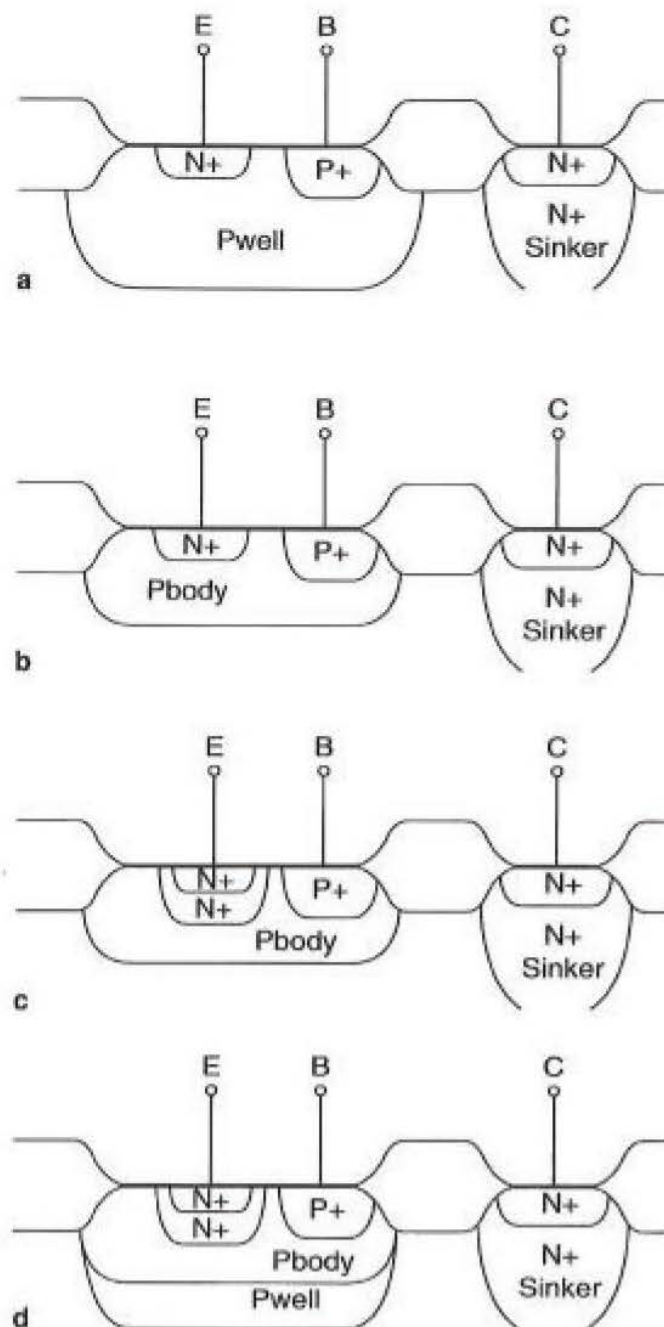


Fig. 1.41 Cross-section of the Lateral PNP transistor: a BCD-I; b BCD-II and BCD-III

Fig. 1.42 Cross-section of different types of NPN transistors



A first kind of NPN transistor can be made up by using as a base the CMOS P-well layer and as an emitter the N^+ source/drain contact (Fig. 1.42a). Due to the low doping profile of the P-well layer, coupled with the shallow emitter, the component exhibits high gain, but, owing to the high base width, the cut-off frequency is low.

A second one replaces the P well as a base profile with the P-body layer of the DMOS transistor (Fig. 1.42b): in this case the gain is lower but very constant (over more than two decades of collector current) and the cut-off frequency is increased.

From BCD-III onwards, the introduction of the single-Poly EPROM and EEPROM allows to exploit the N^+ control gate as a high efficiency emitter. Because its junction depth is deeper than the N^+ source/drain contact, if the P-body layer is used as a base (Fig. 1.42 c), the BV_{CEO} is lower (> 16 V) but a cut-off frequency value higher than 1 GHz can be reached. When a higher BV_{CEO} is required, the same structure is embedded in a P-well region (Fig. 1.42 d), allowing to achieve 30 V.

While the BV_{CEO} values are fixed by the doping profiles involved in the process, the BV_{CBO} values can be increased to the maximum voltage capability of the process by protecting the base/collector junction with field plates.

To reduce the collector contribution to the saturation resistance a sinker plug is normally used in the collector region of all the NPN transistors.

1.7.3

CMOS

The CMOS part represents the structure that mostly benefits of the lithographic reduction in terms of density and speed, therefore the evolution of the BCD processes has been mainly driven by the increasing demand to integrate more and more complex CMOS circuits. In fact, while in BCD-I the CMOS is obtained just adding a P-well layer to the DMOS process, from BCD-II onwards the architecture of the processes is conceived to optimize CMOS features.

The main advantage in size reduction going from BCD-I to BCD-II comes from the introduction of the LOCOS field isolation and from the use of specific implants to realize PMOS source/drain regions. In BCD-I, in fact, P^+ rings surround each NMOS active areas to avoid P-well surface inversion performing the field isolation and the DMOS P-body layer is used to form source and drain for PMOS.

In both process generations the CMOS gate oxide and polysilicon gate electrode are common to the DMOS structure and the epitaxial layer is the PMOS body. Moreover, when matched threshold voltages are required, an optional Boron implant is added to the PMOS channel region.

In BCD-III a dedicated gate oxide and polysilicon layer are introduced together with a self-aligned twin-well structure. The minimum gate lengths are equal to $1.2\text{ }\mu\text{m}$ therefore to avoid limitation to the maximum operating voltage induced by punch-through and hot electron effects, a LDD (Lightly Doped Drain) solution is adopted on the NMOS device using spacers (Fig. 1.25 b).

In BCD-V the gate lengths are reduced to $0.8\text{ }\mu\text{m}$ and the LDD solution becomes necessary for the PMOS transistor, too.

As regards immunity to latch-up, the CMOS takes advantage of the presence of the low shunt resistance of the N^+ buried layer positioned under the whole CMOS structure and of the availability of the sinker plug to reduce the series resistance to the PMOS body contact.

In the circuit design it is useful to have not only 5 V CMOS but also higher operating voltage capabilities to directly interface different supplies and to drive the DMOS power stage. To satisfy these requirements drain extension solutions

Table 1.3 5 V CMOS characteristics in different BCD process generations

	L-gate (μm)		T_{oxgate} (nm)	V_{TH} (V)	K_{LIN} ($\mu\text{A}/\text{V}^2$)		CMOS density (tr./mm ²)
	NMOS	PMOS			NMOS	PMOS	
BCD-I	4.00	7.00	85	1.30	27	10	650
BCD-II	3.00	4.00	60	1.10	40	15	1600
BCD-III	1.20	1.20	28	0.90	60	21	4000
BCD-V	0.8	0.9	20	0.85	85	28	15000

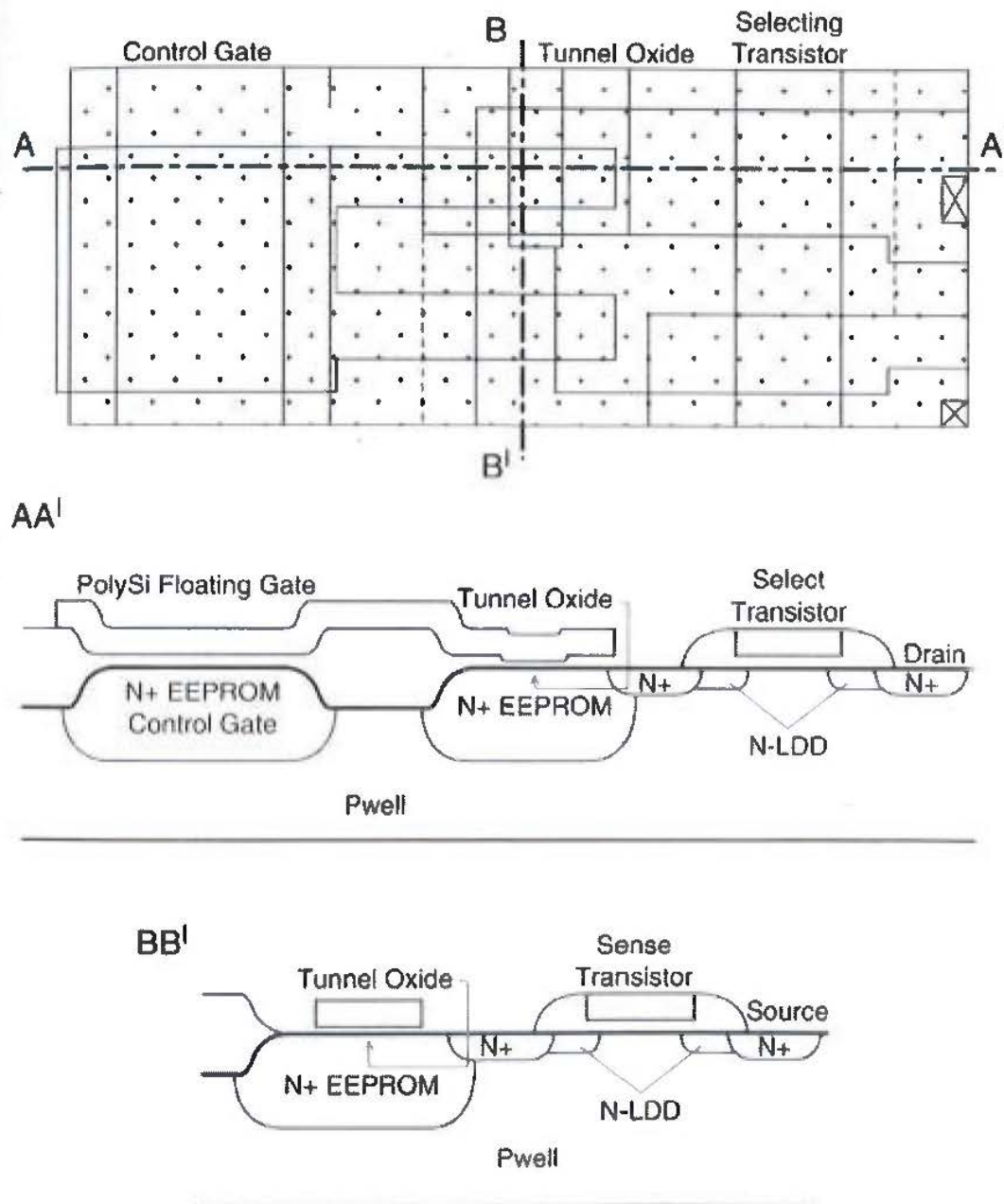


Fig. 1.43 Cross-section and layout of a single-poly EEPROM cell integrated in BCD-III

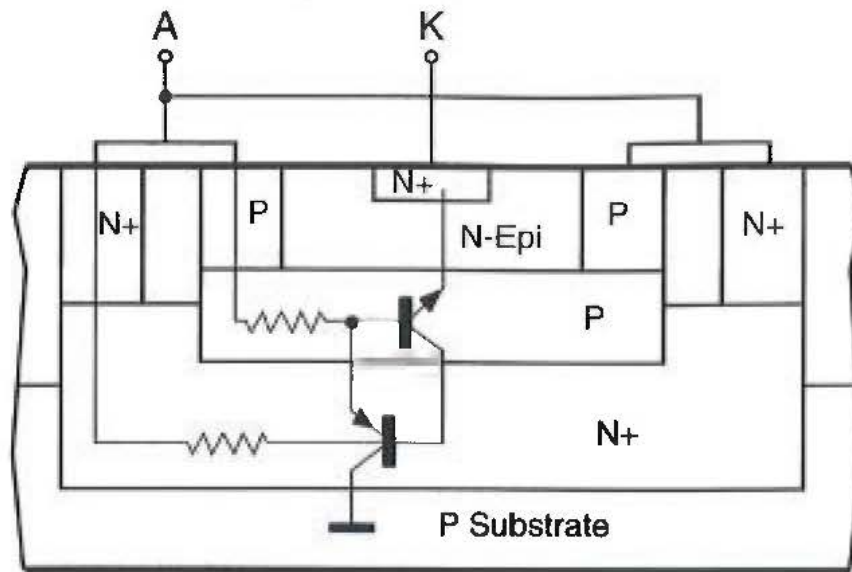


Fig. 1.45 Cross-section of the Low Leakage Diode (LLD) showing the associated parasitic substrate PNP and NPN transistors

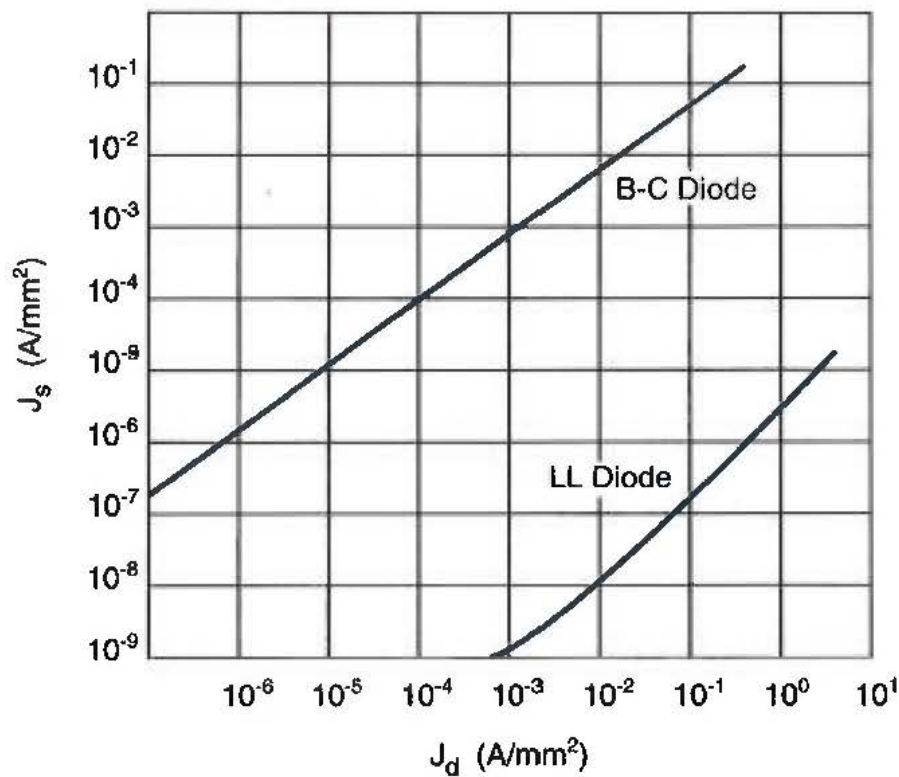


Fig. 1.46 Parasitic current density J_s injected into the substrate versus forward current density J_d in low leakage base/collector diode and in LLD

The simpler one is a NPN base/collector diode where the base is surrounded by a N^+ sinker ring short-circuited to a P ring acting as a lateral PNP extra collector (Fig. 1.44).

To further reduce the current loss, the emitter efficiency of the parasitic PNP is decreased adding the N^+ source/drain layer in the anode region [45].

In this kind of diode a current in the range of 1% of the diode current is injected into the substrate.

In the BCD processes that use an up-down junction-isolation approach, another kind of more efficient low leakage diode can be implemented [46].

In Fig. 1.45, the cross-section of this structure is shown together with the associated parasitic elements.

The buried anode is embedded in the N^+ buried layer and the deep anode contact is surrounded by a N^+ sinker ring. The deep anode and the N^+ sinker ring are short-circuited.

In this way, the base/emitter junction of the associated parasitic PNP can not be forward biased and the current loss into the substrate becomes negligible (Fig. 1.46).

The embedding of the anode in an N-type region isolates the diode from the substrate and makes it possible to use this component also tied to the high voltage rail.

1.8

Parasitic Structures

In a mixed process using the junction-isolation technique like Multipower-BCD, the large variety of different active components that can be integrated into the same chip cohabits also with parasitic structures of two species: surface and bulk.

1.8.1

Surface Parasitic Elements

The surface parasitic elements are MOS structures induced by polysilicon and metal interconnections, plastic packages or more in general by undesired external ionic contamination and by any charging effects due to high electric fields that, acting as parasitic gates, create surface inversion connecting two silicon regions of the same polarity.

In order to prevent surface inversion, channel stopper structures have to be inserted across the possible inversion path.

- At first, one way can be achieved by increasing the surface doping concentration in the channel region by inserting a heavily doped layer normally available in a mixed process (Fig. 1.47).

To be effective the channel stopper width and surface concentration must be properly dimensioned according to the required maximum voltage drop between silicon and parasitic gates.

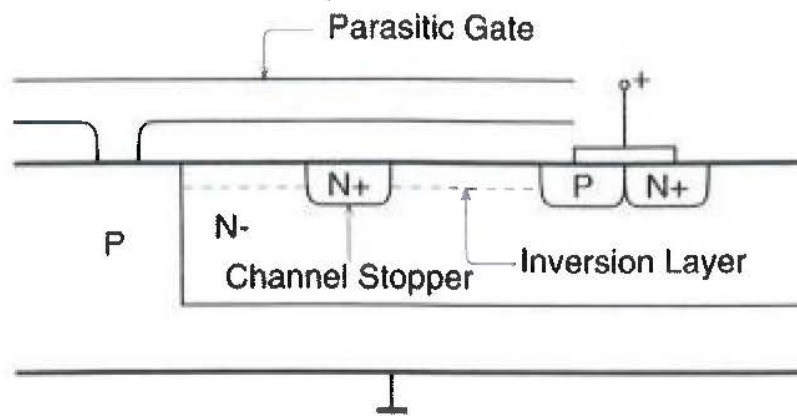


Fig. 1.47 Example of a possible inversion path stopped by a heavily doped region

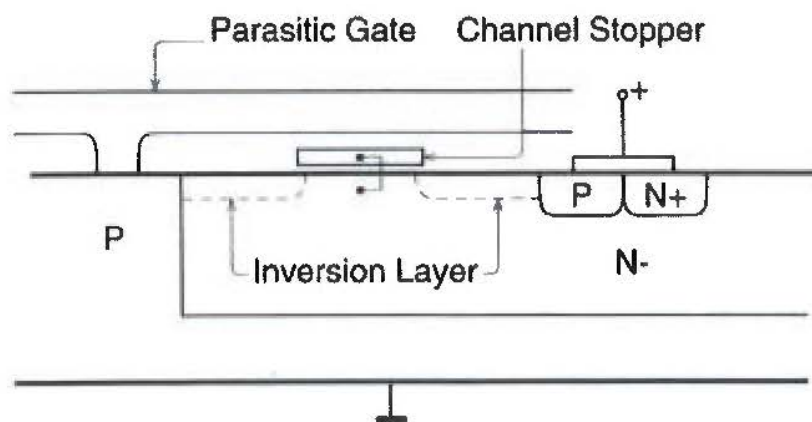


Fig. 1.48 Example of a possible inversion path stopped by a polysilicon electrostatic shield

- A second way of realization is to use polysilicon or metal interconnections as electrostatic shields tied to the same voltage of the silicon regions that have to be protected. In this case, the effectiveness depends on the channel stopper width that is also related to the underlying dielectric thickness (Fig. 1.48).

1.8.2

Bulk Parasitic Elements

The two main bulk parasitic elements are bipolar structures that can be activated in the following ways.

- When an epitaxial pocket bias is forced below the substrate potential, the base/emitter junction of a parasitic NPN is switched on (Fig. 1.49). Any other epitaxial pocket acts as a collector of this parasitic lateral device. This induces a higher power dissipation in the chip and can cause loss of driving control.
- When a P-type diffusion is biased above the supply level in an epitaxial pocket tied to the supply voltage, a parasitic vertical PNP transistor is turned on

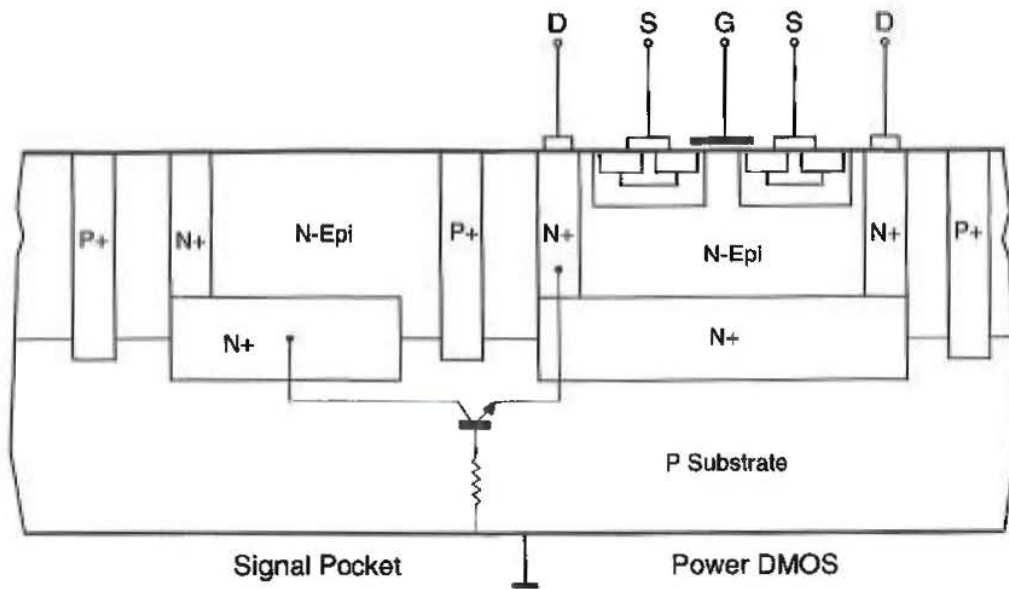


Fig. 1.49 Parasitic lateral NPN transistor between two epitaxial pockets

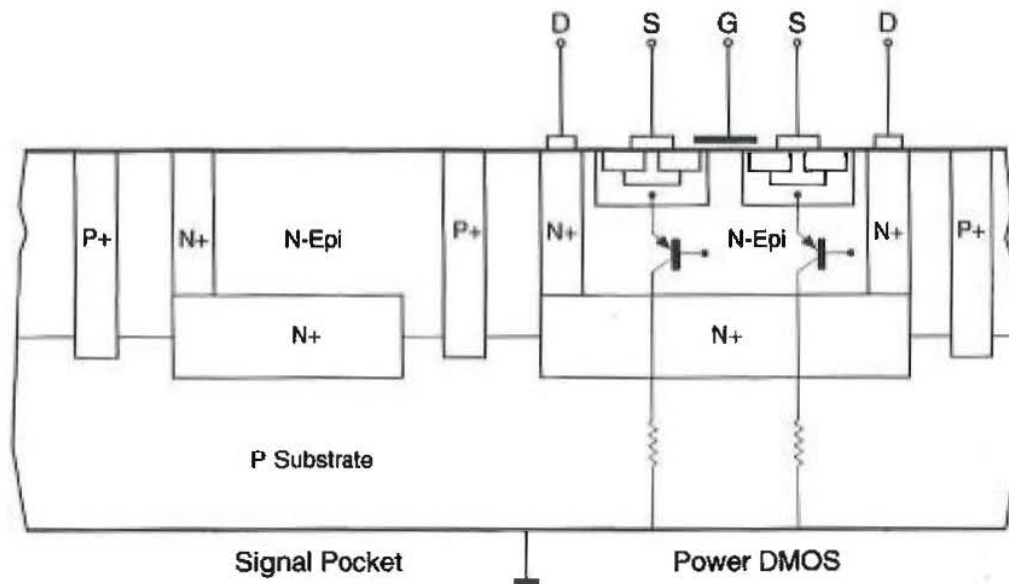


Fig. 1.50 Parasitic vertical PNP transistor

having the substrate acting as a collector. The PNP collector current increases locally the substrate potential; neighbouring epitaxial pockets that are biased to an equally or weakly positive potential compared to the substrate, act as emitters of parasitic lateral NPN transistors (Fig. 1.50).

The combined effect of parasitic lateral NPN and vertical PNP transistors builds up a SCR structure that can be regenerative and induces device burn-out.

In a junction-isolation approach the bulk parasitic elements cannot be completely suppressed and there are several techniques that limit their negative influence on the active components. These techniques mainly consist in the introduction of extra collectors for the parasitic lateral NPNs implemented via dummy epitaxial pockets, in the use of a diode (like the DMOS body/drain diode) in parallel to the epi/substrate junction, in order to sink part of the current flowing in the parasitic lateral NPN base/emitter junction, and in careful positioning of the critical components and of the substrate contacts in the IC layout.

Sometimes another approach to the problem is the reduction of substrate resistivity to limit the substrate voltage rise during parasitic PNP activation. However, low resistivity substrates enhance the parasitic NPN action via a reduced base resistance, therefore a careful choice of the substrate resistivity is often important in the control of the junction-isolation parasitics [47].

1.9

Electrostatic Discharge (ESD) Protection Structures

In the integrated circuits created with BCD processes, the large variety of possible applications, the multi-supply IC environment and the wide number of different basic components that can be integrated, require the adoption of unconventional ESD protection strategies and structures.

While the pure CMOS part can be protected via conventional ESD protection structures, like lateral NPN transistors or grounded gate field oxide MOS transistors [48–49], the mixed and high voltage parts of the ICs often require appropriate combination of the above structures to match the voltage requirements of the circuit or specific structures which may be realised as an active clamp implemented via a macro circuit. The active clamp is designed to provide a current path from the supply lines to ground, while all the pins that are related to those lines can be connected to the active clamp by plain diodes. An ESD network is therefore enforced which guarantees pin-to-pin protection against the ESD discharge.

This approach is very flexible as the active clamp can be designed with reference to the different existing ESD standards [50–53].

1.10

Future Perspectives

After more than ten years of evolution of BCD processes, a remarkable progress has been made in the increase of the voltage capability spectrum, of the variety of the integrable component arsenal and in the reduction of the lithography features. This progress has been pursued favouring the ability to provide flexibility in order to satisfy the wide range of Smart Power applications instead of running after the leading edge silicon technologies. This explains why BCD is now and will always be two or one generations behind BiCMOS and pure CMOS (Fig. 1.51).

Today the first products designed in BCD-III at $1.2\text{ }\mu\text{m}$ are going to be commercially introduced while the fifth generation designed at $0.6\text{ }\mu\text{m}$ is under

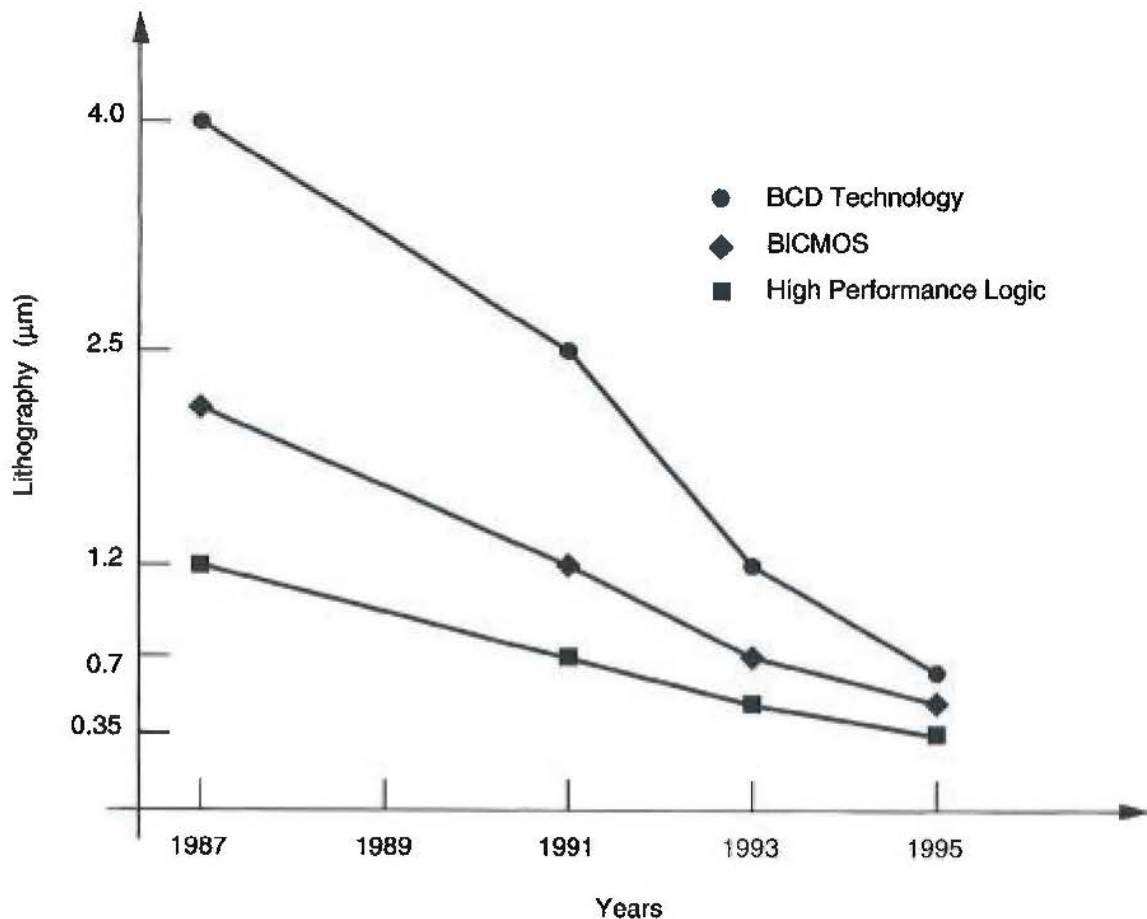


Fig. 1.51 Lithography trend in different process families

development. This last process version, which will include not only EEPROM but will also be compatible with Flash memory if asked by the market, will allow to integrate extremely complex systems on a single chip. A unique dedicated VLSI circuit will replace at a competitive price many systems realised today using a multi-chip approach.

In the near future, in the BCD development road map it will not be possible to ignore the Dielectric Isolation approach using SOI + trench. In fact, the integration of the active components in fully dielectrically isolated tubs will permit not only a further increase of the packing density, but also to suppress the bulk parasitics eliminating the interactions between the power stages and the more and more sophisticated and sensitive signal part.

Besides, an improvement in the frequency operation and a reduction in the current substrate leakage will be also achieved. Finally, it has to be mentioned that, together with the usage of the Dielectric Isolation approach, a worse thermal conductivity will have to be dealt with. To overcome the induced problems in power dissipation, new substrate materials with higher thermal conductivity will have to be developed.

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Packaging

C. Cagnetti · E. Kobayashi

13.1

Introduction

The most evident progress in electronics is *system miniaturization*. It took place in the early '80s, with the commercialization of very compact consumer sets; but since the last few years it is so common that new designs in almost all market segments have the same imperative: "Small, Light and Cheap". This is especially the case of portables, like PCs and phones.

Basically, miniaturization is obtained from the improvement of both semiconductor and Printed Circuit Board (PCB). As a consequence, reduction in the component count is achieved for the same function, with substantial improvement in miniaturization.

But this concept would have severe limitations without new PCB technologies.

Also PCB is in permanent progress toward higher density of interconnections in smaller volumes. This is recognized as major advantage offered by the Surface Mount Technology (SMT) which was born 15 years ago and is now arrived to maturity, with very fine line at 100 micron pitch and reliable, cost effective multilayers.

But, even if in so close relationship, semiconductor and PCB are also very different.

The need exists of some "bridge" between the sophisticated, fragile, submicron world of silicon and the robust, submillimeter world of printed board.

This "bridge" is the semiconductor package, assisted by a family of interconnection technologies.

In the last five years, package and interconnections merited as much effort as the silicon itself with the development of new structures, materials and processes in large number.

In order to quantify this progress, three parameters can be used as an example:

- 1) *the lead pitch*, which moved from 2.54 mm typical of Dual-in line packages (DIP) to 0.3 mm used at present in the most aggressive Plastic Quad Flat Packages (PQFP);
- 2) *the pin count*, which was not higher than 40–60 in DIPs and is now close to 500 in the Ball Grid Array (BGA) family;
- 3) *the efficiency of interconnection*, intended as ratio between the active chip and the package footprint which was below 1–2 % in DIPs and is now close to 50 % with memory packages like Thin Small Outline Packages (TSOP).

In this chapter, packaging for Smart Power ICs will be presented and discussed.

13.2

Concept of Smart Power IC Package

Smart Power IC is the integration of components capable of delivering a significant amount of power to a given load, with circuits providing several logic functions, like control, detection, sensing and diagnostics; it is used in applications (automotive, industrial, consumer, computer peripherals) very sensitive to cost and reliability.

The four main functions provided by Smart Power IC package are:

- 1) *electrical interconnection* between the silicon and the external circuit (PCB), by means of a *large number of leads* (up to 100) requested by the complexity of the "Smart" section of the chip;
- 2) *mechanical and chemical protection*, for very low failure rate which in automotive systems will be fractions of ppm;
- 3) *device cooling*, by means of thermally conductive elements (slug) able to transfer the heat generated in operation (1–40 W) from the silicon directly to the ambient or to external heatsinks;
- 4) *electrical isolation*, (up to 4000 V) especially in case of technologies based on vertical power MOS transistors. As the transistor drain is connected to package slug, the need exists of using isolated packages for cost and safety reasons.

Driving forces and design criteria of Smart Power IC packages are summarized in Table 13.1.

13.3

Smart Power IC Package Types

Packages for Smart Power IC's can be classified according to the level of power dissipation.

Table 13.1 Driving forces and design criteria of Smart Power ICs Packages

Driving force	Design criteria
Power dissipation (1–40 W)	Power enhanced structure
Logic functions	Large pin count (5–100)
Low cost (< 0.01 US \$/pin)	Plastic self isolation (2500–4000 V)
Low failure rate (< 1 ppm)	Material selection

Two families are commonly considered:

- a) medium power packages, up to about 2 W;
- b) high power packages, for more than 2 W up to 30–40 W.

13.3.1

Medium Power Packages

A simple way to achieve power dissipation up to 2 W is to transform the available signal packages and modify their leadframe in order to have high thermal conduction patterns from the silicon to the printed board.

This solution is used for all of the most common package types (Fig. 13.1):

- a) for Through Hole Technology (THT) in DIP, with pin count up to 28;
- b) for Surface Mount Technology (SMT) in SOP with pin count up to 28; in PLCC (Plastic Leaded Chip Carrier) for pin count up to 44–68; for PQFP (Plastic Quad Flat Package) for pin count up to 80–100.

Modification involves a number of lead (heat transfer leads) which are connected to the die pad in order to minimize the junction to pin thermal resistance θ_{jp} and to improve the thermal exchange from chip to substrate.

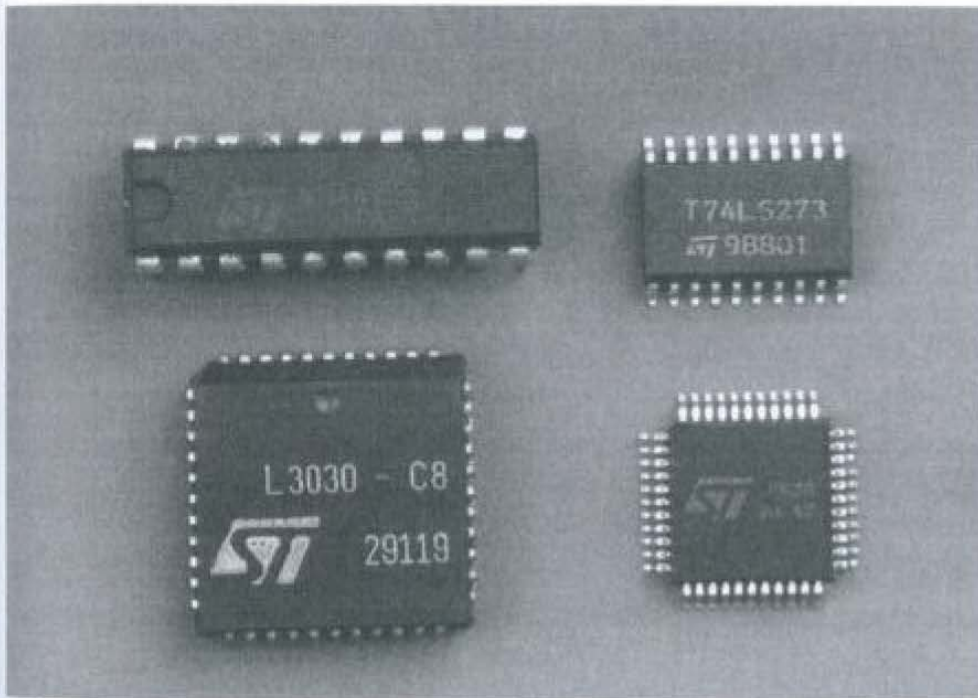


Fig. 13.1 Plastic packages of different generations: Dual In Line (DIP), Small Outline (SOP), Plastic Leaded Chip Carrier (PLCC) and Plastic Quad Flat Pack (PQFP)

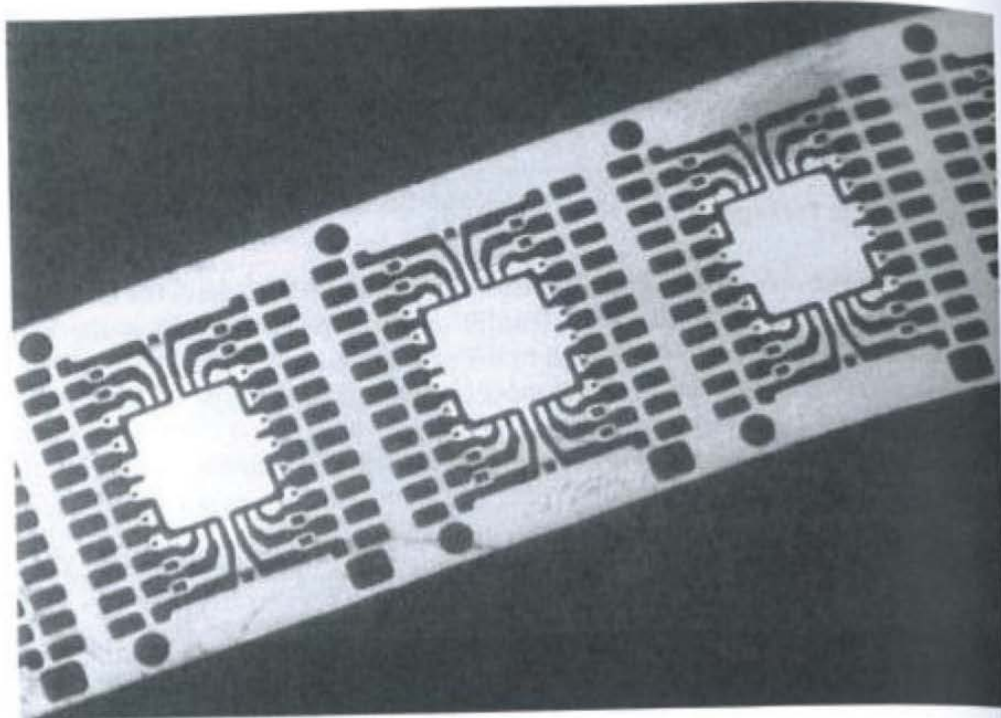


Fig. 13.2 Leadframe of medium power SOP, with heat transfer leads connected to die-pad

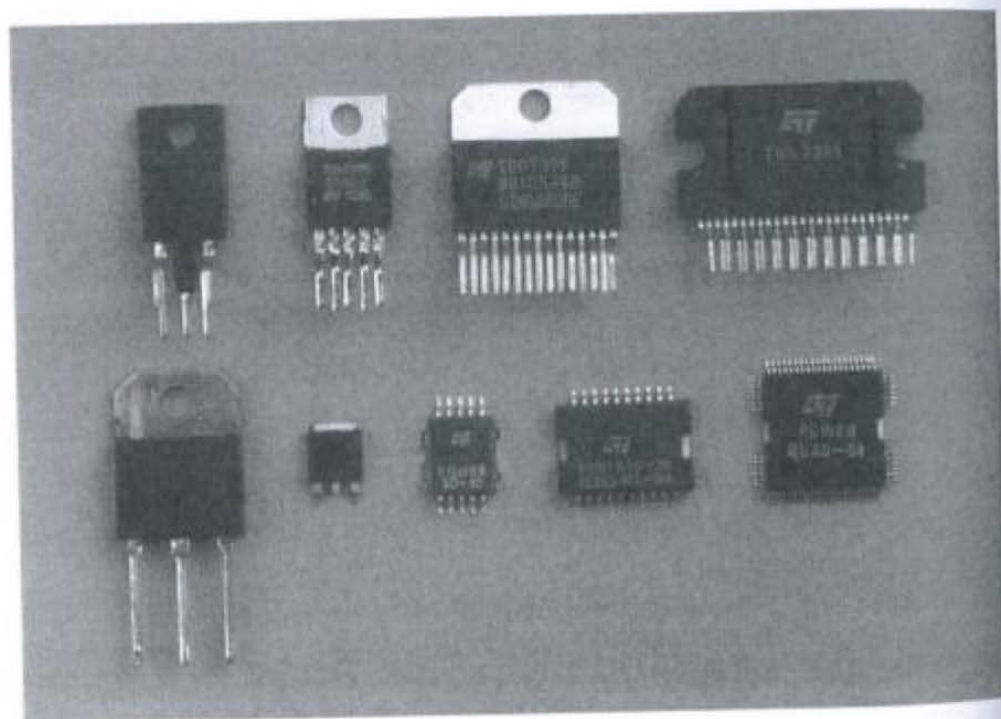


Fig. 13.3 Evolution of plastic power packages, from insertion to surface mount

As the external dimensions of the package are not changed, the undoubted advantage is obtained of being compatible with existing handling and testing tools.

Modified leadframes are shown in Fig. 13.2. Due to the particular shape of their lead frames, medium power packages are called "batwing" or "crab" packages.

13.3.2

High Power Packages

For thermal dissipation higher than 2 W, external heatsinks are used, whose dimension is chosen according to the dissipated power. In order to have efficient heat transfer from the silicon to the heatsink, massive copper slugs are integrated in the body of high power packages.

Evolution of this family is shown in the roadmap of Fig. 13.3, where three main subgroups can be identified:

- a) insertion packages
- b) isolated packages
- c) surface mount packages

13.3.2.1

Insertion High Power Packages

The group is originated from the two most widely used power packages, both with 3 leads: the TO-220 and the SOT-93 (TO-218), shown in Fig. 13.4.

The main difference between these two packages is the size, hence the size of die which they can accommodate. This also defines maximum operating current and power dissipation capability. Their characteristics are summarized in Table 13.2. (see section 12 for definition of θ_{jc} junction to case thermal resistance).

These packages are inserted in THT boards and secured to the external heat-sink using screws through the fixing hole existing in the upper portion of the slug. In recent years substitution of screws with clips has become more common for cost reasons.

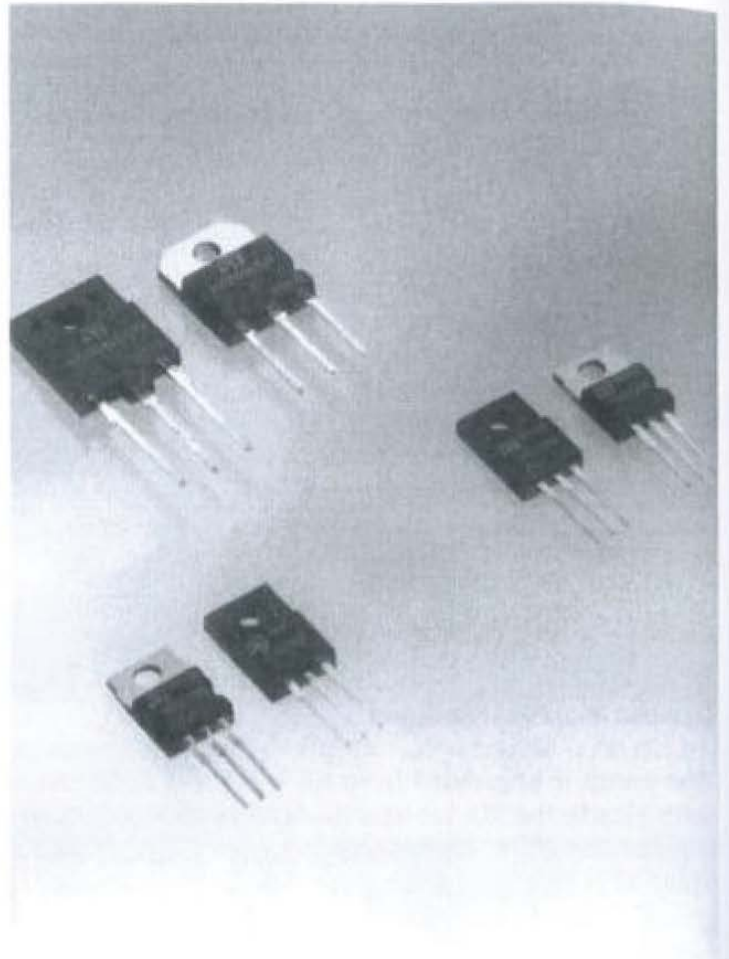
For more than 3 leads, a number of packages have been derived from TO-220 and SOT 93 structure (Fig. 13. 5).

with 5 leads:	Pentawatt, PentaSOT
with 7 leads:	Heptawatt, HeptaSOT
with 8, 11, 15 leads:	Multiwatt
with 15, 21, 25, 27 leads:	Flexiwatt

Table 13.2 Characteristics of TO-220 and SOT-93 (TO-218)

	Max die Size (mm ²)	Max Current (A)	θ_{jc} (C/W)
TO-220	25.50	60.00	0.5–1.5
SOT-93 (TO-218)	54.00	80.00	0.3–0.7

Fig. 13.4 Plastic power packages for discretes: TO-220 and SOT-93 with their isolated versions



13.3.2.2

Isolated Packages

In many applications a number of devices are secured to one single heatsink. If package slug is connected to the drain of a vertical MOS transistor each individual package must be isolated from the heatsink.

This can be achieved by placing a thin sheet of mica or adhesive mylar between slug and heatsink. This solution is relatively expensive, due to the manual assembly of the isolation layer and is not very consistent for what refers the thermal performance.

In order to minimize above problems, isolation can be conveniently obtained during the molding process, if a thin layer of molding compound is formed on the external surface of the slug. The solution is very competitive, especially if high thermal conductivity compounds are used (Table 13.3).

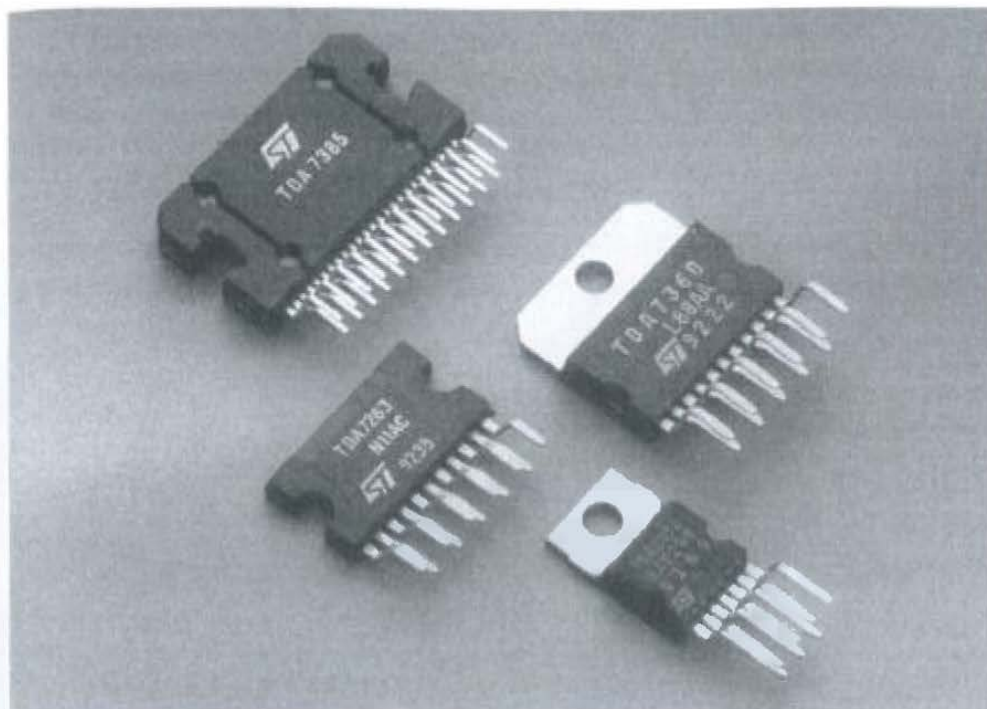


Fig. 13.5 Power insertion plastic packages for integrated circuits

Table 13.3 Comparison of isolation methods (with equivalent die size and dissipated power)

Package	Isolation	θ_{JC} (C/W)
TO-220	None	1.3
TO-220	100 micron mica	3.3
TO-220	Mylar	4.4
Isowatt-220	None	3.0
Isowatt-218	None	2.1

The isolated version of TO-220 and SOT-93 (TO-218) are called ISOWATT-220 and ISOWATT-218 respectively. Both exist with 3, 5, 7 leads.

ISOWATT-221 is the high voltage version of ISOWATT-220.

ISOWATT packages are shown in Fig. 13.4

13.3.2.3

Surface Mount Power Packages

Very recently, the extension of surface mount technology to power applications, requested the development of new package structures, which can associate miniaturization with good thermal characteristics.

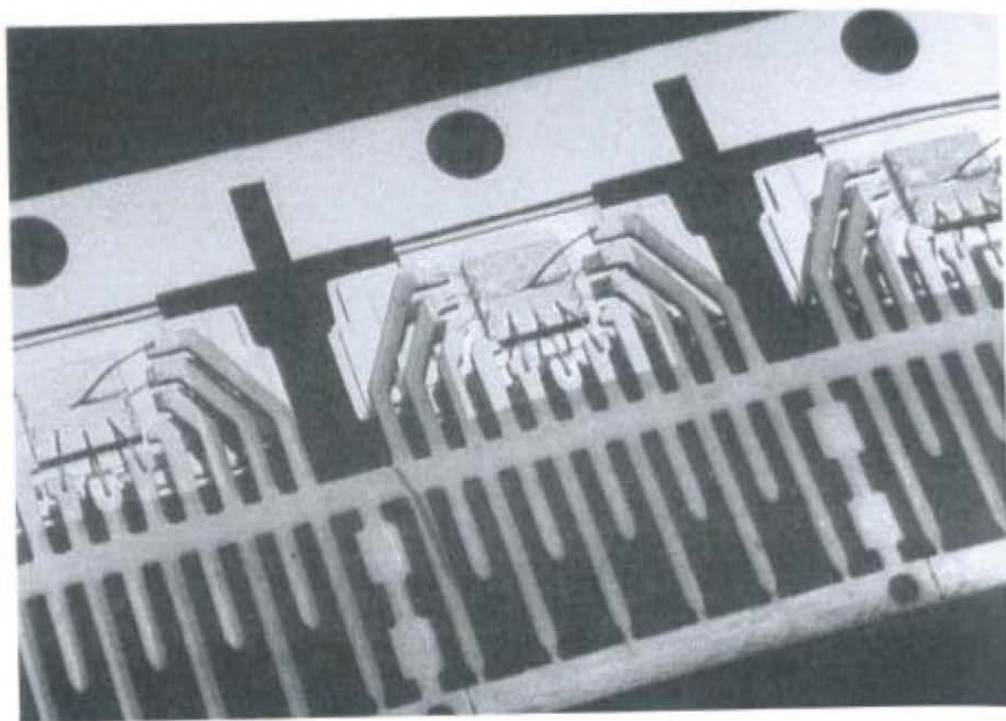


Fig. 13.6 Mixed wire interconnection for high current IC

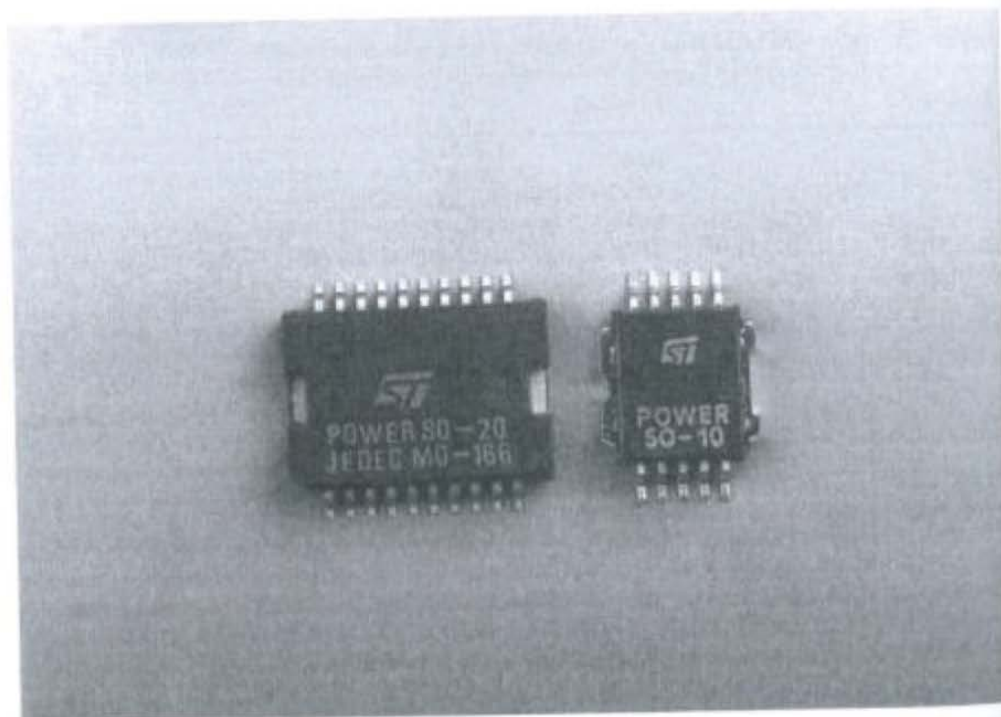


Fig. 13.7 Recently developed power surface mount IC packages: Power SO-10 (MO-184) and Power SO-20 (MO-166)

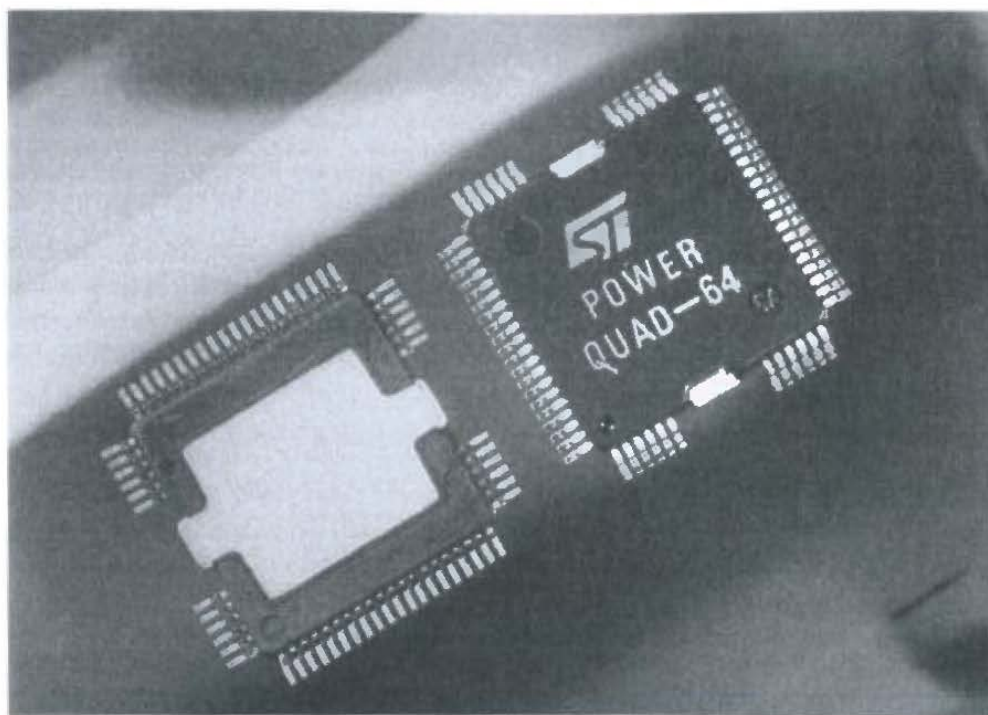


Fig. 13.8 Surface mount Power Quad, for Smart Power IC up to 64 I/O

Table 13.4 Smart Power IC Package Types

	Medium power < 2 W	High power 2–40 W	Isolated
Insertion	Dip	TO-220	Isowatt-220
		SOT-94	Isowatt-221
		Pentawatt PW	Isowatt-218
		Heptawatt HW	
		Multiwatt MW	
		Flexiwatt FW	
Surface Mounting	SO	PowerSO	
	PLCC	PowerQUAD	
	PQFP		

They are ideal packages for Smart Power Technology of last generation, whose complexity needs a relatively high pin count, up to 80–100.

They are purpose designed packages having leads on two sides – like PowerSO-10 and PowerSO-20 (see Fig. 13.7) or on 4 sides – like PowerQUAD – (see Fig. 13.8).

They are used directly on laminate boards, on high conductivity Isolated Metal Substrates (IMS), and in contact with external heatsinks, for dissipation ranking between 2 and 20 W.

Package types described in this paragraph are summarized in Table 13.4.

13.4 Thermal Management

13.4.1 Thermal Resistance

Thermal resistance is the physical quantity which indicates how “easily” the heat flows between two points A and B. If thermal resistance is small, heat is transferred from A to B with little temperature difference between A and B. If thermal resistance is large, transfer of the same quantity of heat requires a much higher temperature difference in the two points.

Thermal resistance is defined as:

$$\theta_{AB} = \frac{\Delta T_{AB}}{P}$$

(Note: θ is often written as R_{th})

where P is the power, or the rate of flow of heat between the two points, while ΔT_{AB} is the temperature difference between the two points.

In electronic devices, the two most important temperatures are the ambient temperature T_a and the temperature T_j reached by the junction when a given thermal power P_d is generated in the silicon.

Thermal resistance junction to ambient θ_{ja} is the ratio between junction temperature increase and dissipated power:

$$\theta_{ja} = \frac{T_j - T_a}{P_d} \quad (13.1)$$

θ_{ja} depends upon a number of factors, including size of the device, thermal conductivity of the materials, size and shape of the heatsink.

Device failure rate is affected by the junction temperature and about doubles for every 10 °C increase of T_j .

The main aim of thermal design is to keep the junction temperature within defined limits, which is usually lower than 150–170 °C for discretes, and 125–150 °C for ICs. At the same time, systems are increasingly being used in ambient temperatures up to 125 °C, for example in “under the hood” car electronics. In this case, $T_j - T_a$ can be as low as 20–25 °C. This causes particular problems where large amounts of power (10–20 W) are to be dissipated and θ_{ja} must be limited to a few C/Watt.

θ_{ja} is controlled by placing a suitably sized heatsink in contact with the power package slug. From a physical viewpoint, a thermal chain exists from the silicon to the ambient through the die attach, the slug, the interface between the slug and the external dissipator and finally the dissipator itself (see Fig. 13.9)

This can be represented as follows:

$$\theta_{ja} = \theta_{jc} + \theta_c + \theta_s \quad (13.2)$$

where θ_{jc} is the thermal resistance from the junction to the case, defined by the conduction properties of the device from the junction to the portion of the case

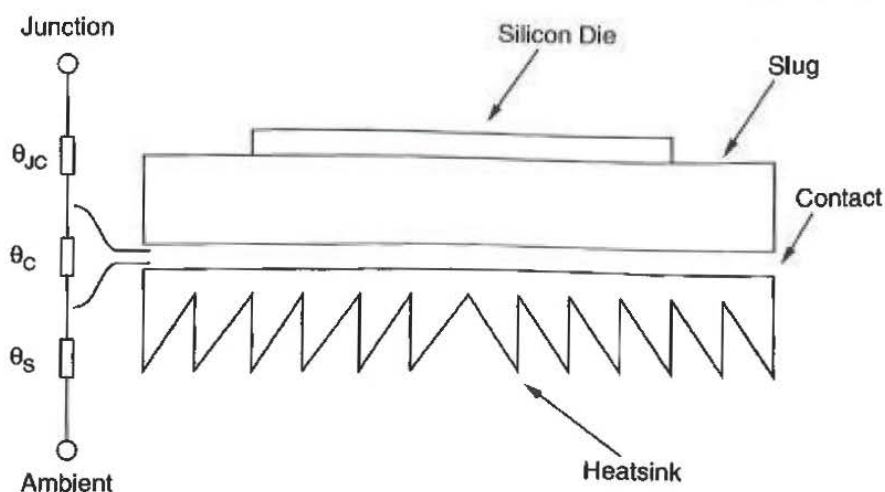


Fig. 13.9 Thermal chain from silicon to external heatsink

where the heatsink is applied; θ_c is a parasitic element describing the loss at the contact between package and heatsink; θ_s is the thermal resistance of the external sink, which indicates its efficiency in dissipating heat through convection and radiation.

13.4.2

Thermal Resistance and Heat Transfer Mechanisms

The flow of heat from the silicon to the ambient is ruled by three important mechanisms: conduction, convection and radiation.

13.4.2.1

Thermal Conduction and θ_{jc}

Conduction is the heat transfer mechanism due to thermal excitation at molecular level, by direct contact. No motion of material is associated to this mechanism. Thermal resistance depends on the thermal conductivity c of the material and its dimensions: length L and cross sectional area A according to the relationship:

$$\theta = \frac{1}{c} \frac{L}{A} \quad (13.3)$$

Equation 13.3 can be applied to the J-C pattern as shown in Fig. 13.10.

In this simple model, the heat generated at the junction flows in a 45° cone through the silicon, the die attach alloy and the copper slug up to its external surface. Table 13.5 shows the thermal conductivity of some materials commonly used in microelectronics.

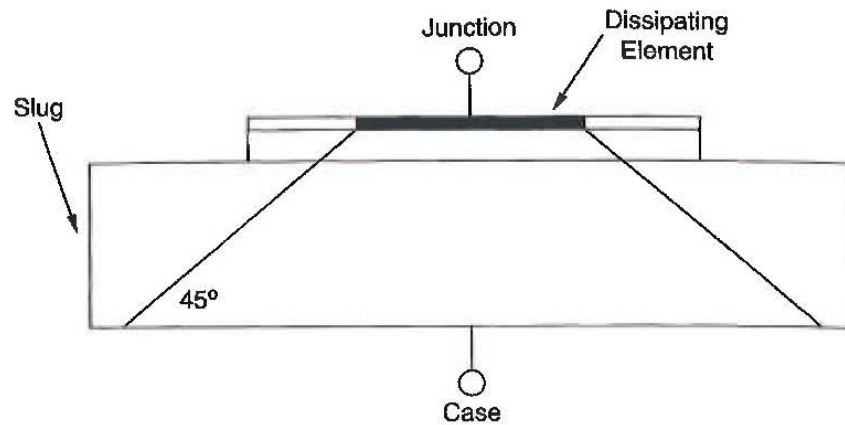


Fig. 13.10 Thermal dissipation pattern in power IC package

Table 13.5 Thermal conductivity of materials commonly used in packaging

Material	Thermal conductivity ($\text{Wm}^{-1} \text{K}^{-1}$)
Copper	390.00
Silicon	150.00
Glass (Silicon Oxide, SiO_2)	0.60
Silicon Carbide (SiC)	85.00
Aluminium	210.00
Aluminium Nitride (AlN)	150.00
Aluminium Oxide (Al_2O_3)	30.00
Resin (Standard packages)	0.71
Resin (Isolated packages)	2.51
Mica	0.50
Air	0.03

The following points should be noted:

- θ_{jc} is mainly affected by the chip size and by the size of power element(s) in the chip. The theoretical relationship is given in Fig. 13.11 [1].
- The thermal conductivity of silicon increases with an increase of temperature. In the temperature range considered in microelectronics a variation of 20–30% is common.
- The dimensions of the slug are important. In principle, a thinner slug should provide a lower resistance (as there will be a shorter conducting path); in practice, due to the existence of parasitic effects at the contact with the external heatsink (uneven surface, air, dust, etc.) a thicker and larger slug performs better: indeed it can spread the heat much more than the 45° considered in Fig. 13.10 and reduce the losses at the contact because of the larger area of contact.

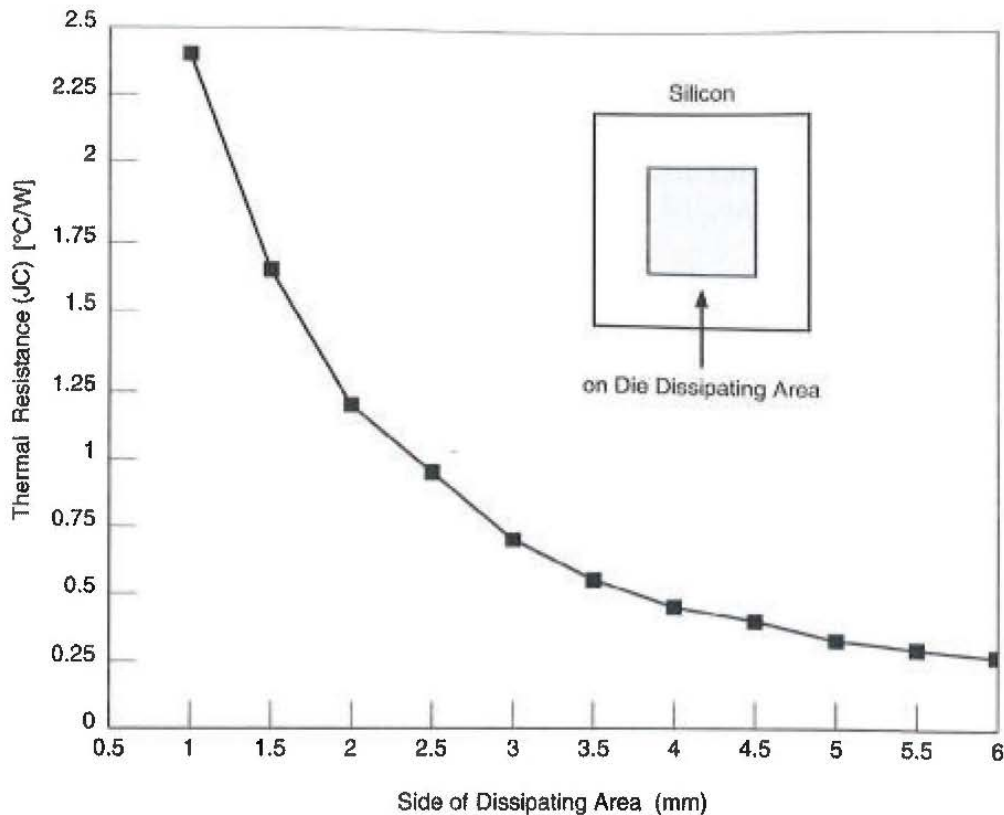


Fig. 13.11 Typical Junction to Case thermal resistance in power IC package (Multiwatt)

13.4.2.2

Convection, Radiation and θ_{ja}

Thermal Convection

Convection is the transfer of heat associated with the movement of material in a fluid (liquid or gas). It is due to the heating of the fluid in contact with the source, which moves and is replaced by cooler fluid upward. The process is ruled by the heat-transfer coefficient h depending on the source temperature T_s and the ambient temperature T_a .

The quantity of heat removed by convection is given by the relationship:

$$Q = h(T_s, T_a) \cdot A \cdot (T_s - T_a) \quad (13.4)$$

where A is the area of the heat exchange surface. In case of forced cooling, h is a function of the speed of the cooling fluid and is always higher than 1 in Eq. 13.4. The following considerations are important:

- the size of the heatsink has the greatest effect on the final performance of the cooling systems. As the exchange surface dominates in Eq. 13.4 it is common to increase it with the use of fins and grooves. However, this solution is most effective in forced cooling.

- b) The higher the source temperature, the stronger the convection effect. This can compensate for the negative effect of the temperature on the θ_{jc} considered in the previous paragraph, and the final result is a θ_{ja} which decreases by increasing power dissipation.
- c) The thickness of the heatsink is important, in order to spread the heat in the sink by conduction, and to have a larger exchange surface.

Thermal Radiation

The transport of electromagnetic energy is associated with radiation, which involves a transmitting surface at temperature T_s and a receiving ambient at temperature T_a .

The heat Q exchanged by radiation from a surface area S is:

$$Q = \sigma \cdot \alpha \cdot S \cdot (T_s^4 - T_a^4) \quad (13.5)$$

where σ is the Stefan-Boltzmann constant and α is the emissivity of the material, which varies between 0 and 1.

Black surfaces have emissivity close to 1, indicating the maximum radiation energy theoretically possible at T_s . Polished, white metals (like aluminium) have the lowest emissivity, between 0.1 and 0.3.

Due to the 4th power relationship with the temperature, radiation dominates only when T_s is much larger than T_a (in absolute units). This is generally not the case for applications in electronics; however the effect of radiation cannot be ignored.

As an example of values associated with convection and radiation, if a 1 mm · 10 cm · 10 cm red (natural oxide) copper sheet is used as a heat-sink positioned vertically at a T_s of 100°C, the thermal resistances due to both radiation and convection are around 7°C/W, giving an overall value of 3.5°C/W.

13.4.2.3

Contact Thermal Resistance θ_c

Power packages are secured to the heatsink using screws, bolts or rivets fixed through the hole in the upper part of the copper tab (Fig. 13.12a). In order to reduce the cost of mounting, the use of clips is becoming more common, with the pressure applied to the top of the plastic body, at the centre (Fig. 13.12b).

The contact thermal resistance θ_c can be minimized by adding a thin layer of silicone grease, uniformly distributed between slug and dissipator and applying an appropriate force.

In case of screw mounting, this force can be controlled by choosing the torque (in kg · cm) applied to the fixing screw, by means of a dynamometric screwdriver.

Experimental value of θ_c are shown in Table 13.6 with different torque levels, for both conditions, with and without grease.

In practical cases, the recommended value of torque is 6–8 Kg · cm.

Fig. 13.12 Methods for mounting power packages onto massive external heatsink: screw and clip

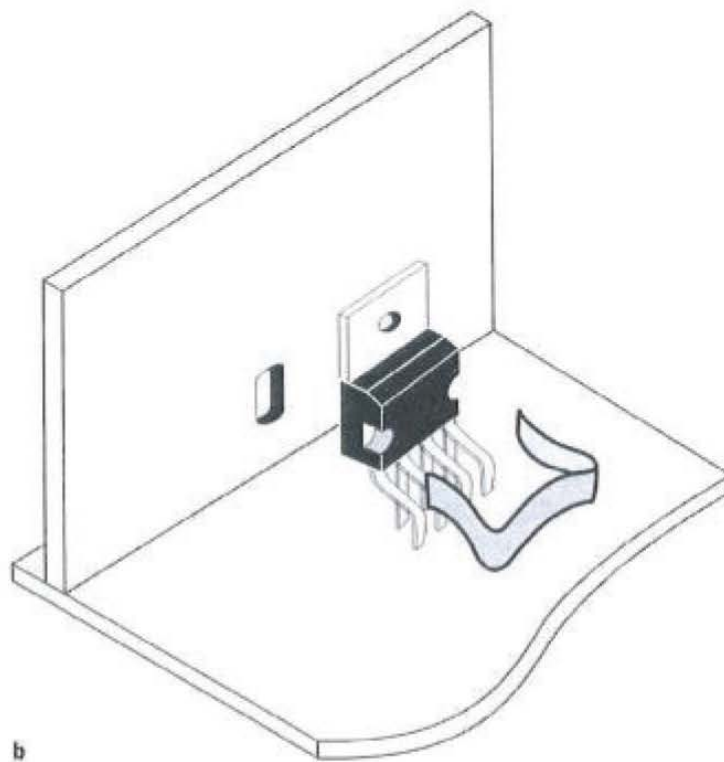
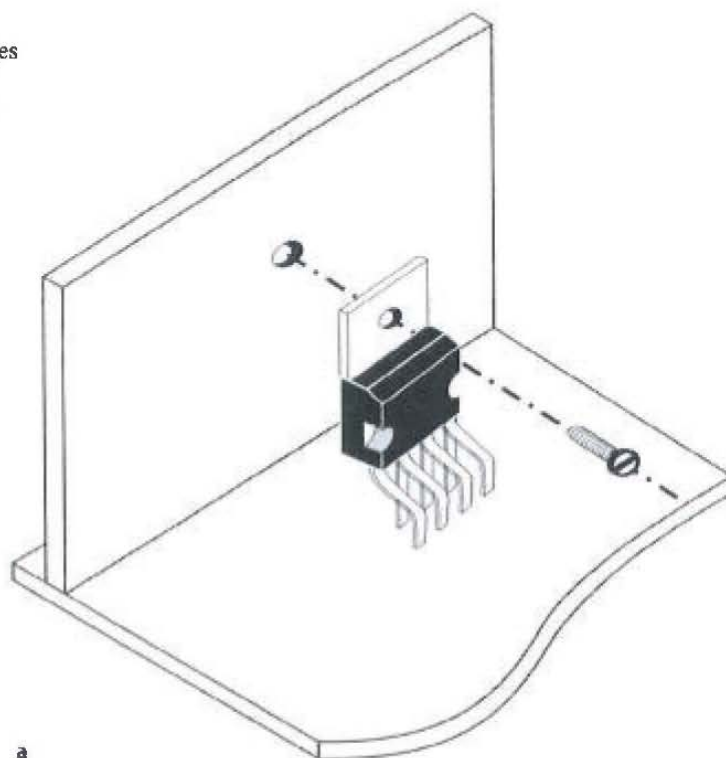


Table 13.6 Contact thermal resistance for TO-220 package (experimental data)

Torque kg · cm	θ_c with grease °C/W	θ_c without grease °C/W
3.00	0.27	0.90
4.00	0.22	0.82
5.00	0.17	0.78
7.00	0.12	0.75
10–15	< 0.1	< 0.7

When a spring clip is used, θ_c is also decreased if the force F of the clip is higher; a minimum of 5 kg is recommended.

13.4.3

Thermal Impedance

In section 13.4.1, thermal exchange was studied in steady state conditions, that is once the system had reached thermal equilibrium. However, in many situations the power dissipation of the system is not uniform, for example when the device operates in pulsed conditions. In this situation thermal capacitance of the system must be taken into account [2].

Thermal capacitance exists because the elements in the heat transfer path take a finite amount of time to heat up or “charge” to their equilibrium temperature. In practice this has beneficial effects: if excessively high dissipation peaks occur, it is possible that the maximum junction temperature will not be exceeded, provided that the pulse is not too long, just as an electrical capacitor will prevent voltages exceeding certain limits in the presence of current spikes.

An important parameter is the thermal capacitance C_{th} associated with the various structural elements of the thermal chain from the junction to the ambient. This parameter can be expressed as:

$$C_{th} = c \cdot d \cdot V \quad (13.6)$$

where c is the specific heat, d is the density and V is the volume of the material.

In a simple model, the above elements are the silicon, the slug and the external heat sink. They can be modeled as RC cells, as shown in Fig. 13.13.

The first cell represents the thermal behaviour of the silicon with a small volume and a correspondingly low thermal capacitance (a few mJ/°C). The thermal resistance between the junction and the silicon/slug interface is about 0.2–2 °C/W depending on the die size and on the size of the dissipating element on the chip. The time constant τ ($= RC$) of this first cell is typically in the order of few milliseconds.

The second cell represents the copper slug, with a relatively large thermal capacitance and a time constant of a few seconds.

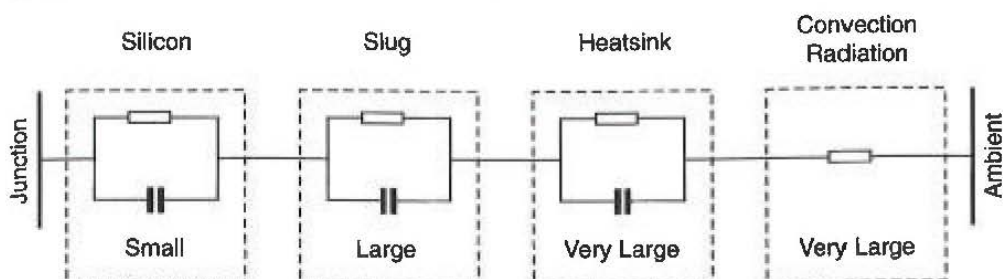


Fig. 13.13 RC equivalent of the thermal chain from junction to ambient

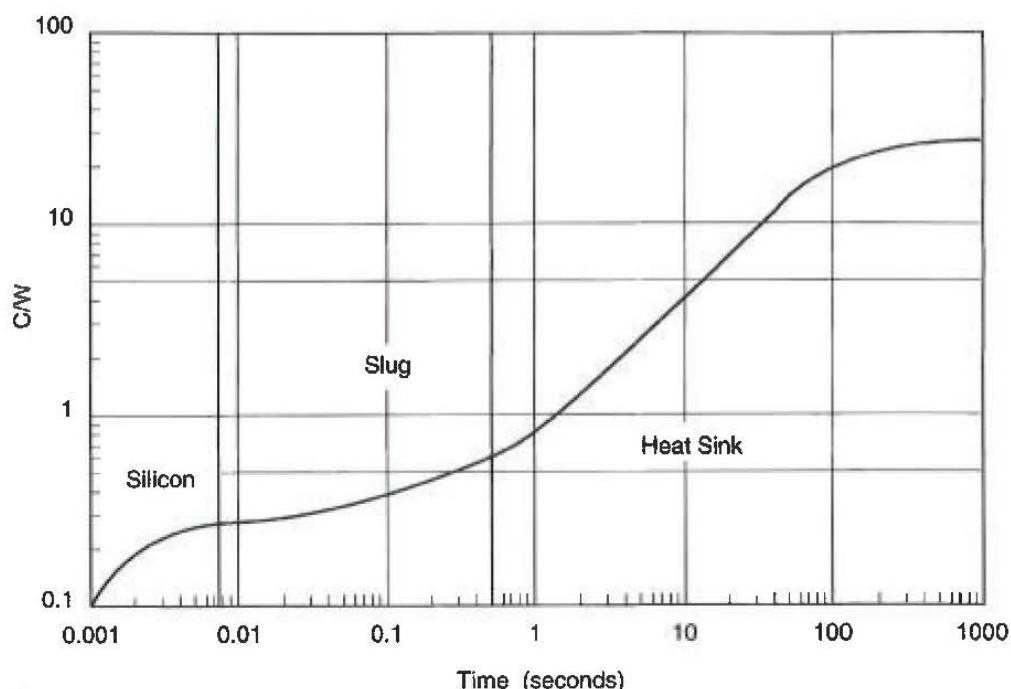


Fig. 13.14 Typical thermal impedance of power IC package (Multiwatt)

When an external heat sink is used the third cell can have a time constant of hundreds of second and equilibrium can take several minutes. Each element is ruled by the theoretical relationship

$$\Delta T = \theta \cdot P_d (1 - e^{-t/\tau}) \quad (13.7)$$

and the actual behaviour of the package is a combination of the effects of the three cells.

A large plateau occurs up to 1–2 sec, due to the copper slug, limiting the thermal impedance to 0.2–2.0°C/W (Fig. 13.14). This effect is often used in switching applications, as a large number of power pulses can be dissipated before a large variation in the junction temperature takes place.

13.5

Process and Materials [3, 4]

The operation of plastic packaging assembly is a sequence of five main processes: (Fig. 13.15): die attach, wire bonding, molding, lead plating, lead forming. Some important difference exists between medium power and high power packages, which will be outlined in the next few paragraphs.

Due to their strong impact on device performance and reliability, materials like tin based alloys, encapsulation compounds, and surface plating deposits, have vital importance in plastic packaging technology, and its evolution towards cost effective solutions and low failure rates. In Fig. 13.16, thermomechanical characteristics of most important packaging materials are compared.

13.5.1

Leadframe

The leadframe is the mechanical support and the electrical and thermal interconnection of silicon chip. Leadframe for low-medium dissipation have a uniform thickness of 5–10 mils (125–250 micron); most frequently, copper alloys are chosen (instead of the very popular Fe/Ni Alloy 42), due to the excellent thermal and electrical conductivity [5, 6].

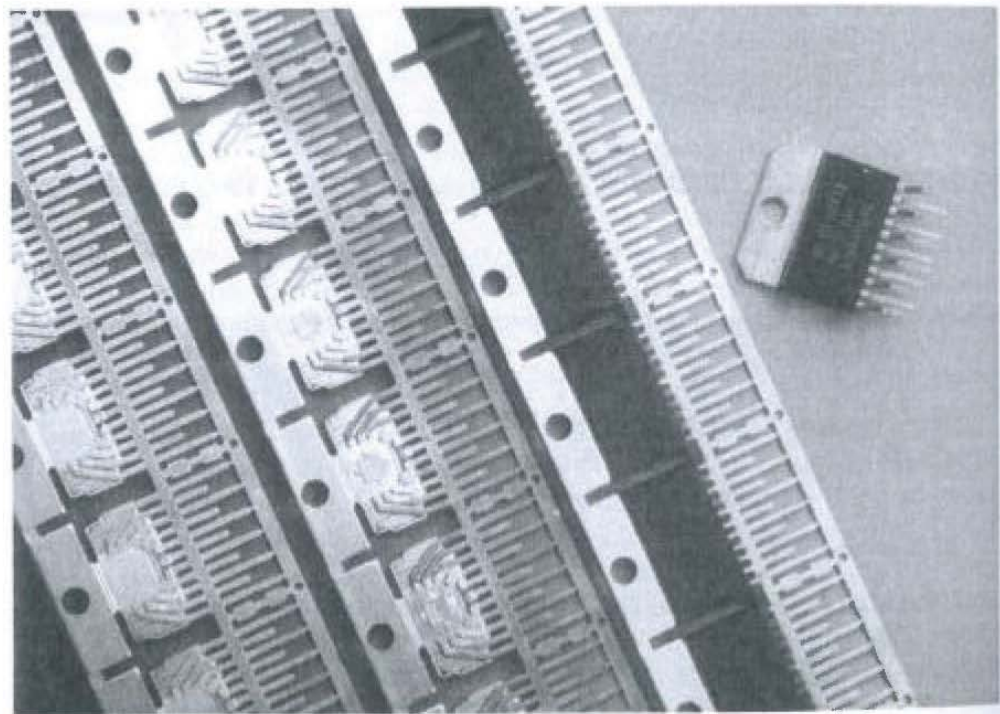


Fig. 13.15 Assembly process, from leadframe to finished product through: die attach, wire bonding, molding, lead plating, lead forming

		Coefficient of Linear Expansion ($^{\circ}\text{C}^{-1}$)			
		10^{-7}	10^{-6}	10^{-5}	10^{-4}
Device	CVDPSPG	Si_3N_4	Si	Al	
				Polymide	
Lead Frame			42	Cu	
			Alloy	Alloy	
Lead Frame			Ni	Ag	
Plating				Ag	Solder
Die Bonding				Glue	
Wire Bonding				Au	
Encapsulant				Epoxy Resin	
Plating to Outer Lead				Sn/Pb	Sn

Fig. 13.16 Thermomechanical characteristics of typical packaging materials

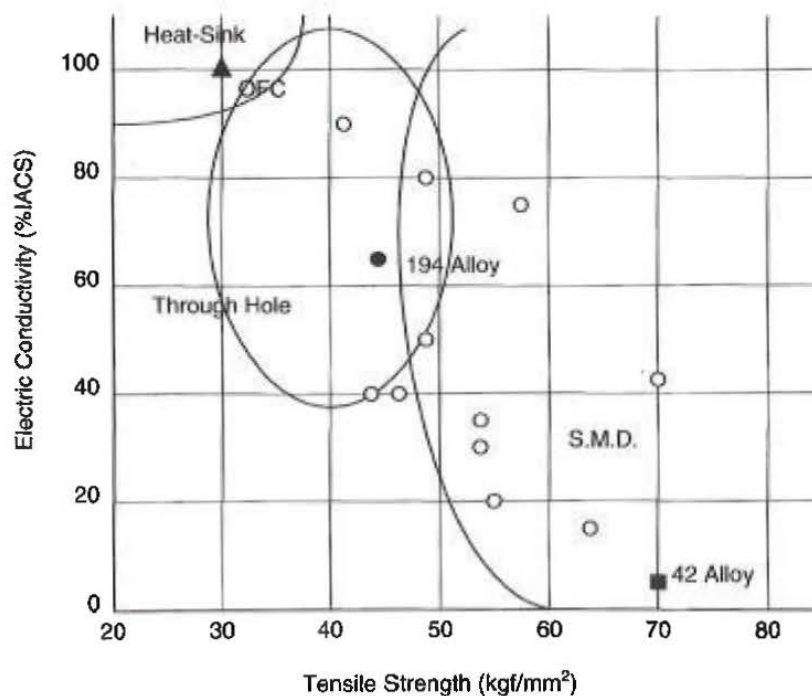


Fig. 13.17 Thermomechanical characteristics of copper alloys used in slug and leadframe fabrication

As Surface Mount Devices (SMD) are progressing toward fine pitch and multipins, lead position and planarity after assembly and testing are very critical issues. Due to this reason, special copper alloys have been developed offering a good compromise in mechanical stability and thermal conductivity.

Leadframes for high power devices have a copper slug of appropriate size, in order to reduce the junction to case thermal resistance down to a minimum value and provide some thermal capacitance in pulsed application. Oxygen Free Copper (OFC) or de-oxidized copper is often chosen, in order to have as high thermal conduction as possible.

In Fig. 13.17, thermomechanical characteristics of different copper alloys are shown for the different applications.

Both medium power and power leadframe, are silver or nickel plated in the die attach area and on lead tips, where bonding wire is welded.

13.5.2

Die Attach

After wafer sawing (die fab) high power die is brazed onto the slug using high melting temperature ($> 280^{\circ}\text{C}$) tin based alloys, as PbSn, PbSnAg, SnAgSb.

This process is critical in view of thermal performance and long term reliability; it must produce a uniform, void free joint between silicon back metallization (CrNiAu, CrNiAg, TiNiAu, etc.) and copper slug, in order to avoid hot spots in the active area and mechanical degradation in thermal fatigue.

Characteristics of several solder alloys are given in Table 13.7 [7].

For low-medium power die, packages in SO, PLCC and PQFP, epoxy or polyimide glue die attach is commonly used. As it is compatible with the process needed by signal devices assembled in huge quantities in the same lines, this choice is effective in cost, while maintaining acceptable thermal performance. Thermal conductivity of glue is improved by adding a metal filler, commonly Ag.

In Table 13.8, physical characteristics of different glues (basically epoxy glue with and without solvent and polyimide glue) are summarized.

13.5.3

Wire Bonding

After die attach, electrical interconnection between die bonding pads and leadframe is obtained, by means of gold or aluminium wire [8]. They are ultrasonically bonded to the chip and to selected areas in the leadframe, which are Ag plated in Au wire bonding or Ni plated in Al wire bonding.

Choice of Au or Al wire is performed after several considerations:

- 1) Process speed, which is higher for Au bonding, with 6 wires bonded in one second, more than twice the Al speed;
- 2) reliability in epoxy encapsulation, related to the corrosion resistance, critical with Al wires and totally missing in Au wires. Due to this reason, a minimum Al wire diameter in plastic packages is 5–6 mils ($125\text{--}150\text{ }\mu$) versus 1.5 mils ($38\text{ }\mu$) in ceramic packages;

Table 13.7 Properties of soft solder

	Alloy (wt %)	Temperature		Tensile Strength (Kg/mm ²)	Elongation (%)	Hardness (H _B)	Electrical Conductivity (IACS %)	Specific Gravity (g/cm ³)
		Solidus (°C)	Liquidus (°C)					
Pb/Sn	Pb/2 Sn	316	322					11.2
	Pb/5 Sn	300	314					11
	Pb/10 Sn	268	301					10.7
	Pb/20 Sn	183	279					10.2
	Sn/38.1 Pb	*(E) 183					8.4	
	Sn/40 Pb	183	190					8.5
Pb/Ag	Pb/2.5 Ag	*(E) 304		3.1	42		8.8	11.4
	Pb/3.5 Ag	304	317	4.2		8	8.7	11.3
	Pb/5 Ag	304	364	3.5	35		7.2	11.3
Pb/In	Pb/5 In	310	314	3	52	6	5.1	11.1
	Pb/10 In	294	300					10.8
	Pb/25 In	255	265					10
Pb/In/Ag	Pb/5 In/2.5 Ag	304	307	3.2		9	6.9	11
	Pb/5 In/5 Ag	290	310					11
Pb/Sn/Ag	Pb/2 Sn/2.5 Ag	299	304	2.5				11.2
	Pb/5 Sn/1.5 Ag	*(E) 296					7.9	11.1
	Pb/5 Sn/2.5 Ag	296	300	4.5		10	8.1	11.1
	Pb/10 Sn/2 Ag	275	300					10.8
Pb/Sb	Pb/2 Sb	300	314	1.9	51		8.1	11.2
	Pb/5 Sb	252	298	5.8	24	11	6.3	11
Sn/Ag	Sn/3.5 Ag	*(E) 221		2	73	40	14	7.4
	Sn/5 Ag	221	250	5.6	30	14	12.6	7.4
	Sn/10 Ag	221	295					7.5
In/Sn	In/45 Sn	117	119					7.3
	In/48 Sn	*(E) 117		1.2	83	5	11.7	7.3
	In/50 Sn	117	125					7.3
In/Ag	In/3 Ag	*(E) 141						7.4
	In/10 Ag	141	230	1.1	61	2.7	22.1	7.5

* E = Eutectic Alloy.

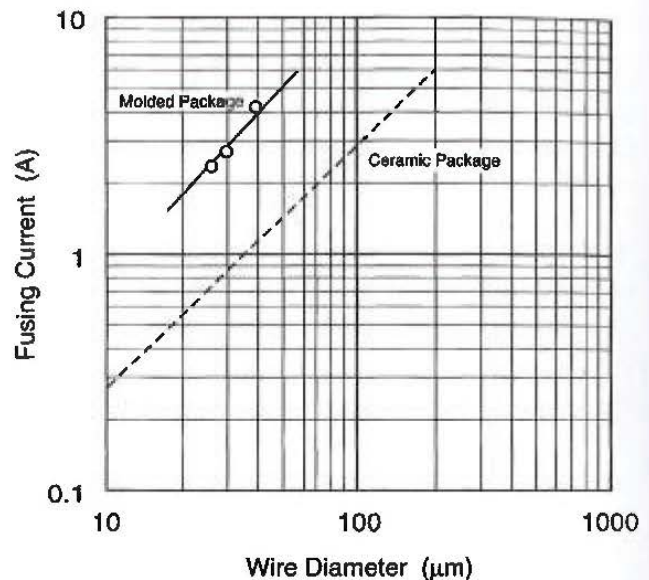
Table 13.8 Physical characteristics of Ag glue

	Epoxy solvent	Epoxy non solvent	Polyimide
H ₂ O absorb ratio	○	△	△
Peeling strength	○	△	⊙
Die share strength	○	△	⊙
Void in die bonding	○	○ ~ △	△
Thermal conductivity (cal/cm s °C)	$4 \sim 5 \cdot 10^{-3}$	$4 \sim 5 \cdot 10^{-3}$	$1 \sim 2 \cdot 10^{-3}$
Electric resistivity (Ω cm)	$1 \sim 10 \cdot 10^{-4}$	$1 \sim 10 \cdot 10^{-4}$	$1 \cdot 10^{-4}$

○ fair

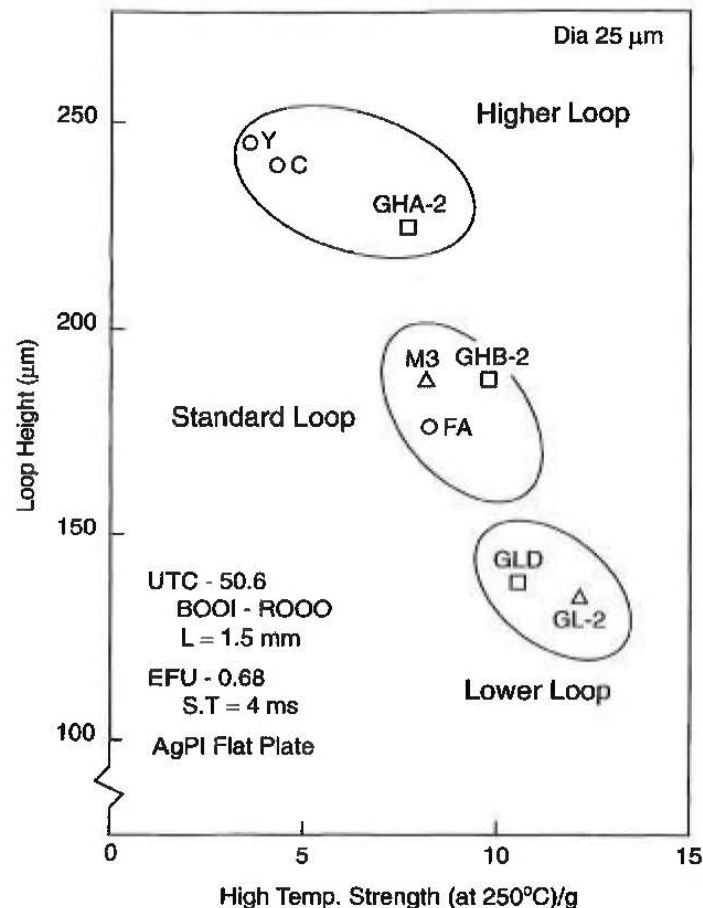
△ good

⊙ very good

Fig. 13.18 Fuse current for Au and Al wires

- 3) capability in handling current, which is related to material, diameter and environment. About wire diameter in plastic package, the empirical rule is 1.3 A/mil as max DC current. Fuse current is shown in Fig. 13.18; it can be noticed that in plastic package, due to the intimate contact between wire and encapsulant, the fuse current is about 3 times higher than in cavity ceramic packages [9];
- 4) bonding design rules, in terms of bonding pad size and loop height control. Especially in low profile power SMD, limitation of this parameter should be taken into account (Fig. 13.19).

Fig. 13.19 Relationship of the wire loop vs the characteristics of bonding wire



13.5.4 Molding

Molding is the third step of assembly, when the leadframe strips are positioned in molding cavities which are then pressure filled with liquid thermosetting compound. After 40–80 s at about 180°C , the compound solidifies in the mold (curing) in order to provide hard, reliable and cost effective encapsulation.

The molding compound is a key factor in package fabrication; it is in permanent evolution toward lower mechanical stress, lower impurity content and better cost [10].

The base material is thermosetting epoxy, filled with fused silica to enhance reliability and control thermal expansion coefficient. A different filler like Al_2O_3 or SiC can be used in order to increase thermal conductivity of the molding compound.

One of the most important properties is the natural absorption of moisture from the ambient. During the board mounting of surface mount devices, due to the relatively high soldering temperature (220 – 240°C) moisture is suddenly

desorbed, with possible cracks and delaminations in the package structure. This event known as "popcorn effect" is a major cause of failure in plastic SMD [11, 12].

13.5.5

Lead Plating and Lead Forming

The last major steps in semiconductor assembly are lead plating and forming.

After molding, external portion of the leadframe is electroplated by a 6–15 μ thick solder alloy (Pb Sn); this tin rich alloy is a low melting temperature coating, which provides a "wetable" surface when devices are soldered on the printed board.

Due to this reason, lead finishing has impact on quality and reliability of the solder joint, at system level. Lead solderability is measured by means of especially developed tests, as described in the next Chapter.

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