

Power Integrated Circuits—A Brief Overview

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Abstract—A brief overview of developments in power and high-voltage integrated circuits is presented. The technology can be classified into two types: 1) smart power devices that contain one or more common drain, vertical power transistors with control, and protective circuitry built on the same chip, and 2) high-voltage integrated circuits that combine lateral high-voltage with CMOS logic and analog bipolar circuits on the same chip. These technologies are being aimed at display drivers, telecommunications, motor drives, power supplies, and automotive electronics. A rapid growth in their application in the future can be expected.

I. INTRODUCTION

UNTIL A FEW years ago, power electronics and integrated circuits have taken separate routes. Power electronics has relied upon the implementation of circuits using discrete components. The major thrust in this area has been the development of power semiconductor devices with higher power handling capability. With the availability of microprocessors, the control system has been amenable to integration. However, the relatively high currents encountered in the gate drive circuits for bipolar transistors has required a discrete part implementation of these circuits.

During the last five years, a new class of MOS controlled power devices has emerged. Among these devices are the power MOSFET and power MOS-IGT [1]. These devices were developed because of their high-input impedance feature. The low-input gate currents required to control these devices makes the size of the components used in the gate drive circuits sufficiently small that these circuits are now amenable to integration. This has created the opportunity to obtain a large decrease in component count, resulting in a reduction in system cost, size, and weight. In addition, the smaller number of interconnects enhances system reliability. These features have created a resurgence in power electronic applications.

Power integrated-circuit technology can be partitioned into two broad categories: 1) "smart" discrete vertical power structures with sense or protection elements and logic or analog circuitry built into the same chip; and 2) high-voltage integrated circuits in which conventional logic and analog circuits are combined with high-voltage lateral devices. Considerable developmental effort is being undertaken in both categories. The smart discrete device effort is mainly targeted to automotive electronics, while the high-voltage integrated circuits are being developed

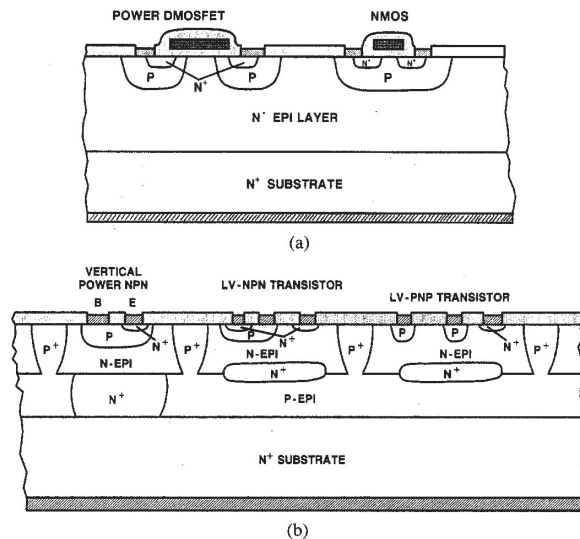


Fig. 1. (a) Discrete vertical double-diffused MOSFET structure with an n-MOS transistor integrated with it using a p-well technology. (b) Discrete vertical bipolar transistor integrated with lateral p-n-p transistor and vertical low-voltage n-p-n transistor using a double epitaxial layer technology with an n⁺ plug.

for motor control, telecommunications, power supplies, displays, etc. The power spectrum over which this power technology can be applied ranges from 50 to 1200 V, with currents of 1 to 100 A.

II. SMART POWER TECHNOLOGY

The base of the smart power device technology is a discrete power device into whose structure other circuit elements are integrated to achieve an increase in functionality. Both discrete bipolar transistors and power MOSFET's have been used to create the desired smart power switches, as illustrated in Fig. 1. The power discrete devices are designed with vertical current flow by using an epitaxial drift layer grown on a highly doped substrate. The circuit elements can be integrated into the device by taking two approaches. In the first approach (Fig. 1(a)) a lightly doped p-well is diffused into the n-epitaxial layer and the lateral integrated elements built in the p-well [2]. In the second approach, a double epitaxial layer is utilized to achieve isolation [3]. In this case, an n⁺ plug is diffused through the p⁺ epitaxial layer in order to create a vertical current path for the power transistor. In addition, n⁺ buried layers are used for reducing the collector

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resistance of the n-p-n transistor and to increase the gain of the lateral p-n-p transistor.

This technology is limited to the integration of CMOS logic and analog sense-protection circuitry with either a single power transistor or an array of common drain power transistors. Such arrays are useful for implementation of a monolithic high side switch in automotive electronics. Complex chips combining CMOS logic for encode/decode functions and analog circuits for current and over-temperature protection with a power MOSFET have been reported [3]. In addition to the bipolar transistor illustrated in Fig. 1(b), several other vertical power structures have been used in this configuration. The power MOSFET is a prime candidate for automotive electronics. The IGT is a candidate for high-voltage systems which require a smart switch with built-in self-protection features. The MOS-gated SCR [4] has also been used as the power device to create a crowbar chip for protection of other integrated circuits against adverse conditions, such as excessive temperature excursion [5].

III. HIGH-VOLTAGE INTEGRATED CIRCUITS

A variety of approaches have been developed to achieve a combination of high-voltage lateral transistors with logic and analog circuits. These technologies can be broadly classified into those based upon self-isolation, junction isolation, and dielectric isolation.

Self-Isolation: This technology utilizes the reverse-biased junction between the source-drain region and the body region to obtain isolation. An illustration of a self-isolated high-voltage device integrated with CMOS logic is provided in Fig. 2. In this process, the p^- substrates serve as the body region of the n^- channel FET's and an n-well is used to form the p-MOS transistors. It should be noted that the high-voltage transistor must be designed with an annular structure where the drain is completely surrounded by the gate-source regions. This limits the technology to common source high-voltage output devices. Breakdown voltages of up to 1000 V have been reported [6]. A typical example of an application for this HVIC approach is in display drivers.

Junction Isolation: This approach utilizes the ability of a reverse biased n^- epitaxial/ p^- substrate junction to provide isolation. Within this context, two alternatives have been explored. In the first, a thick epitaxial layer is used, as shown in Fig. 3(a). This preserves a vertical high-voltage transistor structure that can be optimized for high current handling capability within the limitation of the resistance of the p^+ buried layer and sinker diffusion [7]. The disadvantages of this approach are the poor performance of the low-voltage transistors due to the thick extended drain and the large area consumed by the deep p^+ isolation diffusions and the deep n^+ sinker diffusions.

In the second approach, a thin (5–8 μm) epitaxial layer is used, as shown in Fig. 3(b). Here, the n^- epitaxial layer is optimized to achieve high-performance low-voltage n-p-n and p-n-p transistors. The high-voltage transistor is achieved by using the "RESURF" principle [8]. The RE-

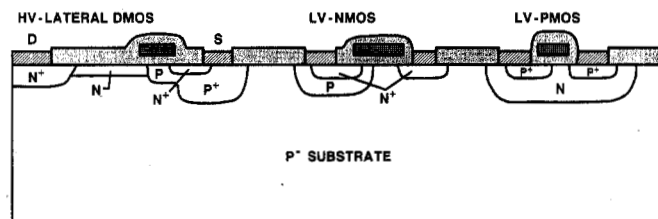


Fig. 2. Self-isolated high-voltage DMOS transistor integrated with CMOS logic components.

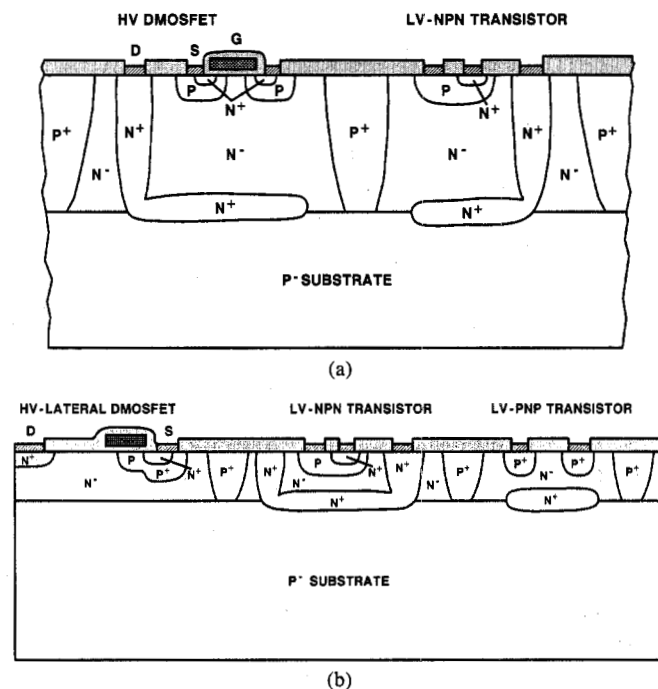


Fig. 3. (a) High-voltage DMOSFET integrated with a low-voltage n-p-n transistor by using thick-epitaxial layer technology. (b) High-voltage lateral DMOSFET integrated with low-voltage n-p-n and p-n-p transistors using the RESURF concept.

SURF concept is based upon using an optimized charge in the n^- epitaxial layer in the range of 0.5 to $1 \times 10^{12}/\text{cm}^2$. This limited charge forces a two-dimensional redistribution of the electric field so that a high voltage can be supported laterally between the source and drain of the DMOSFET. An important advantage of this technology is that the breakdown voltage of the high-voltage devices can be scaled up by simply increasing the distance between the gate-source region and the drain region on the masks without any process alteration. This allows the use of a single manufacturing process for fabrication of a variety of high-voltage IC's suited to applications at different voltages. It even allows the fabrication of optimized high-voltage devices of different voltage ratings on a single chip. Due to the ability to form high-performance latchup-resistant CMOS circuitry and bipolar analog circuitry on the same chip with high-voltage lateral transistors, this technology can be used for a variety of applications, such as motor controls and power supplies [9].

Dielectric Isolation: The above isolation approaches cannot be used for the integration of all desirable com-

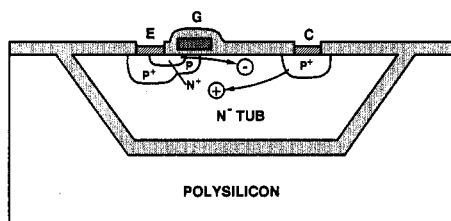


Fig. 4. A high-voltage lateral insulated gate transistor structure formed in a dielectrically isolated tub.

ponents and are prone to latchup failure at high temperatures. These problems can be overcome by using dielectric isolation. An example of a dielectrically isolated MOS bipolar transistor is shown in Fig. 4. In this example, an n-channel IGT is shown. In the on-state, the IGT operates with a high concentration of minority-carriers injected into the drift region [10]. This results in a high operating current density that can be utilized to raise the power handling capability of the power IC by an order of magnitude [11]. Such bipolar power devices cannot be implemented with junction isolation due to large substrate current flow. Dielectric isolation also provides a much higher packing density due to the smaller area taken up by the isolation region. This can offset the higher cost of the starting material [11].

Dielectrically isolated cross-point arrays are now being used in high volume in telecommunication systems [12]. Considerable effort is being undertaken to lower the cost of the starting material by developing alternate methods to produce dielectrically isolated tubs [13], [14]. As the cost of the starting material decreases, this technology can be expected to be favored for more and more high-voltage integrated circuits.

IV. CONCLUSIONS

Power and high-voltage integrated circuits are being developed for a wide variety of applications ranging from automotive electronics, home appliance control, motor drives, and computer power supplies at the higher power levels to cross-point arrays in telecommunications and display drivers at low power levels. A continual growth in the versatility of this technology can be anticipated. At the same time, there is a strong trend toward reducing cost because this technology is relatively new and will progress rapidly down the learning curve. In addition to improved processing techniques and tighter design rules, the integration of MOS-controlled bipolar devices can be expected to boost the power handling capability by at least an order of magnitude. These technical developments are expected to result in a very rapid growth in the application of this technology. As the applications proliferate, computer-aided design (CAD) tools will be necessary to shorten the design cycle since most of the circuits must be customized to suit each application. With the increasing effort being devoted to both process/device technology and CAD tool development, a bright future can be

predicted for these application specific integrated circuits (ASIC's) aimed at power control applications.

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