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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/290,589	12/01/2005	Masao Murade	114542.01

27049
OLIFF PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

CONFIRMATION NO. 9273
POWER OF ATTORNEY NOTICE



OC000000137397057

Date Mailed: 02/15/2023

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/13/2023.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/290,589	12/01/2005	Masao Murade	ZJ0007516US02

CONFIRMATION NO. 9273

POA ACCEPTANCE LETTER



OC000000137397077

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

Date Mailed: 02/15/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/13/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	11/290,589
Filing Date	12/01/2005
First Named Inventor	Masao Murade
Title	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS
Art Unit	2871
Examiner Name	JAMES A DUDEK
Attorney Docket Number	ZJ0007516US02

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael Bartholomew/	Date (Optional)	
Name	Michael Bartholomew	Registration Number	60225
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	138 EAST LCD ADVANCEMENTS LIMITED		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐

*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

36491

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

138 East LCD Advancements Limited

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Garrett Dempsey

Title

Director, 138 East LCD Advancements Limited

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: 138 EAST LCD ADVANCEMENTS LIMITED

Application No./Patent No.: 11/290,589 Filed/Issue Date: 12/01/2005

Titled: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

138 EAST LCD ADVANCEMENTS LIMITED, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: SEIKO EPSON CORPORATION To: 138 EAST LCD ADVANCEMENTS LIMITED

The document was recorded in the United States Patent and Trademark Office at
Reel 050197, Frame 0212, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Michael Bartholomew/

Signature

Michael Bartholomew

Printed or Typed Name

2023-02-13

Date

60225

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	47525821
Application Number:	11290589
International Application Number:	
Confirmation Number:	9273
Title of Invention:	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS
First Named Inventor/Applicant Name:	Masao Murade
Customer Number:	27049
Filer:	Michael Lee Bartholomew/Mary Keshishian
Filer Authorized By:	Michael Lee Bartholomew
Attorney Docket Number:	114542.01
Receipt Date:	13-FEB-2023
Filing Date:	01-DEC-2005
Time Stamp:	17:51:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_ZJ0007516US02.pdf	580734	no	2
			229dae245137834ed3b60af08a127ff5932bce9e		

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	Statement373_ZJ0007516US02.pdf	123112	no	3
			65ff15f9550beb5287b658d3735439e143f10baaf		
Warnings:					
Information:					
Total Files Size (in bytes):			703846		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/290,589	7502079	2871	9200



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 27049 on 10/20/2009

- Correspondence Address
- Power of Attorney Address

The address of record for Customer Number 27049 is:

27049
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	03/10/2009	7502079	114542.01	9273

25944 7590 02/18/2009
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 498 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

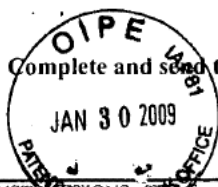
If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Masao Murade, Suwa-shi, JAPAN;

**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. Correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 12/02/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	12/01/2005	Masao Murade	114542.01	9273

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	-\$0	\$1810	03/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
DUDEK, JAMES A	2871	349-039000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oloff & Berridge, PLC

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Seiko Epson Corporation

Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☒ A check is enclosed. check # 214499
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Typed or printed name

Daniel A. Tanner, III

Date: 02/02/2009 00:00:00 11290589

Registration No. 01 FC:1561 02 FC:1504

54,734

1510.00 OP
300.00 OP

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25944 7590 12/02/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER

DUDEK, JAMES A

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 12/02/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	12/01/2005	Masao Murade	114542.01	9273
TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/02/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 12/02/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/290,589	12/01/2005	Masao Murade	114542.01	9273
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TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
DUDEK, JAMES A	2871	349-039000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	12/01/2005	Masao Murade	114542.01	9273
25944	7590	12/02/2008	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			DUDEK, JAMES A	
			ART UNIT	PAPER NUMBER
			2871	
DATE MAILED: 12/02/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 498 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 498 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/290,589	MURADE, MASAO	
	Examiner	Art Unit	
	/James A. Dudek/	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 8/25/08.

2. ☒ The allowed claim(s) is/are 5-7.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/320371 .
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.

 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ . 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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/James A. Dudek/ Primary Examiner Art Unit: 2871	
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	443	349/39.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/09 09:48
S2	1	"6388721".pn.	USPAT	OR	ON	2008/11/13 11:29
S3	489	349/39.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/24 09:55
S4	1	"6388721".pn.	USPAT	OR	ON	2008/11/24 09:55
S5	1	"4239346".pn.	USPAT	OR	ON	2008/11/24 09:56
S6	123	349/47.ccls. not (S3 S5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/24 09:58

11/24/08 10:46:56 AM

C:\Documents and Settings\jdudek\My Documents\EAST\workspaces\11290589.wsp

<i>Index of Claims</i> 	Application/Control No. 11290589	Applicant(s)/Patent Under Reexamination MURADE, MASAO
	Examiner /James A Dudek/	Art Unit 2871

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	06/09/2008	11/24/2008												
	1	✓	-												
	2	✓	-												
	3	✓	-												
	4	✓	-												
1	5		=												
2	6		=												
3	7		=												

Search Notes 	Application/Control No. 11290589	Applicant(s)/Patent Under Reexamination MURADE, MASAO
	Examiner /James A Dudek/	Art Unit 2871

SEARCHED			
Class	Subclass	Date	Examiner
349	43,39,38,113	6/8/08	jad
updated		11/24/08	jad
349	47	11/24/08	jad

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
pgpub as above		11/24/08	jad

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IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 11/290,589

Examiner: J. DUDEK

Filed: December 1, 2005

Docket No.: 114542.01

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

SUMMARY OF SUBSTANCE OF INTERVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

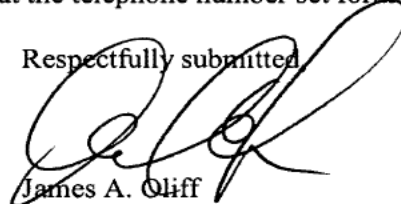
Applicant's representatives conducted a telephone interview, in connection with the above-identified application, with Examiner Dudek on August 26, 2008. Applicant thanks Examiner Dudek for the courtesies extended to Applicant's representatives.

During the interview, Applicant's representatives discussed the Amendment filed August 15, 2008 with the Examiner. Applicant's representatives asserted that U.S. Patent No. 6,388,721 to Murade and U.S. Patent No. 5,748,276 to Uno et al. (hereinafter "Uno") do not teach a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line, as recited in claims 5 and 6.

Examiner Dudek indicated that he would further consider these arguments upon submission of a formal response. The Examiner indicated that a further search would be necessary.

Should any questions or inquiries arise regarding this submission, all inquiries may be directed to Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Daniel A. Tanner, III
Registration No. 54,734

JAO:DAT/add

Date: August 29, 2008

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	12/01/2005	Masao Murade	114542.01	9273
25944 7590 08/28/2008 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER DUDEK, JAMES A	
			ART UNIT 2871	PAPER NUMBER
			MAIL DATE 08/28/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No.	Applicant(s)	
	11/290,589	MURADE, MASAO	
	Examiner	Art Unit	
	/James A. Dudek/	2871	

All participants (applicant, applicant's representative, PTO personnel):

(1) /James A. Dudek/ (3) _____.

(2) Daniel Tanner. (4) _____.

Date of Interview: 26 August 2008.

Type: a) ☒ Telephonic b) ☐ Video Conference
c) ☐ Personal [copy given to: 1) ☐ applicant 2) ☐ applicant's representative]

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☒ No.
If Yes, brief description: _____.

Claim(s) discussed: 5-7.

Identification of prior art discussed: '721, '276.

Agreement with respect to the claims f) ☒ was reached. g) ☐ was not reached. h) ☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: newly submitted claims 5-7 overcome the rejection mailed 6/13/08.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

	//James A. Dudek// Primary Examiner, Art Unit 2871
--	---

Applicant Initiated Interview Request Form

Application No.: 11/290,589 First Named Applicant: Masao MURADE
 Examiner: J. DUDEK Art Unit: 2871 Status of Application: Pending

Tentative Participants:

(1) J. Dudek (2) D. Tanner
 (3) M. Lutwyche (4) _____

Proposed Date of Interview: 08/26/08 Proposed Time: 10:45 AM

Type of Interview Requested:

(1) ☐ Telephonic (2) ☒ Personal (3) ☐ Video Conference

Exhibit To Be Shown or Demonstrated: ☐ YES ☒ NO

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Applied Reference(s)	Discussed	Agreed	Not Agreed
(1) §102(b)	Claims 1-4	U.S. 6,388,721 U.S. 5,748,276	☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Arguments to be Presented:

U.S. Patent No. 6,388,721 and U.S. Patent No. 5,748,276 do not teach the features of independent claims 5 and 6.

An interview was conducted on the above-identified application on _____

NOTE:

This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of substance of this interview (37 CFR 1.133(b)) as soon as possible.

M-L I Lwen
 (Applicant/Applicant's Representative Signature)

 (Examiner/SPB Signature)



Jan

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 11/290,589

Examiner: J. DUDEK

Filed: December 1, 2005

Docket No.: 114542.01

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the June 13, 2008 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-4 (Canceled)

5. (New) An electro-optical device, comprising:

a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

a pixel electrode formed correspondingly to the thin-film transistor;

a data line extending in the direction in which the channel area extends, the data line having a broad-width portion that overlaps the channel area in plan view;

a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion;

a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed-potential capacitor electrode;

a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and

a contact hole electrically connecting the data line and the thin-film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.

6. (New) An electro-optical device, comprising:

a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

a pixel electrode formed correspondingly to the thin-film transistor;

a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, the broad portion being wider than the non-broad portion;

a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;

a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and

a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.

7. (New) The electro-optical device according to claim 6, further comprising a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor a portion where the contact hole is located.

REMARKS

Claims 5-7 are pending in this application. By this Amendment, claims 5-7 are added; and claims 1-4 are canceled without prejudice to or disclaimer of the subject matter recited therein. Support for claims 5-7 can be found in at least Figure 2 and the corresponding description in the specification. Thus, no new matter is added.

I. 35 U.S.C. § 102(b) Rejection Of Claims 1-4

The Office Action rejects claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,388,721 to Murade and U.S. Patent No. 5,748,276 to Uno et al. The rejection of canceled claims 1-4 is moot.

Further, neither Murade nor Uno discloses a contact hole electrically connecting the data line and the thin-film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole, as recited in independent claim 5.

Additionally, neither Murade nor Uno disclose a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line, as recited in independent claim 6. Thus, claim 6 and its dependent claim are patentable over Murade and Uno.

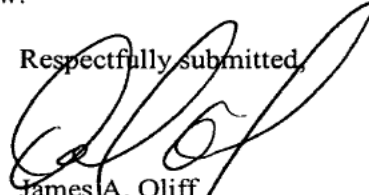
Accordingly, for at least these reasons, Applicant requests withdrawal of the rejection.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Daniel A. Tanner
Registration No. 54,734

JAO:KDB/add

Date: August 15, 2008

OLIFF & BERRIDGE, PLC
P.O. Box 320850
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/290,589		Filing Date 12/01/2005		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	08/15/2008	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 3	Minus	** 20	= 0	X \$ =		OR	X \$50=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =		OR	X \$210=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))					OR				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR				
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/STELLA LITTLE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/290,589	12/01/2005	Masao Murade	114542.01	9273
25944 7590 06/13/2008 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER DUDEK, JAMES A	
			ART UNIT 2871	PAPER NUMBER
			MAIL DATE 06/13/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/290,589	MURADE, MASAO	
	Examiner	Art Unit	
	/James A. Dudek/	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5) ☐ Claim(s) ____ is/are allowed.

6) ☒ Claim(s) 1-4 is/are rejected.

7) ☐ Claim(s) ____ is/are objected to.

8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 12/1/05 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☒ Certified copies of the priority documents have been received in Application No. 10/320,371.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/1/05.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Murade (US 6388721).

Murade discloses an electro-optical device comprising (see at least Figure 1): a substrate; scanning lines above the substrate and extending in a predetermined direction; data lines (3) above the substrate and extending in a direction intersecting the scanning lines (2); thin film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; pixel electrodes (14) formed correspondingly to the thin film transistors; a respective scanning line having a broad width portion (see at least Figure 1) as a gate electrode in a portion facing a channel area (1c) of a respective thin film transistor and a narrow width portion (portions narrowing than broad width portion) in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion intersecting a direction in which a scanning line extends and extending in a single/bi direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole (5), the contact hole electrically connecting the channel area and the data line, the pixel electrodes being arranged in a matrix shape; the respective channel area formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected; the narrow width portion being formed at a position deviated from a center of the first gap, and the broad width portion being formed at the center of the first gap in the intersecting area.

Murade discloses the broad width portion formed at a center of the second gap in the intersecting area (see at least Figure 1).

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Uno (US 5748276, IDS).

Uno discloses an electro-optical device comprising (see at least Figure 1): a substrate; scanning lines above the substrate and extending in a predetermined direction; data lines above the substrate and extending in a direction intersecting the scanning lines; thin film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; pixel electrodes (21) formed correspondingly to the thin film transistors; a respective scanning line having a broad width portion (see at least Figure 1) as a gate electrode (4) in a portion facing a channel area (6) of a respective thin film transistor and a narrow width portion (portions narrowing than broad width portion) in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion intersecting a direction in which a scanning line extends and extending in a single/bi direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole (7b), the contact hole electrically connecting the channel area and the data line, the pixel electrodes being arranged in a matrix shape; the respective channel area formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected; the narrow width portion being formed at a position deviated from a center of the first gap, and the broad width portion being formed at the center of the first gap in the intersecting area.

Murade discloses the broad width portion formed at a center of the second gap in the intersecting area (see at least Figure 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to /James A. Dudek/ whose telephone number is 571-272-2290. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James A. Dudek/
Primary Examiner
Art Unit 2871

Notice of References Cited	Application/Control No. 11/290,589	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner /James A. Dudek/	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,239,346 A	12-1980	Lloyd, Randahl B.	349/44
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 9273

SERIAL NUMBER 11/290,589	FILING or 371(c) DATE 12/01/2005 RULE	CLASS 349	GROUP ART UNIT 2871	ATTORNEY DOCKET NO. 114542.01		
APPLICANTS Masao Murade, Suwa-shi, JAPAN; ** CONTINUING DATA ***** This application is a DIV of 10/320,371 12/17/2002 PAT 7,136,117 ** FOREIGN APPLICATIONS ***** JAPAN 2002-000713 01/07/2002 JAPAN 2002-363864 12/16/2002 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/09/2006						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/JAMES A DUDEK/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 21	TOTAL CLAIMS 4	INDEPENDENT CLAIMS 2
ADDRESS OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850 UNITED STATES						
TITLE Electro-optical device and electronic apparatus						
FILING FEE RECEIVED 1000	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: New U.S. Divisional Application of
Application No. 10/320,371

Filed: December 1, 2005

Docket No.: 114542.01

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. The references were cited by or submitted to the Office in parent application No. 10/320,371, filed December 17, 2002, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, copies of these references are not attached. 37 CFR §1.98(d).

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/axl

Date: December 1, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461
--

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JD/

Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 114542.01		APPLICATION NO. New U.S. Divisional Application of Application No. 10/320,371	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Masao MURADE			
				FILING DATE December 1, 2005			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
	1.	5,668,379	09/1997	Ono et al.			
	2.	5,831,694	11/1998	Onisawa et al.			
	3.	6,583,830	06/24/2003	Yasukawa et al.			
	4.	6,528,822	03/04/2003	Murade			
	5.	US2002-021379	02/21/2002	Kim			
	6.	5,748,276	05/05/1998	Uno et al.			
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
	7.	JP-A-2001-356709	12/26/01	Japan w/English Abstract & Translation			
	8.	WO 01/81994 A1	11/01/2001	PCT w/English Abstract			
	9.	2001-209070	8/3/2001	Japan w/English Translation			
	10.	JP2001-343912A	12/14/2001	Japan			
	11.	JP2001-330859	11/30/2001	Japan w/English Abstract & Translation			
	12.	JP2001-33125A	2/9/2001	Japan			
	13.	JP2001-356709	12/26/2001	Japan w/English Abstract & Translation			
	14.	JP-A-06-120099	04/28/1994	Japan			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
EXAMINER /James Dudek/					DATE CONSIDERED 06/09/2008		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: December 1, 2005

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JD/

<i>Index of Claims</i> 	Application/Control No. 11290589	Applicant(s)/Patent Under Reexamination MURADE, MASAO
	Examiner /James A Dudek/	Art Unit 2871

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	06/09/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								

Search Notes 	Application/Control No. 11290589	Applicant(s)/Patent Under Reexamination MURADE, MASAO
	Examiner /James A Dudek/	Art Unit 2871

SEARCHED			
Class	Subclass	Date	Examiner
349	43,39,38,113	6/8/08	jad

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner



17712 U.S. PTO

120105

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OLIFF & BERRIDGE, PLC
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

Attorney Docket No.: 114542.01

Date: December 1, 2005

113010 U.S. PTO
 11/290589



120105

MAIL STOP PATENT APPLICATION

Customer Number: 25944

**CONTINUING APPLICATION TRANSMITTAL
 RULE 1.53(b)**

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a

☐ Continuation ☒ Divisional ☐ Continuation-in-Part

application of prior pending Application No. 10/320,371, filed December 17, 2002.

For (Title): ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

By (Inventors): Masao MURADE

1. ☒ A Declaration of the inventor(s) is attached. The attached Declaration is:
 - ☒ a. A copy of the Declaration from the parent application. (Used with the same or fewer inventors and (a) a copy of the prior application or (b) a revised, reformatted or edited version of the prior application that does not contain new matter.)
 - ☐ b. A new Declaration. (Used with the same, fewer or additional inventors and (a) a copy of the prior application, (b) a revised, reformatted or edited version of the prior application that does not contain new matter, or (c) a new specification.)
2. ☒ A Power of Attorney is attached. The attached Power of Attorney is:
 - ☒ a. A copy of the Power of Attorney from the parent application.
 - ☐ b. A new Power of Attorney.

☐ The Power of Attorney is a General Power of Attorney.

A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached, and

A copy of the Assignment ☐ is attached to the Transmittal or ☐ was recorded at Reel _____ Frame _____.

☐ The Power of Attorney is a Specific Power of Attorney for this application (filed with or after an Assignment if assigned). A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached.

☒ The Power of Attorney is in a combined Declaration/Power of Attorney.

 - ☒ a. The Power of Attorney identifies no more than ten attorneys.
 - ☐ b. The Power of Attorney identifies more than ten attorneys, and a separate Designation of Ten Attorneys for Power of Attorney is filed herewith.

3. ☒ The fees due upon filing are calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF
ANY PRELIMINARY AMENDMENT NOTED BELOW

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
EXAMINATION FEE		
SEARCH FEE		
TOTAL PAGES OF APPLICATION OVER 100 (____ - 100)	+ 50	= †
TOTAL CLAIMS	4 - 20	= * 0
INDEP CLAIMS	2 - 3	= * 0
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED		

*If the difference is less than zero, enter "0".

†round up to next integer

SMALL ENTITY

RATE	FEE
	\$ 150
	\$ 100
	\$ 250
x 125 =	\$
x 25 =	\$
x 100 =	\$
+ 180 =	\$
TOTAL	\$

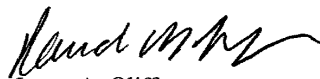
OTHER THAN A
SMALL ENTITY

RATE	FEE
	\$ 300
	\$ 200
	\$ 500
x 250 =	\$
x 50 =	\$
x 200 =	\$
+ 360 =	\$
TOTAL	\$ 1,000

4. ☒ Check No. 173537 in the amount of \$1,000 to cover the fees due upon filing is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.
5. ☒ Application Data Sheet is attached.
6. ☒ Formal drawings (Figs. 1-22) are attached.
- ☐ Use Figure _____ for front page of Publication.
7. ☒ Priority of foreign applications No. 2002-000713 filed January 7, 2002 in Japan and No. 2002-363864 filed December 16, 2002 in Japan is claimed under 35 U.S.C. §119 and/or §365(b).
- ☒ Certified copies were filed in prior Application No. 10/320,371 on February 11, 2003.
- ☐ A certified copy of the above foreign application(s) is filed herewith.
- ☐ A copy of the priority document was transmitted by the International Bureau in prior Application No. _____.
8. ☐ Priority of U.S. Provisional Application(s) No. _____ filed _____ is claimed under 35 U.S.C. §119.
- (A Preliminary Amendment is attached to reflect the claim of benefit in the specification if not already present.)
9. ☒ The prior application is assigned of record to SEIKO EPSON CORPORATION, TOKYO, JAPAN and recorded at Reel 013840, Frame 0487.
10. ☐ This application is filed by fewer than all the inventors named in the prior application (37 C.F.R. §1.53(b)(1)). Delete the following inventor(s) named in the prior application:

11. ☐ A Preliminary Amendment is attached. The Preliminary Amendment amends the specification to reflect the continuation data. Claims added by this Amendment are properly numbered consecutively beginning with the number next following the highest numbered claim in the application and claims canceled are identified in the listing of claims.
12. ☒ An Information Disclosure Statement is attached.
13. ☐ Small entity status:
- ☐ a. Entitlement to small entity status is asserted.
- ☐ b. Small entity status is no longer claimed.
14. ☐ Other: _____
15. ☐ This application is NOT to be published under 35 U.S.C. 122(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not been and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/axl

DEPOSIT ACCOUNT USE
AUTHORIZATION

Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

[0001] This is a Division of Application No. 10/320,371 filed December 17, 2002. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

1. Field of Invention

[0002] The present invention relates to an electro-optical device capable of performing active matrix drive. The invention also relates to an electronic apparatus incorporating such an electro-optical device.

2. Description of Related Art

[0003] The related art includes an electro-optical device including a pair of substrates constructed to sandwich an electro-optical material, such as a liquid crystal, therebetween and electrodes provided in each of the pair of substrates to apply an electric field to the electro-optical material. The electrodes are used to apply an electric field to the electro-optical material to vary the state of the material. According to such an electro-optical device, for example, when the light emitted from a light source enters the device and the state of the electro-optical material is varied, it is possible to control the light transmittance and thus realize desired image display.

[0004] Moreover, in related art electro-optical devices, by providing pixel electrodes arranged in a matrix shape, thin-film transistors (hereinafter "TFT") connected to the respective pixel electrodes, and scanning lines and data lines connected to each of TFTs and provided in parallel to a row direction and a column direction, respectively, on one of the pair of substrates, active matrix drive can be performed. As a result, for each pixel defined by the pixel electrodes or the scanning lines and the data lines, it is possible to control the electric field applied to the electro-optical material and to control the light transmittance.

SUMMARY OF THE INVENTION

[0005] However, in the related art electro-optical devices, there are the following problems. That is, for an electro-optical device capable of performing the above active matrix drive, it is required to precisely drive the TFTs. However, precisely driving the TFTs is a difficult task while satisfying the high precision and miniaturization requirements imposed in related art electro-optical devices.

[0006] A TFT includes a semiconductor layer having a channel area, a source area and a drain area, and a gate electrode formed through an insulating film to cover at least a

part of the channel area of the semiconductor layer. By applying or not applying the electric field to the channel area in accordance with the current applied (or not applied) to the gate electrode, the current flow can be controlled.

[0007] At this time, the length of the channel area, referred to as "channel length" or a width thereof, referred to as "channel width", that is, the size of the channel area is, is important to determine the characteristics of TFTs. Further, an arrangement of the gate electrode on the channel area is also a very important factor. In this regard, in the related art, a conductive member electrically connected to the scanning line or a member constituting a part of the scanning line, can be used as the gate electrode. However, there are problems in arranging the scanning line itself and the channel area.

[0008] In short, it is beneficial or required to realize a suitable arrangement of the channel area (or TFT) and the scanning line (or gate electrode) while realizing the high precision required in the electro-optical devices. Further, it is beneficial or required to realize the difficult task of precisely operating the TFT constructed as such.

[0009] For example, it is not sufficient to only drive the electro-optical device by the TFT, and the scanning line (or the gate electrode) and various elements are additionally required. However, it is generally difficult to accomplish the above arrangement or adjustment in connection with various other elements. Further, in the TFT, there is a disadvantage if it is required to prevent the light leakage current which is generated by the light entering the channel area. That is, it is preferable that the TFT is arranged as far as possible from a light-transmitting area, which is an area that the light contributes to image display in each pixel emitted through transmission or reflection, more specifically, from the pixel electrode. However, since this should be realized while satisfying the requirement of high precision, there is a further disadvantage in that the above arrangement/adjustment becomes an even more difficult task.

[0010] The present invention address the above and/or other problems, and provides an electro-optical device capable of easily adjusting the arrangement of a gate electrode and a scanning line and capable of precisely driving TFT and an electronic apparatus including the electro-optical device.

[0011] In order to address or solve the above problems, the electro-optical device of the present invention includes, on a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction intersecting the scanning lines, thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes formed correspondingly to the thin-film transistors. The respective

scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

[0012] According to the electro-optical device of the present invention, by supplying scan signals and image signals to the thin-film transistors through the scanning lines and the data lines, the pixel electrodes can be driven in an active matrix mode.

[0013] More specifically, in the present invention, since the scanning lines have the broad width portions as the gate electrode in a portion facing the channel area of the thin-film transistor and the narrow width portion in other portion, it is not only possible to realize the narrowness of the scanning line but also to more easily adjust/determine the arrangement between the channel area (or the thin-film transistor) and the scanning line than in the related art.

[0014] For example, when a plurality of pixel electrodes are arranged in a matrix shape, it is generally preferable that the thin-film transistor are configured such that the channel area of the thin-film transistor is positioned at the position farthest from the corner of each pixel electrode, that is, at the center position of a space among adjacent and opposite corners of the pixel electrodes when four pixel electrodes are considered (because it is farthest from the light transmitting area). However, in this case, by allowing the channel area to extend through a space between adjacent pixel electrodes including the center position, it is possible to adequately determine the channel length, and by arranging the scanning line to intersect it, it is possible to realize a structure that the broad width portion of the scanning line exists on the channel area. Therefore, in this case, it is possible to simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices. Further, in this case, the light incidence to the thin-film transistor or the channel area can be prevented as much as possible or reduced under the above-described assumption.

[0015] Like the above, according to the present invention, it is possible to adequately adjust the arrangement between the thin-film transistor and the scanning line or the gate electrode while satisfying the high precision requirements of the electro-optical devices. Further, this structure renders a good outcome even after arrangement of various elements constituting the electro-optical device has been adjusted and determined, in addition to the above scanning line and the thin-film transistor. Furthermore, according to the present invention, it is possible to precisely drive the thin-film transistor, and thus maintain the quality of image to be displayed at high level.

[0016] Further, in the present invention, "broad width" means that it is broader than the width of the "narrow width portion," and "narrow width" means that it is narrower than the width of the "broad width portion". In short, the broad and narrow degree of "the broad width portion" and the "narrow width portion" is determined in accordance with the relative relationship between them. Furthermore, the real width of the broad width portion or the narrow width portion can be adequately determined theoretically, experimentally or by simulation.

[0017] In one aspect of the electro-optical device of the present invention, the broad width portion has a portion lengthened from the narrow width portion.

[0018] According to this aspect, it is possible to form the scanning line relatively easily having the broad width portion and the narrow width portion. More specifically, for example, by employing known, related art or later developed photolithography and etching methods with the assumption that the broad width portion and the narrow width portion are formed through the incorporated pattern, the scanning line according to the present aspect can be easily formed.

[0019] In another aspect of the electro-optical device of the present invention, the broad width portion has a portion connected to the narrow width portion.

[0020] According to this aspect, for example, the broad width portion includes the portion formed by connecting a conductive member and the like prepared separately to the narrow width portion. Even in this case, the broad width portion can be formed relatively easily.

[0021] In another aspect of the electro-optical device of the present invention, the scanning line extends in a direction intersecting the direction in which the channel area extends and the broad width portion extends in a single direction or bi-directionally in which the channel area extends.

[0022] According to this aspect, since the broad width portion extends in the single direction or bi-directionally in which the channel area extends, it is possible to more adequately adjust the arrangement of the thin-film transistor and the scanning line. Further, according to this aspect, since the gate electrode is adequately formed in accordance with the channel length, the electric field can be more effectively applied to the channel area.

[0023] Further, like the above, according to the aspect that the gate electrode, that is, the broad width portion is provided in the portion to be the channel area corresponding to the channel area, for example, the so-called self-aligned formation of the thin-film transistor (that is, formation of the source area and the drain area adjacent to the channel area through

an ion implantation process using the gate electrode as a mask) can be easily executed. However, in this case, strictly speaking, the channel area is formed by carrying out the ion implantation process after forming the broad width portion to be the gate electrode.

[0024] In another aspect of the electro-optical device of the present invention, the pixel electrodes are arranged in a matrix shape and the channel areas are formed in an intersecting area in which a first long gap extending through a space between pixel electrodes sandwiching of the scanning line and being adjacent to each other and a second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected.

[0025] This aspect is similar to the above mentioned aspect and is one of the aspects in which the operational effect of the present invention is exhibited most effectively.

[0026] That is, according to this aspect, the channel area of the thin-film transistor is formed in the intersecting area of the pixel electrodes arranged in a matrix shape. The intersecting area is an area in which the first long gap extending through a space between pixel electrodes sandwiching the scanning line and being adjacent to each other and the second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected in plan view. By such a configuration, it is difficult for light to enter the channel area.

[0027] Further, along with such an operational effect, since the scanning line has the broad width portion as the gate electrode is opposite to the channel area, the arrangement between the channel area (or the thin-film transistor) and the gate electrode (or the scanning line) can be determined most adequately and it is also possible to secure the adequate channel length and narrowness of the scanning line.

[0028] In this aspect, in particular, the narrow width portion is formed at a position deviated from a center of the first gap and the broad width portion, is formed at the center of the first gap in the intersecting area.

[0029] According to this configuration, the narrow width portion of the scanning line extends through the space between the adjacent pixel electrodes but does not exist at the center thereof and is formed at the position deviated from the center thereof. As a result, first, the enhancement in the quality of the displayed image can be obtained, especially for the liquid crystal display device that is an example of the electro-optical device, and the reason thereof is as follows.

[0030] That is, in the present aspect, when performing the rubbing process on a convex portion on the oriented film normally provided in the liquid crystal display device, in

particular, a convex portion formed by "height" of the narrow width portion, nonuniformities are usually generated in the convex portion. Further, it is considered that the degree of nonuniformity is different from each other in the portion associated with the rubbing up convex portion (that is, the direction ascending to the convex portion) and the portion associated with the rubbing down convex portion (that is, the direction descending from the convex portion).

[0031] More specifically, for example, it is more difficult to generate nonuniformity in the portion associated with the rubbing up convex portion than in the portion associated with the rubbing down convex portion.

[0032] Further, if the nonuniformity is left as it is, a poor orientation of the liquid crystal may be caused to result in the operation failure of the electro-optical devices. In the difference in the degree of nonuniformity between the rubbing-up process and the rubbing-down process, the latter has greater possibility to cause the bad orientation of the liquid crystal than the former.

[0033] It is significant that the narrow width portion of the present aspect is formed at a position deviated from the center of the first gap between the pixel electrodes. That is, if the narrow width portion is formed at the above-described position, the vertex of the convex portion caused by the narrow width portion is also formed at the position deviated from the center of the first gap, and this means that it is possible to form almost only half inclined surface of the convex portion on the area corresponding to the first gap, that is, to form only the portion associated with the rubbing-down on the area. Further, in this case, if the light-shielding film is provided corresponding to the first gap, it is possible to effectively shield only the portion associated with the rubbing-down, that is, to effectively shield the corresponding portion of the convex portion to be most influenced by the nonuniformity.

[0034] As a result, according to the present aspect, since the operation failure of the electro-optical device caused by nonuniformities can be substantially prevented or reduced, and the portion of the convex portion associated with the rubbing-up, which is not affected by nonuniformities, is able to transmit the light contributing to the image display. Thus, it is possible to enhance the opening ratio of pixel, that is, to provide a brightened image display. As a result, according to the present aspect, from the above-mentioned point of view, the enhancement in the display image can be obtained.

[0035] Further, by forming the narrow width portion at the position deviated from the center of the first gap, it is also possible to enhance the degree of freedom in designing

the electro-optical devices and to more effectively prevent or reduce light from entering the thin-film transistor. The reason thereof is as follows.

[0036] That is, in the present aspect, the narrow width portion extends through the first gap between the adjacent pixel electrodes, but does not exist at the center thereof. For this reason, by using the area in the first gap where the narrow width portion is not provided, in a plan view, it is possible to provide other wires, such as the capacitive line made up of the same film as the narrow width portion, in parallel to the narrow width portion. That is, the degree of freedom of design is increased.

[0037] Further, in the above-mentioned case, although the narrow width portion is deviated from the center thereof, it is possible to arrange the broad width portion as the gate electrode at the center of the gap, by adjusting the width of the broad width portion, for example, by broadening only one side or by broadening one side more than the other small side. Like the above, since the gate electrode can be arranged at a position advantageous to increase the light-shielding ability regardless of the position of the scanning line, or since the scanning line can be arranged at an arbitrary portion in the gap while arranging the gate electrode at the position advantageous for increasing the light-shielding ability, it is possible to realize a thin-film transistor having a high light-shielding ability while increasing the degree of freedom in arranging wires including the arrangement of the scanning lines.

[0038] In this configuration, further, the broad width portion may be formed at the center of the second gap in the intersecting area.

[0039] According to such construction, the channel area is formed at the position farthest from the adjacent or opposite corners of the electrodes in accordance with the above-described method, when four pixel electrodes are considered to be used. That is, it becomes very difficult for light to enter the channel area.

[0040] In another aspect of the electro-optical device of the present invention, grooves are formed in the substrate along the scanning lines, and the scanning lines are buried at least partially in the grooves directly or through an interlayer insulating film.

[0041] According to this aspect, since the scanning line is buried in the groove formed in the substrate, the generation of a step on the surface of the interlayer insulating film formed as the upper layer or on the surface of the pixel electrodes and the oriented film, etc. caused by the height of the scanning line itself can be prevented or reduced earlier. That is, the surface can be leveled very well. Then, if the surface of the oriented film is leveled, the rubbing process can be adequately performed for the orientation process and the orientated state of the liquid crystal molecules contacting the oriented film can be maintained

well. Therefore, according to the present aspect, since the possibility of bad orientation can be decreased and the light leakage caused by the bad orientation can be markedly prevented or reduced, it is possible to display a high-quality image.

[0042] In another aspect of the electro-optical device of the present invention, the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion not buried in the groove and extending along the scanning line in parallel to a buried portion, and a base of the pixel electrode is positioned high along the scanning line due to the presence of the non-buried portion.

[0043] According to this aspect, the narrow width portion has both the buried portion and the non-buried portion. Then, both of the buried portion and the non-buried portion extend along the scanning line and the base of the pixel electrode protrudes above along the scanning line due to the presence of the non-buried portion.

[0044] Through this construction, first, the effect associated with the above-described leveling can be similarly obtained by the buried portion. That is, the surface of the interlayer insulating film to be formed as the upper layer of the buried portion, or the surfaces of the pixel electrodes and the oriented film have the an excellent leveled feature, and thus it is possible to reduce the possibility of having the bad orientations.

[0045] Next, since the step including the convex portion along the scanning line is formed on the surface of the oriented film to be formed as the upper layer of the non-buried portion and the like, the above-described effects of leveling cannot be obtained by the non-buried portion. However, the following advantages can be obtained.

[0046] First, in electro-optical device according to the present invention, for the purpose of preventing or reducing deterioration of the liquid crystal, increasing the device life and reducing the cross-talk or flicker of the displayed image, a method of dividing the pixel electrodes into two groups and then inversely driving them in separate cycles may be employed. That is, a plurality of pixel electrodes including a first pixel electrode group to be inversely driven at a first period and a second pixel electrode group to be inversely driven at a second period compensatory with the first period, are arranged in a plain on the substrate. There are (i) the adjacent pixel electrodes to be driven with driving voltages of inverse polarities at the respective times in the inverse-driving, and (ii) the adjacent pixel electrodes to be driven with driving voltages of the same polarity at the respective times in the inverse driving. If the pixel electrodes corresponding to (i) are arranged in the direction along the data lines and the pixel electrodes corresponding to (ii) are arranged in the direction along the scanning lines, the pixel electrodes arranged in the direction along any one scanning line are

driven with one polarity and the pixel electrodes arranged in the direction along another scanning line adjacent to the any one scanning line are driven with an inverse polarity to the one polarity (referred to as "1H inverse driving").

[0047] However, in this case, between the pixel electrodes adjacent to each other along the data line, the horizontal electric field based on the driving voltages of inverse polarities is generated. Such horizontal electric field may interfere the electric field (may be referred to as vertical electric field in contrast to the horizontal electric field) generated between the pixel electrode and the opposing electrode, and as a result, it becomes difficult to obtain the orientation state of the liquid crystal molecules as desired, so that the image display may be affected.

[0048] Further, in the present aspect, in a case that such adverse effects may be caused, the convex portion formed on the base of the pixel electrode along the scanning line has a distinct significance.

[0049] That is, first, when the edge portions of the respective pixel electrodes are formed to be positioned on the step, the vertical electric field generated between the respective pixel electrodes and the opposing electrode is intensified compared to the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in the different pixel electrode group). That is, since the electric field generally intensifies as the distance between the electrodes becomes shorter, the edge portions of the pixel electrodes near the opposing electrode by the height of the step generates an intense vertical electric field. Second, whether the edge portions of the respective pixel electrodes are positioned on the step or not, the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in a different pixel electrode group) is weakened by the presence of the step in accordance with the dielectric constant, and even by reducing (replacing partially from the step) the volume of the electro-optical material through which the horizontal electric field passes, the effect that the horizontal electric field has on the electro-optical material can be reduced. Therefore, the operation failure from the electro-optical material, such as the bad orientation of the liquid crystal by the horizontal electric field caused by the inverse driving method, can be reduced. At this time, as described above, the edge portions of the pixel electrodes may be or not be positioned on the step and may be positioned on the inclined step or on an almost vertical side surface thereof.

[0050] In addition, since the light-shielding film to conceal the operation failure caused by the electro-optical material, can be formed small, it is also possible to increase the

opening ratios of the respective pixels without having the bad image display, caused by the light leakage, generated.

[0051] As described above, according to the present aspect, first, due to the presence of the buried portion, the effects associated with the above-described leveling can be obtained, and second, by forming intentionally the step including the convex portion along the scanning line by the presence of the non-buried portion, the generation of the horizontal electric field can be prevented or reduced.

[0052] In another aspect of the electro-optical device of the present invention, a capacitor electrode on a pixel potential side constituting a storage capacitor connected to the pixel electrode and a capacitive line having capacitor electrode on a fixed potential side arranged constituting the storage capacitor arranged opposing the capacitor electrode on the pixel potential side through a dielectric film, may be further provided. The capacitive line has a main line portion extending along the scanning line and a portion extending along the data line, and a width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line.

[0053] According to this aspect, since the storage capacitor, having a construction such that the capacitor electrode on the pixel potential side and the capacitor electrode on the fixed potential side are arranged opposite to each other, is connected to the pixel electrode, the voltage of the image signal written in the pixel electrode can be maintained for a long time. In particular, in the present aspect, since the width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line, it is possible to further lower the resistance of the capacitive line. Further, in the present aspect, since a low resistance of the capacitive line can be realized as described above, from the point of view of the whole device, the narrowness of the capacitive line and further narrowness of the storage capacitor can be accomplished, and as a result, it is possible to enhance the opening ratio. In the "narrowness of the capacitive line", since the capacitive line itself has a width equal to or "broader than" the width of the data line on the surface, it may appear to be a contradiction, but the broad width and the narrow width should be determined from the relative relationship between the capacitive line and the data line, such that from the point of view of the whole device, the "narrowness of the capacitive line" can be accomplished, compared to the related art. Furthermore, in the broad width and narrow width described above or the "broader than" to be described in the present invention, the discrete values of the width can be adequately determined theoretically, experimentally, experientially or by simulation.

[0054] Further, according to the present aspect, it is possible to effectively prevent or reduce the light from entering the thin-film transistor, in particular the channel area thereof, compared to the related art, as well as obtaining the above-described low resistance. This is because, as described above, although in the conventional art, the light reflected from the back of the data line and the like becomes a stray light and thus may enter the thin-film transistor, but according to the present aspect, the possibility that the advance of such stray light is shielded by the capacitive line formed in the width equal to or broader than that of the data line is increased.

[0055] From the above, according to the present invention, the problems, such as the cross-talk or burn-in that were prevalent in the related art, can be reduced by the low resistance of the capacitive line. Further, since the light leak current in the thin-film transistor is reduced, it is possible to display a high quality image.

[0056] Further, in the present invention, since the portion extending along the data line exists in the capacitive line, the area of the storage capacitor can be increased. This markedly contributes to the image display having high quality.

[0057] Furthermore, in order to more effectively accomplish the light-shielding function described above, materials having a good light-shielding feature may be employed for the capacitive line. For example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one from Al (aluminum), Cu (copper), Ti (titan), Cr (chrome), W (tungsten), Ta (tantalum), and Mo (molybdenum) can be adequately employed. Further, in addition to the above, for example, light-absorbing materials such as poly-silicon can be employed.

[0058] In this aspect, a portion overlapping the thin-film transistor in the data line may be formed locally broad, and a width of the portion extending along the data line in the capacitive line may be broader than that of the portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

[0059] By such a construction, the portion overlapping the thin-film transistor in the data line is formed locally broad. Then, the width of the portion formed broad is equal to that of the portion extending along the data line in the above-described capacitive line. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Thus, the light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.

[0060] More specifically, for example, when the capacitive line is made up of metal having a high melting point, the capacitive line can independently have the light-shielding

ability that the transmittance thereof is about 0.1% (2 or more in OD (Optical Density)). However, if the silicide forming process is performed on the capacitive line, the composition thereof is varied and thus the light-shielding ability may be reduced. In this case, only the light-shielding ability having the transmittance of 0.1% or more may be obtained.

[0061] However, in the present aspect, the data line overlapping the capacitive line formed of such a metal film having a high melting point is further provided. If the construction for performing the light shielding of the thin-film transistor by overlapping the capacitive line and the data line is employed, the light-shielding ability corresponding to the added value of these transmittances can be obtained. For example, when the data line is made up of aluminum, etc., the light-shielding ability with a transmittance of 0.001% or less (4 or more in the OD value) can be accomplished.

[0062] Further, in the present aspect, in particular, that the broad width of the portion extending along the data line in the capacitive line is broad means that it is broader than that of the portion not formed broad in the data line.

[0063] Also, a portion overlapping the thin-film transistor in the data line is formed locally broad, and a width of the portion extending along the data line in the capacitive line is broader than that of the portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

[0064] According to this aspect, the portion overlapping the thin-film transistor in the data line is formed locally broad. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Therefore, the light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.

[0065] Furthermore, in the present aspect, in particular, the width of the portion extending along the data line in the capacitive line is formed narrower than that of the data line. That is, in the portion, the width of the data line is narrower than that of the capacitive line. From this construction, for example, when the data line is made up of aluminum having a high light reflexivity, a stray light generated by reflecting the incident light by any element in the electro-optical device, a light returning to the electro-optical device after a light emitted from the electro-optical device is reflected by any element outside of the electro-optical device, or in a projection type display device, such as a color-displayable liquid crystal projector including a plurality of electro-optical devices, a light emitted from other electro-optical device and generated by returning to the electro-optical device is reflected by the data

line to thereby prevent the stray light from being increased. This is because the portion of the data line formed broad is relatively narrower than the capacitive line.

[0066] In this aspect that has the data line having a portion overlapping the thin-film transistor formed broad, the capacitive line is arranged at the overlapped position between the thin-film transistor and the data line, and the data line may be constructed such that the portion provided with a contact hole to connect to the thin-film transistor is formed broad in addition to the portion overlapping the thin-film transistor.

[0067] From this construction, even when the capacitive line as the light-shielding film could is not provided, the decrease in the light-shielding ability can be compensated by forming broad the data line for the contact hole.

[0068] Alternatively, for each thin-film transistor, the data line is formed continuously broad from the portion overlapping the thin-film transistor to the portion in which the contact hole is provided.

[0069] From this construction, the light shielding of the thin-film transistor can be more securely accomplished.

[0070] Further, the portion formed broad in the portion overlapping the thin-film transistor and the portion formed broad in the portion in which the contact hole is provided may be separately formed broad. If arranging the portion overlapping the thin-film transistor and the portion in which the contact hole is provided close to each other and forming them continuously broad as in the present aspect, since the area to be formed broad need not be exceedingly broad, it is advantageous from the point of view of not increasing the inner reflection.

[0071] In another aspect of the electro-optical device of the present invention, another substrate opposing the substrate through an electro-optical material and a light shielding film formed on the another substrate may be further provided, and the width of the data line and the width of a portion extending along the data line in the capacitive line are narrower than that of the light-shielding film.

[0072] From this aspect, if it is assumed that the light is entered from another substrate, the laminated structure of the light-shielding film, the data line and the capacitive line in the order from the light incidence side can be constructed. The width of the former is broader than those of the latter two. That is, the advance of the incident light is blocked by the broader light-shielding film, and only the light passing through it reaches the data line and the capacitive line. Further, when the light passing through the light-shielding film reaches the data line and the capacitive line, the data line and the capacitive line can be expected to

perform the above-described light-shielding function. In short, according to the present aspect, it is possible to enhance the light resistance of the thin-film transistor and to reduce the generation of the light leakage.

[0073] Further, if the pixel electrodes are arranged in a matrix shape, the "light-shielding film" in the present aspect may be formed in a stripe shape or a lattice shape to extend through spaces between the pixel electrodes. Furthermore, according to circumstances, the light-shielding film may be formed as a laminated structure made of, for example, a light-absorbing material, such as chrome or chrome oxide, and a light-reflecting material, such as aluminum.

[0074] An electronic apparatus of the present invention may include the above-described electro-optical device (including various aspects).

[0075] According to the electronic apparatus of the present invention, for example, since it includes the electro-optical device capable of adequately adjusting the arrangement between the thin-film transistor and the scanning line, it is possible to realize various electronic apparatuses, such as a liquid crystal projector, a liquid crystal television, a portable phone, an electronic pocket book, a word processor, a view finder type or monitor direct vision-type videotape recorder, a work station, a video phone, a POS terminal, and a touch panel, capable of precise operation of the thin-film transistor and high quality image display, for example.

[0076] The above effects and other advantages of the present invention will be more apparent from the following exemplary embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0077] FIG. 1 is a schematic circuit diagram illustrating an equivalent circuit of various elements, wirings and the like provided in a plurality of pixels, having a matrix shape, constituting an image display area in an electro-optical device according to an exemplary embodiment of the present invention;

[0078] FIG. 2 is a plan view of a group of adjacent pixels in a TFT array substrate where data lines, scanning lines, pixel electrodes are formed in the electro-optical device according to an exemplary embodiment of the present invention;

[0079] FIG. 3 is a sectional view taken along plane A-A' in FIG. 2;

[0080] FIG. 4 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 2;

[0081] FIG. 5 is a plan view illustrating another exemplary embodiment in which the arrangement of the scanning lines and the TFTs is different from that in FIG. 2;

[0082] FIG. 6 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 5;

[0083] FIG. 7 is a sectional view taken along plane B-B' in FIG. 5;

[0084] FIG. 8 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the scanning lines are buried in the grooves;

[0085] FIG. 9 is a sectional view illustrating a profile of a narrow width portion of the scanning lines shown in FIG. 8;

[0086] FIG. 10 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and a part of the scanning lines are buried in the grooves;

[0087] FIG. 11 is a sectional view illustrating a profile of a narrow width portion of the scanning line shown in FIG. 10;

[0088] FIG. 12 is a sectional view taken along plane T-T' in FIG. 10;

[0089] FIGS. 13(a) and 13(b) are schematics explaining the generation of a horizontal electric field;

[0090] FIG. 14 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the narrow width portion of the scanning line is deviated from the center of a first gap;

[0091] FIG. 15 is a sectional view taken along plane T-T' in FIG. 14;

[0092] FIG. 16 is a plan view illustrating another exemplary embodiment in that a shape of the data line is different from that in FIG. 2;

[0093] FIG. 17 is a sectional view taken along plane P-P' in FIG. 16;

[0094] FIG. 18 is a sectional view taken along plane Q-Q' in FIG. 16;

[0095] FIG. 19 is a sectional view taken along plane R-R' in FIG. 16;

[0096] FIG. 20 is a plan view where the TFT array substrate of the electro-optical device according to the exemplary embodiment of the present invention is viewed from the opposing substrate side along with the respective elements formed thereon;

[0097] FIG. 21 is a sectional view taken along plane H-H' in FIG. 20;

[0098] FIG. 22 is a schematic sectional view illustrating a color liquid crystal projector that is an example of a projection type color display apparatus as an exemplary embodiment of an electronic apparatus of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0099] Preferred exemplary embodiments of the present invention are explained with reference to the drawings. In following exemplary embodiments, an electro-optical device of the present invention is applied to a liquid crystal device.

[0100] First, a construction of a pixel part in the electro-optical device according to an exemplary embodiment of the present invention is explained with reference to FIGS. 1 to 4. Fig. 1 is a schematic that shows an equivalent circuit of various elements, wirings and the like in a plurality of pixels formed in a matrix shape constituting an image display area 10a of the electro-optical device. FIG. 2 is a plan view of a group of a plurality of pixels adjacent to each other on a TFT array substrate in which data lines, scanning lines, pixel electrodes and the like are formed. Further, FIG. 3 is a sectional view taken along plane A-A' in FIG. 2. Further, in FIG. 3, in order for each layer and each member to have recognizable sizes in the drawing, different scales are applied to each layer and each member. Furthermore, FIG. 4 is a plan view illustrating shapes of only the scanning lines extracted from FIG. 2.

[0101] In FIG. 1, in the plurality of pixels formed in a matrix shape constituting the image display area of the electro-optical device according to the present exemplary embodiment, a pixel electrode 9a and a TFT 30 to control switching of the pixel electrode 9a are formed, respectively, and data lines 6a supplied with image signals are electrically connected to sources of the TFTs 30. Image signals S1, S2, ..., Sn to be, in this order, written may be sequentially supplied to the data lines 6a, or may be supplied to each group which has a plurality of data lines 6a adjacent to each other.

[0102] Further, scanning lines 330a are electrically connected to gates of the TFTs 30 and at a predetermined timing, scanning signals G1, G2, ..., Gn are pulse-like applied to the scanning lines 330a in that order. The pixel electrodes 9a are electrically connected to drains of the TFTs 30, and by closing switches of the TFTs 30, that is, switching elements for a predetermined time interval, the image signals S1, S2, ..., Sn supplied from the data lines 6a are written at a predetermined timing.

[0103] A predetermined level of the image signals S1, S2, ..., Sn which have been written through the pixel electrodes 9a to a liquid crystal that is an example of an electro-optical material are maintained for a predetermined time interval between the pixel electrode 9a and an opposing electrode formed on an opposing substrate. The liquid crystal modulates light by varying orientation or order of molecules according to the applied voltage level, and thus it is possible to execute the gradation display. If it is in a normally-white mode, transmittance for the incident light is decreased in accordance with the voltage applied in a

unit of pixel, and if it is in a normally-black mode, the transmittance for the incident light is increased in accordance with the voltage applied in a unit of pixel. Therefore, as a whole, light having a contrast responsive to the image signals is emitted from the electro-optical device.

[0104] In order to reduce or prevent the maintained image signals from being leaked, a storage capacitor 70 is added in parallel to a liquid crystal capacitor formed between the pixel electrode 9a and the opposing electrode.

[0105] A more specific construction of the electro-optical device in which the above-described circuit operation is executed by using the data lines 6a, the scanning lines 330a, the TFTs 30 and the like is explained with reference to FIGS. 2 and 3.

[0106] First, the electro-optical device according to the present exemplary embodiment, as shown in FIG. 3 which is a sectional view taken along plane A-A' in FIG. 2, includes a TFT array substrate 10 and a transparent opposing substrate 20 arranged opposite thereto. The TFT array substrate 10 is made of, for example, a quartz substrate, a glass substrate or a silicon substrate, and the opposing substrate 20 is made of, for example, a glass substrate or a quartz substrate.

[0107] As shown in FIG. 3, the TFT array substrate 10 is provided with a pixel electrode 9a, and an upper portion of the pixel electrode is provided with an oriented film 16 which has been subjected to a predetermined orientation process, such as a rubbing process. The pixel electrode 9a is made of, for example, a transparent conductive film, such as an ITO (Indium Tin Oxide) film.

[0108] The opposing substrate 20 is provided over the whole surface thereof with an opposing electrode 21, and a lower portion of the electrode is provided with an oriented film 22 which has been subjected to a predetermined orientation process, such as a rubbing process. The opposing electrode 21 is made of, for example, a transparent film, such as an ITO film.

[0109] Next, in FIG. 2, a plurality of pixel electrodes 9a (profiles thereof are indicated by dotted lines 9a') are provided in a matrix shape on the TFT array substrate 10 of the electro-optical device, and data lines 6a of aluminum films and scanning lines 330a of poly-silicon films are provided along horizontal and vertical boundaries of the pixel electrodes 9a.

[0110] Each scanning line 330a is arranged opposite to a channel area 1a' indicated by oblique lines area extending from lower left to upper right in the semiconductor layer 1a of a poly-silicon film and functions as a gate electrode. That is, in portions where the

scanning lines 330a and the data lines 6a are intersected, TFTs 30 to switch pixels where broad width portions 331a (to be explained later) of the scanning lines 330a are arranged opposite to the channel areas 1a' as gate electrodes are provided. In other words, TFTs 30 in the present exemplary embodiment, in particular, the channel areas 1a' thereof are formed in intersecting areas of the plurality of pixel electrodes 9a arranged in a matrix shape. The intersecting area means an area where, in plan view, a first long gap (X direction in FIG. 2) extending through a space between adjacent pixel electrodes 9a sandwiching the scanning lines therebetween and a second long gap (Y direction in FIG. 2) extending through a space between adjacent pixel electrodes sandwiching the data line 6a therebetween, are intersected.

[0111] More specifically, with reference to FIG. 2, the intersecting area corresponds to, for example, a position farthest from each of a lower-right corner of the pixel electrode 9a shown on the upper-left side of the plan view, a lower-left corner of the pixel electrode 9a shown on the upper-right side, an upper-right corner of the pixel electrode 9a shown on the lower-left side and an upper-left corner of the pixel electrode 9a shown on the lower-right side of the plan view. Since the TFT 30 is formed at such position, it is difficult for an incident light to directly enter the channel area 1a' of the TFT.

[0112] The TFT 30, as shown in FIG. 3, has an LDD (Lightly Doped Drain) structure, and includes a channel area 1a' of the semiconductor layer 1a where a channel is formed by an electric field from the scanning line which functions as a gate electrode as described above, an insulating film 2 having a gate insulating film to insulate the scanning line 330a from the semiconductor layer 1a, a low-concentration source area 1b, a low-concentration drain area 1c, a high-concentration source area 1d and a high-concentration drain area 1e.

[0113] Further, although it is preferable that the TFT 30 has the LDD structure as shown in FIG. 3, the TFT 30 may have an offset structure in which impurities are prevented or substantially prevented from being infiltrated into the low-concentration source area 1b and the low-concentration drain area 1c, or may be a self-alignment type TFT to infiltrate impurities at high concentration using the gate electrode constituting a part of the scanning line 330a as a mask to automatically form the high-concentration source area and the high-concentration drain area. Furthermore, although, in the present exemplary embodiment, the TFT 30 has a single gate structure where only one gate electrode of the TFT 30 for pixel switching is disposed between the high-concentration source area 1d and the high-concentration drain area 1e, the TFT may have a dual, triple or more gate structure where two or more gates are disposed therebetween. Furthermore, the semiconductor layer 1a

constituting the TFT 30 is not limited to the poly-silicon film, but may be made of an amorphous silicon film or a monocrystalline silicon film. A related art, later developed, or known method, such as a pasting method can be employed in formation of the monocrystalline silicon film. By employing the monocrystalline silicon film for the semiconductor layer 1a, it is possible to promote a high performance of the peripheral circuits.

[0114] In the present exemplary embodiment, for the scanning line 330a serving as the gate electrode of the TFT 30, a portion serving as the gate electrode, that is, a portion facing the channel area 1a' of the TFT 30 is formed broader than the other portion, as shown in FIG. 2. That is, in FIG. 2, the scanning line 330a has a broad width portion 331a extending in the Y direction in FIG. 2 to correspond to the channel area 1a' extending in the Y direction in FIG. 2 and a narrow width portion 332a extending through a space between the adjacent pixel electrodes 9a. In FIG. 4, for the purpose of simplifying the illustration, only the shape pattern of the scanning line 330a is shown.

[0115] In this connection, in the present exemplary embodiment, the broad width portion 331a is lengthened from the narrow width portion 332a. That is, the broad width portion 331a and the narrow width portion 332a are integrally formed. Such a shape can be easily formed, for example, by using a related art, later developed, or known photolithography and etching, on the assumption that a pattern having an integrated shape 332a (see FIG. 4) composed of the broad width portion 331a and the narrow width portion 332a is formed. However, the present invention is not limited to such shape, and includes, for example, even shapes where the broad width portion 331a is formed by connecting other conductive member prepared separately to the narrow width portion 332a, within the scope thereof.

[0116] The storage capacitor 70 shown in FIG. 1 is constructed such that a junction layer 71 as the capacitor electrode on the pixel potential side connected to the high-concentration drain area 1e of the TFT 30 and the pixel electrode 9a and a part of the capacitive line 300 as the capacitor electrode on the fixed potential side are arranged opposite to each other via an dielectric film 75, as shown in FIG. 3. By the storage capacitor 70, it is possible to markedly enhance the potential maintenance characteristics in the pixel electrode 9a.

[0117] The junction layer 71 is made up of, for example, the conductive poly-silicon film and serves as a capacitor electrode on the pixel potential side. However, similar to the capacitive line 300 to be explained in detail below, the junction layer 71 may be made

of a single layer film or multi-layer film containing metal or alloy. In addition to the function as a capacitor electrode on the pixel potential side, the junction layer 71 also has a function of connecting the pixel electrode 9a and the high-concentration drain area 1e of the TFT 30 to each other through contact holes 83 and 85.

[0118] By using such junction layer 71, even if the distance between layers is as long as, for example, 2000nm, both layers can be connected well to each other through serial contact holes having two relatively small diameters while avoiding the technical difficulty of connecting both layers to each other through one contact hole, so that an opening ratio of pixel can be increased. Further, in opening the contact hole, it is helpful to prevent or reduce punchthrough in etching.

[0119] The capacitive line 300 is made of, for example, a conductive film containing metal or alloy, and serves as a capacitor electrode on the fixed potential side. The capacitive line 300 is formed overlapping an area to form the scanning line 330a from a plan view, as shown in FIG. 2. More specifically, the capacitive line 300 has a main line portion extending along the scanning line 330a, a protruding portion protruded upwardly in the Y direction along the data line 6a from a portion intersecting the data line 6a and a constricted portion where the portion corresponding to the contact hole 85 is slightly constricted. The protruding portion contributes to increase in the area to form the storage capacitor 70 by using the area on the scanning line 330a and the area below the data line 6a.

[0120] Further, the capacitive line 300 is made of, for example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one of metals having high melting point, such as Ti, Cr, W, Ta, Mo, and in addition to the function as a capacitor electrode on the fixed potential side of the storage capacitor 70, the capacitive line 300 has a function as a light-shielding layer to shield the TFT 30 from the incident light on the upper side of the TFT 30. However, the capacitive line 300 may have a multi-layer structure in which a first film made of a conductive poly-silicon film and the like and a second film made of a metal silicide film containing metal and the like having high melting point are stacked.

[0121] Furthermore, preferably, the capacitive line 300 extends from the image display area in which the pixel electrodes 9a are arranged to peripheries thereof, and is electrically connected to a potentiostatic source to be a fixed potential. Such potentiostatic source may be a potentiostatic source, such as a plus power source or a minus power source supplied to a data line driving circuit to be explained later, or may be a potentiostatic source supplied to the opposing electrode 21 of the opposing substrate 20.

[0122] A dielectric film 75, as shown in FIG. 3, is constructed of a silicon oxide film such as a HTO (High Temperature Oxide) film or a LTO (Low Temperature Oxide) film having, for example, a relatively thin thickness of about 5~200nm, or a silicon nitride film. From the point of view of increasing the capacitance of the storage capacitor 70, the dielectric film 75 should be preferably as thin as possible as long as the reliability of the film is sufficiently maintained.

[0123] In FIGS. 2 and 3, in addition, the lower side of the TFT 30 is provided with a lower light-shielding film 11a. The lower light-shielding film 11a is patterned in a lattice shape, and as a result, the opening area of each pixel is defined. Further, the opening area may be defined by the intersection of the data line 6a extending in the Y direction in FIG. 2 and the capacitive line 300 extending in the X direction in FIG. 2. Furthermore, similar to the case of the above-described capacitive line 300, the lower light-shielding film 11a may be formed extending from the image display area to the peripheries thereof to be connected to a potentiostatic source so that the potential variation has no adverse effects on the TFT 30.

[0124] Further, a base insulating film 12 is provided below the TFT 30. In addition to the function of insulating the TFT 30 from the lower light-shielding film 11a, since the base insulating film 12 is formed on the whole surface of the TFT array substrate 10, the base insulating film 12 has a function of preventing or reducing the characteristic variation of the TFT 30 for pixel switching caused by rough polished surface of the TFT array substrate 10 or contaminants left after washing.

[0125] In addition, a first interlayer insulating film 41 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 83 communicating with the high-concentrating drain area 1e, respectively, is formed on the scanning line 330a.

[0126] The junction layer 71 and the capacitive line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 85 communicating with the junction layer 71 are formed respectively on the junction layer 71 and the capacitive line 300.

[0127] Furthermore, in the present exemplary embodiment, by baking the first interlayer insulating film 41 at about 1000°C, activation of ions injected into the poly-silicon film constituting the semiconductor layer 1a or the scanning line 330a may be intended. On the other hand, by not baking the second interlayer insulating film 42, relief of stress occurring in the vicinity of the interface of the capacitive line 300 may be intended.

[0128] The data line 6a is formed on the second interlayer insulating film 42, and above them a third interlayer insulating film 43 which has a contact hole 85 communicating the junction layer 71 is formed.

[0129] The surface of the third interlayer insulating film 43 is leveled by means of CMP (Chemical Mechanical Polishing) process, and as a result, the orientation failure of the liquid crystal layer 50 caused by a step generated by various wirings or elements below the third interlayer insulating layer 73 can be reduced.

[0130] However, in place of performing the leveling process for the third interlayer insulating film 43, or in addition to it, a groove, in at least one of the TFT array substrate 10, the base insulating film 12, the first interlayer insulating film 41 or the second interlayer insulating film 42, can be formed to buried the wirings, such as the data line 6a or the TFT 30 to perform the leveling process.

[0131] According to the electro-optical device of the present exemplary embodiment as constructed like the above, since the scanning line 330a has the broad width portion 331a and the narrow width portion 332a and the broad width portion 331a is formed to face the channel area 1a' of the TFT 30, the arrangement between the TFT 30 and the scanning line 330a can be easily adjusted or determined.

[0132] For example, the arrangement between the TFTs 30 and the scanning lines 330a in FIG. 2 described above shows an example of a suitable arrangement responsive to the requirement to effectively prevent or substantially prevent light from entering the channel areas 1a' of the TFTs 30. In addition, for example, the arrangements shown in FIGS. 5 and 6 can be implemented. FIG. 5 is a diagram with the same purpose as FIG. 2, in which an arrangement of the scanning lines and the TFTs is different from that in FIG. 2, and FIG. 6 illustrates only a shape pattern of the scanning lines shown in FIG. 5, similar to FIG. 4.

[0133] In FIGS. 5 and 6, the scanning lines 330a', more specifically, the narrow width portions 332a' are formed at positions deviated from the center of a first long gap extending through a space between the adjacent pixel electrodes 9a sandwiching the scanning lines 330a' therebetween. Further, the broad width portions 331a' are formed to be protruded only upwardly in the Y direction in FIG. 5 and 6. Furthermore, the arranged positions of the channel areas 1a', that is, the arranged positions of the broad width portion 331a' are similar to those in FIG. 2.

[0134] This arrangement can enhance the quality of display image. The reason thereof is as follows. That is, in the electro-optical device according to the present invention, as described above, the oriented film 16 is provided on the pixel electrodes 9a, and on the

surface of the oriented film 16, unevenness due to the "height" of various elements formed below the oriented film 16 can exist. The above-described "various elements" include the scanning lines 330a' of the present exemplary embodiment. FIG. 7 is a sectional view taken along plane B-B' in FIG. 5, in which a convex portion 501 caused by the "height" of the narrow width portion 332a' of the scanning line 330a' is formed on the oriented film 16.

[0135] When the convex portion 501 is generated, there is a possibility of further generating nonuniformity in the above-described rubbing process performed on the oriented film 16. This nonuniformity may cause the bad orientation of the liquid crystal and thus the operation failure of the electro-optical device. Therefore, in the related art, by providing the light-shielding film in the vicinity of the above-described convex portion 501, shielding of the incident light is made possible. That is, the incident light reaching the light-shielding film is reflected or absorbed by the light-shielding film and thus does not contribute to the image display.

[0136] At this time, it is important that the above-described light-shielding film should be provided while satisfying the requirements to enhance the pixel opening ratio. That is, when the light-shielding film is provided only to correspond to the convex portion 501, it may unnecessarily worsen the pixel opening ratio to deteriorate the brightness of image. When the light-shielding film is provided only in a part of the convex portion 501, sufficient light-shielding cannot be accomplished and may cause the deterioration of the contrast ratio. In addition, the influence of the nonuniformity in the convex portion 501 may lead to the operation failure of the electro-optical device.

[0137] In the present exemplary embodiment, it has been paid attention to the fact that the nonuniformity are generated in the convex portion 501, more specifically, that the portion (hereinafter, "rubbing-up portion 501a" in Fig. 7) associated with rubbing up the convex portion 501 (that is, the direction ascending the convex portion 501) and the portion (hereinafter "rubbing-down portion 501b" in Fig. 7) associated with rubbing down the convex portion 501 (that is, the direction descending the convex portion 501), have nonuniformity different from each other.

[0138] More specifically, for example, it has been paid attention to the fact that it is more difficult to generate the nonuniformity in the rubbing-up portion 501a than in the rubbing-down portion 501b, that is, the rubbing-down portion 501b has the higher possibility of causing the bad orientation of the liquid crystal.

[0139] In the present exemplary embodiment, it is important that the narrow width portions 332a' adjacent in the direction of the scanning lines 330a' in FIG. 5 are formed at the

position deviated from the center (see the two-dotted chain line in FIG. 7) between the pixel electrodes 9a. That is, by forming the narrow width portion 332a' at the position shown in FIG. 7, a vertex 501P of the convex portion 501 caused by the narrow width portion 332a' is also formed at the position deviated from the center between the adjacent pixel electrodes 9a. This means that it is possible to construct only almost half of the sloping surface of the convex portion 501 on the area corresponding to the first gap, that is, the rubbing-down portion 501b on the area. Further, in this case, as shown in FIG. 7, by providing the light-shielding capacitive line 300 and the junction layer 71 corresponding to the space between the adjacent pixel electrodes 9a, it is possible to effectively shield only the rubbing-down portion 501b, that is, to effectively shield the corresponding portion of the convex portion 501 expected to be most influenced by the nonuniformity.

[0140] As a result, according to the present exemplary embodiment, since the operation failure of the electro-optical device caused by the nonuniformity can be substantially prevented, and since the rubbing-up portion 501a of the convex portion 501 is not expected to be influenced by the nonuniformity remains to transmit the light contributing to the image display, it is possible to enhance the pixel opening ratio, that is, to maintain the bright image. Consequently, according to the present embodiment, from the above-described point of view, an enhancement in the quality of the display image can be obtained.

[0141] Further, by forming the narrow width portion 332a' at the position deviated from the center of the first gap, it is possible to enhance the degree of freedom in the design of the electro-optical device and to effectively prevent or substantially prevent the light from entering the TFT 30. The reason thereof is as follows.

[0142] That is, although the narrow width portion 332a' in the present exemplary embodiment extends through the first gap between the adjacent pixel electrodes 9a, it does not exist at the center thereof. For this reason, for example, by using an area not provided with the narrow width portion 332a' in the first gap, other wirings such as the capacitive line 300 made of the same film as the narrow width portion 332a' can be formed parallel to the narrow width portion 332a' from a plan view. That is, the degree of freedom in design can be increased.

[0143] Further, in the above-described case, although the narrow width portion 332a' is deviated from the center line, by adjusting the width of the broad width portion 331a', for example, by broadening only one side thereof or by broadening one side thereof more than the other side, it is possible to arrange the broad width portion 331a' as the gate electrode at the center of the gap. In the present exemplary embodiment, as shown in FIGS. 5 and 6, it

can be understood that the broad width portion 331a' is broadened toward only one side. Hence, since the gate electrode can be arranged at a position advantageous to enhance the light-shielding ability irregardless of the position of the scanning line 330a', or since the scanning line 330a' can be arranged at an arbitrary position in the gap while arranging the gate electrode at a position advantageous for improving the light-shielding ability, it is possible to increase the degree of freedom in an arrangement of wirings, such as an arrangement of the scanning line 330a' and to obtain the TFT 30 originally having a substantially high light-shielding ability.

[0144] In short, in the embodiment shown in FIGS. 5 and 6, while satisfying the requirements to enhance the quality of the display image, enhancing the degree of freedom in design and decreasing the light leak current in the TFT 30, it is possible to adequately adjust/determine the arrangement between the channel area 1a' (or the TFT 30) and the gate electrode (or the scanning line 330).

[0145] As described above, according to the electro-optical device of the present exemplary embodiment, since the scanning line, as the gate electrode, has the broad width portion and the narrow width portion, while satisfying the above various requirements or a general requirement, such as high precision of the electro-optical device itself, it is possible to adequately adjust/determine the arrangement between the channel area (or the TFT) and the gate electrode (or the scanning line).

(Second exemplary embodiment)

[0146] Now, a second exemplary embodiment of the present invention is explained with reference to FIGS. 8 to 11. FIGS. 8 and 10 are plan views illustrating another exemplary embodiment different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10 and at least a part of the scanning line is buried in the groove. FIGS. 9 and 11 are sectional views illustrating a profile of the narrow width portion of the scanning line according to the second exemplary embodiment, respectively (FIG. 9 corresponds to FIG. 8, and a section taken along a line Z1-Z1' in FIG. 8 corresponds to a section taken along plane Z1-Z1' in FIG. 9. Further, FIG. 11 corresponds to FIG. 10, and a section taken along plane Z2-Z2' in FIG. 10 corresponds to a section taken along plane Z2-Z2' in FIG. 9). Further, FIG. 12 is a sectional view taken along plane T-T' in FIG. 10. Furthermore, since the basic construction and operation, etc., of the electro-optical device of the second exemplary embodiment are similar to those of the first exemplary embodiment, explanation about distinctive portions in the second exemplary embodiment are mainly described below. Furthermore, the reference numerals in FIGS. 8 and 12 indicate the same elements as in

FIGS. 1 to 7 referred to in the above description, when they indicate substantially equivalent elements.

[0147] First, in one aspect of the second exemplary embodiment, as shown in FIGS. 8 and 9, a groove 3G1 is formed along the scanning line in the TFT array substrate 10. The groove 3G1 is formed except for the area where the semiconductor layer 1a of the TFT 30 is formed. By this construction, in consideration of only the grooves, the grooves 3G1 are arranged in a matrix shape from a plan view (see FIG. 8). Further, a scanning line 340a is formed such that the narrow width portion 342a thereof is entirely buried in the groove 3G1 (see FIG. 9).

[0148] In another aspect of the second embodiment, as shown in FIGS. 10 and 11, a groove 3G2 is formed on the TFT array substrate 10, similarly to the groove 3G1. However, preferably, a groove 3G2 is formed slightly narrower than the groove 3G1. Further, a narrow width portion 352a of the scanning line 350a is formed along the groove 3G2. The narrow width portion 352a has a buried portion 352aB of which a part is buried in the groove 3G2 and a non-buried portion 352aNB which is not buried in the groove 3G2 and extends parallel to the buried portion 352aB. The non-buried portion 352aNB is formed on the surface of the TFT array substrate 10.

[0149] Further, in one aspect and another aspect of the second exemplary embodiment, as shown in FIGS. 8 and 10, a groove 6G1 is formed in the TFT array substrate 10 along the data line. Furthermore, the data line 6a is formed to be entirely buried in the groove 6G1. In addition, the semiconductor layer 1a is also formed to be entirely buried in the groove 6G1.

[0150] According to the electro-optical device of the second exemplary embodiment constructed as above, the following effects can be obtained. First, since the whole part or a part of both of the scanning lines 340a and 350a are buried in the grooves 3G1 or 3G2, as shown in FIGS. 9 and 11, in this buried portion, the surface height of the base insulating film 12 and the height of the buried portion 352aB of the scanning line 340a and the scanning line 350a are almost equal to each other to maintain the leveling feature. By this, the leveling feature of the first to third interlayer insulating film 41 to 43 formed as the upper layers of the scanning lines 340a and 350a, or the pixel electrode 9a and the oriented film 16 can be well obtained. Therefore, in the second exemplary embodiment, for example, since a step along the narrow width portion 342a or the buried portion 352aB does not substantially appear on the surface of the oriented film 16, the rubbing process can be very suitably performed on the oriented film 16 and the bad orientation can be drastically

prevented or reduced. Furthermore, an effect can be obtained that the light leakage caused by the bad orientation and deterioration of the image quality based on the light leakage.

[0151] Such effects on the portion along the data line 6a can be obtained because of the existence of the groove 6G1.

[0152] Further, in FIGS. 10 and 11, in particular, because of the existence of the non-buried portion 352aNB, the following effects can be obtained. The effects are explained in detail below.

[0153] First, in the electro-optical device of the present exemplary embodiment, generally in order to prevent or reduce deterioration of the electro-optical material caused by the application of DC voltage and to prevent or reduce the cross-talk or flicker in the displayed image, an inverse driving method of inverting the polarities of voltages applied to the respective pixel electrodes 9a in a predetermined rule may be employed. More specifically, so-called "1H inverse driving method" is explained below.

[0154] First, as shown in FIG. 13(a), during the time to display image signals for the n-th field (n is a natural number) or frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is driven with the same polarity for every row. Thereafter, as shown in FIG. 13(b), when the image signals for the n+1-th field or frame are displayed, the polarity of the liquid crystal driving voltage for each pixel electrode 9a is inversed and during the time for displaying the image signal of the n+1th field or one frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is not inversed, and each pixel electrode is driven with the same polarity for every row. Then, the state shown in FIG. 13(a) and 13(b) is repeated at the period of one field or one frame. This is the 1H inverse driving method. As a result, while avoiding deterioration of the liquid crystal caused by the application of DC voltage, it is possible to prevent image display with reduced cross-talk or flicker. Further, the 1H inverse driving method is more advantageous than the 1S inverse driving method to be explained later, in that there is no almost cross-talk in the vertical direction (Y direction) in the drawing.

[0155] However, as can be understood from FIG. 13(a) and FIG. 13(b), in the 1H inverse driving method, a horizontal electric field takes place between the pixel electrodes 9a adjacent to each other in the vertical direction (Y direction) in the drawing. In these drawings, an area C1 where the horizontal electric field takes place is always in the vicinity of the gap between the pixel electrodes adjacent to each other in the Y direction. If such horizontal electric field is applied, for the electro-optical material to which a vertical electric field, i.e., an electric field perpendicular to the surface of the substrate, is applied, between

the pixel electrode and the opposing electrode facing each other, the operation failure can be caused by the bad orientation of the liquid crystal in the electro-optical material and by the light leakage in the portion, which leads to a problem of decreasing the contrast ratio.

[0156] With respect to the above, the area where the horizontal electric field is generated can be covered by the light-shielding film. However, in this case, there is a problem that the opening area of pixels becomes narrow in respect to the area where the horizontal electric field is generated. In particular, as the distance between the adjacent pixel electrodes becomes small due to minuteness of the pixel pitch, such horizontal electric field increases, and thus this poses a serious problem in a higher precision electro-optical device.

[0157] In the aspect shown in FIGS. 10 and 11 of the second exemplary embodiment, a step caused by the height of the non-buried portion 352aNB is formed between the pixel electrodes 9a (that is, the adjacent pixel electrodes 9a to which voltage of inverse polarity is applied) adjacent to each other in the vertical direction. Because of the existence of this step, it is possible to intensify the vertical electric field in the vicinity of an edge portion of the pixel electrode 9a arranged on the step and to weaken the horizontal electric field. More specifically, as shown in FIG. 12, the distance between the vicinity of the edge portion of the pixel electrode 9a arranged on the step 430 and the opposing electrode 21 becomes narrower by the height of the step 430. Therefore, in the area C1 where the horizontal electric field is generated, the vertical electric field between the pixel electrode 9a and the opposing electrode 21 can be intensified. Furthermore, in FIG. 12, since the gap between the adjacent pixel electrodes 9a is constant, the intensity of the horizontal electric field to be intensified with the gap getting narrow is constant. Therefore, by making the vertical electric field more prevalent in the area C1 where the horizontal electric field is generated, it is possible to prevent or reduce the bad orientation of the liquid crystal caused by the horizontal electric field. Furthermore, because of the step 430 made of the insulating film, the intensity of the horizontal electric field is weakened, and the portion of the liquid crystal affected by the horizontal electric field is decreased by the amount of replacing the step where the horizontal electric field exists. Therefore, the influence of the horizontal electric field on the liquid crystal layer 50 can be reduced.

[0158] Further, in the above description, the 1H inverse driving method has been explained but the present invention is not limited to such a driving method. For example, 1S inverse driving method of inverting the voltage polarity at a period of a frame or a field for each column while driving pixel electrodes in a column with the potential of the same voltage polarity may be employed in the present invention as the inverse driving method of which

control is relatively easy and which enables the high quality image display. Furthermore, between the pixel electrodes adjacent to each other in both of the column direction and the row direction, the dot inverse driving method of inverting the voltage polarity applied to each pixel electrode has been developed and can be applied to the present invention.

[0159] Further, in the second exemplary embodiment, as shown in FIG. 2, the aspect in which the narrow width portion 342a and 352a is formed to extend through the center of the first gap between the adjacent pixel electrodes 9a has been explained. However, the present invention is not limited to such a construction. That is, as shown in FIGS. 5 and 6, in the aspect where the narrow width portion is formed to extend at the position deviated from the center of the first gap, the grooves 3G1 or 3G2 shown in FIGS. 8 to 11 may be formed in a combination. For example, the construction shown in FIGS. 14 and 15 may be employed. FIG. 14 is a plan view illustrating another aspect different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10, and the narrow width portion of the scanning line is deviated from the center of the first gap, and FIG. 15 is a sectional view taken along plane T-T' in FIG. 14.

[0160] FIG. 14 is similar to FIGS. 5 and 6 in that a narrow width portion 362a of a scanning line 360a is deviated from the center of the long first gap extending through the space between the adjacent pixel electrodes 9a, but FIG. 14 is different from FIGS. 5 and 6 in that the narrow width portion 362a is formed along a groove 3G1' formed on the TFT array substrate 10 and a broad width portion 361a is formed to protrude only downwardly in FIG. 14. In this construction, the narrow width portion 362a of the scanning line 360a is formed from the upper portion in the drawing as viewed from the center of the first gap, and thus the narrow width portion 362a is formed to be positioned right below the contact hole 85 for connecting the pixel electrode 9a and the junction layer 71. Further, the narrow width portion 362a is formed to be entirely buried in the groove 3G1'.

[0161] According to this construction, as shown in FIG. 15, the contact hole 85 is formed on the scanning line 360a formed to be buried in the groove 3G1'. In other words, it is possible to form the contact hole 85 on the assumption that the step caused by the height of the scanning line 360a does not substantially appear on the surface of the third interlayer insulating film 43.

[0162] In such a construction shown in FIGS. 14 and 15, in particular, an advantage from the contact hole 85 which can be easily and securely formed can be obtained. That is, assuming that a step due to the height of the scanning line or the narrow width portion is generated on the surface of the third interlayer insulating film 43, there is a possibility of a

disadvantage in that the contact hole 85 may be formed on the vertex or on the ridge of the step. The present construction overcomes such a drawback.

[0163] The above effects can be understood from the following point of view. That is, in the second exemplary embodiment, since the whole or a part of the scanning line is buried in the groove, and thus a step due to the height of the scanning line does not substantially appear on the surface of the respective interlayer insulating film, the formation position or the extending position of the scanning line need not be considered particularly. In other words, if the scanning line is between the adjacent pixel electrodes in the direction thereof, the scanning line may be formed at any position. This is because, even when the formation position or extending position of the scanning line is selected freely and the contact hole is formed thereon, as described above, the contact hole can be relatively easily and securely formed due to the absence of the step.

[0164] Further, in case the narrow width portion has both the buried portion and the non-buried portion, it is preferable to form the groove such that the buried portion is positioned right below the contact hole 85. FIG. 12 corresponds to an example of such a construction.

(Third exemplary embodiment)

[0165] A third exemplary embodiment of the present invention is explained below with reference to FIGS. 16 to 19. FIG. 16 is a plan view illustrating another aspect in that a shape of the data line is different from that in FIG. 2. FIG. 17 is a sectional view taken along plane P-P' in FIG. 16, FIG. 18 is a sectional view taken along plane Q-Q' in FIG. 16, and FIG. 19 is a sectional view taken along plane R-R' in FIG. 16. Further, since the basic construction and operation of the electro-optical device of the third exemplary embodiment are similar to those of the first exemplary embodiment, explanation about distinguishing features of the third exemplary embodiment is mainly described below. Furthermore, reference numerals in FIGS. 16 to 19 indicate the same elements as in FIGS. 1 to 15 referred to in the above description, when they indicate substantially equivalent elements.

[0166] In the third exemplary embodiment, as shown in FIGS. 16 to 19, a data line 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad. Further, a width W1 of a portion extending along the data line 6a1 in the capacitive line 300, that is, the protruded portion 302, first, is broader than a width W2' of the portions except for the broad width portion 6aW in the data line 6a1 (in particular, see FIG. 17). Second, the width W1 of the protruded portion 302 is almost equal to a width W6 of the broad width portion 6aW in the data line 6a1 (see FIG. 18). The channel area 1a' of the

semiconductor layer 1a is positioned almost at the center in the width direction of the broad width direction 6aW and almost at the center in the width direction of the scanning line 3a. Furthermore, in the third exemplary embodiment, as shown in FIGS. 16, 18 and 19, the broad width portion 6aW of the data line 6a1 is formed continuously from the portion overlapping the TFT 30 to the portion in which the contact hole 81 to connect the semiconductor layer 1a of the TFT and the data line 6a is provided, for each TFT 30 arranged in a matrix shape. In addition, in the third exemplary embodiment, as shown in FIGS. 17 to 19, the light-shielding film 23 is formed on the opposing substrate 20. A width WS of one-by-one lattice of the light-shielding film 23 is greater than that of the broad width portion 6aW.

[0167] In the electro-optical device of the third exemplary embodiment constructed like the above, the following effects can be obtained. That is, first, since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 which is formed broad exist on the TFT 30, so called a double light-shielding effect can be obtained. Therefore, it is difficult for the light to enter the channel area 1a' of the TFT 30, and thus the light leak current can be reduced or minimized.

[0168] In particular, in the third exemplary embodiment, the broad width portion 6aW of the data line 6a also exists on the TFT 30 while overlapping the capacitive line 300. In this case, on the TFT 30, the light-shielding ability corresponding to the integrated value of their transmittances can be obtained. Further, since the channel area 1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width portion 6aW and almost at the center in the width direction of the scanning line 3a, the light-shielding ability can be enhanced.

[0169] Second, in connection with such excellent light-shielding ability, in the third exemplary embodiment, as described above, the width W1 of the protruded portion 302 of the capacitive line 300 and the width W6 of the broad width portion 6aW of the data line 6a are less than the width WS of the light-shielding film 23 on the opposing substrate 20 (that is, $WS > W1$, $WS > W6$). According to this, the light entered from the upper portion of the TFT 30 is first shielded by the light-shielding film 23 and is further shielded by the broad width portion 6aW of the data line 6a. Furthermore, although passing through the broad width portion 6aW, the incident light is next shielded by the protruded portion 302 of the capacitive line 300. In short, in the third exemplary embodiment, since triple light-shielding is implemented, it becomes more difficult for the light to enter the TFT 30.

[0170] Third, in the third exemplary embodiment, the broad width portion 6aW of the data line 6a is formed continuously from the portion overlapping the TFT 30 to the

contact hole 81 for each TFT 30 arranged in a matrix shape. Since the contact hole 81 is provided to connect the semiconductor layer 1a of the TFT 30 and the data line 6a as described above, the capacitive line 300 cannot be formed in the portion. However, in the third exemplary embodiment, in the formation position of the contact hole 81, the broad width portion 6aW of the data line 6a exists similarly to the upper portion of the TFT 30. Therefore, deterioration of the light-shielding ability caused by the absence of the capacitive line 300 can be compensated by the existence of the broad width portion 6aW. In this connection, as in the third exemplary embodiment, according to the aspect that the broad width portion 6a is formed continuously on the TFT 30 and on the formation position of the contact hole 81, since it is not necessary to broaden exceedingly the formation area of the broad width portion 6aW, it is preferable not to increase the inner reflection.

[0171] As described above, in the third exemplary embodiment, by the combination of various effects, the possibility of the light incidence to the channel area 1a' is drastically decreased, and the generation of the light leak current in the TFT 30 and consequently the generation of the flicker and the like on the image due to the light leak current can be effectively suppressed, reduced or minimized.

(The whole construction of the electro-optical device)

[0172] The whole construction of the electro-optical device according to the present exemplary embodiment constructed like the above is explained with reference to FIGS. 20 and 21. Further, FIG. 20 is a plan view of the TFT array substrate along with the respective elements formed thereon viewed from the opposing substrate 20 side, and FIG. 21 is a sectional view taken along plane H-H' in FIG. 20.

[0173] In Figs. 20 and 21, in the electro-optical device according to the present exemplary embodiment, the TFT array substrate 10 and the opposing substrate 20 are arranged opposite to each other. A liquid crystal layer 50 is inserted and sealed between the TFT array substrate 10 and the opposing substrate 20 and the TFT array substrate 10 and the opposing substrate 20 are affixed to each other by a sealing material 52 provided in the sealing area positioned around the image display area 10a.

[0174] In the outer area of the sealing material 52, a data line drive circuit 101 to drive the data line 6a by supplying image signals to the data line 6a at a predetermined timing, and the external circuit connecting terminals 102 are provided along one side of the TFT array substrate 10, and scanning line drive circuits 104 to drive the scanning line 3a by supplying scan signals to the scanning line 3a at a predetermined timing is provided along two sides adjacent to the one side.

[0175] Further, if delay of the scan signals supplied to the scanning line 3a does not matter, the scanning line drive circuit 104 on only one side is sufficient. Furthermore, the data line drive circuit 101 may be arranged on both sides along the sides of the image display area 10a.

[0176] The remaining one side of the TFT array substrate 10 is provided with a plurality of wirings 105 for connection between the scanning line drive circuits 104 provided on both sides of the image display area 10a. Further, at least one corner of the opposing substrate 20 is provided with a conductive material 106 for electrical connection between the TFT array substrate 10 and the opposing substrate 20. Furthermore, as shown in FIG. 21, the opposing substrate 20 having almost the same profile as the sealing material 52 shown in FIG. 20 is bonded to the TFT array substrate 10 through the sealing material 52.

[0177] In FIG. 21, after the TFTs for switching pixels, or wirings, such as the scanning lines, the data lines are formed on the TFT array substrate 10, and the oriented film is formed on the pixel electrodes 9a. In addition to the opposing electrode 21, the oriented film is formed on the uppermost portion of the opposing substrate 20. Further, the liquid crystal layer 50 is formed of the liquid crystal in which, for example, one kind or several kinds of nematic liquid crystal are mixed, and is oriented in a predetermined state between a pair of oriented films.

[0178] Furthermore, on the TFT array substrate 10, in addition to the data line drive circuit 101 and the scanning line drive circuit 104, a sampling circuit to apply image signals to the plurality of data lines 6a at a predetermined timing, a precharge circuit to supply a precharge signal of a predetermined voltage level to the plurality of data lines prior to the image signals, an inspection circuit to inspect the quality or defects of the electro-optical device during production thereof or in shipping thereof and the like may be formed.

(Exemplary Embodiment of electronic apparatus)

[0179] Next, for an embodiment of a color display device of a projection type that is an example of an equipment using the above-described electro-optical device as a light bulb, the whole construction thereof, in particular, the optical construction thereof is explained. FIG. 22 is a diagrammatic sectional view of the color display device of a projection type.

[0180] In FIG. 22, a liquid crystal projector 1100 that is an example of the color display device of a projection type in the present exemplary embodiment includes three liquid crystal modules including the liquid crystal device in which the drive circuit is mounted on the TFT array substrate, and further includes the respective light bulbs 100R, 100G and 100B

for RGB. In the liquid crystal projector 1100, when transmitted light is emitted from a lamp unit of white light source such as a metal halide lamp, the light is divided into the light components R, G and B corresponding to the three primary colors RGB by three mirrors 1106 and two dichroic mirrors 1108 and guided to the light bulbs 100R, 100G and 100B corresponding to the respective colors, respectively. At this time, in particular, in order to prevent or reduce the light loss caused by the long light path, the B light is guided through a relay lens system 1121 composed of an incident lens 1122, a relay lens 1123 and an exit lens 1124. Then, the light components corresponding to the three primary colors modulated, respectively, by the light bulbs 100R, 100G and 100B are synthesized again by a dichroic prism 1112, and then are projected as a color image to a screen 1120 through a projecting lens 1114.

[0181] The present invention is not limited to the above-described exemplary embodiments, and instead may be appropriately varied without departing from the gist or the spirit of the invention known throughout the claims and the specification. The electro-optical devices including such variation, for example, an electrophoresis apparatus or an electro-luminescence display device, or the electronic apparatus including these electro-optical devices are also included in the technical range of the present invention.

What is claimed is:

1. An electro-optical device, comprising:
 - a substrate;
 - scanning lines above the substrate and extending in a predetermined direction;
 - data lines above the substrate and extending in a direction intersecting the scanning lines;
 - thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;
 - pixel electrodes formed correspondingly to the thin-film transistors;
 - a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and
 - a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,
 - the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,
 - a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,
 - the capacitive line being arranged in an overlapping portion between the thin-film transistor and the data line, and
 - the data line being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

2. An electro-optical device, comprising:
 - a substrate;
 - scanning lines above the substrate and extending in a predetermined direction;
 - data lines above the substrate and extending in a direction intersecting the scanning lines;
 - thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;
 - pixel electrodes formed correspondingly to the thin-film transistors;
 - a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and
 - a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,
 - the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,
 - a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,
 - a portion overlapping the thin-film transistor in the data line being formed locally broad, and
 - a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.
3. The electro-optical device according to claim 2, the capacitive line being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

4. The electro-optical device according to claim 2, for each of the thin-film transistors, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

ABSTRACT OF THE DISCLOSURE

An electro-optical device of the present invention includes pixel electrodes, TFTs electrically connected to the pixel electrodes, and scanning lines and data lines connected to the TFTs on a TFT array substrate. Each scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the TFT and the narrow width portion. As a result, an electro-optical device capable of easily adjusting an arrangement of the gate electrodes and the scanning lines and at the same time precisely driving the TFTs is provided.

FIG. 1

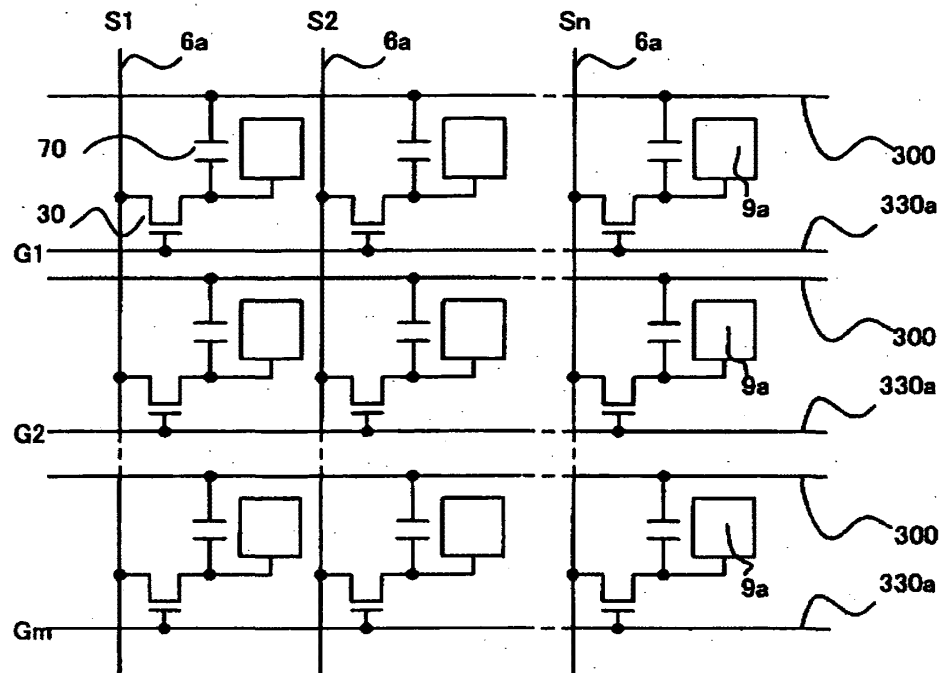


FIG. 2

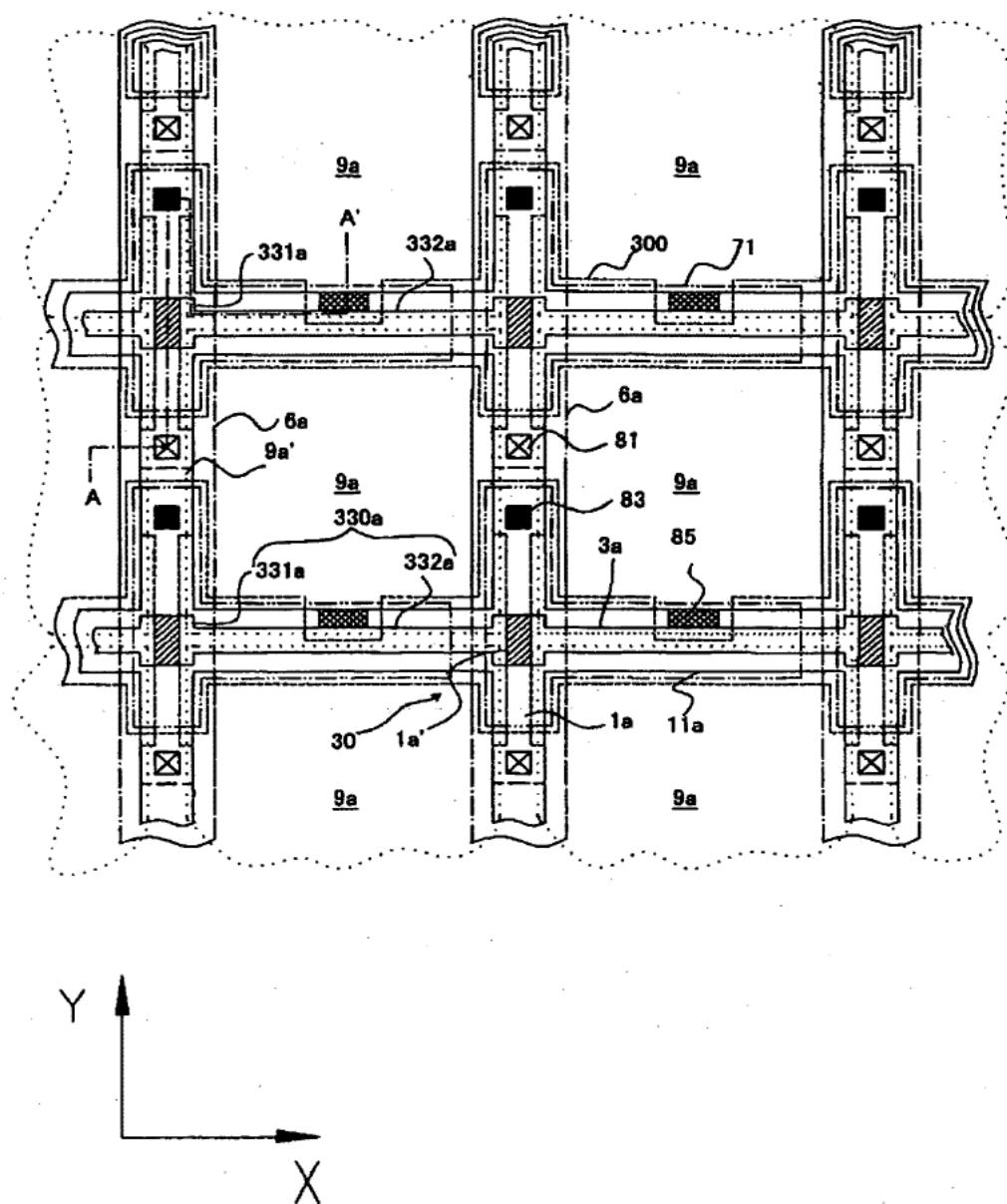


FIG. 3

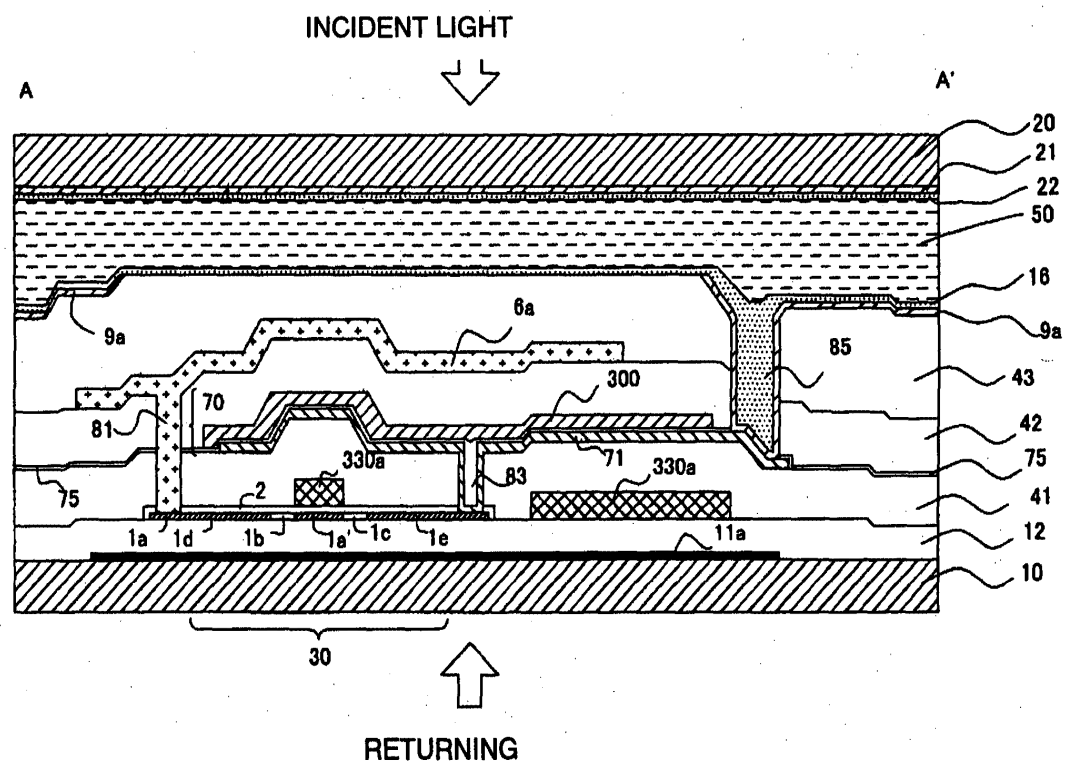


FIG. 4

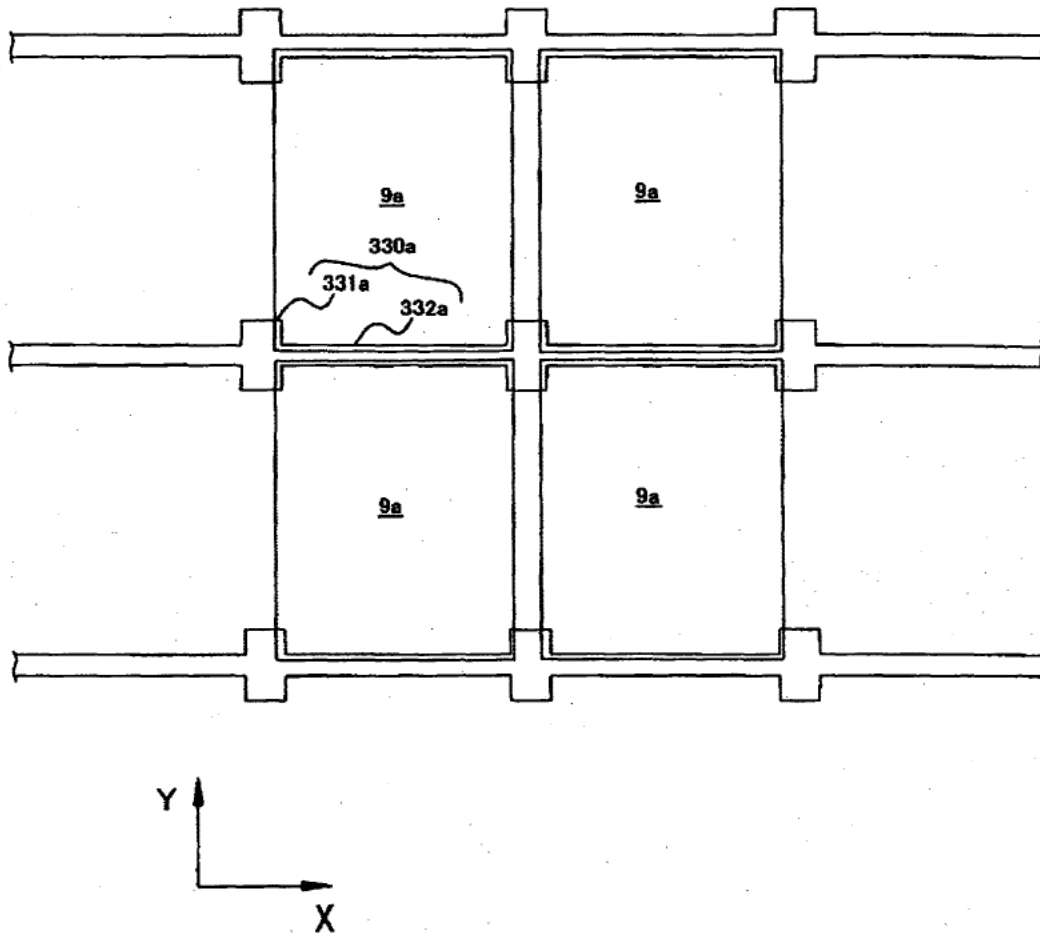


FIG. 5

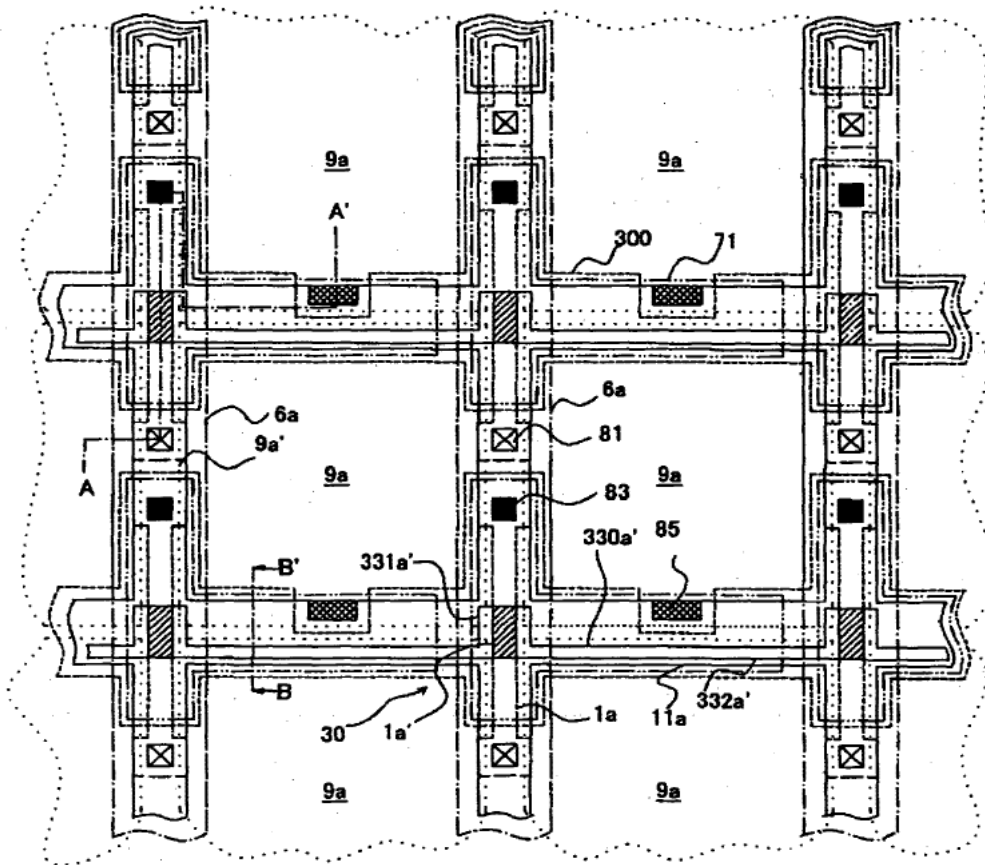


FIG. 6

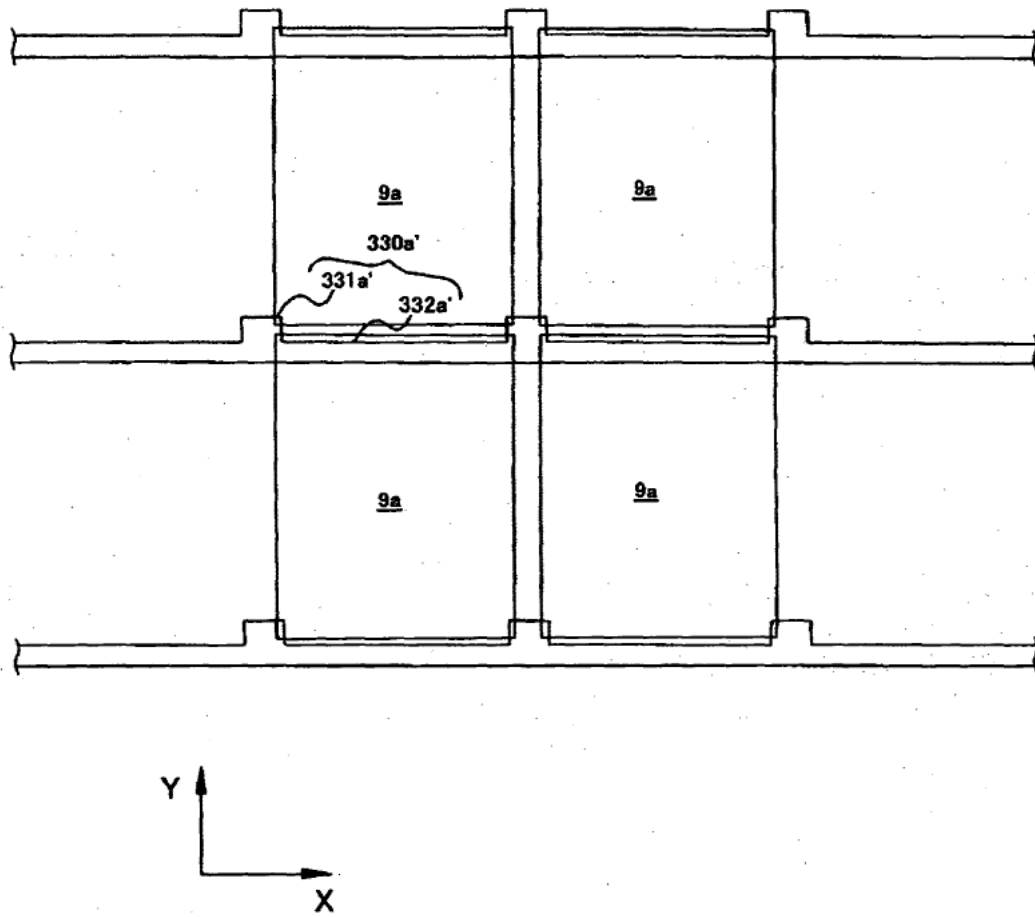


FIG. 7

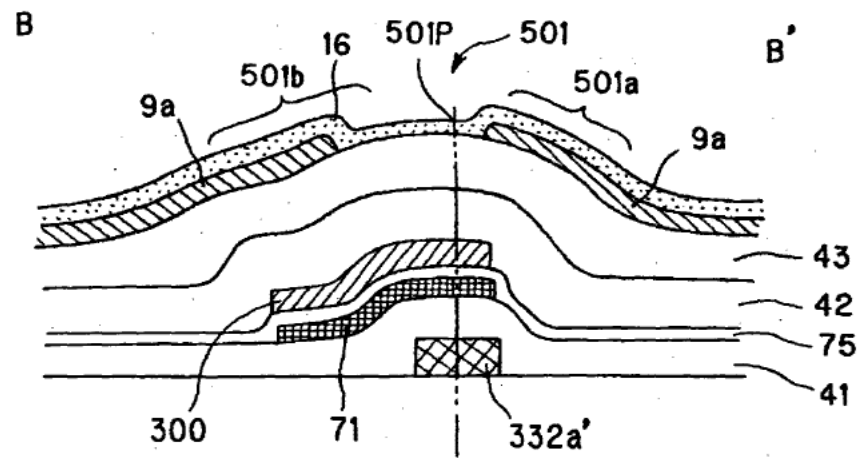


FIG. 8

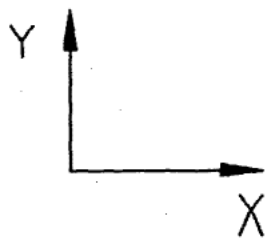
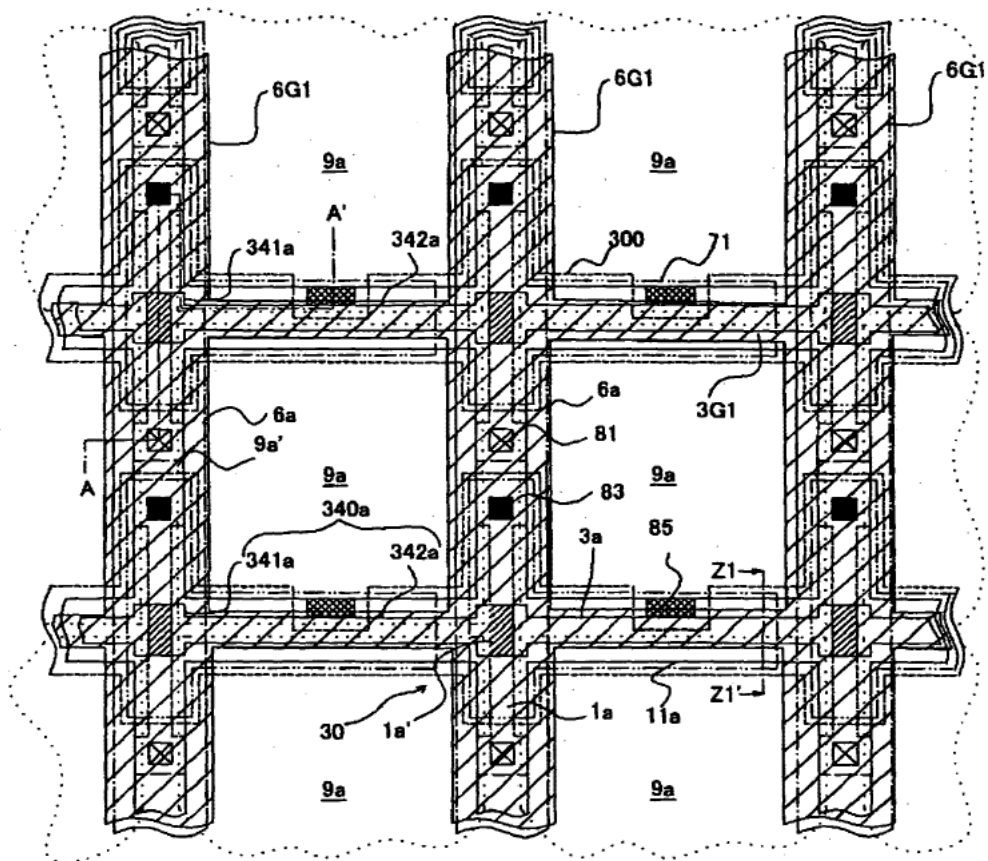


FIG. 9

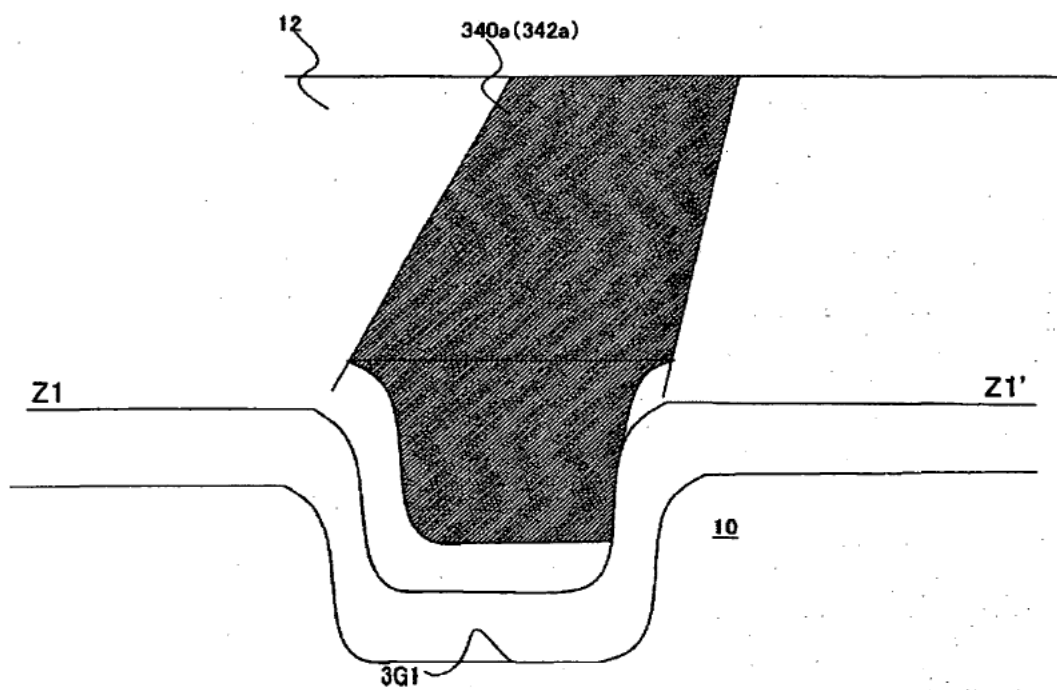


FIG. 10

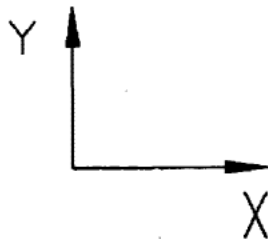
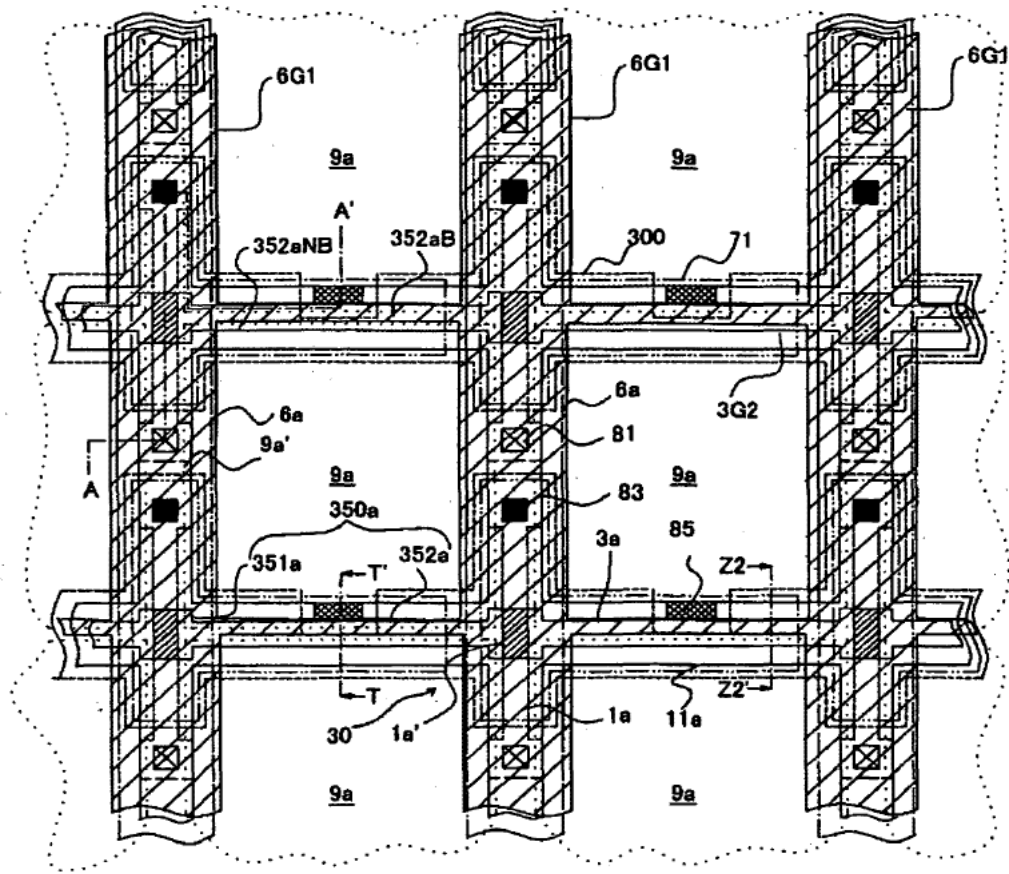


FIG. 11

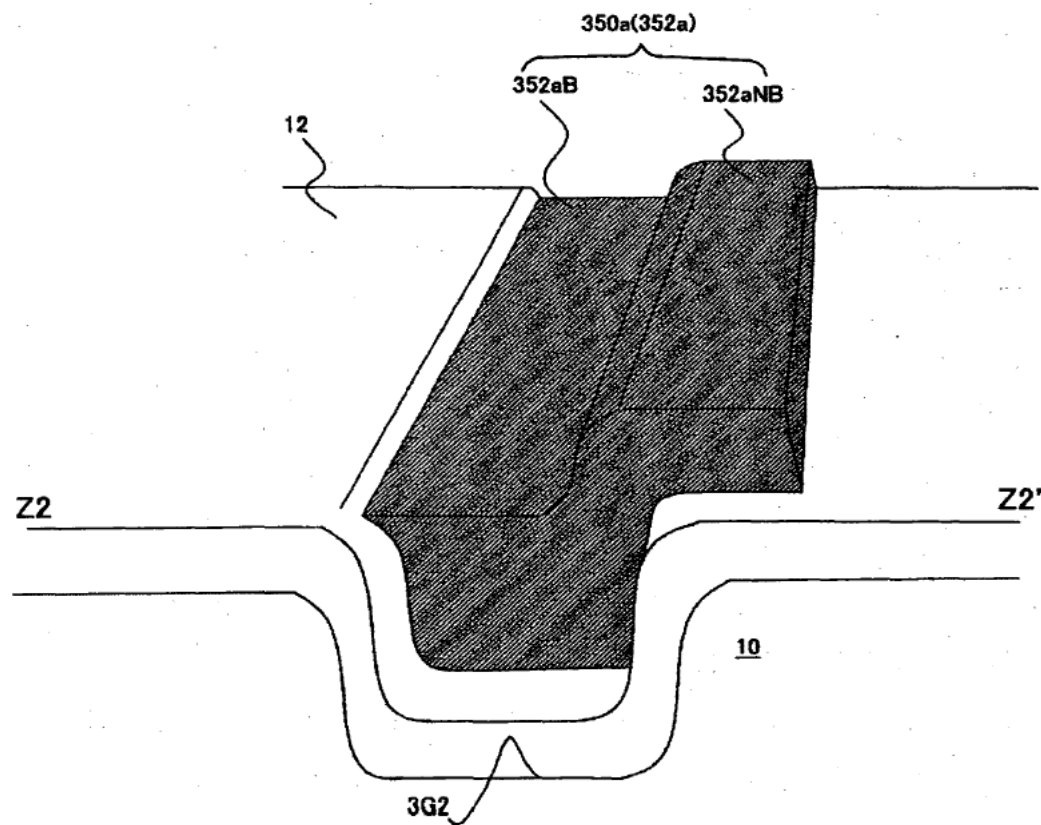


FIG. 12

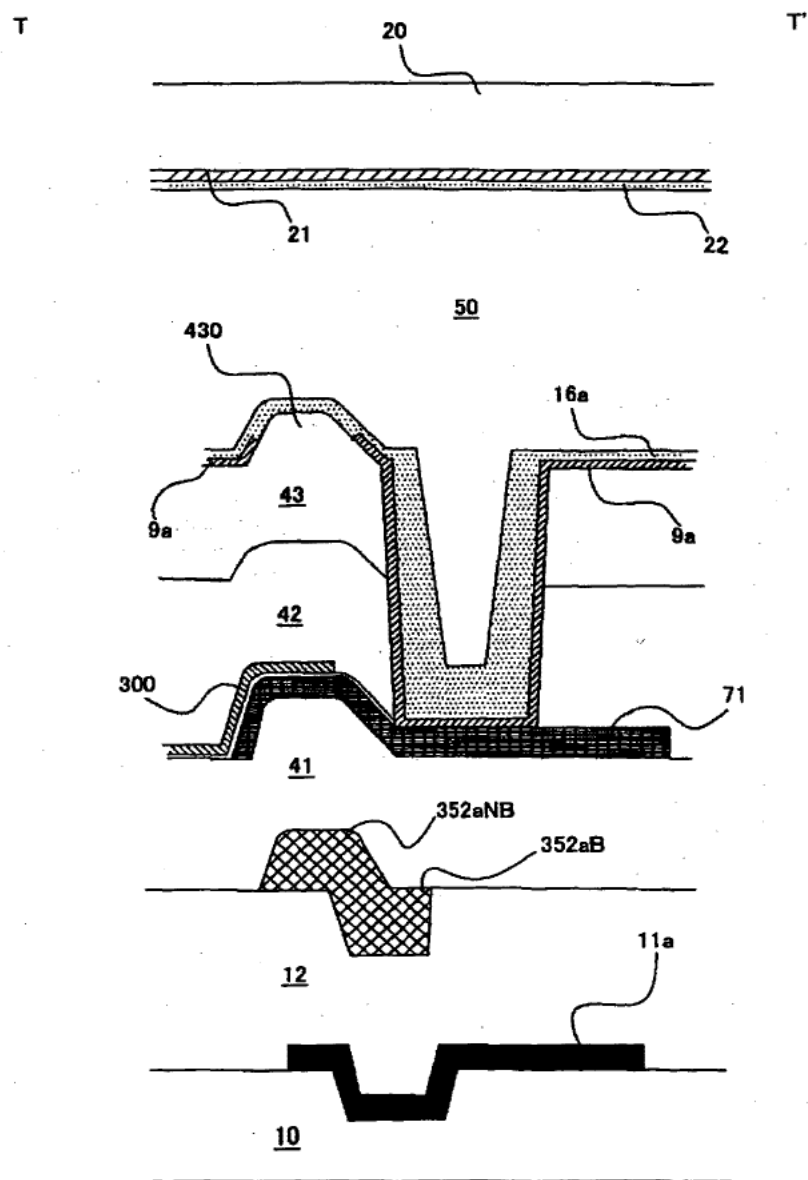


FIG. 13

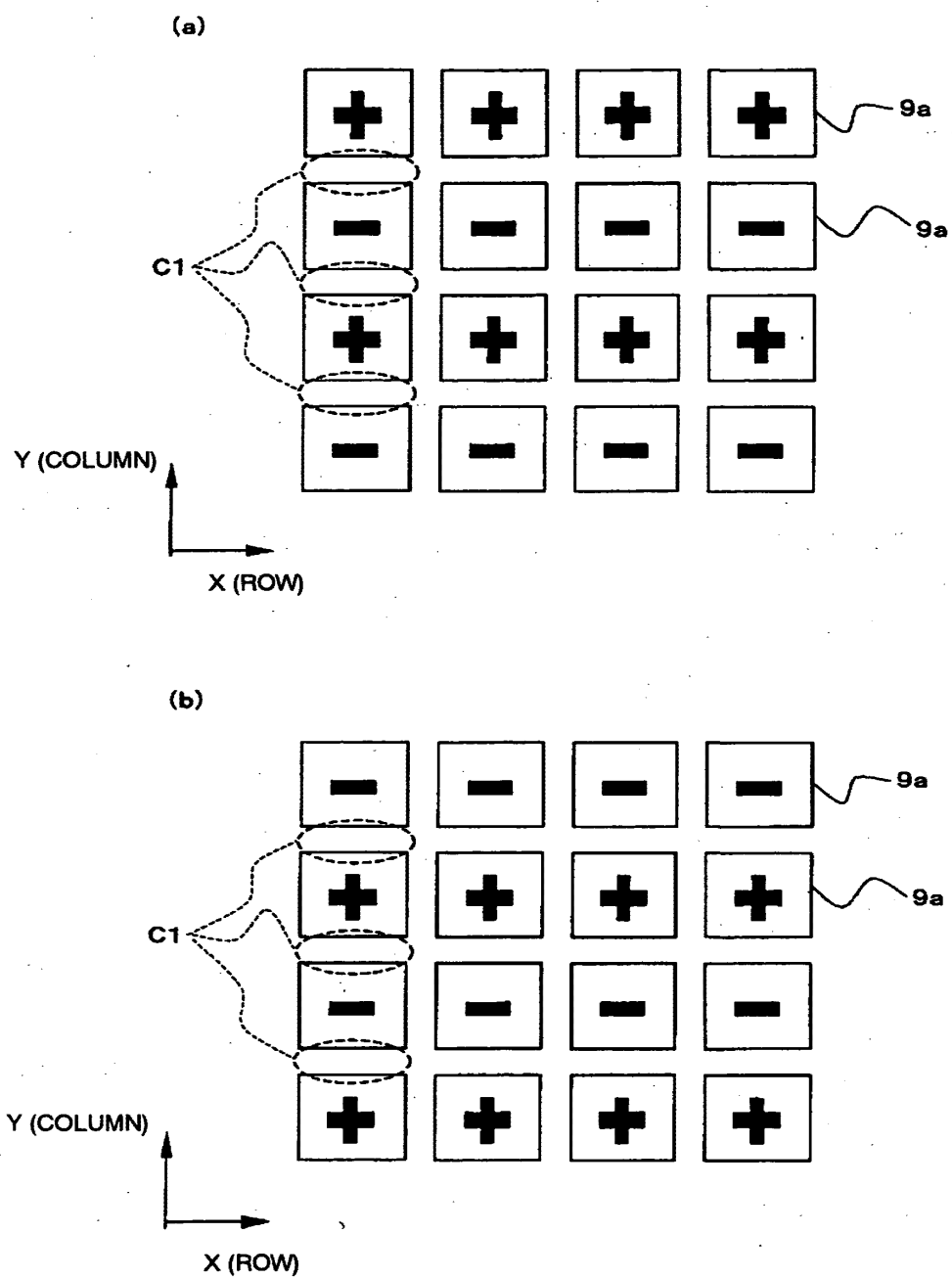


FIG. 14

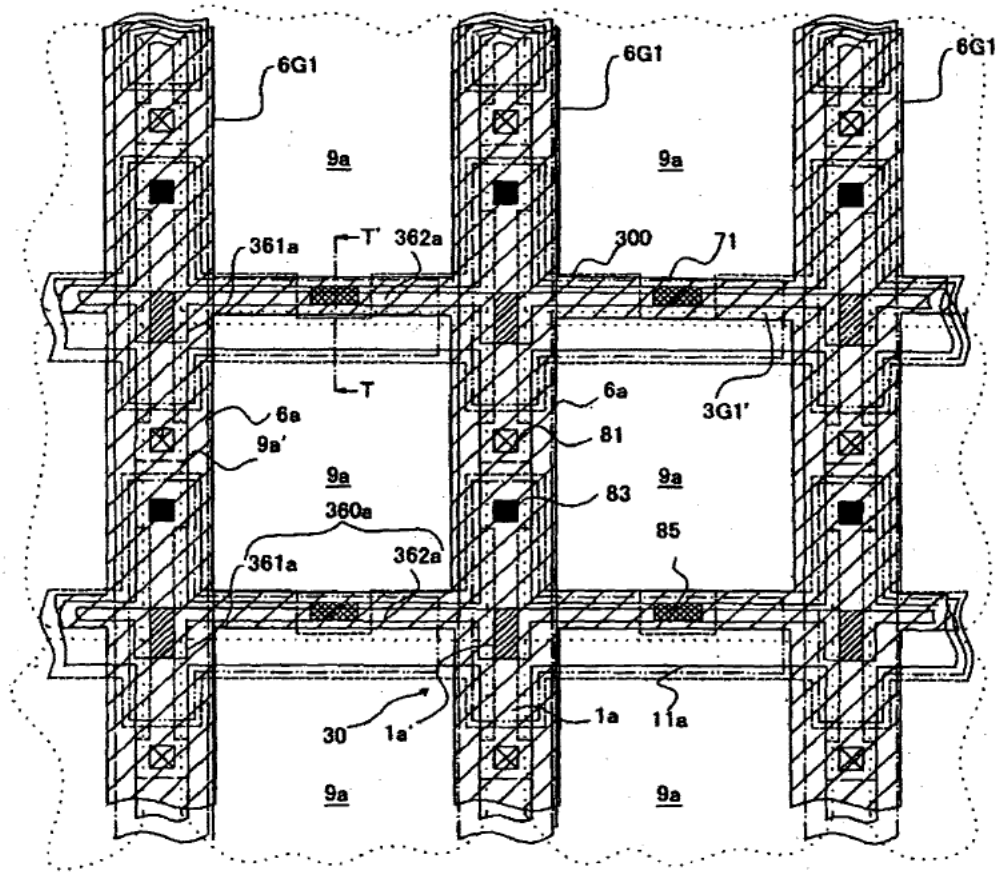


FIG. 15

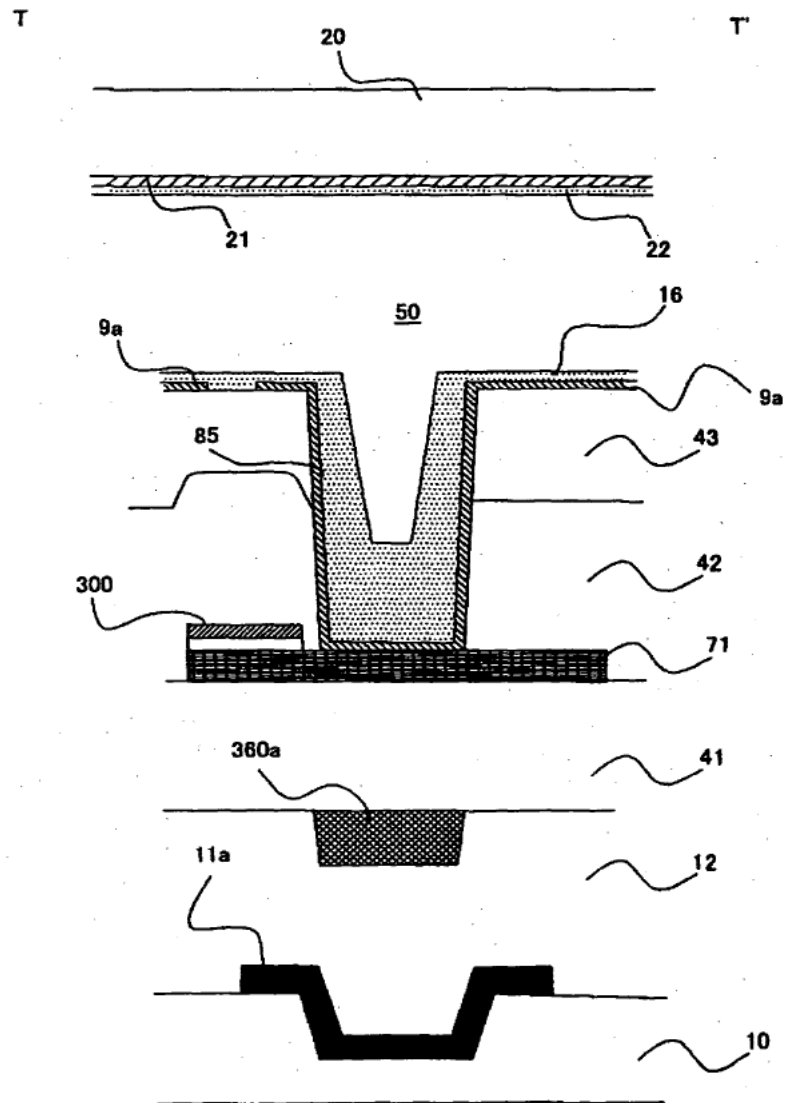


FIG. 16

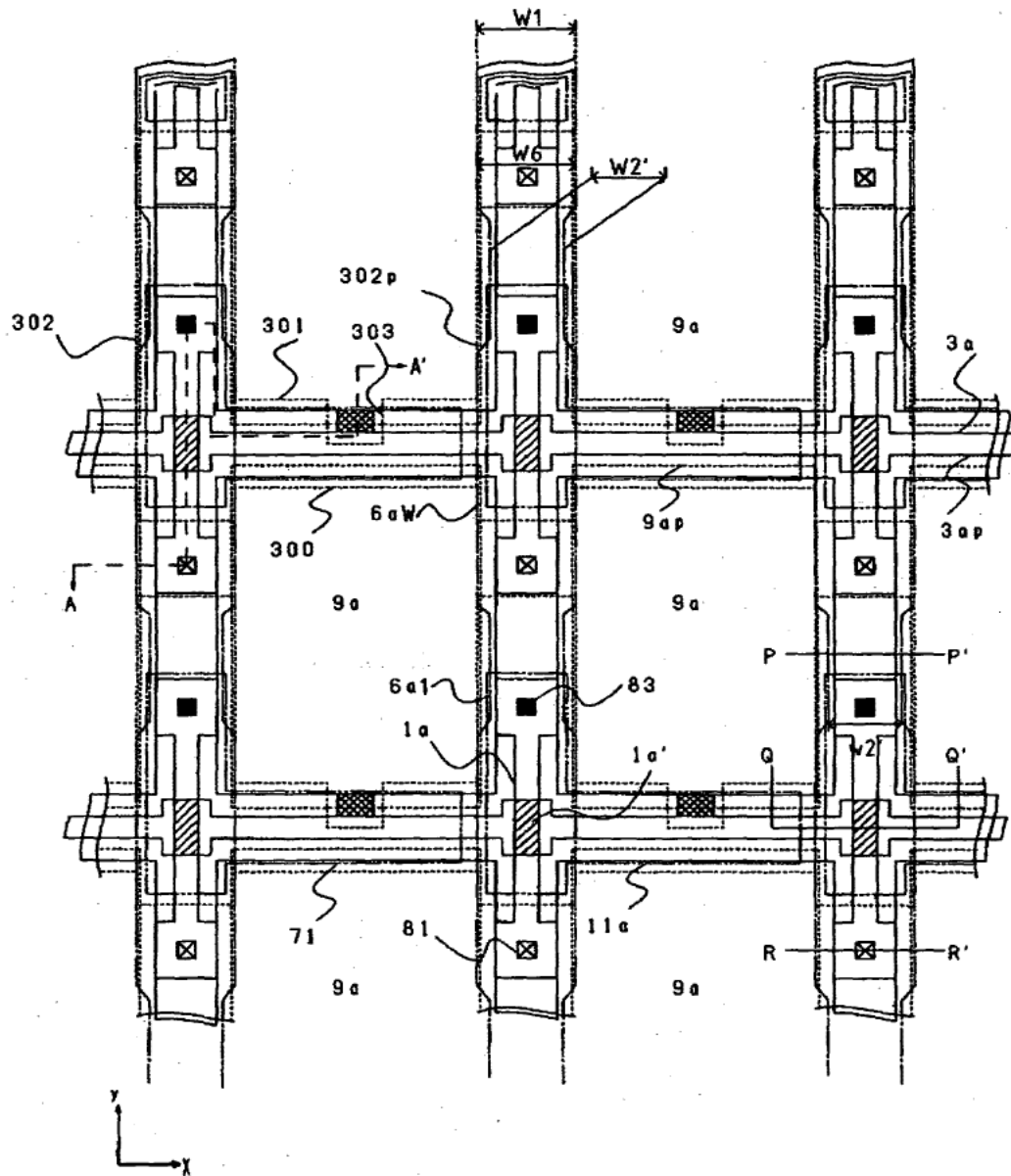


FIG. 17

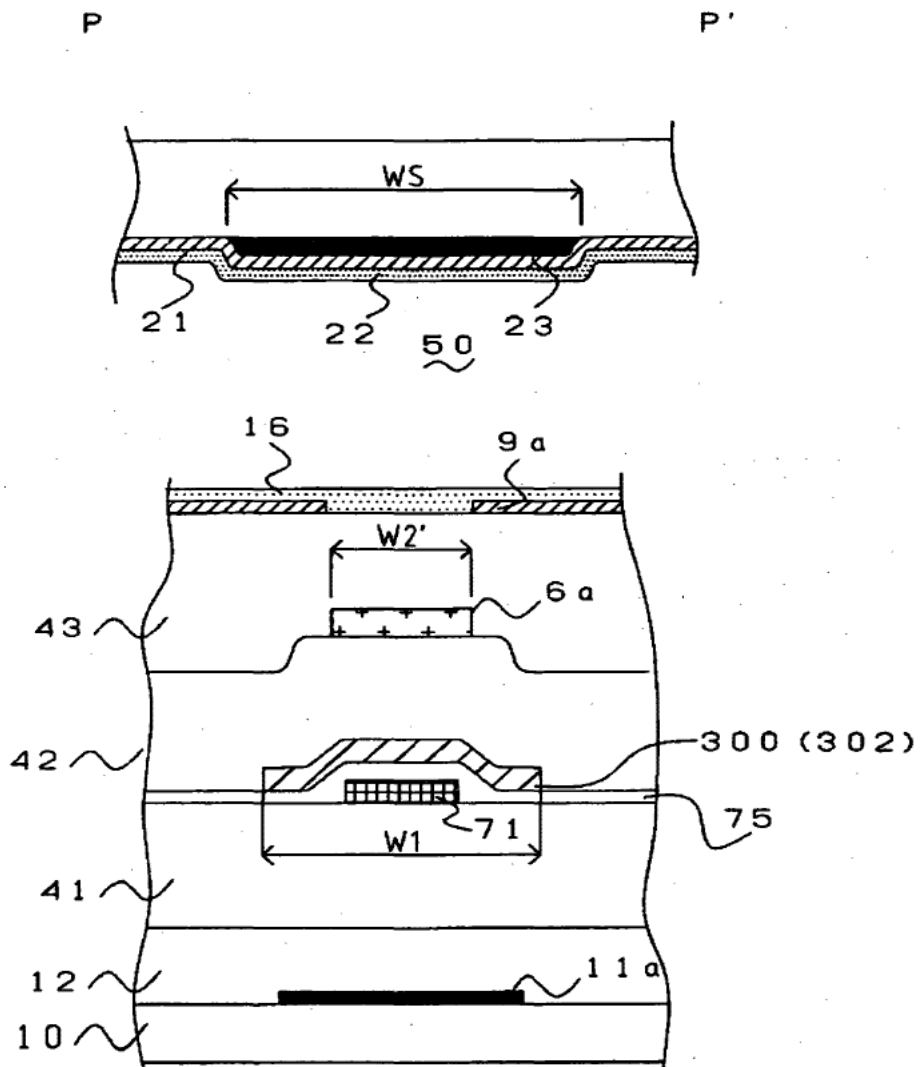


FIG. 18

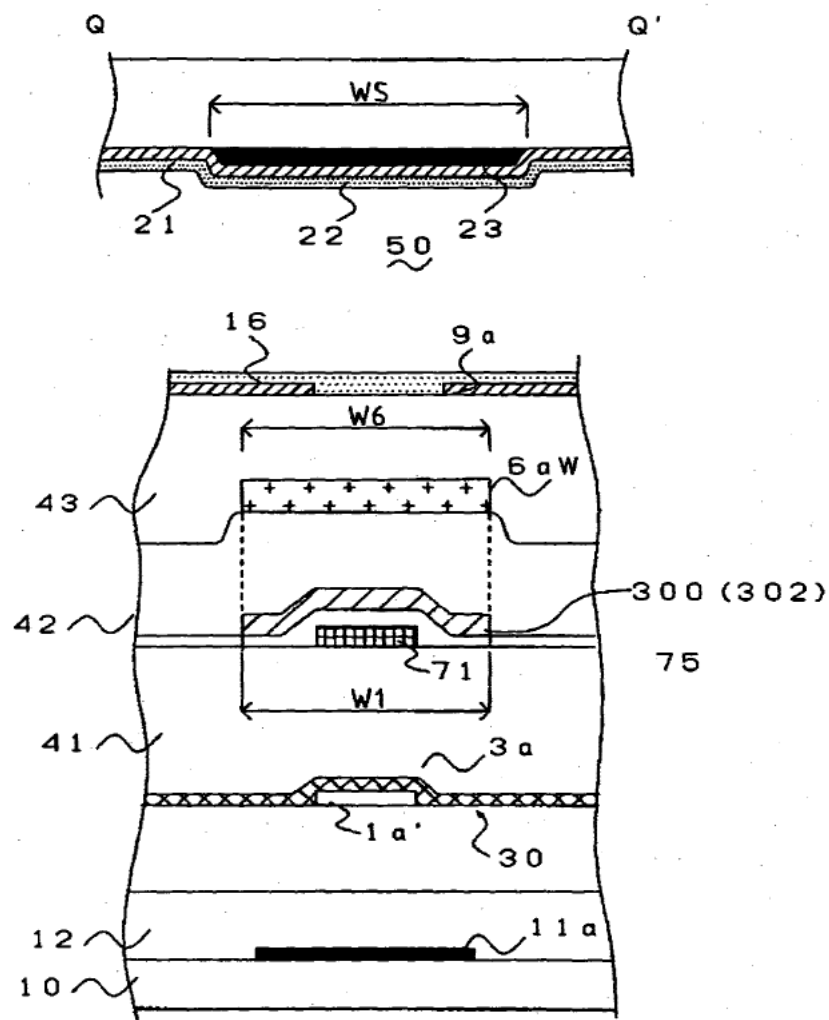


FIG. 19

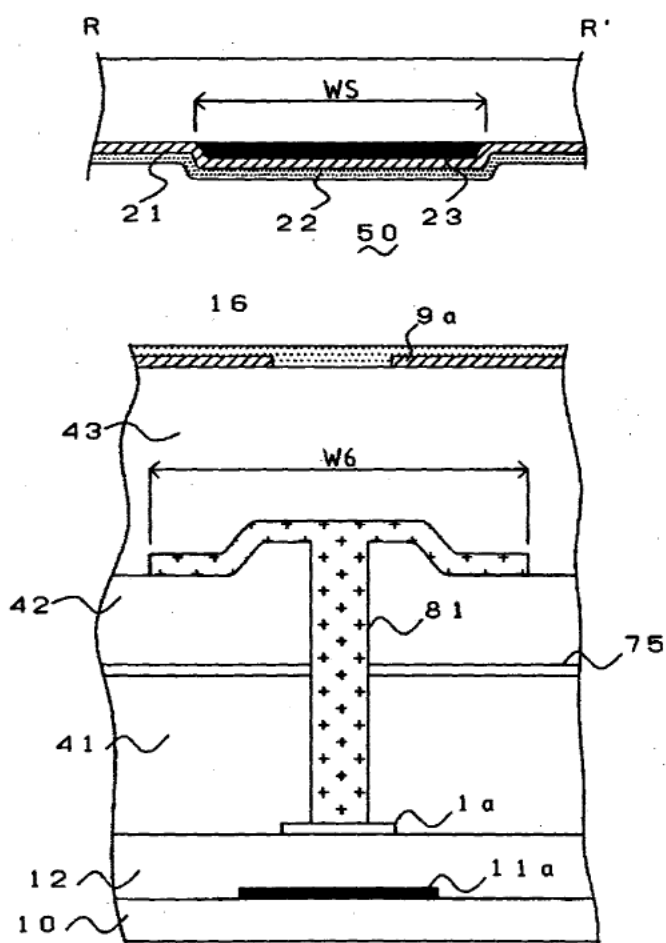


FIG. 20

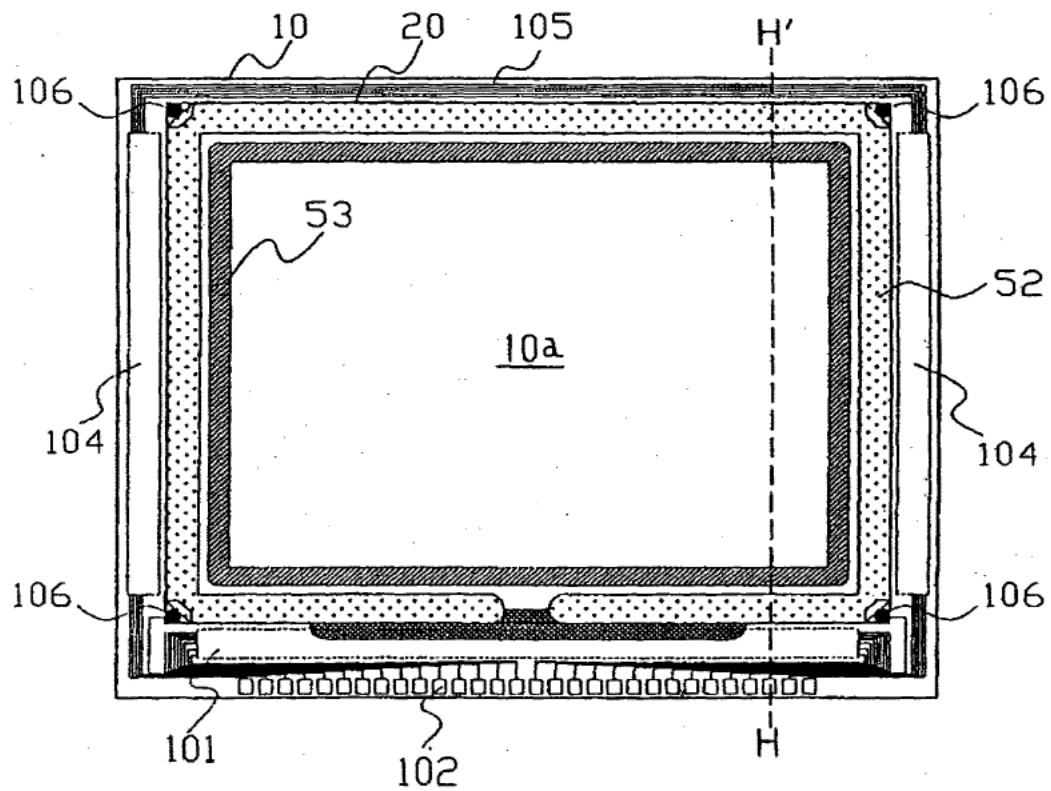


FIG. 21

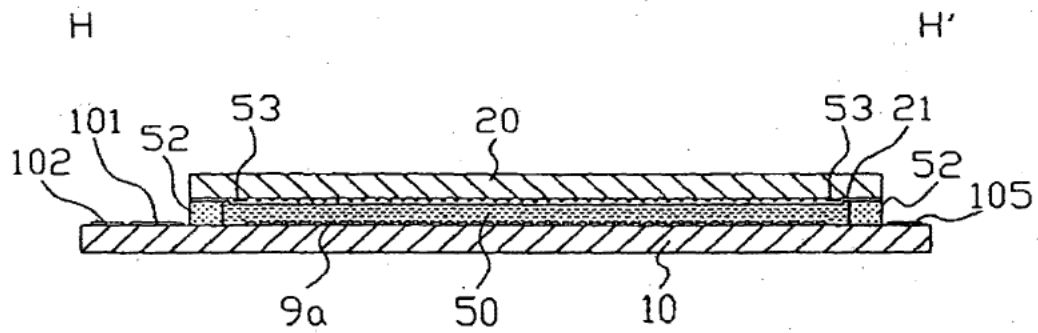
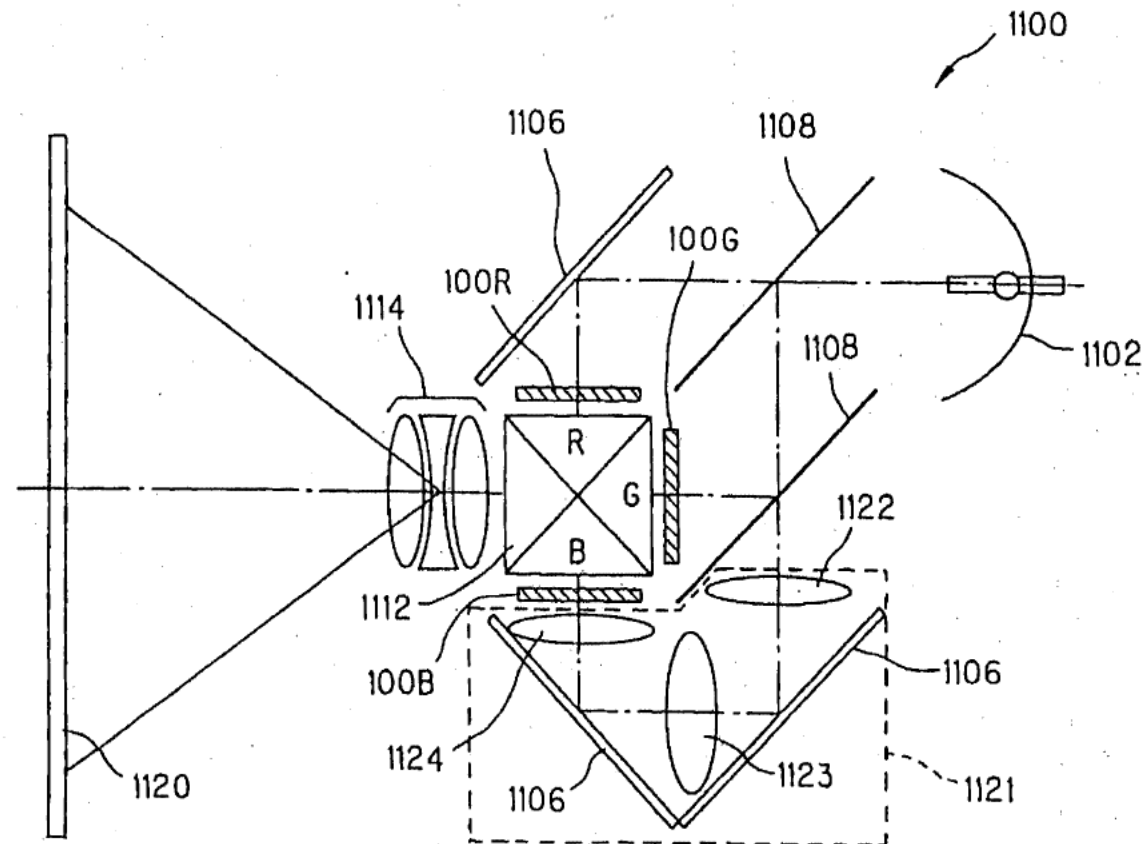


FIG. 22



Seiko Epson Ref. No.: F007516US00

Attorney's Ref. No.: 114542

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

電気光学装置及び電子機器ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

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私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Page 1 of 3

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Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも1ヶ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

外国での先行出願

Priority Not Claimed

優先権主張なし

2002-000713

Japan

07/January/2002

(Number)

(Country)

(Day/Month/Year Filed)

(番号)

(国名)

(出願年月日)

2002-363864

Japan

16/December/2002

(Number)

(Country)

(Day/Month/Year Filed)

(番号)

(国名)

(出願年月日)

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

私は下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1章56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じているところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁理士、または代理人の氏名及び登録番号を明記のこと)

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
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唯一または第一発明者名

村出 正夫

Full name of sole or first inventor

Masao MURADE

発明者の署名

村出 正夫

日付

2003年2月27日

Inventor's signature

Masao Murade

Date

February 27, 2003

住所

日本国, 長野県, 諏訪市

Residence

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Citizenship

Japan

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第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名

日付

Second inventor's signature

Date

住所

日本国, _____, _____

Residence

_____, Japan

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

BEST AVAILABLE COPY

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

12/02/2005 FMETEKI1 00000073 11290589

01 FC:1011	300.00 OP
02 FC:1111	500.00 OP
03 FC:1311	200.00 OP

PTO-1556
(5/87)

U.S. Government Printing Office: 2002 — 486-267/88033

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number

1129 0589

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(d), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	4 minus 20 =	*
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25 =	
X100 =	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50 =	
X200 =	
+360=	
TOTAL	1000

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Data Sheet**Applicant Information**

Applicant Authority type::	Inventor
Primary Citizenship Country::	Japan
Status::	Full Capacity
Given Name::	Masao
Family Name::	MURADE
City of Residence::	Suwa-shi
Country of Residence::	Japan

Correspondence Information

Correspondence Customer Number::	25944
----------------------------------	-------

Application Information

Application Type::	Divisional
Subject Matter::	Utility
CD-ROM or CD-R::	None
Title::	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS
Attorney Docket Number::	114542.01
Total Drawing Sheets::	21
Small Entity::	No

Representative Information

James A. Oliff, Reg. No. 27,075	William P. Berridge, Reg. No. 30,024
Kirk M. Hudson, Reg. No. 27,562	Thomas J. Pardini, Reg. No. 30,411
Edward P. Walker, Reg. No. 31,450	Robert A. Miller, Reg. No. 32,771
Mario A. Costantino, Reg. No. 33,565	

Domestic Priority Information			
Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application is a	Division of	10/320,371	12/17/2002
Foreign Priority Information			
Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2002-000713	01/07/2002	Yes
Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2002-363864	12/16/2002	Yes
Assignee Information			
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		SHINJUKU-KU	
City of mailing address::		TOKYO	
Country of mailing address::		JAPAN	
Postal or Zip Code of mailing address::		163-0811	

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: New U.S. Divisional Application of
Application No. 10/320,371

Filed: December 1, 2005

Docket No.: 114542.01

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. The references were cited by or submitted to the Office in parent application No. 10/320,371, filed December 17, 2002, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, copies of these references are not attached. 37 CFR §1.98(d).

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Randi B. Isaacs
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JAO:RBI/axl

Date: December 1, 2005

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Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 114542.01		APPLICATION NO. New U.S. Divisional Application of Application No. 10/320,371	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Masao MURADE			
				FILING DATE December 1, 2005			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
	1.	5,668,379	09/1997	Ono et al.			
	2.	5,831,694	11/1998	Onisawa et al.			
	3.	6,583,830	06/24/2003	Yasukawa et al.			
	4.	6,528,822	03/04/2003	Murade			
	5.	US2002-021379	02/21/2002	Kim			
	6.	5,748,276	05/05/1998	Uno et al.			
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
	7.	JP-A-2001-356709	12/26/01	Japan w/English Abstract & Translation			
	8.	WO 01/81994 A1	11/01/2001	PCT w/English Abstract			
	9.	2001-209070	8/3/2001	Japan w/English Translation			
	10.	JP2001-343912A	12/14/2001	Japan			
	11.	JP2001-330859	11/30/2001	Japan w/English Abstract & Translation			
	12.	JP2001-33125A	2/9/2001	Japan			
	13.	JP2001-356709	12/26/2001	Japan w/English Abstract & Translation			
	14.	JP-A-06-120099	04/28/1994	Japan			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
EXAMINER					DATE CONSIDERED		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: December 1, 2005