PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 06/22/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	09/22/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
TON, MINH TOAN T	2871	349-043000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oliff & Berridge, PLC
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Seiko Epson Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, Japan

09/14/2006 MAHMED2 00000129 10320371
01 FC:1501 1400.00 OP
02 FC:1504 300.00 OP

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
☒ A check in the amount of the fee(s) is enclosed. ck #184099 ($1,700)
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature J. Adam Neff
Date September 13, 2006

Typed or printed name J. Adam Neff
Registration No. 41,218

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25944 7590 06/22/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
TON, MINH TOAN T	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/22/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	09/22/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
P.O. Box 1450
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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(Depositor's name)
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

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nonprovisional	NO	$1400	$300	$1700	09/22/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
TON, MINH TOAN T	2871	349-043000

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2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

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(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 06/22/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
TON, MINH TOAN T	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/22/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	Toan Ton	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers filed 05/10/06*.

2. ☒ The allowed claim(s) is/are *6,7,9,11 and 13*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TOANTON
PRIMARY EXAMINER

Issue Classification	Application/Control No. 10/320,371	Applicant(s)/Patent under Reexamination MURADE, MASAO
	Examiner Toan Ton	Art Unit 2871

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
349	43	G	0	2	F	/1343				/	
CROSS REFERENCES		G	0	2	F	/136				/	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	G	0	2	F	/1333				/	
349	46 139 39					/				/	
						/				/	
						/				/	
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(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

TOAN TON
PRIMARY EXAMINER

(Primary Examiner) 05/18/06 (Date)

Total Claims Allowed: 5

O.G. Print Claim(s)	O.G. Print Fig.
1	2,3

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
1	6		36		66		96		126		156		186
2	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
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4	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
5	13		43		73		103		133		163		193
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	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	Toan Ton	2871	

SEARCHED			
Class	Subclass	Date	Examiner
349	43	5/18/2006	TTON
	46		
	139		
	(updated)		
	39		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
349	**43,46**	5/18/2006	**TTON**
	139		
	(PGPUB)		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (updated subclasses)	5/18/2006	TTON

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/320,371	MURADE, MASAO
Examiner	**Art Unit**
Toan Ton	2871

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date							
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UNITED STATES PATENT AND TRADEMARK OFFICE

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Bib Data Sheet

CONFIRMATION NO. 1588

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/320,371	12/17/2002 RULE	349	2871	114542

APPLICANTS
Masao Murade, Suwa-shi, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************
JAPAN 2002-000713 01/07/2002
JAPAN 2002-363864 12/16/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/06/2003

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☒ yes ☐ no	JAPAN	21	18	2
35 USC 119 (a-d) conditions met ☒ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
25944

TITLE
Electro-optical device and electronic apparatus

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1400	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

OIPE IAP45 MAY 10 2006 PATENT & TRADEMARK OFFICE

1 FW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: M. TON

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the February 28, 2006 Office Action, reconsideration of the rejections is respectfully requested in light of the following remarks.

Claims 6-7, 9, 11 and 13 are pending. Claims 9, 11 and 13 are withdrawn from consideration.

I. Summary of Personal Interview

Applicant appreciates the courtesies shown to Applicant's representatives by Examiner Ton in the April 20 personal interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

During the interview Applicant's representatives asserted, and the Examiner agreed, that the current claims appear to overcome the 35 U.S.C. 102(b) rejections based upon Murade and Uno. As stated in the Interview Summary prepared by the Examiner, it was

agreed that neither Murade or Uno disclose the limitations of claim 6, in particular, details of the broad width of the gate line, channel and contact hole.

II. Rejections of Claims 6 and 7 Under 35 U.S.C. 102(b)

The Office Action rejects claims 6-7 under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,388,721 to Murade ("Murade"). Further, the Office Action rejects claims 6-7 under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,748,276 to Uno et al. (Uno). Applicant respectfully traverses these rejections.

Independent claim 6 recites an electro-optical device that includes, inter alia, "a respective scanning line having **a broad width portion as a gate electrode** in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, . . . **the broad width portion** and the channel area **extending in a direction extending from the channel area to a contact hole**, the contact hole electrically **connecting the channel area and the data line**." As demonstrated during the April 20 interview based upon a concurrent review of the specifications and drawings, neither Murade nor Uno teach or suggest such a feature.

As shown in Murade at Fig. 1, scanning line 2 is no broader at the gate electrode of the channel area 1c than the narrowest of portions of scanning line 2. Therefore, Murade does not disclose a "scanning line **having a broad width portion as a gate electrode**," as recited in the claims. Further, Murade's extension 2f of scan line 2 does not serve as a gate electrode, and thus does not correspond to the scanning line recited in the claims.

Further, as shown in Uno at Fig. 2, the broad width portion of the scanning line at 24 and the channel area extend in a direction extending from the channel area to a contact hole (i.e., contact hole 7b). However, as stated at col. 5, lines 10-11, contact hole 7b connects transparent electrode pixel electrode 2a to pixel control capacitor electrode 8c, not the data

line. Therefore, Uno does not disclose "**the broad width portion** and the channel area **extending in a direction extending from the channel area to a contact hole**, the contact hole electrically **connecting the channel area and the data line**," as recited in the claims.

Accordingly, as agreed, claim 6 is patentably distinguishable over the applied art. Claim 7 depends from claim 6 and is, therefore, patentably distinguishable over the applied art for at least their dependence on allowable base claims, as well as for additional features claim 7 recites. Accordingly, withdrawal of this rejection is respectfully requested.

Applicant further assert that withdrawn claims 9, 11 and 13 each include a feature similar to that addressed above with respect to claim 6 and, for at least this reason, are patentably distinguishable over the cited prior art for at least the reasons provided above with respect to claims 6 and 7. Accordingly, Applicant respectfully requests that claim 9, 11 and 13 be rejoined to the application and allowed.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

J. Adam Neff
Registration No. 41,218

JAO:JMH/eks

Date: May 9, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Interview Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	Toan Ton	2871	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Toan Ton*. (3) *John Hemenway*.

(2) *Adam Neff*. (4)_____.

Date of Interview: *20 April 2006*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *6*.

Identification of prior art discussed: *Murade (6388721), Uno (5748276)*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *It appears that Murade/Uno fails to disclose the limitations of claim 6, in particular the details of the broad width of the gate line, channel, contact hole. However, further search/consideration will be needed*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

TOANTON
PRIMARY EXAMINER

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 02/28/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
TON, MINH TOAN T	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	Toan Ton	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7,9,11 and 13* is/are pending in the application.

4a) Of the above claim(s) *9,11 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restriction

1. An election of species I comprising claims 6-7 is acknowledged. Each of the species comprises an embodiment that is patentably distinct from each other. Claims 9, 11 and 13 are withdrawn from consideration.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Murade (US 6388721).

Murade discloses an electro-optical device comprising (see at least Figure 1): a substrate; scanning lines above the substrate and extending in a predetermined direction; data lines (3) above the substrate and extending in a direction intersecting the scanning lines (2); thin film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; pixel electrodes (14) formed correspondingly to the thin film transistors; a respective scanning line having a broad width portion (see at least Figure 1) as a gate electrode in a portion facing a channel area (1c) of a respective thin film transistor and a narrow width portion (portions narrowing than broad width portion) in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a

direction in which the channel area extends, and the broad width portion intersecting a direction in which a scanning line extends and extending in a single/bi direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole (5), the contact hole electrically connecting the channel area and the data line, the pixel electrodes being arranged in a matrix shape; the respective channel area formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected; the narrow width portion being formed at a position deviated from a center of the first gap, and the broad width portion being formed at the center of the first gap in the intersecting area.

Murade discloses the broad width portion formed at a center of the second gap in the intersecting area (see at least Figure 1).

Claims 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Uno (US 5748276, IDS).

Uno discloses an electro-optical device comprising (see at least Figure 1): a substrate; scanning lines above the substrate and extending in a predetermined direction; data lines above the substrate and extending in a direction intersecting the scanning lines; thin film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; pixel electrodes (21) formed correspondingly to the thin film transistors; a respective scanning line having a broad width portion (see at least Figure 1) as a gate electrode (4) in a portion facing a

channel area (6) of a respective thin film transistor and a narrow width portion (portions narrowing than broad width portion) in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion intersecting a direction in which a scanning line extends and extending in a single/bi direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole (7b), the contact hole electrically connecting the channel area and the data line, the pixel electrodes being arranged in a matrix shape; the respective channel area formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected; the narrow width portion being formed at a position deviated from a center of the first gap, and the broad width portion being formed at the center of the first gap in the intersecting area.

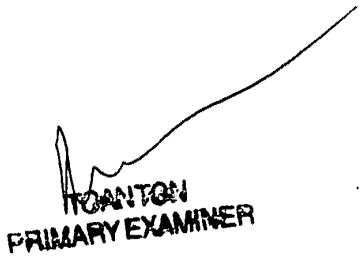
Murade discloses the broad width portion formed at a center of the second gap in the intersecting area (see at least Figure 1).

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Ton whose telephone number is (571) 272-2303.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 24, 2006



Notice of References Cited	Application/Control No. 10/320,371	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner Toan Ton	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,388,721	05-2002	Murade, Masao	349/44
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OIPE JC104 APR 25 2005 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 8-83) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT(S) Masao MURADE	
	FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
M		6,583,830	06/24/2003	Yasukawa et al.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
M		WO 01/81994 A1	11/01/2001	PCT w/English Abstract		
M		2001-209070	8/3/2001	Japan w/English Translation		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
M	07/26/06

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 25, 2005

OIPE JUN 07 2005 PATENT & TRADEMARK OFFICE

Sheet 1 of 1

Form PTO-1449 (REV. 8-83) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT(S) Masao MURADE	
	FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
M	1	* 6,528,822	03/04/2003	Murade		
L	2	** US2002-021379	02/21/2002	Kim		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	3	JP2001-343912A*	12/14/2001	Japan		
M	4	JP2001-330859	11/30/2001	Japan w/Eng. Abs. & Translation		
L	5	JP2001-33125A**	2/9/2001	Japan		
	6	JP2001-356709	12/26/2001	Japan e/Eng. Abs. & Translation		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
	9/2/05

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: June 7, 2005

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PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 8-83) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT(S) Masao MURADE	
	FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
M	1	5,748,276	05/05/1998	UNO et al.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
M	2	JP-A-06-120099 (w/English-language Translation & Abstract)	04/28/1994	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 21, 2005

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/320,371	MURADE, MASAO
Examiner	**Art Unit**
Toan Ton	2871

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	2/24/06								
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/320,371	MURADE, MASAO
	Examiner: Toan Ton	Art Unit: 2871

SEARCHED			
Class	Subclass	Date	Examiner
349	43	2/24/2006	TTON
	46		
	139		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST	2/24/2006	TTON

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1303	349/43.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/24 16:51
L3	1429	349/46.ccls. 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/24 16:52
L4	6	"5748276".pn. "6583830".pn. "6528822".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/24 16:54
L5	134729	(gate scan) adj4 line	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:54
L6	2168758	width	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:54
L7	86949	contact adj2 hole	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:54
L8	1924796	channel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:54
L9	2984859	center	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:55

EAST Search History

L10	2236	5 and 6 and 7 and 8 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:55
L11	2044	349/139.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:56
L13	455531	liquid adj2 crystal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:56
L14	1407	10 and 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:57
L16	1915	11 not 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:56
L17	298	8 and 16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:56
L19	1407	14 and 7 and 8 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/24 16:58

RCE

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/320371

APPLICATION AS FILED – PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR							
BASIC FEE (37 CFR 1.16(a), (b), or (c))				395			790
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

7/25/05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	9	Minus	** 20	=	X 25 =		OR	50 =	
Independent (37 CFR 1.16(h))	5	Minus	*** 5	=	X 100 =		OR	200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))			**		X 25 =		OR	50 =	
Independent (37 CFR 1.16(h))		Minus	***		X 100 =		OR	200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/320371

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))				150			300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

11/1/05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	5	Minus	** 20	=	x 25 =			50 =	
Independent (37 CFR 1.16(h))	3	Minus	*** 3	=	x 100 =		OR	200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180		OR	360	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))		Minus	**		25 =			50	
Independent (37 CFR 1.16(h))		Minus	***		x 100 =			200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					180			360	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INDEX OF CLAIMS 10/320371

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Entered w/RCE 7/25/05

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: G. WANG

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT FILED WITH REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

After entry of the Request for Continued Examination (RCE) filed herewith, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.



1F 2871

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: G. WANG

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT
AND
RESPONSE TO ELECTION OF SPECIES REQUIRMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the October 7, 2005 Election of Species Requirement, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (Previously Presented) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line,

the pixel electrodes being arranged in a matrix shape,

the respective channel area being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a

space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected,

the narrow width portion being formed at a position deviated from a center of the first gap, and

the broad width portion being formed at the center of the first gap in the intersecting area.

7. (Previously Presented) The electro-optical device according to claim 6, the broad width portion being formed at a center of the second gap in the intersecting area.

8. (Canceled)

9. (Withdrawn-Previously Presented) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a

direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line,

grooves being formed in the substrate along the scanning lines, and the scanning lines being buried at least partially in the grooves directly or through an interlayer insulating film,

the narrow width portion having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode being positioned high along the scanning line due to the non-buried portion.

10. (Canceled)

11. (Withdrawn-Previously Presented) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which

the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Canceled)

13. (Withdrawn-Previously Presented) The electro-optical device according to claim 11, for each thin-film transistor, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14-18. (Canceled)

REMARKS

Claims 6, 7, 9, 11 and 13 are pending in this application. By this Amendment, claims 9, 11 and 13 are withdrawn, and claims 12 and 14-18 are canceled without prejudice or disclaimer of the subject matter therein.

I. Election of Species Requirement

Applicant provisionally elects Species 1, with traverse. At least claims 6-7 read on the elected species.

It is also respectfully submitted that the subject matter of all species is sufficiently related that a thorough search for the subject matter of any one species would encompass a search for the subject matter of the remaining species. Thus, it is respectfully submitted that the search and examination of the entire application could be made without serious burden. See MPEP §803 in which it is stated that "if the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions" (emphasis added). It is respectfully submitted that this policy should apply in the present application in order to avoid unnecessary delay and expense to Applicant and duplicative examination by the Patent Office.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/jfb

Date: November 1, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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Charge any fee due to our Deposit Account No. 15-0461

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 10/07/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7,9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *6,7,9 and 11-16* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

(1) the specifics of the electro-optical device comprising a narrow width portion of the scanning electrode being formed at a position deviated from a center of the first gap and the broad with portion of the scanning electrode being formed at the center of the first gap in the intersecting area comprising a first embodiment corresponding to Claims 6-7;

(2) the specifics of the electro-optical device comprising grooves being formed in the substrate along the scanning lines and the scanning lines being buried at least partially in the grooves directly or through a interlayer insulating film and where the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion not buried in the groove extending along the scanning line in parallel to the buried portion comprising a second embodiment corresponding to Claim 9;

(3) the specifics of the electro-optical device comprising a capacitive line having a capactitor electrode where a portion overlapping the thin-film transistor in the date line being formed locally broad and a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed in the data line

and equal to that of the portion formed broad in the data line comprising a third embodiment corresponding to Claims 11 and 13;

(4) the specifics of the electro-optical device comprising a capacitive line having a capactitor electrode where a portion overlapping the thin-film transistor in the date line being formed locally broad and a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed in the data line and narrower than that of the portion formed broad in the data line comprising a fourth embodiment corresponding to Claims 12 and 14-16.

2. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, none of the claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. A telephone call was made to Randi B. Isaacs on September 29, 2005 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Wang
Patent Examiner
AU 2871
September 29, 2005

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/320,371	MURADE, MASAO
Examiner	**Art Unit**
George Y. Wang	2871

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	7/1/04	11/24/04	9/29/05						
	~~1~~	√	√	–						
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OIPE IAP45 SEP 21 2005 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/320,371

Examiner: G. WANG

Filed: December 17, 2002

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits after the filing of a Request for Continued Examination under 37 CFR §1.114. No certification or fee is required.

☒ 2. The References were cited in a counterpart Taiwanese application.

☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 4. An English language Abstract of the non-English language reference is attached hereto.

☒ 5. A computer-generated English language translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See Reference 2.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/jfb

Date: September 21, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

OIPE IAP45
SEP 21 2005
PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 8-83) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT(S) Masao MURADE	
	FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1	5,748,276	05/05/1998	UNO et al.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	2	JP-A-06-120099 (w/English-language Translation & Abstract)	04/28/1994	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 21, 2005

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re the Application of

Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

Group Art Unit: 2871

Examiner: G. WANG

Docket No.: 114542

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant hereby requests continued examination.

☒ Applicant further requests entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 169100 in the amount of ☒ $790.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this page are enclosed.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

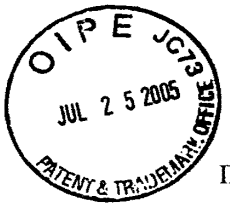
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JAO:RBI/aaw

Date: July 25, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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Charge any fee due to our Deposit Account No. 15-0461



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE	Group Art Unit: 2871
Application No.: 10/320,371	Examiner: G. WANG
Filed: December 17, 2002	Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT FILED WITH REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

After entry of the Request for Continued Examination (RCE) filed herewith, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line,

the pixel electrodes being arranged in a matrix shape,

the respective channel area being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a

space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected,

the narrow width portion being formed at a position deviated from a center of the first gap, and

the broad width portion being formed at the center of the first gap in the intersecting area.

7. (Previously Presented) The electro-optical device according to claim 6, the broad width portion being formed at a center of the second gap in the intersecting area.

8. (Canceled)

9. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends, the broad width portion and the channel area extending in a

direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line,

grooves being formed in the substrate along the scanning lines, and the scanning lines being buried at least partially in the grooves directly or through an interlayer insulating film,

the narrow width portion having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode being positioned high along the scanning line due to the non-buried portion.

10. (Canceled)

11. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which

the channel area ~~extends;~~ extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area ~~extends;~~ extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

the capacitive line being arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. (Previously Presented) The electro-optical device according to claim 11, for each thin-film transistor, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area ~~extends;~~ extends, the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. (Previously Presented) The electro-optical device according to claim 14, the capacitive line being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. (Previously Presented) The electro-optical device according to claim 14, for each of the thin-film transistors, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17-18. (Canceled)

REMARKS

Claims 6, 7, 9, 11 and 12-16 are pending in this application. By this Amendment, claims 6, 9, 11, 12 and 14 are amended. No new matter is added.

The courtesies extended to Applicant's representative by Examiner Wang at the telephone interview held July 20, 2005, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

I. The Claims Define Patentable Subject Matter

The March 24, 2005 Office Action rejects claims 1-18 under 35 U.S.C. §103(a) over U.S. Patent No. 5,668,379 to Ono et al. in view of U.S. Patent No. 5,831,694 to Onisawa. This rejection is respectfully traversed.

Claims 1-5, 8, 10, 17 and 18 are canceled, and thus the rejection of these claims is moot.

None of the applied references teach or suggest an electro-optical device that includes "a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, . . ." as recited in amended independent claim 6 and as similarly recited in amended independent claims 9, 11, 12 and 14. Nowhere does Ono or Onisawa teach or suggest this feature.

During the telephone interview, the Examiner requested that the direction in which the broad width portion and the channel area extend be clarified. Accordingly, by this Amendment, independent claims 6, 9, 11, 12 and 14 are amended to include "the broad width portion and the channel area extending in a direction extending from the channel area to a contact hole, the contact hole electrically connecting the channel area and the data line."

Thus, for at least the reasons discussed above, claims 6, 9, 11, 12 and 14, and the claims depending therefrom, would not have been rendered obvious by Ono in view of Onisawa. Withdrawal of the rejection is thus respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/aaw

Attachments:
Petition for Extension of Time
Request for Continued Examination

Date: July 25, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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OIPE JC73
JUL 25 2005
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date July 25, 2005

re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/320,371

Examiner: G. WANG

Filed: December 17, 2002

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

LARGE ENTITY PETITION FOR 1st - 3rd EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a) AND TRANSMITTAL OF FEE UNDER 37 C.F.R. §1.17

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a response to the outstanding Official Action in the above-identified patent application. The shortened statutory period having expired June 24, 2005, an extension of time for a period of 1 month is hereby requested. Attached hereto is our Check No. 169102 in the amount of $120 in payment for:

X Extension fee for response within first month pursuant to §1.136(a) ($120.00)

_____ Extension fee for response within second month pursuant to §1.136(a) ($450.00)

_____ Extension fee for response within third or subsequent month pursuant to §1.136(a) ($1020.00)

The Commissioner is hereby authorized to charge any additional fee or credit any overpayment associated with this communication to Deposit Account No. 15-0461. Two copies of this petition are enclosed.

07/26/2005 JADD01 00000008 10320371
02 FC:1251 120.00 OP

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/aaw

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 07/12/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 June 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-18.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

GT. NGUYEN
EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments are not persuasive. Applicant's main argument is that the broad width portion of Onisawa does not extend in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends (depicted by arrow A) and asserts, by contrast, how the broad width portion of Onisawa,arrow C, extends in a direction opposite to the direction of channel A. However, there is nothing in Applicant's claimed language or specification that preclude directions that run in opposite directions from "intersecting" with each other. In fact, it appears that these directions, since they are "opposite," actually coincide with each other, thereby rendering an continuous intersecting of directions.

CLAIMS ONLY	Application Number 10326371	Filing Date
	Applicant(s)	

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT			*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend		Indep	Depend	Indep	Depend	Indep	Depend
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Total Indep			5				Total Indep						
Total Depend			5				Total Depend						
Total Claims			10				Total Claims						

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10320371

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20= *	—
INDEPENDENT CLAIMS	2 minus 3 = *	—
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	740

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	* —
Independent	* 2	Minus	*** 3	* —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

9/13/04

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	* —
Independent	* 2	Minus	*** 3	* —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 10	Minus	** 20	* —
Independent	* 5	Minus	*** 3	* 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86= 400	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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OLIFF & BERRIDGE, PLC
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

OIPE JC174 JUN 23 2005 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

Attorney Docket No.: 114542

CUSTOMER NUMBER 25944

AMENDMENT TRANSMITTAL

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/320,371

Examiner: G. WANG

Filed: December 17, 2002

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ Entitlement to small entity status is hereby asserted.

☐ Small entity status of this application has been established.

Any additional claim fees have been calculated as shown below:

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	*9 MINUS	**20	=0	x 25	$		x 50	$
INDEP CLAIMS	*5 MINUS	***3	=2	x 100	$		x 200	$ 400
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+ 180	$	OR	+ 360	$
					$			$ 400

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

☒ Check No. 167635 in the amount of $400.00 is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/aaw
Date: June 23, 2005

OIPE JC174
JUN 23 2005
PATENT & TRADEMARK OFFICE

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BOX AF

PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2871

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: G. WANG

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the March 24, 2005 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

06/24/2005 SZEWDIE1 00000012 10320371
01 FC:1201 400.00 OP

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (Currently Amended) ~~The~~ An electro-optical ~~device according to claim 5,~~ device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends,

the pixel electrodes being arranged in a matrix shape,

the respective channel area being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a

space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected,

the narrow width portion being formed at a position deviated from a center of the first gap, and

the broad width portion being formed at the center of the first gap in the intersecting area.

7. (Previously Presented) The electro-optical device according to claim 6, the broad width portion being formed at a center of the second gap in the intersecting area.

8. (Canceled)

9. (Currently Amended) ~~The~~ An electro-optical ~~device according to claim 8,~~ device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors; and

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends,

grooves being formed in the substrate along the scanning lines, and the scanning lines being buried at least partially in the grooves directly or through an interlayer insulating film,

the narrow width portion having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode being positioned high along the scanning line due to the non-buried portion.

10. (Canceled)

11. (Currently Amended) ~~The~~ An electro-optical ~~device according to claim 10,~~ device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Currently Amended) ~~The~~ An electro-optical ~~device according to claim 11,~~ device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the

respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

the capacitive line being arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. (Previously Presented) The electro-optical device according to claim 11, for each thin-film transistor, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. (Currently Amended) ~~The~~ An electro-optical ~~device according to claim 10,~~ device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines;

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends; and

a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line,

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line,

a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. (Previously Presented) The electro-optical device according to claim 14, the capacitive line being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. (Previously Presented) The electro-optical device according to claim 14, for each of the thin-film transistors, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17-18. (Canceled)

REMARKS

Claims 6, 7, 9, 11 and 12-16 are pending in this application. By this Amendment, claims 1-5, 8, 10, 17 and 18 are canceled and claims 6, 9, 11, 12 and 14 are amended to further clarify the subject matter therein. No new matter is added.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented, because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. The Claims are Supported by the Specification

Claim 6 is amended into independent form to include the subject matter of cancelled claims 1 and 5. Claim 9 is amended into independent form to include the subject matter of cancelled claims 1 and 8. Claims 11, 12 and 14 are amended into independent form to include the subject matter of cancelled claims 1 and 10. Thus, no new matter is added.

II. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1-18 under 35 U.S.C. §103(a) over U.S. Patent No. 5,668,379 to Ono et al. in view of U.S. Patent No. 5,831,694 to Onisawa. This rejection is respectfully traversed.

Claims 1-5, 8, 10, 17 and 18 are canceled, and thus the rejection of these claims is moot.

None of the applied references teach or suggest an electrical electro-optical device that includes "a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends," as recited in amended independent claims 6 and as similarly recited in amended independent claims 9, 11, 12 and 14.

As acknowledged by the Office Action on page 3, Ono fails to specifically disclose this feature. However, Onisawa does not remedy this deficiency.

Onisawa discloses, as shown by Fig. 3 and the Examiner's representation of Fig. 3 of Onisawa on page 3 of the Office Action, the broad width portion depicted by arrow C. However, the broad width portion of Onisawa does not extend in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends (depicted by arrow A). In contrast, the broad width portion of Onisawa, arrow C, extends in a direction opposite in the direction in which the channel area extends, arrow A. Thus, Onisawa does not teach or suggest "the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends," as recited in the independent claims.

Thus, for at least the reasons discussed above, claims 6, 9, 11, 12 and 14, and the claims depending therefrom, would not have been rendered obvious by Ono in view of Onisawa. Withdrawal of the rejection is thus respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/aaw

Attachment:
Amendment Transmittal

Date: **June 23, 2005**

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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OIPE
JUN 07 2005
PATENT & TRADEMARK OFFICE

-AF/ECW 2871/8

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/320,371

Examiner: G. WANG

Filed: December 17, 2002

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but before payment of the Issue Fee. Attached is our Check No. 167446 in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p). Please credit or debit Deposit Account No. 15-0461 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. The references were cited in a counterpart foreign application.

☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 4. English language Abstracts of the non-English language references are attached hereto.

06/08/2005 SDENBOB1 00000120 10320371
01 FC:1806 180.00 OP

☒ 5. A computer-generated English language translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 4 and 6.

☒ 6. The U.S. equivalent of JP2001-331125A is U.S Publication No. 2002/0021379.

☒ 7. The U.S. equivalent of JP2001-343912A is U.S. Patent No. 6,528,822.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/cfr

Date: June 7, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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JUN 07 2005
PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 8-83) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT(S) Masao MURADE	
	FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1	* 6,528,822	03/04/2003	Murade		
	2	** US2002-021379	02/21/2002	Kim		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	3	JP2001-343912A*	12/14/2001	Japan		
	4	JP2001-330859	11/30/2001	Japan w/Eng. Abs. & Translation		
	5	JP2001-33125A**	2/9/2001	Japan		
	6	JP2001-356709	12/26/2001	Japan e/Eng. Abs. & Translation		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: June 7, 2005

OIPE JC104 APR 25 2005 PATENT & TRADEMARK OFFICE

APP 2871

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: G. Wang

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRIC OPTICAL APPARATUS AND ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but before payment of the Issue Fee. Attached is our Check No. 166041 in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p). Please credit or debit Deposit Account No. 15-0461 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. References 2 and 3 were cited in a counterpart foreign application.

☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

04/26/2005 SZEWDIE1 00000099 10320371
01 FC:1806 180.00 OP

☒ 4. An English language Abstracts of the non-English language reference is attached hereto. An English language translation is also attached.

☒ 5. WO 01/81994 is a counterpart of U.S. Patent 6,583,830.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Randi B. Isaacs
Registration No. 56,046

JAO:RBI/cfr

Date: April 25, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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OIPE JC104 APR 25 2005 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Masao MURADE	
		FILING DATE December 17, 2002	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		6,583,830	06/24/2003	Yasukawa et al.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
		WO 01/81994 A1	11/01/2001	PCT w/English Abstract		
		2001-209070	8/3/2001	Japan w/English Translation		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 25, 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 03/24/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,668,379, hereinafter "Ono") in view of Onisawa et al. (U.S. Patent No. 5,831,694, hereinafter "Onisawa").

3. As to claims 1 and 18, Ono discloses an electronic apparatus (fig. 2) having an electro-optical device (fig. 2, ref. TFT SUB) comprising a substrate (fig. 1, ref. SUB1), scanning lines (fig. 2, ref. GL) above the substrate and extending in a predetermined direction, data lines (fig. 1, ref. DL) above the substrate and extending in a direction intersecting the scanning lines, thin-film transistors (TFTs) (fig. 2, ref. TFT) formed at the intersecting areas of the scanning and data lines, pixel electrodes (col. 8, lines 6-8) formed corresponding to the TFTs, and where the scanning lines have a broad width portion (fig. 2, ref. GL) as a gate electrode in a portion of a respective TFT and a narrow width portion in another portion.

However, the reference fails to specifically disclose the broad portion of the scanning line in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends.

Onisawa discloses the broad portion of the scanning line as a gate electrode (fig. 3, ref. 2) in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends (see Response to Arguments).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the broad portion of the scanning line as a gate electrode in a portion facing a channel area of a respective TFT since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

4. Regarding claims 2-3, Ono discloses the electro-optical device as recited above where the broad width portion having a portion lengthened from the narrow width portion and is connected to the narrow width portion (fig. 3, ref. 2).

5. As per claims 4-9, Ono discloses the electro-optical device as recited above, with the pixel electrode arranged in a matrix shape, however, the reference fails to specifically disclose the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film.

Onisawa discloses an electro-optical device with the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends (fig. 3, ref. 2) and scanning lines covered by insulating film (fig. 4, ref. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

6. Regarding claims 10-17, Ono discloses the electro-optical device as recited above having a capacitative line (fig. 2, ref. STORAGE CAPACITOR) to constitute a storage capacitor extending along the scanning line and a portion of the data line and is broader (fig. 2) than the data line, and a light shield (fig. 1, ref. BM) on another substrate (fig. 1, ref. SUB2).

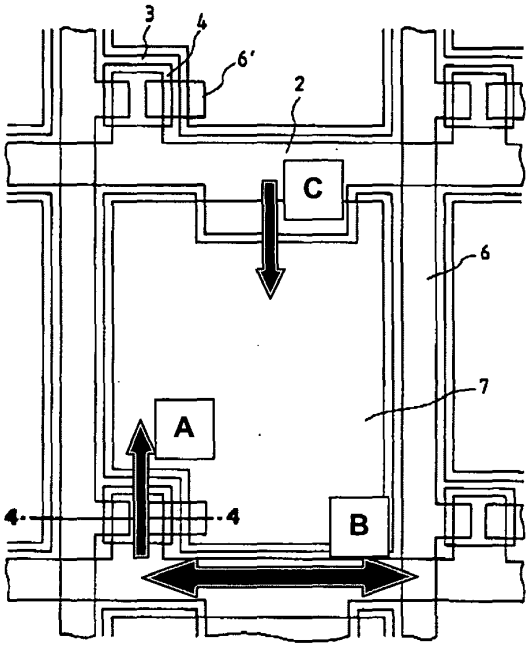
Response to Arguments

7. Applicant's arguments filed September 13, 2004 have been fully considered but they are not persuasive.

Applicant's main argument is that the cited prior art references to do teach the newly added limitations that "the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends." However, the Examiner disagrees. The Onisawa reference clearly teaches these limitations. Referring to Figure 3 below, Onisawa teaches the channel area extending in a direction in which the data lines extend (arrow A), the respective scanning line extending in a direction intersecting a direction in which the channel area extends (arrow B), and the broad width portion extending in a direction intersecting a direction in which the

scanning line extends and extending in a single direction in which the channel area extends (arrow C).

FIG. 3



Therefore, Onisawa clearly cures the deficiencies of Ono and thus satisfies all the limitations of the claimed invention.

Therefore, Examiner holds to the validity of the references used and maintains rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
November 24, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER

Index of Claims

Application No.	Applicant(s)	
10/320,371	MURADE, MASAO	
Examiner	**Art Unit**	
George Y. Wang	2871	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	11/24/04								
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Search Notes	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

SEARCHED			
Class	Subclass	Date	Examiner
Updated	Search	11/24/2004	GW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST Search	11/24/2004	GW

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 12/01/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

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11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

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* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
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4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,668,379, hereinafter "Ono") in view of Onisawa et al. (U.S. Patent No. 5,831,694, hereinafter "Onisawa").

3. As to claims 1 and 18, Ono discloses an electronic apparatus (fig. 2) having an electro-optical device (fig. 2, ref. TFT SUB) comprising a substrate (fig. 1, ref. SUB1), scanning lines (fig. 2, ref. GL) above the substrate and extending in a predetermined direction, data lines (fig. 1, ref. DL) above the substrate and extending in a direction intersecting the scanning lines, thin-film transistors (TFTs) (fig. 2, ref. TFT) formed at the intersecting areas of the scanning and data lines, pixel electrodes (col. 8, lines 6-8) formed corresponding to the TFTs, and where the scanning lines have a broad width portion (fig. 2, ref. GL) as a gate electrode in a portion of a respective TFT and a narrow width portion in another portion.

However, the reference fails to specifically disclose the broad portion of the scanning line in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends.

Onisawa discloses the broad portion of the scanning line as a gate electrode (fig. 3, ref. 2) in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends (see Response to Arguments).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the broad portion of the scanning line as a gate electrode in a portion facing a channel area of a respective TFT since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

4. Regarding claims 2-3, Ono discloses the electro-optical device as recited above where the broad width portion having a portion lengthened from the narrow width portion and is connected to the narrow width portion (fig. 3, ref. 2).

5. As per claims 4-9, Ono discloses the electro-optical device as recited above, with the pixel electrode arranged in a matrix shape, however, the reference fails to specifically disclose the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film.

Onisawa discloses an electro-optical device with the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends (fig. 3, ref. 2) and scanning lines covered by insulating film (fig. 4, ref. 3).

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6. Regarding claims 10-17, Ono discloses the electro-optical device as recited above having a capacitative line (fig. 2, ref. STORAGE CAPACITOR) to constitute a storage capacitor extending along the scanning line and a portion of the data line and is broader (fig. 2) than the data line, and a light shield (fig. 1, ref. BM) on another substrate (fig. 1, ref. SUB2).

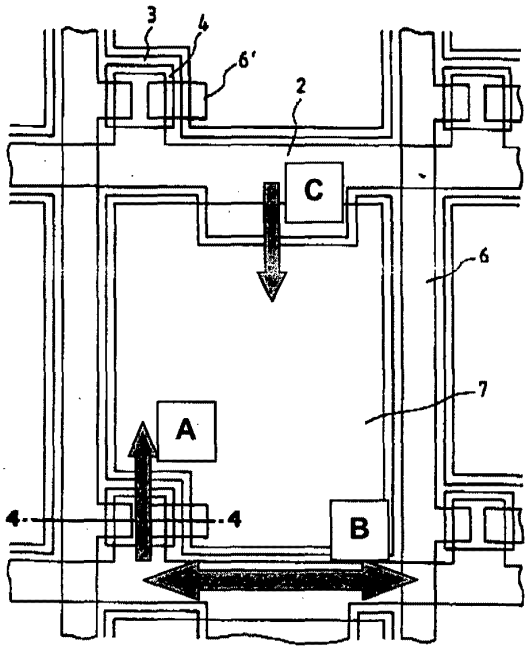
Response to Arguments

7. Applicant's arguments filed September 13, 2004 have been fully considered but they are not persuasive.

Applicant's main argument is that the cited prior art references to do teach the newly added limitations that "the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends." However, the Examiner disagrees. The Onisawa reference clearly teaches these limitations. Referring to Figure 3 below, Onisawa teaches the channel area extending in a direction in which the data lines extend (arrow A), the respective scanning line extending in a direction intersecting a direction in which the channel area extends (arrow B), and the broad width portion extending in a direction intersecting a direction in which the

scanning line extends and extending in a single direction in which the channel area extends (arrow C).

FIG. 3



Therefore, Onisawa clearly cures the deficiencies of Ono and thus satisfies all the limitations of the claimed invention.

Therefore, Examiner holds to the validity of the references used and maintains rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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gw
November 24, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 12/01/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
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4a) Of the above claim(s) _____ is/are withdrawn from consideration.

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9)☐ The specification is objected to by the Examiner.

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a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,668,379, hereinafter "Ono") in view of Onisawa et al. (U.S. Patent No. 5,831,694, hereinafter "Onisawa").

3. As to claims 1 and 18, Ono discloses an electronic apparatus (fig. 2) having an electro-optical device (fig. 2, ref. TFT SUB) comprising a substrate (fig. 1, ref. SUB1), scanning lines (fig. 2, ref. GL) above the substrate and extending in a predetermined direction, data lines (fig. 1, ref. DL) above the substrate and extending in a direction intersecting the scanning lines, thin-film transistors (TFTs) (fig. 2, ref. TFT) formed at the intersecting areas of the scanning and data lines, pixel electrodes (col. 8, lines 6-8) formed corresponding to the TFTs, and where the scanning lines have a broad width portion (fig. 2, ref. GL) as a gate electrode in a portion of a respective TFT and a narrow width portion in another portion.

However, the reference fails to specifically disclose the broad portion of the scanning line in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends.

Onisawa discloses the broad portion of the scanning line as a gate electrode (fig. 3, ref. 2) in a portion facing a channel area of a respective TFT, where the channel area extends in a direction in which the data lines extend, the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a direction intersecting a direction in which the scanning line extends and in a single direction or bi-direction in which the channel area extends (see Response to Arguments).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the broad portion of the scanning line as a gate electrode in a portion facing a channel area of a respective TFT since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

4. Regarding claims 2-3, Ono discloses the electro-optical device as recited above where the broad width portion having a portion lengthened from the narrow width portion and is connected to the narrow width portion (fig. 3, ref. 2).

5. As per claims 4-9, Ono discloses the electro-optical device as recited above, with the pixel electrode arranged in a matrix shape, however, the reference fails to specifically disclose the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film.

Onisawa discloses an electro-optical device with the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends (fig. 3, ref. 2) and scanning lines covered by insulating film (fig. 4, ref. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

6. Regarding claims 10-17, Ono discloses the electro-optical device as recited above having a capacitative line (fig. 2, ref. STORAGE CAPACITOR) to constitute a storage capacitor extending along the scanning line and a portion of the data line and is broader (fig. 2) than the data line, and a light shield (fig. 1, ref. BM) on another substrate (fig. 1, ref. SUB2).

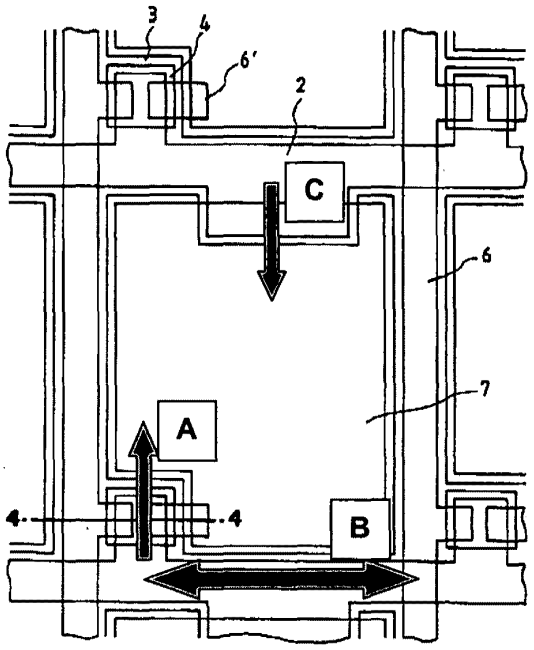
Response to Arguments

7. Applicant's arguments filed September 13, 2004 have been fully considered but they are not persuasive.

Applicant's main argument is that the cited prior art references to do teach the newly added limitations that "the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends." However, the Examiner disagrees. The Onisawa reference clearly teaches these limitations. Referring to Figure 3 below, Onisawa teaches the channel area extending in a direction in which the data lines extend (arrow A), the respective scanning line extending in a direction intersecting a direction in which the channel area extends (arrow B), and the broad width portion extending in a direction intersecting a direction in which the

scanning line extends and extending in a single direction in which the channel area extends (arrow C).

FIG. 3



Therefore, Onisawa clearly cures the deficiencies of Ono and thus satisfies all the limitations of the claimed invention.

Therefore, Examiner holds to the validity of the references used and maintains rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
November 24, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER

Index of Claims

Application No.	Applicant(s)	
10/320,371	MURADE, MASAO	
Examiner	**Art Unit**	
George Y. Wang	2871	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	11/24/04
	1	√
	2	√
	3	√
	4	√
	5	√
	6	√
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	8	√
	9	√
	10	√
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Claim	
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Search Notes	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

SEARCHED			
Class	Subclass	Date	Examiner
Updated	Search	11/24/2004	GW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST Search	11/24/2004	GW

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10320371

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20=	* —
INDEPENDENT CLAIMS	2 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	740

CLAIMS AS AMENDED - PART II

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT A Total	* 18	Minus	** 20	= —
AMENDMENT A Independent	* 2	Minus	*** 3	= —
AMENDMENT A FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE	—	OR	TOTAL ADDIT FEE	—

9/13/04

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT B Total	* 18	Minus	** 20	—
AMENDMENT B Independent	* 2	Minus	*** 3	= —
AMENDMENT B FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

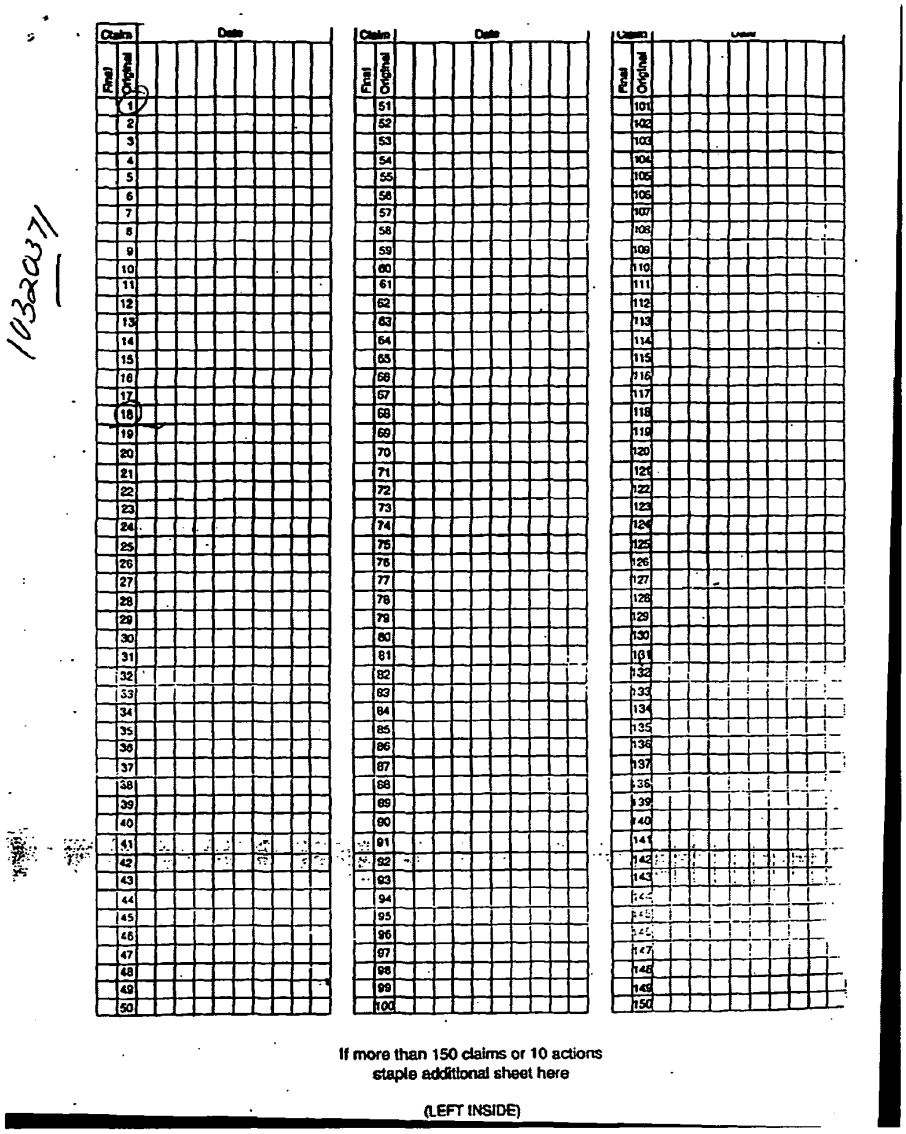
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT C Total	*	Minus	**	=
AMENDMENT C Independent	*	Minus	***	=
AMENDMENT C FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

BEST AVAILABLE COPY


Claim
Date
Final
Original
If more than 150 claims or 10 actions
staple additional sheet here
(LEFT INSIDE)



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2871

Application No.: 10/320,371 — Examiner: G. Wang

Filed: December 17, 2002 — Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the July 12, 2004 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; and

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another ~~portion.~~portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends.

2. (Previously Presented) The electro-optical device according to claim 1, the broad width portion having a portion lengthened from the narrow width portion.

3. (Previously Presented) The electro-optical device according to claim 1, the broad width portion having a portion connected to the narrow width portion.

4. (Previously Presented) The electro-optical device according to claim 1, the respective scanning line extending in a direction intersecting a direction in which the channel

area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends.

5. (Previously Presented) The electro-optical device according to claim 1, the pixel electrodes being arranged in a matrix shape, and

the respective channel area being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected.

6. (Previously Presented) The electro-optical device according to claim 5, the narrow width portion being formed at a position deviated from a center of the first gap, and

the broad width portion being formed at the center of the first gap in the intersecting area.

7. (Previously Presented) The electro-optical device according to claim 6, the broad width portion being formed at a center of the second gap in the intersecting area.

8. (Previously Presented) The electro-optical device according to claim 1, grooves being formed in the substrate along the scanning lines, and the scanning lines being buried at least partially in the grooves directly or through an interlayer insulating film.

9. (Previously Presented) The electro-optical device according to claim 8, the narrow width portion having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode being positioned high along the scanning line due to the non-buried portion.

10. (Previously Presented) The electro-optical device according to claim 1, further comprising a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line, and

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line.

11. (Previously Presented) The electro-optical device according to claim 10, a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Previously Presented) The electro-optical device according to claim 11, the capacitive line being arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. (Previously Presented) The electro-optical device according to claim 11, for each thin-film transistor, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. (Previously Presented) The electro-optical device according to claim 10, a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. (Previously Presented) The electro-optical device according to claim 14, the capacitive line being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. (Previously Presented) The electro-optical device according to claim 14, for each of the thin-film transistors, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17. (Previously Presented) The electro-optical device according to claim 1, further comprising another substrate opposing the substrate through an electro-optical material and a light-shielding film formed on the another substrate,

widths of the data line and a portion extending along the data line in the capacitive line being narrower than that of the light-shielding film.

18. (Currently Amended) An electronic apparatus, comprising:

an electro-optical device including:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors provided correspondingly to intersecting areas of the scanning lines and the data lines; and

pixel electrodes provided correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion opposing a channel area of a respective thin-film transistor and a narrow width portion in another ~~portion.~~portion, the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single direction or bi-direction in which the channel area extends.

REMARKS

Claims 1-18 are pending in this application. By this Amendment, claims 1 and 18 are amended. No new matter is added. In view of the foregoing amendments and following remarks, reconsideration and allowance are respectfully requested.

Applicant appreciates the courtesies shown to Applicant's representative by Examiner Wang in the August 18, 2004 personal interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

I. The Specification Satisfies All Formal Requirements

The Office Action objects to the Abstract asserting that the Abstract has more than one paragraph. This objection is respectfully traversed.

Applicant filed a Preliminary Amendment on March 12, 2003 in the U.S. Patent and Trademark Office in which the Abstract of the Disclosure was reduced to one paragraph to comply with all formal requirements. Accordingly, it is the Applicant's believe that the Examiner erroneously objected to the Abstract.

Prompt consideration of the March 12, 2003 Preliminary Amendment which contains the conforming Abstract and withdrawal of the objection to the Abstract are respectfully requested.

II. The Rejection Under 35 U.S.C. §103(a)

The Office Action rejects claims 1-18 under 35 U.S.C. §103(a) over U.S. Patent No. 5,668,379 to Ono et al. ("Ono") in view of U.S. Patent No. 5,831,694 to Onisawa et al. ("Onisawa"). This rejection is respectfully traversed.

Ono does not teach, disclose or suggest "the channel area extending in a direction in which the data lines extend, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a direction intersecting a direction in which the scanning line extends and extending in a single

direction or bi-direction in which the channel area extends," as recited in claims 1 and 18. As claimed, the broad width portion extends in the single direction or bi-directionally in which the channel area extends and extends in a direction intersecting a direction in which the scanning line extends (specification at paragraph [0020]; and Figs. 2 and 5). The claimed features offer the advantages of at least adjusting the arrangement of the thin-film transistor and the scanning line. Further, since the gate electrode is adequately formed in accordance with the channel length, the electric field can be more effectively applied to the channel area. Ono does not disclose or suggest the claimed features, thus Ono does not possess the advantages of the arrangement of the thin-film transistor and the scanning line.

The Office Action at page 3 admits that Ono "fails to specifically disclose the broad portion of the scanning line in a portion facing a channel area of a respective TFT."

Onisawa does not cure the deficiencies of Ono. Onisawa shows in Fig. 3 the gate electrode line 2 which has a broader portion well removed from an intersection with a drain electrode line 6. Accordingly, Onisawa does not show or suggest the respective scanning line extending in a direction intersecting a direction in which the channel area extends, the broad width portion extending in a direction intersecting a direction in which the scanning line extends, as recited in claims 1 and 18.

Claims 1 and 18 would not have been rendered obvious by Ono in view of Onisawa. Claims 2-17 depend from claim 1, and thus, claims 2-17 also would not have been rendered obvious by Ono in view of Onisawa. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-18 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Richard J. Kim
Registration No. 48,360

JAO:RJK/ksz

Date: September 13, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Interview Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

All participants (applicant, applicant's representative, PTO personnel):

(1) *George Y. Wang*. (3)_____.

(2) *Richard Kim*. (4)_____.

Date of Interview: *18 August 2004*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1 and 18*.

Identification of prior art discussed: *Onisawa et al. (US 5,831,694)*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Discuss consideration of Preliminary Amendment filed March 12, 2003 and proposed amendments to include the limitation to clarify the structural broadening of the scanning lines in a single direction or bidirection. Upon further search and consideration will patentability be determined*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Applicant Initiated Interview Request Form

Application No.: 10/320,371 First Named Applicant: MURADE
Examiner: WANG Art Unit: 2871 Status of Application: NON-FINAL

Tentative Participants:
(1) Ex WANG (2) _____
(3) RICHARD KIM (4) _____

Proposed Date of Interview: AUG 18, 2004 **Proposed Time:** 10:00 (AM/PM)

Type of Interview Requested:
(1) ☐ Telephonic (2) ☐ Personal (3) ☐ Video Conference

Exhibit To Be Shown or Demonstrated: ☐ YES ☑ NO
If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) Obj	Abstract		☐	☐	☐
(2) Rej	1-18	Ono et al Oshimoto et al.	☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Arguments to be Presented: Proposed Amdmt to Cls. 1 & 18:
the channel area extending in a direction in which the data lines extend,
the respective scanning line extending in a direction intersecting a direction in which the channel area extends,
the broad width portion extending in a direction intersecting a direction in which the scanning line extends.

An interview was conducted on the above-identified application on _____

NOTE:

This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of substance of this interview (37 CFR 1.133(b) as soon as possible.

48,360

(Applicant/Applicant's Representative Signature) (Examiner/SPE Signature)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/320,371	12/17/2002	Masao Murade	114542	1588

25944 7590 07/12/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is more than one paragraph. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,668,379, hereinafter "Ono") in view of Onisawa et al. (U.S. Patent No. 5,831,694, hereinafter "Onisawa").

4. As to claims 1 and 18, Ono discloses an electronic apparatus (fig. 2) having an electro-optical device (fig. 2, ref. TFT SUB) comprising a substrate (fig. 1, ref. SUB1), scanning lines (fig. 2, ref. GL) above the substrate and extending in a predetermined direction, data lines (fig. 1, ref. DL) above the substrate and extending in a direction

intersecting the scanning lines, thin-film transistors (TFTs) (fig. 2, ref. TFT) formed at the intersecting areas of the scanning and data lines, pixel electrodes (col. 8, lines 6-8) formed corresponding to the TFTs, and where the scanning lines have a broad width portion (fig. 2, ref. GL) as a gate electrode in a portion of a respective TFT and a narrow width portion in another portion.

However, the reference fails to specifically disclose the broad portion of the scanning line in a portion facing a channel area of a respective TFT.

Onisawa discloses the broad portion of the scanning line as a gate electrode (fig. 3, ref. 2) in a portion facing a channel area of a respective TFT.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the broad portion of the scanning line as a gate electrode in a portion facing a channel area of a respective TFT since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

5. Regarding claims 2-3, Ono discloses the electro-optical device as recited above where the broad width portion having a portion lengthened from the narrow width portion and is connected to the narrow width portion (fig. 3, ref. 2).

6. As per claims 4-9, Ono discloses the electro-optical device as recited above, with the pixel electrode arranged in a matrix shape, however, the reference fails to specifically disclose the scanning line extending in a direction intersecting a direction in

which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film.

Onisawa discloses an electro-optical device with the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends (fig. 3, ref. 2) and scanning lines covered by insulating film (fig. 4, ref. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends, and scanning lines buried pt least partially in the grooves directly or through an insulating film since one would be motivated to provide a low-cost panel capable of yielding high throughput and yield, ultimately to provide a high quality display by reducing resistance (col. 2, lines 33-39).

7. Regarding claims 10-17, Ono discloses the electro-optical device as recited above having a capacitative line (fig. 2, ref. STORAGE CAPACITOR) to constitute a storage capacitor extending along the scanning line and a portion of the data line and is broader (fig. 2) than the data line, and a light shield (fig. 1, ref. BM) on another substrate (fig. 1, ref. SUB2).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
July 1, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER

Sheet _____ of _____

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Masao MURADE	
		FILING DATE December 17, 2002	GROUP

OIPE JC34 FEB 11 2003 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
GW		JP-A-2001-356709 (w/English abstract & JPO translation)	12/26/01	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED 6/29/04

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: February 11, 2003

Notice of References Cited	Application/Control No. 10/320,371	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner George Y. Wang	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,668,379	09-1997	Ono et al.	257/59
	B	US-5,831,694	11-1998	Onisawa et al.	349/43
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)	
10/320,371	MURADE, MASAO	
Examiner	**Art Unit**	
George Y. Wang	2871	

√	Rejected	–	(Through numeral) Canc lled	N	Non-Elect d	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	7/1/04
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Search Notes	Applicati n No.	Applicant(s)	
	10/320,371	MURADE, MASAO	
	Examiner	Art Unit	
	George Y. Wang	2871	

SEARCHED			
Class	Subclass	Date	Examiner
349	43	6/29/2004	GW
349	42	6/29/2004	GW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST Search	6/29/2004	GW

L Number	Hits	Search Text	DB	Time stamp
1	67	(349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))) and (349/43 or 349/42)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/01 11:55
2	53	((349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))) and (349/43 or 349/42)) and capacit$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/01 11:11
3	46	(((349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))) and (349/43 or 349/42)) and capacit$5) and ((light near3 (block$4 or shield$4)) or (black adj matrix))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/01 12:02
4	1	((((349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))) and (349/43 or 349/42)) and capacit$5) and ((light near3 (block$4 or shield$4)) or (black adj matrix))) and groove	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/01 12:02
-	1552	349/43	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/29 14:02
-	2289	349/42	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/29 14:06
-	154	349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/29 14:08
-	3241	349/43 or 349/42	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/29 14:08
-	1	((349/$ and substrate and (((gate or scan$4) and (data or signal$4 or source or drain)) near5 line) and ((thin near3 film) or tft) and (pixel near3 electrode) and ((gate or scan$4) near9 (broad or narrow or taper))) and (349/43 or 349/42)) and groove and capacit$4 and ((light near3 shield$3) or (black near3 matrix))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/29 14:09

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1032037/1

If more than 150 claims or 10 actions staple additional sheet here

(LEFT INSIDE)

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10320371

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20=	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	740.00
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	740

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	=
Independent	* 2	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT FEE		OR	TOTAL ADDIT FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

#4

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002



Attn: Box Missing Parts

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

RESPONSE TO NOTICE TO FILE MISSING PARTS WITH DECLARATION AND TRANSLATION

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In response to the Notice to File Missing Parts of Application - Filing Date Granted (copy attached) mailed on February 6, 2003, submitted herewith are the executed Declaration of the inventor(s) and, upon information and belief, an accurate translation of the application. Any specification attached to and referenced in the Declaration is a copy of the specification and any amendments thereto which were filed in the Office in order to obtain a filing date for the application.

☒ A preliminary amendment is also attached.

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER TRANSLATION	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	*18 MINUS	**20	=0	x 9	$		x 18	$ 0
INDEP CLAIMS	* 2 MINUS	***3	=0	x 42	$		x 84	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140	$	OR	+280	$ 0
					$			$ 0

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

Attached is our Check No. 140038 for ☒$260.00 ☐$195.00 (entitlement to small entity status is asserted) for the fee under 37 C.F.R. §1.16(e) and §1.17(k) and any excess claim fees noted above.

Submitted herewith are 21 sheets of formal drawings (Figs. 1-22) in compliance with 37 C.F.R. 1.84.

Entry of these documents should complete all of the filing formalities and fully satisfy all requirements of the Notice to File Missing Parts. Examination and allowance of this application in due course are respectfully solicited.

The Director is hereby authorized to charge any additional fee (or credit any overpayment) associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this paper are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: March 12, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 10/320,371

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Docket No.: 114542

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☒ A preliminary amendment is also attached.

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER TRANSLATION	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	*18 MINUS	**20	=0	x 9	$		x 18	$ 0
INDEP CLAIMS	* 2 MINUS	***3	=0	x 42	$		x 84	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140	$	OR	+280	$ 0
					$			$ 0

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

Attached is our Check No. 140038 for ☒$260.00 ☐$195.00 (entitlement to small entity status is asserted) for the fee under 37 C.F.R. §1.16(e) and §1.17(k) and any excess claim fees noted above.

Submitted herewith are 21 sheets of formal drawings (Figs. 1-22) in compliance with 37 C.F.R. 1.84.

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James A. Oliff
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UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/320,371	12/17/2002	Masao Murade	114542

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

OIPE JC26 MAR 12 2003 PATENT & TRADEMARK OFFICE

CONFIRMATION NO. 1588
FORMALITIES LETTER

OC000000009488934

Date Mailed: 02/06/2003

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- The application was filed in a language other than English. Applicant is required to provide an English translation of the specification and a statement that the translation is accurate. (See 37 CFR 1.52(d)).
- Applicant must file an English translation of the application, the $ 130 fee set forth in 37 CFR 1.17(i), unless previously submitted, and a statement that the translation is accurate (37 CFR 1.52(d)).
- Because your specification was filed in a language other than English, the Office was unable to determine the number of claims submitted. Additional claim fees may be due once the number of claims can be determined.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
  - The drawing figures contain text that is not in English (including, for example, a flow chart that was originally not in English that has been marked up to include the English text) (see 37 CFR 1.84(p)(2) and 37 CFR 1.52(d)(1)). See Figure(s) All.

03/17/2003 AWONDAF1 00000111 10320371

01 FC:1051 130.00 OP
02 FC:1053 130.00 OP

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$260** for a Large Entity

- **$130** Late oath or declaration Surcharge.
- **$130** for English translation surcharge required.

A copy of this notice MUST be returned with the reply.

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Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

receipt / #7

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE



Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

REQUEST FOR CORRECTION OF PALM RECORDS

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: March 12, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC26 MAR 12 2003 PATENT & TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/320,371	12/17/2002		740	114542	21	18	2

CONFIRMATION NO. 1588

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

FEB 10 2003

FILING RECEIPT

OC000000009488933

Date Mailed: 02/06/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Masao Murade, Suwa-shi, JAPAN;

Assignment For Published Patent Application

Seiko Epson Corporation, Tokyo, JAPAN;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2002-000713 01/07/2002
JAPAN 2002-363864 12/16/2002

If Required, Foreign Filing License Granted: 02/06/2003

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title Electro- device apparatus
~~Electric~~ optical ~~apparatus~~ and electronic ~~device~~

MAR 12 2003
PATENT & TRADEMARK OFFICE

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Yoshikatsu TSUJINO, residing at 3-461-6, Nishihatsuishi Nagareyama-shi, Chiba-ken, 270-0121 Japan, declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the Japanese document entitled "ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS" from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese document to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: December 27, 2002

Yoshikatsu Tsujino

Yoshikatsu TSUJINO

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/320,371	12/17/2002	Masao Murade	114542

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320



CONFIRMATION NO. 1588
FORMALITIES LETTER

OC000000009488934

Date Mailed: 02/06/2003

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- The application was filed in a language other than English. Applicant is required to provide an English translation of the specification and a statement that the translation is accurate. (See 37 CFR 1.52(d)).
- Applicant must file an English translation of the application, the $ 130 fee set forth in 37 CFR 1.17(i), unless previously submitted, and a statement that the translation is accurate (37 CFR 1.52(d)).
- Because your specification was filed in a language other than English, the Office was unable to determine the number of claims submitted. Additional claim fees may be due once the number of claims can be determined.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
  - The drawing figures contain text that is not in English (including, for example, a flow chart that was originally not in English that has been marked up to include the English text) (see 37 CFR 1.84(p)(2) and 37 CFR 1.52(d)(1)). See Figure(s) All.

03/17/2003 AWONDAF1 00000111 10320371

01 FC:1051 130.00 OP
02 FC:1053 130.00 OP

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$260** for a Large Entity

- **$130** Late oath or declaration Surcharge.
- **$130** for English translation surcharge required.

A copy of this notice MUST be returned with the reply.

Customer Service Center
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PART 2 - COPY TO BE RETURNED WITH RESPONSE

10320371 - 031203

#4

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002

OIPE JC26 MAR 12 2003 PATENT & TRADEMARK OFFICE

Attn: Box Missing Parts

Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

RESPONSE TO NOTICE TO FILE MISSING PARTS WITH DECLARATION AND TRANSLATION

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In response to the Notice to File Missing Parts of Application - Filing Date Granted (copy attached) mailed on February 6, 2003, submitted herewith are the executed Declaration of the inventor(s) and, upon information and belief, an accurate translation of the application. Any specification attached to and referenced in the Declaration is a copy of the specification and any amendments thereto which were filed in the Office in order to obtain a filing date for the application.

☒ A preliminary amendment is also attached.

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER TRANSLATION	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	*18 MINUS	**20	=0	x 9	$		x 18	$ 0
INDEP CLAIMS	* 2 MINUS	***3	=0	x 42	$		x 84	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140	$	OR	+280	$ 0
					$			$ 0

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

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*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

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Attached is our Check No. 140038 for ☒$260.00 ☐$195.00 (entitlement to small entity status is asserted) for the fee under 37 C.F.R. §1.16(e) and §1.17(k) and any excess claim fees noted above.

Submitted herewith are 21 sheets of formal drawings (Figs. 1-22) in compliance with 37 C.F.R. 1.84.

Entry of these documents should complete all of the filing formalities and fully satisfy all requirements of the Notice to File Missing Parts. Examination and allowance of this application in due course are respectfully solicited.

The Director is hereby authorized to charge any additional fee (or credit any overpayment) associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this paper are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: March 12, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
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Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re the Application of

Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002 Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE ABSTRACT:

Please replace the Abstract with the Substitute Abstract attached hereto.

IN THE SPECIFICATION:

Please replace the specification with the Substitute Specification attached hereto.

IN THE CLAIMS:

Please replace claims 1-18 as follows:

1. (Amended) An electro-optical device, comprising:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines; and

pixel electrodes formed correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion facing a channel area of a respective thin-film transistor and a narrow width portion in another portion.

2. (Amended) The electro-optical device according to claim 1, the broad width portion having a portion lengthened from the narrow width portion.

3. (Amended) The electro-optical device according to claim 1, the broad width portion having a portion connected to the narrow width portion.

4. (Amended) The electro-optical device according to claim 1, the respective scanning line extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending in a single direction or bi-direction in which the channel area extends.

5. (Amended) The electro-optical device according to claim 1, the pixel electrodes being arranged in a matrix shape, and

the respective channel area being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected.

6. (Amended) The electro-optical device according to claim 5, the narrow width portion being formed at a position deviated from a center of the first gap, and

the broad width portion being formed at the center of the first gap in the intersecting area.

7. (Amended) The electro-optical device according to claim 6, the broad width portion being formed at a center of the second gap in the intersecting area.

8. (Amended) The electro-optical device according to claim 1, grooves being formed in the substrate along the scanning lines, and the scanning lines being buried at least partially in the grooves directly or through an interlayer insulating film.

9. (Amended) The electro-optical device according to claim 8, the narrow width portion having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode being positioned high along the scanning line due to the non-buried portion.

10. (Amended) The electro-optical device according to claim 1, further comprising a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film to constitute the storage capacitor,

the capacitive line having a main line portion extending along the scanning line and a portion extending along the data line, and

a width of the portion extending along the data line in the capacitive line being equal to or broader than that of the data line.

11. (Amended) The electro-optical device according to claim 10, a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Amended) The electro-optical device according to claim 11, the capacitive line being arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. (Amended) The electro-optical device according to claim 11, for each thin-film transistor, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. (Amended) The electro-optical device according to claim 10, a portion overlapping the thin-film transistor in the data line being formed locally broad, and

a width of the portion extending along the data line in the capacitive line being broader than a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. (Amended) The electro-optical device according to claim 14, the capacitive line being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line being formed broad in a portion in which a contact hole to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. (Amended) The electro-optical device according to claim 14, for each of the thin-film transistors, the data line being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17. (Amended) The electro-optical device according to claim 1, further comprising another substrate opposing the substrate through an electro-optical material and a light-shielding film formed on the another substrate,

widths of the data line and a portion extending along the data line in the capacitive line being narrower than that of the light-shielding film.

18. (Amended) An electronic apparatus, comprising:

an electro-optical device including:

a substrate;

scanning lines above the substrate and extending in a predetermined direction;

data lines above the substrate and extending in a direction intersecting the scanning lines;

thin-film transistors provided correspondingly to intersecting areas of the scanning lines and the data lines; and

pixel electrodes provided correspondingly to the thin-film transistors;

a respective scanning line having a broad width portion as a gate electrode in a portion opposing a channel area of a respective thin-film transistor and a narrow width portion in another portion.

REMARKS

Claims 1-18 are pending. By this Preliminary Amendment, the Abstract and specification are replaced with a Substitute Abstract and Substitute Specification, and claims 1-18 are amended.

The attached Appendix includes marked-up copies of the specification (37 C.F.R. §1.125(b)(2)) and each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Prompt and favorable examination on the merits is respectfully requested.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Attachments:
Substitute Abstract
Appendix
Substitute Specification
Marked-up Copy of Specification

Date: March 12, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

ABSTRACT OF THE DISCLOSURE

An electro-optical device of the present invention includes pixel electrodes, TFTs electrically connected to the pixel electrodes, and scanning lines and data lines connected to the TFTs on a TFT array substrate. Each scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the TFT and the narrow width portion. As a result, an electro-optical device capable of easily adjusting an arrangement of the gate electrodes and the scanning lines and at the same time precisely driving the TFTs is provided.

APPENDIX

Changes to Abstract:

The following is a marked-up version of the amended Abstract.

ABSTRACT OF THE DISCLOSURE

An electro-optical device of the present invention ~~comprising~~ includes pixel electrodes, TFTs electrically connected to the pixel electrodes, and scanning lines and data lines connected to the TFTs on a TFT array substrate ~~is disclosed~~. Each scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the TFT and the narrow width portion.

———As a result, an electro-optical device capable of easily adjusting an arrangement of the gate electrodes and the scanning lines and at the same time precisely driving the TFTs is provided.

Changes to Specification:

A Substitute Specification, and a marked up version thereof showing all changes to the specification of record, are attached in accordance with 37 C.F.R. 1.125(b)(2).

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (Amended) An electro-optical device, comprising, ~~above a substrate,~~:

a substrate;

scanning lines above the substrate and extending in a predetermined direction, ~~;~~

data lines above the substrate and extending in a direction intersecting the scanning lines, ~~;~~

thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, ~~;~~ and

pixel electrodes formed correspondingly to the thin-film transistors, ~~;~~

~~wherein the~~ a respective scanning line ~~has~~ having a broad width portion as a gate electrode in a portion facing a channel area of ~~the~~ a respective thin-film transistor and a narrow width portion in ~~the~~ another portion.

2. (Amended) The electro-optical device according to claim 1, ~~wherein~~ the broad width portion ~~has~~ having a portion lengthened from the narrow width portion.

3. (Amended) The electro-optical device according to claim 1, ~~wherein~~ the broad width portion ~~has~~ having a portion connected to the narrow width portion.

4. (Amended) The electro-optical device according to claim 1, ~~wherein~~ the respective scanning line ~~extends~~ extending in a direction intersecting a direction in which the channel area extends, and the broad width portion extending~~extends~~ in a single direction or bi-direction in which the channel area extends.

5. (Amended) The electro-optical device according to claim 1, ~~wherein~~ the pixel electrodes ~~is~~ being arranged in a matrix shape, and

~~wherein~~ the respective channel area ~~is~~ being formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected.

6. (Amended) The electro-optical device according to claim 5, ~~wherein~~ the narrow width portion ~~is~~ being formed at a position deviated from a center of the first gap, and

the broad width portion ~~is~~ being formed at the center of the first gap in the intersecting area.

7. (Amended) The electro-optical device according to claim 6, ~~wherein~~ the broad width portion ~~is~~ being formed at a center of the second gap in the intersecting area.

8. (Amended) The electro-optical device according to claim 1, ~~wherein~~ grooves ~~are~~ being formed in the substrate along the scanning lines, and the scanning lines ~~are~~ being buried at least partially in the grooves directly or through an interlayer insulating film.

9. (Amended) The electro-optical device according to claim 8, ~~wherein~~ the narrow width portion ~~has~~ having a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode ~~is~~ being positioned high along the scanning line due to the non-buried portion.

10. (Amended) The electro-optical device according to claim 1, further comprising a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode ~~for constructing~~to construct a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film ~~for constituting~~to constitute the storage capacitor,

~~wherein~~ the capacitive line ~~has~~ having a main line portion extending along the scanning line and a portion extending along the data line, and

a width of the portion extending along the data line in the capacitive line ~~is~~ being equal to or broader than that of the data line.

11. (Amended) The electro-optical device according to claim 10, ~~wherein~~ a portion overlapping the thin-film transistor in the data line ~~is~~ being formed locally broad, and

~~wherein~~ a width of the portion extending along the data line in the capacitive line ~~is~~ being broader than ~~that~~ a width of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. (Amended) The electro-optical device according to claim 11, ~~wherein~~ the capacitive line ~~is~~ being arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line ~~is~~ being formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. (Amended) The electro-optical device according to claim 11, ~~wherein,~~ for each thin-film transistor, the data line ~~is~~ being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. (Amended) The electro-optical device according to claim 10, ~~wherein~~ a portion overlapping the thin-film transistor in the data line ~~is~~ being formed locally broad, and

a width of the portion extending along the data line in the capacitive line ~~is~~ being broader than ~~that~~ a width of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. (Amended) The electro-optical device according to claim 14, ~~wherein~~ the capacitive line ~~is~~ being arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line ~~is~~ being formed broad in a portion in which a contact hole ~~for connecting~~ to connect to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. (Amended) The electro-optical device according to claim 14, ~~wherein~~ for each of the thin-film transistors, the data line ~~is~~ being formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17. (Amended) The electro-optical device according to claim 1, further comprising another substrate opposing the substrate through an electro-optical material and a light-shielding film formed on the another substrate,

~~wherein~~ widths of the data line and a portion extending along the data line in the capacitive line ~~is~~ being narrower than that of the light-shielding film.

18. (Amended) An electronic apparatus, comprising:

an electro-optical device ~~having, above~~including:

a substrate~~,~~;

scanning lines above the substrate and extending in a predetermined direction~~,~~;

data lines above the substrate and extending in a direction ~~of~~ intersecting the scanning lines~~,~~;

thin-film transistors provided correspondingly to intersecting areas of the scanning lines and the data lines~~,~~; and

pixel electrodes provided correspondingly to the thin-film transistors~~,~~;

~~wherein the~~a respective scanning line ~~has~~ having a broad width portion as a gate electrode in a portion opposing a channel area of ~~the~~ a respective thin-film transistor and a narrow width portion in ~~the~~ another portion.

interlayer insulating film 42, can be formed to buried the wirings such as the data line 6a or the TFT 30 for performing the leveling process.

According to the electro-optical device of the present embodiment as constructed like the above, since the scanning line 330a has the broad width portion 331a and the narrow width portion 332a and the broad width portion 331a is formed to face the channel area 1a' of the TFT 30, the arrangement between the TFT 30 and the scanning line 330a can be easily adjusted or determined.

For example, the arrangement between the TFTs 30 and the scanning lines 330a in FIG. 2 described above shows an example of a suitable arrangement responsive to the requirement for effectively preventing light from entering the channel areas 1a' of the TFTs 30. In addition, for example, the arrangements shown in FIGs. 5 and 6 can be implemented. FIG. 5 is a diagram with the same purpose as FIG. 2, in which an arrangement of the scanning lines and the TFTs is different from that in FIG. 2, and FIG. 6 illustrates only a shape pattern of the scanning lines shown in FIG. 5, similar to FIG. 4.

In FIGs. 5 and 6, the scanning lines 330a', more specifically, the narrow width portions 332a' are formed at positions deviated from the center of a first long gap extending through a space between the adjacent pixel electrodes 9a sandwiching the scanning lines 330a' therebetween. Further, the broad width portions 331a' are formed to be protruded only upwardly in the Y direction in FIG. 5 and 6. Furthermore, the arranged positions of the channel areas 1a', that is, the arranged positions of the broad width portion 331a' are similar to those in FIG. 2.

This arrangement can improve the quality of display image. The reason thereof is as follows. That is, in the electro-optical device according to the present invention, as described above, the oriented film 16 is provided on the pixel electrodes 9a, and on the surface of the oriented film 16, unevenness due to the "height" of various elements formed

below the oriented film 16 can exist. The above-described "various elements" include the scanning lines 330a' of the present embodiment. FIG. 7 is a sectional view taken along a line B-B' in FIG. 5, in which a convex portion 501 caused by the "height" of the narrow width portion 332a' of the scanning line 330a' is formed on the oriented film 16.

When the convex portion 501 is generated, there is a possibility of further generating nonuniformity in the above-described rubbing process performed on the oriented film 16. This nonuniformity may cause the bad orientation of the liquid crystal and thus the operation failure of the electro-optical device. Therefore, conventionally, by providing the light-shielding film in the vicinity of the above-described convex portion 501, shielding of the incident light was made possible. That is, the incident light reaching the light-shielding film is reflected or absorbed by the light-shielding film and thus does not contribute to the image display.

At this time, it is important that the above-described light-shielding film should be provided while satisfying the requirements for improving the pixel opening ratio. That is, when the light-shielding film is provided only to correspond to the convex portion 501, it may unnecessarily worsen the pixel opening ratio to deteriorate the brightness of image. When the light-shielding film is provided only in a part of the convex portion 501, sufficient light-shielding cannot be accomplished and may cause the deterioration of the contrast ratio. In addition, the influence of the nonuniformity in the convex portion 501 may lead to the operation failure of the electro-optical device.

In the present embodiment, it has been paid attention to the fact that the nonuniformity are generated in the convex portion 501, more specifically, that the portion (reference numeral 501a in FIG. 7, hereinafter, referred to as "rubbing-up portion 501a") associated with rubbing up the convex portion 501 (that is, the direction ascending the convex portion 501) and the portion (reference numeral 501b in FIG. 7, hereinafter,

~~referred to as a~~ "rubbing-down portion 501b") associated with rubbing down the convex portion 501 (that is, the direction descending the convex portion 501), have nonuniformity different from each other.

More specifically, for example, it has been paid attention to the fact that it is more difficult to generate the nonuniformity in the rubbing-up portion 501a than in the rubbing-down portion 501b, that is, the rubbing-down portion 501b has the higher possibility of causing the bad orientation of the liquid crystal.

In the present embodiment, it is important that the narrow width portions 332a' adjacent in the direction of the scanning lines 330a' in FIG. 5 are formed at the position deviated from the center (see the two-dotted chain line in FIG. 7) between the pixel electrodes 9a. That is, by forming the narrow width portion 332a' at the position shown in FIG. 7, a vertex 501P of the convex portion 501 caused by the narrow width portion 332a' is also formed at the position deviated from the center between the adjacent pixel electrodes 9a. This means that it is possible to construct only almost half of the sloping surface of the convex portion 501 on the area corresponding to the first gap, that is, the rubbing-down portion 501b on the area. Further, in this case, as shown in FIG. 7, by providing the light-shielding capacitive line 300 and the junction layer 71 corresponding to the space between the adjacent pixel electrodes 9a, it is possible to effectively shield only the rubbing-down portion 501b, that is, to effectively shield the corresponding portion of the convex portion 501 expected to be most influenced by the nonuniformity.

As a result, according to the present embodiment, since the operation failure of the electro-optical device caused by the nonuniformity can be substantially prevented, and since the rubbing-up portion 501a of the convex portion 501 is not expected to be influenced by the nonuniformity remains to transmit the light contributing to the image display, it is possible to ~~improve~~ the pixel opening ratio, that is, to maintain the bright

image. Consequently, according to the present embodiment, from the above-described point of view, an improvement in the quality of the display image can be obtained.

Further, by forming the narrow width portion 332a' at the position deviated from the center of the first gap, it is possible to improve the degree of freedom in the design of the electro-optical device and to effectively prevent the light from entering the TFT 30. The reason thereof is as follows.

That is, although the narrow width portion 332a' in the present embodiment extends through the first gap between the adjacent pixel electrodes 9a, it does not exist at the center thereof. For this reason, for example, by using an area not provided with the narrow width portion 332a' in the first gap, other wirings such as the capacitive line 300 made of the same film as the narrow width portion 332a' can be formed parallel to the narrow width portion 332a' from a plan view. That is, the degree of freedom in design can be increased.

Further, in the above-described case, although the narrow width portion 332a' is deviated from the center line, by adjusting the width of the broad width portion 331a', for example, by broadening only one side thereof or by broadening one side thereof more than the other side, it is possible to arrange the broad width portion 331a' as the gate electrode at the center of the gap. In the present embodiment, as shown in FIGs. 5 and 6, it can be understood that the broad width portion 331a' is broadened toward only one side. Hence, since the gate electrode can be arranged at a position advantageous for improving the light-shielding ability irregardless of the position of the scanning line 330a', or since the scanning line 330a' can be arranged at an arbitrary position in the gap while arranging the gate electrode at a position advantageous for improving the light-shielding ability, it is possible to increase the degree of freedom in an arrangement of wirings such as an arrangement of the scanning line 330a' and to obtain the TFT 30 originally having a

substantially high light-shielding ability.

In short, in the embodiment shown in FIGs. 5 and 6, while satisfying the requirements for improving the quality of the display image, improving the degree of freedom in design and decreasing the light leak current in the TFT 30, it is possible to adequately adjust/determine the arrangement between the channel area 1a' (or the TFT 30) and the gate electrode (or the scanning line 330).

As described above, according to the electro-optical device of the present embodiment, since the scanning line, as the gate electrode, has the broad width portion and the narrow width portion, while satisfying the above various requirements or a general requirement such as high precision of the electro-optical device itself, it is possible to adequately adjust/determine the arrangement between the channel area (or the TFT) and the gate electrode (or the scanning line).

(Second embodiment)

Now, a second embodiment of the present invention will be explained with reference to FIGs. 8 to 11. FIGs. 8 and 10 are diagrams with the same purpose as FIG. 2, respectively, and illustrates another embodiment different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10 and at least a part of the scanning line is buried in the groove. FIGs. 9 and 11 are perspective views illustrating a profile of the narrow width portion of the scanning line according to the second embodiment, respectively (FIG. 9 corresponds to FIG. 8, and a section taken along a line Z1-Z1' in FIG. 8 corresponds to a section taken along a line Z1-Z1' in FIG. 9. Further, FIG. 11 corresponds to FIG. 10, and a section taken along a line Z2-Z2' in FIG. 10 corresponds to a section taken along a line Z2-Z2' in FIG. 9). Further, FIG. 12 is a sectional view taken along a line T-T' in FIG. 10. Furthermore, since the basic construction and operation, etc., of the electro-optical device of the second embodiment are similar to those of the first

embodiment, explanation about distinctive portions in the second embodiment will be mainly described below. Furthermore, the reference numerals in FIGs. 8 and 12 indicate the same elements as in FIGs. 1 to 7 referred to in the above description, when they indicate substantially equivalent elements.

First, in one aspect of the second embodiment, as shown in FIGs. 8 and 9, a groove 3G1 is formed along the scanning line in the TFT array substrate 10. The groove 3G1 is formed except for the area where the semiconductor layer 1a of the TFT 30 is formed. By this construction, in consideration of only the grooves, the grooves 3G1 are arranged in a matrix shape from a plan view (see FIG. 8). Further, a scanning line 340a is formed such that the narrow width portion 342a thereof is entirely buried in the groove 3G1 (see FIG. 9).

In another aspect of the second embodiment, as shown in FIGs. 10 and 11, a groove 3G2 is formed on the TFT array substrate 10, similarly to the groove 3G1. However, preferably, a groove 3G2 is formed slightly narrower than the groove 3G1. Further, a narrow width portion 352a of the scanning line 350a is formed along the groove 3G2. The narrow width portion 352a has a buried portion 352aB of which a part is buried in the groove 3G2 and a non-buried portion 352aNB which is not buried in the groove 3G2 and extends parallel to the buried portion 352aB. The non-buried portion 352aB is formed on the surface of the TFT array substrate 10.

Further, in one aspect and another aspect of the second embodiment, as shown in FIGs. 8 and 10, a groove 6G1 is formed in the TFT array substrate 10 along the data line. Furthermore, the data line 6a is formed to be entirely buried in the groove 6G1. In addition, the semiconductor layer 1a is also formed to be entirely buried in the groove 6G1.

According to the electro-optical device of the second embodiment constructed as above, the following effects can be obtained. First, since the whole part or a part of both

of the scanning lines 340a and 350a are buried in the grooves 3G1 or 3G2, as shown in FIGs. 9 and 11, in this buried portion, the surface height of the base insulating film 12 and the height of the buried portion 352aB of the scanning line 340a and the scanning line 350a are almost equal to each other to maintain the leveling feature. By this, the leveling feature of the first to third interlayer insulating film 41 to 43 formed as the upper layers of the scanning lines 340a and 350a, or the pixel electrode 9a and the oriented film 16 can be well obtained. Therefore, in the second embodiment, for example, since a step along the narrow width portion 342a or the buried portion 352aB does not substantially appear on the surface of the oriented film 16, the rubbing process can be very suitably performed on the oriented film 16 and the bad orientation can be drastically prevented. Furthermore, an effect can be obtained that the light leakage caused by the bad orientation and deterioration of the image quality based on the light leakage.

Such effects on the portion along the data line 6a can be obtained because of the existence of the groove 6G1.

Further, in FIGs. 10 and 11, in particular, because of the existence of the non-buried portion 352aNB, the following effects can be obtained. Now, the effects will be explained in detail.

First, in the electro-optical device of the present embodiment, generally in order to prevent deterioration of the electro-optical material caused by the application of DC voltage and to prevent the cross-talk or flicker in the displayed image, an inverse driving method of inversing the polarities of voltages applied to the respective pixel electrodes 9a in a predetermined rule may be employed. More specifically, so-called "1H inverse driving method" will be explained.

First, as shown in FIG. 13(a), during the time for displaying image signals for the n-th field (n is a natural number) or frame, the polarity of the liquid crystal driving voltage

indicated by + or - for each pixel electrode 9a is driven with the same polarity for every row. Thereafter, as shown in FIG. 13(b), when the image signals for the n+1-th field or frame are displayed, the polarity of the liquid crystal driving voltage for each pixel electrode 9a is inversed and during the time for displaying the image signal of the n+1th field or one frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is not inversed, and each pixel electrode is driven with the same polarity for every row. Then, the state shown in FIG. 13(a) and 13(b) is repeated at the period of one field or one frame. This is the 1H inverse driving method. As a result, while avoiding deterioration of the liquid crystal caused by the application of DC voltage, it is possible to prevent image display with reduced cross-talk or flicker. Further, the 1H inverse driving method is more advantageous than the 1S inverse driving method to be explained later, in that there is no almost cross-talk in the vertical direction (Y direction) in the drawing.

However, as can be understood from FIG. 13(a) and FIG. 13(b), in the 1H inverse driving method, a horizontal electric field takes place between the pixel electrodes 9a adjacent to each other in the vertical direction (Y direction) in the drawing. In these drawings, an area C1 where the horizontal electric field takes place is always in the vicinity of the gap between the pixel electrodes adjacent to each other in the Y direction. If such horizontal electric field is applied, for the electro-optical material to which a vertical electric field, i.e., an electric field perpendicular to the surface of the substrate, is applied, between the pixel electrode and the opposing electrode facing each other, the operation failure can be caused by the bad orientation of the liquid crystal in the electro-optical material and by the light leakage in the portion, which leads to a problem of decreasing the contrast ratio.

With respect to the above, the area where the horizontal electric field is generated

can be covered by the light-shielding film. However, in this case, there is a problem that the opening area of pixels becomes narrow in respect to the area where the horizontal electric field is generated. In particular, as the distance between the adjacent pixel electrodes becomes small due to minuteness of the pixel pitch, such horizontal electric field increases, and thus this poses a serious problem in higher precision electro-optical device.

In the aspect shown in FIGs. 10 and 11 of the second embodiment, a step caused by the height of the non-buried portion 352aNB is formed between the pixel electrodes 9a (that is, the adjacent pixel electrodes 9a to which voltage of inverse polarity is applied) adjacent to each other in the vertical direction. Because of the existence of this step, it is possible to intensify the vertical electric field in the vicinity of an edge portion of the pixel electrode 9a arranged on the step and to weaken the horizontal electric field. More specifically, as shown in FIG. 12, the distance between the vicinity of the edge portion of the pixel electrode 9a arranged on the step 430 and the opposing electrode 21 becomes narrower by the height of the step 430. Therefore, in the area C1 where the horizontal electric field is generated, the vertical electric field between the pixel electrode 9a and the opposing electrode 21 can be intensified. Furthermore, in FIG. 12, since the gap between the adjacent pixel electrodes 9a is constant, the intensity of the horizontal electric field to be intensified with the gap getting narrow is constant. Therefore, by making the vertical electric field more prevalent in the area C1 where the horizontal electric field is generated, it is possible to prevent the bad orientation of the liquid crystal caused by the horizontal electric field. Furthermore, because of the step 430 made of the insulating film, the intensity of the horizontal electric field is weakened, and the portion of the liquid crystal affected by the horizontal electric field is decreased by the amount of replacing the step where the horizontal electric field exists. Therefore, the influence of the horizontal

electric field on the liquid crystal layer 50 can be reduced.

Further, in the above description, the 1H inverse driving method has been explained but the present invention is not limited to such driving method. For example, 1S inverse driving method of inversing the voltage polarity at a period of a frame or a field for each column while driving pixel electrodes in a column with the potential of the same voltage polarity may be employed in the present invention as the inverse driving method of which control is relatively easy and which enables the high quality image display. Furthermore, between the pixel electrodes adjacent to each other in both of the column direction and the row direction, the dot inverse driving method of inversing the voltage polarity applied to each pixel electrode has been developed and can be applied to the present invention.

Further, in the second embodiment, as shown in FIG. 2, the aspect in which the narrow width portion 342a and 352a is formed to extend through the center of the first gap between the adjacent pixel electrodes 9a has been explained. However, the present invention is not limited to such construction. That is, as shown in FIGs. 5 and 6, in the aspect where the narrow width portion is formed to extend at the position deviated from the center of the first gap, the grooves 3G1 or 3G2 shown in FIGs. 8 to 11 may be ~~comprised~~ formed in a combination. For example, the construction shown in FIGs. 14 and 15 may be employed. FIG. 14 is a ~~view with the same purpose as FIG. 2 and~~ plan illustrating another aspect different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10, and the narrow width portion of the scanning line is deviated from the center of the first gap, and FIG. 15 is a sectional view taken along ~~a line~~ plane T-T' in FIG. 14.

FIG. 14 is similar to FIGs. 5 and 6 in that a narrow width portion 362a of a scanning line 360a is deviated from the center of the long first gap extending through the space between the adjacent pixel electrodes 9a, but FIG. 14 is different from FIGs. 5 and 6

in that the narrow width portion 362a is formed along a groove 3G1' formed on the TFT array substrate 10 and a broad width portion 361a is formed to protrude only downwardly in FIG. 14. In this construction, the narrow width portion 362a of the scanning line 360a is formed from the upper portion in the drawing as seen from the center of the first gap and thus the narrow width portion 362a is formed to be positioned right below the contact hole 85 for connecting the pixel electrode 9a and the junction layer 71. Further, the narrow width portion 362a is formed to be entirely buried in the groove 3G1'.

According to this construction, as shown in FIG. 15, the contact hole 85 is formed on the scanning line 360a formed to be buried in the groove 3G1'. In other words, it is possible to form the contact hole 85 on the assumption that the step caused by the height of the scanning line 360a does not substantially appear on the surface of the third interlayer insulating film 43.

In such construction shown in FIGs. 14 and 15, in particular, an advantage from the contact hole 85 which can be easily and securely formed can be obtained. That is, assuming that a step due to the height of the scanning line or the narrow width portion is generated on the surface of the third interlayer insulating film 43, there is a possibility of a disadvantage in that the contact hole 85 may be formed on the vertex or on the ridge of the step. The present construction overcomes such drawback.

The above effects can be understood from the following point of view. That is, in the second embodiment, since the whole or a part of the scanning line is buried in the groove, and thus a step due to the height of the scanning line does not substantially appear on the surface of the respective interlayer insulating film, the formation position or the extending position of the scanning line need not be considered particularly. In other words, if the scanning line is between the adjacent pixel electrodes in the direction thereof, the scanning line may be formed at any position. This is because even when the

formation position or extending position of the scanning line is selected freely and the contact hole is formed thereon, as described above, the contact hole can be relatively easily and securely formed due to the absence of the step.

Further, in case the narrow width portion has both the buried portion and the non-buried portion, it is preferable to form the groove such that the buried portion is positioned right below the contact hole 85. FIG. 12 corresponds to an example of such construction.

(Third embodiment)

Now, a third embodiment of the present invention will be explained with reference to FIGs. 16 to 19. FIG. 16 is a diagram with the same purpose as FIG. 2 and illustrates another aspect that a shape of the data line is different from that in FIG. 2. FIG. 17 is a sectional view taken along a line P-P' in FIG. 16, FIG. 18 is a sectional view taken along a line Q-Q' in FIG. 16, and FIG. 19 is a sectional view taken along a line R-R' in FIG. 16. Further, since the basic construction and operation of the electro-optical device of the third embodiment are similar to those of the first embodiment, explanation about distinguishing features of the third embodiment will be mainly described below. Furthermore, reference numerals in FIGs. 16 to 19 indicate the same elements as in FIGs. 1 to 15 referred to in the above description, when they indicates substantially equivalent elements.

In the third embodiment, as shown in FIGs. 16 to 19, a data line 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad. Further, a width W1 of a portion extending along the data line 6a1 in the capacitive line 300, that is, the protruded portion 302, first, is broader than a width W2' of the portions except for the broad width portion 6aW in the data line 6a1 (in particular, see FIG. 17). Second, the width W1 of the protruded portion 302 is almost equal to a width W6 of the broad width portion 6aW in the data line 6a1 (see FIG. 18). The channel area

1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width direction 6aW and almost at the center in the width direction of the scanning line 3a. Furthermore, in the third embodiment, as shown in FIGs. 16, 18 and 19, the broad width portion 6aW of the data line 6a1 is formed continuously from the portion overlapping the TFT 30 to the portion in which the contact hole 81 for connecting the semiconductor layer 1a of the TFT and the data line 6a is provided, for each TFT 30 arranged in a matrix shape. In addition, in the third embodiment, as shown in FIGs. 17 to 19, the light-shielding film 23 is formed on the opposing substrate 20. A width WS of one-by-one lattice of the light-shielding film 23 is greater than that of the broad width portion 6aW.

In the electro-optical device of the third embodiment constructed like the above, the following effects can be obtained. That is, first, since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 which is formed broad exist on the TFT 30, so called a double light-shielding effect can be obtained. Therefore, it is difficult for the light to enter the channel area 1a' of the TFT 30, and thus the light leak current can be minimized.

In particular, in the third embodiment, the broad width portion 6aW of the data line 6a also exists on the TFT 30 while overlapping the capacitive line 300. In this case, on the TFT 30, the light-shielding ability corresponding to the integrated value of their transmittances can be obtained. Further, since the channel area 1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width portion 6aW and almost at the center in the width direction of the scanning line 3a, the light-shielding ability can be enhanced.

Second, in connection with such excellent light-shielding ability, in the third embodiment, as described above, the width W1 of the protruded portion 302 of the

capacitive line 300 and the width W6 of the broad width portion 6aW of the data line 6a are less than the width WS of the light-shielding film 23 on the opposing substrate 20 (that is, WS>W1, WS>W6). According to this, the light entered from the upper portion of the TFT 30 is first shielded by the light-shielding film 23 and is further shielded by the broad width portion 6aW of the data line 6a. Furthermore, although passing through the broad width portion 6aW, the incident light is next shielded by the protruded portion 302 of the capacitive line 300. In short, in the third embodiment, since triple light-shielding is implemented, it becomes more difficult for the light to enter the TFT 30.

Third, in the third embodiment, the broad width portion 6aW of the data line 6a is formed continuously from the portion overlapping the TFT 30 to the contact hole 81 for each TFT 30 arranged in a matrix shape. Since the contact hole 81 is provided for connecting the semiconductor layer 1a of the TFT 30 and the data line 6a as described above, the capacitive line 300 cannot be formed in the portion. However, in the third embodiment, in the formation position of the contact hole 81, the broad width portion 6aW of the data line 6a exists similarly to the upper portion of the TFT 30. Therefore, deterioration of the light-shielding ability caused by the absence of the capacitive line 300 can be compensated by the existence of the broad width portion 6aW. In this connection, as in the third embodiment, according to the aspect that the broad width portion 6a is formed continuously on the TFT 30 and on the formation position of the contact hole 81, since it is not necessary to broaden exceedingly the formation area of the broad width portion 6aW, it is preferable not to increase the inner reflection.

As described above, in the third embodiment, by means of the combination of various effects, the possibility of the light incidence to the channel area 1a' is drastically decreased, and the generation of the light leak current in the TFT 30 and consequently the generation of the flicker and the like on the image due to the light leak current can be

effectively suppressed.

(The whole construction of the electro-optical device)

The whole construction of the electro-optical device according to the present embodiment constructed like the above will be explained with reference to FIGs. 20 and 21. Further, FIG. 20 is a plan view of the TFT array substrate along with the respective elements formed thereon seen from the opposing substrate 20 side, and FIG. 21 is a sectional view taken along a line H-H' in FIG. 20.

In FIGs. 20 and 21, in the electro-optical device according to the present embodiment, the TFT array substrate 10 and the opposing substrate 20 are arranged opposite to each other. A liquid crystal layer 50 is inserted and sealed between the TFT array substrate 10 and the opposing substrate 20 and the TFT array substrate 10 and the opposing substrate 20 are affixed to each other by means of a sealing material 52 provided in the sealing area positioned around the image display area 10a.

In the outer area of the sealing material 52, a data line drive circuit 101 for driving the data line 6a by supplying image signals to the data line 6a at a predetermined timing, and the external circuit connecting terminals 102 are provided along one side of the TFT array substrate 10, and scanning line drive circuits 104 for driving the scanning line 3a by supplying scan signals to the scanning line 3a at a predetermined timing is provided along two sides adjacent to the one side.

Further, if delay of the scan signals supplied to the scanning line 3a does not matter, the scanning line drive circuit 104 on only one side is sufficient. Furthermore, the data line drive circuit 101 may be arranged on both sides along the sides of the image display area 10a.

The remaining one side of the TFT array substrate 10 is provided with a plurality of wirings 105 for connection between the scanning line drive circuits 104 provided on

both sides of the image display area 10a. Further, at least one corner of the opposing substrate 20 is provided with a conductive material 106 for electrical connection between the TFT array substrate 10 and the opposing substrate 20. Furthermore, as shown in FIG. 21, the opposing substrate 20 having almost the same profile as the sealing material 52 shown in FIG. 20 is bonded to the TFT array substrate 10 through the sealing material 52.

In FIG. 21, after the TFTs for switching pixels, or wirings such as the scanning lines, the data lines are formed on the TFT array substrate 10, and the oriented film is formed on the pixel electrodes 9a. In addition to the opposing electrode 21, the oriented film is formed on the uppermost portion of the opposing substrate 20. Further, the liquid crystal layer 50 is composed of the liquid crystal in which, for example, one kind or several kinds of nematic liquid crystal are mixed, and is oriented in a predetermined state between a pair of oriented films.

Furthermore, on the TFT array substrate 10, in addition to the data line drive circuit 101 and the scanning line drive circuit 104, a sampling circuit for applying image signals to the plurality of data lines 6a at a predetermined timing, a precharge circuit for supplying a precharge signal of a predetermined voltage level to the plurality of data lines prior to the image signals, an inspection circuit for inspecting the quality or defects of the electro-optical device during production thereof or in shipping thereof and the like may be formed.

(Embodiment of electronic apparatus)

Next, for an embodiment of a color display device of a projection type that is an example of an equipment using the above-described electro-optical device as a light bulb, the whole construction thereof, in particular, the optical construction thereof will be explained. Here, FIG. 22 is a diagrammatic sectional view of the color display device of a projection type.

In FIG. 22, a liquid crystal projector 1100 that is an example of the color display device of a projection type in the present embodiment comprises three liquid crystal modules including the liquid crystal device in which the drive circuit is mounted on the TFT array substrate, and further comprises the respective light bulbs 100R, 100G and 100B for RGB. In the liquid crystal projector 1100, when transmitted light is emitted from a lamp unit of white light source such as a metal halide lamp, the light is divided into the light components R, G and B corresponding to the three primary colors RGB by means of three mirrors 1106 and two dichroic mirrors 1108 and guided to the light bulbs 100R, 100G and 100B corresponding to the respective colors, respectively. At this time, in particular, in order to prevent the light loss caused by the long light path, the B light is guided through a relay lens system 1121 composed of an incident lens 1122, a relay lens 1123 and an exit lens 1124. Then, the light components corresponding to the three primary colors modulated, respectively, by the light bulbs 100R, 100G and 100B are synthesized again by a dichroic prism 1112, and then are projected as a color image to a screen 1120 through a projecting lens 1114.

The present invention is not limited to the above-described embodiments but may be appropriately varied without departing from the gist or the spirit of the invention known throughout the claims and the specification. The electro-optical devices including such variation, for example, an electrophoresis apparatus or an electro-luminescence display device, or the electronic apparatus including these electro-optical devices are also included in the technical range of the present invention.

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~~SPECIFICATION~~

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND OF THE INVENTION

entered

1. Field of the invention

The present invention relates to an electro-optical device capable of performing active matrix drive and to an electronic apparatus ~~having the same~~ device. The invention also related incorporating such an electro-optical

2. Description of the related art

~~Conventionally,~~ The related art includes an electro-optical device ~~comprising~~ including a pair of substrates constructed to sandwich an electro-optical material such as a liquid crystal therebetween and electrodes provided in each of the pair of substrates ~~for~~ to applying an electric field to the electro-optical material is ~~known.~~ The electrodes are used ~~for~~ to applying an electric field to the electro-optical material to vary the state of the material. According to such an electro-optical device, for example, when the light emitted from a light source enters the device and the state of the electro-optical material is varied, it is possible to control the light transmittance and thus realize desired image display.

Moreover, in related art electro-optical devices, by providing pixel electrodes arranged in a matrix shape, thin-film transistors (hereinafter ~~referred to as~~ "TFT") connected to the respective pixel electrodes, and scanning lines and data lines connected to each of TFTs and provided in parallel to a row direction and a column direction, respectively, on one of the pair of substrates, ~~it is known that~~ active matrix drive can be performed. As a result, for each pixel defined by the pixel electrodes or the scanning lines and the data lines, it is possible to control the electric field applied to the electro-optical material and to control

the light transmittance.

SUMMARY OF THE INVENTION

However, in conventional electro-optical devices, there are following problems. That is, for an electro-optical device capable of performing the above active matrix drive, it is required to precisely drive the TFTs. However, to precisely drive the TFTs is a difficult task while satisfying the high precision and miniaturization requirements imposed in the current electro-optical device.

A TFT comprises a semiconductor layer having a channel area, a source area and a drain area, and a gate electrode formed through an insulating film to cover at least a part of the channel area of the semiconductor layer. By applying or not applying the electric field to the channel area in accordance with the current applied (or not applied) to the gate electrode, the current flow can be controlled.

At this time, the length of the channel area, referred to as "channel length" or a width thereof, referred to as "channel width", that is, the size of the channel area is, is important for determining the characteristics of TFTs. Further, an arrangement of the gate electrode on the channel area is also a very important factor. In this regard, conventionally, a conductive member electrically connected to the scanning line or a member constituting a part of the scanning line was used as the gate electrode. However, there are problems in arranging the scanning line itself and the channel area.

In short, it is required to realize a suitable arrangement of the channel area (or TFT) and the scanning line (or gate electrode) while realizing the high precision required in the electro-optical devices. Further, it is required to realize the difficult task of precisely operating the TFT constructed as such.

For example, it is not sufficient to drive the electro-optical device only by the TFT

and the scanning line (or the gate electrode) and various elements are additionally required. However, it is generally difficult to accomplish the above arrangement or adjustment in connection with various other elements. Further, in the TFT, there is a disadvantage in that it is required to prevent the light leakage current which is generated by the light entering the channel area. That is, it is preferable that the TFT is arranged as far as possible from a light-transmitting area, which is an area that the light contributes to image display in each pixel emitted through transmission or reflection, more specifically, from the pixel electrode. However, since this should be realized while satisfying the requirement of high precision, there is a further disadvantage in that the above arrangement/adjustment becomes more difficult ~~an even more different~~ task.

The present invention ~~is made in consideration of the above~~ problems. ~~Therefore, an object of the present invention is to~~ provide an electro-optical device capable of easily adjusting the arrangement of a gate electrode and a scanning line and capable of precisely driving TFT and an electronic apparatus ~~comprising~~ the electro-optical device.

In order to solve the above problems, the electro-optical device of the present invention ~~comprises~~, on a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction intersecting the scanning lines, thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes formed correspondingly to the thin-film transistors, ~~wherein~~ the respective scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

According to the electro-optical device of the present invention, by supplying scan signals and image signals to the thin-film transistors through the scanning lines and the data lines, the pixel electrodes can be driven in an active matrix mode.

More specifically, in the present invention, since the scanning lines have the broad width portions as the gate electrode in a portion facing the channel area of the thin-film transistor and the narrow width portion in other portion, it is not only possible to realize the narrowness of the scanning line but also to more easily adjust/determine the arrangement between the channel area (or the thin-film transistor) and the scanning line than in the ~~conventional~~ related art.

For example, when a plurality of pixel electrodes are arranged in a matrix shape, it is generally preferable that the thin-film transistor are configured such that the channel area of the thin-film transistor is positioned at the position farthest from the corner of each pixel electrode, that is, at the center position of a space among adjacent and opposite corners of the pixel electrodes when four pixel electrodes are considered (because it is farthest from the light transmitting area). However, in this case, by allowing the channel area to extend through a space between adjacent pixel electrodes including the center position, it is possible to adequately determine the channel length, and by arranging the scanning line to intersect it, it is possible to realize a structure that the broad width portion of the scanning line exists on the channel area. Therefore, in this case, it is possible to simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices. Further, in this case, the light incidence to the thin-film transistor or the channel area can be prevented as much as possible or reduced under the above-described assumption.

Like the above, according to the present invention, it is possible to adequately adjust the arrangement between the thin-film transistor and the scanning line or the gate electrode while satisfying the high precision requirements of the electro-optical devices.

Further, this structure renders a good outcome even after arrangement of various elements constituting the electro-optical device has been adjusted and determined, in addition to the above scanning line and the thin-film transistor. Furthermore, according to the present invention, it is possible to precisely drive the thin-film transistor, and thus maintain the quality of image to be displayed at high level.

Further, in the present invention, "broad width" means that it is broader than the width of the "narrow width portion" and "narrow width" means that it is narrower than the width of the "broad width portion". In short, broad and narrow degree of "the broad width portion" and the "narrow width portion" is determined in accordance with the relative relationship between them. Furthermore, the real width of the broad width portion or the narrow width portion can be adequately determined theoretically, experimentally or by ~~means of~~ simulation.

In one aspect of the electro-optical device of the present invention, the broad width portion has a portion lengthened from the narrow width portion.

According to this aspect, it is possible to form the scanning line relatively easily having the broad width portion and the narrow width portion. More specifically, for example, by employing the known photolithography and etching methods with the assumption that the broad width portion and the narrow width portion are formed through the incorporated pattern, the scanning line according to the present aspect can be easily formed.

In another aspect of the electro-optical device of the present invention, the broad width portion has a portion connected to the narrow width portion.

According to this aspect, for example, the broad width portion includes the portion formed by connecting a conductive member and the like prepared separately to the narrow width portion. Even in this case, the broad width portion can be formed

relatively easily.

In another aspect of the electro-optical device of the present invention, the scanning line extends in a direction intersecting the direction in which the channel area extends and the broad width portion extends in a single direction or bi-directionally in which the channel area extends.

According to this aspect, since the broad width portion extends in the single direction or bi-directionally in which the channel area extends, it is possible to more adequately adjust the arrangement of the thin-film transistor and the scanning line. Further, according to this aspect, since the gate electrode is adequately formed in accordance with the channel length, the electric field can be more effectively applied to the channel area.

Further, like the above, according to the aspect that the gate electrode, that is, the broad width portion is provided in the portion to be the channel area corresponding to the channel area, for example, the so-called self-aligned formation of the thin-film transistor (that is, formation of the source area and the drain area adjacent to the channel area through an ion implantation process using the gate electrode as a mask) can be easily executed. However, in this case, strictly speaking, the channel area is formed by carrying out the ion implantation process after forming the broad width portion to be the gate electrode.

In another aspect of the electro-optical device of the present invention, the pixel electrodes are arranged in a matrix shape and the channel areas are formed in an intersecting area in which a first long gap extending through a space between pixel electrodes sandwiching of the scanning line and being adjacent to each other and a second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected.

delete space

This aspect is similar to the above mentioned aspect and is one of the aspects in which the operational effect of the present invention is exhibited most effectively.

That is, according to this aspect, the channel area of the thin-film transistor is formed in the intersecting area of the pixel electrodes arranged in a matrix shape. The intersecting area is an area in which the first long gap extending through a space between pixel electrodes sandwiching the scanning line and being adjacent to each other and the second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected in a plan view. By such a configuration, it is difficult for light to enter the channel area.

Further, along with such an operational effect, since the scanning line has the broad width portion as the gate electrode is opposite to the channel area, the arrangement between the channel area (or the thin-film transistor) and the gate electrode (or the scanning line) can be determined most adequately and it is also possible to secure the adequate channel length and narrowness of the scanning line.

In this aspect, in particular, the narrow width portion is formed at a position deviated from a center of the first gap and the broad width portion, is formed at the center of the first gap in the intersecting area.

According to this configuration, the narrow width portion of the scanning line extends through the space between the adjacent pixel electrodes but does not exist at the center thereof and is formed at the position deviated from the center thereof. As a result, first, the ~~improvement~~ enhancement in the quality of the displayed image can be obtained, especially for the liquid crystal display device that is an example of the electro-optical device, and the reason thereof is as follows.

That is, in the present aspect, when performing the rubbing process on a convex portion on the oriented film normally provided in the liquid crystal display device, in

particular, a convex portion formed by "height" of the narrow width portion, nonuniformities are usually generated in the convex portion. Further, it is considered that the degree of nonuniformity is different from each other in the portion associated with the rubbing up convex portion (that is, the direction ascending to the convex portion) and the portion associated with the rubbing down convex portion (that is, the direction descending from the convex portion).

More specifically, for example, it is more difficult to generate nonuniformity in the portion associated with the rubbing up convex portion than in the portion associated with the rubbing down convex portion.

Further, if the nonuniformity is left as it is, a poor orientation of the liquid crystal may be caused to result in the operation failure of the electro-optical devices. In the difference in the degree of nonuniformity between the rubbing-up process and the rubbing-down process, the latter has greater possibility to cause the bad orientation of the liquid crystal than the former.

It is significant that the narrow width portion of the present aspect is formed at a position deviated from the center of the first gap between the pixel electrodes. That is, if the narrow width portion is formed at the above-described position, the vertex of the convex portion caused by the narrow width portion is also formed at the position deviated from the center of the first gap, and this means that it is possible to form almost only half inclined surface of the convex portion on the area corresponding to the first gap, that is, to form only the portion associated with the rubbing-down on the area. Further, in this case, if the light-shielding film is provided corresponding to the first gap, it is possible to effectively shield only the portion associated with the rubbing-down, that is, to effectively shield the corresponding portion of the convex portion to be most influenced by the nonuniformity.

As a result, according to the present aspect, since the operation failure of the electro-optical device caused by nonuniformities can be substantially prevented, and the portion of the convex portion associated with the rubbing-up, which is not affected by nonuniformities, is able to transmit the light contributing to the image display. Thus, it is possible to improve the opening ratio of pixel, that is, to provide a brightened image display. As a result, according to the present aspect, from the above-mentioned point of view, the improvement in the display image can be obtained.

Further, by forming the narrow width portion at the position deviated from the center of the first gap, it is also possible to improve the degree of freedom in designing the electro-optical devices and to more effectively prevent light from entering the thin-film transistor. The reason thereof is as follows.

That is, in the present aspect, the narrow width portion extends through the first gap between the adjacent pixel electrodes, but does not exist at the center thereof. For this reason, by using the area in the first gap where the narrow width portion is not provided, in a plan view, it is possible to provide other wires such as the capacitive line made up of the same film as the narrow width portion, in parallel to the narrow width portion. That is, the degree of freedom of design is increased.

Further, in the above-mentioned case, although the narrow width portion is deviated from the center thereof, it is possible to arrange the broad width portion as the gate electrode at the center of the gap, by adjusting the width of the broad width portion, for example, by broadening only one side or by broadening one side more than the other side small. Like the above, since the gate electrode can be arranged at a position advantageous for increasing the light-shielding ability regardless of the position of the scanning line, or since the scanning line can be arranged at an arbitrary portion in the gap while arranging the gate electrode at the position advantageous for increasing the light-

shielding ability, it is possible to realize a thin-film transistor having a high light-shielding ability while increasing the degree of freedom in arranging wires including the arrangement of the scanning lines.

In this configuration, further, the broad width portion may be formed at the center of the second gap in the intersecting area.

According to such construction, the channel area is formed at the position farthest from the adjacent or opposite corners of the electrodes in accordance with the above-described method, when four pixel electrodes are considered to be used. That is, it becomes very difficult for light to enter the channel area.

In another aspect of the electro-optical device of the present invention, grooves are formed in the substrate along the scanning lines, and the scanning lines are buried at least partially in the grooves directly or through an interlayer insulating film.

According to this aspect, since the scanning line is buried in the groove formed in the substrate, the generation of a step on the surface of the interlayer insulating film formed as the upper layer or on the surface of the pixel electrodes and the oriented film, etc. caused by the height of the scanning line itself can be prevented earlier. That is, the surface can be leveled very well. Then, if the surface of the oriented film is leveled, the rubbing process can be adequately performed for the orientation process and the orientated state of the liquid crystal molecules contacting the oriented film can be maintained well. Therefore, according to the present aspect, since the possibility of bad orientation can be decreased and the light leakage caused by the bad orientation can be markedly prevented, it is possible to display a high-quality image.

In another aspect of the electro-optical device of the present invention, the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion not buried in the groove and extending along the scanning

line in parallel to a buried portion, and a base of the pixel electrode is positioned high along the scanning line due to the presence of the non-buried portion.

According to this aspect, the narrow width portion has both the buried portion and the non-buried portion. Then, the both of the buried portion and the non-buried portion extend along the scanning line and the base of the pixel electrode protrudes above along the scanning line due to the presence of the non-buried portion.

Through this construction, first, the effect associated with the above-described leveling can be similarly obtained by the buried portion. That is, the surface of the interlayer insulating film to be formed as the upper layer of the buried portion, or the surfaces of the pixel electrodes and the oriented film have the an excellent leveled feature, and thus it is possible to reduce the possibility of having the bad orientations.

Next, since the step including the convex portion along the scanning line is formed on the surface of the oriented film to be formed as the upper layer of the non-buried portion and the like, the above-described effects of leveling cannot be obtained by the non-buried portion. However, the following advantages can be obtained.

First, in electro-optical device according to the present invention, for the purpose of preventing deterioration of the liquid crystal, increasing the device life and reducing the cross-talk or flicker of the displayed image, a method of dividing the pixel electrodes into two groups and then inversely driving them in separate cycles may be employed. That is, a plurality of pixel electrodes including a first pixel electrode group to be inversely driven at a first period and a second pixel electrode group to be inversely driven at a second period compensatory with the first period, are arranged in a plain on the substrate. There are (i) the adjacent pixel electrodes to be driven with driving voltages of inverse polarities at the respective times in the inverse-driving and (ii) the adjacent pixel electrodes to be driven with driving voltages of the same polarity at the respective times in

the inverse driving. If the pixel electrodes corresponding to (i) are arranged in the direction along the data lines and the pixel electrodes corresponding to (ii) are arranged in the direction along the scanning lines, the pixel electrodes arranged in the direction along any one scanning line are driven with one polarity and the pixel electrodes arranged in the direction along another scanning line adjacent to the any one scanning line are driven with an inverse polarity to the one polarity (~~so-called~~ "1H inverse driving").

However, in this case, between the pixel electrodes adjacent to each other along the data line, the horizontal electric field based on the driving voltages of inverse polarities is generated. Such horizontal electric field may interfere the electric field (may be referred to as vertical electric field in contrast to the horizontal electric field) generated between the pixel electrode and the opposing electrode, and as a result, it becomes difficult to obtain the orientation state of the liquid crystal molecules as desired, so that the image display may be affected.

Further, in the present aspect, in a case that such adverse effects may be caused, the convex portion formed on the base of the pixel electrode along the scanning line has a distinct significance.

That is, first, when the edge portions of the respective pixel electrodes are formed to be positioned on the step, the vertical electric field generated between the respective pixel electrodes and the opposing electrode is intensified compared to the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in the different pixel electrode group). That is, since the electric field generally intensifies as the distance between the electrodes becomes shorter, the edge portions of the pixel electrodes near the opposing electrode by the height of the step generates an intense vertical electric field. Second, whether the edge portions of the respective pixel electrodes are positioned on the step or not, the horizontal electric field

generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in a different pixel electrode group) is weakened by the presence of the step in accordance with the dielectric constant, and even by reducing (replacing partially from the step) the volume of the electro-optical material through which the horizontal electric field passes, the effect that the horizontal electric field has on the electro-optical material can be reduced. Therefore, the operation failure from the electro-optical material such as the bad orientation of the liquid crystal by the horizontal electric field caused by the inverse driving method, can be reduced. At this time, as described above, the edge portions of the pixel electrodes may be or not be positioned on the step and may be positioned on the inclined step or on almost vertical side surface thereof.

In addition, since the light-shielding film for concealing the operation failure caused by the electro-optical material, can be formed small, it is also possible to increase the opening ratios of the respective pixels without having the bad image display, caused by the light leakage, generated.

As described above, according to the present aspect, first, due to the presence of the buried portion, the effects associated with the above-described leveling can be obtained, and second, by forming intentionally the step including the convex portion along the scanning line by the presence of the non-buried portion, the generation of the horizontal electric field can be prevented.

In another aspect of the electro-optical device of the present invention, a capacitor electrode on a pixel potential side constituting a storage capacitor connected to the pixel electrode and a capacitive line having capacitor electrode on a fixed potential side arranged constituting the storage capacitor arranged opposing the capacitor electrode on the pixel potential side through a dielectric film, may be further comprised. The capacitive line has a main line portion extending along the scanning line and a portion extending

along the data line, and a width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line.

According to this aspect, since the storage capacitor, ~~having a construction~~ such that the capacitor electrode on the pixel potential side and the capacitor electrode on the fixed potential side are arranged opposite to each other, is connected to the pixel electrode, the voltage of the image signal written in the pixel electrode can be maintained for a long time. In particular, in the present aspect, since the width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line, it is possible to further lower the resistance of the capacitive line. Further, in the present aspect, since a low resistance of the capacitive line can be realized as described above, from the point of view of the whole device, the narrowness of the capacitive line and further narrowness of the storage capacitor can be accomplished, and as a result, it is possible to ~~improve~~ the opening ratio. In the "narrowness of the capacitive line", since the capacitive line itself has a width equal to or "broader than" the width of the data line on the surface, it may appear to be a contradiction, but the broad width and the narrow width should be determined from the relative relationship between the capacitive line and the data line, such that from the point of view of the whole device, the "narrowness of the capacitive line" can be accomplished, compared to the ~~conventional~~ art. Furthermore, in the broad width and narrow width described above or the "broader than" to be described in the present invention, the discrete values of the width can be adequately determined theoretically, experimentally, experientially or by means of simulation.

Further, according to the present aspect, it is possible to effectively prevent the light from entering the thin-film transistor, in particular the channel area thereof, compared to the ~~conventional~~ art, as well as obtaining the above-described low resistance. This is because, as described above, although in the conventional art, the light reflected

from the back of the data line and the like becomes a stray light and thus may enter the thin-film transistor, but according to the present aspect, the possibility that the advance of such stray light is shielded by the capacitive line formed in the width equal to or broader than that of the data line is increased.

From the above, according to the present invention, the problems such as the cross talk or burn-in that were prevalent in the conventional art can be reduced by means of the low resistance of the capacitive line. Further, since the light leak current in the thin-film transistor is reduced, it is possible to display a high quality image.

Further, in the present invention, since the portion extending along the data line exists in the capacitive line, the area of the storage capacitor can be increased. This markedly contributes to the image display having high quality.

Furthermore, in order to more effectively accomplish the light-shielding function described above, materials having a good light-shielding feature may be employed for the capacitive line. For example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one from Al (aluminum), Cu (copper), Ti (titan), Cr (chrome), W (tungsten), Ta (tantalum), and Mo (molybdenum) can be adequately employed. Further, in addition to the above, for example, light-absorbing materials such as poly-silicon can be employed.

In this aspect, a portion overlapping the thin-film transistor in the data line may be formed locally broad, and a width of the portion extending along the data line in the capacitive line may be broader than that of the portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

By such construction, the portion overlapping the thin-film transistor in the data line is formed locally broad. Then, the width of the portion formed broad is equal to that of the portion extending along the data line in the above-described capacitive line. That

is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Thus, the light entered from the upper portion of the thin-film transistor can be more securely prevented.

More specifically, for example, when the capacitive line is made up of metal having a high melting point, the capacitive line can independently have the light-shielding ability that the transmittance thereof is about 0.1% (2 or more in OD (Optical Density)). However, if the silicide forming process is performed on the capacitive line, the composition thereof is varied and thus the light-shielding ability may be reduced. In this case, only the light-shielding ability having the transmittance of 0.1% or more may be obtained.

However, in the present aspect, the data line overlapping the capacitive line composed of such a metal film having a high melting point is further comprised. If the construction for performing the light shielding of the thin-film transistor by means of overlapping the capacitive line and the data line is employed, the light-shielding ability corresponding to the added value of these transmittances can be obtained. For example, when the data line is made up of aluminum, etc., the light-shielding ability with a transmittance of 0.001% or less (4 or more in the OD value) can be accomplished.

Further, in the present aspect, in particular, that the broad width of the portion extending along the data line in the capacitive line is broad means that it is broader than that of the portion not formed broad in the data line.

Also, a portion overlapping the thin-film transistor in the data line is formed locally broad, and a width of the portion extending along the data line in the capacitive line is broader than that of the portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

According to this aspect, the portion overlapping the thin-film transistor in the

data line is formed locally broad. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Therefore, the light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.

Furthermore, in the present aspect, in particular, the width of the portion extending along the data line in the capacitive line is formed narrower than that of the data line. That is, in the portion, the width of the data line is narrower than that of the capacitive line. From this construction, for example, when the data line is made up of aluminum having a high light reflexibility, a stray light generated by reflecting the incident light by any element in the electro-optical device, a light returning to the electro-optical device after a light emitted from the electro-optical device is reflected by any element outside of the electro-optical device, or in a projection type display device such as a color-displayable liquid crystal projector comprising a plurality of electro-optical devices, a light emitted from other electro-optical device and generated by returning to the electro-optical device is reflected by the data line to thereby prevent the stray light from being increased. This is because the portion of the data line formed broad is relatively narrower than the capacitive line.

In this aspect that has the data line having a portion overlapping the thin-film transistor formed broad, the capacitive line is arranged at the overlapped position between the thin-film transistor and the data line, and the data line may be constructed such that the portion provided with a contact hole for connecting to the thin-film transistor is formed broad in addition to the portion overlapping the thin-film transistor.

From this construction, even when the capacitive line as the light-shielding film could is not provided, the decrease in the light-shielding ability can be compensated by forming broad the data line for the contact hole.

Alternatively, for each thin-film transistor, the data line is formed continuously broad from the portion overlapping the thin-film transistor to the portion in which the contact hole is provided.

From this construction, the light shielding of the thin-film transistor can be more securely accomplished.

Further, the portion formed broad in the portion overlapping the thin-film transistor and the portion formed broad in the portion in which the contact hole is provided may be separately formed broad. If arranging the portion overlapping the thin-film transistor and the portion in which the contact hole is provided close to each other and forming them continuously broad as in the present aspect, since the area to be formed broad need not be exceedingly broad, it is advantageous from the point of view of not increasing the inner reflection.

In another aspect of the electro-optical device of the present invention, another substrate opposing the substrate through an electro-optical material and a light shielding film formed on the another substrate may be further ~~comprised~~ provided, and the width of the data line and the width of a portion extending along the data line in the capacitive line are narrower than that of the light-shielding film.

From this aspect, if it is assumed that the light is entered from another substrate, the laminated structure of the light-shielding film, the data line and the capacitive line in the order from the light incidence side can be constructed. The width of the former is broader than those of the latter two. That is, the advance of the incident light is blocked by the broader light-shielding film, and only the light passing through it reaches the data line and the capacitive line. Further, when the light passing through the light-shielding film reaches the data line and the capacitive line, the data line and the capacitive line can be expected to perform the above-described light-shielding function. In short, according

to the present aspect, it is possible to improve the light resistance of the thin-film transistor and to reduce the generation of the light leakage.

Further, if the pixel electrodes are arranged in a matrix shape, the "light-shielding film" in the present aspect may be formed in a stripe shape or a lattice shape to extend through spaces between the pixel electrodes. Furthermore, according to circumstances, the light-shielding film may be formed as a laminated structure made of, for example, a light-absorbing material such as chrome or chrome oxide and a light-reflecting material such as aluminum.

An electronic apparatus of the present invention may comprise the above-described electro-optical device (including various aspects).

According to the electronic apparatus of the present invention, for example, since it comprises the electro-optical device capable of adequately adjusting the arrangement between the thin-film transistor and the scanning line, it is possible to realize various electronic apparatuses such as a liquid crystal projector, a liquid crystal television, a portable phone, an electronic pocket book, a word processor, a view finder type or monitor direct vision-type videotape recorder, a work station, a video phone, a POS terminal, and a touch panel, capable of precise operation of the thin-film transistor and high quality image display.

The above effects and other advantages of the present invention will be more apparent from the following embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating an equivalent circuit of various elements, wirings and the like provided in a plurality of pixels, having a matrix shape, constituting an image display area in an electro-optical device according to an embodiment of the

present invention;

FIG. 2 is a plan view of a group of adjacent ~~plural~~ pixels in a TFT array substrate where data lines, scanning lines, pixel electrodes are formed in the electro-optical device according to an embodiment of the present invention;

FIG. 3 is a sectional view taken along ~~a line~~ A-A' in FIG. 2;

FIG. 4 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 2;

FIG. 5 is a ~~diagram with the same purpose as FIG. 2 and~~ illustrates another embodiment in which the arrangement of the scanning lines and the TFTs is different from that in FIG. 2;

FIG. 6 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 5;

FIG. 7 is a sectional view taken along ~~a line~~ B-B' in FIG. 5;

FIG. 8 is a ~~diagram with the same purpose as FIG. 2 and~~ illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the scanning lines are buried in the grooves;

FIG. 9 is a sectional view illustrating a profile of a narrow width portion of the scanning lines shown in FIG. 8;

FIG. 10 is a ~~diagram with the same purpose as FIG. 2 and~~ illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and a part of the scanning lines are buried in the grooves;

FIG. 11 is a sectional view illustrating a profile of a narrow width portion of the scanning line shown in FIG. 10;

FIG. 12 is a sectional view taken along ~~a line~~ T-T' in FIG. 10;

FIG. 13 ~~is an explanatory diagram for~~ explaining the generation of a horizontal

electric field;

FIG. 14 is a ~~diagram with the same purpose as FIG. 2 and~~ illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the narrow width portion of the scanning line is deviated from the center of a first gap;

FIG. 15 is a sectional view taken along ~~a line~~ T-T' in FIG. 14;

FIG. 16 is a ~~diagram with the same purpose as FIG. 2 and~~ illustrates another embodiment that a shape of the data line is different from that in FIG. 2;

FIG. 17 is a sectional view taken along ~~a line~~ P-P' in FIG. 16;

FIG. 18 is a sectional view taken along ~~a line~~ Q-Q' in FIG. 16;

FIG. 19 is a sectional view taken along ~~a line~~ R-R' in FIG. 16;

FIG. 20 is a plan view when the TFT array substrate of the electro-optical device according to the embodiment of the present invention is ~~seen~~ from the opposing substrate side along with the respective elements formed thereon;

FIG. 21 is a sectional view taken along ~~a line~~ H-H' in FIG. 20;

FIG. 22 is a schematic sectional view illustrating a color liquid crystal projector that is an example of a projection type color display apparatus as an embodiment of an electronic apparatus of the present invention.

~~[reference numerals]~~

1a	SEMICONDUCTOR LAYER
1a'	CHANNEL AREA
330a, 330a', 340a, 350a, 360a	SCANNING LINE
331a, 331a', 341a, 351a, 361a	BROAD WIDTH PORTION
~~332a, 332a', 342a, 352a, 362a~~	~~NARROW WIDTH PORTION~~

~~P007516~~

~~3G1, 3G1', 3G2~~	~~GROOVE~~
352aB	BURIED PORTION
352aNB	NON-BURIED PORTION
430	STEP
9a	PIXEL ELECTRODE
10	TFT ARRAY SUBSTRATE
16	ORIENTED FILM
30	TFT
~~50~~	~~LIQUID CRYSTAL LAYER~~

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

~~Now,~~ preferred embodiments of the present invention ~~will be~~ are explained with reference to the drawings. In following embodiments, an electro-optical device of the present invention is applied to a liquid crystal device.

First, a construction of a pixel part in the electro-optical device according to an embodiment of the present invention ~~will be~~ is explained with reference to FIGs. 1 to 4. Fig. 1 shows an equivalent circuit of various elements, wirings and the like in a plurality of ~~pixels formed in a matrix~~ shape constituting an image display area 10a of the electro-optical device. FIG. 2 is a plan view of a group of a plurality of pixels adjacent to each other on a TFT array substrate in which data lines, scanning lines, pixel electrodes and the like are formed. Further, FIG. 3 is a sectional view taken along ~~a line~~ A-A' in FIG. 2. Further, in FIG. 3, in order for each layer and each member to have recognizable sizes ~~on~~ in the drawing, different scales are applied to each layer and each member. Furthermore, FIG. 4 is a plan view illustrating shapes of only the scanning lines extracted from FIG. 2.

In FIG. 1, in the plurality of pixels formed in a matrix shape constituting the

image display area of the electro-optical device according to the present embodiment, a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed, respectively, and data lines 6a supplied with image signals are electrically connected to sources of the TFTs 30. Image signals S1, S2, ..., Sn to be, in this order, written may be sequentially supplied to the data lines 6a, or may be supplied to each group which has a plurality of data lines 6a adjacent to each other.

Further, scanning lines 330a are electrically connected to gates of the TFTs 30 and at a predetermined timing, scanning signals G1, G2, ..., Gn are pulse-like applied to the scanning lines 330a in that order. The pixel electrodes 9a are electrically connected to drains of the TFTs 30, and by closing switches of the TFTs 30, that is, switching elements for a predetermined time interval, the image signals S1, S2, ..., Sn supplied from the data lines 6a are written at a predetermined timing.

A predetermined level of the image signals S1, S2, ..., Sn which have been written through the pixel electrodes 9a to a liquid crystal that is an example of an electro-optical material are maintained for a predetermined time interval between the pixel electrode 9a and an opposing electrode formed on an opposing substrate. The liquid crystal modulates light by varying orientation or order of molecules according to the applied voltage level and thus it is possible to execute the gradation display. If it is in a normally-white mode, transmittance for the incident light is decreased in accordance with the voltage applied in a unit of pixel and if it is in a normally-black mode, the transmittance for the incident light is increased in accordance with the voltage applied in a unit of pixel. Therefore, as a whole, light having a contrast responsive to the image signals is emitted from the electro-optical device.

In order to prevent the maintained image signals from being leaked, a storage capacitor 70 is added in parallel to a liquid crystal capacitor formed between the pixel

electrode 9a and the opposing electrode.

Now, a more specific construction of the electro-optical device in which the above-described circuit operation is executed by using the data lines 6a, the scanning lines 330a, the TFTs 30 and the like will be explained with reference to FIGs. 2 and 3.

First, the electro-optical device according to the present embodiment, as shown in FIG. 3 which is a sectional view taken along a line A-A' in FIG. 2, comprises a TFT array substrate 10 and a transparent opposing substrate 20 arranged opposite thereto. The TFT array substrate 10 is made of, for example, a quartz substrate, a glass substrate or a silicon substrate, and the opposing substrate 20 is made of, for example, a glass substrate or a quartz substrate.

As shown in FIG. 3, the TFT array substrate 10 is provided with a pixel electrode 9a, and an upper portion of the pixel electrode is provided with an oriented film 16 which has been subjected to a predetermined orientation process such as a rubbing process. The pixel electrode 9a is made of, for example, a transparent conductive film such as an ITO (Indium Tin Oxide) film.

The opposing substrate 20 is provided over the whole surface thereof with an opposing electrode 21, and a lower portion of the electrode is provided with an oriented film 22 which has been subjected to a predetermined orientation process such as a rubbing process. The opposing electrode 21 is made of, for example, a transparent film such as an ITO film.

Next, in FIG. 2, a plurality of pixel electrodes 9a (profiles thereof are indicated by dotted lines 9a') are provided in a matrix shape on the TFT array substrate 10 of the electro-optical device, and data lines 6a of aluminum films and scanning lines 330a of poly-silicon films are provided along horizontal and vertical boundaries of the pixel electrodes 9a.

Each scanning line 330a is arranged opposite to a channel area 1a' indicated by oblique lines area extending from lower left to upper right in the semiconductor layer 1a of a poly-silicon film and functions as a gate electrode. That is, in portions where the scanning lines 330a and the data lines 6a are intersected, TFTs 30 for switching pixels where broad width portions 331a (to be explained later) of the scanning lines 330a are arranged opposite to the channel areas 1a' as gate electrodes are provided. In other words, TFTs 30 in the present embodiment, in particular, the channel areas 1a' thereof are formed in intersecting areas of the plurality of pixel electrodes 9a arranged in a matrix shape. The intersecting area means an area where, in plan view, a first long gap (X direction in FIG. 2) extending through a space between adjacent pixel electrodes 9a sandwiching the scanning lines therebetween and a second long gap (Y direction in FIG. 2) extending through a space between adjacent pixel electrodes sandwiching the data line 6a therebetween, are intersected.

More specifically, with reference to FIG. 2, the intersecting area corresponds to, for example, a position farthest from each of a lower-right corner of the pixel electrode 9a shown on the upper-left side of the plan view, a lower-left corner of the pixel electrode 9a shown on the upper-right side, an upper-right corner of the pixel electrode 9a shown on the lower-left side and an upper-left corner of the pixel electrode 9a shown on the lower-right side of the plan view. Since the TFT 30 is formed at such position, it is difficult for an incident light to directly enter the channel area 1a' of the TFT.

The TFT 30, as shown in FIG. 3, has an LDD (Lightly Doped Drain) structure, and ~~comprises~~ includes a channel area 1a' of the semiconductor layer 1a where a channel is formed by an electric field from the scanning line which functions as a gate electrode as described above, an insulating film 2 having a gate insulating film for insulating the scanning line 330a from the semiconductor layer 1a, a low-concentration source area 1b, a low-

concentration drain area 1c, a high-concentration source area 1d and a high-concentration drain area 1e.

Further, although it is preferable that the TFT 30 has the LDD structure as shown in FIG. 3, the TFT 30 may have an offset structure in which impurities are prevented from being infiltrated into the low-concentration source area 1b and the low-concentration drain area 1c, or may be a self-alignment type TFT for infiltrating impurities at high concentration using the gate electrode constituting a part of the scanning line 330a as a mask to automatically form the high-concentration source area and the high-concentration drain area. Furthermore, although, in the present embodiment, the TFT 30 has a single gate structure where only one gate electrode of the TFT 30 for pixel switching is disposed between the high-concentration source area 1d and the high-concentration drain area 1e, the TFT may have a dual, triple or more gate structure where two or more gates are disposed therebetween. Furthermore, the semiconductor layer 1a constituting the TFT 30 is not limited to the poly-silicon film, but may be made of an amorphous silicon film or a monocrystalline silicon film. A known method such as a pasting method can be employed in formation of the monocrystalline silicon film. By employing the monocrystalline silicon film for the semiconductor layer 1a, it is possible to promote a high performance of the peripheral circuits.

In the present embodiment, for the scanning line 330a serving as the gate electrode of the TFT 30, a portion serving as the gate electrode, that is, a portion facing the channel area 1a' of the TFT 30 is formed broader than the other portion, as shown in FIG. 2. That is, in FIG. 2, the scanning line 330a has a broad width portion 331a extending in the Y direction in FIG. 2 to correspond to the channel area 1a' extending in the Y direction in FIG. 2 and a narrow width portion 332a extending through a space between the adjacent pixel electrodes 9a. In FIG. 4, for the purpose of simplifying the illustration, only the

shape pattern of the scanning line 330a is shown.

In this connection, in the present embodiment, the broad width portion 331a is lengthened from the narrow width portion 332a. That is, the broad width portion 331a and the narrow width portion 332a are integrally formed. Such shape can be easily formed, for example, by using a known photolithography and etching, on the assumption that a pattern having an integrated shape 332a (see FIG. 4) composed of the broad width portion 331a and the narrow width portion 332a is formed. However, the present invention is not limited to such shape, and includes, for example, even shapes where the broad width portion 331a is formed by connecting other conductive member prepared separately to the narrow width portion 332a, within the scope thereof.

The storage capacitor 70 shown in FIG. 1 is constructed such that a junction layer 71 as the capacitor electrode on the pixel potential side connected to the high-concentration drain area 1e of the TFT 30 and the pixel electrode 9a and a part of the capacitive line 300 as the capacitor electrode on the fixed potential side are arranged opposite to each other via an dielectric film 75, as shown in FIG. 3. By means of the storage capacitor 70, it is possible to markedly improve the potential maintenance characteristics in the pixel electrode 9a.

The junction layer 71 is made up of, for example, the conductive poly-silicon film and serves as a capacitor electrode on the pixel potential side. However, similar to the capacitive line 300 to be explained in detail later, the junction layer 71 may be made of a single layer film or multi-layer film containing metal or alloy. In addition to the function as a capacitor electrode on the pixel potential side, the junction layer 71 also has a function for connecting the pixel electrode 9a and the high-concentration drain area 1e of the TFT 30 to each other through contact holes 83 and 85.

By using such junction layer 71, even if the distance between layers is as long as,

for example, 2000nm, both layers can be connected well to each other through serial contact holes having two relatively small diameters while avoiding the technical difficulty of connecting both layers to each other through one contact hole, so that an opening ratio of pixel can be increased. Further, in opening the contact hole, it is helpful to prevent punchthrough in etching.

The capacitive line 300 is made of, for example, a conductive film containing metal or alloy, and serves as a capacitor electrode on the fixed potential side. The capacitive line 300 is formed overlapping an area for forming the scanning line 330a from a plan view, as shown in FIG. 2. More specifically, the capacitive line 300 has a main line portion extending along the scanning line 330a, a protruding portion protruded upwardly in the Y direction along the data line 6a from a portion intersecting the data line 6a and a constricted portion where the portion corresponding to the contact hole 85 is slightly constricted. The protruding portion contributes to increase in the area for forming the storage capacitor 70 by using the area on the scanning line 330a and the area below the data line 6a.

Further, the capacitive line 300 is made of, for example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one of metals having high melting point such as Ti, Cr, W, Ta, Mo, and in addition to the function as a capacitor electrode on the fixed potential side of the storage capacitor 70, the capacitive line 300 has a function as a light-shielding layer for shielding the TFT 30 from the incident light on the upper side of the TFT 30. However, the capacitive line 300 may have a multi-layer structure in which a first film made of a conductive poly-silicon film and the like and a second film made of a metal silicide film containing metal and the like having high melting point are stacked.

Furthermore, preferably, the capacitive line 300 extends from the image display

area in which the pixel electrodes 9a are arranged to peripheries thereof, and is electrically connected to a potentiostatic source to be a fixed potential. Such potentiostatic source may be a potentiostatic source such as a plus power source or a minus power source supplied to a data line driving circuit to be explained later, or may be a potentiostatic source supplied to the opposing electrode 21 of the opposing substrate 20.

A dielectric film 75, as shown in FIG. 3, is constructed of a silicon oxide film such as a HTO (High Temperature Oxide) film or ~~a LTO~~ (Low Temperature Oxide) film having, for example, a relatively thin thickness of about 5~200nm, or a silicon nitride film. From the point of view of increasing the capacitance of the storage capacitor 70, the dielectric film 75 should be preferably as thin as possible as long as the reliability of the film is sufficiently maintained.

In FIGs. 2 and 3, in addition, the lower side of the TFT 30 is provided with a lower light-shielding film 11a. The lower light-shielding film 11a is patterned in a lattice shape, and as a result, the opening area of each pixel is defined. Further, the opening area may be defined by the intersection of the data line 6a extending in the Y direction in FIG. 2 and the capacitive line 300 extending in the X direction in FIG. 2. Furthermore, similar to the case of the above-described capacitive line 300, the lower light-shielding film 11a may be formed extending from the image display area to the peripheries thereof to be connected to a potentiostatic source so that the potential variation has no adverse effects on the TFT 30.

Further, a base insulating film 12 is provided below the TFT 30. In addition to the function for insulating the TFT 30 from the lower light-shielding film 11a, since the base insulating film 12 is formed on the whole surface of the TFT array substrate 10, the base insulating film 12 has a function for preventing the characteristic variation of the TFT 30 for pixel switching caused by rough polished surface of the TFT array substrate 10 or

contaminants left after washing.

In addition, a first interlayer insulating film 41 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 83 communicating with the high-concentrating drain area 1e, respectively, is formed on the scanning line 330a.

The junction layer 71 and the capacitive line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 85 communicating with the junction layer 71 are formed respectively on the junction layer 71 and the capacitive line 300.

Furthermore, in the present embodiment, by baking the first interlayer insulating film 41 at about 1000°C, activation of ions injected into the poly-silicon film constituting the semiconductor layer 1a or the scanning line 330a may be intended. On the other hand, by not baking the second interlayer insulating film 42, relief of stress occurring in the vicinity of the interface of the capacitive line 300 may be intended.

The data line 6a is formed on the second interlayer insulating film 42, and above them a third interlayer insulating film 43 which has a contact hole 85 communicating the junction layer 71 is formed.

The surface of the third interlayer insulating film 43 is leveled by means of CMP (Chemical Mechanical Polishing) process, and as a result, the orientation failure of the liquid crystal layer 50 caused by a step generated by various wirings or elements below the third interlayer insulating layer 73 can be reduced.

However, in place of performing the leveling process for the third interlayer insulating film 43, or in addition to it, a groove, in at least one of the TFT array substrate 10, the base insulating film 12, the first interlayer insulating film 41, or the second

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND OF THE INVENTION

1. Field of Invention

[0001] The present invention relates to an electro-optical device capable of performing active matrix drive. The invention also relates to an electronic apparatus incorporating such an electro-optical device.

2. Description of Related Art

[0002] The related art includes an electro-optical device including a pair of substrates constructed to sandwich an electro-optical material, such as a liquid crystal, therebetween and electrodes provided in each of the pair of substrates to apply an electric field to the electro-optical material. The electrodes are used to apply an electric field to the electro-optical material to vary the state of the material. According to such an electro-optical device, for example, when the light emitted from a light source enters the device and the state of the electro-optical material is varied, it is possible to control the light transmittance and thus realize desired image display.

[0003] Moreover, in related art electro-optical devices, by providing pixel electrodes arranged in a matrix shape, thin-film transistors (hereinafter "TFT") connected to the respective pixel electrodes, and scanning lines and data lines connected to each of TFTs and provided in parallel to a row direction and a column direction, respectively, on one of the pair of substrates, active matrix drive can be performed. As a result, for each pixel defined by the pixel electrodes or the scanning lines and the data lines, it is possible to control the electric field applied to the electro-optical material and to control the light transmittance.

SUMMARY OF THE INVENTION

[0004] However, in the related art electro-optical devices, there are the following problems. That is, for an electro-optical device capable of performing the above active matrix drive, it is required to precisely drive the TFTs. However, precisely driving the TFTs is a difficult task while satisfying the high precision and miniaturization requirements imposed in related art electro-optical devices.

[0005] A TFT includes a semiconductor layer having a channel area, a source area and a drain area, and a gate electrode formed through an insulating film to cover at least a part of the channel area of the semiconductor layer. By applying or not applying the electric

field to the channel area in accordance with the current applied (or not applied) to the gate electrode, the current flow can be controlled.

[0006] At this time, the length of the channel area, referred to as "channel length" or a width thereof, referred to as "channel width", that is, the size of the channel area is, is important to determine the characteristics of TFTs. Further, an arrangement of the gate electrode on the channel area is also a very important factor. In this regard, in the related art, a conductive member electrically connected to the scanning line or a member constituting a part of the scanning line, can be used as the gate electrode. However, there are problems in arranging the scanning line itself and the channel area.

[0007] In short, it is beneficial or required to realize a suitable arrangement of the channel area (or TFT) and the scanning line (or gate electrode) while realizing the high precision required in the electro-optical devices. Further, it is beneficial or required to realize the difficult task of precisely operating the TFT constructed as such.

[0008] For example, it is not sufficient to only drive the electro-optical device by the TFT, and the scanning line (or the gate electrode) and various elements are additionally required. However, it is generally difficult to accomplish the above arrangement or adjustment in connection with various other elements. Further, in the TFT, there is a disadvantage if it is required to prevent the light leakage current which is generated by the light entering the channel area. That is, it is preferable that the TFT is arranged as far as possible from a light-transmitting area, which is an area that the light contributes to image display in each pixel emitted through transmission or reflection, more specifically, from the pixel electrode. However, since this should be realized while satisfying the requirement of high precision, there is a further disadvantage in that the above arrangement/adjustment becomes an even more difficult task.

[0009] The present invention address the above and/or other problems, and provides an electro-optical device capable of easily adjusting the arrangement of a gate electrode and a scanning line and capable of precisely driving TFT and an electronic apparatus including the electro-optical device.

[0010] In order to address or solve the above problems, the electro-optical device of the present invention includes, on a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction intersecting the scanning lines, thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes formed correspondingly to the thin-film transistors. The respective

scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

[0011] According to the electro-optical device of the present invention, by supplying scan signals and image signals to the thin-film transistors through the scanning lines and the data lines, the pixel electrodes can be driven in an active matrix mode.

[0012] More specifically, in the present invention, since the scanning lines have the broad width portions as the gate electrode in a portion facing the channel area of the thin-film transistor and the narrow width portion in other portion, it is not only possible to realize the narrowness of the scanning line but also to more easily adjust/determine the arrangement between the channel area (or the thin-film transistor) and the scanning line than in the related art.

[0013] For example, when a plurality of pixel electrodes are arranged in a matrix shape, it is generally preferable that the thin-film transistor are configured such that the channel area of the thin-film transistor is positioned at the position farthest from the corner of each pixel electrode, that is, at the center position of a space among adjacent and opposite corners of the pixel electrodes when four pixel electrodes are considered (because it is farthest from the light transmitting area). However, in this case, by allowing the channel area to extend through a space between adjacent pixel electrodes including the center position, it is possible to adequately determine the channel length, and by arranging the scanning line to intersect it, it is possible to realize a structure that the broad width portion of the scanning line exists on the channel area. Therefore, in this case, it is possible to simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices. Further, in this case, the light incidence to the thin-film transistor or the channel area can be prevented as much as possible or reduced under the above-described assumption.

[0014] Like the above, according to the present invention, it is possible to adequately adjust the arrangement between the thin-film transistor and the scanning line or the gate electrode while satisfying the high precision requirements of the electro-optical devices. Further, this structure renders a good outcome even after arrangement of various elements constituting the electro-optical device has been adjusted and determined, in addition to the above scanning line and the thin-film transistor. Furthermore, according to the present invention, it is possible to precisely drive the thin-film transistor, and thus maintain the quality of image to be displayed at high level.

[0015] Further, in the present invention, "broad width" means that it is broader than the width of the "narrow width portion," and "narrow width" means that it is narrower than the width of the "broad width portion". In short, the broad and narrow degree of "the broad width portion" and the "narrow width portion" is determined in accordance with the relative relationship between them. Furthermore, the real width of the broad width portion or the narrow width portion can be adequately determined theoretically, experimentally or by simulation.

[0016] In one aspect of the electro-optical device of the present invention, the broad width portion has a portion lengthened from the narrow width portion.

[0017] According to this aspect, it is possible to form the scanning line relatively easily having the broad width portion and the narrow width portion. More specifically, for example, by employing known, related art or later developed photolithography and etching methods with the assumption that the broad width portion and the narrow width portion are formed through the incorporated pattern, the scanning line according to the present aspect can be easily formed.

[0018] In another aspect of the electro-optical device of the present invention, the broad width portion has a portion connected to the narrow width portion.

[0019] According to this aspect, for example, the broad width portion includes the portion formed by connecting a conductive member and the like prepared separately to the narrow width portion. Even in this case, the broad width portion can be formed relatively easily.

[0020] In another aspect of the electro-optical device of the present invention, the scanning line extends in a direction intersecting the direction in which the channel area extends and the broad width portion extends in a single direction or bi-directionally in which the channel area extends.

[0021] According to this aspect, since the broad width portion extends in the single direction or bi-directionally in which the channel area extends, it is possible to more adequately adjust the arrangement of the thin-film transistor and the scanning line. Further, according to this aspect, since the gate electrode is adequately formed in accordance with the channel length, the electric field can be more effectively applied to the channel area.

[0022] Further, like the above, according to the aspect that the gate electrode, that is, the broad width portion is provided in the portion to be the channel area corresponding to the channel area, for example, the so-called self-aligned formation of the thin-film transistor (that is, formation of the source area and the drain area adjacent to the channel area through

an ion implantation process using the gate electrode as a mask) can be easily executed. However, in this case, strictly speaking, the channel area is formed by carrying out the ion implantation process after forming the broad width portion to be the gate electrode.

[0023] In another aspect of the electro-optical device of the present invention, the pixel electrodes are arranged in a matrix shape and the channel areas are formed in an intersecting area in which a first long gap extending through a space between pixel electrodes sandwiching of the scanning line and being adjacent to each other and a second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected.

[0024] This aspect is similar to the above mentioned aspect and is one of the aspects in which the operational effect of the present invention is exhibited most effectively.

[0025] That is, according to this aspect, the channel area of the thin-film transistor is formed in the intersecting area of the pixel electrodes arranged in a matrix shape. The intersecting area is an area in which the first long gap extending through a space between pixel electrodes sandwiching the scanning line and being adjacent to each other and the second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected in plan view. By such a configuration, it is difficult for light to enter the channel area.

[0026] Further, along with such an operational effect, since the scanning line has the broad width portion as the gate electrode is opposite to the channel area, the arrangement between the channel area (or the thin-film transistor) and the gate electrode (or the scanning line) can be determined most adequately and it is also possible to secure the adequate channel length and narrowness of the scanning line.

[0027] In this aspect, in particular, the narrow width portion is formed at a position deviated from a center of the first gap and the broad width portion, is formed at the center of the first gap in the intersecting area.

[0028] According to this configuration, the narrow width portion of the scanning line extends through the space between the adjacent pixel electrodes but does not exist at the center thereof and is formed at the position deviated from the center thereof. As a result, first, the enhancement in the quality of the displayed image can be obtained, especially for the liquid crystal display device that is an example of the electro-optical device, and the reason thereof is as follows.

[0029] That is, in the present aspect, when performing the rubbing process on a convex portion on the oriented film normally provided in the liquid crystal display device, in

particular, a convex portion formed by "height" of the narrow width portion, nonuniformities are usually generated in the convex portion. Further, it is considered that the degree of nonuniformity is different from each other in the portion associated with the rubbing up convex portion (that is, the direction ascending to the convex portion) and the portion associated with the rubbing down convex portion (that is, the direction descending from the convex portion).

[0030] More specifically, for example, it is more difficult to generate nonuniformity in the portion associated with the rubbing up convex portion than in the portion associated with the rubbing down convex portion.

[0031] Further, if the nonuniformity is left as it is, a poor orientation of the liquid crystal may be caused to result in the operation failure of the electro-optical devices. In the difference in the degree of nonuniformity between the rubbing-up process and the rubbing-down process, the latter has greater possibility to cause the bad orientation of the liquid crystal than the former.

[0032] It is significant that the narrow width portion of the present aspect is formed at a position deviated from the center of the first gap between the pixel electrodes. That is, if the narrow width portion is formed at the above-described position, the vertex of the convex portion caused by the narrow width portion is also formed at the position deviated from the center of the first gap, and this means that it is possible to form almost only half inclined surface of the convex portion on the area corresponding to the first gap, that is, to form only the portion associated with the rubbing-down on the area. Further, in this case, if the light-shielding film is provided corresponding to the first gap, it is possible to effectively shield only the portion associated with the rubbing-down, that is, to effectively shield the corresponding portion of the convex portion to be most influenced by the nonuniformity.

[0033] As a result, according to the present aspect, since the operation failure of the electro-optical device caused by nonuniformities can be substantially prevented or reduced, and the portion of the convex portion associated with the rubbing-up, which is not affected by nonuniformities, is able to transmit the light contributing to the image display. Thus, it is possible to enhance the opening ratio of pixel, that is, to provide a brightened image display. As a result, according to the present aspect, from the above-mentioned point of view, the enhancement in the display image can be obtained.

[0034] Further, by forming the narrow width portion at the position deviated from the center of the first gap, it is also possible to enhance the degree of freedom in designing

the electro-optical devices and to more effectively prevent or reduce light from entering the thin-film transistor. The reason thereof is as follows.

[0035] That is, in the present aspect, the narrow width portion extends through the first gap between the adjacent pixel electrodes, but does not exist at the center thereof. For this reason, by using the area in the first gap where the narrow width portion is not provided, in a plan view, it is possible to provide other wires, such as the capacitive line made up of the same film as the narrow width portion, in parallel to the narrow width portion. That is, the degree of freedom of design is increased.

[0036] Further, in the above-mentioned case, although the narrow width portion is deviated from the center thereof, it is possible to arrange the broad width portion as the gate electrode at the center of the gap, by adjusting the width of the broad width portion, for example, by broadening only one side or by broadening one side more than the other small side. Like the above, since the gate electrode can be arranged at a position advantageous to increase the light-shielding ability regardless of the position of the scanning line, or since the scanning line can be arranged at an arbitrary portion in the gap while arranging the gate electrode at the position advantageous for increasing the light-shielding ability, it is possible to realize a thin-film transistor having a high light-shielding ability while increasing the degree of freedom in arranging wires including the arrangement of the scanning lines.

[0037] In this configuration, further, the broad width portion may be formed at the center of the second gap in the intersecting area.

[0038] According to such construction, the channel area is formed at the position farthest from the adjacent or opposite corners of the electrodes in accordance with the above-described method, when four pixel electrodes are considered to be used. That is, it becomes very difficult for light to enter the channel area.

[0039] In another aspect of the electro-optical device of the present invention, grooves are formed in the substrate along the scanning lines, and the scanning lines are buried at least partially in the grooves directly or through an interlayer insulating film.

[0040] According to this aspect, since the scanning line is buried in the groove formed in the substrate, the generation of a step on the surface of the interlayer insulating film formed as the upper layer or on the surface of the pixel electrodes and the oriented film, etc. caused by the height of the scanning line itself can be prevented or reduced earlier. That is, the surface can be leveled very well. Then, if the surface of the oriented film is leveled, the rubbing process can be adequately performed for the orientation process and the orientated state of the liquid crystal molecules contacting the oriented film can be maintained

well. Therefore, according to the present aspect, since the possibility of bad orientation can be decreased and the light leakage caused by the bad orientation can be markedly prevented or reduced, it is possible to display a high-quality image.

[0041] In another aspect of the electro-optical device of the present invention, the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion not buried in the groove and extending along the scanning line in parallel to a buried portion, and a base of the pixel electrode is positioned high along the scanning line due to the presence of the non-buried portion.

[0042] According to this aspect, the narrow width portion has both the buried portion and the non-buried portion. Then, both of the buried portion and the non-buried portion extend along the scanning line and the base of the pixel electrode protrudes above along the scanning line due to the presence of the non-buried portion.

[0043] Through this construction, first, the effect associated with the above-described leveling can be similarly obtained by the buried portion. That is, the surface of the interlayer insulating film to be formed as the upper layer of the buried portion, or the surfaces of the pixel electrodes and the oriented film have the an excellent leveled feature, and thus it is possible to reduce the possibility of having the bad orientations.

[0044] Next, since the step including the convex portion along the scanning line is formed on the surface of the oriented film to be formed as the upper layer of the non-buried portion and the like, the above-described effects of leveling cannot be obtained by the non-buried portion. However, the following advantages can be obtained.

[0045] First, in electro-optical device according to the present invention, for the purpose of preventing or reducing deterioration of the liquid crystal, increasing the device life and reducing the cross-talk or flicker of the displayed image, a method of dividing the pixel electrodes into two groups and then inversely driving them in separate cycles may be employed. That is, a plurality of pixel electrodes including a first pixel electrode group to be inversely driven at a first period and a second pixel electrode group to be inversely driven at a second period compensatory with the first period, are arranged in a plain on the substrate. There are (i) the adjacent pixel electrodes to be driven with driving voltages of inverse polarities at the respective times in the inverse-driving, and (ii) the adjacent pixel electrodes to be driven with driving voltages of the same polarity at the respective times in the inverse driving. If the pixel electrodes corresponding to (i) are arranged in the direction along the data lines and the pixel electrodes corresponding to (ii) are arranged in the direction along the scanning lines, the pixel electrodes arranged in the direction along any one scanning line are

driven with one polarity and the pixel electrodes arranged in the direction along another scanning line adjacent to the any one scanning line are driven with an inverse polarity to the one polarity (referred to as "1H inverse driving").

[0046] However, in this case, between the pixel electrodes adjacent to each other along the data line, the horizontal electric field based on the driving voltages of inverse polarities is generated. Such horizontal electric field may interfere the electric field (may be referred to as vertical electric field in contrast to the horizontal electric field) generated between the pixel electrode and the opposing electrode, and as a result, it becomes difficult to obtain the orientation state of the liquid crystal molecules as desired, so that the image display may be affected.

[0047] Further, in the present aspect, in a case that such adverse effects may be caused, the convex portion formed on the base of the pixel electrode along the scanning line has a distinct significance.

[0048] That is, first, when the edge portions of the respective pixel electrodes are formed to be positioned on the step, the vertical electric field generated between the respective pixel electrodes and the opposing electrode is intensified compared to the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in the different pixel electrode group). That is, since the electric field generally intensifies as the distance between the electrodes becomes shorter, the edge portions of the pixel electrodes near the opposing electrode by the height of the step generates an intense vertical electric field. Second, whether the edge portions of the respective pixel electrodes are positioned on the step or not, the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in a different pixel electrode group) is weakened by the presence of the step in accordance with the dielectric constant, and even by reducing (replacing partially from the step) the volume of the electro-optical material through which the horizontal electric field passes, the effect that the horizontal electric field has on the electro-optical material can be reduced. Therefore, the operation failure from the electro-optical material, such as the bad orientation of the liquid crystal by the horizontal electric field caused by the inverse driving method, can be reduced. At this time, as described above, the edge portions of the pixel electrodes may be or not be positioned on the step and may be positioned on the inclined step or on an almost vertical side surface thereof.

[0049] In addition, since the light-shielding film to conceal the operation failure caused by the electro-optical material, can be formed small, it is also possible to increase the

opening ratios of the respective pixels without having the bad image display, caused by the light leakage, generated.

[0050] As described above, according to the present aspect, first, due to the presence of the buried portion, the effects associated with the above-described leveling can be obtained, and second, by forming intentionally the step including the convex portion along the scanning line by the presence of the non-buried portion, the generation of the horizontal electric field can be prevented or reduced.

[0051] In another aspect of the electro-optical device of the present invention, a capacitor electrode on a pixel potential side constituting a storage capacitor connected to the pixel electrode and a capacitive line having capacitor electrode on a fixed potential side arranged constituting the storage capacitor arranged opposing the capacitor electrode on the pixel potential side through a dielectric film, may be further provided. The capacitive line has a main line portion extending along the scanning line and a portion extending along the data line, and a width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line.

[0052] According to this aspect, since the storage capacitor, having a construction such that the capacitor electrode on the pixel potential side and the capacitor electrode on the fixed potential side are arranged opposite to each other, is connected to the pixel electrode, the voltage of the image signal written in the pixel electrode can be maintained for a long time. In particular, in the present aspect, since the width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line, it is possible to further lower the resistance of the capacitive line. Further, in the present aspect, since a low resistance of the capacitive line can be realized as described above, from the point of view of the whole device, the narrowness of the capacitive line and further narrowness of the storage capacitor can be accomplished, and as a result, it is possible to enhance the opening ratio. In the "narrowness of the capacitive line", since the capacitive line itself has a width equal to or "broader than" the width of the data line on the surface, it may appear to be a contradiction, but the broad width and the narrow width should be determined from the relative relationship between the capacitive line and the data line, such that from the point of view of the whole device, the "narrowness of the capacitive line" can be accomplished, compared to the related art. Furthermore, in the broad width and narrow width described above or the "broader than" to be described in the present invention, the discrete values of the width can be adequately determined theoretically, experimentally, experientially or by simulation.

[0053] Further, according to the present aspect, it is possible to effectively prevent or reduce the light from entering the thin-film transistor, in particular the channel area thereof, compared to the related art, as well as obtaining the above-described low resistance. This is because, as described above, although in the conventional art, the light reflected from the back of the data line and the like becomes a stray light and thus may enter the thin-film transistor, but according to the present aspect, the possibility that the advance of such stray light is shielded by the capacitive line formed in the width equal to or broader than that of the data line is increased.

[0054] From the above, according to the present invention, the problems, such as the cross-talk or burn-in that were prevalent in the related art, can be reduced by the low resistance of the capacitive line. Further, since the light leak current in the thin-film transistor is reduced, it is possible to display a high quality image.

[0055] Further, in the present invention, since the portion extending along the data line exists in the capacitive line, the area of the storage capacitor can be increased. This markedly contributes to the image display having high quality.

[0056] Furthermore, in order to more effectively accomplish the light-shielding function described above, materials having a good light-shielding feature may be employed for the capacitive line. For example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one from Al (aluminum), Cu (copper), Ti (titan), Cr (chrome), W (tungsten), Ta (tantalum), and Mo (molybdenum) can be adequately employed. Further, in addition to the above, for example, light-absorbing materials such as poly-silicon can be employed.

[0057] In this aspect, a portion overlapping the thin-film transistor in the data line may be formed locally broad, and a width of the portion extending along the data line in the capacitive line may be broader than that of the portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

[0058] By such a construction, the portion overlapping the thin-film transistor in the data line is formed locally broad. Then, the width of the portion formed broad is equal to that of the portion extending along the data line in the above-described capacitive line. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Thus, the light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.

[0059] More specifically, for example, when the capacitive line is made up of metal having a high melting point, the capacitive line can independently have the light-shielding

ability that the transmittance thereof is about 0.1% (2 or more in OD (Optical Density)). However, if the silicide forming process is performed on the capacitive line, the composition thereof is varied and thus the light-shielding ability may be reduced. In this case, only the light-shielding ability having the transmittance of 0.1% or more may be obtained.

[0060] However, in the present aspect, the data line overlapping the capacitive line formed of such a metal film having a high melting point is further provided. If the construction for performing the light shielding of the thin-film transistor by overlapping the capacitive line and the data line is employed, the light-shielding ability corresponding to the added value of these transmittances can be obtained. For example, when the data line is made up of aluminum, etc., the light-shielding ability with a transmittance of 0.001% or less (4 or more in the OD value) can be accomplished.

[0061] Further, in the present aspect, in particular, that the broad width of the portion extending along the data line in the capacitive line is broad means that it is broader than that of the portion not formed broad in the data line.

[0062] Also, a portion overlapping the thin-film transistor in the data line is formed locally broad, and a width of the portion extending along the data line in the capacitive line is broader than that of the portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

[0063] According to this aspect, the portion overlapping the thin-film transistor in the data line is formed locally broad. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Therefore, the light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.

[0064] Furthermore, in the present aspect, in particular, the width of the portion extending along the data line in the capacitive line is formed narrower than that of the data line. That is, in the portion, the width of the data line is narrower than that of the capacitive line. From this construction, for example, when the data line is made up of aluminum having a high light reflexibility, a stray light generated by reflecting the incident light by any element in the electro-optical device, a light returning to the electro-optical device after a light emitted from the electro-optical device is reflected by any element outside of the electro-optical device, or in a projection type display device, such as a color-displayable liquid crystal projector including a plurality of electro-optical devices, a light emitted from other electro-optical device and generated by returning to the electro-optical device is reflected by the data

line to thereby prevent the stray light from being increased. This is because the portion of the data line formed broad is relatively narrower than the capacitive line.

[0065] In this aspect that has the data line having a portion overlapping the thin-film transistor formed broad, the capacitive line is arranged at the overlapped position between the thin-film transistor and the data line, and the data line may be constructed such that the portion provided with a contact hole to connect to the thin-film transistor is formed broad in addition to the portion overlapping the thin-film transistor.

[0066] From this construction, even when the capacitive line as the light-shielding film could is not provided, the decrease in the light-shielding ability can be compensated by forming broad the data line for the contact hole.

[0067] Alternatively, for each thin-film transistor, the data line is formed continuously broad from the portion overlapping the thin-film transistor to the portion in which the contact hole is provided.

[0068] From this construction, the light shielding of the thin-film transistor can be more securely accomplished.

[0069] Further, the portion formed broad in the portion overlapping the thin-film transistor and the portion formed broad in the portion in which the contact hole is provided may be separately formed broad. If arranging the portion overlapping the thin-film transistor and the portion in which the contact hole is provided close to each other and forming them continuously broad as in the present aspect, since the area to be formed broad need not be exceedingly broad, it is advantageous from the point of view of not increasing the inner reflection.

[0070] In another aspect of the electro-optical device of the present invention, another substrate opposing the substrate through an electro-optical material and a light shielding film formed on the another substrate may be further provided, and the width of the data line and the width of a portion extending along the data line in the capacitive line are narrower than that of the light-shielding film.

[0071] From this aspect, if it is assumed that the light is entered from another substrate, the laminated structure of the light-shielding film, the data line and the capacitive line in the order from the light incidence side can be constructed. The width of the former is broader than those of the latter two. That is, the advance of the incident light is blocked by the broader light-shielding film, and only the light passing through it reaches the data line and the capacitive line. Further, when the light passing through the light-shielding film reaches the data line and the capacitive line, the data line and the capacitive line can be expected to

perform the above-described light-shielding function. In short, according to the present aspect, it is possible to enhance the light resistance of the thin-film transistor and to reduce the generation of the light leakage.

[0072] Further, if the pixel electrodes are arranged in a matrix shape, the "light-shielding film" in the present aspect may be formed in a stripe shape or a lattice shape to extend through spaces between the pixel electrodes. Furthermore, according to circumstances, the light-shielding film may be formed as a laminated structure made of, for example, a light-absorbing material, such as chrome or chrome oxide, and a light-reflecting material, such as aluminum.

[0073] An electronic apparatus of the present invention may include the above-described electro-optical device (including various aspects).

[0074] According to the electronic apparatus of the present invention, for example, since it includes the electro-optical device capable of adequately adjusting the arrangement between the thin-film transistor and the scanning line, it is possible to realize various electronic apparatuses, such as a liquid crystal projector, a liquid crystal television, a portable phone, an electronic pocket book, a word processor, a view finder type or monitor direct vision-type videotape recorder, a work station, a video phone, a POS terminal, and a touch panel, capable of precise operation of the thin-film transistor and high quality image display, for example.

[0075] The above effects and other advantages of the present invention will be more apparent from the following exemplary embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0076] FIG. 1 is a schematic circuit diagram illustrating an equivalent circuit of various elements, wirings and the like provided in a plurality of pixels, having a matrix shape, constituting an image display area in an electro-optical device according to an exemplary embodiment of the present invention;

[0077] FIG. 2 is a plan view of a group of adjacent pixels in a TFT array substrate where data lines, scanning lines, pixel electrodes are formed in the electro-optical device according to an exemplary embodiment of the present invention;

[0078] FIG. 3 is a sectional view taken along plane A-A' in FIG. 2;

[0079] FIG. 4 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 2;

[0080] FIG. 5 is a plan view illustrating another exemplary embodiment in which the arrangement of the scanning lines and the TFTs is different from that in FIG. 2;

[0081] FIG. 6 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 5;

[0082] FIG. 7 is a sectional view taken along plane B-B' in FIG. 5;

[0083] FIG. 8 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the scanning lines are buried in the grooves;

[0084] FIG. 9 is a sectional view illustrating a profile of a narrow width portion of the scanning lines shown in FIG. 8;

[0085] FIG. 10 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and a part of the scanning lines are buried in the grooves;

[0086] FIG. 11 is a sectional view illustrating a profile of a narrow width portion of the scanning line shown in FIG. 10;

[0087] FIG. 12 is a sectional view taken along plane T-T' in FIG. 10;

[0088] FIGS. 13(a) and 13(b) are schematics explaining the generation of a horizontal electric field;

[0089] FIG. 14 is a plan view illustrating another exemplary embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the narrow width portion of the scanning line is deviated from the center of a first gap;

[0090] FIG. 15 is a sectional view taken along plane T-T' in FIG. 14;

[0091] FIG. 16 is a plan view illustrating another exemplary embodiment in that a shape of the data line is different from that in FIG. 2;

[0092] FIG. 17 is a sectional view taken along plane P-P' in FIG. 16;

[0093] FIG. 18 is a sectional view taken along plane Q-Q' in FIG. 16;

[0094] FIG. 19 is a sectional view taken along plane R-R' in FIG. 16;

[0095] FIG. 20 is a plan view where the TFT array substrate of the electro-optical device according to the exemplary embodiment of the present invention is viewed from the opposing substrate side along with the respective elements formed thereon;

[0096] FIG. 21 is a sectional view taken along plane H-H' in FIG. 20;

[0097] FIG. 22 is a schematic sectional view illustrating a color liquid crystal projector that is an example of a projection type color display apparatus as an exemplary embodiment of an electronic apparatus of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0098] Preferred exemplary embodiments of the present invention are explained with reference to the drawings. In following exemplary embodiments, an electro-optical device of the present invention is applied to a liquid crystal device.

[0099] First, a construction of a pixel part in the electro-optical device according to an exemplary embodiment of the present invention is explained with reference to FIGS. 1 to 4. Fig. 1 is a schematic that shows an equivalent circuit of various elements, wirings and the like in a plurality of pixels formed in a matrix shape constituting an image display area 10a of the electro-optical device. FIG. 2 is a plan view of a group of a plurality of pixels adjacent to each other on a TFT array substrate in which data lines, scanning lines, pixel electrodes and the like are formed. Further, FIG. 3 is a sectional view taken along plane A-A' in FIG. 2. Further, in FIG. 3, in order for each layer and each member to have recognizable sizes in the drawing, different scales are applied to each layer and each member. Furthermore, FIG. 4 is a plan view illustrating shapes of only the scanning lines extracted from FIG. 2.

[0100] In FIG. 1, in the plurality of pixels formed in a matrix shape constituting the image display area of the electro-optical device according to the present exemplary embodiment, a pixel electrode 9a and a TFT 30 to control switching of the pixel electrode 9a are formed, respectively, and data lines 6a supplied with image signals are electrically connected to sources of the TFTs 30. Image signals S1, S2, ..., Sn to be, in this order, written may be sequentially supplied to the data lines 6a, or may be supplied to each group which has a plurality of data lines 6a adjacent to each other.

[0101] Further, scanning lines 330a are electrically connected to gates of the TFTs 30 and at a predetermined timing, scanning signals G1, G2, ..., Gn are pulse-like applied to the scanning lines 330a in that order. The pixel electrodes 9a are electrically connected to drains of the TFTs 30, and by closing switches of the TFTs 30, that is, switching elements for a predetermined time interval, the image signals S1, S2, ..., Sn supplied from the data lines 6a are written at a predetermined timing.

[0102] A predetermined level of the image signals S1, S2, ..., Sn which have been written through the pixel electrodes 9a to a liquid crystal that is an example of an electro-optical material are maintained for a predetermined time interval between the pixel electrode 9a and an opposing electrode formed on an opposing substrate. The liquid crystal modulates light by varying orientation or order of molecules according to the applied voltage level, and thus it is possible to execute the gradation display. If it is in a normally-white mode, transmittance for the incident light is decreased in accordance with the voltage applied in a

unit of pixel, and if it is in a normally-black mode, the transmittance for the incident light is increased in accordance with the voltage applied in a unit of pixel. Therefore, as a whole, light having a contrast responsive to the image signals is emitted from the electro-optical device.

[0103] In order to reduce or prevent the maintained image signals from being leaked, a storage capacitor 70 is added in parallel to a liquid crystal capacitor formed between the pixel electrode 9a and the opposing electrode.

[0104] A more specific construction of the electro-optical device in which the above-described circuit operation is executed by using the data lines 6a, the scanning lines 330a, the TFTs 30 and the like is explained with reference to FIGS. 2 and 3.

[0105] First, the electro-optical device according to the present exemplary embodiment, as shown in FIG. 3 which is a sectional view taken along plane A-A' in FIG. 2, includes a TFT array substrate 10 and a transparent opposing substrate 20 arranged opposite thereto. The TFT array substrate 10 is made of, for example, a quartz substrate, a glass substrate or a silicon substrate, and the opposing substrate 20 is made of, for example, a glass substrate or a quartz substrate.

[0106] As shown in FIG. 3, the TFT array substrate 10 is provided with a pixel electrode 9a, and an upper portion of the pixel electrode is provided with an oriented film 16 which has been subjected to a predetermined orientation process, such as a rubbing process. The pixel electrode 9a is made of, for example, a transparent conductive film, such as an ITO (Indium Tin Oxide) film.

[0107] The opposing substrate 20 is provided over the whole surface thereof with an opposing electrode 21, and a lower portion of the electrode is provided with an oriented film 22 which has been subjected to a predetermined orientation process, such as a rubbing process. The opposing electrode 21 is made of, for example, a transparent film, such as an ITO film.

[0108] Next, in FIG. 2, a plurality of pixel electrodes 9a (profiles thereof are indicated by dotted lines 9a') are provided in a matrix shape on the TFT array substrate 10 of the electro-optical device, and data lines 6a of aluminum films and scanning lines 330a of poly-silicon films are provided along horizontal and vertical boundaries of the pixel electrodes 9a.

[0109] Each scanning line 330a is arranged opposite to a channel area 1a' indicated by oblique lines area extending from lower left to upper right in the semiconductor layer 1a of a poly-silicon film and functions as a gate electrode. That is, in portions where the

scanning lines 330a and the data lines 6a are intersected, TFTs 30 to switch pixels where broad width portions 331a (to be explained later) of the scanning lines 330a are arranged opposite to the channel areas 1a' as gate electrodes are provided. In other words, TFTs 30 in the present exemplary embodiment, in particular, the channel areas 1a' thereof are formed in intersecting areas of the plurality of pixel electrodes 9a arranged in a matrix shape. The intersecting area means an area where, in plan view, a first long gap (X direction in FIG. 2) extending through a space between adjacent pixel electrodes 9a sandwiching the scanning lines therebetween and a second long gap (Y direction in FIG. 2) extending through a space between adjacent pixel electrodes sandwiching the data line 6a therebetween, are intersected.

[0110] More specifically, with reference to FIG. 2, the intersecting area corresponds to, for example, a position farthest from each of a lower-right corner of the pixel electrode 9a shown on the upper-left side of the plan view, a lower-left corner of the pixel electrode 9a shown on the upper-right side, an upper-right corner of the pixel electrode 9a shown on the lower-left side and an upper-left corner of the pixel electrode 9a shown on the lower-right side of the plan view. Since the TFT 30 is formed at such position, it is difficult for an incident light to directly enter the channel area 1a' of the TFT.

[0111] The TFT 30, as shown in FIG. 3, has an LDD (Lightly Doped Drain) structure, and includes a channel area 1a' of the semiconductor layer 1a where a channel is formed by an electric field from the scanning line which functions as a gate electrode as described above, an insulating film 2 having a gate insulating film to insulate the scanning line 330a from the semiconductor layer 1a, a low-concentration source area 1b, a low-concentration drain area 1c, a high-concentration source area 1d and a high-concentration drain area 1e.

[0112] Further, although it is preferable that the TFT 30 has the LDD structure as shown in FIG. 3, the TFT 30 may have an offset structure in which impurities are prevented or substantially prevented from being infiltrated into the low-concentration source area 1b and the low-concentration drain area 1c, or may be a self-alignment type TFT to infiltrate impurities at high concentration using the gate electrode constituting a part of the scanning line 330a as a mask to automatically form the high-concentration source area and the high-concentration drain area. Furthermore, although, in the present exemplary embodiment, the TFT 30 has a single gate structure where only one gate electrode of the TFT 30 for pixel switching is disposed between the high-concentration source area 1d and the high-concentration drain area 1e, the TFT may have a dual, triple or more gate structure where two or more gates are disposed therebetween. Furthermore, the semiconductor layer 1a

constituting the TFT 30 is not limited to the poly-silicon film, but may be made of an amorphous silicon film or a monocrystalline silicon film. A related art, later developed, or known method, such as a pasting method can be employed in formation of the monocrystalline silicon film. By employing the monocrystalline silicon film for the semiconductor layer 1a, it is possible to promote a high performance of the peripheral circuits.

[0113] In the present exemplary embodiment, for the scanning line 330a serving as the gate electrode of the TFT 30, a portion serving as the gate electrode, that is, a portion facing the channel area 1a' of the TFT 30 is formed broader than the other portion, as shown in FIG. 2. That is, in FIG. 2, the scanning line 330a has a broad width portion 331a extending in the Y direction in FIG. 2 to correspond to the channel area 1a' extending in the Y direction in FIG. 2 and a narrow width portion 332a extending through a space between the adjacent pixel electrodes 9a. In FIG. 4, for the purpose of simplifying the illustration, only the shape pattern of the scanning line 330a is shown.

[0114] In this connection, in the present exemplary embodiment, the broad width portion 331a is lengthened from the narrow width portion 332a. That is, the broad width portion 331a and the narrow width portion 332a are integrally formed. Such a shape can be easily formed, for example, by using a related art, later developed, or known photolithography and etching, on the assumption that a pattern having an integrated shape 332a (see FIG. 4) composed of the broad width portion 331a and the narrow width portion 332a is formed. However, the present invention is not limited to such shape, and includes, for example, even shapes where the broad width portion 331a is formed by connecting other conductive member prepared separately to the narrow width portion 332a, within the scope thereof.

[0115] The storage capacitor 70 shown in FIG. 1 is constructed such that a junction layer 71 as the capacitor electrode on the pixel potential side connected to the high-concentration drain area 1e of the TFT 30 and the pixel electrode 9a and a part of the capacitive line 300 as the capacitor electrode on the fixed potential side are arranged opposite to each other via an dielectric film 75, as shown in FIG. 3. By the storage capacitor 70, it is possible to markedly enhance the potential maintenance characteristics in the pixel electrode 9a.

[0116] The junction layer 71 is made up of, for example, the conductive poly-silicon film and serves as a capacitor electrode on the pixel potential side. However, similar to the capacitive line 300 to be explained in detail below, the junction layer 71 may be made

of a single layer film or multi-layer film containing metal or alloy. In addition to the function as a capacitor electrode on the pixel potential side, the junction layer 71 also has a function of connecting the pixel electrode 9a and the high-concentration drain area 1e of the TFT 30 to each other through contact holes 83 and 85.

[0117] By using such junction layer 71, even if the distance between layers is as long as, for example, 2000nm, both layers can be connected well to each other through serial contact holes having two relatively small diameters while avoiding the technical difficulty of connecting both layers to each other through one contact hole, so that an opening ratio of pixel can be increased. Further, in opening the contact hole, it is helpful to prevent or reduce punchthrough in etching.

[0118] The capacitive line 300 is made of, for example, a conductive film containing metal or alloy, and serves as a capacitor electrode on the fixed potential side. The capacitive line 300 is formed overlapping an area to form the scanning line 330a from a plan view, as shown in FIG. 2. More specifically, the capacitive line 300 has a main line portion extending along the scanning line 330a, a protruding portion protruded upwardly in the Y direction along the data line 6a from a portion intersecting the data line 6a and a constricted portion where the portion corresponding to the contact hole 85 is slightly constricted. The protruding portion contributes to increase in the area to form the storage capacitor 70 by using the area on the scanning line 330a and the area below the data line 6a.

[0119] Further, the capacitive line 300 is made of, for example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one of metals having high melting point, such as Ti, Cr, W, Ta, Mo, and in addition to the function as a capacitor electrode on the fixed potential side of the storage capacitor 70, the capacitive line 300 has a function as a light-shielding layer to shield the TFT 30 from the incident light on the upper side of the TFT 30. However, the capacitive line 300 may have a multi-layer structure in which a first film made of a conductive poly-silicon film and the like and a second film made of a metal silicide film containing metal and the like having high melting point are stacked.

[0120] Furthermore, preferably, the capacitive line 300 extends from the image display area in which the pixel electrodes 9a are arranged to peripheries thereof, and is electrically connected to a potentiostatic source to be a fixed potential. Such potentiostatic source may be a potentiostatic source, such as a plus power source or a minus power source supplied to a data line driving circuit to be explained later, or may be a potentiostatic source supplied to the opposing electrode 21 of the opposing substrate 20.

[0121] A dielectric film 75, as shown in FIG. 3, is constructed of a silicon oxide film such as a HTO (High Temperature Oxide) film or a LTO (Low Temperature Oxide) film having, for example, a relatively thin thickness of about 5~200nm, or a silicon nitride film. From the point of view of increasing the capacitance of the storage capacitor 70, the dielectric film 75 should be preferably as thin as possible as long as the reliability of the film is sufficiently maintained.

[0122] In FIGS. 2 and 3, in addition, the lower side of the TFT 30 is provided with a lower light-shielding film 11a. The lower light-shielding film 11a is patterned in a lattice shape, and as a result, the opening area of each pixel is defined. Further, the opening area may be defined by the intersection of the data line 6a extending in the Y direction in FIG. 2 and the capacitive line 300 extending in the X direction in FIG. 2. Furthermore, similar to the case of the above-described capacitive line 300, the lower light-shielding film 11a may be formed extending from the image display area to the peripheries thereof to be connected to a potentiostatic source so that the potential variation has no adverse effects on the TFT 30.

[0123] Further, a base insulating film 12 is provided below the TFT 30. In addition to the function of insulating the TFT 30 from the lower light-shielding film 11a, since the base insulating film 12 is formed on the whole surface of the TFT array substrate 10, the base insulating film 12 has a function of preventing or reducing the characteristic variation of the TFT 30 for pixel switching caused by rough polished surface of the TFT array substrate 10 or contaminants left after washing.

[0124] In addition, a first interlayer insulating film 41 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 83 communicating with the high-concentrating drain area 1e, respectively, is formed on the scanning line 330a.

[0125] The junction layer 71 and the capacitive line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 85 communicating with the junction layer 71 are formed respectively on the junction layer 71 and the capacitive line 300.

[0126] Furthermore, in the present exemplary embodiment, by baking the first interlayer insulating film 41 at about 1000°C, activation of ions injected into the poly-silicon film constituting the semiconductor layer 1a or the scanning line 330a may be intended. On the other hand, by not baking the second interlayer insulating film 42, relief of stress occurring in the vicinity of the interface of the capacitive line 300 may be intended.

[0127] The data line 6a is formed on the second interlayer insulating film 42, and above them a third interlayer insulating film 43 which has a contact hole 85 communicating the junction layer 71 is formed.

[0128] The surface of the third interlayer insulating film 43 is leveled by means of CMP (Chemical Mechanical Polishing) process, and as a result, the orientation failure of the liquid crystal layer 50 caused by a step generated by various wirings or elements below the third interlayer insulating layer 73 can be reduced.

[0129] However, in place of performing the leveling process for the third interlayer insulating film 43, or in addition to it, a groove, in at least one of the TFT array substrate 10, the base insulating film 12, the first interlayer insulating film 41 or the second interlayer insulating film 42, can be formed to buried the wirings, such as the data line 6a or the TFT 30 to perform the leveling process.

[0130] According to the electro-optical device of the present exemplary embodiment as constructed like the above, since the scanning line 330a has the broad width portion 331a and the narrow width portion 332a and the broad width portion 331a is formed to face the channel area 1a' of the TFT 30, the arrangement between the TFT 30 and the scanning line 330a can be easily adjusted or determined.

[0131] For example, the arrangement between the TFTs 30 and the scanning lines 330a in FIG. 2 described above shows an example of a suitable arrangement responsive to the requirement to effectively prevent or substantially prevent light from entering the channel areas 1a' of the TFTs 30. In addition, for example, the arrangements shown in FIGS. 5 and 6 can be implemented. FIG. 5 is a diagram with the same purpose as FIG. 2, in which an arrangement of the scanning lines and the TFTs is different from that in FIG. 2, and FIG. 6 illustrates only a shape pattern of the scanning lines shown in FIG. 5, similar to FIG. 4.

[0132] In FIGS. 5 and 6, the scanning lines 330a', more specifically, the narrow width portions 332a' are formed at positions deviated from the center of a first long gap extending through a space between the adjacent pixel electrodes 9a sandwiching the scanning lines 330a' therebetween. Further, the broad width portions 331a' are formed to be protruded only upwardly in the Y direction in FIG. 5 and 6. Furthermore, the arranged positions of the channel areas 1a', that is, the arranged positions of the broad width portion 331a' are similar to those in FIG. 2.

[0133] This arrangement can enhance the quality of display image. The reason thereof is as follows. That is, in the electro-optical device according to the present invention, as described above, the oriented film 16 is provided on the pixel electrodes 9a, and on the

surface of the oriented film 16, unevenness due to the "height" of various elements formed below the oriented film 16 can exist. The above-described "various elements" include the scanning lines 330a' of the present exemplary embodiment. FIG. 7 is a sectional view taken along plane B-B' in FIG. 5, in which a convex portion 501 caused by the "height" of the narrow width portion 332a' of the scanning line 330a' is formed on the oriented film 16.

[0134] When the convex portion 501 is generated, there is a possibility of further generating nonuniformity in the above-described rubbing process performed on the oriented film 16. This nonuniformity may cause the bad orientation of the liquid crystal and thus the operation failure of the electro-optical device. Therefore, in the related art, by providing the light-shielding film in the vicinity of the above-described convex portion 501, shielding of the incident light is made possible. That is, the incident light reaching the light-shielding film is reflected or absorbed by the light-shielding film and thus does not contribute to the image display.

[0135] At this time, it is important that the above-described light-shielding film should be provided while satisfying the requirements to enhance the pixel opening ratio. That is, when the light-shielding film is provided only to correspond to the convex portion 501, it may unnecessarily worsen the pixel opening ratio to deteriorate the brightness of image. When the light-shielding film is provided only in a part of the convex portion 501, sufficient light-shielding cannot be accomplished and may cause the deterioration of the contrast ratio. In addition, the influence of the nonuniformity in the convex portion 501 may lead to the operation failure of the electro-optical device.

[0136] In the present exemplary embodiment, it has been paid attention to the fact that the nonuniformity are generated in the convex portion 501, more specifically, that the portion (hereinafter, "rubbing-up portion 501a" in Fig. 7) associated with rubbing up the convex portion 501 (that is, the direction ascending the convex portion 501) and the portion (hereinafter "rubbing-down portion 501b" in Fig. 7) associated with rubbing down the convex portion 501 (that is, the direction descending the convex portion 501), have nonuniformity different from each other.

[0137] More specifically, for example, it has been paid attention to the fact that it is more difficult to generate the nonuniformity in the rubbing-up portion 501a than in the rubbing-down portion 501b, that is, the rubbing-down portion 501b has the higher possibility of causing the bad orientation of the liquid crystal.

[0138] In the present exemplary embodiment, it is important that the narrow width portions 332a' adjacent in the direction of the scanning lines 330a' in FIG. 5 are formed at the

position deviated from the center (see the two-dotted chain line in FIG. 7) between the pixel electrodes 9a. That is, by forming the narrow width portion 332a' at the position shown in FIG. 7, a vertex 501P of the convex portion 501 caused by the narrow width portion 332a' is also formed at the position deviated from the center between the adjacent pixel electrodes 9a. This means that it is possible to construct only almost half of the sloping surface of the convex portion 501 on the area corresponding to the first gap, that is, the rubbing-down portion 501b on the area. Further, in this case, as shown in FIG. 7, by providing the light-shielding capacitive line 300 and the junction layer 71 corresponding to the space between the adjacent pixel electrodes 9a, it is possible to effectively shield only the rubbing-down portion 501b, that is, to effectively shield the corresponding portion of the convex portion 501 expected to be most influenced by the nonuniformity.

[0139] As a result, according to the present exemplary embodiment, since the operation failure of the electro-optical device caused by the nonuniformity can be substantially prevented, and since the rubbing-up portion 501a of the convex portion 501 is not expected to be influenced by the nonuniformity remains to transmit the light contributing to the image display, it is possible to enhance the pixel opening ratio, that is, to maintain the bright image. Consequently, according to the present embodiment, from the above-described point of view, an enhancement in the quality of the display image can be obtained.

[0140] Further, by forming the narrow width portion 332a' at the position deviated from the center of the first gap, it is possible to enhance the degree of freedom in the design of the electro-optical device and to effectively prevent or substantially prevent the light from entering the TFT 30. The reason thereof is as follows.

[0141] That is, although the narrow width portion 332a' in the present exemplary embodiment extends through the first gap between the adjacent pixel electrodes 9a, it does not exist at the center thereof. For this reason, for example, by using an area not provided with the narrow width portion 332a' in the first gap, other wirings such as the capacitive line 300 made of the same film as the narrow width portion 332a' can be formed parallel to the narrow width portion 332a' from a plan view. That is, the degree of freedom in design can be increased.

[0142] Further, in the above-described case, although the narrow width portion 332a' is deviated from the center line, by adjusting the width of the broad width portion 331a', for example, by broadening only one side thereof or by broadening one side thereof more than the other side, it is possible to arrange the broad width portion 331a' as the gate electrode at the center of the gap. In the present exemplary embodiment, as shown in FIGS. 5 and 6, it

can be understood that the broad width portion 331a' is broadened toward only one side. Hence, since the gate electrode can be arranged at a position advantageous to enhance the light-shielding ability irregardless of the position of the scanning line 330a', or since the scanning line 330a' can be arranged at an arbitrary position in the gap while arranging the gate electrode at a position advantageous for improving the light-shielding ability, it is possible to increase the degree of freedom in an arrangement of wirings, such as an arrangement of the scanning line 330a' and to obtain the TFT 30 originally having a substantially high light-shielding ability.

[0143] In short, in the embodiment shown in FIGS. 5 and 6, while satisfying the requirements to enhance the quality of the display image, enhancing the degree of freedom in design and decreasing the light leak current in the TFT 30, it is possible to adequately adjust/determine the arrangement between the channel area 1a' (or the TFT 30) and the gate electrode (or the scanning line 330).

[0144] As described above, according to the electro-optical device of the present exemplary embodiment, since the scanning line, as the gate electrode, has the broad width portion and the narrow width portion, while satisfying the above various requirements or a general requirement, such as high precision of the electro-optical device itself, it is possible to adequately adjust/determine the arrangement between the channel area (or the TFT) and the gate electrode (or the scanning line).

(Second exemplary embodiment)

[0145] Now, a second exemplary embodiment of the present invention is explained with reference to FIGS. 8 to 11. FIGS. 8 and 10 are plan views illustrating another exemplary embodiment different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10 and at least a part of the scanning line is buried in the groove. FIGS. 9 and 11 are sectional views illustrating a profile of the narrow width portion of the scanning line according to the second exemplary embodiment, respectively (FIG. 9 corresponds to FIG. 8, and a section taken along a line Z1-Z1' in FIG. 8 corresponds to a section taken along plane Z1-Z1' in FIG. 9. Further, FIG. 11 corresponds to FIG. 10, and a section taken along plane Z2-Z2' in FIG. 10 corresponds to a section taken along plane Z2-Z2' in FIG. 9). Further, FIG. 12 is a sectional view taken along plane T-T' in FIG. 10. Furthermore, since the basic construction and operation, etc., of the electro-optical device of the second exemplary embodiment are similar to those of the first exemplary embodiment, explanation about distinctive portions in the second exemplary embodiment are mainly described below. Furthermore, the reference numerals in FIGS. 8 and 12 indicate the same elements as in

FIGS. 1 to 7 referred to in the above description, when they indicate substantially equivalent elements.

[0146] First, in one aspect of the second exemplary embodiment, as shown in FIGS. 8 and 9, a groove 3G1 is formed along the scanning line in the TFT array substrate 10. The groove 3G1 is formed except for the area where the semiconductor layer 1a of the TFT 30 is formed. By this construction, in consideration of only the grooves, the grooves 3G1 are arranged in a matrix shape from a plan view (see FIG. 8). Further, a scanning line 340a is formed such that the narrow width portion 342a thereof is entirely buried in the groove 3G1 (see FIG. 9).

[0147] In another aspect of the second embodiment, as shown in FIGS. 10 and 11, a groove 3G2 is formed on the TFT array substrate 10, similarly to the groove 3G1. However, preferably, a groove 3G2 is formed slightly narrower than the groove 3G1. Further, a narrow width portion 352a of the scanning line 350a is formed along the groove 3G2. The narrow width portion 352a has a buried portion 352aB of which a part is buried in the groove 3G2 and a non-buried portion 352aNB which is not buried in the groove 3G2 and extends parallel to the buried portion 352aB. The non-buried portion 352aB is formed on the surface of the TFT array substrate 10.

[0148] Further, in one aspect and another aspect of the second exemplary embodiment, as shown in FIGS. 8 and 10, a groove 6G1 is formed in the TFT array substrate 10 along the data line. Furthermore, the data line 6a is formed to be entirely buried in the groove 6G1. In addition, the semiconductor layer 1a is also formed to be entirely buried in the groove 6G1.

[0149] According to the electro-optical device of the second exemplary embodiment constructed as above, the following effects can be obtained. First, since the whole part or a part of both of the scanning lines 340a and 350a are buried in the grooves 3G1 or 3G2, as shown in FIGS. 9 and 11, in this buried portion, the surface height of the base insulating film 12 and the height of the buried portion 352aB of the scanning line 340a and the scanning line 350a are almost equal to each other to maintain the leveling feature. By this, the leveling feature of the first to third interlayer insulating film 41 to 43 formed as the upper layers of the scanning lines 340a and 350a, or the pixel electrode 9a and the oriented film 16 can be well obtained. Therefore, in the second exemplary embodiment, for example, since a step along the narrow width portion 342a or the buried portion 352aB does not substantially appear on the surface of the oriented film 16, the rubbing process can be very suitably performed on the oriented film 16 and the bad orientation can be drastically

prevented or reduced. Furthermore, an effect can be obtained that the light leakage caused by the bad orientation and deterioration of the image quality based on the light leakage.

[0150] Such effects on the portion along the data line 6a can be obtained because of the existence of the groove 6G1.

[0151] Further, in FIGS. 10 and 11, in particular, because of the existence of the non-buried portion 352aNB, the following effects can be obtained. The effects are explained in detail below.

[0152] First, in the electro-optical device of the present exemplary embodiment, generally in order to prevent or reduce deterioration of the electro-optical material caused by the application of DC voltage and to prevent or reduce the cross-talk or flicker in the displayed image, an inverse driving method of inversing the polarities of voltages applied to the respective pixel electrodes 9a in a predetermined rule may be employed. More specifically, so-called "1H inverse driving method" is explained below.

[0153] First, as shown in FIG. 13(a), during the time to display image signals for the n-th field (n is a natural number) or frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is driven with the same polarity for every row. Thereafter, as shown in FIG. 13(b), when the image signals for the n+1-th field or frame are displayed, the polarity of the liquid crystal driving voltage for each pixel electrode 9a is inversed and during the time for displaying the image signal of the n+1th field or one frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is not inversed, and each pixel electrode is driven with the same polarity for every row. Then, the state shown in FIG. 13(a) and 13(b) is repeated at the period of one field or one frame. This is the 1H inverse driving method. As a result, while avoiding deterioration of the liquid crystal caused by the application of DC voltage, it is possible to prevent image display with reduced cross-talk or flicker. Further, the 1H inverse driving method is more advantageous than the 1S inverse driving method to be explained later, in that there is no almost cross-talk in the vertical direction (Y direction) in the drawing.

[0154] However, as can be understood from FIG. 13(a) and FIG. 13(b), in the 1H inverse driving method, a horizontal electric field takes place between the pixel electrodes 9a adjacent to each other in the vertical direction (Y direction) in the drawing. In these drawings, an area C1 where the horizontal electric field takes place is always in the vicinity of the gap between the pixel electrodes adjacent to each other in the Y direction. If such horizontal electric field is applied, for the electro-optical material to which a vertical electric field, i.e., an electric field perpendicular to the surface of the substrate, is applied, between

the pixel electrode and the opposing electrode facing each other, the operation failure can be caused by the bad orientation of the liquid crystal in the electro-optical material and by the light leakage in the portion, which leads to a problem of decreasing the contrast ratio.

[0155] With respect to the above, the area where the horizontal electric field is generated can be covered by the light-shielding film. However, in this case, there is a problem that the opening area of pixels becomes narrow in respect to the area where the horizontal electric field is generated. In particular, as the distance between the adjacent pixel electrodes becomes small due to minuteness of the pixel pitch, such horizontal electric field increases, and thus this poses a serious problem in a higher precision electro-optical device.

[0156] In the aspect shown in FIGS. 10 and 11 of the second exemplary embodiment, a step caused by the height of the non-buried portion 352aNB is formed between the pixel electrodes 9a (that is, the adjacent pixel electrodes 9a to which voltage of inverse polarity is applied) adjacent to each other in the vertical direction. Because of the existence of this step, it is possible to intensify the vertical electric field in the vicinity of an edge portion of the pixel electrode 9a arranged on the step and to weaken the horizontal electric field. More specifically, as shown in FIG. 12, the distance between the vicinity of the edge portion of the pixel electrode 9a arranged on the step 430 and the opposing electrode 21 becomes narrower by the height of the step 430. Therefore, in the area C1 where the horizontal electric field is generated, the vertical electric field between the pixel electrode 9a and the opposing electrode 21 can be intensified. Furthermore, in FIG. 12, since the gap between the adjacent pixel electrodes 9a is constant, the intensity of the horizontal electric field to be intensified with the gap getting narrow is constant. Therefore, by making the vertical electric field more prevalent in the area C1 where the horizontal electric field is generated, it is possible to prevent or reduce the bad orientation of the liquid crystal caused by the horizontal electric field. Furthermore, because of the step 430 made of the insulating film, the intensity of the horizontal electric field is weakened, and the portion of the liquid crystal affected by the horizontal electric field is decreased by the amount of replacing the step where the horizontal electric field exists. Therefore, the influence of the horizontal electric field on the liquid crystal layer 50 can be reduced.

[0157] Further, in the above description, the 1H inverse driving method has been explained but the present invention is not limited to such a driving method. For example, 1S inverse driving method of inversing the voltage polarity at a period of a frame or a field for each column while driving pixel electrodes in a column with the potential of the same voltage polarity may be employed in the present invention as the inverse driving method of which

control is relatively easy and which enables the high quality image display. Furthermore, between the pixel electrodes adjacent to each other in both of the column direction and the row direction, the dot inverse driving method of inversing the voltage polarity applied to each pixel electrode has been developed and can be applied to the present invention.

[0158] Further, in the second exemplary embodiment, as shown in FIG. 2, the aspect in which the narrow width portion 342a and 352a is formed to extend through the center of the first gap between the adjacent pixel electrodes 9a has been explained. However, the present invention is not limited to such a construction. That is, as shown in FIGS. 5 and 6, in the aspect where the narrow width portion is formed to extend at the position deviated from the center of the first gap, the grooves 3G1 or 3G2 shown in FIGS. 8 to 11 may be formed in a combination. For example, the construction shown in FIGS. 14 and 15 may be employed. FIG. 14 is a plan view illustrating another aspect different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10, and the narrow width portion of the scanning line is deviated from the center of the first gap, and FIG. 15 is a sectional view taken along plane T-T' in FIG. 14.

[0159] FIG. 14 is similar to FIGS. 5 and 6 in that a narrow width portion 362a of a scanning line 360a is deviated from the center of the long first gap extending through the space between the adjacent pixel electrodes 9a, but FIG. 14 is different from FIGS. 5 and 6 in that the narrow width portion 362a is formed along a groove 3G1' formed on the TFT array substrate 10 and a broad width portion 361a is formed to protrude only downwardly in FIG. 14. In this construction, the narrow width portion 362a of the scanning line 360a is formed from the upper portion in the drawing as viewed from the center of the first gap, and thus the narrow width portion 362a is formed to be positioned right below the contact hole 85 for connecting the pixel electrode 9a and the junction layer 71. Further, the narrow width portion 362a is formed to be entirely buried in the groove 3G1'.

[0160] According to this construction, as shown in FIG. 15, the contact hole 85 is formed on the scanning line 360a formed to be buried in the groove 3G1'. In other words, it is possible to form the contact hole 85 on the assumption that the step caused by the height of the scanning line 360a does not substantially appear on the surface of the third interlayer insulating film 43.

[0161] In such a construction shown in FIGS. 14 and 15, in particular, an advantage from the contact hole 85 which can be easily and securely formed can be obtained. That is, assuming that a step due to the height of the scanning line or the narrow width portion is generated on the surface of the third interlayer insulating film 43, there is a possibility of a

disadvantage in that the contact hole 85 may be formed on the vertex or on the ridge of the step. The present construction overcomes such a drawback.

[0162] The above effects can be understood from the following point of view. That is, in the second exemplary embodiment, since the whole or a part of the scanning line is buried in the groove, and thus a step due to the height of the scanning line does not substantially appear on the surface of the respective interlayer insulating film, the formation position or the extending position of the scanning line need not be considered particularly. In other words, if the scanning line is between the adjacent pixel electrodes in the direction thereof, the scanning line may be formed at any position. This is because, even when the formation position or extending position of the scanning line is selected freely and the contact hole is formed thereon, as described above, the contact hole can be relatively easily and securely formed due to the absence of the step.

[0163] Further, in case the narrow width portion has both the buried portion and the non-buried portion, it is preferable to form the groove such that the buried portion is positioned right below the contact hole 85. FIG. 12 corresponds to an example of such a construction.

(Third exemplary embodiment)

[0164] A third exemplary embodiment of the present invention is explained below with reference to FIGS. 16 to 19. FIG. 16 is a plan view illustrating another aspect in that a shape of the data line is different from that in FIG. 2. FIG. 17 is a sectional view taken along plane P-P' in FIG. 16, FIG. 18 is a sectional view taken along plane Q-Q' in FIG. 16, and FIG. 19 is a sectional view taken along plane R-R' in FIG. 16. Further, since the basic construction and operation of the electro-optical device of the third exemplary embodiment are similar to those of the first exemplary embodiment, explanation about distinguishing features of the third exemplary embodiment is mainly described below. Furthermore, reference numerals in FIGS. 16 to 19 indicate the same elements as in FIGS. 1 to 15 referred to in the above description, when they indicates substantially equivalent elements.

[0165] In the third exemplary embodiment, as shown in FIGS. 16 to 19, a data line 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad. Further, a width W1 of a portion extending along the data line 6a1 in the capacitive line 300, that is, the protruded portion 302, first, is broader than a width W2' of the portions except for the broad width portion 6aW in the data line 6a1 (in particular, see FIG. 17). Second, the width W1 of the protruded portion 302 is almost equal to a width W6 of the broad width portion 6aW in the data line 6a1 (see FIG. 18). The channel area 1a' of the

semiconductor layer 1a is positioned almost at the center in the width direction of the broad width direction 6aW and almost at the center in the width direction of the scanning line 3a. Furthermore, in the third exemplary embodiment, as shown in FIGS. 16, 18 and 19, the broad width portion 6aW of the data line 6a1 is formed continuously from the portion overlapping the TFT 30 to the portion in which the contact hole 81 to connect the semiconductor layer 1a of the TFT and the data line 6a is provided, for each TFT 30 arranged in a matrix shape. In addition, in the third exemplary embodiment, as shown in FIGS. 17 to 19, the light-shielding film 23 is formed on the opposing substrate 20. A width WS of one-by-one lattice of the light-shielding film 23 is greater than that of the broad width portion 6aW.

[0166] In the electro-optical device of the third exemplary embodiment constructed like the above, the following effects can be obtained. That is, first, since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 which is formed broad exist on the TFT 30, so called a double light-shielding effect can be obtained. Therefore, it is difficult for the light to enter the channel area 1a' of the TFT 30, and thus the light leak current can be reduced or minimized.

[0167] In particular, in the third exemplary embodiment, the broad width portion 6aW of the data line 6a also exists on the TFT 30 while overlapping the capacitive line 300. In this case, on the TFT 30, the light-shielding ability corresponding to the integrated value of their transmittances can be obtained. Further, since the channel area 1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width portion 6aW and almost at the center in the width direction of the scanning line 3a, the light-shielding ability can be enhanced.

[0168] Second, in connection with such excellent light-shielding ability, in the third exemplary embodiment, as described above, the width W1 of the protruded portion 302 of the capacitive line 300 and the width W6 of the broad width portion 6aW of the data line 6a are less than the width WS of the light-shielding film 23 on the opposing substrate 20 (that is, WS>W1, WS>W6). According to this, the light entered from the upper portion of the TFT 30 is first shielded by the light-shielding film 23 and is further shielded by the broad width portion 6aW of the data line 6a. Furthermore, although passing through the broad width portion 6aW, the incident light is next shielded by the protruded portion 302 of the capacitive line 300. In short, in the third exemplary embodiment, since triple light-shielding is implemented, it becomes more difficult for the light to enter the TFT 30.

[0169] Third, in the third exemplary embodiment, the broad width portion 6aW of the data line 6a is formed continuously from the portion overlapping the TFT 30 to the

contact hole 81 for each TFT 30 arranged in a matrix shape. Since the contact hole 81 is provided to connect the semiconductor layer 1a of the TFT 30 and the data line 6a as described above, the capacitive line 300 cannot be formed in the portion. However, in the third exemplary embodiment, in the formation position of the contact hole 81, the broad width portion 6aW of the data line 6a exists similarly to the upper portion of the TFT 30. Therefore, deterioration of the light-shielding ability caused by the absence of the capacitive line 300 can be compensated by the existence of the broad width portion 6aW. In this connection, as in the third exemplary embodiment, according to the aspect that the broad width portion 6a is formed continuously on the TFT 30 and on the formation position of the contact hole 81, since it is not necessary to broaden exceedingly the formation area of the broad width portion 6aW, it is preferable not to increase the inner reflection.

[0170] As described above, in the third exemplary embodiment, by the combination of various effects, the possibility of the light incidence to the channel area 1a' is drastically decreased, and the generation of the light leak current in the TFT 30 and consequently the generation of the flicker and the like on the image due to the light leak current can be effectively suppressed, reduced or minimized.

(The whole construction of the electro-optical device)

[0171] The whole construction of the electro-optical device according to the present exemplary embodiment constructed like the above is explained with reference to FIGS. 20 and 21. Further, FIG. 20 is a plan view of the TFT array substrate along with the respective elements formed thereon viewed from the opposing substrate 20 side, and FIG. 21 is a sectional view taken along plane H-H' in FIG. 20.

[0172] In Figs. 20 and 21, in the electro-optical device according to the present exemplary embodiment, the TFT array substrate 10 and the opposing substrate 20 are arranged opposite to each other. A liquid crystal layer 50 is inserted and sealed between the TFT array substrate 10 and the opposing substrate 20 and the TFT array substrate 10 and the opposing substrate 20 are affixed to each other by a sealing material 52 provided in the sealing area positioned around the image display area 10a.

[0173] In the outer area of the sealing material 52, a data line drive circuit 101 to drive the data line 6a by supplying image signals to the data line 6a at a predetermined timing, and the external circuit connecting terminals 102 are provided along one side of the TFT array substrate 10, and scanning line drive circuits 104 to drive the scanning line 3a by supplying scan signals to the scanning line 3a at a predetermined timing is provided along two sides adjacent to the one side.

[0174] Further, if delay of the scan signals supplied to the scanning line 3a does not matter, the scanning line drive circuit 104 on only one side is sufficient. Furthermore, the data line drive circuit 101 may be arranged on both sides along the sides of the image display area 10a.

[0175] The remaining one side of the TFT array substrate 10 is provided with a plurality of wirings 105 for connection between the scanning line drive circuits 104 provided on both sides of the image display area 10a. Further, at least one corner of the opposing substrate 20 is provided with a conductive material 106 for electrical connection between the TFT array substrate 10 and the opposing substrate 20. Furthermore, as shown in FIG. 21, the opposing substrate 20 having almost the same profile as the sealing material 52 shown in FIG. 20 is bonded to the TFT array substrate 10 through the sealing material 52.

[0176] In FIG. 21, after the TFTs for switching pixels, or wirings, such as the scanning lines, the data lines are formed on the TFT array substrate 10, and the oriented film is formed on the pixel electrodes 9a. In addition to the opposing electrode 21, the oriented film is formed on the uppermost portion of the opposing substrate 20. Further, the liquid crystal layer 50 is formed of the liquid crystal in which, for example, one kind or several kinds of nematic liquid crystal are mixed, and is oriented in a predetermined state between a pair of oriented films.

[0177] Furthermore, on the TFT array substrate 10, in addition to the data line drive circuit 101 and the scanning line drive circuit 104, a sampling circuit to apply image signals to the plurality of data lines 6a at a predetermined timing, a precharge circuit to supply a precharge signal of a predetermined voltage level to the plurality of data lines prior to the image signals, an inspection circuit to inspect the quality or defects of the electro-optical device during production thereof or in shipping thereof and the like may be formed.

(Exemplary Embodiment of electronic apparatus)

[0178] Next, for an embodiment of a color display device of a projection type that is an example of an equipment using the above-described electro-optical device as a light bulb, the whole construction thereof, in particular, the optical construction thereof is explained. FIG. 22 is a diagrammatic sectional view of the color display device of a projection type.

[0179] In FIG. 22, a liquid crystal projector 1100 that is an example of the color display device of a projection type in the present exemplary embodiment includes three liquid crystal modules including the liquid crystal device in which the drive circuit is mounted on the TFT array substrate, and further includes the respective light bulbs 100R, 100G and 100B

for RGB. In the liquid crystal projector 1100, when transmitted light is emitted from a lamp unit of white light source such as a metal halide lamp, the light is divided into the light components R, G and B corresponding to the three primary colors RGB by three mirrors 1106 and two dichroic mirrors 1108 and guided to the light bulbs 100R, 100G and 100B corresponding to the respective colors, respectively. At this time, in particular, in order to prevent or reduce the light loss caused by the long light path, the B light is guided through a relay lens system 1121 composed of an incident lens 1122, a relay lens 1123 and an exit lens 1124. Then, the light components corresponding to the three primary colors modulated, respectively, by the light bulbs 100R, 100G and 100B are synthesized again by a dichroic prism 1112, and then are projected as a color image to a screen 1120 through a projecting lens 1114.

[0180] The present invention is not limited to the above-described exemplary embodiments, and instead may be appropriately varied without departing from the gist or the spirit of the invention known throughout the claims and the specification. The electro-optical devices including such variation, for example, an electrophoresis apparatus or an electro-luminescence display device, or the electronic apparatus including these electro-optical devices are also included in the technical range of the present invention.

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SPECIFICATION

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to an electro-optical device capable of performing active matrix drive and to an electronic apparatus having the same device.

2. Description of the related art

Conventionally, an electro-optical device comprising a pair of substrates constructed to sandwich an electro-optical material such as a liquid crystal therebetween and electrodes provided in each of the pair of substrates for applying an electric field to the electro-optical material is known. The electrodes are used for applying an electric field to the electro-optical material to vary the state of the material. According to such electro-optical device, for example, when the light emitted from a light source enters the device and the state of the electro-optical material is varied, it is possible to control the light transmittance and thus realize desired image display.

Moreover, in electro-optical devices, by providing pixel electrodes arranged in a matrix shape, thin-film transistors (hereinafter, referred to as "TFT") connected to the respective pixel electrodes, and scanning lines and data lines connected to each of TFTs and provided in parallel to a row direction and a column direction, respectively, on one of the pair of substrates, it is known that active matrix drive can be performed. As a result, for each pixel defined by the pixel electrodes or the scanning lines and the data lines, it is possible to control the electric field applied to the electro-optical material and to control

the light transmittance.

SUMMARY OF THE INVENTION

However, in conventional electro-optical devices, there are following problems. That is, for an electro-optical device capable of performing the above active matrix drive, it is required to precisely drive the TFTs. However, to precisely drive the TFTs is a difficult task while satisfying the high precision and miniaturization requirements imposed in the recent electro-optical device.

TFT comprises a semiconductor layer having a channel area, a source area and a drain area, and a gate electrode formed through an insulating film to cover at least a part of the channel area of the semiconductor layer. By applying or not applying the electric field to the channel area in accordance with the current applied (or not applied) to the gate electrode, the current flow can be controlled.

At this time, the length of the channel area, refereed to as "channel length" or a width thereof, refereed to as "channel width", that is, the size of the channel area is, is important for determining the characteristics of TFTs. Further, an arrangement of the gate electrode on the channel area is also a very important factor. In this regard, conventionally, a conductive member electrically connected to the scanning line or a member constituting a part of the scanning line was used as the gate electrode. However, there are problems in arranging the scanning line itself and the channel area.

In short, it is required to realize a suitable arrangement of the channel area (or TFT) and the scanning line (or gate electrode) while realizing the high precision required in the electro-optical devices. Further, it is required to realize the difficult task of precisely operating the TFT constructed as such.

For example, it is not sufficient to drive the electro-optical device only by the TFT

and the scanning line (or the gate electrode) and various elements are additionally required. However, it is generally difficult to accomplish the above arrangement or adjustment in connection with various other elements. Further, in the TFT, there is a disadvantage in that if is required to prevent the light leakage current which is generated by the light entering the channel area. That is, it is preferable that the TFT is arranged as far as possible from a light-transmitting area, which is an area that the light contributes to image display in each pixel emitted through transmission or reflection, more specifically, from the pixel electrode. However, since this should be realized while satisfying the requirement of high precision, there is a further disadvantage in that the above arrangement/adjustment becomes more difficult an even more different task.

The present invention is made in consideration of the above problems. Therefore, an object of the present invention is to provide an electro-optical device capable of easily adjusting the arrangement of a gate electrode and a scanning line and capable of precisely driving TFT and an electronic apparatus comprising the electro-optical device.

In order to solve the above problems, the electro-optical device of the present invention comprises, on a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction intersecting the scanning lines, thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes formed correspondingly to the thin-film transistors, wherein the respective scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

According to the electro-optical device of the present invention, by supplying scan signals and image signals to the thin-film transistors through the scanning lines and the data lines, the pixel electrodes can be driven in an active matrix mode.

More specifically, in the present invention, since the scanning lines have the broad width portions as the gate electrode in a portion facing the channel area of the thin-film transistor and the narrow width portion in other portion, it is not only possible to realize the narrowness of the scanning line but also to more easily adjust/determine the arrangement between the channel area (or the thin-film transistor) and the scanning line than in the conventional art.

For example, when a plurality of pixel electrodes are arranged in a matrix shape, it is generally preferable that the thin-film transistor are configured such that the channel area of the thin-film transistor is positioned at the position farthest from the corner of each pixel electrode, that is, at the center position of a space among adjacent and opposite corners of the pixel electrodes when four pixel electrodes are considered (because it is farthest from the light transmitting area). However, in this case, by allowing the channel area to extend through a space between adjacent pixel electrodes including the center position, it is possible to adequately determine the channel length, and by arranging the scanning line to intersect it, it is possible to realize a structure that the broad width portion of the scanning line exists on the channel area. Therefore, in this case, it is possible to simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices. Further, in this case, the light incidence to the thin-film transistor or the channel area can be prevented as much as possible under the above-described assumption.

Like the above, according to the present invention, it is possible to adequately adjust the arrangement between the thin-film transistor and the scanning line or the gate electrode while satisfying the high precision requirements of the electro-optical devices.

Further, this structure renders a good outcome even after arrangement of various elements constituting the electro-optical device has been adjusted and determined, in addition to the above scanning line and the thin-film transistor. Furthermore, according to the present invention, it is possible to precisely drive the thin-film transistor, and thus maintain the quality of image to be displayed at high level.

Further, in the present invention, "broad width" means that it is broader than the width of the "narrow width portion" and "narrow width" means that it is narrower than the width of the "broad width portion". In short, broad and narrow degree of "the broad width portion" and the "narrow width portion" is determined in accordance with the relative relationship between them. Furthermore, the real width of the broad width portion or the narrow width portion can be adequately determined theoretically, experimentally or by means of simulation.

In one aspect of the electro-optical device of the present invention, the broad width portion has a portion lengthened from the narrow width portion.

According to this aspect, it is possible to form the scanning line relatively easily having the broad width portion and the narrow width portion. More specifically, for example, by employing the known photolithography and etching methods with the assumption that the broad width portion and the narrow width portion are formed through the incorporated pattern, the scanning line according to the present aspect can be easily formed.

In another aspect of the electro-optical device of the present invention, the broad width portion has a portion connected to the narrow width portion.

According to this aspect, for example, the broad width portion includes the portion formed by connecting a conductive member and the like prepared separately to the narrow width portion. Even in this case, the broad width portion can be formed

relatively easily.

In another aspect of the electro-optical device of the present invention, the scanning line extends in a direction intersecting the direction in which the channel area extends and the broad width portion extends in a single direction or bi-directionally in which the channel area extends.

According to this aspect, since the broad width portion extends in the single direction or bi-directionally in which the channel area extends, it is possible to more adequately adjust the arrangement of the thin-film transistor and the scanning line. Further, according to this aspect, since the gate electrode is adequately formed in accordance with the channel length, the electric field can be more effectively applied to the channel area.

Further, like the above, according to the aspect that the gate electrode, that is, the broad width portion is provided in the portion to be the channel area corresponding to the channel area, for example, the so-called self-aligned formation of the thin-film transistor (that is, formation of the source area and the drain area adjacent to the channel area through an ion implantation process using the gate electrode as a mask) can be easily executed. However, in this case, strictly speaking, the channel area is formed by carrying out the ion implantation process after forming the broad width portion to be the gate electrode.

In another aspect of the electro-optical device of the present invention, the pixel electrodes are arranged in a matrix shape and the channel areas are formed in an intersecting area in which a first long gap extending through a space between pixel electrodes sandwiching of the scanning line and being adjacent to each other and a second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected.

This aspect is similar to the above mentioned aspect and is one of the aspects in which the operational effect of the present invention is exhibited most effectively.

That is, according to this aspect, the channel area of the thin-film transistor is formed in the intersecting area of the pixel electrodes arranged in a matrix shape. The intersecting area is an area in which the first long gap extending through a space between pixel electrodes sandwiching the scanning line and being adjacent to each other and the second long gap extending through a space between pixel electrodes sandwiching the data line and being adjacent to each other are intersected in a plan view. By such configuration, it is difficult for light to enter the channel area.

Further, along with such operational effect, since the scanning line has the broad width portion as the gate electrode is opposite to the channel area, the arrangement between the channel area (or the thin-film transistor) and the gate electrode (or the scanning line) can be determined most adequately and it is also possible to secure the adequate channel length and narrowness of the scanning line.

In this aspect, in particular, the narrow width portion is formed at a position deviated from a center of the first gap and the broad width portion, is formed at the center of the first gap in the intersecting area.

According to this configuration, the narrow width portion of the scanning line extends through the space between the adjacent pixel electrodes but does not exist at the center thereof and is formed at the position deviated from the center thereof. As a result, first, the improvement in the quality of the displayed image can be obtained, especially for the liquid crystal display device that is an example of the electro-optical device, and the reason thereof is as follows.

That is, in the present aspect, when performing the rubbing process on a convex portion on the oriented film normally provided in the liquid crystal display device, in

particular, a convex portion formed by "height" of the narrow width portion, nonuniformities are usually generated in the convex portion. Further, it is considered that the degree of nonuniformity is different from each other in the portion associated with the rubbing up convex portion (that is, the direction ascending to the convex portion) and the portion associated with the rubbing down convex portion (that is, the direction descending from the convex portion).

More specifically, for example, it is more difficult to generate nonuniformity in the portion associated with the rubbing up convex portion than in the portion associated with the rubbing down convex portion.

Further, if the nonuniformity is left as it is, a poor orientation of the liquid crystal may be caused to result in the operation failure of the electro-optical devices. In the difference in the degree of nonuniformity between the rubbing-up process and the rubbing-down process, the latter has greater possibility to cause the bad orientation of the liquid crystal than the former.

It is significant that the narrow width portion of the present aspect is formed at a position deviated from the center of the first gap between the pixel electrodes. That is, if the narrow width portion is formed at the above-described position, the vertex of the convex portion caused by the narrow width portion is also formed at the position deviated from the center of the first gap, and this means that it is possible to form almost only half inclined surface of the convex portion on the area corresponding to the first gap, that is, to form only the portion associated with the rubbing-down on the area. Further, in this case, if the light-shielding film is provided corresponding to the first gap, it is possible to effectively shield only the portion associated with the rubbing-down, that is, to effectively shield the corresponding portion of the convex portion to be most influenced by the nonuniformity.

As a result, according to the present aspect, since the operation failure of the electro-optical device caused by nonuniformities can be substantially prevented, and the portion of the convex portion associated with the rubbing-up, which is not affected by nonuniformities, is able to transmit the light contributing to the image display. Thus, it is possible to improve the opening ratio of pixel, that is, to provide a brightened image display. As a result, according to the present aspect, from the above-mentioned point of view, the improvement in the display image can be obtained.

Further, by forming the narrow width portion at the position deviated from the center of the first gap, it is also possible to improve the degree of freedom in designing the electro-optical devices and to more effectively prevent light from entering the thin-film transistor. The reason thereof is as follows.

That is, in the present aspect, the narrow width portion extends through the first gap between the adjacent pixel electrodes, but does not exist at the center thereof. For this reason, by using the area in the first gap where the narrow width portion is not provided, in a plan view, it is possible to provide other wires such as the capacitive line made up of the same film as the narrow width portion, in parallel to the narrow width portion. That is, the degree of freedom of design is increased.

Further, in the above-mentioned case, although the narrow width portion is deviated from the center thereof, it is possible to arrange the broad width portion as the gate electrode at the center of the gap, by adjusting the width of the broad width portion, for example, by broadening only one side or by broadening one side more than the other side small. Like the above, since the gate electrode can be arranged at a position advantageous for increasing the light-shielding ability regardless of the position of the scanning line, or since the scanning line can be arranged at an arbitrary portion in the gap while arranging the gate electrode at the position advantageous for increasing the light-

shielding ability, it is possible to realize a thin-film transistor having a high light-shielding ability while increasing the degree of freedom in arranging wires including the arrangement of the scanning lines.

In this configuration, further, the broad width portion may be formed at the center of the second gap in the intersecting area.

According to such construction, the channel area is formed at the position farthest from the adjacent or opposite corners of the electrodes in accordance with the above-described method, when four pixel electrodes are considered to be used. That is, it becomes very difficult for light to enter the channel area.

In another aspect of the electro-optical device of the present invention, grooves are formed in the substrate along the scanning lines, and the scanning lines are buried at least partially in the grooves directly or through an interlayer insulating film.

According to this aspect, since the scanning line is buried in the groove formed in the substrate, the generation of a step on the surface of the interlayer insulating film formed as the upper layer or on the surface of the pixel electrodes and the oriented film, etc. caused by the height of the scanning line itself can be prevented earlier. That is, the surface can be leveled very well. Then, if the surface of the oriented film is leveled, the rubbing process can be adequately performed for the orientation process and the orientated state of the liquid crystal molecules contacting the oriented film can be maintained well. Therefore, according to the present aspect, since the possibility of bad orientation can be decreased and the light leakage caused by the bad orientation can be markedly prevented, it is possible to display a high-quality image.

In another aspect of the electro-optical device of the present invention, the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion not buried in the groove and extending along the scanning

line in parallel to a buried portion, and a base of the pixel electrode is positioned high along the scanning line due to the presence of the non-buried portion.

According to this aspect, the narrow width portion has both the buried portion and the non-buried portion. Then, the both of the buried portion and the non-buried portion extend along the scanning line and the base of the pixel electrode protrudes above along the scanning line due to the presence of the non-buried portion.

Through this construction, first, the effect associated with the above-described leveling can be similarly obtained by the buried portion. That is, the surface of the interlayer insulating film to be formed as the upper layer of the buried portion, or the surfaces of the pixel electrodes and the oriented film have the an excellent leveled feature, and thus it is possible to reduce the possibility of having the bad orientations.

Next, since the step including the convex portion along the scanning line is formed on the surface of the oriented film to be formed as the upper layer of the non-buried portion and the like, the above-described effects of leveling cannot be obtained by the non-buried portion. However, the following advantages can be obtained.

First, in electro-optical device according to the present invention, for the purpose of preventing deterioration of the liquid crystal, increasing the device life and reducing the cross talk or flicker of the displayed image, a method of dividing the pixel electrodes into two groups and then inversely driving them in separate cycles may be employed. That is, a plurality of pixel electrodes including a first pixel electrode group to be inversely driven at a first period and a second pixel electrode group to be inversely driven at a second period compensatory with the first period, are arranged in a plain on the substrate. There are (i) the adjacent pixel electrodes to be driven with driving voltages of inverse polarities at the respective times in the inverse-driving and (ii) the adjacent pixel electrodes to be driven with driving voltages of the same polarity at the respective times in

the inverse driving. If the pixel electrodes corresponding to (i) are arranged in the direction along the data lines and the pixel electrodes corresponding to (ii) are arranged in the direction along the scanning lines, the pixel electrodes arranged in the direction along any one scanning line are driven with one polarity and the pixel electrodes arranged in the direction along another scanning line adjacent to the any one scanning line are driven with an inverse polarity to the one polarity (so-called "1H inverse driving").

However, in this case, between the pixel electrodes adjacent to each other along the data line, the horizontal electric field based on the driving voltages of inverse polarities is generated. Such horizontal electric field may interfere the electric field (may be referred to as vertical electric field in contrast to the horizontal electric field) generated between the pixel electrode and the opposing electrode, and as a result, it becomes difficult to obtain the orientation state of the liquid crystal molecules as desired, so that the image display may be affected.

Further, in the present aspect, in a case that such adverse effects may be caused, the convex portion formed on the base of the pixel electrode along the scanning line has a distinct significance.

That is, first, when the edge portions of the respective pixel electrodes are formed to be positioned on the step, the vertical electric field generated between the respective pixel electrodes and the opposing electrode is intensified compared to the horizontal electric field generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in the different pixel electrode group). That is, since the electric field generally intensifies as the distance between the electrodes becomes shorter, the edge portions of the pixel electrodes near the opposing electrode by the height of the step generates an intense vertical electric field. Second, whether the edge portions of the respective pixel electrodes are positioned on the step or not, the horizontal electric field

generated between the adjacent pixel electrodes (in particular, the pixel electrodes included in a different pixel electrode group) is weakened by the presence of the step in accordance with the dielectric constant, and even by reducing (replacing partially from the step) the volume of the electro-optical material through which the horizontal electric field passes, the effect that the horizontal electric field has on the electro-optical material can be reduced. Therefore, the operation failure from the electro-optical material such as the bad orientation of the liquid crystal by the horizontal electric field caused by the inverse driving method, can be reduced. At this time, as described above, the edge portions of the pixel electrodes may be or not be positioned on the step and may be positioned on the inclined step or on almost vertical side surface thereof.

In addition, since the light-shielding film for concealing the operation failure caused by the electro-optical material, can be formed small, it is also possible to increase the opening ratios of the respective pixels without having the bad image display, caused by the light leakage, generated.

As described above, according to the present aspect, first, due to the presence of the buried portion, the effects associated with the above-described leveling can be obtained, and second, by forming intentionally the step including the convex portion along the scanning line by the presence of the non-buried portion, the generation of the horizontal electric field can be prevented.

In another aspect of the electro-optical device of the present invention, a capacitor electrode on a pixel potential side constituted a storage capacitor connected to the pixel electrode and a a capacitive line having capacitor electrode on a fixed potential side arranged constituting the storage capacitor arranged opposing the capacitor electrode on the pixel potential side through a dielectric film, may be further comprised. The capacitive line has a main line portion extending along the scanning line and a portion extending

along the data line, and a width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line.

According to this aspect, since the storage capacitor, having a construction such that the capacitor electrode on the pixel potential side and the capacitor electrode on the fixed potential side are arranged opposite to each other, is connected to the pixel electrode, the voltage of the image signal written in the pixel electrode can be maintained for a long time. In particular, in the present aspect, since the width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line, it is possible to further lower the resistance of the capacitive line. Further, in the present aspect, since a low resistance of the capacitive line can be realized as described above, from the point of view of the whole device, the narrowness of the capacitive line and further narrowness of the storage capacitor can be accomplished, and as a result, it is possible to improve the opening ratio. In the "narrowness of the capacitive line", since the capacitive line itself has a width equal to or "broader than" the width of the data line on the surface, it may appears to be a contradiction, but the broad width and the narrow width should be determined from the relative relationship between the capacitive line and the data line, such that from the point of view of the whole device, the "narrowness of the capacitive line" can be accomplished, compared to the conventional art. Furthermore, in the broad width and narrow width described above or the "broader than" to be described in the present invention, the discrete values of the width can be adequately determined theoretically, experimentally, experientially or by means of simulation.

Further, according to the present aspect, it is possible to effectively prevent the light from entering the thin-film transistor, in particular the channel area thereof, compared to the conventional art, as well as obtaining the above-described low resistance. This is because, as described above, although in the conventional art, the light reflected

from the back of the data line and the like becomes a stray light and thus may enter the thin-film transistor, but according to the present aspect, the possibility that the advance of such stray light is shielded by the capacitive line formed in the width equal to or broader than that of the data line is increased.

From the above, according to the present invention, the problems such as the cross talk or burn-in that were prevalent in the conventional art can be reduced by means of the low resistance of the capacitive line. Further, since the light leak current in the thin-film transistor is reduced, it is possible to display a high quality image.

Further, in the present invention, since the portion extending along the data line exists in the capacitive line, the area of the storage capacitor can be increased. This markedly contributes to the image display having high quality.

Furthermore, in order to more effectively accomplish the light-shielding function described above, materials having a good light-shielding feature may be employed for the capacitive line. For example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one from Al (aluminum), Cu (copper), Ti (titan), Cr (chrome), W (tungsten), Ta (tantalum), and Mo (molybdenum) can be adequately employed. Further, in addition to the above, for example, light-absorbing materials such as poly-silicon can be employed.

In this aspect, a portion overlapping the thin-film transistor in the data line may be formed locally broad, and a width of the portion extending along the data line in the capacitive line may be broader than that of the portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

By such construction, the portion overlapping the thin-film transistor in the data line is formed locally broad. Then, the width of the portion formed broad is equal to that of the portion extending along the data line in the above-described capacitive line. That

is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Thus, the light entered from the upper portion of the thin-film transistor can be more securely prevented.

More specifically, for example, when the capacitive line is made up of metal having a high melting point, the capacitive line can independently have the light-shielding ability that the transmittance thereof is about 0.1% (2 or more in OD (Optical Density)). However, if the silicide forming process is performed on the capacitive line, the composition thereof is varied and thus the light-shielding ability may be reduced. In this case, only the light-shielding ability having the transmittance of 0.1% or more may be obtained.

However, in the present aspect, the data line overlapping the capacitive line composed of such metal film having a high melting point is further comprised. If the construction for performing the light shielding of the thin-film transistor by means of overlapping the capacitive line and the data line is employed, the light-shielding ability corresponding to the added value of these transmittances can be obtained. For example, when the data line is made up of aluminum, etc., the light-shielding ability with a transmittance of 0.001% or less (4 or more in the OD value) can be accomplished.

Further, in the present aspect, in particular, that the broad width of the portion extending along the data line in the capacitive line is broad means that it is broader than that of the portion not formed broad in the data line.

Also, a portion overlapping the thin-film transistor in the data line is formed locally broad, and a width of the portion extending along the data line in the capacitive line is broader than that of the portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

According to this aspect, the portion overlapping the thin-film transistor in the

data line is formed locally broad. That is, from this construction, the data line and the capacitive line all formed broad are positioned on the thin-film transistor. Therefore, the light entered from the upper portion of the thin-film transistor can be more securely prevented.

Furthermore, in the present aspect, in particular, the width of the portion extending along the data line in the capacitive line is formed narrower than that of the data line. That is, in the portion, the width of the data line is narrower than that of the capacitive line. From this construction, for example, when the data line is made up of aluminum having a high light reflexibility, a stray light generated by reflecting the incident light by any element in the electro-optical device, a light returning to the electro-optical device after a light emitted from the electro-optical device is reflected by any element outside of the electro-optical device, or in a projection type display device such as a color-displayable liquid crystal projector comprising a plurality of electro-optical devices, a light emitted from other electro-optical device and generated by returning to the electro-optical device is reflected by the data line to thereby prevent the stray light from being increased. ⑫ This is because the portion of the data line formed broad is relatively narrower than the capacitive line.

In this aspect that has the data line having a portion overlapping the thin-film transistor formed broad, the capacitive line is arranged at the overlapped position between the thin-film transistor and the data line, and the data line may be constructed such that the portion provided with a contact hole for connecting to the thin-film transistor is formed broad in addition to the portion overlapping the thin-film transistor.

From this construction, even when the capacitive line as the light-shielding film could is not provided, the decrease in the light-shielding ability can be compensated by forming broad the data line for the contact hole.

Alternatively, for each thin-film transistor, the data line is formed continuously broad from the portion overlapping the thin-film transistor to the portion in which the contact hole is provided.

From this construction, the light shielding of the thin-film transistor can be more securely accomplished.

Further, the portion formed broad in the portion overlapping the thin-film transistor and the portion formed broad in the portion in which the contact hole is provided may be separately formed broad. If arranging the portion overlapping the thin-film transistor and the portion in which the contact hole is provided close to each other and forming them continuously broad as in the present aspect, since the area to be formed broad need not be exceedingly broad, it is advantageous from the point of view of not increasing the inner reflection.

In another aspect of the electro-optical device of the present invention, another substrate opposing the substrate through an electro-optical material and a light shielding film formed on the another substrate may be further comprised, and the width of the data line and the width of a portion extending along the data line in the capacitive line are narrower than that of the light-shielding film.

From this aspect, if it is assumed that the light is entered from another substrate, the laminated structure of the light-shielding film, the data line and the capacitive line in the order from the light incidence side can be constructed. The width of the former is broader than those of the latter two. That is, the advance of the incident light is blocked by the broader light-shielding film, and only the light passing through it reaches the data line and the capacitive line. Further, when the light passing through the light-shielding film reaches the data line and the capacitive line, the data line and the capacitive line can be expected to perform the above-described light-shielding function. In short, according

to the present aspect, it is possible to improve the light resistance of the thin-film transistor and to reduce the generation of the light leakage.

Further, if the pixel electrodes are arranged in a matrix shape, the "light-shielding film" in the present aspect may be formed in a stripe shape or a lattice shape to extend through spaces between the pixel electrodes. Furthermore, according to circumstances, the light-shielding film may be formed as a laminated structure made of, for example, a light-absorbing material such as chrome or chrome oxide and a light-reflecting material such as aluminum.

An electronic apparatus of the present invention may comprise the above-described electro-optical device (including various aspects).

According to the electronic apparatus of the present invention, for example, since it comprises the electro-optical device capable of adequately adjusting the arrangement between the thin-film transistor and the scanning line, it is possible to realize various electronic apparatuses such as a liquid crystal projector, a liquid crystal television, a portable phone, an electronic pocket book, a word processor, a view finder type or monitor direct vision-type videotape recorder, a work station, a video phone, a POS terminal, and a touch panel, capable of precise operation of the thin-film transistor and high quality image display.⑫

The above effects and other advantages of the present invention will be more apparent from the following embodiments.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a circuit diagram illustrating an equivalent circuit of various elements, wirings and the like provided in a plurality of pixels, having a matrix shape, constituting an image display area in an electro-optical device according to an embodiment of the

present invention.

FIG. 2 is a plan view of a group of adjacent plural pixels in a TFT array substrate where data lines, scanning lines, pixel electrodes are formed in the electro-optical device according to an embodiment of the present invention.

FIG. 3 is a sectional view taken along a line A-A' in FIG. 2.

FIG. 4 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 2.

FIG. 5 is a diagram with the same purpose as FIG. 2 and illustrates another embodiment in which the arrangement of the scanning lines and the TFTs is different from that in FIG. 2.

FIG. 6 is a plan view illustrating only a shape pattern of the scanning lines shown in FIG. 5.

FIG. 7 is a sectional view taken along a line B-B' in FIG. 5.

FIG. 8 is a diagram with the same purpose as FIG. 2 and illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the scanning lines are buried in the grooves.

FIG. 9 is a sectional view illustrating a profile of a narrow width portion of the scanning lines shown in FIG. 8.

FIG. 10 is a diagram with the same purpose as FIG. 2 and illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and a part of the scanning lines are buried in the grooves.

FIG. 11 is a sectional view illustrating a profile of a narrow width portion of the scanning line shown in FIG. 10.

FIG. 12 is a sectional view taken along a line T-T' in FIG. 10.

FIG. 13 is an explanatory diagram for explaining the generation of a horizontal

electric field.

FIG. 14 is a diagram with the same purpose as FIG. 2 and illustrates another embodiment different from that in FIG. 2 in that grooves are formed on the TFT array substrate and the narrow width portion of the scanning line is deviated from the center of a first gap.

FIG. 15 is a sectional view taken along a line T-T' in FIG. 14.

FIG. 16 is a diagram with the same purpose as FIG. 2 and illustrates another embodiment that a shape of the data line is different from that in FIG. 2.

FIG. 17 is a sectional view taken along a line P-P' in FIG. 16.

FIG. 18 is a sectional view taken along a line Q-Q' in FIG. 16.

FIG. 19 is a sectional view taken along a line R-R' in FIG. 16.

FIG. 20 is a plan view when the TFT array substrate of the electro-optical device according to the embodiment of the present invention is seen from the opposing substrate side along with the respective elements formed thereon.

FIG. 21 is a sectional view taken along a line H-H' in FIG. 20.

FIG. 22 is a schematic sectional view illustrating a color liquid crystal projector that is an example of a projection type color display apparatus as an embodiment of an electronic apparatus of the present invention.

[reference numerals]

1a	SEMICONDUCTOR LAYER
1a'	CHANNEL AREA
330a, 330a', 340a, 350a, 360a	SCANNING LINE
331a, 331a', 341a, 351a, 361a	BROAD WIDTH PORTION
332a, 332a', 342a, 352a, 362a	NARROW WIDTH PORTION

3G1, 3G1', 3G2	GROOVE
352aB	BURIED PORTION
352aNB	NON-BURIED PORTION
430	STEP
9a	PIXEL ELECTRODE
10	TFT ARRAY SUBSTRATE
16	ORIENTED FILM
30	TFT
50	LIQUID CRYSTAL LAYER

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Now, preferred embodiments of the present invention will be explained with reference to the drawings. In following embodiments, an electro-optical device of the present invention is applied to a liquid crystal device.

First, a construction of a pixel part in the electro-optical device according to an embodiment of the present invention will be explained with reference to FIGs. 1 to 4. Fig.1 shows an equivalent circuit of various elements, wirings and the like in a plurality of pixels formed in a matrix shape constituting an image display area 10a of the electro-optical device. FIG. 2 is a plan view of a group of a plurality of pixels adjacent to each other on a TFT array substrate in which data lines, scanning lines, pixel electrodes and the like are formed. Further, FIG. 3 is a sectional view taken along a line A-A' in FIG. 2. Further, in FIG. 3, in order for each layer and each member to have recognizable sizes on the drawing, different scales are applied to each layer and each member. Furthermore, FIG. 4 is a plan view illustrating shapes of only the scanning lines extracted from FIG. 2.

In FIG. 1, in the plurality of pixels formed in a matrix shape constituting the

image display area of the electro-optical device according to the present embodiment, a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed, respectively, and data lines 6a supplied with image signals are electrically connected to sources of the TFTs 30. Image signals S1, S2, ..., Sn to be, in this order, written may be sequentially supplied to the data lines 6a, or may be supplied to each group which has a plurality of data lines 6a adjacent to each other.

Further, scanning lines 330a are electrically connected to gates of the TFTs 30 and at a predetermined timing, scanning signals G1, G2, ..., Gn are pulse-like applied to the scanning lines 330a in that order. The pixel electrodes 9a are electrically connected to drains of the TFTs 30, and by closing switches of the TFTs 30, that is, switching elements for a predetermined time interval, the image signals S1, S2, ..., Sn supplied from the data lines 6a are written at a predetermined timing.

A predetermined level of the image signals S1, S2, ..., Sn which have been written through the pixel electrodes 9a to a liquid crystal that is an example of an electro-optical material are maintained for a predetermined time interval between the pixel electrode 9a and an opposing electrode formed on an opposing substrate. The liquid crystal modulates light by varying orientation or order of molecules according to the applied voltage level and thus it is possible to execute the gradation display. If it is in a normally-white mode, transmittance for the incident light is decreased in accordance with the voltage applied in a unit of pixel and if it is in a normally-black mode, the transmittance for the incident light is increased in accordance with the voltage applied in a unit of pixel. Therefore, as a whole, light having a contrast responsive to the image signals is emitted from the electro-optical device.

In order to prevent the maintained image signals from being leaked, a storage capacitor 70 is added in parallel to a liquid crystal capacitor formed between the pixel

electrode 9a and the opposing electrode.

Now, a more specific construction of the electro-optical device in which the above-described circuit operation is executed by using the data lines 6a, the scanning lines 330a, the TFTs 30 and the like will be explained with reference to FIGs. 2 and 3.

First, the electro-optical device according to the present embodiment, as shown in FIG. 3 which is a sectional view taken along a line A-A' in FIG. 2, comprises a TFT array substrate 10 and a transparent opposing substrate 20 arranged opposite thereto. The TFT array substrate 10 is made of, for example, a quartz substrate, a glass substrate or a silicon substrate, and the opposing substrate 20 is made of, for example, a glass substrate or a quartz substrate.

As shown in FIG. 3, the TFT array substrate 10 is provided with a pixel electrode 9a, and an upper portion of the pixel electrode is provided with an oriented film 16 which has been subjected to a predetermined orientation process such as a rubbing process. The pixel electrode 9a is made of, for example, a transparent conductive film such as an ITO (Indium Tin Oxide) film.

The opposing substrate 20 is provided over the whole surface thereof with an opposing electrode 21, and a lower portion of the electrode is provided with an oriented film 22 which has been subjected to a predetermined orientation process such as a rubbing process. The opposing electrode 21 is made of, for example, a transparent film such as an ITO film.

Next, in FIG. 2, a plurality of pixel electrodes 9a (profiles thereof are indicated by dotted lines 9a') are provided in a matrix shape on the TFT array substrate 10 of the electro-optical device, and data lines 6a of aluminum films and scanning lines 330a of poly-silicon films are provided along horizontal and vertical boundaries of the pixel electrodes 9a.

Each scanning line 330a is arranged opposite to a channel area 1a' indicated by oblique lines area extending from lower left to upper right in the semiconductor layer 1a of a poly-silicon film and functions as a gate electrode. That is, in portions where the scanning lines 330a and the data lines 6a are intersected, TFTs 30 for switching pixels where broad width portions 331a (to be explained later) of the scanning lines 330a are arranged opposite to the channel areas 1a' as gate electrodes are provided. In other words, TFTs 30 in the present embodiment, in particular, the channel areas 1a' thereof are formed in intersecting areas of the plurality of pixel electrodes 9a arranged in a matrix shape. The intersecting area means an area where, in plan view, a first long gap (X direction in FIG. 2) extending through a space between adjacent pixel electrodes 9a sandwiching the scanning lines therebetween and a second long gap (Y direction in FIG. 2) extending through a space between adjacent pixel electrodes sandwiching the data line 6a therebetween, are intersected.

More specifically, with reference to FIG. 2, the intersecting area corresponds to, for example, a position farthest from each of a lower-right corner of the pixel electrode 9a shown on the upper-left side of the plan view, a lower-left corner of the pixel electrode 9a shown on the upper-right side, an upper-right corner of the pixel electrode 9a shown on the lower-left side and an upper-left corner of the pixel electrode 9a shown on the lower-right side of the plan view. Since the TFT 30 is formed at such position, it is difficult for an incident light to directly enter the channel area 1a' of the TFT.

The TFT 30, as shown in FIG. 3, has an LDD (Lightly Doped Drain) structure, and comprises a channel area 1a' of the semiconductor layer 1a where a channel is formed by an electric field from the scanning line which functions as a gate electrode as described above, an insulating film 2 having a gate insulating film for insulating the scanning line 330a from the semiconductor layer 1a, a low-concentration source area 1b, a low-

concentration drain area 1c, a high-concentration source area 1d and a high-concentration drain area 1e.

Further, although it is preferable that the TFT 30 has the LDD structure as shown in FIG. 3, the TFT 30 may have an offset structure in which impurities are prevented from being infiltrated into the low-concentration source area 1b and the low-concentration drain area 1c, or may be a self-alignment type TFT for infiltrating impurities at high concentration using the gate electrode constituting a part of the scanning line 330a as a mask to automatically form the high-concentration source area and the high-concentration drain area. Furthermore, although, in the present embodiment, the TFT 30 has a single gate structure where only one gate electrode of the TFT 30 for pixel switching is disposed between the high-concentration source area 1d and the high-concentration drain area 1e, the TFT may have a dual, triple or more gate structure where two or more gates are disposed therebetween. Furthermore, the semiconductor layer 1a constituting the TFT 30 is not limited to the poly-silicon film, but may be made of an amorphous silicon film or a monocrystalline silicon film. A known method such as a pasting method can be employed in formation of the monocrystalline silicon film. By employing the monocrystalline silicon film for the semiconductor layer 1a, it is possible to promote a high performance of the peripheral circuits.

In the present embodiment, for the scanning line 330a serving as the gate electrode of the TFT 30, a portion serving as the gate electrode, that is, a portion facing the channel area 1a' of the TFT 30 is formed broader than the other portion, as shown in FIG. 2. That is, in FIG. 2, the scanning line 330a has a broad width portion 331a extending in the Y direction in FIG. 2 to correspond to the channel area 1a' extending in the Y direction in FIG. 2 and a narrow width portion 332a extending through a space between the adjacent pixel electrodes 9a. In FIG. 4, for the purpose of simplifying the illustration, only the

shape pattern of the scanning line 330a is shown.

In this connection, in the present embodiment, the broad width portion 331a is lengthened from the narrow width portion 332a. That is, the broad width portion 331a and the narrow width portion 332a are integrally formed. Such shape can be easily formed, for example, by using a known photolithography and etching, on the assumption that a pattern having an integrated shape 332a (see FIG. 4) composed of the broad width portion 331a and the narrow width portion 332a is formed. However, the present invention is not limited to such shape, and includes, for example, even shapes where the broad width portion 331a is formed by connecting other conductive member prepared separately to the narrow width portion 332a, within the scope thereof.

The storage capacitor 70 shown in FIG. 1 is constructed such that a junction layer 71 as the capacitor electrode on the pixel potential side connected to the high-concentration drain area 1e of the TFT 30 and the pixel electrode 9a and a part of the capacitive line 300 as the capacitor electrode on the fixed potential side are arranged opposite to each other via an dielectric film 75, as shown in FIG. 3. By means of the storage capacitor 70, it is possible to markedly improve the potential maintenance characteristics in the pixel electrode 9a.

The junction layer 71 is made up of, for example, the conductive poly-silicon film and serves as a capacitor electrode on the pixel potential side. However, similar to the capacitive line 300 to be explained in detail later, the junction layer 71 may be made of a single layer film or multi-layer film containing metal or alloy. In addition to the function as a capacitor electrode on the pixel potential side, the junction layer 71 also has a function for connecting the pixel electrode 9a and the high-concentration drain area 1e of the TFT 30 to each other through contact holes 83 and 85.

By using such junction layer 71, even if the distance between layers is as long as,

for example, 2000nm, both layers can be connected well to each other through serial contact holes having two relatively small diameters while avoiding the technical difficulty of connecting both layers to each other through one contact hole, so that an opening ratio of pixel can be increased. Further, in opening the contact hole, it is helpful to prevent punchthrough in etching.

The capacitive line 300 is made of, for example, a conductive film containing metal or alloy, and serves as a capacitor electrode on the fixed potential side. The capacitive line 300 is formed overlapping an area for forming the scanning line 330a from a plan view, as shown in FIG. 2. More specifically, the capacitive line 300 has a main line portion extending along the scanning line 330a, a protruding portion protruded upwardly in the Y direction along the data line 6a from a portion intersecting the data line 6a and a constricted portion where the portion corresponding to the contact hole 85 is slightly constricted. The protruding portion contributes to increase in the area for forming the storage capacitor 70 by using the area on the scanning line 330a and the area below the data line 6a.

Further, the capacitive line 300 is made of, for example, single metal, alloy, metal silicide, poly-silicide or laminated layer thereof, containing at least one of metals having high melting point such as Ti, Cr, W, Ta, Mo, and in addition to the function as a capacitor electrode on the fixed potential side of the storage capacitor 70, the capacitive line 300 has a function as a light-shielding layer for shielding the TFT 30 from the incident light on the upper side of the TFT 30. However, the capacitive line 300 may have a multi-layer structure in which a first film made of a conductive poly-silicon film and the like and a second film made of a metal silicide film containing metal and the like having high melting point are stacked.

Furthermore, preferably, the capacitive line 300 extends from the image display

area in which the pixel electrodes 9a are arranged to peripheries thereof, and is electrically connected to a potentiostatic source to be a fixed potential. Such potentiostatic source may be a potentiostatic source such as a plus power source or a minus power source supplied to a data line driving circuit to be explained later, or may be a potentiostatic source supplied to the opposing electrode 21 of the opposing substrate 20.

A dielectric film 75, as shown in FIG. 3, is constructed of a silicon oxide film such as a HTO (High Temperature Oxide) film or a LTO (Low Temperature Oxide) film having, for example, a relatively thin thickness of about 5~200nm, or a silicon nitride film. From the point of view of increasing the capacitance of the storage capacitor 70, the dielectric film 75 should be preferably as thin as possible as long as the reliability of the film is sufficiently maintained.

In FIGs. 2 and 3, in addition, the lower side of the TFT 30 is provided with a lower light-shielding film 11a. The lower light-shielding film 11a is patterned in a lattice shape, and as a result, the opening area of each pixel is defined. Further, the opening area may be defined by the intersection of the data line 6a extending in the Y direction in FIG. 2 and the capacitive line 300 extending in the X direction in FIG. 2. Furthermore, similar to the case of the above-described capacitive line 300, the lower light-shielding film 11a may be formed extending from the image display area to the peripheries thereof to be connected to a potentiostatic source so that the potential variation has no adverse effects on the TFT 30.

Further, a base insulating film 12 is provided below the TFT 30. In addition to the function for insulating the TFT 30 from the lower light-shielding film 11a, since the base insulating film 12 is formed on the whole surface of the TFT array substrate 10, the base insulating film 12 has a function for preventing the characteristic variation of the TFT 30 for pixel switching caused by rough polished surface of the TFT array substrate 10 or

contaminants left after washing.

In addition, a first interlayer insulating film 41 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 83 communicating with the high-concentrating drain area 1e, respectively, is formed on the scanning line 330a.

The junction layer 71 and the capacitive line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 which has a contact hole 81 communicating with the high-concentration source area 1d and a contact hole 85 communicating with the junction layer 71 are formed respectively on the junction layer 71 and the capacitive line 300.

Furthermore, in the present embodiment, by baking the first interlayer insulating film 41 at about 1000°C, activation of ions injected into the poly-silicon film constituting the semiconductor layer 1a or the scanning line 330a may be intended. On the other hand, by not baking the second interlayer insulating film 42, relief of stress occurring in the vicinity of the interface of the capacitive line 300 may be intended.

The data line 6a is formed on the second interlayer insulating film 42, and above them a third interlayer insulating film 43 which has a contact hole 85 communicating the junction layer 71 is formed.

The surface of the third interlayer insulating film 43 is leveled by means of CMP (Chemical Mechanical Polishing) process, and as a result, the orientation failure of the liquid crystal layer 50 caused by a step generated by various wirings or elements below the third interlayer insulating layer 73 can be reduced.

However, in place of performing the leveling process for the third interlayer insulating film 43, or in addition to it, a groove, in at least one of the TFT array substrate 10, the base insulating film 12, the first interlayer insulating film 41 or the second

interlayer insulating film 42, can be formed to buried the wirings such as the data line 6a or the TFT 30 for performing the leveling process.

According to the electro-optical device of the present embodiment as constructed like the above, since the scanning line 330a has the broad width portion 331a and the narrow width portion 332a and the broad width portion 331a is formed to face the channel area 1a' of the TFT 30, the arrangement between the TFT 30 and the scanning line 330a can be easily adjusted or determined.

For example, the arrangement between the TFTs 30 and the scanning lines 330a in FIG. 2 described above shows an example of a suitable arrangement responsive to the requirement for effectively preventing light from entering the channel areas 1a' of the TFTs 30. In addition, for example, the arrangements shown in FIGs. 5 and 6 can be implemented. FIG. 5 is a diagram with the same purpose as FIG. 2, in which an arrangement of the scanning lines and the TFTs is different from that in FIG. 2, and FIG. 6 illustrates only a shape pattern of the scanning lines shown in FIG. 5, similar to FIG. 4.

In FIGs. 5 and 6, the scanning lines 330a', more specifically, the narrow width portions 332a' are formed at positions deviated from the center of a first long gap extending through a space between the adjacent pixel electrodes 9a sandwiching the scanning lines 330a' therebetween. Further, the broad width portions 331a' are formed to be protruded only upwardly in the Y direction in FIG. 5 and 6. Furthermore, the arranged positions of the channel areas 1a', that is, the arranged positions of the broad width portion 331a' are similar to those in FIG. 2.

This arrangement can improve the quality of display image. The reason thereof is as follows. That is, in the electro-optical device according to the present invention, as described above, the oriented film 16 is provided on the pixel electrodes 9a, and on the surface of the oriented film 16, unevenness due to the "height" of various elements formed

below the oriented film 16 can exist. The above-described "various elements" include the scanning lines 330a' of the present embodiment. FIG. 7 is a sectional view taken along a line B-B' in FIG. 5, in which a convex portion 501 caused by the "height" of the narrow width portion 332a' of the scanning line 330a' is formed on the oriented film 16.

When the convex portion 501 is generated, there is a possibility of further generating nonuniformity in the above-described rubbing process performed on the oriented film 16. This nonuniformity may cause the bad orientation of the liquid crystal and thus the operation failure of the electro-optical device. Therefore, conventionally, by providing the light-shielding film in the vicinity of the above-described convex portion 501, shielding of the incident light was made possible. That is, the incident light reaching the light-shielding film is reflected or absorbed by the light-shielding film and thus does not contribute to the image display.

At this time, it is important that the above-described light-shielding film should be provided while satisfying the requirements for improving the pixel opening ratio. That is, when the light-shielding film is provided only to correspond to the convex portion 501, it may unnecessarily worsen the pixel opening ratio to deteriorate the brightness of image. When the light-shielding film is provided only in a part of the convex portion 501, sufficient light-shielding cannot be accomplished and may cause the deterioration of the contrast ratio. In addition, the influence of the nonuniformity in the convex portion 501 may lead to the operation failure of the electro-optical device.

In the present embodiment, it has been paid attention to the fact that the nonuniformity are generated in the convex portion 501, more specifically, that the portion (reference numeral 501a in FIG. 7. Hereinafter, referred to as a "rubbing-up portion 501a") associated with rubbing up the convex portion 501 (that is, the direction ascending the convex portion 501) and the portion (reference numeral 501b in FIG. 7. Hereinafter,

referred to as a "rubbing-down portion 501b") associated with rubbing down the convex portion 501 (that is, the direction descending the convex portion 501), have nonuniformity different from each other.

More specifically, for example, it has been paid attention to the fact that it is more difficult to generate the nonuniformity in the rubbing-up portion 501a than in the rubbing-down portion 501b, that is, the rubbing-down portion 501b has the higher possibility of causing the bad orientation of the liquid crystal.

In the present embodiment, it is important that the narrow width portions 332a' adjacent in the direction of the scanning lines 330a' in FIG. 5 are formed at the position deviated from the center (see the two-dotted chain line in FIG. 7) between the pixel electrodes 9a. That is, by forming the narrow width portion 332a' at the position shown in FIG. 7, a vertex 501P of the convex portion 501 caused by the narrow width portion 332a' is also formed at the position deviated from the center between the adjacent pixel electrodes 9a. This means that it is possible to construct only almost half of the sloping surface of the convex portion 501 on the area corresponding to the first gap, that is, the rubbing-down portion 501b on the area. Further, in this case, as shown in FIG. 7, by providing the light-shielding capacitive line 300 and the junction layer 71 corresponding to the space between the adjacent pixel electrodes 9a, it is possible to effectively shield only the rubbing-down portion 501b, that is, to effectively shield the corresponding portion of the convex portion 501 expected to be most influenced by the nonuniformity.

As a result, according to the present embodiment, since the operation failure of the electro-optical device caused by the nonuniformity can be substantially prevented, and since the rubbing-up portion 501a of the convex portion 501 is not expected to be influenced by the nonuniformity remains to transmit the light contributing to the image display, it is possible to improve the pixel opening ratio, that is, to maintain the bright

image. Consequently, according to the present embodiment, from the above-described point of view, an improvement in the quality of the display image can be obtained.

Further, by forming the narrow width portion 332a' at the position deviated from the center of the first gap, it is possible to improve the degree of freedom in the design of the electro-optical device and to effectively prevent the light from entering the TFT 30. The reason thereof is as follows.

That is, although the narrow width portion 332a' in the present embodiment extends through the first gap between the adjacent pixel electrodes 9a, it does not exist at the center thereof. For this reason, for example, by using an area not provided with the narrow width portion 332a' in the first gap, other wirings such as the capacitive line 300 made of the same film as the narrow width portion 332a' can be formed parallel to the narrow width portion 332a' from a plan view. That is, the degree of freedom in design can be increased.

Further, in the above-described case, although the narrow width portion 332a' is deviated from the center line, by adjusting the width of the broad width portion 331a', for example, by broadening only one side thereof or by broadening one side thereof more than the other side, it is possible to arrange the broad width portion 331a' as the gate electrode at the center of the gap. In the present embodiment, as shown in FIGs. 5 and 6, it can be understood that the broad width portion 331a' is broadened toward only one side. Hence, since the gate electrode can be arranged at a position advantageous for improving the light-shielding ability irregardless of the position of the scanning line 330a', or since the scanning line 330a' can be arranged at an arbitrary position in the gap while arranging the gate electrode at a position advantageous for improving the light-shielding ability, it is possible to increase the degree of freedom in an arrangement of wirings such as an arrangement of the scanning line 330a' and to obtain the TFT 30 originally having a

substantially high light-shielding ability.

In short, in the embodiment shown in FIGs. 5 and 6, while satisfying the requirements for improving the quality of the display image, improving the degree of freedom in design and decreasing the light leak current in the TFT 30, it is possible to adequately adjust/determine the arrangement between the channel area 1a' (or the TFT 30) and the gate electrode (or the scanning line 330).

As described above, according to the electro-optical device of the present embodiment, since the scanning line, as the gate electrode, has the broad width portion and the narrow width portion, while satisfying the above various requirements or a general requirement such as high precision of the electro-optical device itself, it is possible to adequately adjust/determine the arrangement between the channel area (or the TFT) and the gate electrode (or the scanning line).

(Second embodiment)

Now, a second embodiment of the present invention will be explained with reference to FIGs. 8 to 11. FIGs. 8 and 10 are diagrams with the same purpose as FIG. 2, respectively, and illustrates another embodiment different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10 and at least a part of the scanning line is buried in the groove. FIGs. 9 and 11 are perspective views illustrating a profile of the narrow width portion of the scanning line according to the second embodiment, respectively (FIG. 9 corresponds to FIG. 8, and a section taken along a line Z1-Z1' in FIG. 8 corresponds to a section taken along a line Z1-Z1' in FIG. 9. Further, FIG. 11 corresponds to FIG. 10, and a section taken along a line Z2-Z2' in FIG. 10 corresponds to a section taken along a line Z2-Z2' in FIG. 9). Further, FIG. 12 is a sectional view taken along a line T-T' in FIG. 10. Furthermore, since the basic construction and operation, etc., of the electro-optical device of the second embodiment are similar to those of the first

embodiment, explanation about distinctive portions in the second embodiment will be mainly described below. Furthermore, the reference numerals in FIGs. 8 and 12 indicates the same elements as in FIGs. 1 to 7 referred to in the above description, when they indicates substantially equivalent elements.

First, in one aspect of the second embodiment, as shown in FIGs. 8 and 9, a groove 3G1 is formed along the scanning line in the TFT array substrate 10. The groove 3G1 is formed except for the area where the semiconductor layer 1a of the TFT 30 is formed. By this construction, in consideration of only the grooves, the grooves 3G1 are arranged in a matrix shape from a plan view (see FIG. 8). Further, a scanning line 340a is formed such that the narrow width portion 342a thereof is entirely buried in the groove 3G1 (see FIG. 9).

In another aspect of the second embodiment, as shown in FIGs. 10 and 11, a groove 3G2 is formed on the TFT array substrate 10, similarly to the groove 3G1. However, preferably, a groove 3G2 is formed slightly narrower than the groove 3G1. Further, a narrow width portion 352a of the scanning line 350a is formed along the groove 3G2. The narrow width portion 352a has a buried portion 352aB of which a part is buried in the groove 3G2 and a non-buried portion 352aNB which is not buried in the groove 3G2 and extends parallel to the buried portion 352aB. The non-buried portion 352aB is formed on the surface of the TFT array substrate 10.

Further, in one aspect and another aspect of the second embodiment, as shown in FIGs. 8 and 10, a groove 6G1 is formed in the TFT array substrate 10 along the data line. Furthermore, the data line 6a is formed to be entirely buried in the groove 6G1. In addition, the semiconductor layer 1a is also formed to be entirely buried in the groove 6G1.

According to the electro-optical device of the second embodiment constructed as above, the following effects can be obtained. First, since the whole part or a part of both

of the scanning lines 340a and 350a are buried in the grooves 3G1 or 3G2, as shown in FIGs. 9 and 11, in this buried portion, the surface height of the base insulating film 12 and the height of the buried portion 352aB of the scanning line 340a and the scanning line 350a are almost equal to each other to maintain the leveling feature. By this, the leveling feature of the first to third interlayer insulating film 41 to 43 formed as the upper layers of the scanning lines 340a and 350a, or the pixel electrode 9a and the oriented film 16 can be well obtained. Therefore, in the second embodiment, for example, since a step along the narrow width portion 342a or the buried portion 352aB does not substantially appear on the surface of the oriented film 16, the rubbing process can be very suitably performed on the oriented film 16 and the bad orientation can be drastically prevented. Furthermore, an effect can be obtained that the light leakage caused by the bad orientation and deterioration of the image quality based on the light leakage.

Such effects on the portion along the data line 6a can be obtained because of the existence of the groove 6G1.

Further, in FIGs. 10 and 11, in particular, because of the existence of the non-buried portion 352aNB, the following effects can be obtained. Now, the effects will be explained in detail.

First, in the electro-optical device of the present embodiment, generally in order to prevent deterioration of the electro-optical material caused by the application of DC voltage and to prevent the cross talk or flicker in the displayed image, an inverse driving method of inversing the polarities of voltages applied to the respective pixel electrodes 9a in a predetermined rule may be employed. More specifically, so-called "1H inverse driving method" will be explained.

First, as shown in FIG. 13(a), during the time for displaying image signals for the n-th field (n is a natural number) or frame, the polarity of the liquid crystal driving voltage

indicated by + or - for each pixel electrode 9a is driven with the same polarity for every row. Thereafter, as shown in FIG. 13(b), when the image signals for the n+1-th field or frame are displayed, the polarity of the liquid crystal driving voltage for each pixel electrode 9a is inversed and during the time for displaying the image signal of the n+1th field or one frame, the polarity of the liquid crystal driving voltage indicated by + or - for each pixel electrode 9a is not inversed, and each pixel electrode is driven with the same polarity for every row. Then, the state shown in FIG. 13(a) and 13(b) is repeated at the period of one field or one frame. This is the 1H inverse driving method. As a result, while avoiding deterioration of the liquid crystal caused by the application of DC voltage, it is possible to prevent image display with reduced cross talk or flicker. Further, the 1H inverse driving method is more advantageous than the 1S inverse driving method to be explained later, in that there is no almost cross talk in the vertical direction (Y direction) in the drawing.

However, as can be understood from FIG. 13(a) and FIG. 13(b), in the 1H inverse driving method, a horizontal electric field takes place between the pixel electrodes 9a adjacent to each other in the vertical direction (Y direction) in the drawing. In these drawings, an area C1 where the horizontal electric field takes place is always in the vicinity of the gap between the pixel electrodes adjacent to each other in the Y direction. If such horizontal electric field is applied, for the electro-optical material to which a vertical electric field, i.e., an electric field perpendicular to the surface of the substrate, is applied, between the pixel electrode and the opposing electrode facing each other, the operation failure can be caused by the bad orientation of the liquid crystal in the electro-optical material and by the light leakage in the portion, which leads to a problem of decreasing the contrast ratio.

With respect to the above, the area where the horizontal electric field is generated

can be covered by the light-shielding film. However, in this case, there is a problem that the opening area of pixels becomes narrow in respect to the area where the horizontal electric field is generated. In particular, as the distance between the adjacent pixel electrodes becomes small due to minuteness of the pixel pitch, such horizontal electric field increases, and thus this poses a serious problem in higher precision electro-optical device.

In the aspect shown in FIGs. 10 and 11 of the second embodiment, a step caused by the height of the non-buried portion 352aNB is formed between the pixel electrodes 9a (that is, the adjacent pixel electrodes 9a to which voltage of inverse polarity is applied) adjacent to each other in the vertical direction. Because of the existence of this step, it is possible to intensify the vertical electric field in the vicinity of an edge portion of the pixel electrode 9a arranged on the step and to weaken the horizontal electric field. More specifically, as shown in FIG. 12, the distance between the vicinity of the edge portion of the pixel electrode 9a arranged on the step 430 and the opposing electrode 21 becomes narrower by the height of the step 430. Therefore, in the area C1 where the horizontal electric field is generated, the vertical electric field between the pixel electrode 9a and the opposing electrode 21 can be intensified. Furthermore, in FIG. 12, since the gap between the adjacent pixel electrodes 9a is constant, the intensity of the horizontal electric field to be intensified with the gap getting narrow is constant. Therefore, by making the vertical electric field more prevalent in the area C1 where the horizontal electric field is generated, it is possible to prevent the bad orientation of the liquid crystal caused by the horizontal electric field. Furthermore, because of the step 430 made of the insulating film, the intensity of the horizontal electric field is weakened, and the portion of the liquid crystal affected by the horizontal electric field is decreased by the amount of replacing the step where the horizontal electric field exists. Therefore, the influence of the horizontal

electric field on the liquid crystal layer 50 can be reduced.

Further, in the above description, the 1H inverse driving method has been explained but the present invention is not limited to such driving method. For example, 1S inverse driving method of inversing the voltage polarity at a period of a frame or a field for each column while driving pixel electrodes in a column with the potential of the same voltage polarity may be employed in the present invention as the inverse driving method of which control is relatively easy and which enables the high quality image display. Furthermore, between the pixel electrodes adjacent to each other in both of the column direction and the row direction, the dot inverse driving method of inversing the voltage polarity applied to each pixel electrode has been developed and can be applied to the present invention.

Further, in the second embodiment, as shown in FIG. 2, the aspect in which the narrow width portion 342a and 352a is formed to extend through the center of the first gap between the adjacent pixel electrodes 9a has been explained. However, the present invention is not limited to such construction. That is, as shown in FIGs. 5 and 6, in the aspect where the narrow width portion is formed to extend at the position deviated from the center of the first gap, the grooves 3G1 or 3G2 shown in FIGs. 8 to 11 may be comprised in a combination. For example, the construction shown in FIGs. 14 and 15 may be employed. FIG. 14 is a view with the same purpose as FIG. 2 and illustrates another aspect different from that in FIG. 2 in that a groove is formed on the TFT array substrate 10, and the narrow width portion of the scanning line is deviated from the center of the first gap, and FIG. 15 is a sectional view taken along a line T-T' in FIG. 14.

FIG. 14 is similar to FIGs. 5 and 6 in that a narrow width portion 362a of a scanning line 360a is deviated from the center of the long first gap extending through the space between the adjacent pixel electrodes 9a, but FIG. 14 is different from FIGs. 5 and 6

in that the narrow width portion 362a is formed along a groove 3G1' formed on the TFT array substrate 10 and a broad width portion 361a is formed to protrud only downwardly in FIG. 14. In this construction, the narrow width portion 362a of the scanning line 360a is formed from the upper portion in the drawing as seen from the center of the first gap and thus the narrow width portion 362a is formed to be positioned right below the contact hole 85 for connecting the pixel electrode 9a and the junction layer 71. Further, the narrow width portion 362a is formed to be entirely buried in the groove 3G1'.

According to this construction, as shown in FIG. 15, the contact hole 85 is formed on the scanning line 360a formed to be buried in the groove 3G1'. In other words, it is possible to form the contact hole 85 on the assumption that the step caused by the height of the scanning line 360a does not substantially appear on the surface of the third interlayer insulating film 43.

In such construction shown in FIGs. 14 and 15, in particular, an advantage from the contact hole 85 which can be easily and securely formed can be obtained. That is, assuming that a step due to the height of the scanning line or the narrow width portion is generated on the surface of the third interlayer insulating film 43, there is a possibility of a disadvantage in that the contact hole 85 may be formed on the vertex or on the ridge of the step. The present construction overcomes such drawback.

The above effects can be understood from the following point of view. That is, in the second embodiment, since the whole or a part of the scanning line is buried in the groove, and thus a step due to the height of the scanning line does not substantially appear on the surface of the respective interlayer insulating film, the formation position or the extending position of the scanning line need not be considered particularly. In other words, if the scanning line is between the adjacent pixel electrodes in the direction thereof, the scanning line may be formed at any position. This is because even when the

formation position or extending position of the scanning line is selected freely and the contact hole is formed thereon, as described above, the contact hole can be relatively easily and securely formed due to the absence of the step.

Further, in case the narrow width portion has both the buried portion and the non-buried portion, it is preferable to form the groove such that the buried portion is positioned right below the contact hole 85. FIG. 12 corresponds to an example of such construction.

(Third embodiment)

Now, a third embodiment of the present invention will be explained with reference to FIGs. 16 to 19. FIG. 16 is a diagram with the same purpose as FIG. 2 and illustrates another aspect that a shape of the data line is different from that in FIG. 2. FIG. 17 is a sectional view taken along a line P-P' in FIG. 16, FIG. 18 is a sectional view taken along a line Q-Q' in FIG. 16, and FIG. 19 is a sectional view taken along a line R-R' in FIG. 16. Further, since the basic construction and operation of the electro-optical device of the third embodiment are similar to those of the first embodiment, explanation about distinguishing features of the third embodiment will be mainly described below. Furthermore, reference numerals in FIGs. 16 to 19 indicate the same elements as in FIGs. 1 to 15 referred to in the above description, when they indicates substantially equivalent elements.

In the third embodiment, as shown in FIGs. 16 to 19, a data line 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad. Further, a width W1 of a portion extending along the data line 6a1 in the capacitive line 300, that is, the protruded portion 302, first, is broader than a width W2' of the portions except for the broad width portion 6aW in the data line 6a1 (in particular, see FIG. 17). Second, the width W1 of the protruded portion 302 is almost equal to a width W6 of the broad width portion 6aW in the data line 6a1 (see FIG. 18). The channel area

1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width direction 6aW and almost at the center in the width direction of the scanning line 3a. Furthermore, in the third embodiment, as shown in FIGs. 16, 18 and 19, the broad width portion 6aW of the data line 6a1 is formed continuously from the portion overlapping the TFT 30 to the portion in which the contact hole 81 for connecting the semiconductor layer 1a of the TFT and the data line 6a is provided, for each TFT 30 arranged in a matrix shape. In addition, in the third embodiment, as shown in FIGs. 17 to 19, the light-shielding film 23 is formed on the opposing substrate 20. A width WS of one-by-one lattice of the light-shielding film 23 is greater than that of the broad width portion 6aW.

In the electro-optical device of the third embodiment constructed like the above, the following effects can be obtained. That is, first, since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 which is formed broad exist on the TFT 30, so called a double light-shielding effect can be obtained. Therefore, it is difficult for the light to enter the channel area 1a' of the TFT 30, and thus the light leak current can be minimized.

In particular, in the third embodiment, the broad width portion 6aW of the data line 6a also exists on the TFT 30 while overlapping the capacitive line 300. In this case, on the TFT 30, the light-shielding ability corresponding to the integrated value of their transmittances can be obtained. Further, since the channel area 1a' of the semiconductor layer 1a is positioned almost at the center in the width direction of the broad width portion 6aW and almost at the center in the width direction of the scanning line 3a, the light-shielding ability can be enhanced.

Second, in connection with such excellent light-shielding ability, in the third embodiment, as described above, the width W1 of the protruded portion 302 of the

capacitive line 300 and the width W6 of the broad width portion 6aW of the data line 6a are less than the width WS of the light-shielding film 23 on the opposing substrate 20 (that is, WS>W1, WS>W6). According to this, the light entered from the upper portion of the TFT 30 is first shielded by the light-shielding film 23 and is further shielded by the broad width portion 6aW of the data line 6a. Furthermore, although passing through the broad width portion 6aW, the incident light is next shielded by the protruded portion 302 of the capacitive line 300. In short, in the third embodiment, since triple light-shielding is implemented, it becomes more difficult for the light to enter the TFT 30.

Third, in the third embodiment, the broad width portion 6aW of the data line 6a is formed continuously from the portion overlapping the TFT 30 to the contact hole 81 for each TFT 30 arranged in a matrix shape. Since the contact hole 81 is provided for connecting the semiconductor layer 1a of the TFT 30 and the data line 6a as described above, the capacitive line 300 cannot be formed in the portion. However, in the third embodiment, in the formation position of the contact hole 81, the broad width portion 6aW of the data line 6a exists similarly to the upper portion of the TFT 30. Therefore, deterioration of the light-shielding ability caused by the absence of the capacitive line 300 can be compensated by the existence of the broad width portion 6aW. In this connection, as in the third embodiment, according to the aspect that the broad width portion 6a is formed continuously on the TFT 30 and on the formation position of the contact hole 81, since it is not necessary to broaden exceedingly the formation area of the broad width portion 6aW, it is preferable not to increase the inner reflection.

As described above, in the third embodiment, by means of the combination of various effects, the possibility of the light incidence to the channel area 1a' is drastically decreased, and the generation of the light leak current in the TFT 30 and consequently the generation of the flicker and the like on the image due to the light leak current can be

effectively suppressed.

(The whole construction of the electro-optical device)

The whole construction of the electro-optical device according to the present embodiment constructed like the above will be explained with reference to FIGs. 20 and 21. Further, FIG. 20 is a plan view of the TFT array substrate along with the respective elements formed thereon seen from the opposing substrate 20 side, and FIG. 21 is a sectional view taken along a line H-H' in FIG. 20.

In FIGs. 20 and 21, in the electro-optical device according to the present embodiment, the TFT array substrate 10 and the opposing substrate 20 are arranged opposite to each other. A liquid crystal layer 50 is inserted and sealed between the TFT array substrate 10 and the opposing substrate 20 and the TFT array substrate 10 and the opposing substrate 20 are affixed to each other by means of a sealing material 52 provided in the sealing area positioned around the image display area 10a.

In the outer area of the sealing material 52, a data line drive circuit 101 for driving the data line 6a by supplying image signals to the data line 6a at a predetermined timing, and the external circuit connecting terminals 102 are provided along one side of the TFT array substrate 10, and scanning line drive circuits 104 for driving the scanning line 3a by supplying scan signals to the scanning line 3a at a predetermined timing is provided along two sides adjacent to the one side.

Further, if delay of the scan signals supplied to the scanning line 3a does not matter, the scanning line drive circuit 104 on only one side is sufficient. Furthermore, the data line drive circuit 101 may be arranged on both sides along the sides of the image display area 10a.

The remaining one side of the TFT array substrate 10 is provided with a plurality of wirings 105 for connection between the scanning line drive circuits 104 provided on

both sides of the image display area 10a. Further, at least one corner of the opposing substrate 20 is provided with a conductive material 106 for electrical connection between the TFT array substrate 10 and the opposing substrate 20. Furthermore, as shown in FIG. 21, the opposing substrate 20 having almost the same profile as the sealing material 52 shown in FIG. 20 is bonded to the TFT array substrate 10 through the sealing material 52.

In FIG. 21, after the TFTs for switching pixels, or wirings such as the scanning lines, the data lines are formed on the TFT array substrate 10, and the oriented film is formed on the pixel electrodes 9a. In addition to the opposing electrode 21, the oriented film is formed on the uppermost portion of the opposing substrate 20. Further, the liquid crystal layer 50 is composed of the liquid crystal in which, for example, one kind or several kinds of nematic liquid crystal are mixed, and is oriented in a predetermined state between a pair of oriented films.

Furthermore, on the TFT array substrate 10, in addition to the data line drive circuit 101 and the scanning line drive circuit 104, a sampling circuit for applying image signals to the plurality of data lines 6a at a predetermined timing, a precharge circuit for supplying a precharge signal of a predetermined voltage level to the plurality of data lines prior to the image signals, an inspection circuit for inspecting the quality or defects of the electro-optical device during production thereof or in shipping thereof and the like may be formed.

(Embodiment of electronic apparatus)

Next, for an embodiment of a color display device of a projection type that is an example of an equipment using the above-described electro-optical device as a light bulb, the whole construction thereof, in particular, the optical construction thereof will be explained. Here, FIG. 22 is a diagrammatic sectional view of the color display device of a projection type.

In FIG. 22, a liquid crystal projector 1100 that is an example of the color display device of a projection type in the present embodiment comprises three liquid crystal modules including the liquid crystal device in which the drive circuit is mounted on the TFT array substrate, and further comprises the respective light bulbs 100R, 100G and 100B for RGB. In the liquid crystal projector 1100, when transmitted light is emitted from a lamp unit of white light source such as a metal halide lamp, the light is divided into the light components R, G and B corresponding to the three primary colors RGB by means of three mirrors 1106 and two dichroic mirrors 1108 and guided to the light bulbs 100R, 100G and 100B corresponding to the respective colors, respectively. At this time, in particular, in order to prevent the light loss caused by the long light path, the B light is guided through a relay lens system 1121 composed of an incident lens 1122, a relay lens 1123 and an exit lens 1124. Then, the light components corresponding to the three primary colors modulated, respectively, by the light bulbs 100R, 100G and 100B are synthesized again by a dichroic prism 1112, and then are projected as a color image to a screen 1120 through a projecting lens 1114.

The present invention is not limited to the above-described embodiments but may be appropriately varied without departing from the gist or the spirit of the invention known throughout the claims and the specification. The electro-optical devices including such variation, for example, an electrophoresis apparatus or an electro-luminescence display device, or the electronic apparatus including these electro-optical devices are also included in the technical range of the present invention.

What is claimed is:

1. An electro-optical device comprising, above a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction intersecting the scanning lines, thin-film transistors formed correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes formed correspondingly to the thin-film transistors,

wherein the respective scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

2. The electro-optical device according to claim 1, wherein the broad width portion has a portion lengthened from the narrow width portion.

3. The electro-optical device according to claim 1, wherein the broad width portion has a portion connected to the narrow width portion.

4. The electro-optical device according to claim 1, wherein the respective scanning line extends in a direction intersecting a direction in which the channel area extends, and the broad width portion extends in a single direction or bi-direction in which the channel area extends.

5. The electro-optical device according to claim 1, wherein the pixel electrode is arranged in a matrix shape, and

wherein the respective channel area is formed in an intersecting area in which a first long gap extending through a space between the pixel electrodes sandwiching the scanning line and being adjacent to each other and a second long gap extending through a space between the pixel electrodes sandwiching the data line and being adjacent to each other, are intersected.

6. The electro-optical device according to claim 5, wherein the narrow width portion is formed at a position deviated from a center of the first gap, and

the broad width portion is formed at the center of the first gap in the intersecting area.

7. The electro-optical device according to claim 6, wherein the broad width portion is formed at a center of the second gap in the intersecting area.

8. The electro-optical device according to claim 1, wherein grooves are formed in the substrate along the scanning lines and the scanning lines are buried at least partially in the grooves directly or through an interlayer insulating film.

9. The electro-optical device according to claim 8, wherein the narrow width portion has a buried portion buried in the groove and extending along the scanning line and a non-buried portion non-buried in the groove and extending along the scanning line in parallel to the buried portion, and

a base of the pixel electrode is positioned high along the scanning line due to the non-buried portion.

10. The electro-optical device according to claim 1, further comprising a capacitive line having a capacitor electrode on a pixel potential side connected to the pixel electrode for constructing a storage capacitor and a capacitor electrode on a fixed potential side opposing the capacitor electrode on the pixel potential side through a dielectric film for constituting the storage capacitor,

wherein the capacitive line has a main line portion extending along the scanning line and a portion extending along the data line, and

a width of the portion extending along the data line in the capacitive line is equal to or broader than that of the data line.

11. The electro-optical device according to claim 10, wherein a portion

overlapping the thin-film transistor in the data line is formed locally broad, and

wherein a width of the portion extending along the data line in the capacitive line is broader than that of a portion not formed broad in the data line and equal to that of the portion formed broad in the data line.

12. The electro-optical device according to claim 11, wherein the capacitive line is arranged in an overlapping portion between the thin-film transistor and the data line, and

the data line is formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

13. The electro-optical device according to claim 11, wherein, for each thin-film transistor, the data line is formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

14. The electro-optical device according to claim 10, wherein a portion overlapping the thin-film transistor in the data line is formed locally broad, and

a width of the portion extending along the data line in the capacitive line is broader than that of a portion not formed broad in the data line and narrower than that of the portion formed broad in the data line.

15. The electro-optical device according to claim 14, wherein the capacitive line is arranged in the overlapping portion between the thin-film transistor and the data line, and

the data line is formed broad in a portion in which a contact hole for connecting to the thin-film transistor is provided, in addition to the portion overlapping the thin-film transistor in the data line.

16. The electro-optical device according to claim 14, wherein for each of the

thin-film transistors, the data line is formed continuously broad from the portion overlapping the thin-film transistor to a portion in which the contact hole is formed.

17. The electro-optical device according to claim 1, further comprising another substrate opposing the substrate through an electro-optical material and a light-shielding film formed on the another substrate,

wherein widths of the data line and a portion extending along the data line in the capacitive line is narrower than that of the light-shielding film.

18. An electronic apparatus comprising an electro-optical device having, above a substrate, scanning lines extending in a predetermined direction, data lines extending in a direction of intersecting the scanning lines, thin-film transistors provided correspondingly to intersecting areas of the scanning lines and the data lines, and pixel electrodes provided correspondingly to the thin-film transistors,

wherein the respective scanning line has a broad width portion as a gate electrode in a portion opposing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.

ABSTRACT OF THE DISCLOSURE

An electro-optical device of the present invention comprising pixel electrodes, TFTs electrically connected to the pixel electrodes, and scanning lines and data lines connected to the TFTs on a TFT array substrate is disclosed. Each scanning line has a broad width portion as a gate electrode in a portion facing a channel area of the TFT and the narrow width portion.

As a result, an electro-optical device capable of easily adjusting an arrangement of the gate electrodes and the scanning lines and at the same time precisely driving the TFTs is provided.

FIG. 1

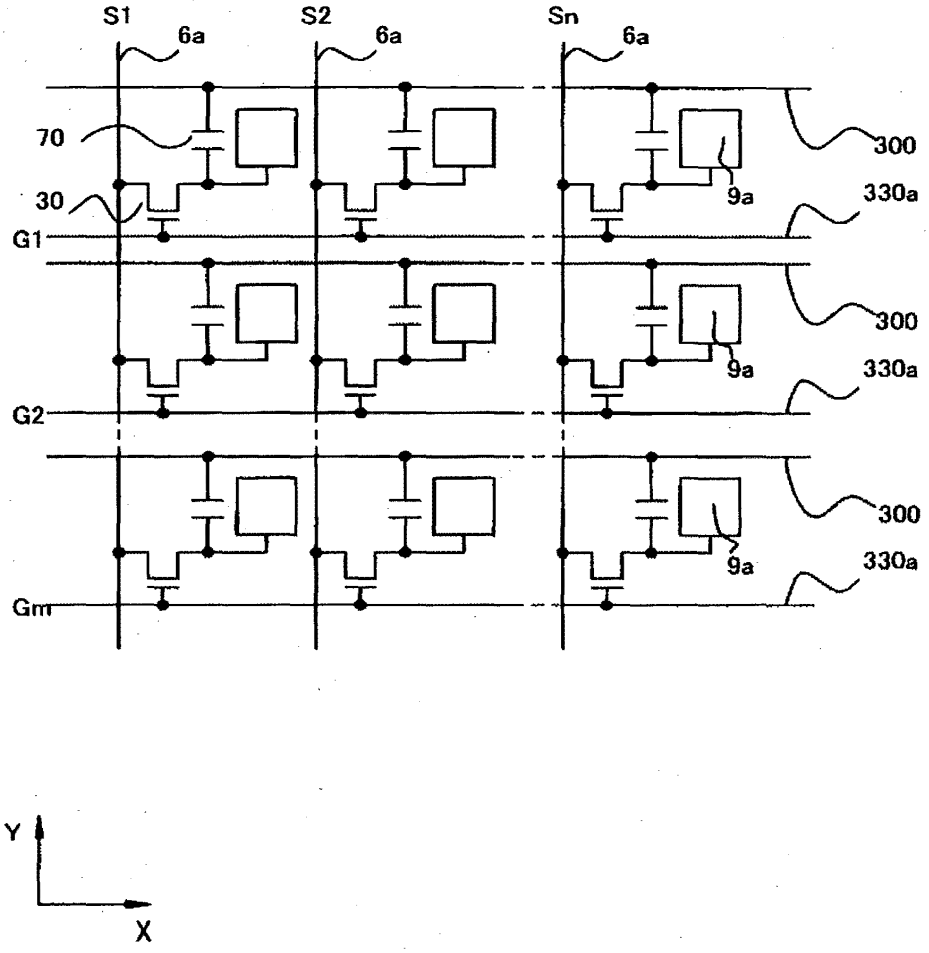

S1
6a
S2
6a
Sn
6a
70
30
G1
G2
Gm
300
9a
330a
300
9a
330a
300
9a
330a
Y
X

FIG. 2

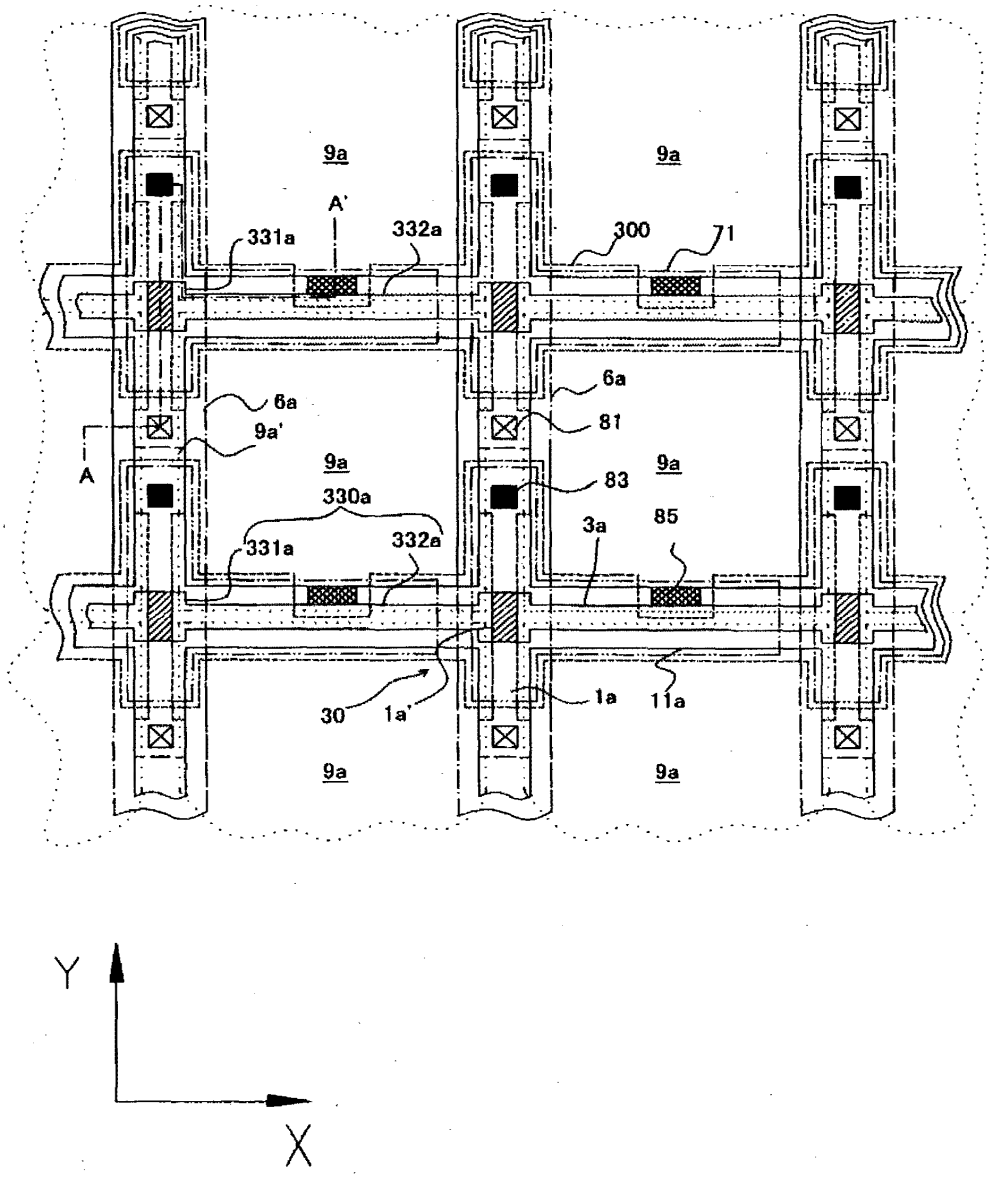

9a
9a
A'
331a
332a
300
71
6a
6a
9a'
81
A
9a
9a
330a
83
85
3a
331a
332a
30
1a'
1a
11a
9a
9a
Y
X

FIG. 3

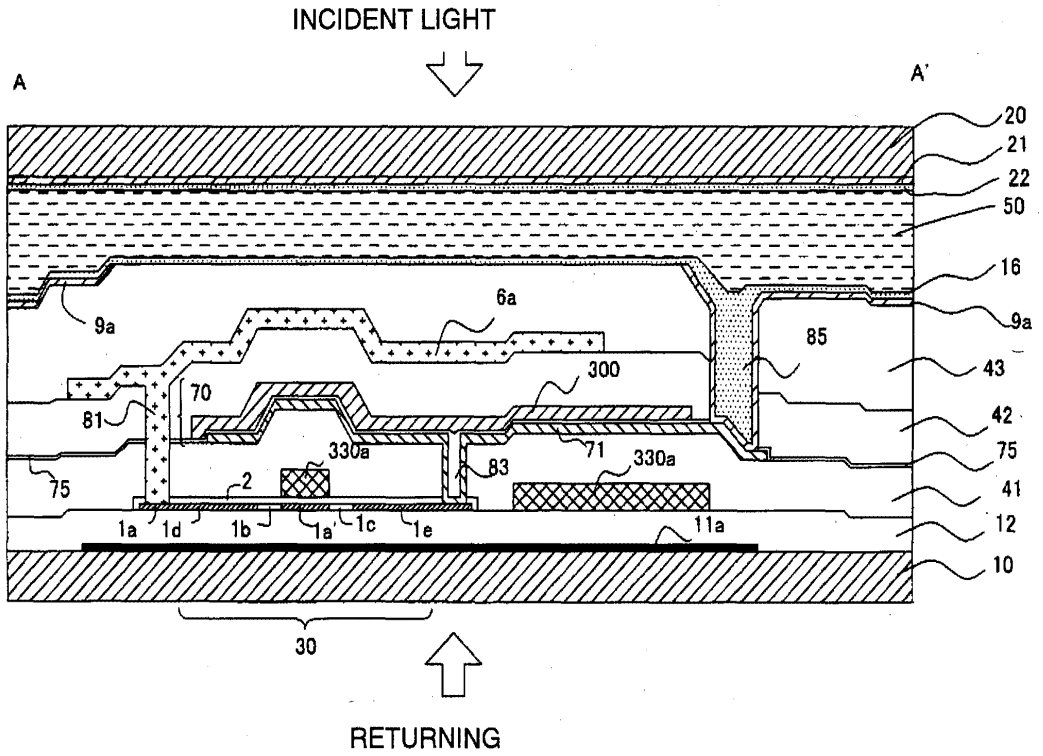

INCIDENT LIGHT
A
A'
20
21
22
50
16
9a
6a
9a
85
43
300
70
81
42
330a
71
330a
75
83
75
2
41
1a
1d
1b
1a'
1c
1e
11a
12
10
30
RETURNING

FIG. 4

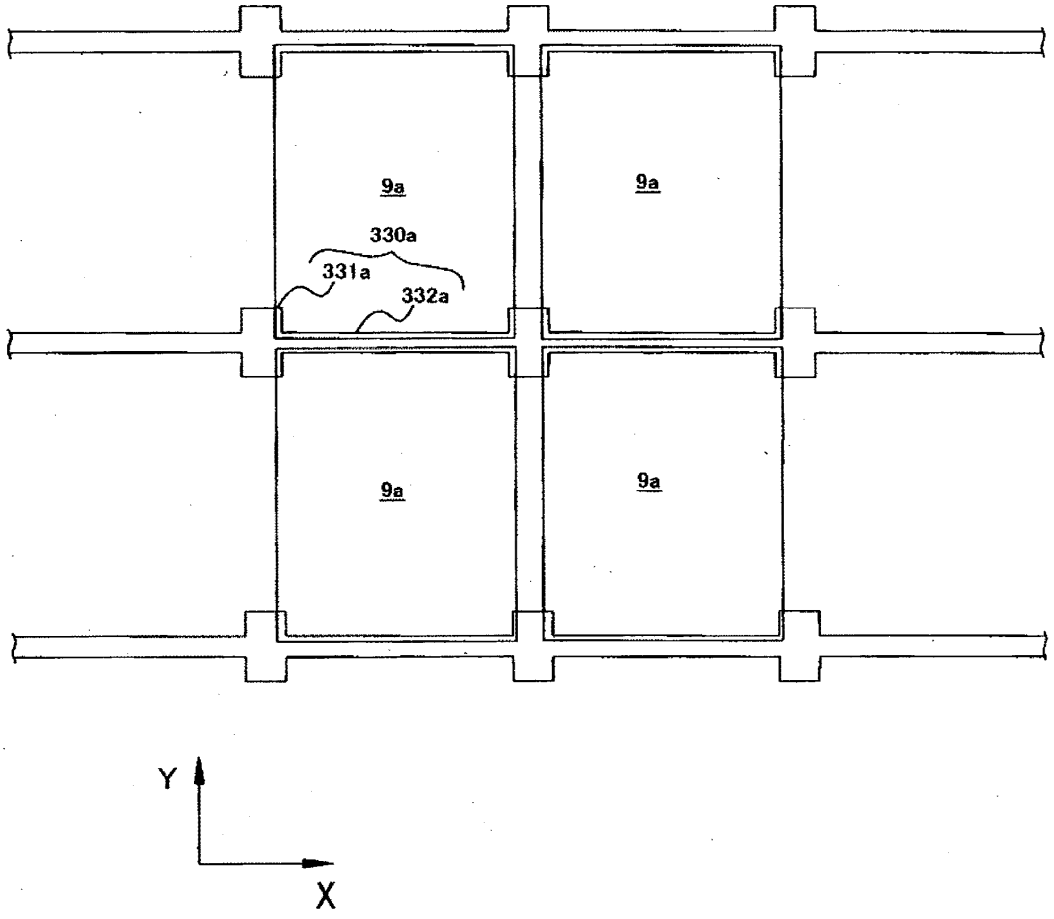


FIG. 5

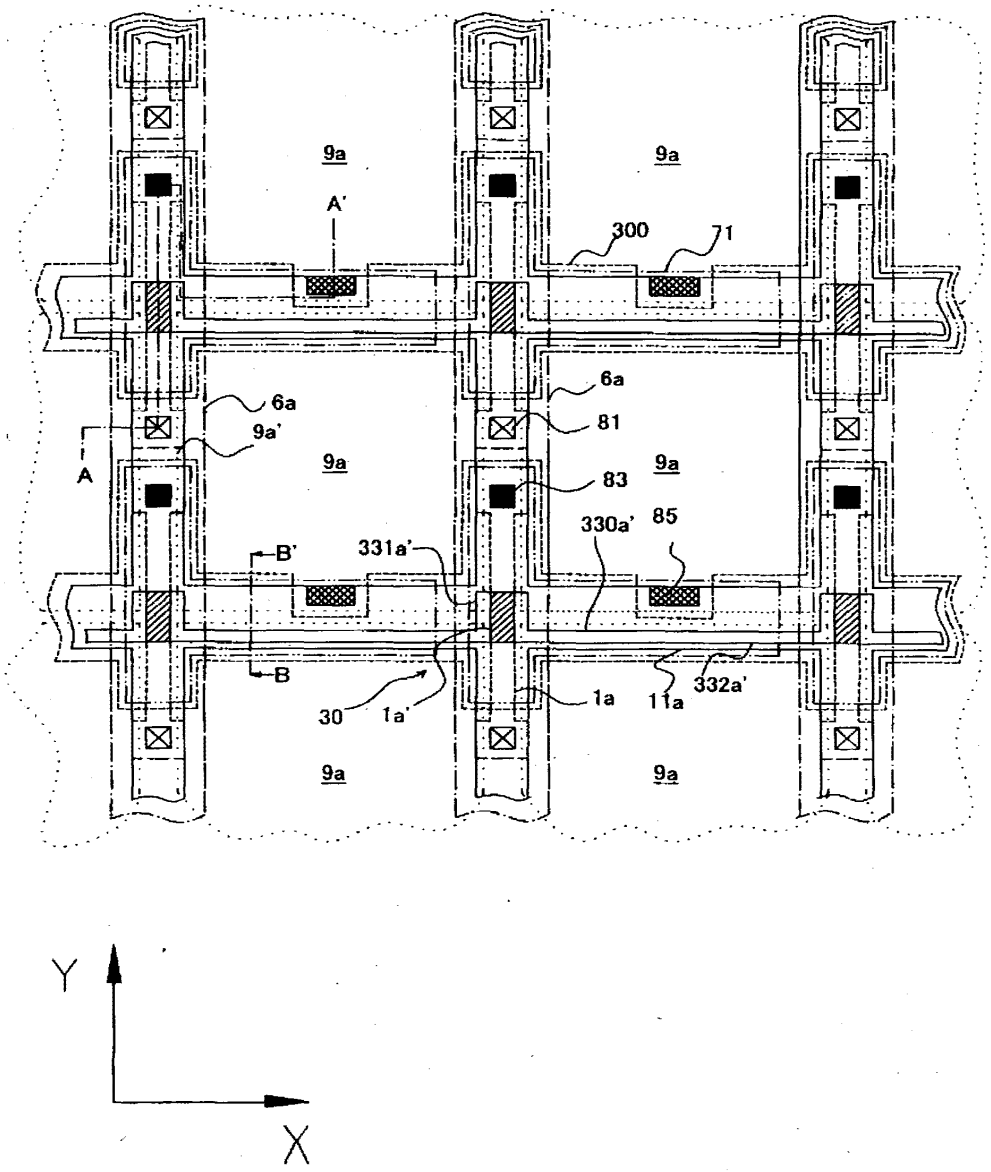


FIG. 6

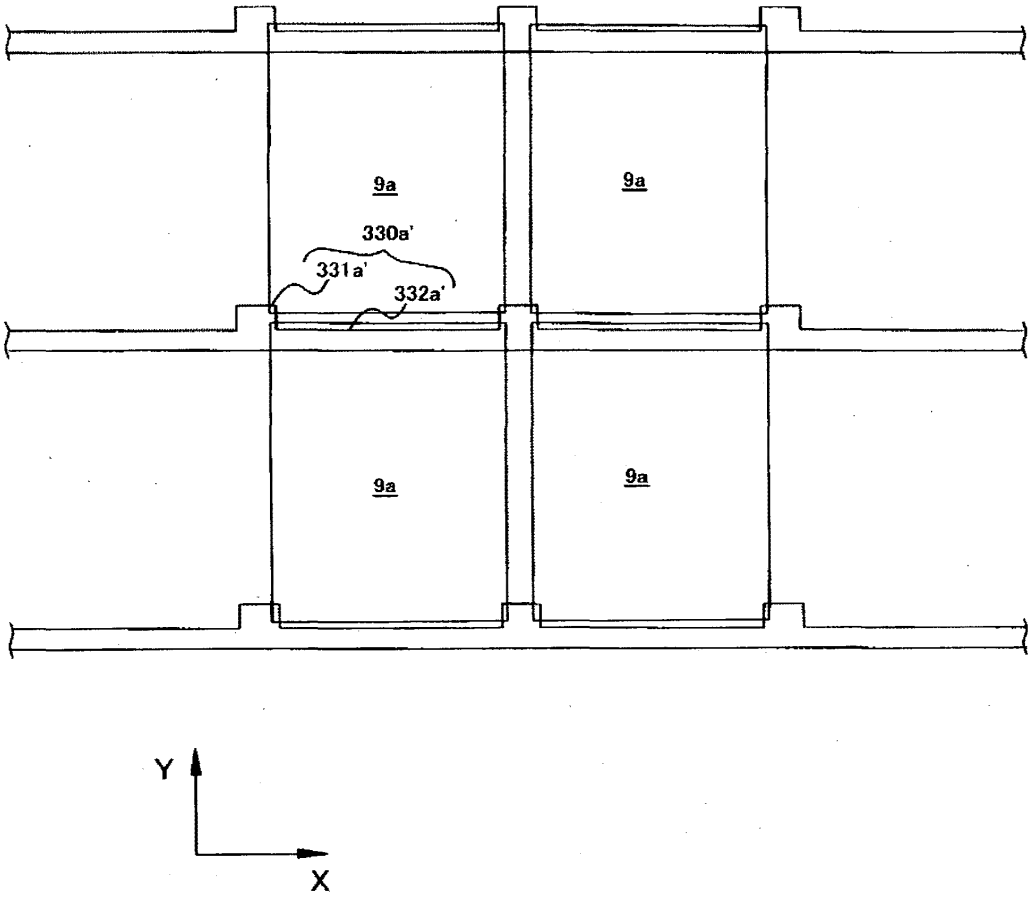


FIG. 7

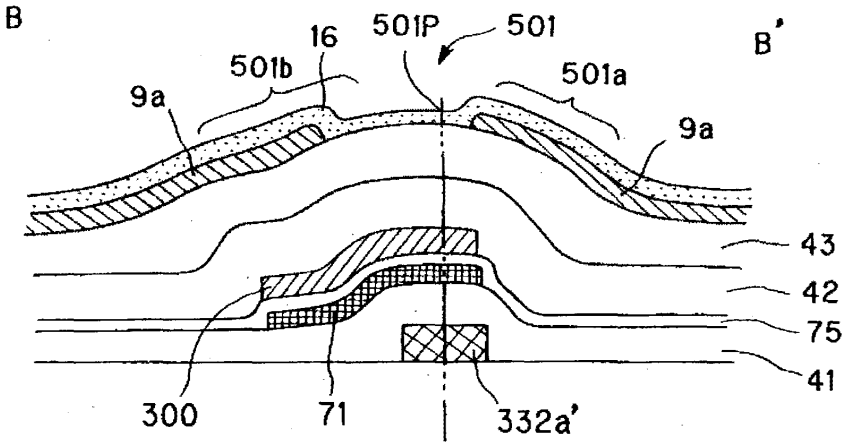


FIG. 8

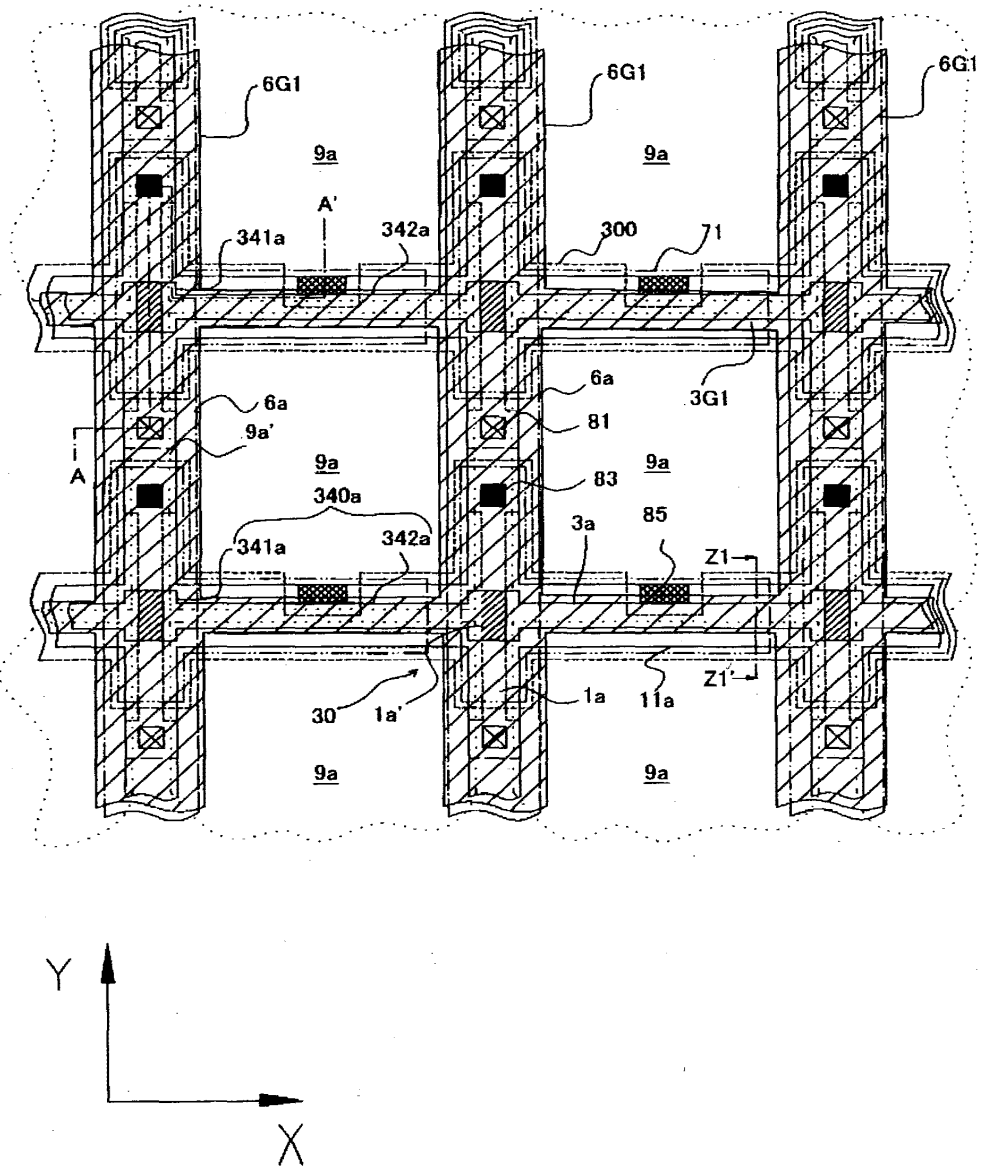

6G1
6G1
6G1
9a
9a
A'
341a
342a
300
71
6a
9a'
6a
81
3G1
A
9a
9a
340a
83
85
341a
342a
3a
Z1
Z1'
30
1a'
1a
11a
9a
9a
Y
X

FIG. 9

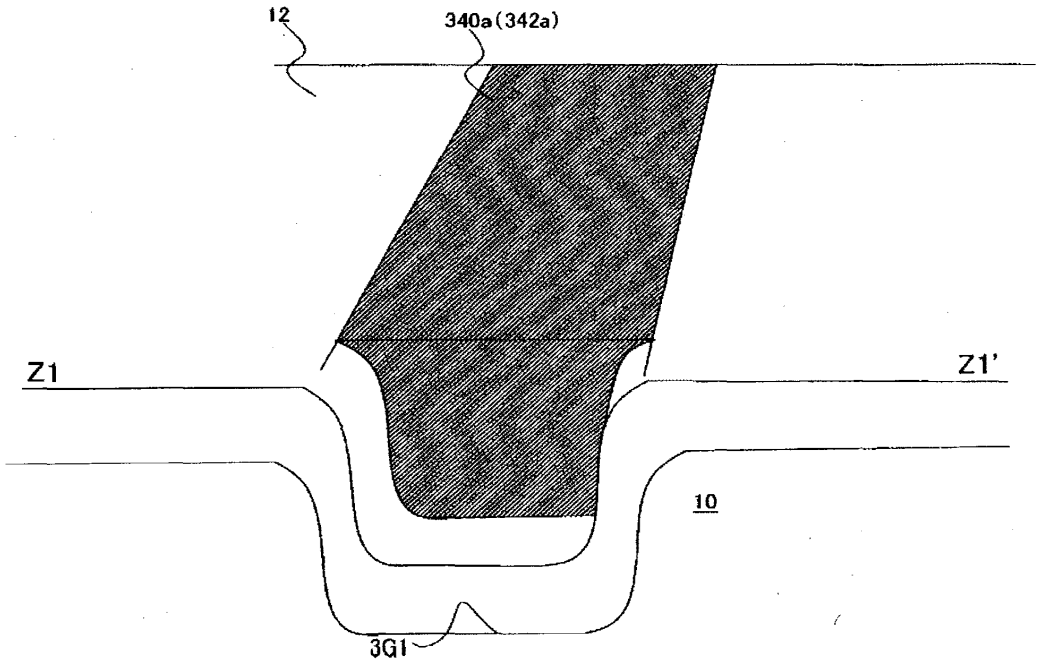


FIG. 10

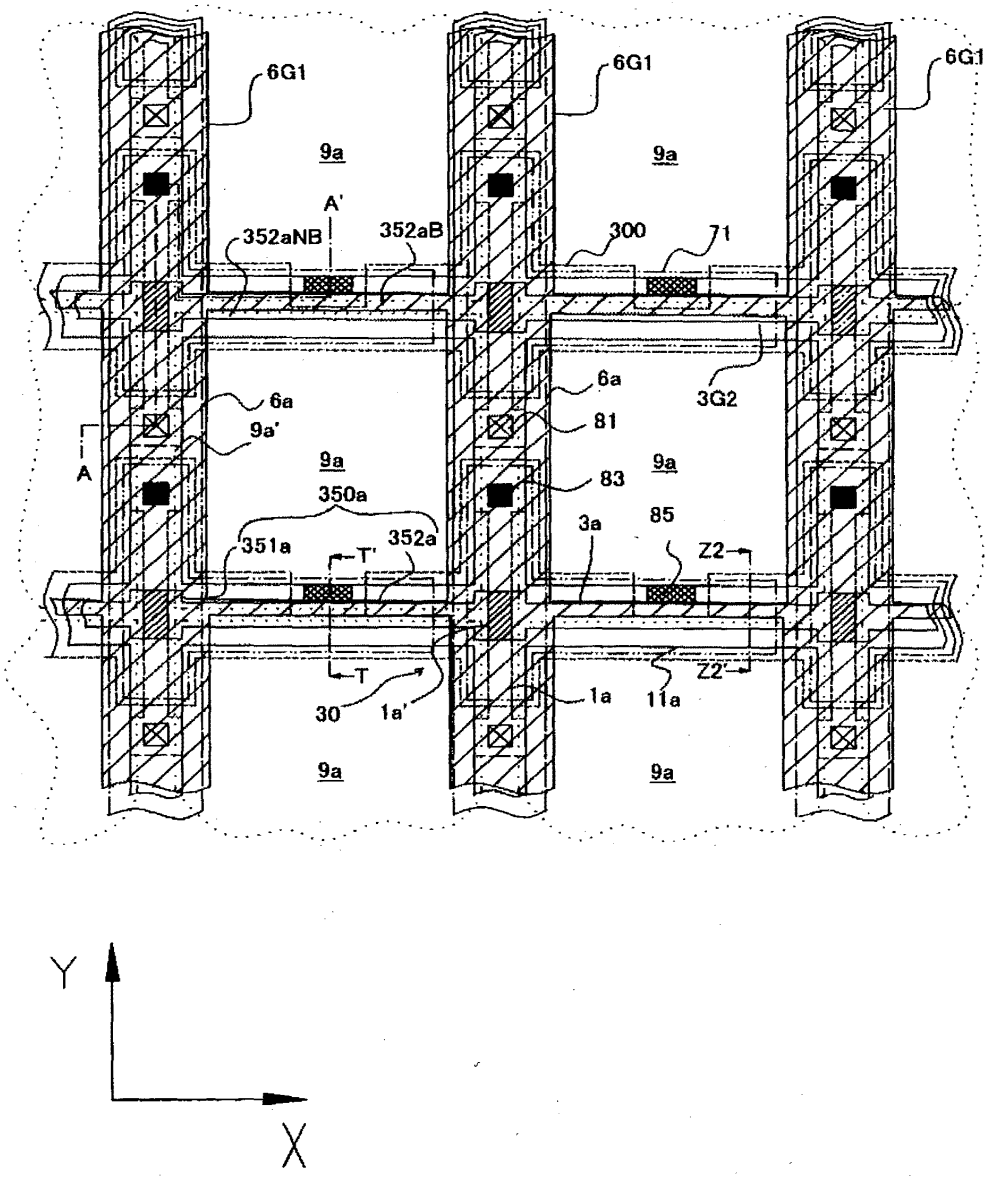

6G1
6G1
6G1
9a
9a
A'
352aNB
352aB
300
71
6a
3G2
81
6a
9a'
A
9a
9a
83
350a
85
3a
351a
352a
T'
Z2
T
Z2'
30
1a'
1a
11a
9a
9a
Y
X

FIG. 11

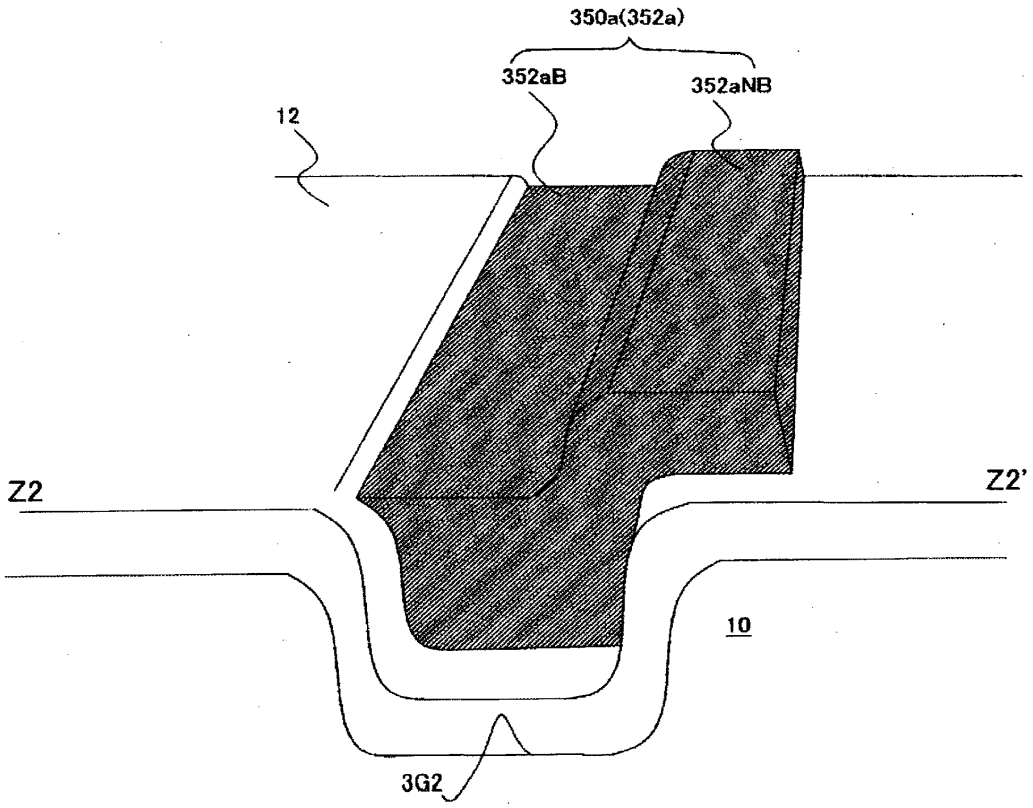


FIG. 12

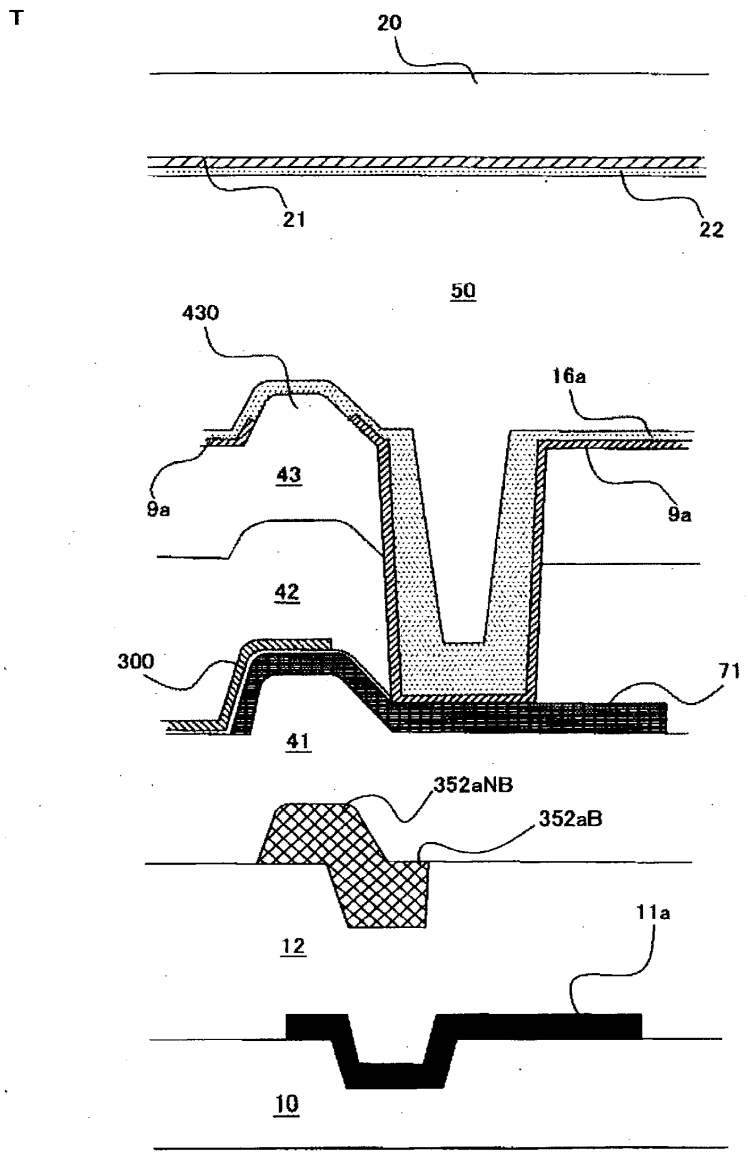


FIG. 13

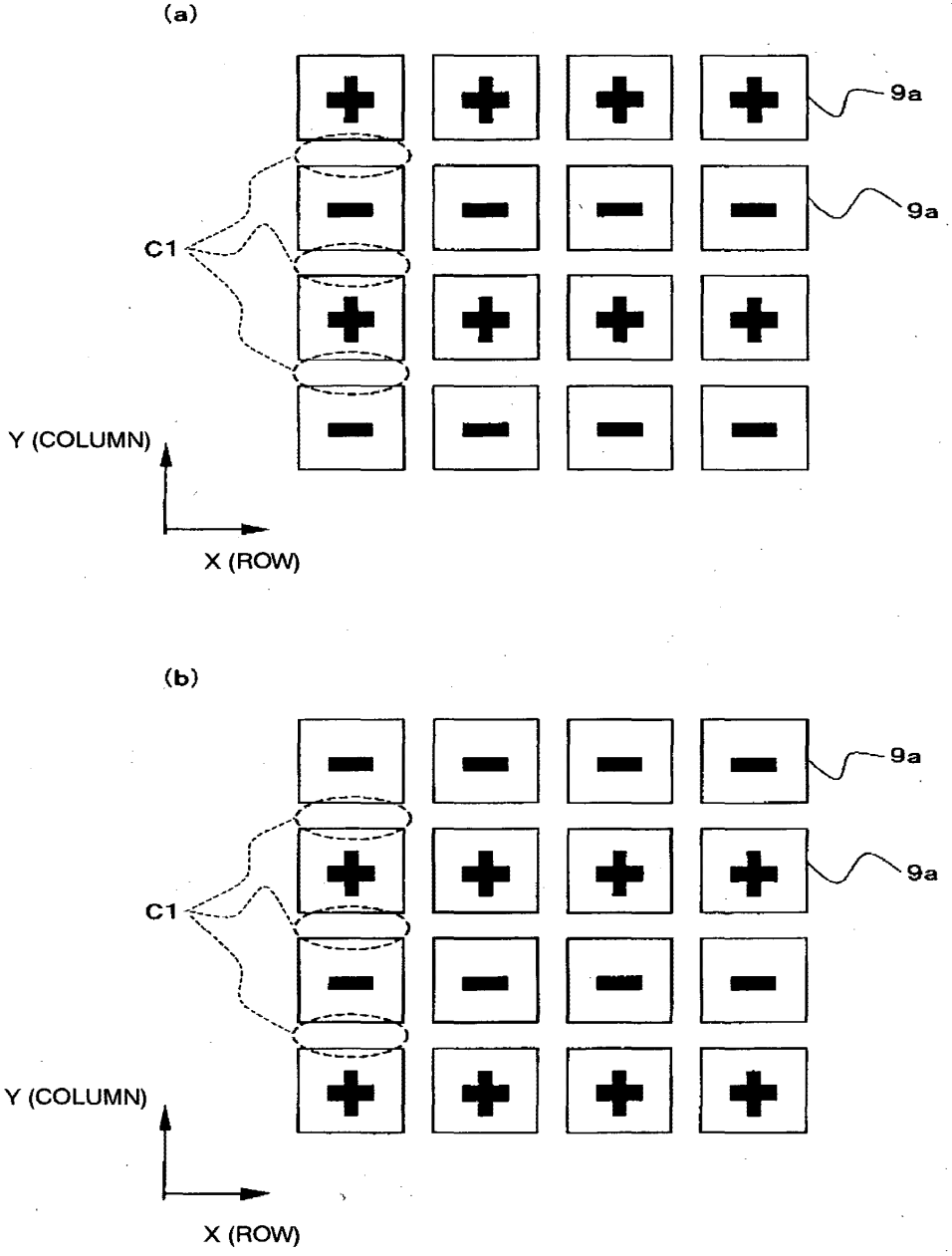


FIG. 14

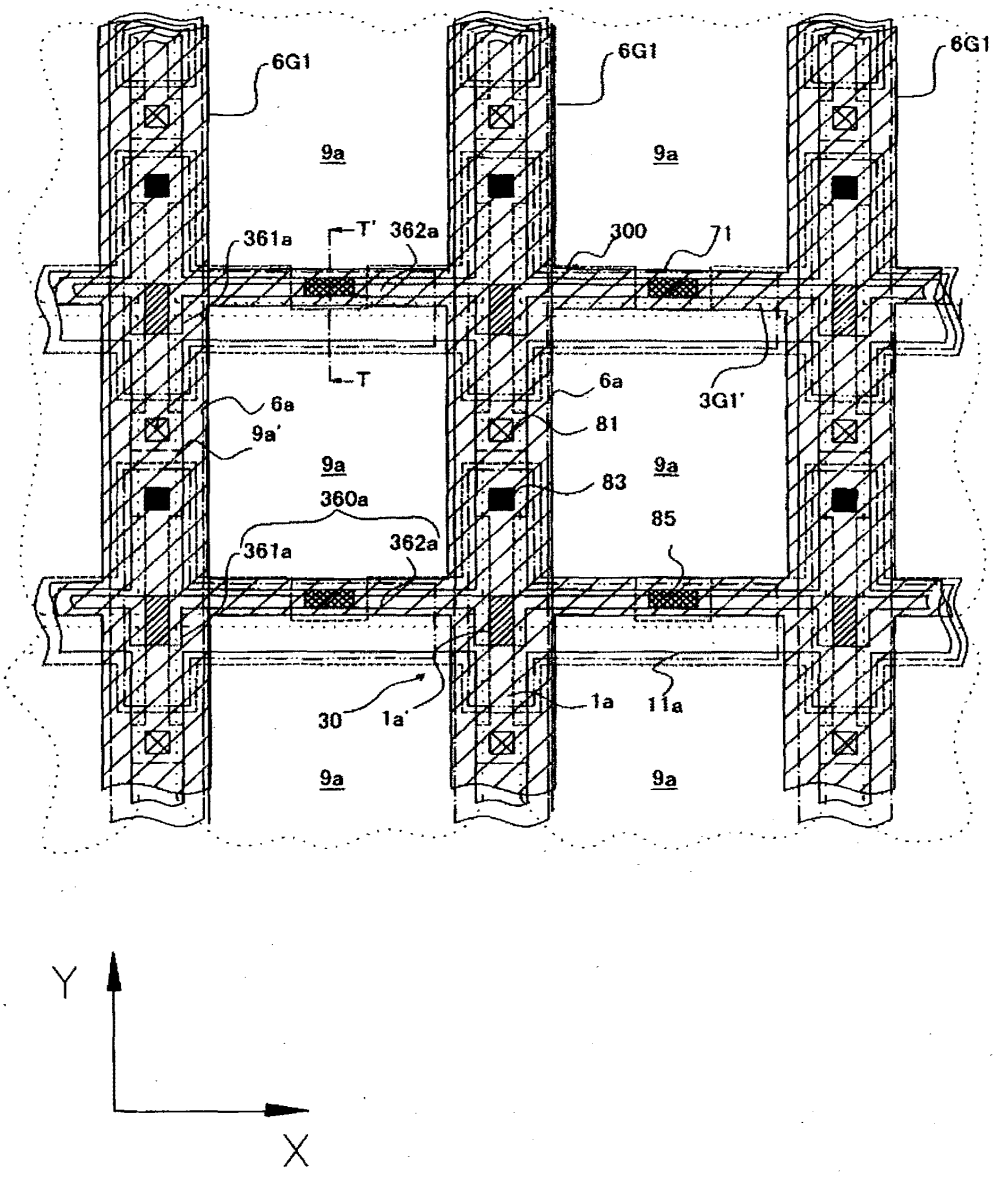

6G1
6G1
6G1
9a
9a
361a
T'
362a
300
71
T
6a
6a
3G1'
9a'
81
9a
9a
360a
83
85
361a
362a
30
1a'
1a
11a
9a
9a
Y
X

FIG. 15

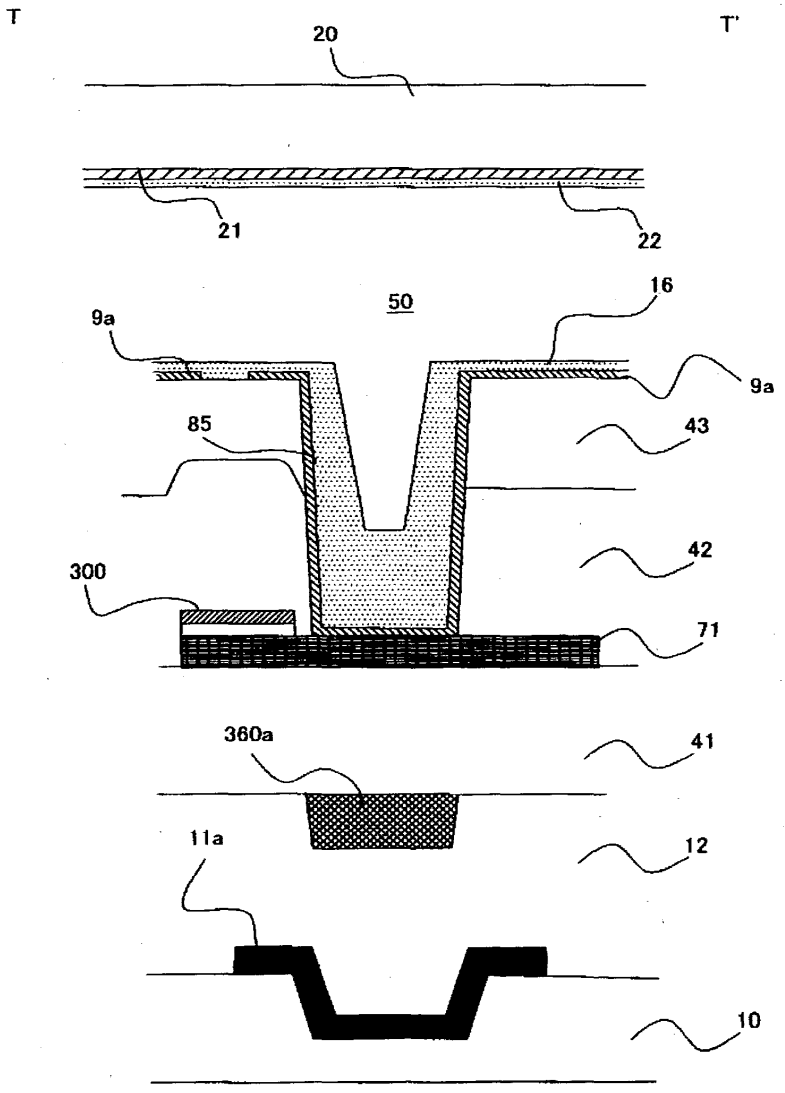


FIG. 16

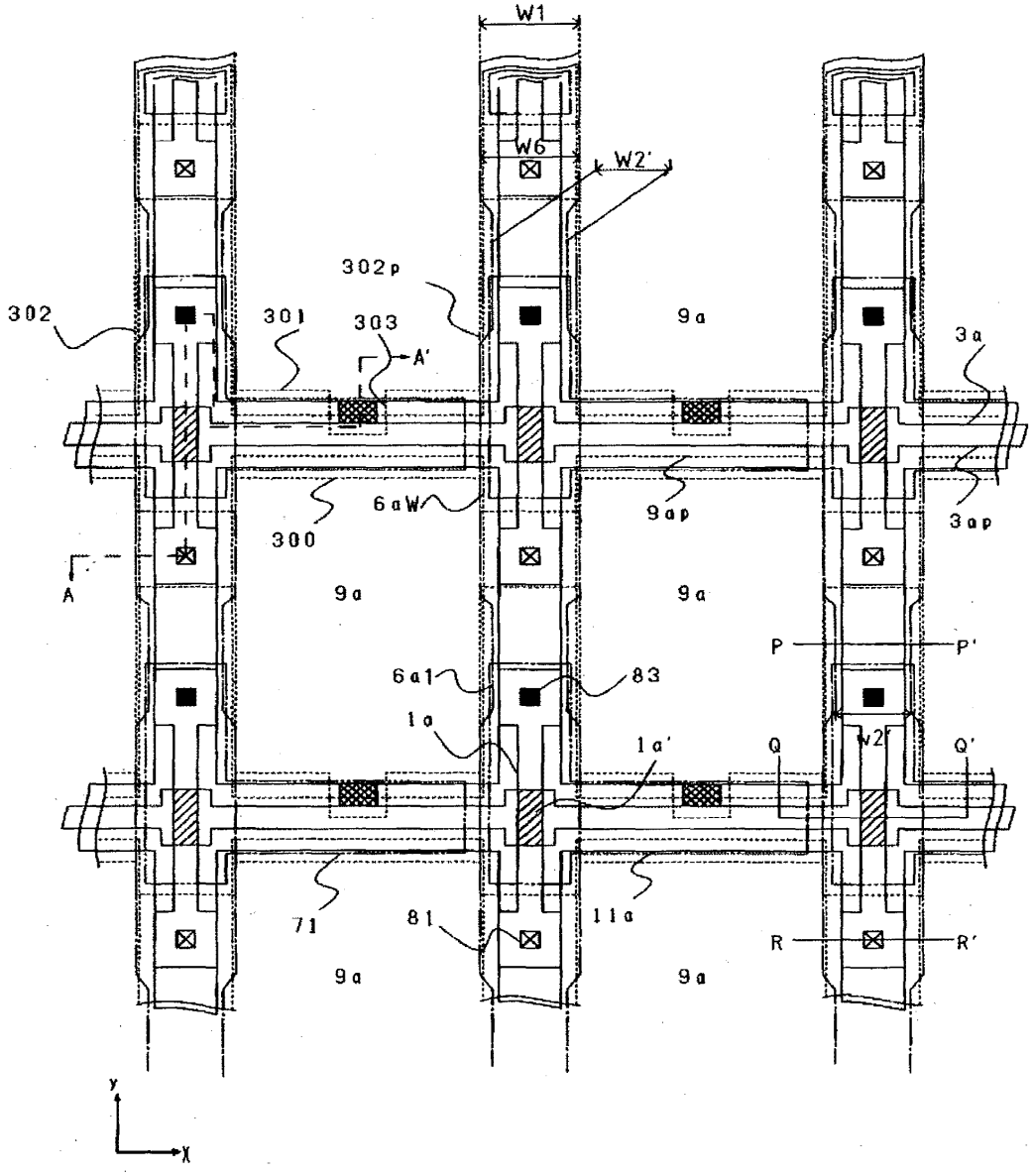

W1
W6
W2'
302p
302
301
303
A'
9a
3a
6aW
300
9ap
3ap
A
9a
9a
P
P'
6a1
83
1a
1a'
Q
W2
Q'
71
81
11a
R
R'
9a
9a
y
X

FIG. 17

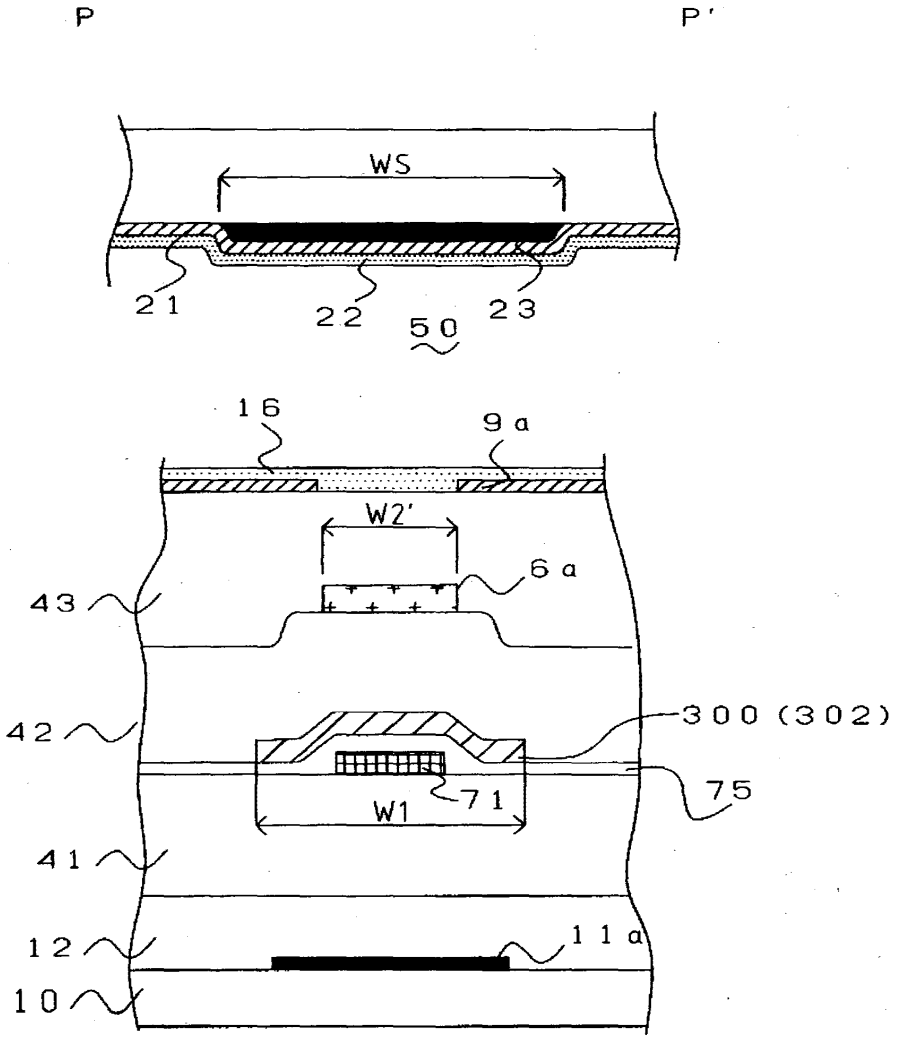


FIG. 18

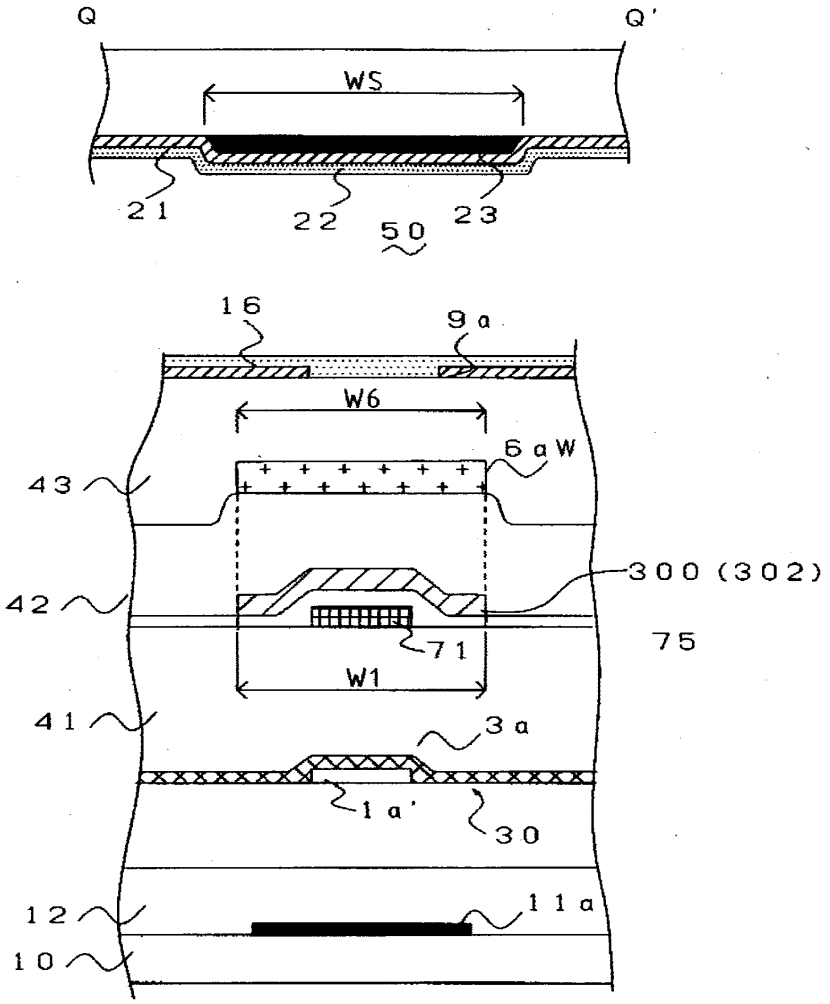

Q
Q'
WS
21
22
23
50
16
9a
W6
6aW
43
42
300 (302)
71
75
W1
41
3a
1a'
30
12
11a
10

FIG. 19

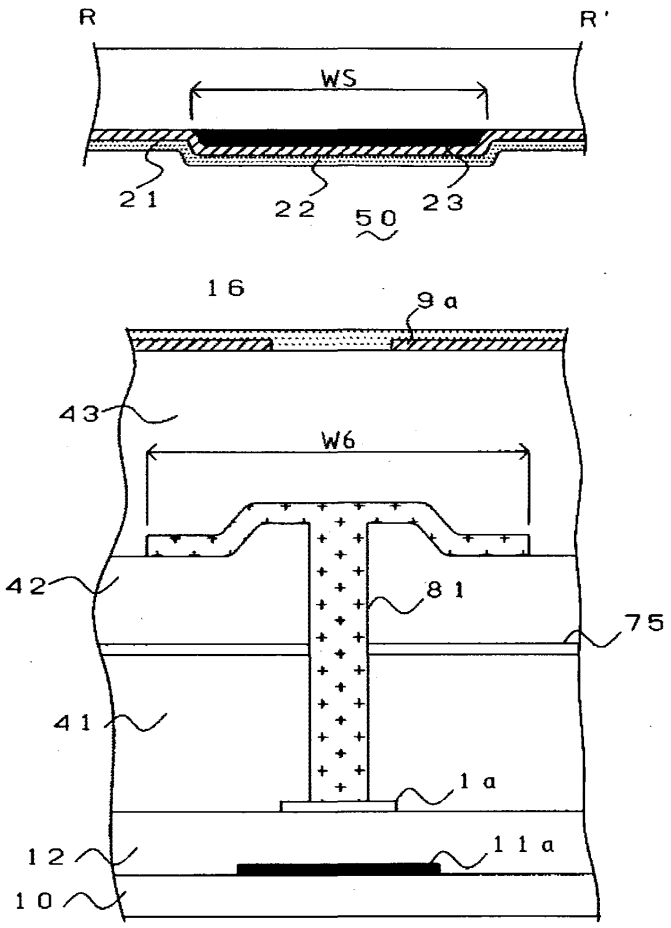


FIG. 20

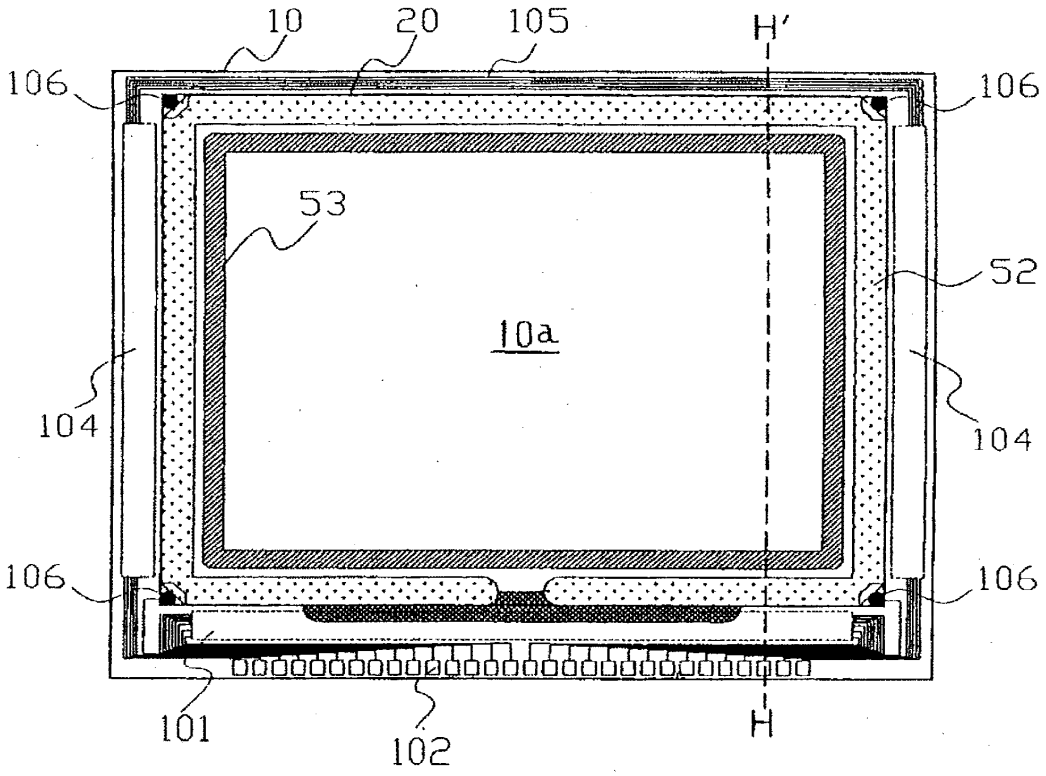

10
20
105
H'
106
106
53
52
10a
104
104
106
106
101
102
H

FIG. 21

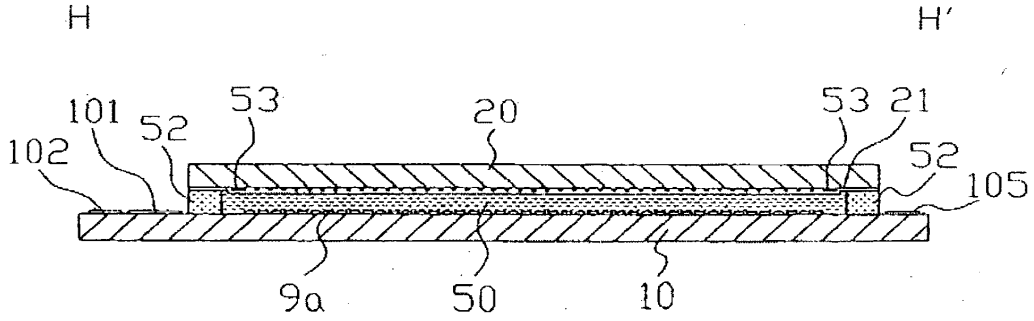
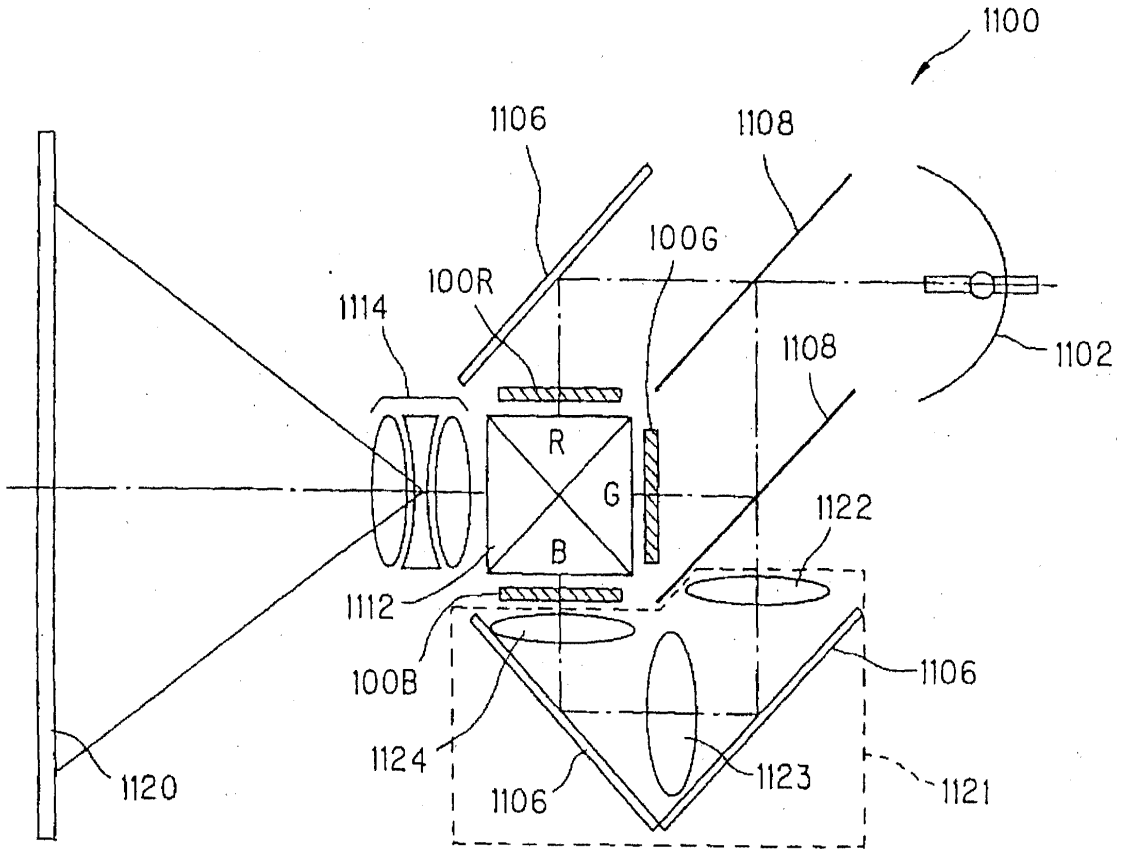

H
H'
101
52
53
20
53
21
102
52
105
9a
50
10

FIG. 22


1100
1106
1108
100G
100R
1114
1108
1102
R
G
B
1122
1112
100B
1106
1124
1123
1121
1106
1120

PTO/SB/106 (8-96)
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Seiko Epson Ref. No.: F007516US00 Attorney's Ref. No.: 114542

Declaration and Power of Attorney For Patent Application

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特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。	As a below named inventor, I hereby declare that:
私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。	My residence, post office address and citizenship are as stated next to my name.
下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
電気光学装置及び電子機器	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS
上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、	the specification of which is attached hereto unless the following box is checked:
☒ 2002年12月17日に提出され、米国出願番号または特許協定条約 国際出願番号を 10/320,371 とし、（該当する場合） _____ に訂正されました。	☒ was filed on December 17, 2002 as United States Application Number or PCT International Application Number 10/320,371 and was amended on _____ (if applicable).
私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。	I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。	I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office. Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks. Washington, DC 20231.

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(日本語宣言書)

私は、米国法典第３５編１１９条（ａ）-（ｄ)項又は３６５条（ｂ)項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条(ａ)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
2002-000713	Japan	07/January/2002	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
2002-363864	Japan	16/December/2002	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

私は、第３５編米国法典１１９条(ｅ)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(ｃ)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１章５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration
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委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

書類送付先：
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P.O. Box 19928
Alexandria, Virginia 22320

Send Correspondence to:
OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320

直接電話連絡先： (名前及び電話番号)
OLIFF & BERRIDGE, PLC
(703) 836-6400

Direct Telephone Calls to: *(name and telephone number)*
OLIFF & BERRIDGE, PLC
(703) 836-6400

唯一または第一発明者名
村出 正夫

Full name of sole or first inventor
Masao MURADE

発明者の署名 日付
村出正夫 2003年2月27日

Inventor's signature Date
Masao Murade February 27, 2003

住所
日本国, 長野県, 諏訪市

Residence
Suwa-shi, Nagano-ken, Japan

国籍
日本

Citizenship
Japan

私書箱
392-8502 日本国長野県諏訪市大和3丁目3番5号
セイコーエプソン株式会社内

Post Office Address
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3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan

第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名 日付

Second inventor's signature Date

住所
日本国, _____, _____

Residence
_____, _____, Japan

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

CIPE JC34 FEB 11 2003 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 10/320,371

Filed: December 17, 2002 Docket No.: 114542

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. An English-language Abstract of the non-English language reference is attached hereto.

☒ 3. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office (http://www.jpo.go.jp), and is attached, but has not been reviewed for accuracy. See Reference JP-A-2001-356709.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Date: February 11, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Sheet _____ of _____

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114542	APPLICATION NO. 10/320,371
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Masao MURADE	
		FILING DATE December 17, 2002	GROUP

OIPE JC54 FEB 11 2003 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
		JP-A-2001-356709 (w/English abstract & JPO translation)	12/26/01	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: February 11, 2003

UNITED STATES
PATENT AND
TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/320,371	12/17/2002	Masao Murade	114542

CONFIRMATION NO. 1588

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

FORMALITIES LETTER

OC000000009488934

Date Mailed: 02/06/2003

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- The application was filed in a language other than English. Applicant is required to provide an English translation of the specification and a statement that the translation is accurate. (See 37 CFR 1.52(d)).
- Applicant must file an English translation of the application, the $ 130 fee set forth in 37 CFR 1.17(i), unless previously submitted, and a statement that the translation is accurate (37 CFR 1.52(d)).
- Because your specification was filed in a language other than English, the Office was unable to determine the number of claims submitted. Additional claim fees may be due once the number of claims can be determined.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
  - The drawing figures contain text that is not in English (including, for example, a flow chart that was originally not in English that has been marked up to include the English text) (see 37 CFR 1.84(p)(2) and 37 CFR 1.52(d)(1)). See Figure(s) All.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$260** for a Large Entity

- **$130** Late oath or declaration Surcharge.
- **$130** for English translation surcharge required.

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

12/18/2002 HLE333 00000011 10320371
01 FC:1001 740.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1998-459-062/19144

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY

SERIAL NO.	FILING DATE
APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1			/			
2				/		
3				/		
4				/		
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TOTAL IND.			2			
TOTAL DEP.			16			
TOTAL CLAIMS			18			

	*		*		*	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

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12/17/02

NONPROVISIONAL PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

Attorney Docket No.: 114542

Date: December 17, 2002

BOX PATENT APPLICATION

J1036 U.S. PTO
10/320371
12/17/02

Customer Number: 25944

NONPROVISIONAL APPLICATION TRANSMITTAL
RULE §1.53(b)

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional patent application

For (Title): ELECTRIC OPTICAL APPARATUS AND ELECTRONIC DEVICE

By (Inventors): Masao MURADE

☒ Formal drawings (Figs. 1-22; 21 sheets) are attached.
☐ Use Figure for front page of Publication.
☐ A Declaration and Power of Attorney is filed herewith.
☒ This patent application is assigned to Seiko Epson Corporation.
☐ The executed Assignment is filed herewith.
☐ An Information Disclosure Statement is filed herewith.
☐ Entitlement to small entity status is hereby asserted.
☐ A Preliminary Amendment is filed herewith.
☐ Please amend the specification by inserting before the first line the sentence --This nonprovisional application claims the benefit of U.S. Provisional Application No. _____, filed _____.--
☒ Priority of foreign applications No. 2002-000713 filed January 7, 2002 in Japan and No. 2002-363864 filed December 16, 2002 in Japan are claimed (35 U.S.C. §119).
☐ A certified copy of the above corresponding foreign application(s) is filed herewith.
☐ This application is NOT to be published under 35 U.S.C. 112(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not been and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.
☒ The filing fee is calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF ANY PRELIMINARY AMENDMENT NOTED ABOVE

FOR:	NO. FILED	NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
BASIC FEE				$ 370	OR		$ 740
TOTAL CLAIMS	18 - 20	= 0	x 9 =	$	OR	x 18	$ ----
INDEP CLAIMS	2 - 3	= 0	x 42 =	$	OR	x 84	$ ----
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ 140 =	$	OR	+ 280	$ ----
			TOTAL	$	OR	TOTAL	$ 740

* If the difference is less than zero, enter "0".

☒ Check No. 137340 in the amount of $740.00 to cover the filing fee is attached. Except as otherwise noted herein, the Director is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

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JAO:EDM/cmm

OLIFF & BERRIDGE, PLC
ATTORNEYS AT LAW

Application Data Sheet

Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R:	None
Title::	ELECTRIC OPTICAL APPARATUS AND ELECTRONIC DEVICE
Attorney Docket Number::	114542
Total Drawing Sheets::	21
Small Entity::	No

Applicant Information

Applicant Authority type::	Inventor
Primary Citizenship Country::	Japan
Status::	Full Capacity
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Family Name::	MURADE
City of Residence::	Suwa-shi
Country of Residence::	Japan

Correspondence Information

Correspondence Customer Number:: 25944

Foreign Priority Information			
Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2002-000713	01/07/2002	Yes
Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2002-363864	12/16/2002	Yes

Assignee Information	
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Country of mailing address::	Japan
Postal or Zip Code of mailing address::	163-0811

SPECIFICATION

電気光学装置及び電子機器

BACKGROUND OF THE INVENTION

1. Field of the invention

本発明は、アクティブマトリクス駆動が可能な電気光学装置及び該電気光学装置を具備してなる電子機器の技術分野に属する。

2. Description of the related art

従来、液晶等の電気光学物質を挟持してなる一対の基板と、前記電気光学物質に対して電界を印加するため前記一対の基板のそれぞれに設けられた電極等とを備える電気光学装置が知られている。ここに、前記電極は、前記電気光学物質に電界を印加し、該電気光学物質の状態を適宜変化させるために利用される。そして、このような電気光学装置によれば、該装置に対して、例えば光源から発せられた光等を入射させるとともに、電気光学物質の状態を上述の如く適宜変化させれば、該光の透過率を制御することが可能となり、もって画像の表示を実現することが可能となる。

そして、このような電気光学装置においては、前記一対の基板の一方において、前記電極としてマトリクス状に配列された画素電極を備えるとともに、該画素電極の各々に接続された薄膜トランジスタ（Thin Film Transistor；以下適宜、「ＴＦＴ」という。）、該ＴＦＴの各々に接続され、行及び列方向それぞれに平行に設けられた走査線及びデータ線等を備えることで、いわゆるアクティブマトリクス駆動が可能なものが知られている。これにより、前記画素電極、あるいは前記走査線及び前記データ線により画される一つ一つの画素毎に、前記電気光学物質に対する電界の印加を制御して、画素毎に光の透過率を制御することが可能となる。

SUMMARY OF THE INVENTION

しかしながら、従来における電気光学装置には、次のような問題があった。すなわち、上述したようなアクティブマトリクス駆動が可能な電気光学装置においては、そもそもＴＦＴを正確に駆動する必要があるが、近年の電気光学装置に対する高精細化ないし小型化の要請を満たしながら、それを実現することはより困難になっているということである。

ここで、ＴＦＴは、チャネル領域、ソース領域及びドレイン領域を有する半導体層と、該半導体層における前記チャネル領域の少なくとも一部を覆うように絶縁膜を介して設けられたゲート電極を備え、該ゲート電極に対する通電・非通電を通じて、前記チャネル領域に電界を印加・非印加することで、電流の流れを制御する。

この際、前記チャネル領域の長さ、いわゆる「チャネル長」や、その幅、いわゆる「チャネル幅」をどのようにするか、換言するとチャネル領域の大きさをどの程度にするかは、ＴＦＴの特性を決める上で重要な事項となる。また、それに加えて、該チャネル領域上における前記ゲート電極の配設態様をどのようにするかも極めて重要である。ちなみに、従来においては、ゲート電極として、前記走査線に電気的に接続されている導電性部材や、前記走査線の一部を構成している部材があてられることがあったが、このような場合には、走査線それ自体とチャネル領域との配設態様も問題となる。

要するに、ＴＦＴないしチャネル領域と、走査線ないしゲート電極との好適な配置関係を、上述した電気光学装置の高精細化という要請をも加味した上で実現することが求められており、かつ、そのように構成されたＴＦＴ等による正確な動作を実現することが求められているということになるが、これは容易なことではない。

例えば、電気光学装置を駆動するためには、ＴＦＴ及び走査線ないしゲート電極だけ存在すればよいというのでは勿論なく、その他各種の構成要素を備える必要があるが、それらとの兼ね合いの中で、上記したような配置・調整を達成することは一般に困難であることが容易に想像しえる。また、ＴＦＴについては、前記チャネル領域に対して光が入射すると、光リーク電流が発生するという不都合が生じるから、これを防止しなければならないという要請もある。すなわち、Ｔ

ＦＴは、各画素において実際に画像表示に寄与する光が透過又は反射により出射する領域たる光透過域、より具体的には画素電極から、可能な限り離隔した方が好ましいが、高精細化が要求される中でこれを満たさなければならないとすると、上述の配置・調整には、より困難な課題を抱えることとなる。

本発明は、上記問題点に鑑みてなされたものであり、ゲート電極及び走査線の配置関係の調整がより容易に実現されるとともに、ＴＦＴの正確な駆動が可能とされた電気光学装置及び該電気光学装置を具備してなる電子機器を提供することを課題とする。

本発明の電気光学装置は、上記課題を解決するため、基板上に、一定の方向に延びる走査線及び該走査線に交差する方向に延びるデータ線と、前記走査線及び前記データ線の交差領域に対応して設けられた薄膜トランジスタと、該薄膜トランジスタに対応して設けられた画素電極とを備え、前記走査線は、前記薄膜トランジスタのチャネル領域に対向する部分にゲート電極としての幅広部を有するとともに、他の部分に幅狭部を有している。

本発明の電気光学装置によれば、走査線及びデータ線を介して走査信号及び画像信号を薄膜トランジスタに供給することにより、画素電極をアクティブマトリクス駆動できる。

そして特に、本発明では、前記走査線は、前記薄膜トランジスタのチャネル領域に対向する部分にゲート電極としての幅広部を有するとともに、他の部分に幅狭部を有していることから、走査線の狭小化等を実現しうるにもかかわらず、薄膜トランジスタないしそのチャネル領域と走査線との配置関係の調整・決定を、従来に比べて容易に実現しうることになる。

例えば、前記画素電極がマトリクス状に複数配列されている場合においては、それら一つ一つの画素電極の角部から最も離れた位置、換言すれば、四つの画素電極を想定したときに、隣接し、かつ対向する角部間のちょうど中間地点に、薄膜トランジスタのチャネル領域が位置するように当該薄膜トランジスタを形成することが一般的に好ましい（なぜなら、光透過域から最も離れているから）が、そのような場合において、チャネル領域を前記中間地点を含み隣接する画素電極

間の中間を縫うように延在させることで、チャネル長を好適にとることが可能な上、これに交差するように走査線を設けるとともに該走査線の幅広部が前記チャネル領域についてのみ存在するような構成を実現することが可能となる。したがって、この場合においては、好適なチャネル長の確保、すなわち、薄膜トランジスタの好適な動作の確保及び走査線の狭小化、すなわち、電気光学装置の高精細化ないし小型化という、いわば相反するともみえる要請が、ともに実現されることになる。また、この場合、上述の仮定から当然に、薄膜トランジスタないしチャネル領域に対する光入射を極力防止することも可能である。

このように、本発明によれば、電気光学装置の高精細化という要請を満たしながら、薄膜トランジスタ及び走査線ないしゲート電極との配置態様に関する調整を好適に実施することが可能となる。また、このことは、上述の走査線及び薄膜トランジスタ以外の、電気光学装置を構成する各種の要素の配置を調整・決定する上でも、好ましい影響を与える。さらに、本発明によれば、薄膜トランジスタの正確な駆動を実現することもでき、これにより、表示すべき画像の品質を高く保持することも可能となる。

なお、本発明において、「幅広」というのは、「幅狭部」が有する幅に対して広いという意味であり、「幅狭」というのは、「幅広部」が有する幅に対して狭いという意味である。要するに、「幅広部」及び「幅狭部」というときの具体的な広狭の程度は、両者の相対的な関係で決せられる。また、これに関連して、幅広部、あるいは幅狭部が実際に有すべき幅値は、理論的、経験的、実験的、あるいはシミュレーション等によって適宜決定しうる。

本発明の電気光学装置の一態様では、前記幅広部は、前記幅狭部から延設されて形成されている部分を含む。

この態様によれば、幅広部及び幅狭部を有する走査線を、比較的容易に形成することが可能となる。具体的には例えば、幅広部及び幅狭部がいわば一体的であるようなパターンを形成することを前提とした、公知のフォトリソグラフィ及びエッチングを用いることにより、本態様に係る走査線を容易に形成することが可能となる。

本発明の電気光学装置の他の態様では、前記幅広部は、前記幅狭部に接続され

て形成されている部分を含む。

この態様によれば、例えば、幅広部は、別に用意された導電部材等を幅狭部に対して接続することにより形成されている部分を含むことになる。このような場合であっても、比較的容易に幅広部を形成することが可能となる。

本発明の電気光学装置の他の態様では、前記走査線は、前記チャネル領域の延在する方向と交わる方向に延在しており、前記幅広部は、当該チャネル領域の延在する方向の一方又は両方に延在している。

この態様によれば、幅広部は、チャネル領域の延在する一方又は両方に延在されていることから、薄膜トランジスタ及び走査線との配置態様の調整を、より好適に実施しうることになる。また、この態様によれば、チャネル長に応じた適切なゲート電極が形成されることになるから、チャネル領域に対する電界の印加が、より効果的に実施されることになる。

また、このように、幅広部たるゲート電極が、チャネル領域となるべき部分にいわば追随するような形で設けられる態様によれば、例えば、いわゆる自己整合的な薄膜トランジスタの形成（すなわち、ゲート電極をマスクとして、イオン注入工程を行うことにより、チャネル領域に相隣接するソース領域及びドレイン領域の形成）を容易に行うことができる。ただし、この場合、厳密にいえば、ゲート電極となるべき幅広部を形成した後に、前記イオン注入工程を行うことで、チャネル領域が形成されることになる。

本発明の電気光学装置の他の態様では、前記画素電極は、マトリクス状に配列がなされてなり、前記チャネル領域は、平面的に見て前記走査線を挟んで相隣接する画素電極間を縫って延びる長手状の第１間隙と、前記データ線を挟んで相隣接する画素電極間を縫って延びる長手状の第２間隙とが交わる交点領域内に形成されている。

この態様は、既に述べた態様に類似し、本発明の作用効果が最も効果的に発揮されうる態様の一つである。

すなわち、この態様によれば、薄膜トランジスタのチャネル領域が、マトリクス状に複数配列された画素電極において、その交点領域内に形成されている。ここに、交点領域とは、平面的に見て前記走査線を挟んで相隣接する画素電極間を

縫って延びる長手状の第１間隙と前記データ線を挟んで相隣接する画素電極間を縫って延びる長手状の第２間隙とが交わる領域である。このような構成により、該チャネル領域に対する光の入射は生じにくい状態が現出されている。

そして、このような作用効果を有しながら、走査線は、前記チャネル領域に対向するようにゲート電極としての幅広部を有していることから、チャネル領域ないし薄膜トランジスタと、ゲート電極ないし走査線との配置態様を最も好適に決定しうるとともに、好適なチャネル長の確保と走査線の狭小化をも実現することが可能となるのである。

この態様では特に、前記幅狭部は、前記第１間隙の中央よりもずれた位置に形成され、前記幅広部は、前記交点領域内において前記第１間隙の中央に形成されている。

このような構成によれば、走査線の幅狭部は、隣接する画素電極間を縫うようには存在するが、その中央には存在せず、該中央よりもずれた位置に形成される。このことにより、まず第１に、表示画像の品質向上を図ることができる。これは、とりわけ電気光学装置の一例たる液晶表示装置等において該当し、その理由は以下の事情による。

すなわち、本態様では、前記液晶表示装置に通常設けられる配向膜上の凸部、とりわけ前記幅狭部の「高さ」に起因して形成される凸部に対するラビング処理を実施すると、該凸部においてラビングのムラが生じることに着目し、更には、前記凸部において、ラビングの擦り上げ（すなわち、凸部を登る方向）に係る部分と擦り下げ（すなわち、凸部を下る方向）に係る部分とでは、前記ムラの程度に差があることに着目する。

より具体的には、例えば、前記擦り上げに係る部分の方が、前記擦り下げに係る部分よりも、前記ムラが生じにくい。

そして、上記したようなムラをそのままに放置すると、液晶の配向不良等を招来し、電気光学装置の動作不良の原因となる場合がある。上述の擦り上げ及び擦り下げ間のムラの程度の差にしたがって言えば、後者の方が前者の方よりも、液晶の配向不良等を招来する可能性が高いことになる。

ここで、本態様における幅狭部が、前記画素電極間の第１間隙の中央から外れ

た位置に形成されることが意味を帯びる。すなわち、幅狭部をこのような位置に形成することによれば、該幅狭部に起因する凸部の頂点もまた、第１間隙の中央から外れた位置に形成されることになり、このことは、当該第１間隙に対応する領域上に、当該凸部のほぼ半斜面だけを存在させるような構成を採ること、すなわち該領域上に、前記擦り下げに係る部分だけを存在させるような構成を採ることが可能であることを意味する。そして、この場合において、遮光膜を前記第１間隙に対応するように設ければ、前記擦り下げに係る部分だけを有効に遮光すること、つまりムラの影響が最も生じると考えられる凸部の当該部分を有効に遮光することが可能となるのである。

以上の結果、本態様によれば、ムラの影響による電気光学装置の動作不良等を生じさせることが殆どなく、また、ムラの影響がより生じにくいと考えられる凸部の擦り上げに係る部分は、画像表示に寄与する光を透過可能のままにしておくことになるから、画素開口率の向上、すなわち画像は明るいままこれを維持することが可能となるのである。結局、本態様によれば、以上述べたような意味において、表示画像の品質向上が図られることになるのである。

また、幅狭部を、第１間隙の中央よりもずれた位置に形成することによれば、第２に、電気光学装置の設計の自由度を向上すること、また、薄膜トランジスタに対する光入射をより効果的に防止することができる。これは以下の事情による。

すなわち、本態様における幅狭部は、隣接する画素電極間の第１間隙を縫うようには存在するが、その中央には存在しない。このため例えば、第１間隙の領域中、幅狭部が設けられていない領域を利用することにより、平面的にみて、該幅狭部に平行に該幅狭部と同一膜から構成された容量線等の他の配線を配線することが可能となる。すなわち、設計の自由度が増大するのである。

また、上述のような場合に、幅狭部は中央線からはずれているものの、幅広部はその幅広の程度を調整することにより、例えば、一方側のみを幅広に広げたり、一方側を大きく幅広に且つ他方側を小さく幅広にすることで、ゲート電極としての幅広部を、間隙の中央に配置させることが可能となる。このように、走査線の位置によらずにゲート電極の配置を遮光性を高めるのに都合の良い位置に配

置できるので、或いはゲート電極の配置を遮光性を高めるのに都合の良い位置に配置しながら、走査線の配置を間隙内における任意の位置に配置できるので、最終的には、走査線配置を含めた配線配置の自由度を高めつつ遮光性が本質的に高い薄膜トランジスタを実現できる。

この構成では更に、前記幅広部は、前記交点領域内において前記第２間隙の中央に形成されているようにするとよい。

このような構成によれば、チャネル領域は、既述した言い方に沿えば、四つの画素電極を想定した場合に、隣接し、又は対向する、該電極の角部から最も離れた位置に形成されることになる。すなわち、該チャネル領域に対しては、最も光の入射が発生しにくい状態が現出されることになる。

本発明の電気光学装置の他の態様では、前記基板には、前記走査線に沿って溝が掘られており、前記走査線は該溝内に直接又は層間絶縁膜を介して少なくとも部分的に埋め込まれている。

この態様によれば、走査線が基板に形成された溝内に埋め込まれていることから、該走査線自身が有する高さに起因して、その上層として形成される層間絶縁膜、或いは画素電極及び配向膜等の表面に段差を生じさせることを未然に防止することができる。つまり、当該表面を極めて良好に平坦化することができる。そして、このように配向膜等の表面が平坦であると、該配向膜に対するラビング処理を好適に実施することができ、該配向膜に接する液晶分子の配向状態を良好に維持することができる。したがって、本態様によれば、配向不良が生じる可能性を減退させ、該配向不良の部分を起因とする光抜け等の発生を極力防止することができることになるから、高品質な画像を表示することが可能となる。

本発明の電気光学装置の他の態様では、前記幅狭部は、前記溝内に埋め込まれているとともに前記走査線に沿って延びる埋め込み部分と、前記溝内に埋め込まれないとともに前記埋め込み部と並んで前記走査線に沿って延びる非埋め込み部分とを有し、該非埋め込み部分の存在によって、前記画素電極の下地は、前記走査線に沿って盛り上がっている。

この態様によれば、前記幅狭部は埋め込み部と非埋め込み部とを有している。そして、これら埋め込み部及び非埋め込み部はいずれも走査線に沿って延びてお

り、このうち非埋め込み部分の存在によって、前記画素電極の下地は、前記走査線に沿って盛り上がっている。

これによれば、まず、埋め込み部に関しては、上述の平坦化にかかる作用効果が同様に得られることになる。つまり、該埋め込み部上の上層として形成される層間絶縁膜、或いは画素電極及び配向膜等の表面は極めて良好な平坦性を呈示することになり、当該部分における配向不良等を生じさせる可能性を低減することができる。

次に、非埋め込み部に関しては、該非埋め込み部の上層として形成される前記配向膜等の表面に、あえて走査線に沿った凸部を含む段差が形成されるが如き状態になるから、上述の平坦化に係る作用効果は得られないものの、次のような利点を得ることができる。

まず、本発明に係る電気光学装置では、液晶の劣化を防止し装置寿命の長期化等を図るとともに、表示画像上のクロストークやフリッカ等を低減することを目的として、前記画素電極を二つの群に分けた上、これらを別々の周期で反転駆動する駆動方法が採用されることがある。すなわち、第１の周期で反転駆動されるための第１の画素電極群と、第１の周期と相補の第２の周期で反転駆動されるための第２の画素電極群とを含む複数の画素電極が基板上に平面配列されており、(i) 反転駆動時に各時刻において相互に逆極性の駆動電圧で駆動される相隣接する画素電極と(ii)反転駆動時に各時刻において相互に同一極性の駆動電圧で駆動される相隣接する画素電極との両者が存在している。ここで、前記（ｉ）に該当する画素電極がデータ線に沿う方向に並べられ、前記（ｉｉ）に該当する画素電極が走査線に沿う方向に並べられているとすると、或る一の走査線に沿う方向に並ぶ画素電極が一の極性で駆動されるとともに、前記或る一の走査線に相隣接する他の走査線に沿う方向に並ぶ画素電極が前記一の極性の反対の極性で駆動されるということになる（いわゆる「１Ｈ反転駆動」）。

しかしながら、この場合、データ線に沿って相隣接する画素電極間では、逆極性の駆動電圧による駆動に基づく横電界が発生することになる。このような横電界は、画素電極及び対向電極間で発生する電界（前記横電界に対する「縦電界」と呼べる。）に乱れを生じさせるおそれがあり、その結果、液晶分子の配向状態

を所望通りにとらせることが困難となり、画像表示に影響を及ぼす可能性がある。

そして、本態様では、このような不具合の発生する可能性がある場合において、画素電極の下地に形成された、走査線に沿う凸部が特有の意義を帯びてくることになる。

すなわち、第１に、各画素電極の縁部が前記段差上に位置するように形成されるとすれば、各画素電極と対向電極との間に生じる縦電界を、相隣接する画素電極（特に、異なる画素電極群に属する画素電極）の間に生じる横電界と比べて、相対的に強められる。即ち、一般に電界は電極間の距離が短くなるにつれて強くなるので、段差の高さの分だけ、画素電極の縁部が対向電極に近づき、両者間に生じる縦電界が強められるのである。第２に、各画素電極の縁部がこの段差上に位置するか否かに拘わらず、相隣接する画素電極（特に、異なる画素電極群に属する画素電極）の間に生じる横電界が段差の存在により段差の誘電率に応じて弱められると共に横電界が通過する電気光学物質の体積を（段差で部分的に置き換えることにより）減ずることによっても、当該横電界の電気光学物質に対する作用を低減できる。従って、反転駆動方式に伴う横電界による液晶の配向不良等の電気光学物質の動作不良を低減できる。この際、上述のように画素電極の縁部は、段差上に位置してもよいし位置していなくてもよく、更に段差の傾斜した或いは略垂直な側面の途中に位置していてもよい。

加えて、電気光学物質の動作不良個所を隠すための遮光膜も小さくできるので、光抜け等の画像不良を起こさずに各画素の開口率を高めることも可能となる。

以上説明したように、本態様によれば、第一に埋め込み部の存在により、前述した平坦化に係る作用効果を得ることができると同時に、第二に非埋め込み部の存在により、走査線に沿う凸部を含む段差をあえて形成することにより、横電界の発生を防止するという作用効果を得ることができる。

本発明の電気光学装置の他の態様では、前記画素電極に接続されており蓄積容量を構成する画素電位側容量電極と、該画素電位側容量電極に誘電体膜を介して対向配置されており前記蓄積容量を構成する固定電位側容量電極を含む容量線と

を更に備えてなり、前記容量線は、前記走査線に沿って延びる本線部と前記データ線に沿って延びる部分とを有し、前記容量線における前記データ線に沿って延びる部分の幅は、当該データ線の幅と同一又はより広く形成されている。

この態様によれば、画素電極には、画素電位側容量電極と固定電位側容量電極とが対向配置されてなる蓄積容量が接続されているので、画素電極に書き込まれた画像信号の電圧を長期にわたって保持できる。そして特に、本態様においては、容量線における前記データ線に沿って延びる部分の幅は、当該データ線の幅と同一又はより広く形成されていることにより、容量線をより低抵抗化することが可能となる。また、本態様においては、上述のように容量線の低抵抗化を実現しうることから、装置全体から見て、容量線の狭小化、ひいては蓄積容量の狭小化を達成しうることとなり、その結果、開口率の向上を図ることができる。ここで、「容量線の狭小化」というとき、容量線自体は、その幅がデータ線の幅と同一か、又は「より広く」形成されるのであるから、一見矛盾するかのように見えるが、そこに想定されている幅広・幅狭という概念は、あくまでも容量線とデータ線との相対的な関係から決定されるべきものであるから、装置全体から見れば、従来に比べて、「容量線の狭小化」が達成しうるのである。なお、上述にいう幅広・幅狭、あるいは本発明にいう「より広く」という場合の、具体的な幅値は、理論的・実験的・経験的、あるいはシミュレーションによって、適宜好適なものを決定しうる。

さらに、本態様によれば、上述の低抵抗化だけではなく、薄膜トランジスタ、とりわけそのチャネル領域に対する光入射を、従来に比べてより効果的に防止することが可能となる。というのも、既述したように、従来においては、データ線の裏面等で反射した光が迷光となって、結局、薄膜トランジスタに入射する場合があったところ、本態様によれば、そのような迷光であっても、データ線の幅と同一か、又はより広く形成された容量線により、その光の進行が遮られる可能性が高くなるからである。

以上のことから、本発明によれば、容量線の低抵抗化により、従来問題となっていたクロストークや焼き付き等の問題が生じる可能性が低減する。また、薄膜トランジスタにおける光リーク電流の発生が低減されることにより、高い品質を

もつ画像を表示することが可能となる。

また、本発明においては、容量線において、前記データ線に沿って延びる部分が存在していることにより、蓄積容量の増大化を実現することができる。これも、高い品質をもつ画像の表示に大きく資することになる。

なお、上述したような光遮蔽機能を、より好適に発揮させるためには、容量線を構成する材料として、光遮光性の優れたものをあてるとよい。例えば、Ａｌ（アルミニウム）、Ｃｕ（銅）、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）等のうち少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等が好適に使用できる。また、これに加えて、例えば、ポリシリコン等の光吸収性の材料を使用することもできる。

この態様では、前記データ線は、前記薄膜トランジスタに重なる部分が局所的に幅広に形成されており、前記容量線における前記データ線に沿って延びる部分の幅は、前記データ線における幅広に形成されていない部分の幅より広く且つ前記データ線における前記幅広に形成された部分の幅と同一に形成されているように構成するとよい。

このような構成によれば、データ線における薄膜トランジスタに重なる部分が局所的に幅広に形成されている。そして、この幅広に形成された部分の幅は、前述した容量線におけるデータ線に沿って延びる部分の幅と同一とされている。すなわち、これによると、該薄膜トランジスタの上方には、いずれも幅広に形成されたデータ線及び容量線が形成されていることになる。したがって、該薄膜トランジスタの上方からの光入射を、より確実に防止することができる。

より具体的には例えば、容量線が高融点金属等からなる場合においては、該容量線単独で、透過率にして０．１％程度（ＯＤ（Optical Density）値では、２以上）の遮光性能を発揮させることができる。しかしながら、当該容量線に対してシリサイド化処理等を実施すると、その組成が変化すること等により、その遮光性能が低下する場合がある。この場合、前述の透過率０．１％以上の遮光性能しか享受できないという場合もあり得る。

しかるに、本態様においては、このような高融点金属膜からなる容量線に重ね

て、データ線もまた存在する。このように、容量線及びデータ線の重なり合いにより、薄膜トランジスタの遮光を行う構成を採用すれば、これらの透過率の積算値に該当する遮光性能を得ることができる。例えば、データ線がアルミニウム等からなる場合においては、透過率にして、０．００１％以下程度（ＯＤ値では、４以上）の遮光性能を発揮させることができる。

なお、本態様では特に、容量線におけるデータ線に沿って延びる部分の幅が広いとは、データ線における幅広に形成されていない部分の幅よりも広いという意味である。

あるいは、前記データ線は、前記薄膜トランジスタに重なる部分が局所的に幅広に形成されており、前記容量線における前記データ線に沿って延びる部分の幅は、前記データ線における幅広に形成されていない部分の幅より広く且つ前記データ線における前記幅広に形成された部分の幅より狭く形成されている。

この態様によれば、データ線における薄膜トランジスタに重なる部分が局所的に幅広に形成されている。すなわち、これによると、該薄膜トランジスタの上方には、いずれも幅広に形成されたデータ線及び容量線が形成されていることになる。したがって、該薄膜トランジスタの上方からの光入射を、より確実に防止することができる。

なお、本態様では特に、容量線におけるデータ線に沿って延びる部分の幅は、幅広に形成されたデータ線より幅狭に形成されている。つまり、当該部分において、データ線は容量線よりも幅狭とされている。これにより、例えばデータ線を光反射率の高いアルミニウム等で構成する場合において、入射光が電気光学装置内部の何らかの要素で反射して生じる迷光や、いったん電気光学装置を出射した光が該電気光学装置外部の何らかの要素で反射して再び電気光学装置に戻ってくる戻り光、或いは電気光学装置が複数設置されるカラー表示可能な液晶プロジェクタ等の投射型表示装置において他の電気光学装置を出射した光が当該電気光学装置に戻ってくる戻り光等が、前記データ線で反射することによって迷光を増大させるという事態を防止することができる。これは、データ線における幅広に形成された部分が、容量線に比べて相対的に幅狭に形成されているからである。

このような薄膜トランジスタに重なる部分が幅広に形成されたデータ線を備え

る態様では、前記容量線は、前記薄膜トランジスタと前記データ線との間の積層位置に配置されており、前記データ線は、前記薄膜トランジスタに重なる部分に加えて、前記薄膜トランジスタとの接続用のコンタクトホールが設けられた部分が、幅広に形成されているように構成するとよい。

このような構成によれば、このコンタクトホールのために、遮光膜としての容量線を設けることができなくても、その分の遮光性能の低下を、データ線を幅広に形成することで補うことが可能となる。

あるいは、前記データ線は、前記薄膜トランジスタごとに、前記薄膜トランジスタに重なる部分から前記コンタクトホールが設けられた部分までが連続して幅広に形成されているように構成するとよい。

このような構成によれば、薄膜トランジスタに対する遮光をより確実になしうる。

なお、薄膜トランジスタに重なる部分における幅広に形成された部分と、コンタクトホールが設けられた部分における幅広に形成された部分とは、別々に幅広に形成されていてもよい。薄膜トランジスタに重なる部分とコンタクトホールが設けられた部分とを近接配置して、当該態様の如く、連続して幅広に形成すると、幅広に形成する領域をむやみに広げないで済むので、内面反射を増大させない観点から有利である。

本発明の電気光学装置の他の態様によれば、前記基板に電気光学物質を介して対向配置された他の基板と、該他の基板上に形成された遮光膜とを更に備えてなり、前記データ線及び前記容量線における前記データ線に沿って延びる部分の幅は、前記遮光膜の幅よりも狭い。

この態様によれば、前記他の基板から光が入射すると仮定すると、その光の入射側から順に、遮光膜、データ線及び容量線という積層構造を構築することが可能となる。ここで、このうちの前者の幅は、後二者の幅よりも広い。すなわち、入射光は、より幅広の遮光膜によってその進行が遮られることになり、そこを通り抜けた光だけが、データ線及び容量線に到達することになる。更に、遮光膜を通り抜けた光が、データ線及び容量線に到達する場合には、これらデータ線及び容量線による前述の遮光機能の発揮を期待することができる。要するに、本態様

によれば、薄膜トランジスタの耐光性をより高めることができ、光リーク電流の発生する可能性をより減退させることができる。

なお、本態様にいう「遮光膜」は、例えば前記画素電極がマトリクス状に配列されるのであれば、該画素電極の間隙を縫うようにストライプ状、或いは格子状に形成することが可能である。また、場合により、該遮光膜を、例えばクロム或いはクロミナ等の光吸収性材料及びアルミニウム等の光反射性材料からなる積層構造として形成することも可能である。

本発明の電子機器は、上述した本発明の電気光学装置（ただし、その各種態様を含む。）を具備してなる。

本発明の電子機器によれば、例えば、上述したように、薄膜トランジスタと走査線との配置態様の好適な調整を行うことができる電気光学装置を具備してなることにより、薄膜トランジスタの正確な動作、またこれによる高品質な画像の表示が可能な、例えば、液晶プロジェクタ、液晶テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネル等の各種電子機器を実現することができる。

本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにされる。

BRIEF DESCRIPTION OF THE DRAWING

図１は、本発明の実施形態の電気光学装置における画像表示領域を構成するマトリクス状の複数の画素に設けられた各種素子、配線等の等価回路を示す回路図である。

図２は、本発明の実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

図３は、図２のＡ－Ａ´断面図である。

図４は、図２に示す走査線の形状パターンのみを示す平面図である。

図５は、図２と同趣旨の図であって、当該図とは走査線及びＴＦＴの配置関係が異なる態様となるものを示す図である。

図６は、図５に示す走査線の形状パターンのみを示す平面図である。

図７は、図５のＢ－Ｂ’断面図である。

図８は、図２と同趣旨の図であって、同図とはＴＦＴアレイ基板上に溝が形成されている点及び該溝内に走査線が埋め込まれている点等について異なる態様を示すものである。

図９は、図８に示す走査線の幅狭部の様子を示す断面図である。

図１０は、図２と同趣旨の図であって、同図とはＴＦＴアレイ基板上に溝が形成されている点及び該溝内に走査線の一部が埋め込まれている点等について異なる態様を示すものである。

図１１は、図１０に示す走査線の幅狭部の様子を示す断面図である。

図１２は、図１０のＴ－Ｔ´断面図である。

図１３は、横電界の発生機構について説明するための説明図である。

図１４は、図２と同趣旨の図であって、同図とはＴＦＴアレイ基板上に溝が形成されている点及び走査線の幅狭部が第１間隙の中央から外れて形成されている点等について異なる態様を示すものである。

図１５は、図１４のＴ－Ｔ´断面図である。

図１６は、図２と同趣旨の図であって、同図とはデータ線の形態が異なるものを示す図である。

図１７は、図１６のＰ－Ｐ´断面図である。

図１８は、図１６のＱ－Ｑ´断面図である。

図１９は、図１６のＲ－Ｒ´断面図である。

図２０は、本発明の実施形態の電気光学装置におけるＴＦＴアレイ基板を、その上に形成された各構成要素とともに対向基板の側から見た平面図である。

図２１は、図２０のＨ－Ｈ´断面図である。

図２２は、本発明の電子機器の実施形態である投射型カラー表示装置の一例たるカラー液晶プロジェクタを示す図式的断面図である。

【符号の説明】

１ａ…半導体層

１ａ´…チャネル領域

３３０ａ、３３０ａ´、３４０ａ、３５０ａ、３６０ａ…走査線
３３１ａ、３３１ａ´、３４１ａ、３５１ａ、３６１ａ…幅広部
３３２ａ、３３２ａ´、３４２ａ、３５２ａ、３６２ａ…幅狭部
３Ｇ１、３Ｇ１´、３Ｇ２…溝
３５２ａＢ…埋め込み部
３５２ａＮＢ…非埋め込み部
４３０…段差
９ａ…画素電極
１０…ＴＦＴアレイ基板
１６…配向膜
３０…ＴＦＴ
５０…液晶層

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

以下では、本発明の実施の形態について図を参照しつつ説明する。以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

まず、本発明の実施形態における電気光学装置の画素部における構成について、図１から図４を参照して説明する。ここに、図１は、電気光学装置の画像表示領域１０ａを構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。図２は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。そして、図３は、図２のＡ－Ａ´断面図である。なお、図３においては、各層・各部材を図面上で認識可能な程度の大きさとするため、該各層・各部材ごとに縮尺を異ならしめてある。また、図４は、図２に示す走査線のみを抜き出してその形状を示す平面図である。

図１において、本実施形態における電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素には、それぞれ、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されてい

る。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給しても構わないし、相隣接する複数のデータ線６ａ同士に対して、グループ毎に供給するようにしてもよい。

また、ＴＦＴ３０のゲートに走査線３３０ａが電気的に接続されており、所定のタイミングで、走査線３３０ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。

画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板に形成された対向電極との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能とする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストをもつ光が出射する。

ここで保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。

以下では、上記データ線６ａ、走査線３３０ａ、ＴＦＴ３０等による、上述のような回路動作が実現される電気光学装置の、より具体的な構成について、図２及び図３を参照して説明する。

まず、本実施形態に係る電気光学装置は、図２のＡ－Ａ´断面図たる図３に示すように、ＴＦＴアレイ基板１０と、これに対向配置される透明な対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば、石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。

図３に示すように、ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは、例えばＩＴＯ（Indium Tin Oxide）膜等の透明

導電性膜からなる。

他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は、例えばＩＴＯ膜等の透明導電性膜からなる。

次に、図２において、電気光学装置のＴＦＴアレイ基板１０上には、マトリクス状に複数の画素電極９ａ（点線部９ａ´により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってアルミニウム膜のデータ線６ａ及びポリシリコン膜の走査線３３０ａが設けられている。

走査線３３０ａは、ポリシリコン膜の半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ´に対向するように配置されており、走査線３３０ａはゲート電極として機能する。すなわち、走査線３３０ａとデータ線６ａとの交差する箇所にはそれぞれ、チャネル領域１ａ´に走査線３３０ａの幅広部３３１ａ（後述）がゲート電極として対向配置された画素スイッチング用のＴＦＴ３０が設けられている。換言すれば、本実施形態におけるＴＦＴ３０、その中でもチャネル領域１ａ´は、マトリクス状に複数配列された画素電極９ａにおいて、その交点領域内に形成されている。ここで、交点領域とは、平面的に見て前記走査線を挟んで相隣接する画素電極９ａ間を縫って延びる長手状の第１間隙（図２中ではＸ方向）と前記データ線６ａを挟んで相隣接する画素電極９ａ間を縫って延びる長手状の第２間隙（図２中ではＹ方向）とが交わる領域である。より具体的に図２に沿って言えば、例えば、左上に示される画素電極９ａの右下角部、右上に示される画素電極９ａの左下角部、左下に示される画素電極９ａの右上角部、及び、右下に示される画素電極９ａの左上角部、のそれぞれから最も離れた位置が、それに該当することとなる。このような位置にＴＦＴ３０が形成されていることにより、該ＴＦＴ３０のチャネル領域１ａ´に対しては、直接的な光入射が生じがたい状況が現出されていることになる。

ＴＦＴ３０は、図３に示すように、ＬＤＤ（Lightly Doped Drain）構造を有しており、その構成要素としては、上述したようにゲート電極として機能する走査線３３０ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ´、走査線３３０ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁

膜２、半導体層１ａにおける低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを備えている。

なお、ＴＦＴ３０は、好ましくは図３に示したようにＬＤＤ構造をもつが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造をもってよいし、走査線３３０ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース領域及び高濃度ドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。また、本実施形態では、画素スイッチング用ＴＦＴ３０のゲート電極を、高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置して、デュアルゲート、あるいはトリプルゲート以上でＴＦＴを構成しても良い。さらに、ＴＦＴ３０を構成する半導体層１ａはポリシリコン膜に限らず、アモルファスシリコン膜や単結晶シリコン膜でも構わない。単結晶シリコン膜の形成には、貼り合わせ法等の公知の方法を用いることができる。半導体層１ａを単結晶シリコン膜とすることで、特に周辺回路の高性能化を図ることができる。

ここで本実施形態においては特に、このＴＦＴ３０のゲート電極として機能する上記走査線３３０ａは、図２に示すように、当該ゲート電極として機能する部分、すなわちＴＦＴ３０のチャネル領域１ａ´に対向して存在する部分が、他の部分に比べて幅広に形成されている。すなわち、図２において、走査線３３０ａは、図２中Ｙ方向に延在するチャネル領域１ａ´に対応するように、図２中Ｙ方向に延在する幅広部３３１ａと、隣接する画素電極９ａ間を縫うように延在する幅狭部３３２ａとを有している。図４においては、その形態が明瞭となるように、走査線３３０ａの形状パターンのみを図示している。

ちなみに、この走査線３３０ａの幅広部３３１ａは、本実施形態において、幅狭部３３２ａから延設されて形成されている。すなわち、幅広部３３１ａ及び幅狭部３３２ａは、いわば一体的に形成されているのである。このような形状は、例えば、当該幅広部３３１ａ及び幅狭部３３２ａにより形作られる一体的な形状（図４参照）を有するパターンを形成することを前提とした、公知のフォトリソグラフィ及びエッチングによって、容易に形成することが可能である。ただし、

本発明は、このような形態に限定されるものではなく、例えば、幅狭部３３２ａに対して、別途用意した別の導電性部材を接続することにより、幅広部３３１ａを形成するような形態であっても、その範囲内に収めるものである。

さて一方、図１に示した、蓄積容量７０が、図３に示すように、ＴＦＴ３０の高濃度ドレイン領域１ｅ及び画素電極９ａに接続された画素電位側容量電極としての中継層７１と、固定電位側容量電極としての容量線３００の一部とが、誘電体膜７５を介して対向配置されることにより形成されている。この蓄積容量７０によれば、画素電極９ａにおける電位保持特性を顕著に高めることが可能となる。

中継層７１は、例えば導電性のポリシリコン膜からなり画素電位側容量電極として機能する。ただし、中継層７１は、後に詳述する容量線３００と同様に、金属又は合金を含む単一層膜又は多層膜から構成してもよい。中継層７１は、画素電位側容量電極としての機能のほか、コンタクトホール８３及び８５を介して、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する機能をもつ。

このように中継層７１を利用すれば、層間距離が例えば２０００ｎｍ程度と長くても、両者間を一つのコンタクトホールで接続する技術的困難性を回避しつつ、比較的小径の二つ以上の直列なコンタクトホールで両者間を良好に接続することができ、画素開口率を高めることが可能となる。また、コンタクトホール開孔時におけるエッチングの突き抜け防止にも役立つ。

容量線３００は、例えば金属又は合金を含む導電膜からなり固定電位側容量電極として機能する。この容量線３００は、平面的に見ると、図２に示すように、走査線３３０ａの形成領域に重ねて形成されている。より具体的には容量線３００は、走査線３３０ａに沿って延びる本線部と、図中、データ線６ａと交差する各個所からデータ線６ａに沿ってＹ方向における上方に夫々突出した突出部と、コンタクトホール８５に対応する個所が僅かに括れた括れ部とを備えている。このうち突出部は、走査線３３０ａ上の領域及びデータ線６ａ下の領域を利用して、蓄積容量７０の形成領域の増大に貢献する。

また、容量線３００は、例えば、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ等の高融点金属

のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等からなり、蓄積容量７０の固定電位側容量電極としての機能のほか、ＴＦＴ３０の上側において入射光からＴＦＴ３０を遮光する遮光層としての機能をもつ。ただし、容量線３００は、例えば導電性のポリシリコン膜等からなる第１膜と高融点金属を含む金属シリサイド膜等からなる第２膜とが積層された多層構造をもってもよい。

また、容量線３００は、好ましくは、画素電極９ａが配置された画像表示領域からその周囲に延設され、定電位源と電気的に接続されて、固定電位とされる。このような定電位源としては、後述するデータ線駆動回路に供給される正電源や負電源の定電位源でもよいし、対向基板２０の対向電極２１に供給される定電位でも構わない。

誘電体膜７５は、図３に示すように、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ（High Temperature Oxide）膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄いほどよい。

図２及び図３においては、上記のほか、ＴＦＴ３０の下側に、下側遮光膜１１ａが設けられている。下側遮光膜１１ａは、格子状にパターニングされており、これにより各画素の開口領域を規定している。なお、開口領域の規定は、図２中Ｙ方向に延びるデータ線６ａと図２中Ｘ方向に延びる容量線３００とが相交差して形成されることによっても、なされている。また、下側遮光膜１１ａについても、前述の容量線３００の場合と同様に、その電位変動がＴＦＴ３０に対して悪影響を及ぼすことを避けるために、画像表示領域からその周囲に延設して定電位源に接続するとよい。

また、ＴＦＴ３０下には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、下側遮光膜１１ａからＴＦＴ３０を層間絶縁する機能のほか、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性変化を防止する機能を有する。

加えて、走査線３３０ａ上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８３がそれぞれ開孔された第１層間絶縁膜４１が形成されている。

第１層間絶縁膜４１上には、中継層７１、及び容量線３００が形成されており、これらの上には高濃度ソース領域１ｄへ通じるコンタクトホール８１及び中継層７１へ通じるコンタクトホール８５がそれぞれ開孔された第２層間絶縁膜４２が形成されている。

なお、本実施形態では、第１層間絶縁膜４１に対しては、約１０００℃の焼成を行うことにより、半導体層１ａや走査線３３０ａを構成するポリシリコン膜に注入したイオンの活性化を図ってもよい。他方、第２層間絶縁膜４２に対しては、このような焼成を行わないことにより、容量線３００の界面付近に生じるストレスの緩和を図るようにしてもよい。

第２層間絶縁膜４２上には、データ線６ａが形成されており、これらの上には中継層７１へ通じるコンタクトホール８５が形成された第３層間絶縁膜４３が形成されている。

第３層間絶縁膜４３の表面は、ＣＭＰ（Chemical Mechanical Polishing）処理等により平坦化されており、その下方に存在する各種配線や素子等による段差に起因する液晶層５０の配向不良を低減する。

ただし、このように第３層間絶縁膜４３に平坦化処理を施すのに代えて、又は加えて、ＴＦＴアレイ基板１０、下地絶縁膜１２、第１層間絶縁膜４１及び第２層間絶縁膜４２のうち少なくとも一つに溝を掘って、データ線６ａ等の配線やＴＦＴ３０等を埋め込むことにより、平坦化処理を行ってもよい。

以上説明したような構成となる本実施形態の電気光学装置によれば、上述したように、走査線３３０ａが、幅広部３３１ａ及び幅狭部３３２ａを有するとともに、前記幅広部３３１ａがＴＦＴ３０のチャネル領域１ａ´に対向するように設けられることから、ＴＦＴ３０と走査線３３０ａとの配置態様の調整・決定を容易になしうる。

例えば、既に説明を加えた図２における、ＴＦＴ３０及び走査線３３０ａの配置関係は、ＴＦＴ３０のチャネル領域１ａ´に対する光入射を効果的に防止する

という要請に応えうる好適な配置関係の一例を示すものであるが、その他にも例えば、図５及び図６等に示すような配置関係を実現することができる。ここに、図５は、図２と同趣旨の図であるが、当該図とはＴＦＴ及び走査線の配置関係が異なる態様となるもの、図６は、図４と同様に、図５に示す走査線の形状パターンのみを示す図である。

図５及び図６においては、走査線３３０ａ´、より正確には、その幅狭部３３２ａ´は、走査線３３０ａ´を挟んで相隣接する画素電極９ａ間を縫って延びる長手状の第１間隙の中央よりもずれた位置に形成されている。そして、幅広部３３１ａ´は、図５又は図６中Ｙ方向における上方にのみ突出した形として形成されている。なお、チャネル領域１ａ´の配置位置、すなわち幅広部３３１ａ´の配置位置は、図２と異ならない。

このような配置関係となる場合、まず第１に、表示画像の品質向上を図ることができる。これは以下の事情による。すなわち、本実施形態に係る電気光学装置では、上述したように、画素電極９ａ上に配向膜１６が設けられているが、この配向膜１６の表面には一般に、該配向膜１６下に形成される各種構成要素の「高さ」に起因した凹凸が存在する場合がある。ここにいう「各種構成要素」の中には、本形態に係る走査線３３０´ａも含まれる。図７は、図５におけるＢ－Ｂ’線に沿った断面図を示しており、該走査線３３０ａ´の幅狭部３３２ａ´の「高さ」に起因した凸部５０１が、配向膜１６上に形成されている様子が示されている。

しかしながら、このような凸部５０１が生じると、配向膜１６に対して実施される上述したラビング処理にムラを生じさせるおそれがある。このムラは、液晶の配向不良等を招来し、電気光学装置の動作不良の原因となる場合がある。したがって、従来においては、上述のような凸部５０１付近に、遮光膜を設けることで入射光を遮蔽すること、すなわち、当該遮光膜に到達した入射光は、該遮光膜により反射又は吸収されることで画像表示に寄与しないこと等が行われていた。

この際問題となるのは、画素開口率の向上という要請を満たしながら、上述の遮光膜を設けなければならないことにある。すなわち、凸部５０１に対応するように、ただ単に遮光膜を設けるのでは、徒に画素開口率を低下させることにな

り、画像の明るさを損なう。といって、凸部５０１のごく一部にだけ遮光膜を設けるのでは、十分な遮光を行うことができずコントラスト比の低下を招くことになるほか、該凸部５０１における前記ムラの影響を受けて、電気光学装置の動作不良等を招くことになる。

ここで、本実施形態では、凸部５０１に上述したようなムラが生じること、より進んで、前記凸部５０１において、ラビングの擦り上げ（すなわち、凸部５０１を登る方向）に係る部分（図７における符号５０１ａ。以下「擦り上げ部５０１ａ」と称す。）と擦り下げ（すなわち、凸部５０１を下る方向）に係る部分（図７における符号５０１ｂ。以下「擦り下げ部５０１ｂ」と称す。）とでは、前記ムラの程度に差があることに着目する。

より具体的には、例えば、前記擦り上げ部５０１ａの方が、前記擦り下げ部５０１ｂよりも、前記ムラが生じにくいこと、つまり、擦り下げ部５０１ｂの方が、液晶の配向不良等を招来する可能性が高いことに着目する。

ここで、本実施形態においては、図５における走査線３３０ａ´方向に隣接する幅狭部３３２ａ´が、画素電極間９ａ間の中央（図７における二点鎖線参照）から外れた位置に形成されていることが意味を帯びる。すなわち、幅狭部３３２ａ´を図７に示すような位置に形成することによれば、該幅狭部３３２ａ´に起因する凸部５０１の頂点５０１Ｐもまた、隣接する画素電極間９ａ間の中央から外れた位置に形成されることになり、このことは、当該第１間隙に対応する領域上に、当該凸部５０１のほぼ半斜面だけを存在させるような構成を採ること、すなわち該領域上に、前記擦り下げ部５０１ｂだけを存在させるような構成を採ることが可能であることを意味する。そして、この場合において、遮光性の容量線３００及び中継層７１を、図７に示すように、前記隣接する画素電極間９ａ間に対応するように設ければ、前記擦り下げ部５０１ｂだけを有効に遮光すること、つまりムラの影響が最も生じると考えられる凸部５０１の当該部分を有効に遮光することが可能となるのである。

以上の結果、本形態によれば、ムラの影響による電気光学装置の動作不良等を生じさせることが殆どなく、また、ムラの影響がより生じにくいと考えられる凸部５０１ａの擦り上げ部５０１ａは、画像表示に寄与する光を透過可能のままに

しておくことになるから、画素開口率の向上、すなわち画像は明るいままこれを維持することが可能となるのである。結局、本形態によれば、以上述べたような意味において、表示画像の品質向上が図られることになるのである。

また、幅狭部３３２ａ´を、第１間隙の中央よりもずれた位置に形成することによれば、第２に、電気光学装置の設計の自由度を向上すること、また、ＴＦＴ３０に対する光入射をより効果的に防止することができる。これは以下の事情による。

すなわち、本形態における幅狭部３３２ａ´は、隣接する画素電極９ａ間の第１間隙を縫うようには存在するが、その中央には存在しない。このため例えば、第１間隙の領域中、幅狭部３３２ａ´が設けられていない領域を利用することにより、平面的にみて、該幅狭部３３２ａ´に平行に該幅狭部３３２ａ´と同一膜から構成された容量線３００等の他の配線を配線することが可能となる。すなわち、設計の自由度が増大するのである。

また、上述のような場合に、幅狭部３３２ａ´は中央線からはずれているものの、幅広部３３１ａ´はその幅広の程度を調整することにより、例えば、一方側のみを幅広に広げたり、一方側を大きく幅広に且つ他方側を小さく幅広にすることで、ゲート電極としての幅広部３３１ａ´を、間隙の中央に配置させることが可能となる。本形態においては、図５及び図６に示すように、幅広部３３１ａ´は、一方側のみに広げられていることがわかる。このように、走査線３３０ａ´の位置によらずにゲート電極の配置を遮光性を高めるのに都合の良い位置に配置できるので、或いはゲート電極の配置を遮光性を高めるのに都合の良い位置に配置しながら、走査線３３０ａ´の配置を間隙内における任意の位置に配置できるので、最終的には、走査線３３０ａ´の配置を含めた配線配置の自由度を高めつつ遮光性が本質的に高いＴＦＴ３０を実現できるのである。

要するに、図５及び図６に示す形態によれば、表示画像の品質向上、設計の自由度向上及びＴＦＴ３０における光リーク電流の低減等の要請を達成しながら、チャネル領域１ａ´ないしＴＦＴ３０と、ゲート電極ないし走査線３３０ａ´との配置関係を好適に調整・決定することができることになる。

以上述べたように、本実施形態に係る電気光学装置によれば、走査線がゲート

電極としての幅広部及び幅狭部を有することにより、上述した各種要請や電気光学装置それ自体の高精細化といった一般的要請等に応えながら、チャネル領域ないしＴＦＴと、ゲート電極ないし走査線との配置関係を好適に調整・決定することができるのである。

（第２実施形態）

以下では、本発明の第２の実施形態について、図８乃至図１１を参照しながら説明する。ここに図８及び図１０はそれぞれ、図２と同趣旨の図であって、同図とはＴＦＴアレイ基板１０上に溝が形成されている点及び該溝内に走査線の少なくとも一部が埋め込まれている点等について異なる態様を示すものであり、図９及び図１１はそれぞれ、第２実施形態に係る走査線の幅狭部における形態について、その断面の様子とともに示す斜視図である（図９は、図８に対応しており、図８中におけるＺ１－Ｚ１´線での断面が、図９中におけるＺ１－Ｚ１´断面に対応している。また、図１１は、図１０に対応しており、図１０中におけるＺ２－Ｚ２´線での断面が、図９中におけるＺ２－Ｚ２´断面に対応している。）。また、図１２は、図１０のＴ－Ｔ´断面図である。なお、第２実施形態の電気光学装置の基本的な構成及び作用等は上記第１実施形態と同様であるので、以下では、第２実施形態において特徴的な部分について主に説明を加えることとする。また、図８及び図１２で使用する符号は、実質的に同一の要素を指し示す場合においては、前述までに参照した図１乃至図７において使用した符号と同一のものを使用することとする。

まず、第２実施形態の一態様では、図８及び図９に示すように、ＴＦＴアレイ基板１０に走査線方向に沿って溝３Ｇ１が形成されている。この溝３Ｇ１は、ＴＦＴ３０の半導体層１ａが形成されている領域を除いて形成されている。これにより、溝３Ｇ１は、それのみに着目すると、平面視してマトリクス状に配列されるように形成されていることになる（図８参照）。そして、走査線３４０ａは、その幅狭部３４２ａがこの溝３Ｇ１内にいわば完全に埋め込まれるようにして形成されている（図９参照）。

他方、第２実施形態の他の態様では、図１０及び図１１に示すように、前記溝３Ｇ１と略同様に、ＴＦＴアレイ基板１０上に溝３Ｇ２が形成されている。ただ

し、この溝３Ｇ２は、前記溝３Ｇ１に比べて、若干狭く形成することが好ましい。そして、走査線３５０ａは、その幅狭部３５２ａがこの溝３Ｇ２に沿って形成されている。幅狭部３５２ａは、その一部が溝３Ｇ２内に埋め込まれた埋め込み部３５２ａＢと、該埋め込み部３５２ａＢと平行して延在し溝３Ｇ２に埋め込まれない非埋め込み部３５２ａＮＢとを有している。このうち非埋め込み部３５２ａＢは、ＴＦＴアレイ基板１０の表面上に形成されることになる。

なお、第２実施形態の一態様及び他の態様においては、図８及び図１０に示すように、ＴＦＴアレイ基板１０にデータ線方向に沿って溝６Ｇ１が形成されている。そして、データ線６ａは、この溝６Ｇ１内にいわば完全に埋め込まれるようにして形成されている。加えて、溝６Ｇ１には半導体層１ａもいわば完全に埋め込まれるようにして形成されている。

このような構成を擁する第２実施形態の電気光学装置によれば、次のような作用効果が奏されることとなる。まず、走査線３４０ａ及び３５０ａのいずれについても、溝３Ｇ１又は３Ｇ２にその全部又は一部が埋め込まれていることから、図９及び図１１に示すように、この埋め込み部分においては、下地絶縁膜１２と走査線３４０ａ及び走査線３５０ａの埋め込み部３５２ａＢの表面高さがほぼ同じで平坦性が維持されている。これにより、当該走査線３４０ａ及び３５０ａの上層として形成される第１乃至第３層間絶縁膜４１乃至４３、或いは画素電極９ａ及び配向膜１６の平坦性も良好に確保され得ることになる。したがって、第２実施形態によれば例えば、配向膜１６の表面には前記幅狭部３４２ａ又は前記埋め込み部３５２ａＢに沿うような段差は殆ど生じないから、該配向膜１６に対するラビング処理を好適に実施することができ、配向不良等を殆ど発生させることがなく、更には、該配向不良を原因とする光抜け及びこれに基づく画質劣化等をほとんど発生させることもないという作用効果が得られることになる。

このような作用効果は、溝６Ｇ１の存在により、データ線６ａに沿う部分についても同様に得られる。

また、図１０及び図１１においては特に、非埋め込み部３５２ａＮＢが存在することにより、次のような作用効果が得られる。以下、これを詳しく説明する。

まず、本実施形態のような電気光学装置では、一般に、直流電圧印加による電

気光学物質の劣化防止、表示画像におけるクロストークやフリッカの防止などのために、各画素電極９ａに印加される電圧極性を所定規則で反転させる反転駆動方式が採用される場合がある。より具体的に、いわゆる「１Ｈ反転駆動方式」について説明すると、次のようである。

まず、図１３（ａ）に示すように、ｎ（但し、ｎは自然数）番目のフィールド或いはフレームの画像信号を表示する期間中には、画素電極９ａ毎に＋又は－で示す液晶駆動電圧の極性は反転されず、行毎に同一極性で画素電極９ａが駆動される。その後図１３（ｂ）に示すように、ｎ＋１番目のフィールド或いは１フレームの画像信号を表示するに際し、各画素電極９ａにおける液晶駆動電圧の極性は反転され、このｎ＋１番目のフィールド或いは１フレームの画像信号を表示する期間中には、画素電極９ａ毎に＋又は－で示す液晶駆動電圧の極性は反転されず、行毎に同一極性で画素電極９ａが駆動される。そして、図１３（ａ）及び図１３（ｂ）に示した状態が、１フィールド又は１フレームの周期で繰り返される。これが、１Ｈ反転駆動方式による駆動である。この結果、直流電圧印加による液晶の劣化を避けつつ、クロストークやフリッカの低減された画像表示を行える。尚、１Ｈ反転駆動方式によれば、後述する１Ｓ反転駆動方式と比べて、図中縦方向（Ｙ方向）のクロストークが殆ど無い点で有利である。

ところが、図１３（ａ）及び図１３（ｂ）から分かるように、１Ｈ反転駆動方式では、図中縦方向（Ｙ方向）に相隣接する画素電極９ａ間で横電界が発生することになる。これらの図では、横電界の発生領域Ｃ１は常時、Ｙ方向に相隣接する画素電極９ａ間の間隙付近となる。このような横電界が印加されると、相対向する画素電極と対向電極との間の縦電界（即ち、基板面に垂直な方向の電界）の印加が想定されている電気光学物質に対して、液晶の配向不良の如き電気光学物質の動作不良が生じ、この部分における光抜け等が発生してコントラスト比が低下してしまうという問題が生じる。

これに対し、横電界が生じる領域を遮光膜により覆い隠すことは可能であるが、これでは横電界が生じる領域の広さに応じて画素の開口領域が狭くなってしまうという問題点が生じる。特に、画素ピッチの微細化により相隣接する画素電極間の距離が縮まるのに伴って、このような横電界は大きくなるため、これらの

問題は電気光学装置の高精細化が進む程深刻化してしまう。

しかるに、第２実施形態中、前記の図１０及び図１１に示す形態においては、非埋め込み部３５２ａＮＢの高さに起因した段差が、縦方向に相隣接する画素電極９ａ（即ち、逆極性の電位が印加される相隣接する画素電極９ａ）の間に形成されることになる。この段差の存在によれば、該段差上に配置された画素電極９ａの縁付近における縦電界を強めると共に横電界を弱めることが可能となる。より具体的には、図１２に示すように、段差４３０上に配置された画素電極９ａの縁付近と対向電極２１との距離を段差４３０の高さの分だけ狭める。従って、図１３に示した横電界の発生領域Ｃ１において、画素電極９ａと対向電極２１との間における縦電界を強めることができるのである。そして、図１２において、相隣接する画素電極９ａ間の間隙は一定であるため、間隙が狭まる程に強まる横電界の大きさも一定である。よって、図１３に示した横電界の発生領域Ｃ１において、縦電界をより支配的にすることにより、横電界による液晶の配向不良を防止できるのである。更に、絶縁膜からなる段差４３０の存在により、横電界の強度も弱められると共に、横電界が存在する段差４３０に置き換えられた分だけ横電界の影響を受ける液晶部分が減るので、当該横電界の液晶層５０に対する作用を減ずることができる。

なお、上述では、１Ｈ反転駆動について説明したが、本発明は、このような駆動方式に限定して適用されるものではない。例えば、同一列の画素電極を同一極性の電位により駆動しつつ、係る電圧極性を列毎にフレーム又はフィールド周期で反転させる１Ｓ反転駆動方式も、制御が比較的容易であり高品位の画像表示を可能ならしめる反転駆動方式として用いられているが、本発明は、これに対して適用可能である。更に、列方向及び行方向の両方向に相隣接する画素電極間で、各画素電極に印加される電圧極性を反転させるドット反転駆動方式も開発されているが、本発明は、これに対しても適用することが可能であることは言うまでもない。

なお、第２実施形態においては、幅狭部３４２ａ及び３５２ａが、図２に示したように、相隣接する画素電極９ａ間の第１間隙の中央を縫うようにして形成されている態様について説明したが、本発明は、このような形態に限定されるもの

ではない。すなわち、図５及び図６に示したように、幅狭部を前記第１間隙の中央から外れた位置に延在するように形成する態様において、図８から図１１に示したような溝３Ｇ１又は３Ｇ２を併せもつ形態としてよい。このようなものとしては例えば、図１４及び図１５に示すような形態を採用することが可能である。ここに図１４は、図２と同趣旨の図であって、同図とはＴＦＴアレイ基板１０上に溝が形成されている点及び走査線の幅狭部が第１間隙の中央から外れて形成されている点等について異なる態様を示すものであり、図１５は、図１４のＴ－Ｔ´断面図である。

図１４において、走査線３６０ａは、図５及び図６と比べて、幅狭部３６２ａが相隣接する画素電極９ａ間を縫って延びる長手状の第１間隙の中央よりもずれた位置に形成されている点は同じであるが、幅狭部３６２ａがＴＦＴアレイ基板１０上に形成された溝３Ｇ１´に沿って形成されている点、また、幅広部３６１ａが、図１４中下方にのみ突出した形として形成されている点が異なっている。これにより、当該走査線３６０ａの幅狭部３６２ａは、第１間隙の中央からみて図中上方よりに形成されることとなり、したがって、該幅狭部３６２ａは、画素電極９ａと中継層７１とを接続するためのコンタクトホール８５の直下に位置するように形成されることになる。なお、この幅狭部３６２ａは、溝３Ｇ１´内に完全に埋め込まれるようにして形成されている。

このような構成によると、図１５に示されるように、コンタクトホール８５は、溝３Ｇ１´内に埋め込まれて形成された走査線３６０ａの上に形成されることになる。言い換えると、コンタクトホール８５は、走査線３６０ａの高さに起因した段差が殆ど生じていない第３層間絶縁膜４３の表面を前提として形成することが可能となる。

ちなみに、このような図１４及び図１５に示す形態においては特に、コンタクトホール８５の形成を比較的容易且つ確実に行うことができるという利点が得られる。すなわち、仮に幅狭部ないし走査線の高さに起因する段差が第３層間絶縁膜４３の表面に現れる場合を仮定すると、コンタクトホール８５の形成は、当該段差の頂上或いはその稜面上に対して行わなければならないという不具合を被る可能性がある。本形態では、このような不利益を被らなくて済むのである。

このような作用効果は、次のような観点から捉えることもできる。すなわち、第２実施形態においては、走査線の全部又は一部が溝内に埋め込まれることにより、該走査線の高さを起因とした段差が各層間絶縁膜の表面上には殆ど生じないことになるから、走査線の形成位置、或いは延在位置について特に注意を払う必要がない、換言すれば、走査線方向の隣接する画素電極間であればどこに形成してもよいということができるのである。走査線の形成位置、或いは延在位置を自由に選択し、且つその上にコンタクトホール等を形成する場合であっても、上述のように、該コンタクトホール等の形成は、前記段差が存在しないことにより、比較的容易且つ確実に行うことができるからである。

なお、幅狭部が埋め込み部及び非埋め込み部からなる場合においては、そのうちの埋め込み部側がコンタクトホール８５の直下に位置するように、溝を形成すると好ましい。前述した図１２は、このような形態の一例に該当する。

（第３実施形態）

以下では、本発明の第３の実施形態について、図１６乃至図１９を参照しながら説明する。ここに図１６は、図２と同趣旨の図であって、同図とはデータ線の形態が異なるものを示す図であり、図１７は図１６のＰ－Ｐ´断面図であり、図１８は図１６のＱ－Ｑ´断面図であり、図１９は図１６のＲ－Ｒ´断面図である。なお、第３実施形態の電気光学装置の基本的な構成及び作用等は上記第１実施形態と同様であるので、以下では、第３実施形態において特徴的な部分について主に説明を加えることとする。また、図１６乃至図１９で使用する符号は、実質的に同一の要素を指し示す場合においては、前述までに参照した図１乃至図１５において使用した符号と同一のものを使用することとする。

第３実施形態では、図１６乃至図１９に示すように、データ線６ａ１は、ＴＦＴ３０に重なる部分が局所的に幅広に形成された幅広部６ａＷを備えている。そして、容量線３００におけるデータ線６ａ１に沿って延びる部分、すなわち突出部３０２の幅Ｗ１は、第一に、データ線６ａ１における幅広部６ａＷ以外の部分の幅Ｗ２´より広く形成されている（特に、図１７参照）。そして第二に、該突出部３０２の幅Ｗ１は、データ線６ａ１における幅広部６ａＷの幅Ｗ６とほぼ同一に形成されている（図１８参照）。半導体層１ａのチャネル領域１ａ´は、こ

の幅広部６ａＷの幅方向のほぼ中央に位置するとともに、走査線３ａの幅方向のほぼ中央に位置する。さらに、第３実施形態では、図１６或いは図１８及び図１９に示すように、データ線６ａ１の幅広部６ａＷは、マトリクス状に配列されたＴＦＴ３０ごとに、該ＴＦＴ３０に重なる部分から該ＴＦＴ３０の半導体層１ａとデータ線６ａとを接続するコンタクトホール８１が設けられた部分まで連続している。加えて、第３実施形態では、図１７乃至図１９に示すように、対向基板２０上に遮光膜２３が形成されている。そして、この遮光膜２３の一本一本の格子の幅ＷＳは、前記の幅広部６ａＷよりも大きくされている。

このような構成となる第３実施形態の電気光学装置では、次のような作用効果が得られることになる。すなわち、第一に、ＴＦＴ３０上には、いずれも幅広に形成されたデータ線６ａ１の幅広部６ａＷ及び容量線３００の突出部３０２が存在することにより、いわば二重の遮光作用が得られることになる。したがって、ＴＦＴ３０のチャネル領域１ａ´に対する光入射は、前記の実施形態にも増して生じ難く、よって、光リーク電流も発生し難い。

特に、第３実施形態においては、ＴＦＴ３０上に、このような容量線３００に重ねて、データ線６ａの幅広部６ａＷもまた存在する。この場合、ＴＦＴ３０上では、これらの透過率の積算値に該当する遮光性能を得ることができる。また、半導体層１ａのチャネル領域１ａ´は、幅広部６ａＷの幅方向のほぼ中央に位置するとともに、走査線３ａの幅方向のほぼ中央に位置することから、遮光性能はよりよく享受できる。

第二に、このような優れた遮光性能に関連して更に、第３実施形態においては、上述のように、容量線３００の突出部３０２の幅Ｗ１及びデータ線６ａの幅広部６ａＷの幅Ｗ６は、対向基板２０上の遮光膜２３の幅ＷＳよりも小さく（即ち、ＷＳ＜Ｗ１、ＷＳ＜Ｗ６）されている。これによると、ＴＦＴ３０の上方から入射する光は、まず、遮光膜２３で遮られるか、或いはこれを通過しても、次なるデータ線６ａの幅広部６ａＷで遮られる。更に、入射光が、この幅広部６ａＷを通過しても、次なる容量線３００の突出部３０２によって遮られることになる。要するに、第３実施形態においては、三重の遮光が実現されることになるから、ＴＦＴ３０に対する光入射は更に生じ難い状況にある。

更に第三に、第３実施形態では、データ線６ａの幅広部６ａＷが、マトリクス状に配列されたＴＦＴ３０ごとに、ＴＦＴ３０に重なる部分からコンタクトホール８１に至るまで連続して形成されている。ここで、このコンタクトホール８１は、前述のようにＴＦＴ３０の半導体層１ａとデータ線６ａとを接続するために設けられているから、当該部分においては、容量線３００を形成することができないが、第３実施形態では、このコンタクトホール８１の形成部位において、ＴＦＴ３０の上方と同様に、データ線６ａの幅広部６ａＷが存在している。したがって、容量線３００を形成することができない分、被り得る遮光性能の低下は、この幅広部６ａＷの存在によって補うことが可能となる。ちなみに、第３実施形態のように、ＴＦＴ３０上及びコンタクトホール８１の形成部位の幅広部６ａを連続するように形成する態様によれば、幅広部６ａＷの形成領域をむやみに広げないで済むので、内面反射を増大させない観点から好ましい。

以上のように、第３実施形態においては、各種の作用効果が相俟って、チャネル領域１ａ´に対する光入射の可能性は極めて減退されており、ＴＦＴ３０における光リーク電流発生、ひいては該光リーク電流を起因とする画像上のフリッカ等の発生は有効に抑制されることになる。

（電気光学装置の全体構成）

以上のように構成された本実施形態に係る電気光学装置の全体構成を、図２０及び図２１を参照して説明する。なお、図２０は、ＴＦＴアレイ基板をその上に形成された各構成要素とともに対向基板２０の側からみた平面図であり、図２１は図２０のＨ－Ｈ´断面図である。

図２０及び図２１において、本実施形態に係る電気光学装置では、ＴＦＴアレイ基板１０と対向基板２０とが対向配置されている。ＴＦＴアレイ基板１０と対向基板２０との間には、液晶層５０が封入されており、ＴＦＴアレイ基板１０と対向基板２０とは、画像表示領域１０ａの周囲に位置するシール領域に設けられたシール材５２により相互に接着されている。

シール材５２の外側の領域には、データ線６ａに画像信号を所定のタイミングで供給することにより該データ線６ａを駆動するデータ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、

走査線３ａに走査信号を所定のタイミングで供給することにより、走査線３ａを駆動する走査線駆動回路１０４が、この一辺に隣接する二辺に沿って設けられている。

なお、走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでもよいことは言うまでもない。また、データ線駆動回路１０１を画像表示領域１０ａの辺に沿って両側に配列してもよい。

ＴＦＴアレイ基板１０の残る一辺には、画像表示領域１０ａの両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも一箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的に導通をとるための導通材１０６が設けられている。そして、図２１に示すように、図２０に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。

図２１において、ＴＦＴアレイ基板１０上には、画素スイッチング用のＴＦＴや走査線、データ線等の配線が形成された後の画素電極９ａ上に、配向膜が形成されている。他方、対向基板２０上には、対向電極２１のほか、最上層部分に配向膜が形成されている。また、液晶層５０は、例えば一種又は数種類のネマティク液晶を混合した液晶からなり、これら一対の配向膜間で、所定の配向状態をとる。

なお、ＴＦＴアレイ基板１０上には、これらのデータ線駆動回路１０１、走査線駆動回路１０４等に加えて、複数のデータ線６ａに画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線６ａに所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等を形成してもよい。

（電子機器の実施形態）

次に、以上詳細に説明した電気光学装置をライトバルブとして用いた電子機器の一例たる投射型カラー表示装置の実施形態について、その全体構成、特に光学的な構成について説明する。ここに、図２２は、投射型カラー表示装置の図式的

断面図である。

図２２において、本実施形態における投射型カラー表示装置の一例たる液晶プロジェクタ１１００は、駆動回路がＴＦＴアレイ基板上に搭載された液晶装置を含む液晶モジュールを３個用意し、それぞれＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロックミラー１１０８によって、ＲＧＢの三原色に対応する光成分Ｒ、Ｇ及びＢに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにそれぞれ導かれる。この際特に、Ｂ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂによりそれぞれ変調された三原色に対応する光成分は、ダイクロックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨、あるいは思想に反しない範囲で適宜変更可能であり、そのような変更を伴う電気光学装置、例えば、電気泳動装置やエレクトロルミネッセンス表示装置や、それら電気光学装置を含む及び電子機器もまた、本発明の技術的範囲に含まれるものである。

What is claim is:

1．電気光学装置であって、

基板上に、一定の方向に延びる走査線及び該走査線に交差する方向に延びるデータ線と、前記走査線及び前記データ線の交差領域に対応して設けられた薄膜トランジスタと、該薄膜トランジスタに対応して設けられた画素電極とを備え、

前記走査線は、前記薄膜トランジスタのチャネル領域に対向する部分にゲート電極としての幅広部を有するとともに他の部分に幅狭部を有していることを特徴とする。

2．クレーム１の電気光学装置であって、

前記幅広部は、前記幅狭部から延設されて形成されている部分を含むことを特徴とする。

3．クレーム１の電気光学装置であって、

前記幅広部は、前記幅狭部に接続されて形成されている部分を含むことを特徴とする。

4．クレーム１の電気光学装置であって、

前記走査線は、前記チャネル領域の延在する方向と交わる方向に延在しており、前記幅広部は、当該チャネル領域の延在する方向の一方又は両方に延在していることを特徴とする。

5．クレーム１の電気光学装置であって、

前記画素電極は、マトリクス状の配列がなされてなり、

前記チャネル領域は、平面的に見て前記走査線を挟んで相隣接する画素電極間を縫って延びる長手状の第１間隙と、前記データ線を挟んで相隣接する画素電極間を縫って延びる長手状の第２間隙とが交わる交点領域内に形成されていることを特徴とする。

6．クレーム５の電気光学装置であって、

前記幅狭部は、前記第１間隙の中央よりもずれた位置に形成され、

前記幅広部は、前記交点領域内において前記第１間隙の中央に形成されていることを特徴とする。

７．クレーム６の電気光学装置であって、

前記幅広部は、前記交点領域内において前記第２間隙の中央に形成されていることを特徴とする。

８．クレーム１の電気光学装置であって、

前記基板には、前記走査線に沿って溝が掘られており、前記走査線は該溝内に直接又は層間絶縁膜を介して少なくとも部分的に埋め込まれていることを特徴とする。

９．クレーム８の電気光学装置であって、

前記幅狭部は、前記溝内に埋め込まれているとともに前記走査線に沿って延びる埋め込み部分と、前記溝内に埋め込まれないとともに前記埋め込み部と並んで前記走査線に沿って延びる非埋め込み部分とを有し、

該非埋め込み部分の存在によって、前記画素電極の下地は、前記走査線に沿って盛り上がっていることを特徴とする。

１０．クレーム１の電気光学装置であって、

前記画素電極に接続されており蓄積容量を構成する画素電位側容量電極と、

該画素電位側容量電極に誘電体膜を介して対向配置されており前記蓄積容量を構成する固定電位側容量電極を含む容量線とを更に備えてなり、

前記容量線は、前記走査線に沿って延びる本線部と前記データ線に沿って延びる部分とを有し、

前記容量線における前記データ線に沿って延びる部分の幅は、当該データ線の幅と同一又はより広く形成されていることを特徴とする。

１１．クレーム１０の電気光学装置であって、

前記データ線は、前記薄膜トランジスタに重なる部分が局所的に幅広に形成されており、

前記容量線における前記データ線に沿って延びる部分の幅は、

前記データ線における幅広に形成されていない部分の幅より広く且つ前記データ線における前記幅広に形成された部分の幅と同一に形成されていることを特徴とする。

１２．クレーム１１の電気光学装置であって、

前記容量線は、前記薄膜トランジスタと前記データ線との間の積層位置に配置されており、

前記データ線は、前記薄膜トランジスタに重なる部分に加えて、前記薄膜トランジスタとの接続用のコンタクトホールが設けられた部分が、幅広に形成されていることを特徴とする。

１３．クレーム１１の電気光学装置であって、

前記データ線は、前記薄膜トランジスタごとに、前記薄膜トランジスタに重なる部分から前記コンタクトホールが設けられた部分までが連続して幅広に形成されていることを特徴とする。

１４．クレーム１０の電気光学装置であって、

前記データ線は、前記薄膜トランジスタに重なる部分が局所的に幅広に形成されており、

前記容量線における前記データ線に沿って延びる部分の幅は、

前記データ線における幅広に形成されていない部分の幅より広く且つ前記データ線における前記幅広に形成された部分の幅より狭く形成されていることを特徴とする。

１５．クレーム１４の電気光学装置であって、

前記容量線は、前記薄膜トランジスタと前記データ線との間の積層位置に配置されており、

前記データ線は、前記薄膜トランジスタに重なる部分に加えて、前記薄膜トランジスタとの接続用のコンタクトホールが設けられた部分が、幅広に形成されていることを特徴とする。

１６．クレーム１４の電気光学装置であって、

前記データ線は、前記薄膜トランジスタごとに、前記薄膜トランジスタに重なる部分から前記コンタクトホールが設けられた部分までが連続して幅広に形成されていることを特徴とする。

１７．クレーム１の電気光学装置であって、

前記基板に電気光学物質を介して対向配置された他の基板と、

該他の基板上に形成された遮光膜とを更に備えてなり、

前記データ線及び前記容量線における前記データ線に沿って延びる部分の幅は、前記遮光膜の幅よりも狭いことを特徴とする。

１８．電子機器であって、

前記電子機器は、電気光学装置を備え、

前記電気光学装置は、

基板上に、一定の方向に延びる走査線及び該走査線に交差する方向に延びるデータ線と、前記走査線及び前記データ線の交差領域に対応して設けられた薄膜トランジスタと、該薄膜トランジスタに対応して設けられた画素電極とを備え、

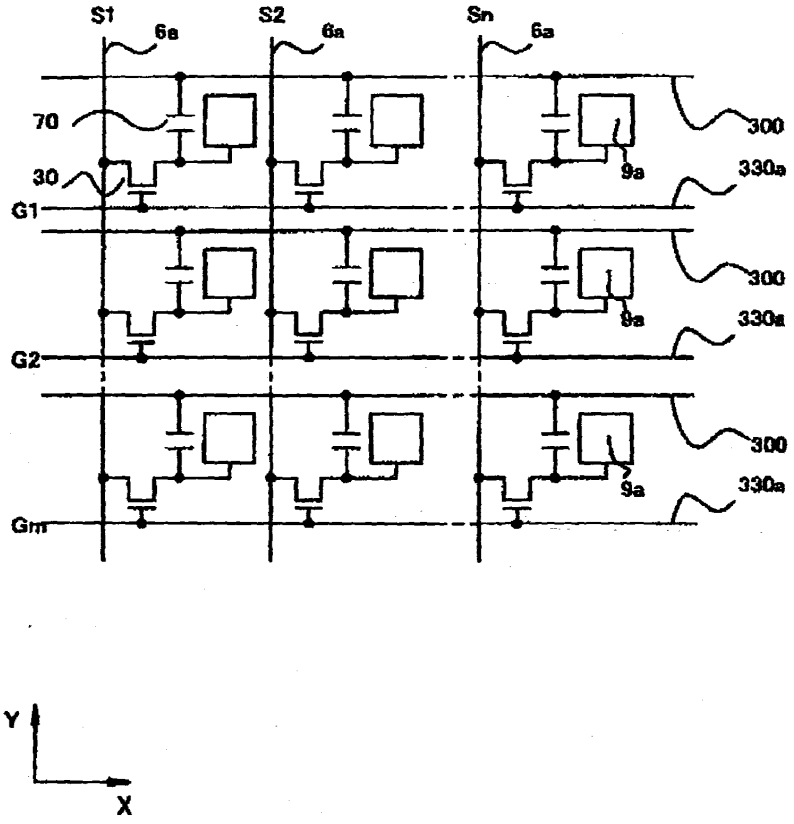
前記走査線は、前記薄膜トランジスタのチャネル領域に対向する部分にゲート電極としての幅広部を有するとともに他の部分に幅狭部を有していることを特徴とする。

ABSTRACT OF THE DISCLOSURE

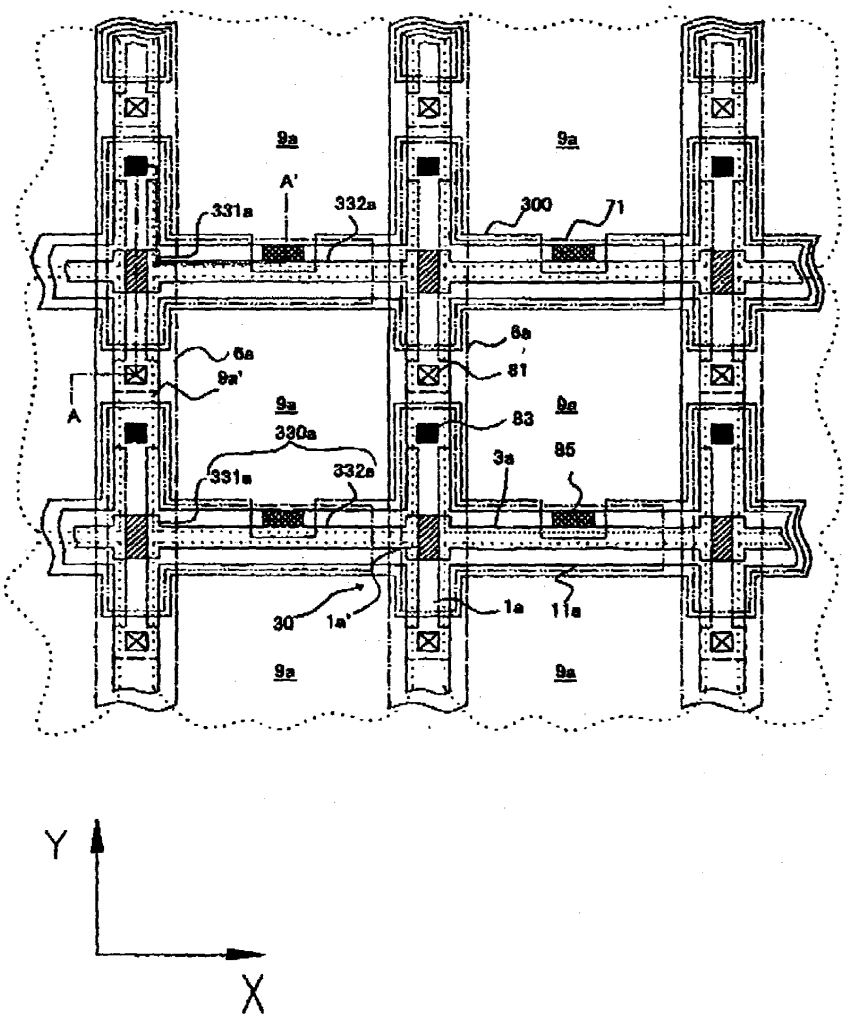
本発明の電気光学装置は、ＴＦＴアレイ基板上に、画素電極とこれに接続されたＴＦＴ、このＴＦＴに接続された走査線及びデータ線を備え、前記走査線は、前記ＴＦＴのチャネル領域に対向する部分にゲート電極としての幅広部を有するとともに他の部分に幅狭部を有している。

これにより、ゲート電極及び走査線の配置関係の調整がより容易に実現されるとともに、ＴＦＴの正確な駆動が可能とされた電気光学装置を提供する。

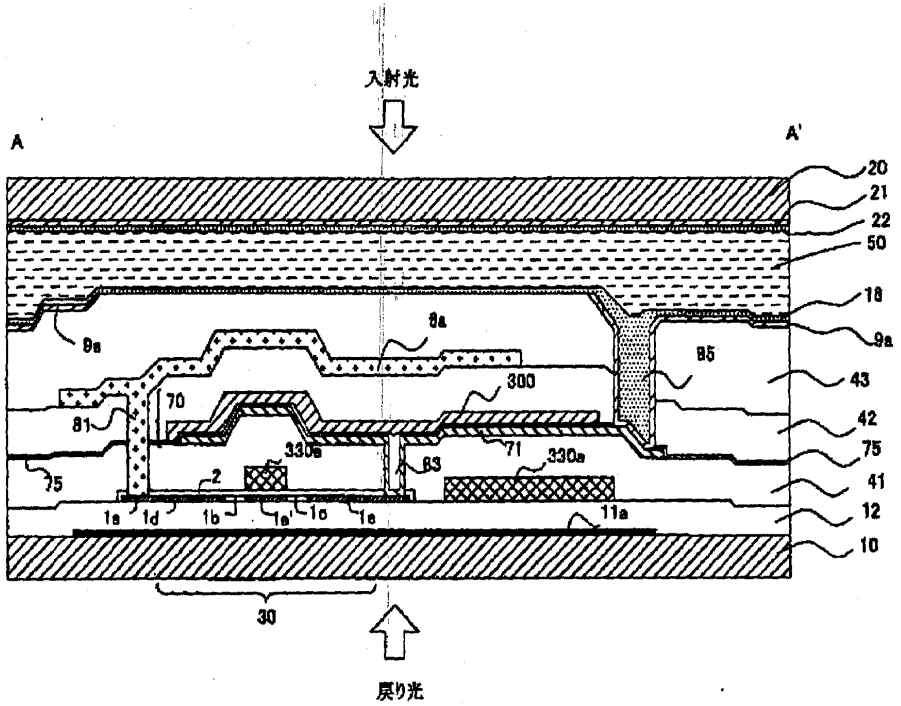
【図1】


S1
6a
S2
6a
Sn
6a
70
30
G1
G2
Gm
300
9a
330a
300
9a
330a
300
9a
330a
Y
X

【図２】

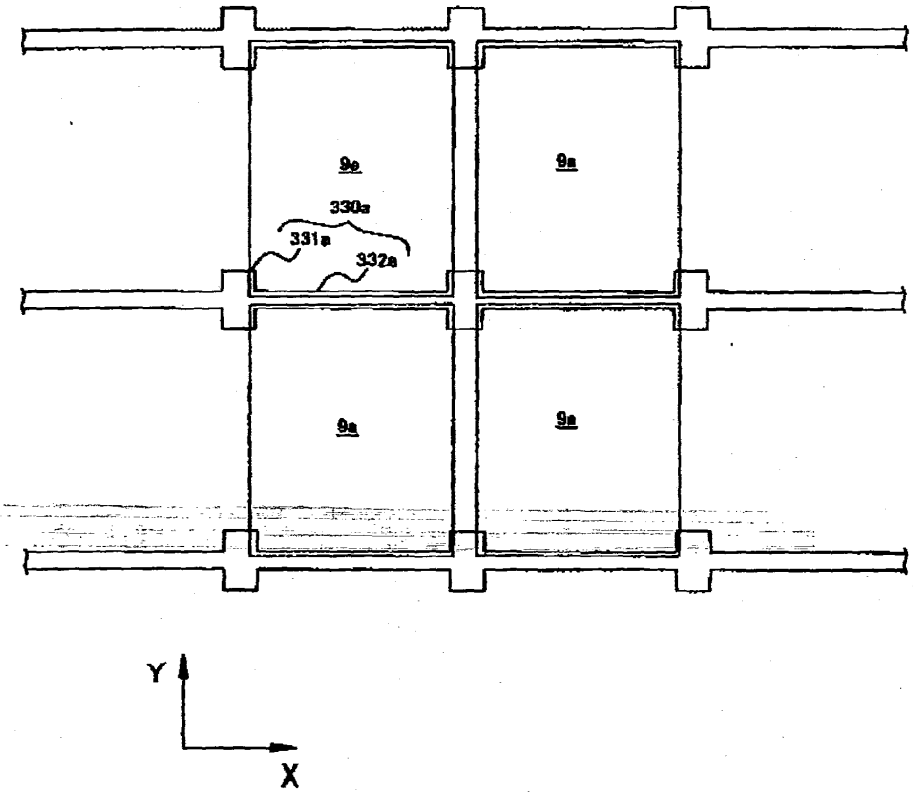

9a
A'
331a
332a
300
71
6a
9a'
A
9a
330a
331a
332a
6a
81
83
9a
85
3a
30
1a'
1a
11a
9a
9a
Y
X

【図３】

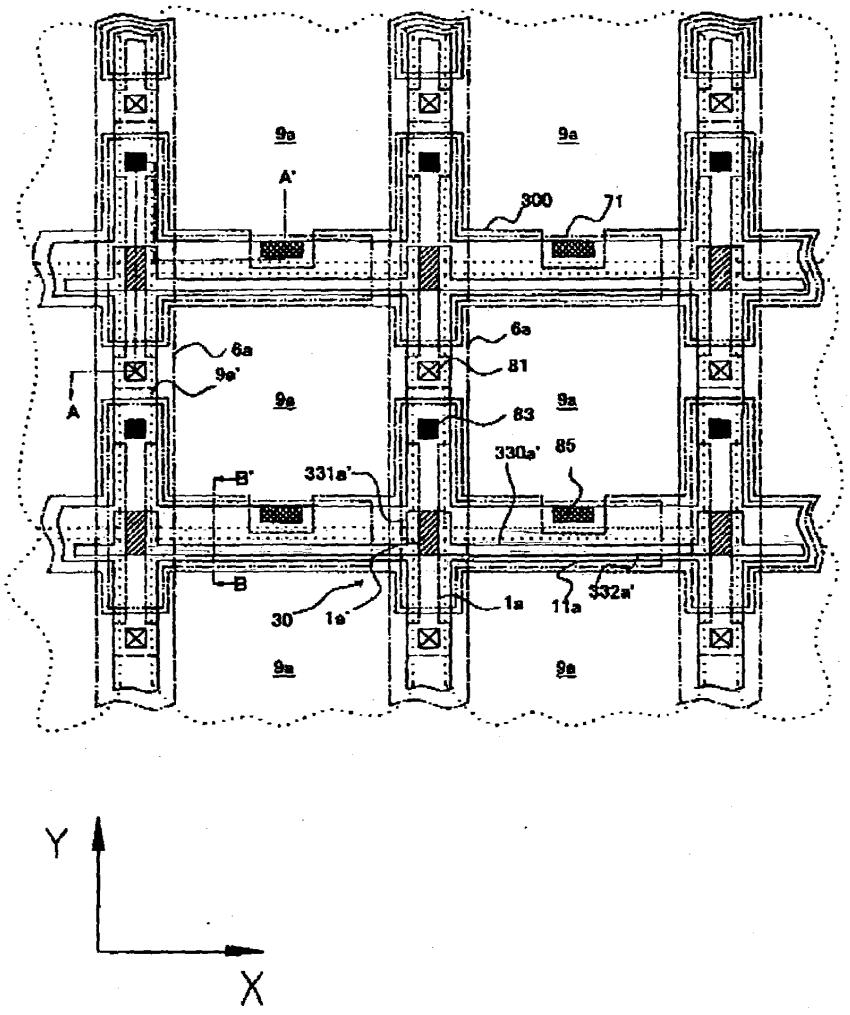


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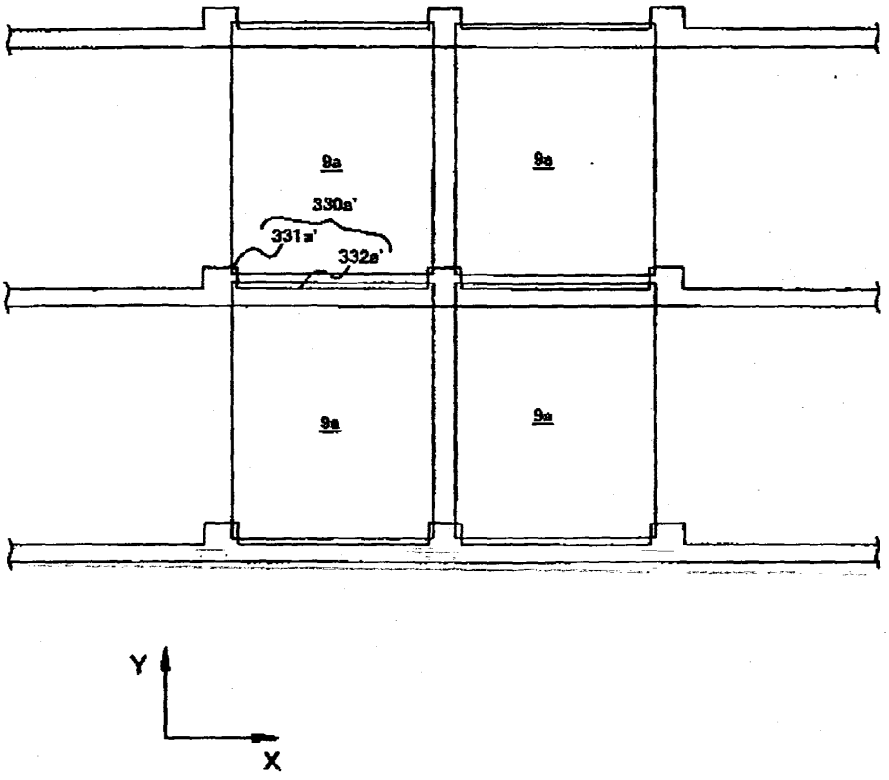
【図4】



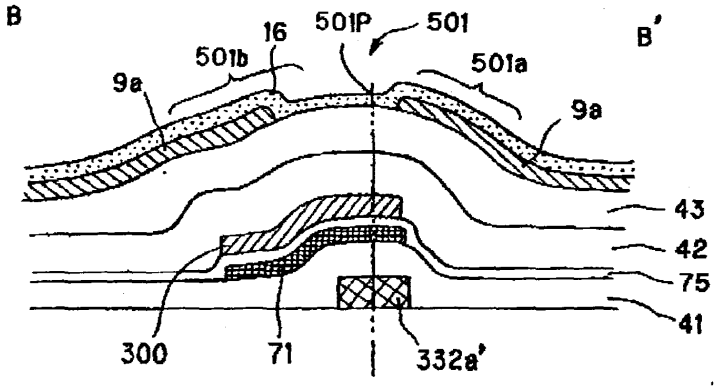
【図5】



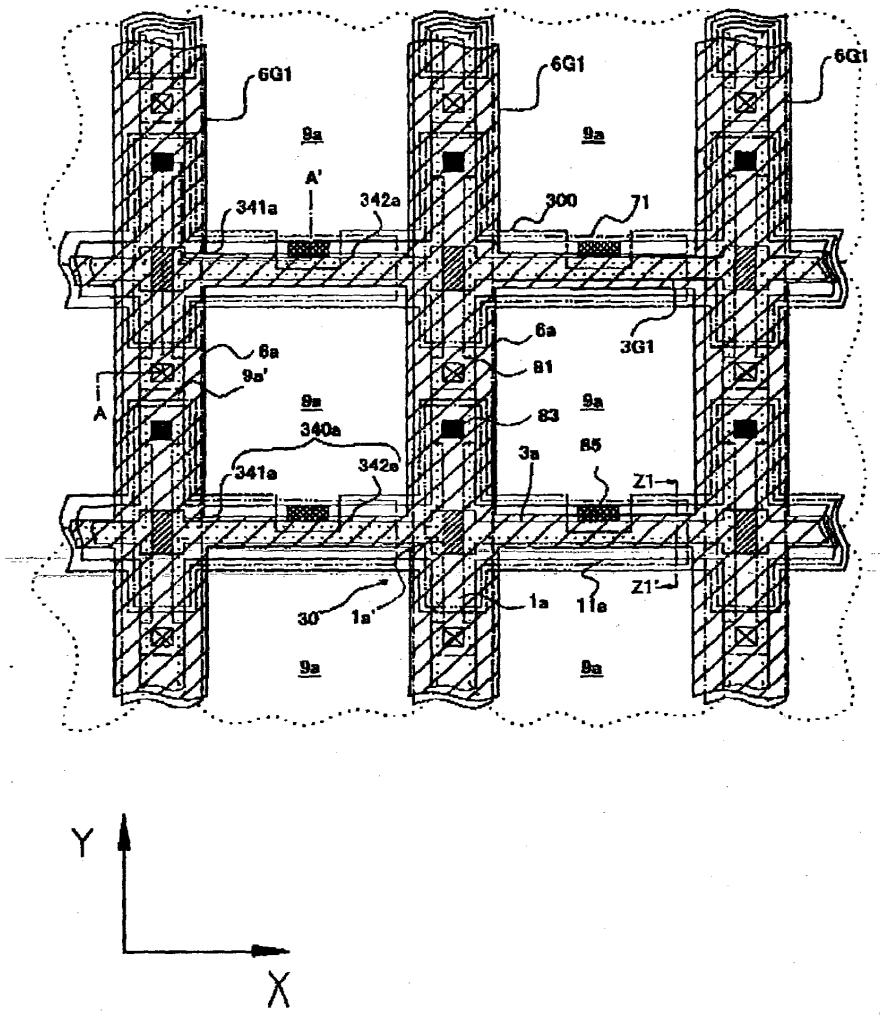
【図６】



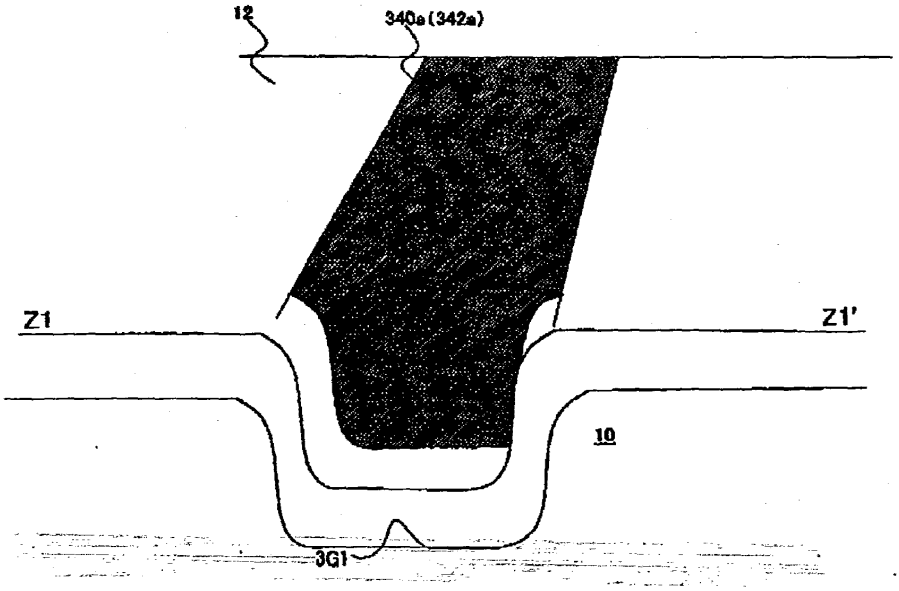
【図7】



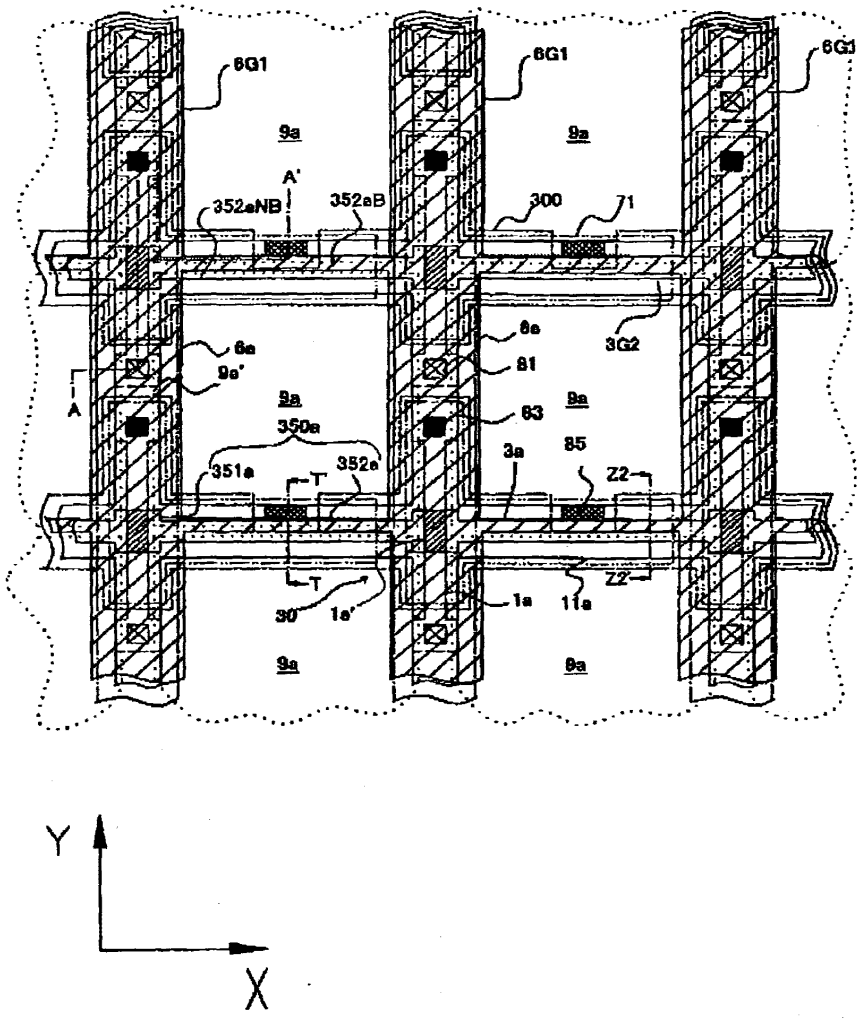
【図８】


6G1
6G1
6G1
9a
9a
A'
341a
342a
300
71
6a
3G1
6a
9a'
81
A
9a
9a
340a
83
85
3a
341a
342a
Z1
Z1'
30
1a'
1a
11a
9a
9a
Y
X

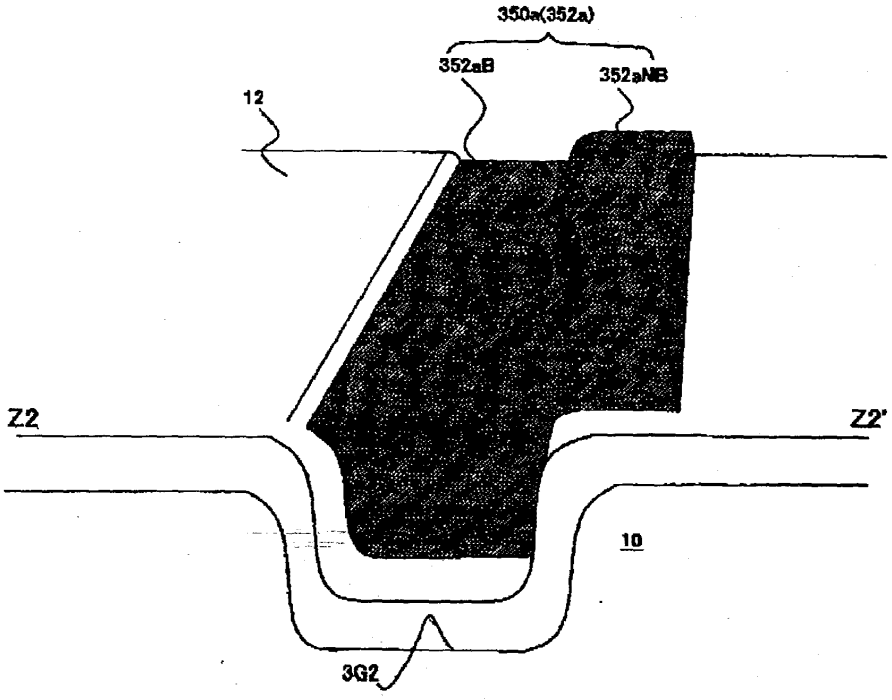
【図9】



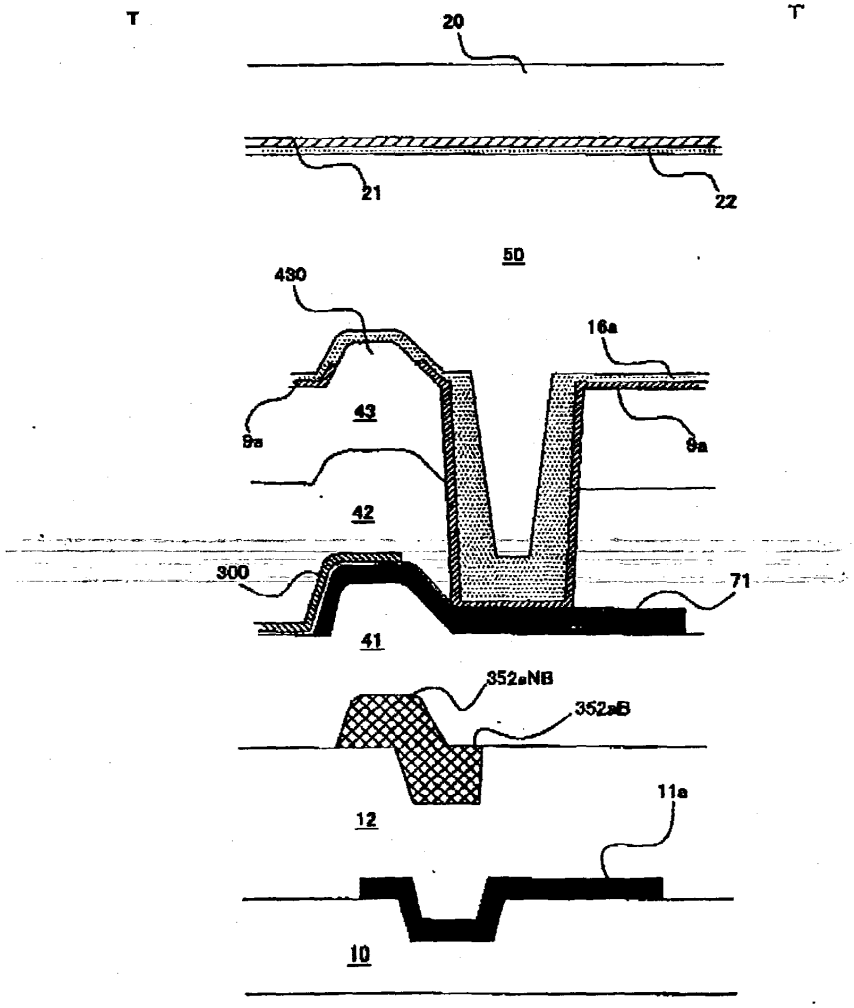
【図１０】


6G1
6G1
6G1
9a
9a
A'
352aNB
352aB
300
71
6a
9a'
6a
81
3G2
A
9a
9a
350a
63
351a
T
352a
3a
85
Z2
T
Z2
30
1a'
1a
11a
9a
9a
Y
X

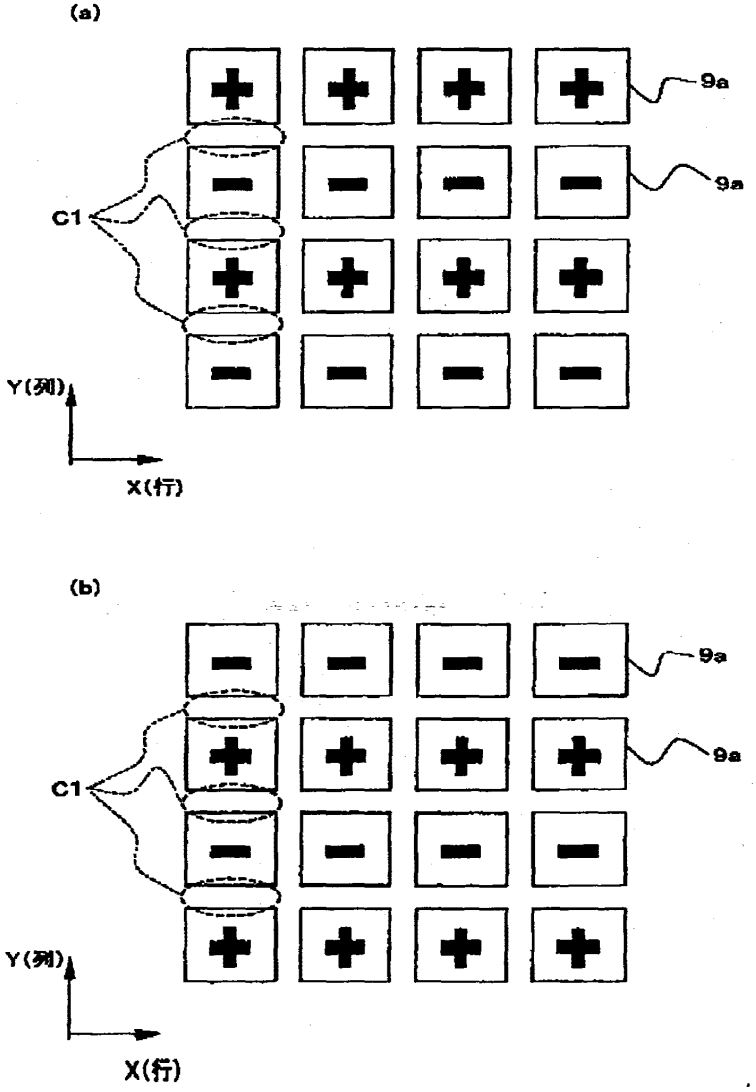
【図１１】



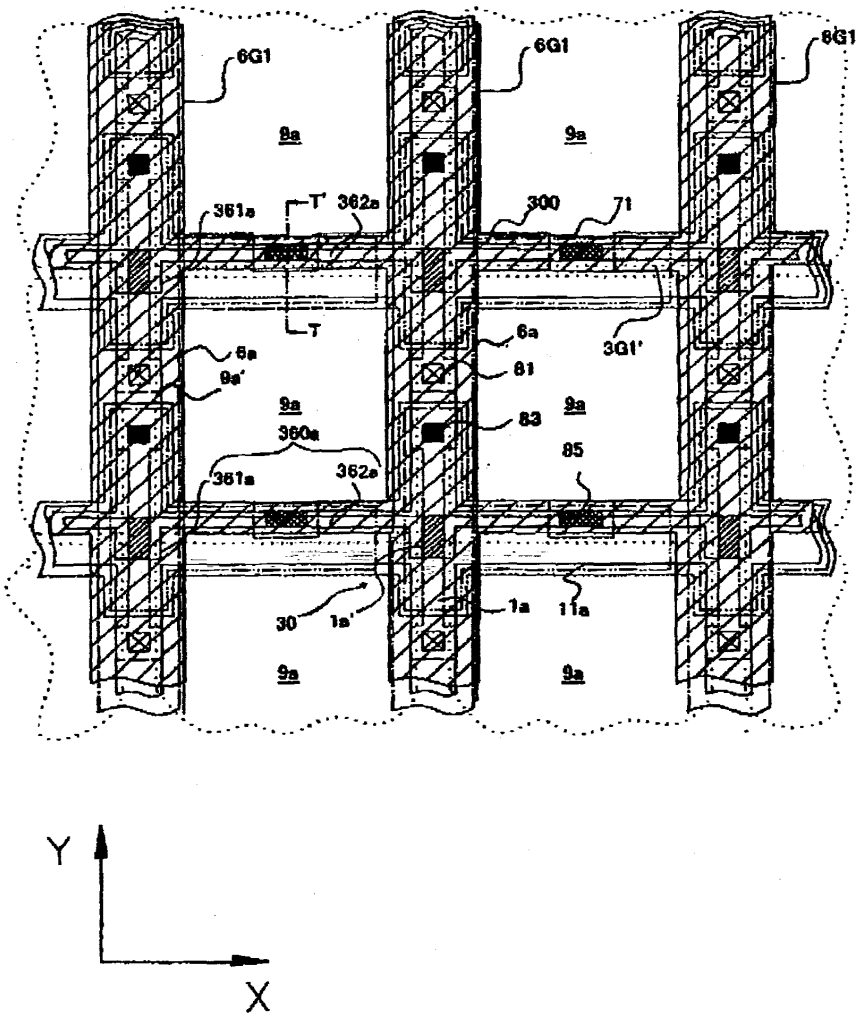
【図１２】



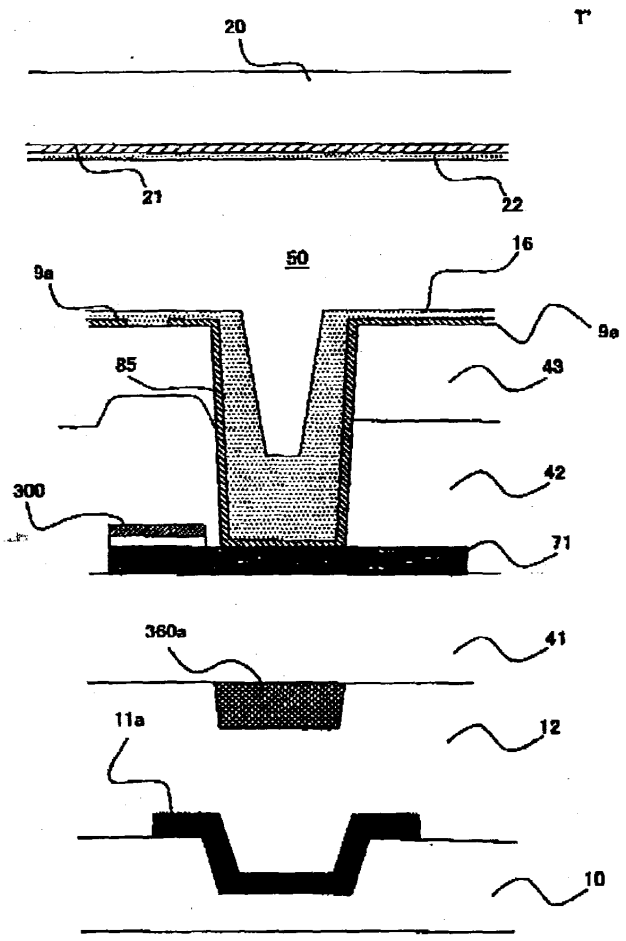
【図１３】



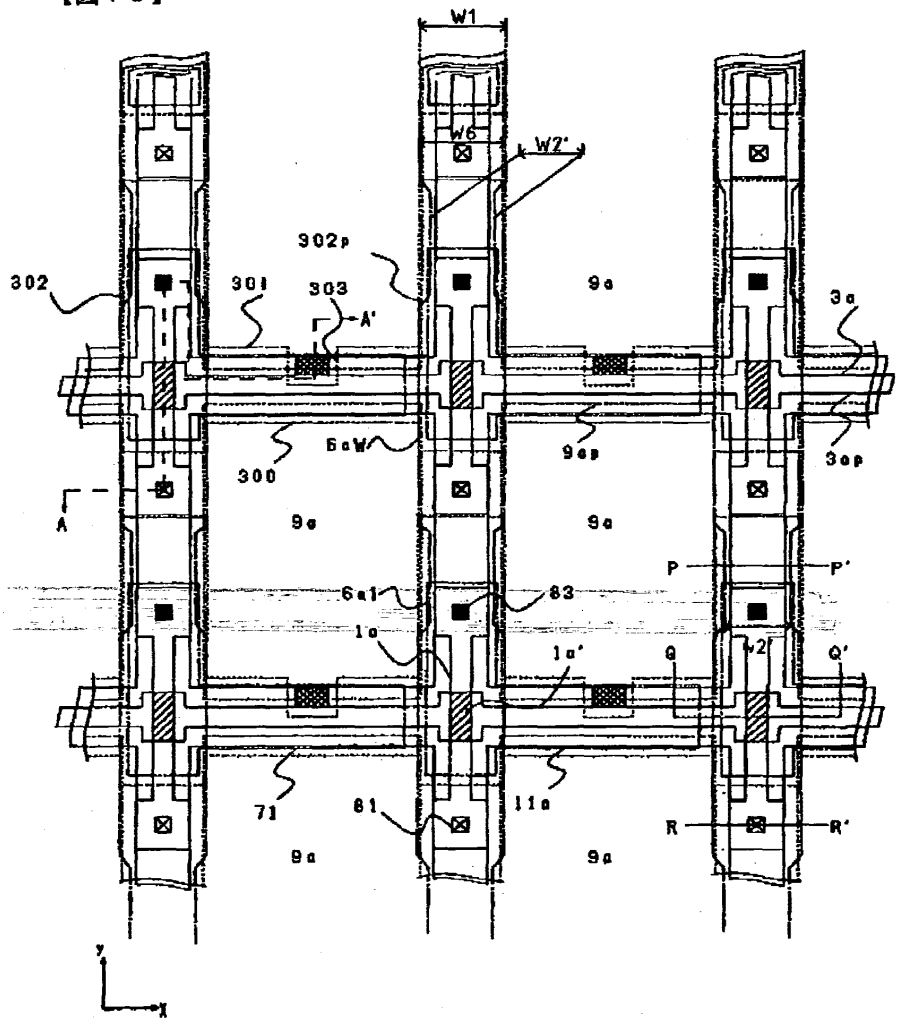
【図１４】


6G1
6G1
6G1
9a
9a
361a
T'
362a
300
71
T
6a
3G1'
6a
9a'
81
9a
9a
360a
83
85
361a
362a
30
1a'
1a
11a
9a
9a
Y
X

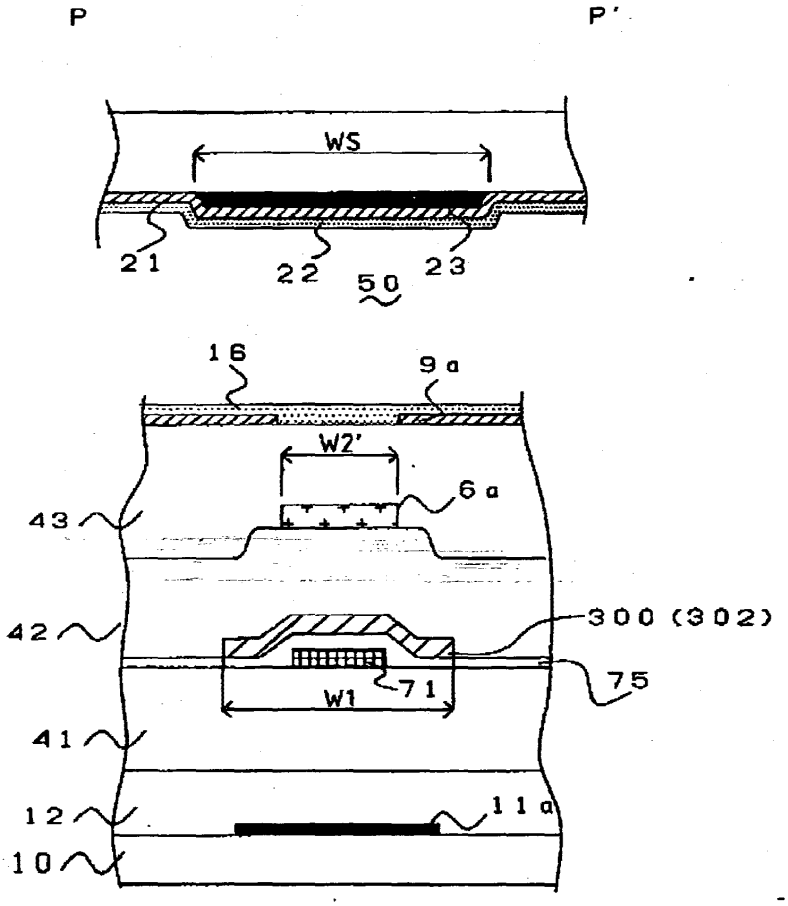
【図１５】



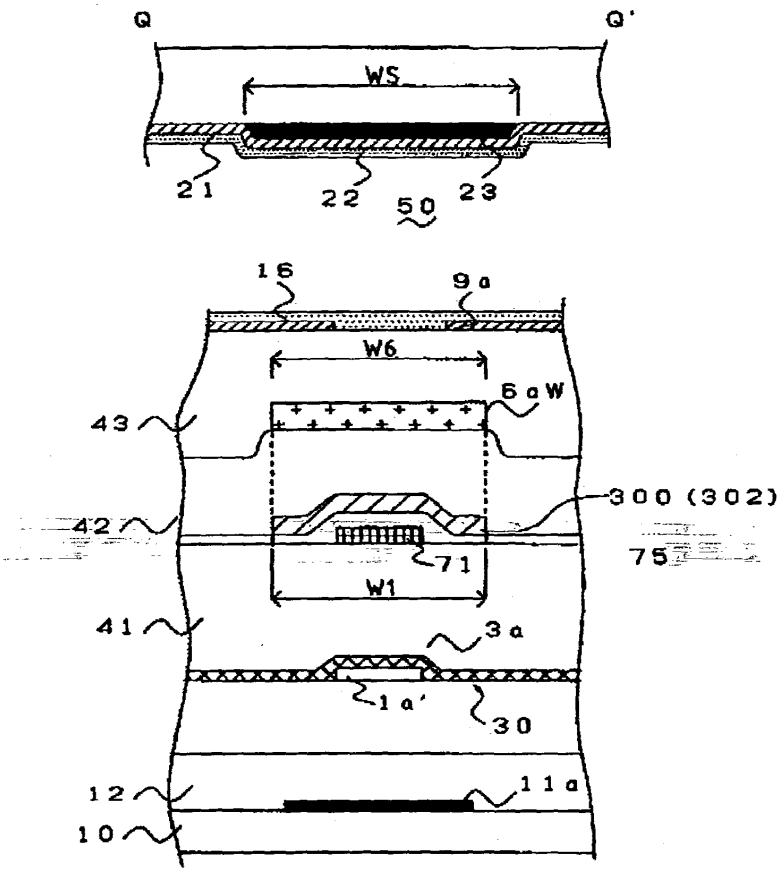
【図１６】


W1
W6
W2'
302p
302
301
303
A'
9a
3a
6aW
300
9ap
3ap
A
9a
9a
P
P'
6a1
83
1a
1a'
Q
W2
Q'
71
81
11a
R
R'
9a
9a
y
x

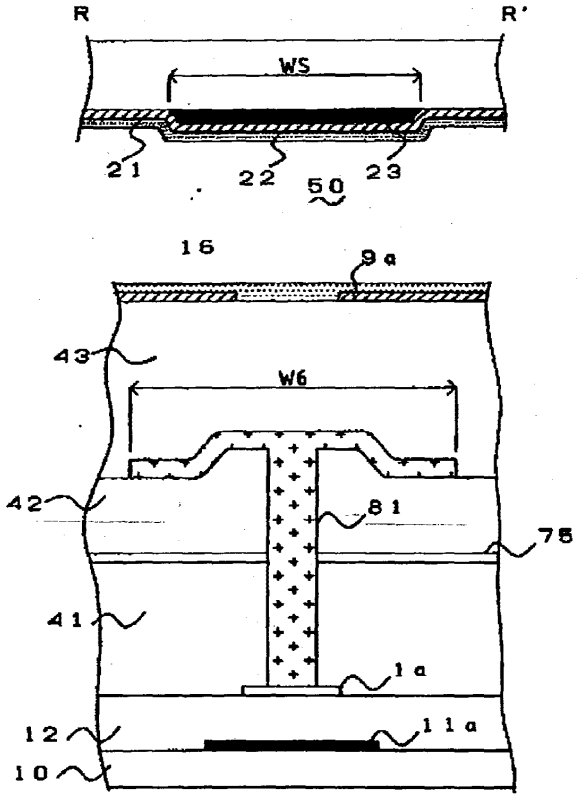
【図17】



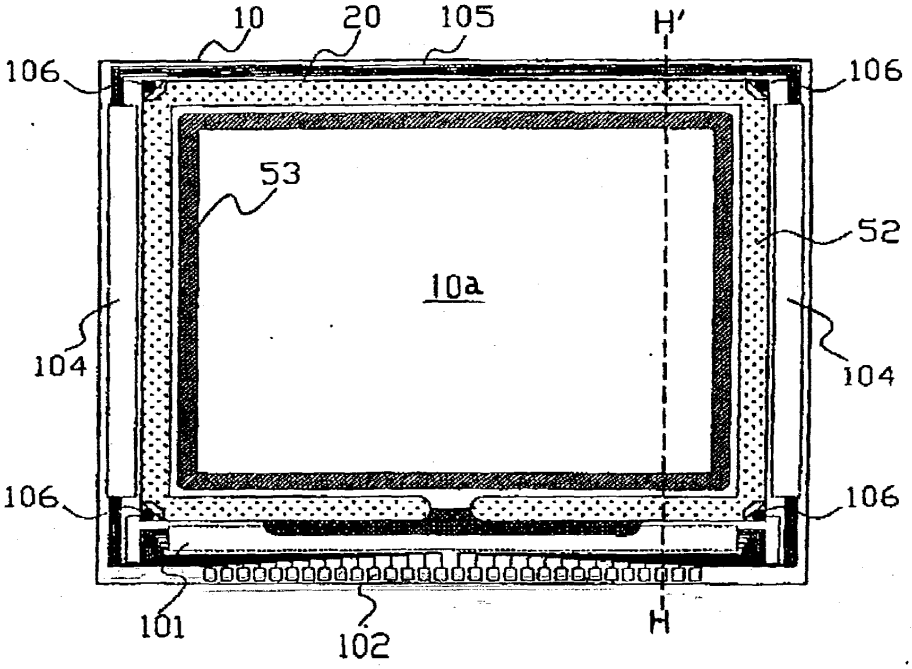
【図１８】


Q
Q'
WS
21
22
50
23
16
9a
W6
6aW
43
42
300 (302)
71
75
W1
41
3a
1a'
30
12
11a
10

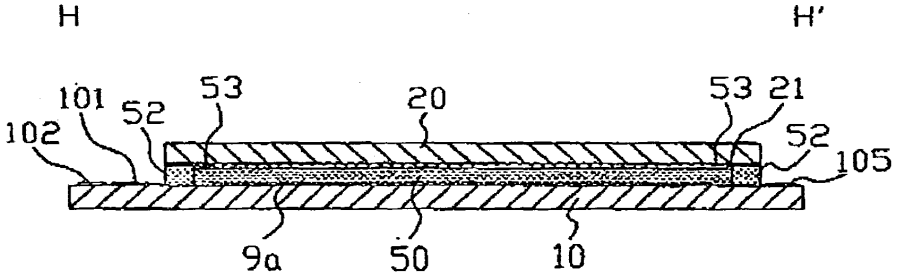
【図19】



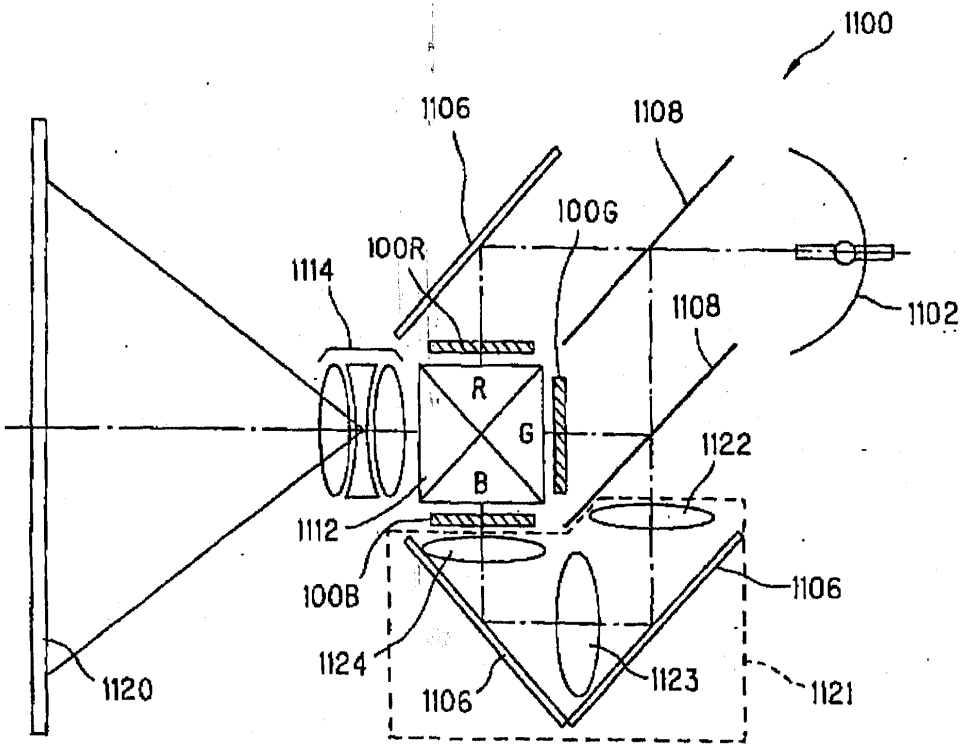
【図２０】


10
20
105
H'
106
106
53
52
10a
104
104
106
106
101
102
H

【図２１】


H
H'
101
52
53
20
53
21
102
52
105
9a
50
10

【図22】


1100
1106
1108
100G
100R
1114
1108
1102
R
G
B
1122
1112
100B
1106
1124
1123
1121
1106
1120

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Application papers not suitable for publication

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- ☐ Landscape orientation of text ☐ Specification ☐ Claims ☐ Abstract
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- ☐ Improper margins
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  - ☐ Drawing page(s)_____ ☐ Claim(s)
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  - ☐ Paper too thin
  - ☐ Glossy pages
  - ☐ Non-white background

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  - ☐ Claim(s)
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  - ☐ Line quality is too light, drawing(s)_____
  - ☐ More than 1 drawing and not numbered correctly
  - ☐ Non-English text, drawing(s)_____
  - ☐ Excessive text, drawing(s)_____
  - ☐ Photographs capable of illustration, drawing(s)_____

[redacted]