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AMORPHOUS SILICON THIN FILM TRANSISTOR FABRICATED WITH A NEW COPPER DRY ETCHING METHOD

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An inverted, staggered tri-layer amorphous thin film transistor (a-Si:H TFT) has been fabricated based on the two-photomask process and a new plasma-based copper etching method. Process steps and dry etching selectivity between n^+ a-Si and SiN_x were discussed in detail. At the linear region, $I_{\text{on}}/I_{\text{off}}$ ratio of the a-Si:H TFT was around 10^6 with threshold voltage (V_{th}) of 4.6 V. The I_{off} was below 10^{-12} A, the threshold voltage was 5.2V, and the $I_{\text{on}}/I_{\text{off}}$ ratio greater than 10^8 at the saturation region ($V_{\text{ds}}=10\text{V}$). A vertical or sloped copper profile can be prepared with the new plasma based etching process. This new process can be applied to large area and high-resolution liquid crystal displays as well as many non-display areas.

INTRODUCTION

The demand of large-area, high-resolution panels for applications in notebook and desktop computers, and digital wall TVs has been increasing drastically recently. With the increase of the panel size and the pixel number, gate- and data-line signal delays have to be decreased because they may create problems such as insufficient pixel charging, flickering, and vertical crosstalk on the screen [1-5]. The delay also causes non-uniform brightness, and, consequently, degradation of the display quality. Therefore, the gate signal delay can be considered a key performance limiting factor to the large-size and high-resolution a-Si:H TFT liquid crystal display (LCD). If the conventional high resistivity metals are to be used for the large size displays, the gate line thickness or width needs to be increased. A thick gate line causes a great challenge to the step coverage for the inverted, staggered TFT structure. A wide gate line is not desirable because it reduces the pixel aperture ratio and increases the line-to-line parasitic capacitance that adds additional signal delays. To follow the same argument of gate lines, the data line resistance and geometry could also benefit from the application of low resistivity metals. Therefore, metals such as aluminum and copper eventually have to be introduced into the interconnection part of the display.

Copper has many good characteristics such as very low resistivity, i.e., $1.67\mu\Omega\cdot\text{cm}$, lack of the electromigration problem, and no concern of hillocks formation. In spite of the tremendous amounts of research efforts done on copper, there are still many challenges. For example, copper has poor adhesion on glass, is easy to oxidize at low temperature, has a large diffusion constant in silicon, and has poor resistance to chemical attacks [6-9]. In order to solve the adhesion problem, a thin tantalum, molybdenum, titanium, or titanium nitride layer can be deposited between copper and glass as an adhesion layer. In addition, it is well known that copper is difficult to pattern with the

conventional plasma etching method because of the lack of volatility of the plasma-copper reacted product [10, 11]. Many new methods, such as adding a high-density plasma source or an ultraviolet or infrared or laser source to the reactive ion etching reactor, have been used to enhance the etch rate. However, these technologies are complicated and cannot be applied to the large-area substrate because of the uniformity problem. Recently, a new copper dry etching technology based on a novel plasma-copper reaction has been reported [12, 13]. The process could be carried out with a parallel-plate electrode design and at room temperature. This novel method can be used to supply vertical or sloped copper profile depending on the process condition.

In this paper, we study the a-Si:H TFT with copper source and drain pattern defined by the new dry etching method.

DEVICE FABRICATION

In addition to the copper/molybdenum metallurgy, the fabrication process of the a-Si:H TFT is very similar to that of a conventional a-Si:H TFT. The devices were characterized using HP 4155B semiconductor parameter analyzer.

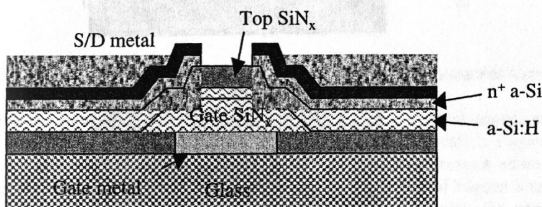


Figure 1 Vertical cross section of the tri-layer a-Si:H TFT with two masks.

Figure 1 shows the cross-sectional view of the tri-layer a-Si:H TFT fabricated with two photomasks [14]. For copper gate and source/drain contacts, thin molybdenum film was deposited as an adhesion layer using RF sputtering. This process has been successively used to prepare a-Si:H TFT with other metallic materials [15]. After the gate electrode deposition, copper was patterned using the new copper dry etching method (first photo mask) [12, 13]. The gate SiN_x , a-Si:H, and top SiN_x tri-layer was sequentially deposited without breaking vacuum by plasma enhanced chemical vapor deposition (PECVD) at 250°C . Then, a positive photo resist (AZ 1512) was coated on the top SiN_x . The back lithography step was carried out with a UV exposure tool (Karl Suss MJB C) using the gate pattern as the self-aligned mask. The source and drain areas were defined with the second mask. The copper layer was etched with the plasma method discussed in Ref. [12]. The molybdenum layer was wet etched and the n^+ layer was plasma etched.

The parallel electrode type plasma reactor, PlasmaTerm 700, in the RIE mode was used for the plasma etch processes. In the copper etching process, copper was converted into CuCl_x by reacting with chlorine (Cl_2) plasma gas. Instead of removing the CuCl_x compound formed in the plasma process, it was accumulated on the substrate surface.

After the plasma exposure, the sample was dipped in a diluted hydrochloric acids solution where CuCl_x was instantaneously dissolved.

Figure 2 shows SEM pictures of the patterned copper sample before and after plasma exposure at 25°C and 25 mTorr (Cl_2 20 sccm) for 2 min. As shown in Figure 2 (b), the exposed copper was completely converted into CuCl_x after the plasma exposure. CuCl_x is rougher and more porous than copper. Figure 2 (c) shows a vertical copper profile after the removal of the CuCl_x compound and the photoresist. A copper conversion rate as high as 4000Å per minute was obtained.

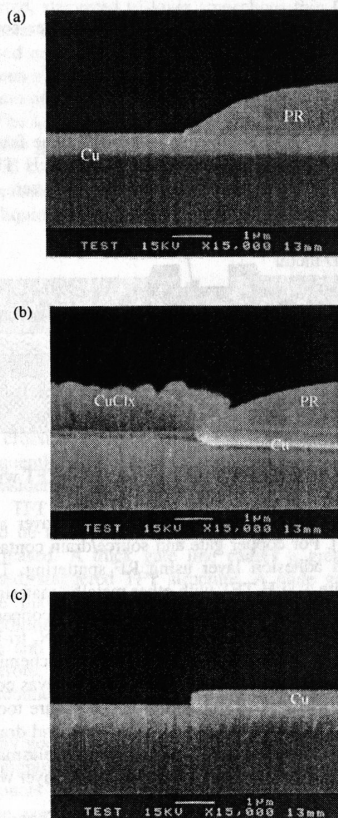


Figure 2 SEM pictures of the copper dry etching process (a) before and (b) after plasma exposure, and (c) after removal of CuCl_x and photoresist.

In order to protect the channel region, a high etch selectivity between the n^+ a-Si layer and top SiN_x has to be achieved. This is usually done with RIE because the wet process could have left a conductive residue [16].

Figure 3 shows that the n^+ a-Si to SiN_x etch selectivity is a function of the gas composition in the $\text{CF}_4 + \text{Cl}_2$ mixture. A selectivity as high as 45 was obtained with 0.28% CF_4 , which is close to that of previously reported value [14]. This kind of selectivity is especially useful in the preparing of large area TFT array.

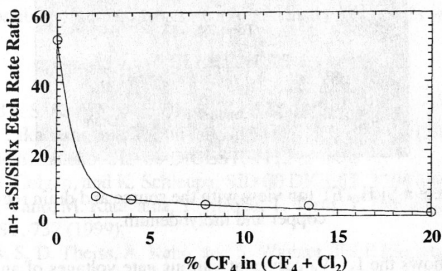


Figure 3 Dry etch selectivity between n^+ a-Si and SiN_x vs. CF_4 concentration

Although the new copper etching method can supply a vertical copper profile, as shown in Fig. 2(c), it can also be used to prepare a sloped copper profile. Figure 4 is the SEM picture of a sloped copper pattern with an underneath molybdenum adhesion film. The copper plasma etch condition was slightly modified from that of Figure 2 in order to obtain the sloped profile. The molybdenum layer was wet etched after the copper etch. This kind of profile is ideal for the gate structure of an inverted, staggered TFT.

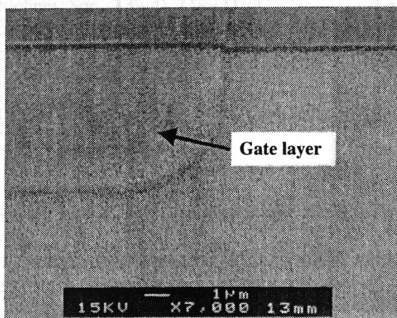


Figure 4 A SEM picture of an etched molybdenum/copper film

Figure 5 shows a complete a-Si:H TFT with the copper/molybdenum source and drain regions. The metal stack was over etched in this case, but the n⁺ a-Si layer has little undercut.

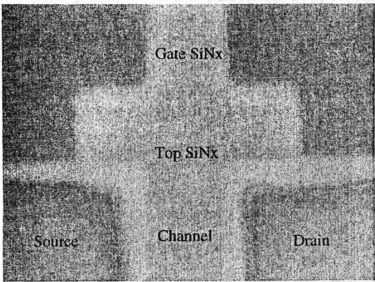


Figure 5 A complete a-Si:H TFT top view with the source and drain regions composed of copper and molybdenum.

Figure 6 shows the $I_d - V_d$ curves at various gate voltages of an a-Si:H TFT with copper source and drain electrodes prepared with the new plasma etching method. These $I_d - V_d$ curves show no current crowding. Therefore, good ohmic contacts were formed on the source and drain regions. This TFT has transfer characteristics similar with those of a conventional, non-copper a-Si:H TFT.

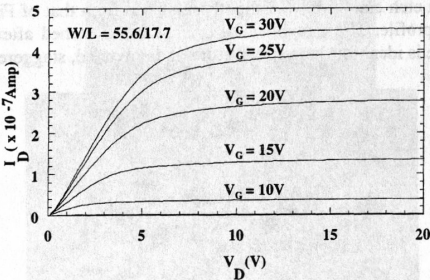


Figure 6 Transfer characteristics ($I_d - V_d$) of a-Si:H TFT.

At the linear region, I_{on}/I_{off} ratio of the a-Si:TFT was around 10^6 with a threshold voltage (V_{th}) of 4.6 V. At the saturation region ($V_{ds}=10V$), it has a subthreshold swing approximately 0.9V/dec, an I_{off} below 10^{-12} A, a V_{th} of 5.2V, an I_{on}/I_{off} ratio greater than 10^8 .

CONCLUSION

The inverted, staggered tri-layer a-Si:H TFT with copper source and drain electrodes has been successfully fabricated based on a two-photomask process and a new Cl_2 plasma-based copper etching method. The novel copper dry etching process can be used to prepare a vertical profile for the source/drain application and a sloped profile for the gate application. An etching rate higher than 4000 Å per minute was achieved. The TFT's transfer characteristics are comparable with those of a conventional, non-copper TFT. This copper etching method can be used to prepared patterns over a large area. Therefore, it is possible to prepare large-area, high density TFT LCDs with this method.

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