

MATERIALS SCIENCE

R. A. Street (Ed.)

# Technology and Applications of Amorphous Silicon



Springer

*Editors:* R. Hull · R. M. Osgood, Jr. · H. Sakaki · A. Zunger

Springer Series in Materials Science covers the complete spectrum of materials physics, including fundamental principles, physical properties, materials theory and design. Recognizing the increasing importance of materials science in future device technologies, the book titles in this series reflect the state-of-the-art in understanding and controlling the structure and properties of all important classes of materials.

- |                                                                                                             |                                                                                                                  |
|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| 31 <b>Nanostructures and Quantum Effects</b><br>By H. Sakaki and H. Noge                                    | 36 <b>Ceramics</b><br>Mechanical Properties, Failure<br>Behaviour, Materials Selection<br>By D. Munz and T. Fett |
| 32 <b>Nitride Semiconductors and Devices</b><br>By H. Morkoç                                                | 37 <b>Technology and Applications<br/>of Amorphous Silicon</b><br>Editor: R. A. Street                           |
| 33 <b>Supercarbon</b><br>Synthesis, Properties and Applications<br>Editors: S. Yoshimura and R. P. H. Chang | 38 <b>Fullerene Polymers<br/>and Fullerene Polymer Composites</b><br>Editors: P. C. Eklund and A. M. Rao         |
| 34 <b>Computational Materials Design</b><br>Editor: T. Saito                                                |                                                                                                                  |
| 35 <b>Macromolecular Science<br/>and Engineering</b><br>New Aspects<br>Editor: Y. Tanabe                    |                                                                                                                  |

Robert A. Street (Ed.)

# Technology and Applications of Amorphous Silicon

With 279 Figures and 20 Tables

Dr. Robert A. Street  
Xerox PARC  
3333 Coyote Hill Road  
CA 94304 Palo Alto  
USA

*Series Editors:*

Prof. Robert Hull  
University of Virginia  
Dept. of Materials Science and Engineering  
Thornton Hall  
Charlottesville, VA 22903-2442, USA

Prof. R. M. Osgood, Jr.  
Microelectronics Science Laboratory  
Department of Electrical Engineering  
Columbia University  
Seeley W. Mudd Building  
New York, NY 10027, USA

Prof. H. Sakaki  
Institute of Industrial Science  
University of Tokyo  
7-22-1 Roppongi, Minato-ku  
Tokyo 106, Japan

Prof. Alex Zunger  
NREL  
National Renewable Energy Laboratory  
1617 Cole Boulevard  
Golden Colorado 80401-3393, USA

ISSN 0933-033x

ISBN 978-3-642-08499-7 ISBN 978-3-662-04141-3 (eBook)  
DOI 10.1007/978-3-662-04141-3

*Library of Congress Cataloging-in-Publication Data.*

Technology and applications of amorphous silicon / R. A. Street (ed.). p.cm. – (Springer series in materials science; v. 37). Includes bibliographical references and index. 1. Amorphous semiconductors. 2. Silicon. 3. Optoelectronic devices – Materials. 4. Liquid crystal displays. I. Street, R.A. II. Series: Springer series in materials science; v. 37. TK7871.99.A45T38 2000 621.3815'2–dc21 99-23864

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilm or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer-Verlag. Violations are liable for prosecution under the German Copyright Law.

© Springer-Verlag Berlin Heidelberg 2000

Originally published by Springer-Verlag Berlin Heidelberg New York in 2000.  
Softcover reprint of the hardcover 1st edition 2000

The use of general descriptive names, registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

Typesetting: Data conversion by Steingraeber Satztechnik GmbH, Heidelberg  
Cover concept: eStudio Calamar Steinen  
Cover production: design & production GmbH, Heidelberg

SPIN: 10719334 57/3144/tr - 5 4 3 2 1 0 - Printed on acid-free paper



## 2.2.2 Pixel Design

**Twisted-Nematic Cell.** There are many variations in the pixel design layout. First, the designer must choose whether the a-Si:H TFTs will be configured as back-channel-etched TFTs or channel-passivated TFTs (see Sect. 2.3.1). Next, the TFT layout and the pixel electrode design must be considered. Then, the configuration of the storage capacitance has to be decided. Two examples of possible configurations are shown in Fig. 2.6. In the additional capacitance ( $C_{add}$ ) scheme (Fig. 2.6a), the pattern of the gate busline is formed to overlap the transparent pixel electrode of ITO (Indium Tin Oxide), so that no extra buslines are needed. In the storage capacitance design of  $C_{st}$  (Fig. 2.6b), an independent electrode is provided for the storage capacitance. The  $C_{add}$  design is simple to fabricate, but it increases the gate busline capacitance. On the other hand, the  $C_{st}$  design has an increased number of cross-over points between the  $C_{st}$  busline and the data busline; possible shorts between these buslines can lower the production yield of TFT panels, and the panel processing becomes more complex.

The design rule defines the minimum pattern size and the gap or spacing between various patterns. For example, it sets the minimum size for the spacing between pixel electrodes and data buslines, and also governs the channel length of a-Si:H TFTs. A design rule or minimum design size of  $10\ \mu\text{m}$  is generally adopted for panels with a diagonal size of around 10 in. and video-graphic-array (VGA) resolution ( $640 \times 480$ ). For higher resolution panels, sub  $10\ \mu\text{m}$  technology is used for the design and processing. Effects of modifying the design rule are discussed in Sect. 2.2.4.

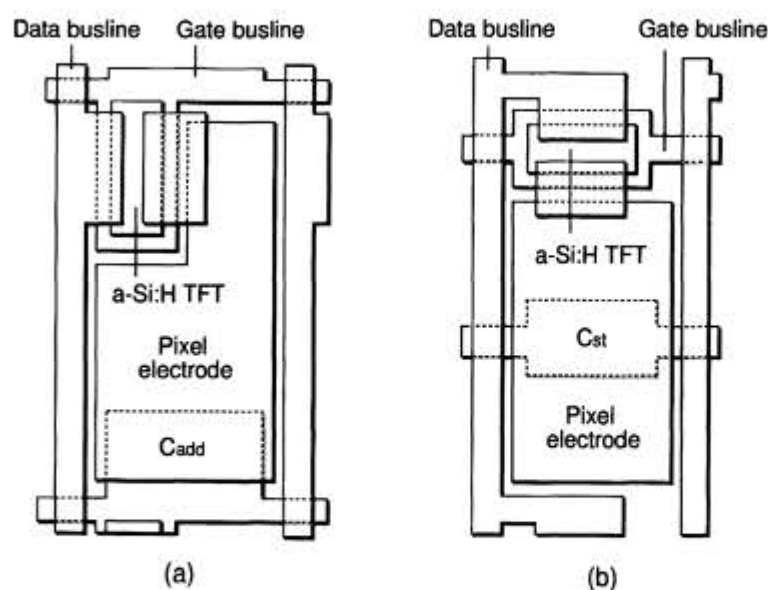


**Fig. 2.6a,b.** Examples of pixel layout of a TN cell: (a) the additional capacitance case,  $C_{add}$ , and (b) the storage capacitance case,  $C_{st}$

As described before (Fig. 2.4), the utility factor of the backlight illumination is limited by the aperture ratio of the pixels. The aperture is defined as the area ratio of the transparent electrode to the pixel. Since light can only be modulated at the transparent pixel electrodes, light passing through the gaps between the pixel electrodes and the metallization patterns degrades the display quality and should be blocked. Therefore, the gap between metallizations is covered by an opaque material; this is the so-called “black matrix” design. The black matrix is usually formed on the color-filter substrate. Since the two glass substrates, i.e., the color-filter and TFT substrates, are assembled and aligned after processing each substrate separately, the alignment cannot be as precise as can be achieved on a single substrate. Therefore, the black matrix must have a large margin, resulting in a reduced aperture ratio. This large margin can be decreased by fabricating the black matrix on the TFT substrate. Precise alignment can be achieved in this scheme, allowing the aperture and brightness to be increased. However, since the materials for the black matrix are metals like chromium, capacitive coupling between the black matrix and the electrodes can be a problem. Therefore, the black matrix is usually fabricated on the color-filter substrate. When chromium is used for the black matrix, it reflects light from outside, degrading the display quality of the panel. This effect can be lessened by the use of a chromium oxide. Another role of the black matrix is to shield the a-Si:H TFTs from incident light. Since a-Si:H is very sensitive to visible radiation, the visible light from the backlight incident upon the TFTs generates a photocurrent which increases the TFT off-current. Thus, the black matrix is designed to cover the whole TFT area.

The aperture ratio is also affected by the disclination of the liquid crystal. The disclination line corresponds to the boundary between regions of the liquid crystal that have directors with opposite orientations. In a twisted-nematic TFT LCD, the electric field is generally applied vertically or perpendicular to the glass substrate. However, the electrode configuration on the TFT substrate gives rise to a local horizontal electric field. This local field, in turn, induces reverse tilt domains or disclinations. This phenomenon is also related to the rubbing direction of the alignment layer. Generally, the rubbing direction is at  $45^\circ$  to the busline direction and the disclination tends to occur at the corner of each pixel electrode corresponding to the tail of the rubbing direction. The reverse tilt introduces transmittance irregularities and decreases the contrast ratio in that region. Therefore, in order to avoid undesirable effects, this area has to be covered by the black matrix, even though reverse tilt only occurs occasionally.

**In-Plane-Switching Mode.** In the preceding section, the pixel design based on the twisted-nematic (TN) liquid-crystal cell was discussed. These TN-cell-based displays suffer from the narrow viewing-angle characteristics. One of the most promising cell modes to overcome this situation is the in-

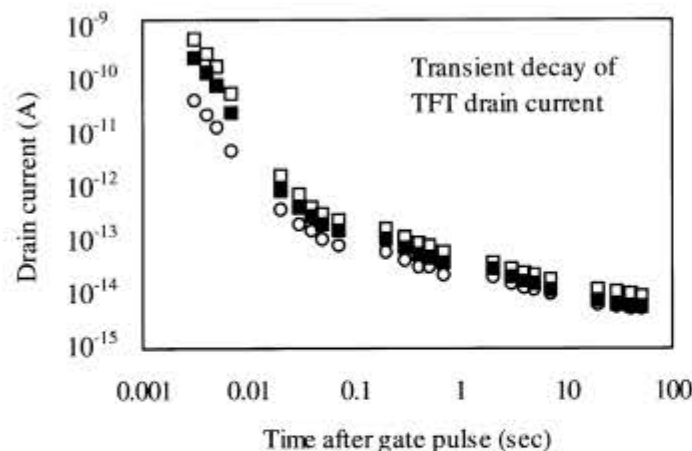


**Fig. 4.9.** Transient response of the TFT leakage current showing the slow decay to the steady state value. The TFT has  $W/L = 75/8.5 \mu\text{m}$  and the Source-drain voltage is 5 V (circles), 7.5 V (closed squares) and 12.5 V (open squares) [4.26]

where  $V_G$  is the gate voltage,  $V_T$  is the threshold voltage,  $W$  is the TFT width and  $L$  is the length. A nitride thickness of  $3000 \text{ \AA}$  has a gate capacitance,  $C_G$  of  $5 \times 10^{-8} \text{ F/cm}^2$ , and a field effect mobility,  $\mu_{FE}$ , of  $0.8 \text{ cm}^2/\text{Vs}$ , yields,

$$R_{ON} = 25[(V_G - V_T)W/L]^{-1} \text{ M}\Omega. \quad (4.11)$$

An on-resistance of a few  $\text{M}\Omega$  is achieved with a width-to-length ratio,  $W/L \sim 1\text{--}5$  and  $V_G - V_T \sim 10 \text{ V}$ , and the threshold voltage is usually  $0\text{--}2 \text{ V}$ .

The TFT transfer characteristics are shown in Fig. 4.8 [4.24]. In the sub-threshold region with  $V_G$  below  $V_T$ , the current increases exponentially. The minimum leakage current is attained with  $V_G$  between  $-5 \text{ V}$  and  $-10 \text{ V}$ , and the corresponding off-resistance is extremely large,  $> 10^{15} \Omega$ . Contributing to the low current are the barrier formed by the n-type source and drain contacts, the low density of states at the a-Si:H/nitride interface and the low mobility of a-Si:H. The leakage current is much lower than in polysilicon devices and make the a-Si:H device preferred for image sensors. The leakage current is probably a bulk generation current in the channel [4.25], similar to the mechanism of photodiode leakage described in Sect. 4.2.1.

There is a significant slow transient decay to the TFT leakage current when the device is turned off, as indicated in Fig. 4.9 [4.26]. The slow decay is similar to that of the photodiode in Fig. 4.4 and reaches a steady state only after several seconds. The effect is most likely due to the release of trapped charge and affects the image sensor by providing a source of fixed charge that can be subtracted from the signal provided that the signal and offset images are acquired with the same timing conditions.

The capacitance of the TFT is a combination of the channel capacitance,  $C_G WL$ , and the parasitic capacitance of the source and drain overlaps, which are also proportional to  $W$ . Smaller feature sizes greatly reduce the capacitance, and since this is a major contribution to the electronic noise of the

imager, there are immediate benefits in reducing the photolithography feature sizes for the large area arrays.

Undoped a-Si:H is a highly photoconductive material, so that the TFT leakage current is sensitive to illumination even when the channel is very thin. It is therefore usually necessary to provide a light shield for the TFT to obtain the very low leakage currents that are required. Shielding is readily accomplished with a metal line placed over the TFT, and the gate metal already provides a light shield from below.

**Other TFT Materials.** Arrays are also fabricated with different active semiconductor materials for the TFTs. The two most widely explored are polycrystalline silicon and CdSe. The use of polycrystalline silicon in active matrix LCDs has been investigated extensively, and aspects of the technology are described in Chap. 2. The interest in poly-silicon is to provide higher performance devices to allow the drive circuitry to be integrated into the array, and LCDs with completely integrated drivers have recently been introduced onto the market. The main issue with poly-silicon is to fabricate TFTs on glass substrates. High temperature processing that closely follows the silicon IC technology uses thermal oxidation to fabricate the TFT gate dielectric and annealing to activate dopants. This process results in excellent TFTs, but cannot be performed on glass substrates. Efforts to use intermediate temperatures near the glass softening point have given way to laser crystallization that allows the silicon films to be melted without heating the glass substrate. The laser crystallized material has a mobility of typically  $20\text{--}100 \text{ cm}^2/\text{Vs}$ , which is high enough to fabricate integrated drivers [4.27]. However, the off-current is significantly higher than for a-Si:H, and as is discussed in Sect. 4.3.2, a low off-current is essential for the pixel switch of image sensor arrays. This requirement has led to the development of a hybrid technology that allows selective crystallization of some TFTs so that both devices can be made on the same array, and this is the subject of Chap. 3.

Polycrystalline CdSe has also been studied as a TFT material [4.28]. The devices are usually fabricated with a bottom gate and an  $\text{SiO}_2$  gate dielectric. Low temperature deposition is consistent with the use of glass substrates. The carrier mobility is usually in the range  $50\text{--}150 \text{ cm}^2/\text{Vs}$ , and sometimes even higher. The leakage current can be made to be almost as low as a-Si:H, with the low values helped by the use of a double gate structure. Despite the good properties, CdSe TFTs are not widely used, evidently because the processing is difficult. Amorphous and poly-crystalline silicon benefit greatly from the fact that the processing chemistry is very similar to that used for the single crystal silicon IC industry and so can benefit from the extensive developments that have taken place.