

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

Case No. IPR2024-00976

U.S. Patent No. 7,502,079

**DECLARATION OF RICHARD A. FLASCK
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,502,079**

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I. INTRODUCTION

1. I, Richard A. Flasck, submit this declaration to state my opinions on the matter described below. I am over the age of 21 and am competent to make this declaration.

2. I have been retained by counsel for BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”), as an independent expert in this proceeding before the United States Patent and Trademark Office (“USPTO”). My company, RAF Electronics Corp., charges \$395 per hour for my time plus expenses for work performed in connection with this project, which is my regular rate for consulting work. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case. I have no other interest in this proceeding.

3. I understand that this proceeding involves U.S. Patent No. 7,502,079, (“the ’079 patent”), and I have been asked to provide my opinions as to the patentability of the claims of the ’079 patent. I understand that the application for the ’079 patent was filed on December 1, 2005, and claims priority to an earlier U.S. priority document filed on December 17, 2002, as well as foreign priority documents having filing dates of December 16, 2002, and January 7, 2002. As I explain below

in Section VI.C (paragraphs 91-95), it is my opinion that the January 7 priority document does not disclose the subject matter claimed in the '079 patent; therefore, it is my understanding from counsel that the claims are not entitled to priority before December 16, 2002.

4. I have been asked to consider the validity of the claims of the '079 patent based on certain prior art references. I have also been asked to consider the state of the art and prior art available as of December 16, 2002. Based on the prior art discussed in this declaration, it is my opinion that claims 1-3 of the '079 patent are unpatentable for the reasons provided below.

II. EXPERIENCE AND QUALIFICATIONS

5. My qualifications for forming the opinions set forth in this Report are summarized here and explained in more detail in my curriculum vitae, which is submitted as an Exhibit 1003.

6. I received a Bachelor of Science degree in Physics from the University of Michigan, Ann Arbor, in 1970. I thereafter received a Master of Science degree in Physics from Oakland University in Rochester, Michigan, in 1976. I am the founder and CEO/owner of RAF Electronics, where I developed and patented Liquid Crystal on Silicon (LCOS) microdisplay projection technology and LED-based lighting products.

7. After receiving my Bachelor's degree, I was employed as a scientist and a manager by Energy Conversion Devices, Inc., from 1970 through 1982. My work at Energy Conversion Devices concerned the development of thin film photovoltaics, ablative imaging films, non-volatile memory, multi-chip modules, superconducting materials, electroluminescent materials, and thin film transistors (TFTs).

8. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active matrix liquid crystal displays (AMLCDs). My work at Alphasil included TFT process and back-plane circuit design, data driver and gate driver design, scalars, video circuits, gamma correction circuits, backlighting unit (BLU), and inverter design. At Alphasil, I established the world's first amorphous silicon TFT active matrix LCD pilot production line. I worked at Alphasil from 1982 through 1989.

9. After leaving Alphasil, I founded RAF Electronics Corp., described above. I have served as CEO/owner of RAF Electronics since that time. At RAF Electronics, I developed and designed LCD microdisplays, and HDTV projectors. In 1997, I took the position of President and COO at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects

Agency (DARPA) contract, and for implementing MEM fluidic self-assembly (FSA) technology for use in flat panel displays and RFID tags. I left the position in 1999.

10. In 2002, I co-founded and served as COO of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for LCD HDTV projectors, such as polarization optics, condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED devices and LCD microdisplays. I left Diablo in 2007.

11. In 2019 I was awarded a CalSeed grant of \$150,000 from the California Energy Commission based on my patented non-imaging optics lighting platform.

12. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My inventions concern technologies including LCD, LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, and wafer based active matrices. Of particular interest may be the following patents:

- a. U.S. Patent No. 6,266,037 (July 24, 2001), “Wafer Based Active Matrix.”

- b. U.S. Patent No. 5,123,847 (June 23, 1992), “Method of Manufacturing Flat Panel Back Planes, Display Transistors.”
- c. U.S. Patent No. 4,651,185 (Mar. 17, 1987), “Method of Manufacturing Thin Film Transistors and Transistors Made Thereby.”
- d. U.S. Patent No. 4,545,112 (Oct. 8, 1985), “Method of Manufacturing Thin Film Transistors and Transistors Made Thereby.”

13. I have authored or co-authored twenty-five articles or conference presentations, including numerous papers and presentations concerning LCD and lighting technologies. My curriculum vitae lists these articles and conference presentations. Of particular interest may be the following papers and presentations:

- a. R. Flasck, and S. Holmberg, “Amorphous Silicon Thin Film Transistor (TFT) Driven Liquid Crystal Displays (LCD),” Advances in Display Technology V, Elliott Schlam, Editor, Proceedings of SPIE, Vol 526, 94-98 (1985).
- b. R. Flasck, “U.S. Display Suppliers and Developers: Comments on Developments and Manufacturing,” Flat Panel Displays 1988

Conference and Exhibition; Stanford Resources, Inc. (1988). –
Invited Presentation and Expert Panel Member.

c. R. Flasck, “Current and Near Term Applications of Flat Panel
Display Devices,” Applications of Electronic Imaging; John
Urbach, Editor; Proceedings of SPIE, Vol 1082 (1989). – Invited
Critical Review Paper.

d. R. Flasck, “The Care and Feeding of Single Crystal Silicon Light
Valve Design,” Society for Information Display FPD Strategic
and Technical Symposium, September 9-10, 1998.

14. I believe that I am well qualified to serve as a technical expert in this
matter based upon my educational and work experience, and specifically, flat panel
display devices, including liquid crystal displays.

15. I have served as an expert witness on at least 50 patent disputes (district
court cases, ITC hearings, IPRs, EPRs, and PGRs). Many of these matters involved
LCD, active matrix, and/or flat panel displays. I have testified in district court and
before the ITC.

16. Therefore, based on my education, professional experience, scholarly
books and publications, I am an expert in the relevant field of the '079 patent and
have been an expert in this field since before the '079 patent was filed with the

USPTO. I am familiar with how a person having ordinary skill in the art would have understood and used the terminology found in the '079 patent at the time of its filing.

III. MATERIALS CONSIDERED

17. In forming my opinions, I have reviewed the '079 Patent, its prosecution history and references cited by the Examiner, the materials cited in the List of Exhibits below, and the materials cited throughout my declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,502,079 to Murade (“’079 patent”)
Ex. 1004	Prosecution File History of the '079 patent
Ex. 1005	Prosecution File History of U.S. Application No. 10/320,371
Ex. 1006	JP-2002-000713 (Jan. 7, 2002) Asserted Foreign Priority Application for the '079 Patent, along with Certified Translation
Ex. 1008	JP-2002-090721A to Kurashina (“ <i>Kurashina</i> ”), along with Certified Translation
Ex. 1009	U.S. Pub. No. 2002/0014627A1 to Sato (“ <i>Sato</i> ”)
Ex. 1010	JP-2002-158360A to Takahara (“ <i>Takahara</i> ”), along with Certified Translation
Ex. 1011	U.S. Pub. No. 2001/0048109A1 to Murade (“ <i>Murade-109</i> ”)
Ex. 1012	JP-2001-331125A to Murade (“ <i>Murade-125</i> ”), along with Certified Translation
Ex. 1013	U.S. Patent No. 5,668,379 to Ono (“ <i>Ono</i> ”)
Ex. 1014	U.S. Patent No. 5,831,694 to Onisawa (“ <i>Onisawa</i> ”)

Exhibit	Description
Ex. 1015	U.S. Patent No. 6,388,721 to Murade (“ <i>Murade-721</i> ”)
Ex. 1016	U.S. Patent No. 5,748,276 to Uno (“ <i>Uno</i> ”)
Ex. 1017	L.W. MacDonald and A.C. Lowe, Display Systems (1997) (excerpts) (“MacDonald and Lowe”)
Ex. 1018	W. den Boer, Active Matrix Liquid Crystal Displays: Fundamentals and Applications (2005) (excerpts) (“den Boer”)
Ex. 1019	S. Lee et al., “Amorphous Silicon Thin Film Transistor Fabricated with a New Copper Dry Etching Method,” Electrochemical Society Proceedings, vol. 2000-31 (2000) (“Lee”)
Ex. 1020	R.C. Dorf, ed., The Electrical Engineering Handbook (2d. Ed. 1997) (excerpts) (“Dorf”)
Ex. 1025	J.W. Nilsson and S.A. Riedel, Electric Circuits (9th Ed. 2011) (excerpts) (“Nilsson”)
Ex. 1026	R.A. Street, Technology and Applications of Amorphous Silicon (2000) (excerpts) (“Street”)
Ex. 1027	J. Kanicki, ed., Amorphous & Microcrystalline Semiconductor Devices, Vol. II: Materials and Device Physics (1992) (excerpts) (“Kanicki”)
Ex. 1028	T. Yamazaki, et al., “Color TFT Liquid Crystal Displays” (1996) (excerpts) (“Yamazaki”)
Ex. 1029	S. Kaplan, Wiley Electrical and Electronics Engineering Dictionary (2004) (excerpts) (“Kaplan Dictionary”)
Ex. 1030	P.A. Laplante, Electrical Engineering Dictionary (2000) (excerpts) (“Laplante Dictionary”)
Ex. 1031	U.S. Patent No. 6,380,560B1 to Yamazaki (“Yamazaki-560”)

IV. LEGAL STANDARDS

18. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

19. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

20. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

21. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-3 of the '079 patent from the perspective of

a person of ordinary skill in the art at the earliest date in 2002 to which the '079 patent claims may be entitled to priority, as described in more detail below.

22. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

23. In forming my opinions and considering the subject matter of the '079 patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

24. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims.

25. I understand that a claimed invention is only patentable when it is new, useful, and non-obvious in light of the “prior art.” That is, the invention, as defined by the claims of the patent, must not be anticipated by or rendered obvious by the prior art.

A. Level of Ordinary Skill in the Art

26. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

27. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Claim Construction

28. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of one of ordinary skill in the art at the time of the alleged invention.

29. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand,

however, that claim terms are generally not limited by the embodiments described in the specification.

30. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

C. Prior Art

31. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

D. Anticipation

32. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

E. Obviousness

33. I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

34. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;

- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

35. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, I applied a date of invention of December 16, 2002, as discussed herein. My opinions would not change if I assumed a later date of invention.

36. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

37. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed

invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

38. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

39. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are

a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

40. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

41. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to

combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

42. I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '079 patent.

43. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

F. Legal Standards for Determining Priority Date

44. I understand that the “priority date” or “effective filing date” of a patent is the date on which it is filed, or the date on which an earlier-filed U.S. or international patent application was filed if the patentee claims the benefit of priority to that earlier-filed application.

45. I understand that in the patent application process, the applicant may keep the originally filed claims, or change the claims between the time the patent application is first filed and the time a patent is issued. An applicant may amend the

claims or add new claims. These changes may narrow or broaden the scope of the claims. I understand that a patent application is entitled to the benefit of the filing date of an earlier-filed application only if the disclosure of the earlier application provides support for the claims of the later application as required by the “written description” requirement of 35 U.S.C. § 112. I further understand that for a patent application to have an adequate written description of the invention, it must show the inventor was in possession of the invention at the time the patent application was filed.

46. When determining whether a specification of a patent application contains adequate written description of the claimed invention, I understand that one must make an objective inquiry into the four corners of the specification from the perspective of a POSITA. Further, I understand that the standard for written description is stricter than the standard for determining whether or not a patent claim would have been obvious based on the prior art.

47. In particular, the question for purposes of written description is not merely whether the claimed invention is an obvious variant of what the specification discloses. Instead, the application itself must describe the invention, and do so in sufficient detail that a POSITA can clearly conclude that the inventor invented the claimed invention as of the date when the application was filed.

48. Similarly, I understand the issue of written description is separate from the question of “enablement” (i.e., whether a specification allows a POSITA to practice the claimed invention without undue experimentation). A specification may adequately enable a claimed invention, yet fail to provide written description support.

49. Finally, I understand that the standard for whether or not a disclosure is sufficient to provide written description support for a claim is different from the standard for whether a disclosure anticipates a claim. To support a claim, the description must be sufficient to convey to a POSITA that the inventors were in possession of the full scope of the claimed subject matter. By contrast, a description anticipates a claim if it discloses even a single species within the scope of the claim. Thus, in the case of “genus” claims covering two or more different species, I understand that there can be situations in which a given disclosure is sufficient to anticipate the claim even though that same disclosure is not adequate to support the claim and entitle the inventors to an earlier priority date.

50. I understand that in order to claim priority to an application through a chain of applications, every single application in the chain (going back to the particular application on which the inventors want to rely) needs to support the claim as a matter of written description. In other words, each application in the chain must

allow a person of ordinary skill in the art to discern that the inventors were in possession of the claimed invention at the time of the application. It is not sufficient under this standard for the disclosure in the specification to render the claimed invention obvious.

V. OVERVIEW OF LCD DISPLAY TECHNOLOGY

A. Brief History of Display Technology

51. The Cathode Ray Tube (CRT) was the dominant display device from the 1940's through the end of the last century. The CRT relies on raster scanning a focused electron beam inside a large vacuum tube, allowing the beam to impinge on a phosphor coating on the inner surface of the tube. The phosphor emits light in proportion to the electron beam intensity. Pictures are thus drawn on the inner surface of the CRT with an electron beam of modulated intensity.

52. During the 1970's, interest began to arise to find a "flat panel" technology to supplant the large, heavy CRT displays. Many technologies were pursued, including electroluminescent, electro-chromic, electrophoretic, vacuum fluorescent, plasma, liquid crystal, and others. By 1990, liquid crystal displays (LCD) began emerging as the winning technology to supplant the CRT in most commercial and consumer applications. The first LCDs were low segment count, direct driven displays, such as wrist-watch and calculator displays. Each segment

had a common upper and a patterned lower electrode. These electrodes were continuously actively driven. Each segment required a separate dedicated conductor running to the segment. While this was feasible for low information content displays, passive and active matrix LCDs were required for higher pixel count display devices. Active matrix generally has brightness, contrast, response time, and viewing angle advantages over passive matrix.

53. Although there are exceptions, most commercial LCD displays comprise two outer polarizer sheets, with a glass plate adjacent to each polarizer. The inner surfaces of the glass plates have transparent indium-tin-oxide (ITO) conductive electrodes. The small gap (usually 1 to 5 micrometers) between the ITO electrodes is filled with liquid crystal material. An epoxy rim seal keeps the liquid crystal material in place.

54. There are several types of liquid crystal material, and generally several modes in which each type of liquid crystal material can be used. The types of liquid crystal materials include twisted nematic (TN), Electrically Controllable Birefringent (ECB), cholesteric, smectic, and ferro-electric, among others. Various modes include 90° twist, super (270°) twist, Polymer Dispersed (PDLC), vertically aligned (VA), In Plane Switching (IPS), Hybrid Aligned (HAN), bi-stable, normally white and normally black.

55. The industry has migrated from direct driven segmented watch and calculator displays to active matrix thin film transistor (TFT) LCD's. Consumer demand has continually grown.

B. Active Matrix Liquid Crystal Displays (AMLCDs)

56. Most LCD-based monitors and televisions today use Active Matrix Liquid Crystal Display (AMLCD) technology with Thin Film Transistors (TFTs).¹ AMLCDs use TN with a 90 degree twist, or a vertically aligned (VA) ECB with negative dielectric constant anisotropy operating in the normally black mode, or In Plane Switching (IPS). Common to each of these modes is the fact that the light transmission at each pixel (picture element) is controlled by the voltage across the pixel electrodes. In the early 2000's, most liquid crystal displays used the TN mode.

Color TFT LCDs are turning up everywhere these days.

The color TFT display, a light, slender display, with a beautiful image that does not tire the eyes even when viewed for hours at a time, is finding its way into many products, even in demanding environments, like the

¹ In addition to LCD displays, various commercial displays for smart phones, computers, television sets and other devices also use organic light-emitting diodes (OLEDs) that directly emit colored light for displaying images.

dashboard of a car. Because the color TFT display is an LCD (liquid crystal display) panel incorporating thin film transistors, it can reproduce a wider range of colors than can competing technologies. The color TFT shows extremely uniform brightness, with no color degradation or distortion, even in the corners of the screen.

Ex. 1028 [Yamazaki] at 3 (book page 1).²

The momentum the LCD industry has gained is difficult to supplant by alternative flat panel technologies. Even if, on paper, they may have advantages over LCDs.

Ex. 1018 [den Boer] at 3 (book page 7).

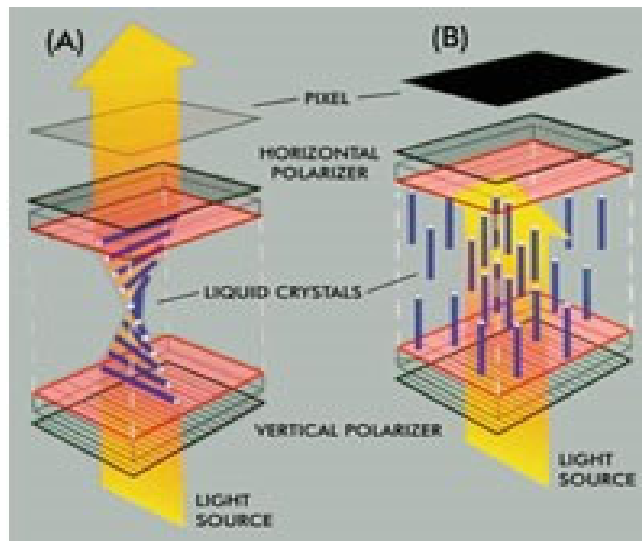
57. The quotes above testify to the fact that by the early 2000's POSITAs were well aware of the basic structure and operating principles of the ubiquitous Active Matrix Liquid Crystal Display (AMLCD). Herein below is a summary of that technology.

58. Liquid Crystal Materials (LCMs) are unusual liquids which exhibit stable states with long range order, wherein the stable state can be determined by the

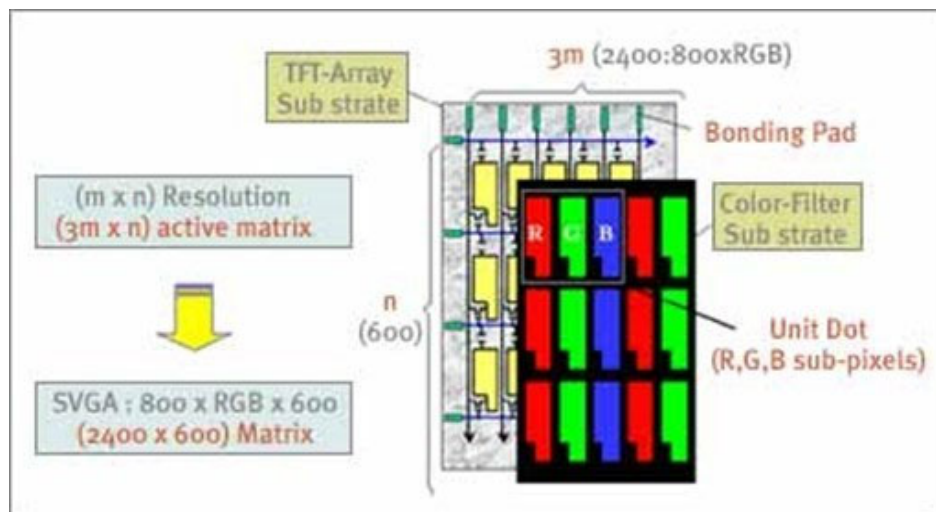
² The citations in my Declaration are made to exhibit page numbers, not original page numbers, unless noted otherwise (such as here by reference to "book page 1" in parentheses).

strength of the imposed electric field. These stable states can exhibit differing optical properties. These differing optical properties are exploited to vary the transmission of small segments (pixels or picture elements) of the display by application of an electric field.

59. A typical AMLCD comprises an array of color pixels. Each color pixel can comprise color sub-pixels, usually red, green and blue. At each sub-pixel is a sample and hold circuit, addressed by a thin film transistor, wherein the voltage across the LCM is held by a storage capacitor. There are many LCD mode in use today including twisted nematic (TN), in-plane switching (IPS), and vertically aligned (VA), but they generally all rely on modulating the polarization of light passing through the panel. Each subpixel acts like a variable shutter, allowing a level of light transmission based on the voltage across the LCM, as shown below. In the figure below, on the left there is no voltage and all light is allowed to pass. On the right, full voltage is applied, and no light is allowed to pass. At intermediate voltages, an intermediate level of light is allowed to pass.

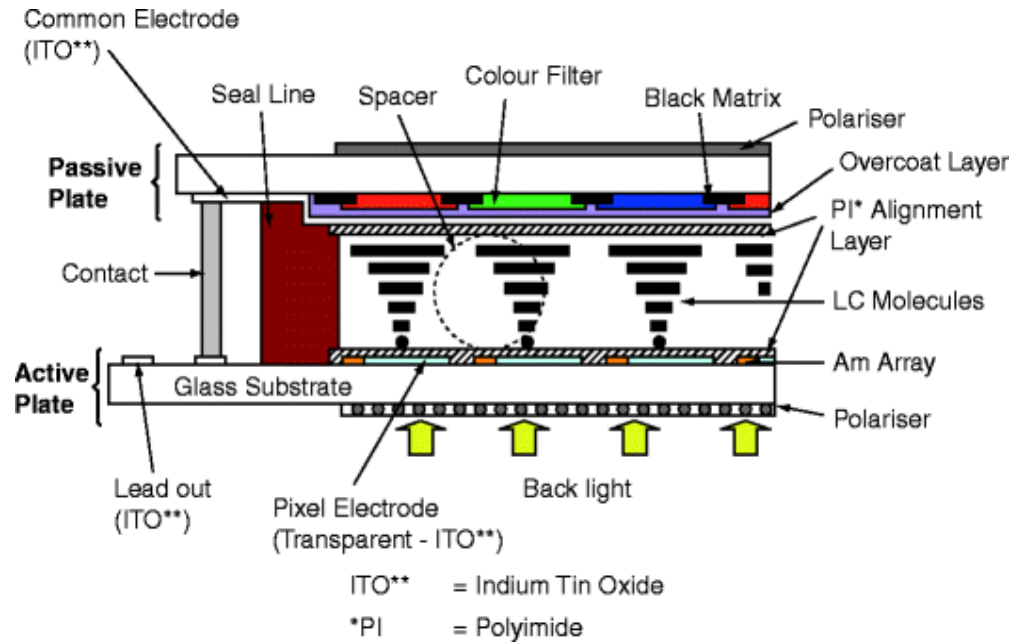


60. Each color pixel is usually organized as three or more subpixels: for example, one red, one green and one blue in various color pixel designs. The color produced by each pixel is determined by the color filter patch over each subpixel, as shown below:

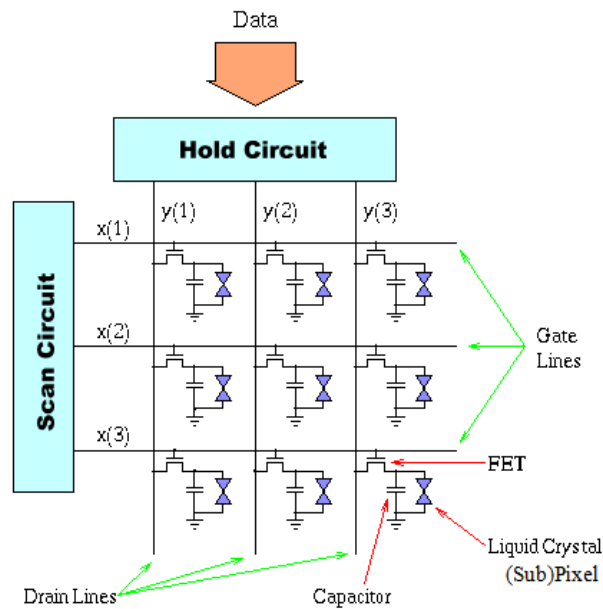


61. The specific color perceived by the human eye (including white) is determined by the proportions of red, green and blue light transmitted by each pixel.

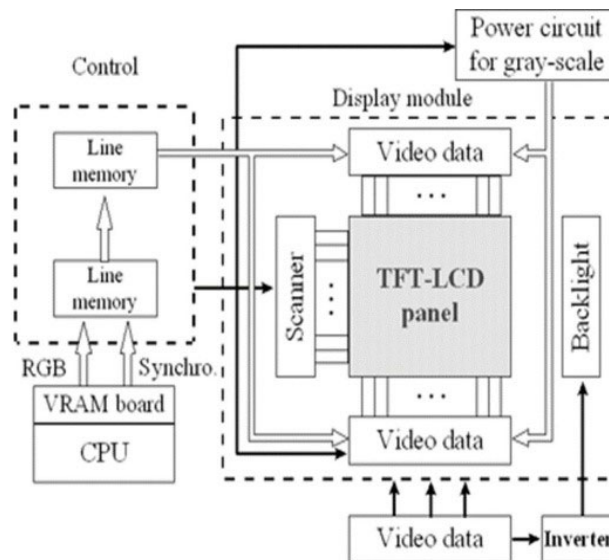
62. As previously mentioned each subpixel circuit comprises a Thin Film Transistor (TFT), a capacitor, and the LCM between the upper and lower pixel electrode. Below is a typical cross section of a pixel comprising three color subpixels:



63. I include a figure below to illustrate a typical electrical diagram of the TFT active matrix:



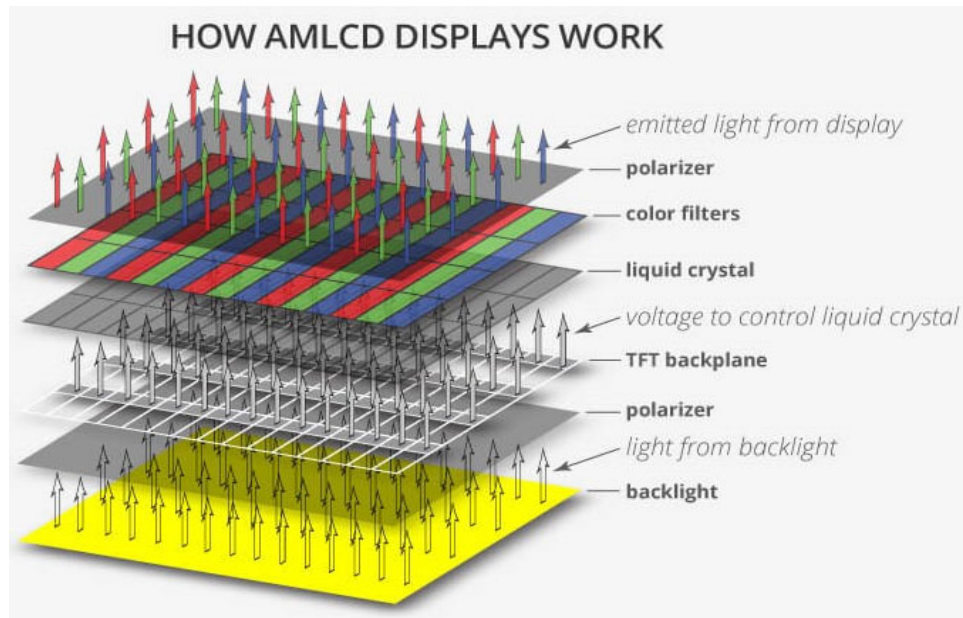
64. I further include below a block diagram of an AMLCD device.



65. Brightness information is loaded into the matrix one line (row) at a time. After the scan drive selects a line, the data driver sends the brightness voltage down all of the data lines simultaneously to program each pixel capacitor on the line

with the correct pixel brightness voltage. Then the selected line is deselected and the next line is selected for writing.

66. The physical structure of the typical AMLCD is shown below:



67. The AMLCD is a non-emissive technology where the pixels control the light passing through, rather than generating light. Therefore, virtually all AMLCDs comprise a backlight unit (BLU) as indicated in several of the images above.

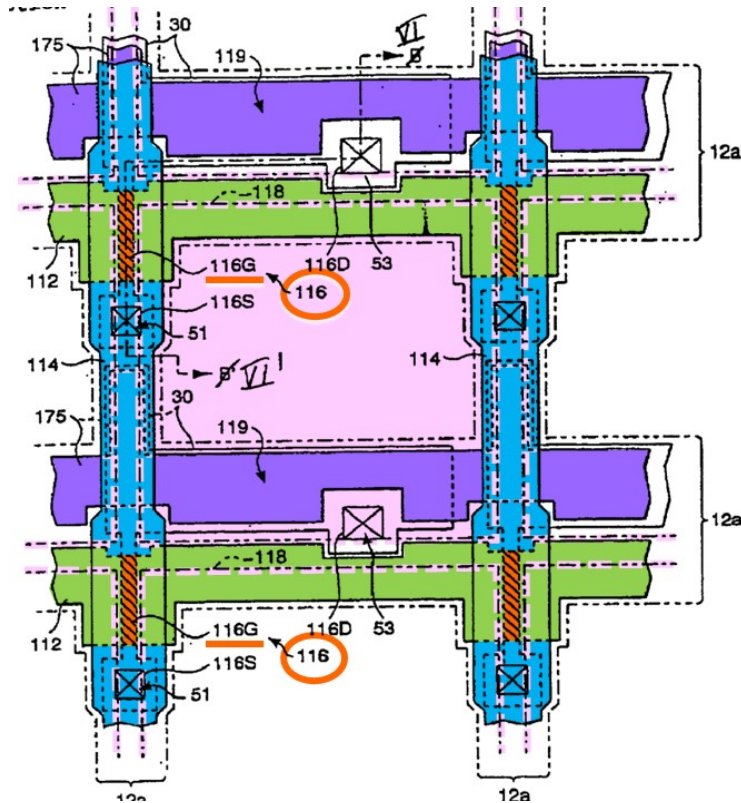
C. Line and TFT Configuration in an AMLCD

68. Before the '079 patent, an AMLCD was understood to have the following basic structure:

[O]ne substrate . . . is provided with a plurality of **scanning lines** and a plurality of **data lines** intersecting with each other. At each intersection thereof, a three-

terminal switching element, such as a **TFT (Thin Film Transistor)**, and a **pixel electrode** are formed as a set, and peripheral circuits for driving the individual scanning lines and data lines are provided in the periphery of the region (display region) in which these **pixel electrodes** are formed. The other substrate is provided with a transparent counter electrode facing the **pixel electrodes**.

Murade-109, ¶[0004] (discussing Fig. 5, below). Throughout this report, I have highlighted various terms using bold, colored text for emphasis, and highlighted and/or annotated corresponding structure in patent figures using the same colors. The coloring does not appear in the original documents.



Murade-109, Fig. 5

69. An AMLCD, such as the foregoing example, is operated by applying voltage to the TFT via signals along the scanning and data lines, causing the TFT to selectively block or transmit light through individual pixels of the display. As the '079 patent describes the state of the art, "for each pixel defined by the pixel electrodes or the scanning lines and the data lines, it is possible to control the electric field applied to the electro-optical [liquid crystal] material and to control the light transmittance." '709 patent, 1:28-38.

70. Continued development of AMLCD technology corresponded to the development of displays for personal electronic devices, such as personal computers, personal digital assistants (PDAs), mobile phones, and the like. Thus, by the mid-1990's, the industry recognized that the "needs for LCD devices as display units are increasing as information processing devices such as personal computers become smaller in size and lighter in weight and are used more widely." *Onisawa*, 1:9-12. As such, the industry sought "improvement of performance such as larger display area, higher resolution, faster response and full color." *Id.*, 1:12-14. In short, even as the art sought to reduce LCD screen size, it also sought to increase LCD screen resolution and brightness.

71. Historically, improving screen resolution and brightness of an LCD typically involved increasing pixel density (which the art referred to in terms of reducing "pixel pitch") and/or increasing the area of the aperture relative to the area of the complete light valve (also known as "aperture ratio"). *See* Ex. 1017 [MacDonald & Lowe] at 4 (book page 73). Before the '079 patent, it was understood that narrowing the width of components between the pixels could increase aperture ratio by minimizing light blockage by peripheral components and traces when the pixel is illuminated. *See* Ex. 1019 [Lee] at 3 (book page 34) ("A wide gate line is not desirable because it reduces the pixel aperture ratio and increases the line-to-line

parasitic capacitance that adds additional signal delays.”). As *Murade-109* illustrates in Figure 5, above, such narrowing included narrowing portions of the **data line** (114) and **scanning line** (112) between the **pixel electrodes** (118).

72. Even while narrowing the respective lines, however, other portions of the **data line** and **scanning line**—i.e., those forming the TFT—require certain minimum dimensions to achieve proper function. For example, den Boer taught that “[f]or larger displays, some of the key parameters are the busline resistances, which need to be low enough to minimize signal propagation delays and resulting distortions of address pulses.” Ex. 1018 [den Boer] at 6 (book page 61); *see also* Ex. 1019 [Lee] at 3 (book page 34) (noting that “gate line thickness or width needs to be increased” to achieve minimum resistance); Ex. 1031 [Yamazaki-560], 1:45-53 (“Although the improvement of an operation speed of a TFT can be made for the time being by decreasing the size of the TFT, the reduction of the channel length (or gate length) results in the short channel effect, so that disadvantages such as lowering of a drain withstand voltage is caused.”), 7:65-67 (“[W]hen the short channel effect occurs, a drain withstand voltage is lowered and deterioration of an element becomes remarkable.”). Accordingly, as shown by *Murade-109*, a POSITA understood that the TFT portions of each line may be formed broader than the other portions. Indeed, multiple sources specifically taught to provide scanning lines that are “widened at

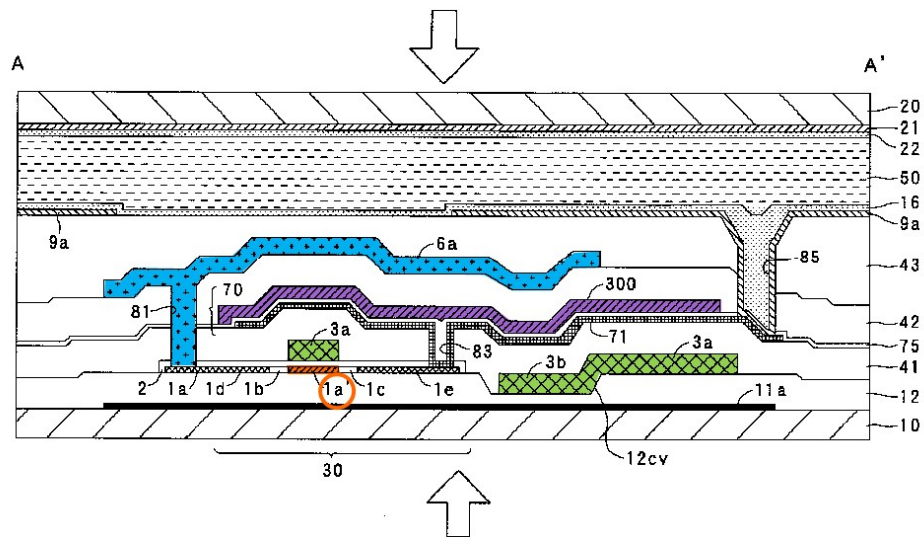
portions where they act as the gate electrodes” or are “formed with a wide width at the location at which it becomes the gate.” *Sato*, ¶[0091]; *Takahara*, ¶[0053].

73. Reducing pixel pitch presented new challenges (or exacerbated pre-existing challenges) for LCD display design. In order for the TFT of an AMLCD to function correctly, the TFT channel must be protected against light leakage, whether from the environment (e.g., sunlight or room lighting) or from the LCD backlight, which can cause problems of “flicker or the like due to changes in the transistor characteristics of the TFT.” *Takahara*, ¶[0006]. But as one reference noted, reducing pixel pitch makes it “more difficult to implement sufficient light shielding” to protect the TFT channel from such light leakage. *Takahara*, ¶[0006].

74. As background, “light shielding” is typically provided as part of the fabrication process of an AMLCD. That process will often begin with the deposition and patterning of a black matrix layer, the purpose of which is to block light in the inter-pixel areas and shield the TFT channel from ambient light. *See den Boer*, at 5 (book page 36). An opaque, low reflectance layer above the TFT channel is desirable as a light shield to prevent photo-leakage currents in the TFT and to simultaneously minimize display reflectance. *Id.* at 8 (book page 142). In reality, the TFT channel requires shielding from both ambient light as well as light generated by nearby pixels. This is because undoped amorphous silicon is a highly photoconductive

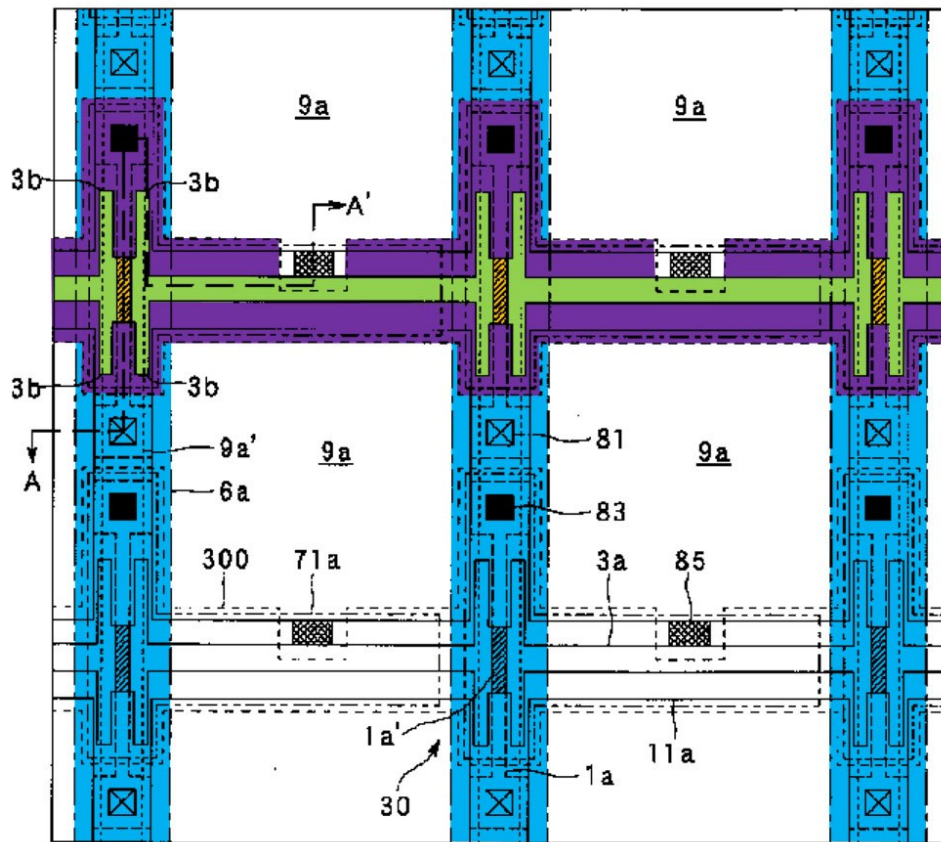
material. As a result, ambient light incident on a TFT channel can dramatically modify the electrical characteristics of the TFT, shifting the threshold voltage and inducing a photocurrent, which is “undesirable in the TFTs because it reduces the on/off ratio of the transistor and thus the ability to act as an efficient switch.” *See* Ex. 1027 [Kanicki] at 4 (book page 426). As such, it is typically necessary to include a light shield to achieve the very low leakage currents required for a display application, and is often accomplished using a metal trace over the TFT, while the underside of the TFT channel is shielded by the gate electrode. *See* Ex. 1026 [Street] at 5 (book page 159).

75. To provide necessary light shielding, the art shaped and positioned existing components (capacitor lines, data lines, and scanning lines) specifically to block light from reaching the TFT channel. For example, *Takahara* taught to use a **capacitor line** and **data line** as “light shielding films” overlapping the **TFT channel** (1a’). *Takahara*, ¶[0082], Fig. 3 (below). In this way, *Takahara*’s **capacitor line** and **data line** protected against ambient light (from the direction indicated by the top arrow) reaching the TFT channel.



Takahara, Fig. 3 (annotated)

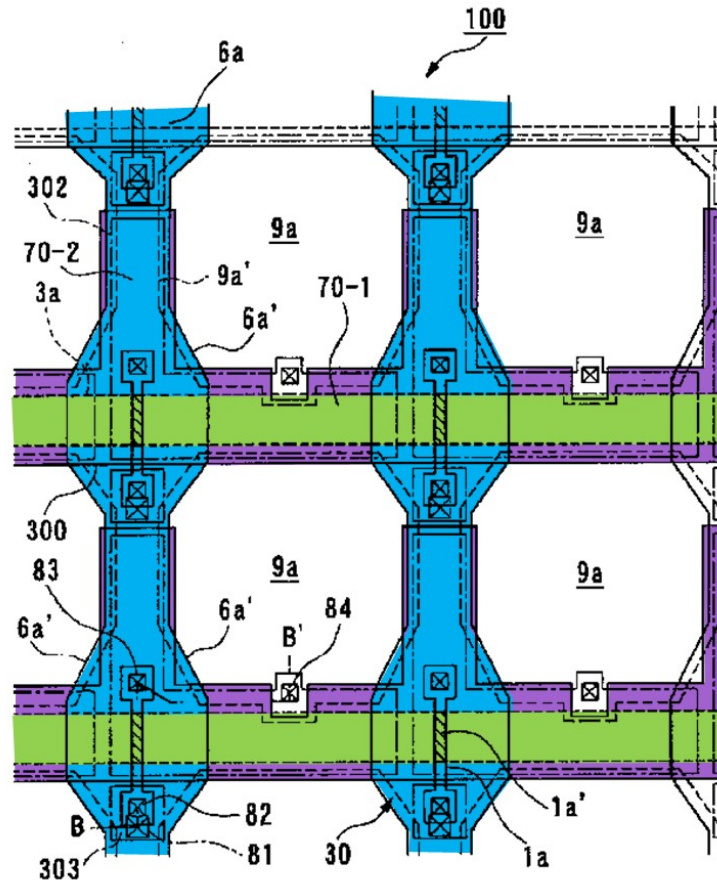
76. As additional protection, **scanning lines** could also be used to block light coming from other angles—providing them with “**protruding portions**” near the TFT gates to improve “the light-shielding performance . . . with respect to oblique light that impinges three-dimensionally from various directions.” *Takahara*, ¶[0018], Fig. 2 (below). In other words, from references such as *Takahara*, a POSITA also understood to position and shape various components to protect against *internal* light leakage (e.g., light from the pixel or LCD backlight that might reflect back toward the TFT channel).



Takahara, Fig. 2 (annotated)

77. Even further protection was provided to address light coming from the corners of each pixel electrode, which presented a particular source of light leakage. See *Kurashina*, ¶¶[0015]-[0017]. Specifically a POSITA understood that, the **data line** could be “formed with a wide width in the vicinities of the TFTs 30, as shown in FIG. 3, and made to serve as light-shielding layers against the incidence of light from the corner portions of the pixel electrodes 9a.” *Kurashina*, ¶[0052], Fig. 3 (below). According to references like *Kurashina*, the **data line** (6a) may be shaped

to vary from a narrow width (e.g., narrower than an overlapped portion of the **capacitor line**) to a broad width at portions overlapping the TFT.



Kurashina, Fig. 3 (annotated)

78. Thus, in summary, a POSITA understood the challenges of improving the quality of an active-matrix controlled electro-optical LCD display, as well as the related consequences of light leakage. A POSITA further understood the solutions to those challenges and problems, including using widened portions of the data line, capacitive line, and scanning line to shield against light leakage. A POSITA further

understood the requirement to use a relatively wide/long gate portion in order to achieve desired TFT functionality.

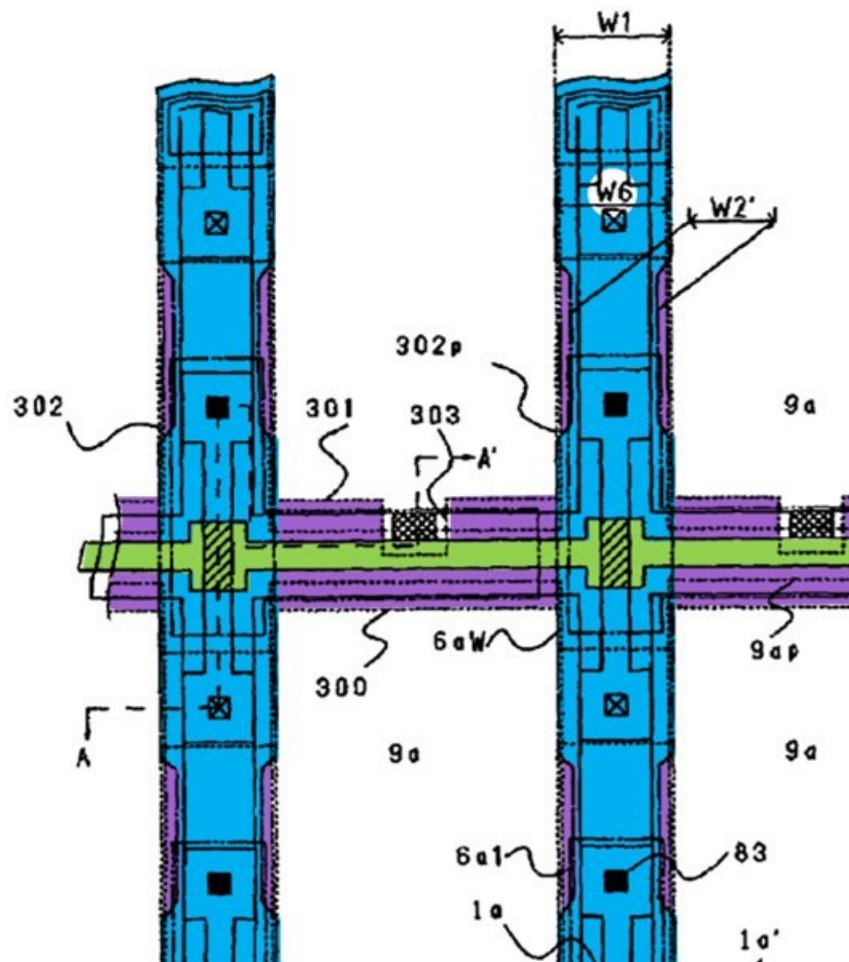
VI. THE '079 PATENT

A. Overview of the '079 Patent

79. By way of background, the '079 patent discloses the general structure and configuration of an active-matrix drive for an electro-optical device, such as an LCD, acknowledging that the components thereof were known in the “related art.” *See* Ex. 1001, 1:28-38.

80. The '079 patent identifies the same LCD challenges and provides the same solutions that, as discussed above, a POSITA already understood. Specifically, the '079 patent purports to address the technical problems associated with “precisely driving the TFTs [of an electro-optical device] . . . while satisfying the high precision [i.e., ‘high-definition’] and miniaturization requirements imposed in related art electro-optical devices.” '079 patent, 1:45-48. And the patent suggests solving those problems by shaping its signal lines to have varied widths—i.e., (1) providing a **scanning line** with a “broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor” and (2) forming a **data line** “locally broad” at the portion “overlapping the thin-film transistor” such that “light entered from the upper portion of the thin-film transistor can be more securely

prevented or reduced.” ’079 patent, 2:33-36, 8:66-9:7. The ’079 patent illustrates this varied-width design in a “third exemplary embodiment,” illustrated below in Figure 16, in which a vertical “**data line** 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad.” Ex. 1001, 22:65-23:1.



Ex. 1001, Fig. 16 (annotated)

81. In the illustrated embodiment, the data line has two main widths: W2' (narrow portion) and W6 (wide portion). '079 patent, 23:1-7. The **capacitive line** (300) has a projection (302p) of width W1, which is described as "broader than a width W2'" and "almost equal to a width W6 of the broad width portion 6aW in the data line 6a1." *Id.* In claim 2, the widths relate to each other as follows: $W2' < W1 < W6$. *Id.* The '079 patent explains that "since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 ... exist on the TFT 30, [a] so called ... double light-shielding effect can be obtained" and "thus light leak current [into the TFT] can be reduced or minimized." '079 patent, 23:24-30. (Of course, as noted above in paragraphs 71-72 and 77, a POSITA already understood to make the data line locally wide in this fashion.)

82. As also illustrated in Figure 16, a horizontal **scanning line** 3a is provided. '079 patent, 23:11. The **scanning line** has a narrow-width portion between the pixels and a broad-width portion at the channel area where the scanning line intersects with the data line. Although the '079 patent does not specifically describe the geometry of the scanning line in Figure 16, it describes a similar (if not identical) scanning line configuration appearing in Fig. 2. '079 patent, 14:25-30. The description and illustration of the scanning line in Figure 2 generally apply to the scanning line in Figure 16, because, as the '079 patent states, "reference numerals in

FIGS. 16 to 19 indicate the same elements as in FIGS. 1 to 15 . . . when they indicate[] substantially equivalent elements.” ’079 patent, 22:61-64. According to the ’079 patent, providing a locally broad scanning line (as illustrated in Figure 16) may “simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices.” *Id.*, 2:57-3:2. In other words, as the art already understood (*see* paragraphs 71-72 above), a narrow scanning line facilitates increased pixel density, while broadening the portion of the scanning line at the channel area ensures requisite TFT-gate length.

83. The foregoing features of the “third embodiment” of the ’079 patent are required by each of the patent’s two independent claims, as summarized in the following chart.

Independent Claim 1	Independent Claim 2
“ data line having a <u>broad-width portion</u> that <u>overlaps the channel area</u> ”	“ data line having a <u>broad portion</u> that <u>overlaps the thin-film transistor</u> ”
“ scanning line having a <u>broad-width portion</u> in a portion <u>overlapping the channel area</u> of the thin-film transistor”	“ scanning line having a <u>broad-width portion</u> in a portion <u>facing the channel area</u> of the thin-film transistor”

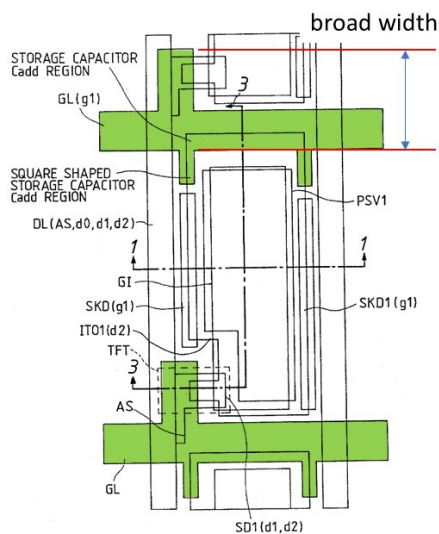
“ capacitive line ” portion with a “width that is <u>equal to or broader than a width of the data line</u> ”	“ capacitive line ” portion with a “width that is <u>narrower than the broad portion of the data line</u> and . . . <u>wider than the non-broad portion of the data line</u> ”
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B. Prosecution History of the '079 Patent and its U.S. Parent Application

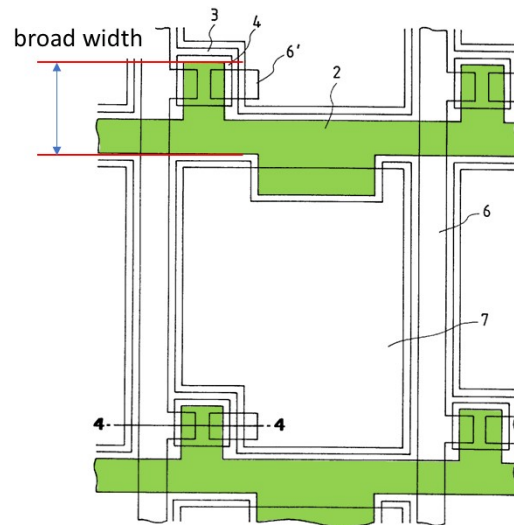
84. I have reviewed the prosecution history of the application that led to the '079 patent. Ex. 1004. I have also reviewed the prosecution history of the U.S. parent application to which the '079 patent claims priority. Ex. 1005. I understand that the prosecution of one patent application may be relevant to understand the disclosure and claims of a related application. Below I summarize certain events in the prosecution of both patents.

85. In the parent application, the patent applicant originally claimed a scanning line having a similar geometry to the scanning line later claimed in the '079 patent. Ex. 1005 at 157 (3/12/2003 Preliminary Amendment). Specifically, claim 1 of the parent application recited a “scanning line having a broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.” *Id.* The patent examiner rejected the claim, finding the “scanning line” feature was disclosed by at least two prior art

references— *Ono* (Ex. 1013, U.S. Patent No. 5,668,379) and *Onisawa* (Ex. 1014, U.S. Patent No. 5,831,694). Ex. 1005 at 133-134 (7/12/2004 Office Action). According to the examiner, *Ono* disclosed “scanning lines having a broad width portion (fig. 2, ref. GL)” and *Onisawa* disclosed “the broad portion of the scanning line as a gate electrode (fig. 3, ref. 2) in a portion facing a channel area of a respective TFT.” *Id.* at 134. Below, I have highlighted the scanning lines of *Ono* and *Onisawa* that the examiner relied upon when making the rejection.

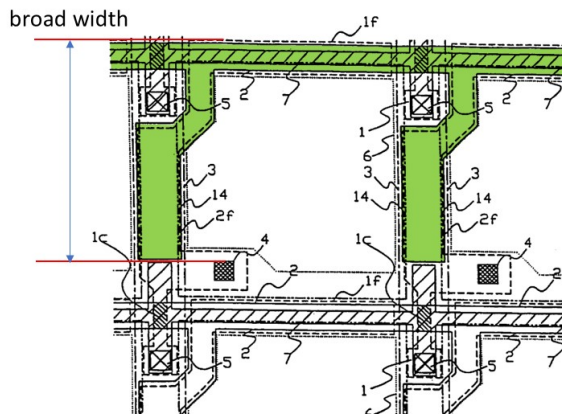


Ono, Fig. 2 (annotated)

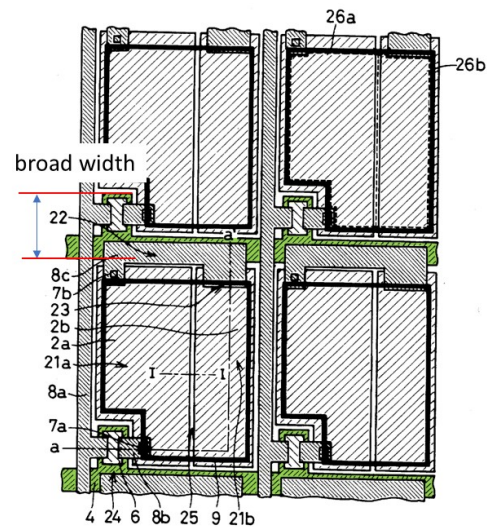


Onisawa, Fig. 3 (annotated)

86. Later, the patent examiner rejected a claim reciting the same “scanning line” limitation based on two additional references— *Murade-721* (Ex. 1015, U.S. Patent No. 6,388,721) and *Uno* (Ex. 1016, U.S. Patent No. 5,748,276. Below, I have highlighted the “scanning line” depicted by each reference.



Murade-721, Fig. 1 (capacitive line 2 highlighted)



Uno, Fig. 1a (capacitive line 4 highlighted)

87. Following additional prosecution, the parent patent application was later allowed based on an additional feature of “the broad width portion and the channel area extending in a direction extending from the channel area to the contact hole, the contact hole electrically connecting the channel area and the data line.” See Ex. 1005 at 11 (5/10/2006 Request for Reconsideration). Ultimately, the patent applicant did not dispute that a capacitive line having a broad-width portion was known in the prior art.

88. During prosecution of the parent application, the '079 patent was filed as a “divisional” application. Ex. 1004 at 43. In the new application, the examiner rejected the originally filed claims based on the same *Murade-721* and *Uno* references applied to the parent application. Ex. 1004 at 34-35 (6/13/2008 Office

Action). As the examiner explained, both references included a “scanning line having a broad width portion.” *Id.*

89. In response, the applicant for the '079 patent did not dispute that a “broad width portion” of a scanning line was known (just as the applicant did not dispute that fact during prosecution of the parent application). Ex. 1004 at 27-29 (8/15/2008 Amendment). Instead, the patent applicant argued that the prior art did not disclose (a) “a contact hole . . . positioned at a portion of the broad-width portion of the data line” as recited in claim 5 (which later issued as claim 1) and (b) “a capacitive line [with a] portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line” as recited in claim 6 (which later issued as claim 2). *Id.* at 29.

90. Later, in an examiner interview, the applicant for the '079 patent focused on the “capacitive line” limitation, arguing that *Murade-721* and *Uno* lack a “capacitive line having a . . . portion extending along the data line having a width that is equal to or broader than a width of the data line, as recited in claims 5 and 6.” Ex. 1004 at 21 (8/29/2008 Interview Summary). Contrary to the applicant’s argument, the foregoing “equal to or broader” feature appeared *only* in application claim 5 (now claim 1) and *not* in application claim 6 (now claim 2). The examiner,

however, did not remark on that discrepancy, and simply allowed the claims without further explanation. Ex. 1004 at 13 (12/2/2008 Notice of Allowance).

C. Priority Date for the '079 Patent Claims

91. As part of my analysis, I have been asked to consider whether JP-2002-000713 (“JP-713,” Ex. 1006), the January 7, 2002, Japanese priority document discloses the subject matter claimed in the '079 patent. It is my opinion that the claimed subject matter is not disclosed in the January 7, 2002, Japanese priority document, for the reasons stated below.

92. Claims 1-3 of the '079 patent require a combination of several limitations that were not disclosed in JP-713. Claim 1 requires (a) a “data line having a broad-width portion that overlaps the channel area” and (b) a “capacitive line having . . . a portion extending along the data line [with] a width that is equal to or broader than a width of the data line.” Similarly, claim 2 (and claim 3 which depends from claim 2 and incorporates all its limitations) requires (a) a “data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor” and (b) a “capacitive line having . . . a portion extending along the data line [with] a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

93. In the '079 patent, written description for the foregoing claim features appears (if at all) only in the “third exemplary embodiment,” which is described in column 22:48-24:15 and illustrated in Figs. 16-19. Those text and figures, however, do not appear in JP-713. Rather, JP-713 includes only Figures 1-10, which correspond to Figs. 1-7 and 20-22 of the '079 patent. Additionally, JP-713's description of embodiments (¶¶[042]-[094]) corresponds directly to column 12:1-19:2 and column 24:16-25:49 of the '079 patent, which do not describe the claimed “third exemplary embodiment.”

94. In my assessment, JP-713 illustrates only a data line having a *uniform width*—i.e., no “broad portion” or “non-broad portion.” *See, e.g.*, Ex. 1006, Fig. 2 (element 6a), Fig. 5 (element 6a). Likewise, JP-713 discloses only a capacitive line that is *narrower* than the data line—i.e., not “equal to or broader than a width of the data line” or “wider than the non-broad portion of the data line.” The text of JP-713 does not describe any alternative configuration that would support the features later claimed in the '079 patent. *See, e.g.*, Ex. 1006, ¶[0061] (describing relationship between data line and capacitance line in Fig. 2).

95. Because JP-713 does not disclose the subject matter claimed in the '079 patent, it is my understanding that the '079 patent claims are not entitled to priority any earlier than December 16, 2002 (the date of the second Japanese priority

document, JP-2002-363864) or December 17, 2002 (the date of the U.S. priority application no. 10/320,371). I have not examined the latter two priority documents to determine whether they disclose the subject matter claimed in the '079 patent, because I have been advised that each reference analyzed in my declaration qualifies as prior art *at least* based on the asserted December 2002 priority dates.

D. Person of Ordinary Skill in the Art

96. I am informed that patentability must be analyzed from the perspective of “one of ordinary skill in the art” in the same field as the '079 patent at the time of the invention. I am also informed that several factors are considered in assessing the level of ordinary skill in the art, including (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the field.

97. In my opinion, a person of ordinary skill in the art pertinent to the '079 patent as of its earliest priority date would have had at least a at least a four-year undergraduate degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional education could substitute for professional experience and vice versa. For example, a master’s degree in electrical

engineering, computer science, physics, or a similar field can be a substitute for two years of experience designing semiconductor display devices. Although I surpass this definition of one of ordinary skill in the art now and when the '079 patent application was first filed in 2002, my analysis regarding the '079 patent has been based on the perspective of one ordinary skill in the art as of the priority date of the '079 patent.

98. I am also familiar with the knowledge of the person of ordinary skill in the art as of the priority date of the '079 patent. I am able to opine on how the person of ordinary skill in the art would have understood the disclosure and claims of the '079 patent, the disclosures of the prior art, the motivation to combine the prior art, and what combinations would have been obvious to one of ordinary skill in the art.

VII. CLAIM CONSTRUCTION OF TERMS OF THE '079 PATENT

99. As I discussed above, I have been informed that for purposes of *inter-partes* reviews, the standard for claim construction of terms within the claims of the patent is the same as that applied in federal district court litigation.

100. Except for the terms identified below, I have been asked to assume that the claim terms generally have their plain and ordinary meaning to a person skilled in the art in light of the specification and the prosecution history. I expect to respond in the event that Patent Owner proposes or the Board adopts a different construction.

101. Each claim of the '079 patent requires one or more components with a “broad-width portion” or a “broad portion.” Specifically, claim 1 recites a “data line having a *broad-width portion*” and a “scanning line having a *broad-width portion*.” Claim 2 recites a “data line having a *broad portion*” and a “scanning line having a *broad-width portion*.” Under their plain meaning, the terms “broad width portion” and “broad portion” are terms of relative size, connoting that the portion is broader than another portion of the subject element.

102. The '079 patent appears to set forth its own definition of “broad width”; however, I note that the definition is consistent with the ordinary meaning of the term:

Further, in the present invention, “broad width” means that it is broader than the width of the “narrow width portion,” and “narrow width” means that it is narrower than the width of the “broad width portion”. In short, the broad and narrow degree of “the broad width portion” and the “narrow width portion” is determined in accordance with the relative relationship between them.

'079 patent, 3:17-23.

103. In my opinion, the foregoing definition of “broad width” and the plain and ordinary meaning of “broad width portion” and “broad portion” all point to the

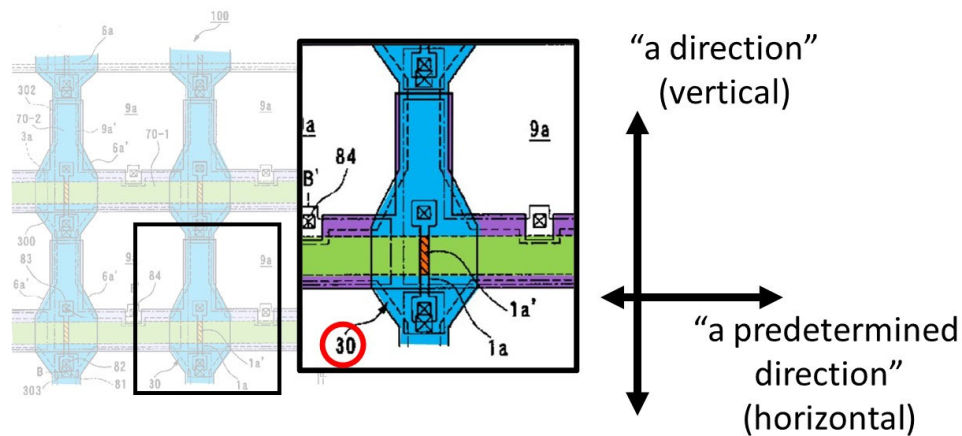
same understanding of the claim terms. That is, a “broad width portion” and a “broad portion” both mean “a portion that is broader than another portion of the subject element.”

VIII. SUMMARY OF OPINIONS ON UNPATENTABILITY

104. In my opinion, claims 1-3 of the '079 patent are unpatentable based on combinations of prior art.

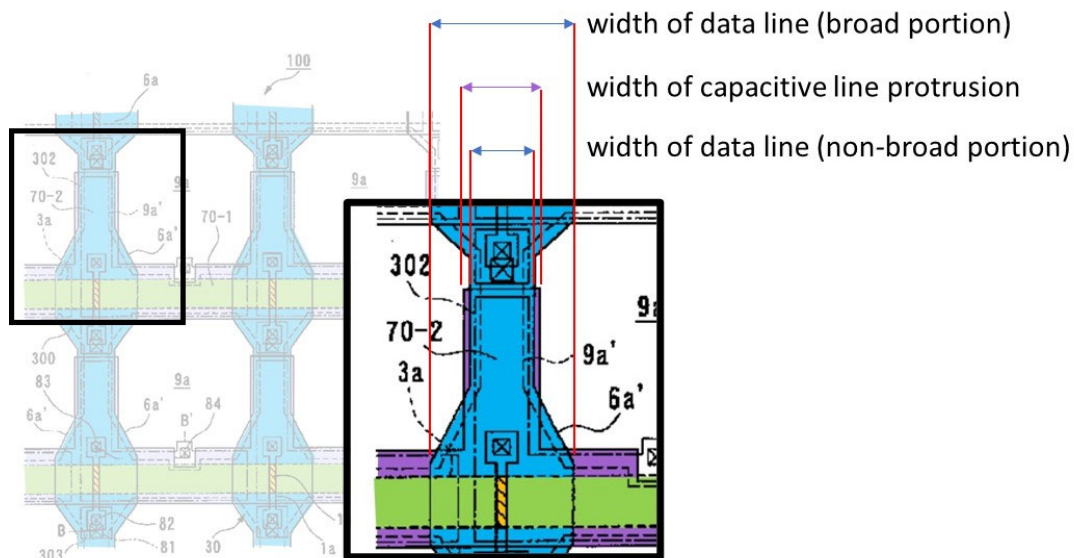
105. The '079 patent suggests that the relative widths of its data line, scanning line, and capacitive line provided an advance over the prior art. The features appear in challenged independent claims 1 and 2. During prosecution, the applicant also identified the claimed “contact hole” (recited in claim 1 and dependent claim 3) as an advance. All such features, however, were well known before the application for the '079 patent was filed.

106. *Kurashina*, for example, discloses “**data lines** 6a,” which “extend linearly, but have **wide portions** 6a’ . . . at the portions where they intersect with the scanning lines 3a.” *Kurashina*, ¶[0055].



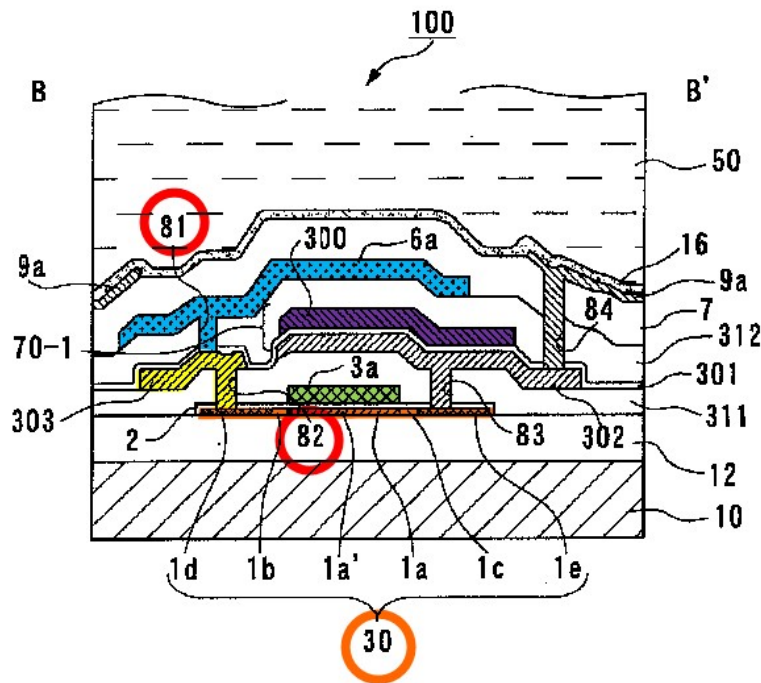
Kurashina, Fig. 3 (annotated)

107. The *Kurashina* reference also teaches a projecting portion of the **capacitance line** 300 (extending vertically in the image below) that is both *narrower* than the broad portion of the **data line** and *wider* than the non-broad portion of the **data line**, as illustrated below.



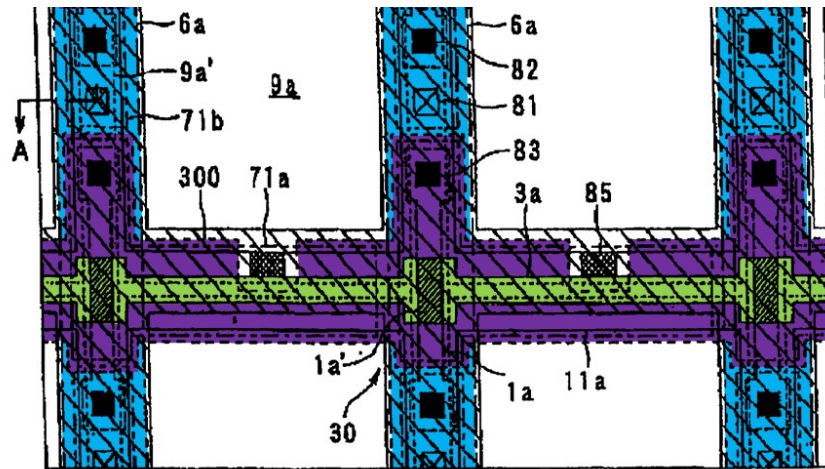
Kurashina, Fig. 3 (annotated)

108. As to the “contact hole” limitations, *Kurashina* depicts **contact holes** 81, 82 positioned beneath a broad-width portion of the **data line** (6a) that extends from the **channel area** (1a’ of TFT 30) toward the **contact holes**.



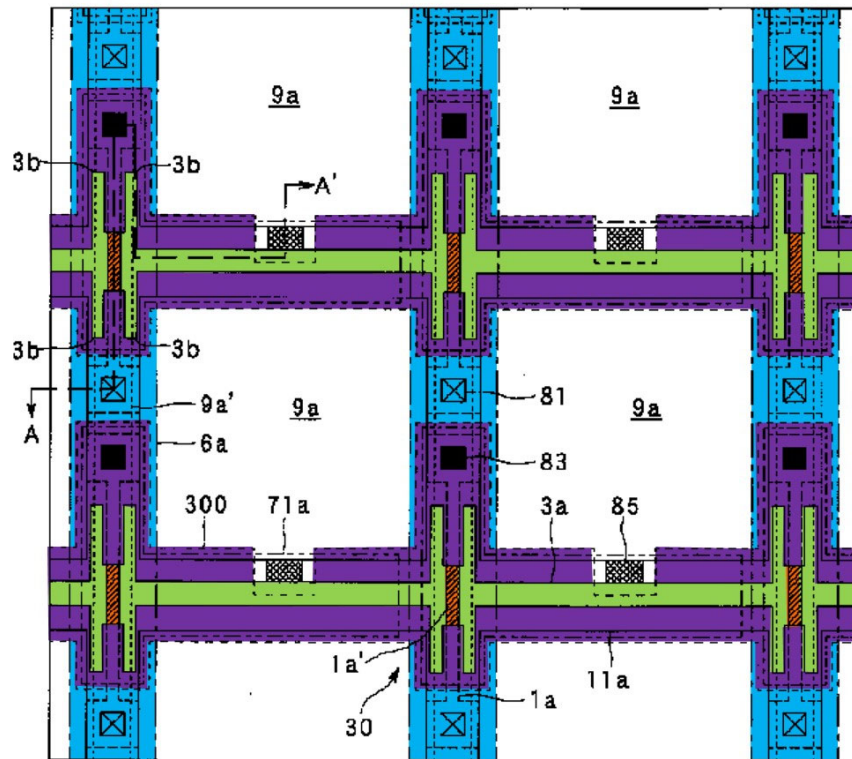
Kurashina, Fig. 4 (annotated)

109. As a second example, *Sato* discloses “**scanning lines** 3a [that] are widened at portions where they act as the gate electrodes,” as illustrated below. *Sato*, ¶[0091], Fig. 2. That is, *Sato* teaches providing scanning line with a broad/broad-width portion, as illustrated below.



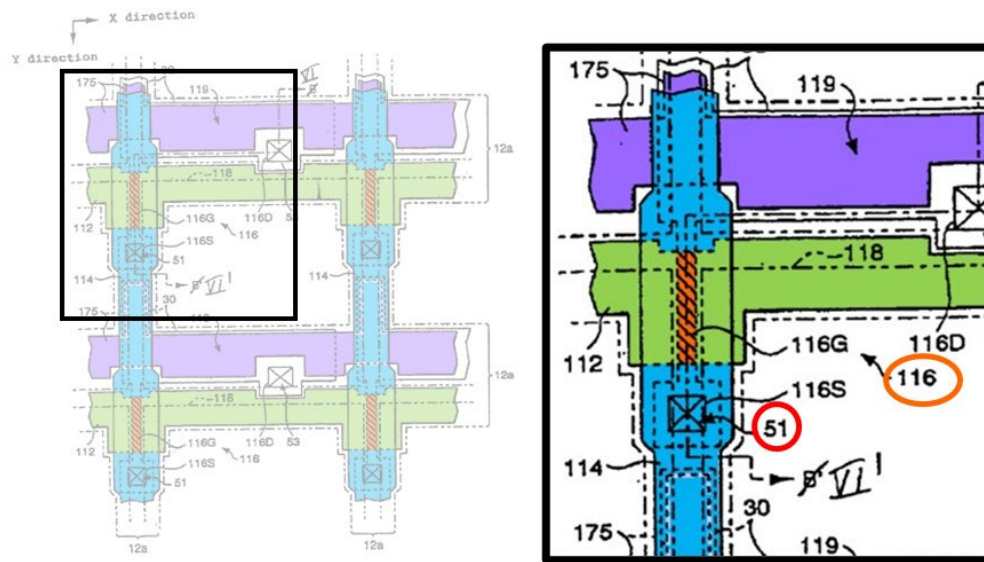
Sato, Fig. 2

110. As another example, *Takahara* discloses a “**protruding portion 3b**” of a **scanning line 3a**, overlapped by a **data line 6a** as illustrated below. *Takahara*, ¶¶[0053], [0079]. According to *Takahara*, the **protruding portion 3b** is provided specifically to protect the TFT **channel (1a’)** against “incident light and return light that obliquely travel with respect to the substrate surface of the TFT array substrate.” *Id.*, ¶¶[0079], [0081]. In other words, *Takahara* teaches providing scanning line with a broad/broad-width portion.



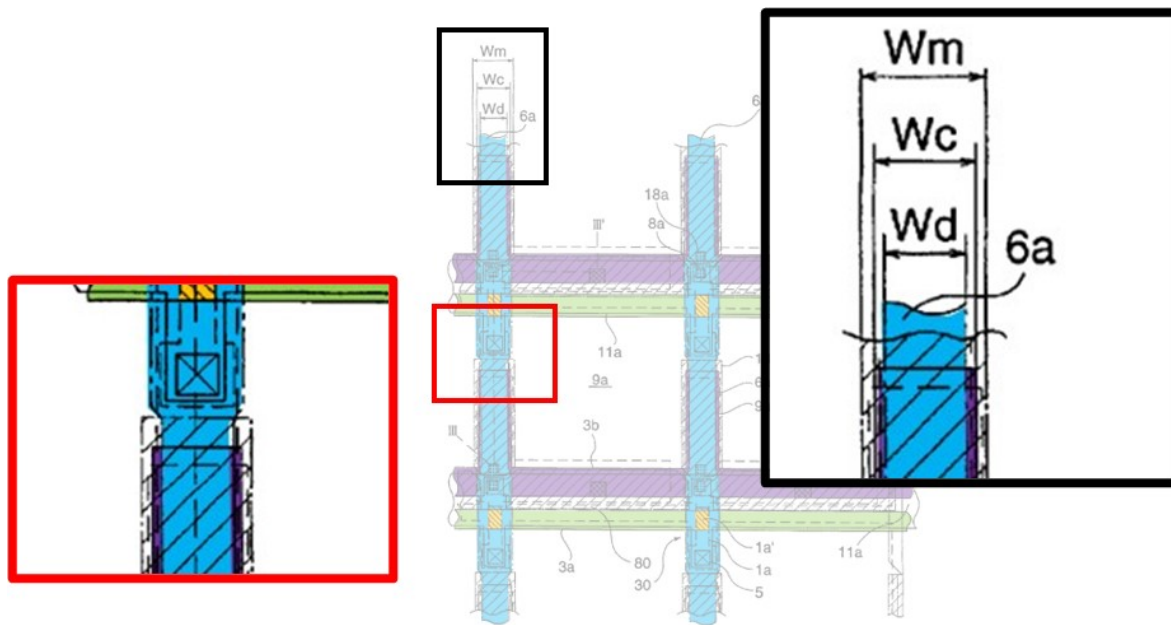
Takahara, Fig. 2 (annotated)

111. Still another example of the prior-art disclosing the relative-width features of the '079 patent claims is found in *Murade-109*, a prior-art patent application filed by the same inventor of the '079 patent. *Murade-109* discloses “principal elements, such as the **data line** 114, the **scanning line** 112, the **capacitor line** 175, and the **TFT** 116,” as illustrated below. *Murade-109*, ¶[0135]. *Murade-109* also shows a **contact hole** (51) positioned beneath a broad-width portion of the **data line** (114) that extends from the **channel area** (116, **gate portion** 116G highlighted) toward the **contact hole**.



Murade-109, Fig. 5 (annotated)

112. Finally, the prior-art *Murade-125* reference—yet another application filed by the same inventor as the '079 patent—discloses making a **capacitive line** extension (extending along the **data line**) with a width (W_c) *broad*er than a non-broad portion of the **data line** (width W_d), as illustrated below.



Murade-125, Fig. 2 (annotated detail)

113. The *Murade-125* reference was submitted to the USPTO during prosecution of the '079 patent (unlike *Kurashina*, *Takahara*, and *Murade-109*, which were not submitted). Ex. 1004 at 113. I understand, however, that the *Murade-125* reference was submitted only in the Japanese language with no English-language abstract or translation. Ex. 1004 at 113. And neither the examiner nor the patent applicant addressed the fact that *Murade-125* disclosed the same feature that the patent applicant argued distinguished its claims over the asserted prior art—i.e., a “capacitive line having a . . . portion extending along the data line having a width that is equal to or broader than a width of the data line.” Ex. 1004 at 21 (8/29/2008 Interview Summary).

114. As detailed herein, *Kurashina* and *Murade-109* form the basis for my opinions that the subject matter of claims 1-3 of the '079 patent was well known to a POSITA. More specifically, in the analysis that follows, I identify the following combinations of prior art that, in my opinion, anticipate and/or render obvious the claims:

Ground	Claims	Prior Art
1	1-3	<i>Kurashina</i> (Ex. 1008) in view of <i>Sato</i> (Ex. 1009)
2	1-3	<i>Kurashina</i> (Ex. 1008) in view of <i>Takahara</i> (Ex. 1010)
3	1-3	<i>Murade-109</i> (Ex. 1011) in view of <i>Murade-125</i> (Ex. 1012)

IX. GROUND 1: KURASHINA IN COMBINATION WITH SATO RENDERS OBVIOUS CLAIMS 1-3

115. As detailed below, *Kurashina* (Ex. 1008) together with *Sato* (Ex. 1009) provide every feature of claims 1-3 and, in my opinion, a POSITA would have found each claim to be obvious over the combination of references.

116. *Kurashina* recognized the challenge of light leakage posed by the industry's push to decrease the pixel pitch and improve aperture ratio of LCD displays—in particular the challenge posed by light leakage from the corners of the LCD pixels. *Kurashina*, ¶¶[0015]-[00017]. *Kurashina* solved that challenge by

widening portions of the data line near the TFT—i.e., near the corners of the pixels. *Kurashina*, ¶[0052] (data line “formed with a wide width in the vicinities of the TFTs 30, as shown in FIG. 3, and made to serve as light-shielding layers against the incidence of light from the corner portions of the pixel electrodes 9a.”).

117. As detailed below, *Kurashina*’s data line and capacitance line provide the same light-shielding functionality as the analogous components claimed in the ’079 patent. *Kurashina* further discloses other limitations of the challenged claims as detailed below.

118. To the extent it is argued that *Kurashina* does not explicitly disclose a scanning line having a broad-width portion, it is my opinion that a POSITA would have considered it obvious to provide the feature, not least because the feature was very well known as the patent examiner established (and the patent applicant did not dispute) during prosecution of the ’079 patent. *See* Section VI.B above. Moreover, the POSITA’s knowledge and understanding would have been confirmed based on teachings in other relevant references, including, for example, *Sato* (Ex. 1009) that widening a portion of the scanning line near the TFT would, at a minimum, be an obvious design choice. As I explain below in Ground 2, *Takahara* (Ex. 1010) teaches a similar feature, and also teaches to provide the scanning line with a protruding portion (3b) specifically to protect the TFT channel (1a’) against

“incident light and return light that obliquely travel with respect to the substrate surface of the TFT array substrate.” *Takahara*, ¶¶[0079], [0081].

A. Independent Claim 2

119. In my analysis of the '079 patent claims, I will address independent claim 2 (and its dependent, claim 3) before independent claim 1. Claim 2 is, in some respects, the broader claim because claims 1 and 3 generally include the same or similar elements but add a “contact hole” feature. Thus, it makes logical sense to address claim 2 first.

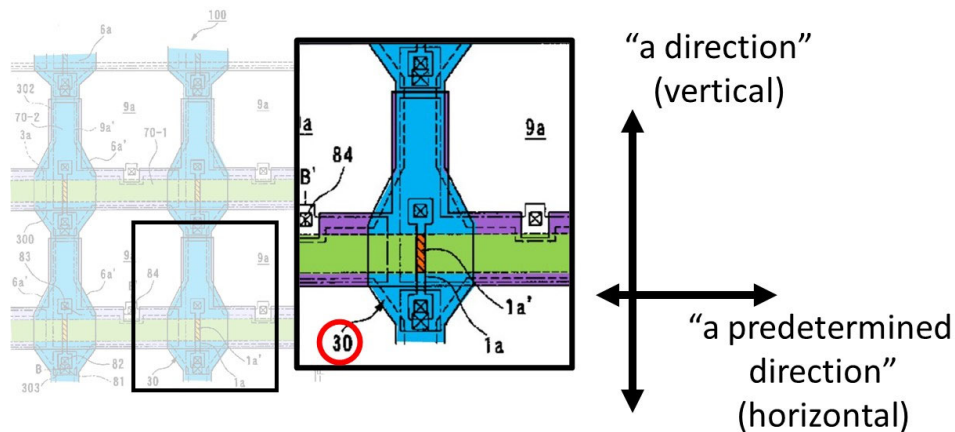
2[pre] An electro-optical device, comprising:

120. *Kurashina* teaches the preamble of claim 2. *Kurashina* discloses “an electro-optical device having improved light blocking performance at the corners of pixel electrodes.” *Kurashina*, ¶[0001].

2[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

121. *Kurashina* discloses 2[a]. *Kurashina* discloses a “pixel switching **TFT 30**” having a “**channel region 1a**’.” See *Kurashina*, ¶[0032]. While the foregoing text specifically relates to Figure 1, *Kurashina* states that “in Figs. 3 and 4, components having the same functions as those in Figs. 1 and 2 are denoted by the same reference numerals.” *Kurashina*, ¶[0053]. Thus, the “**TFT 30**” and a

“**channel region 1a**” are highlighted in Figure 3 below. *See also Kurashina*, ¶[0054] (identifying “TFT 30” in Figure 3).



Kurashina, Fig. 3 (annotated)

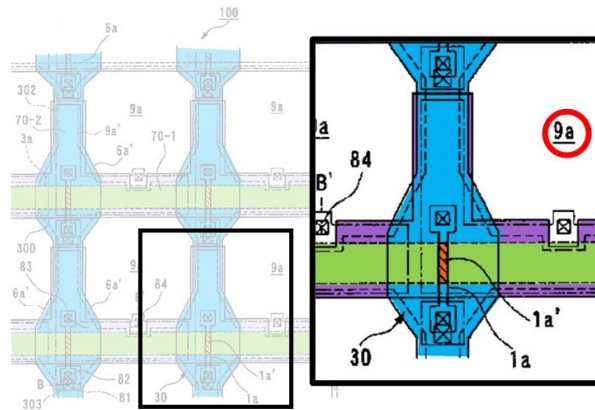
122. As illustrated in Figure 3 above, the channel area (**channel region 1a**) extends in a direction (vertical) and intersects a predetermined direction (horizontal) that intersects the direction.

123. Thus, *Kurashina* discloses “a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction.”

2[b] a pixel electrode formed correspondingly to the thin-film transistor;

124. *Kurashina* discloses 2[b]. In *Kurashina*, “a plurality of transparent **pixel electrodes 9a** [are] provided in a matrix shape in a pixel portion on a TFT array substrate,” as illustrated below. *Kurashina*, ¶[0054]. Further, a POSITA would

understand that the pixel electrode is “formed correspondingly to the thin-film transistor,” as claimed, because the “pixel-switching TFT 30, which is for performing switching control of the corresponding pixel electrode 9a, is provided in a corner portion of *each of the pixel electrodes 9a* along the corresponding data line 6a”—and each TFT connects to and controls a specific pixel electrode. *Id.* (emphasis added).

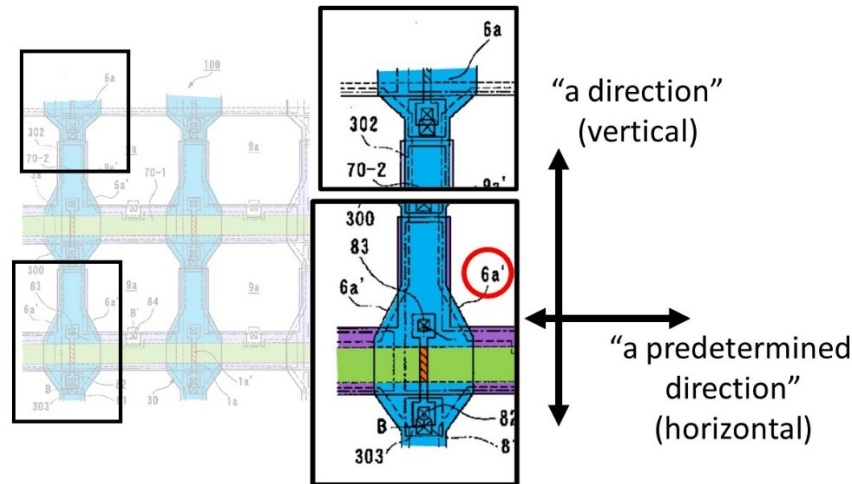


Kurashina, Fig. 3 (annotated)

2[c] a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, the broad portion being wider than the non-broad portion;

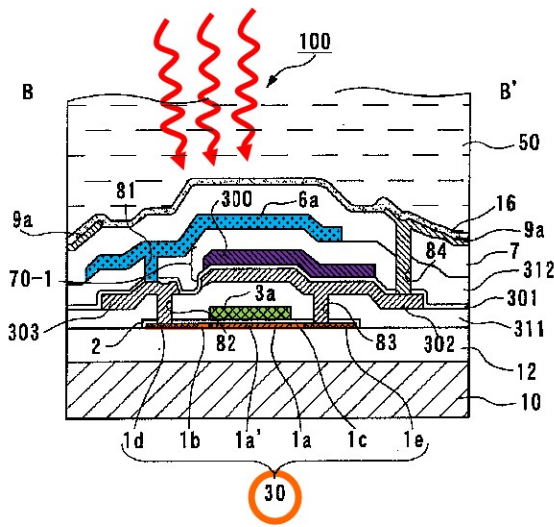
125. *Kurashina* discloses 2[c]. In *Kurashina*, the “**data lines** 6a and the **scan lines** 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a.” *Kurashina*, ¶[0054]. As illustrated below, the data line extends vertically, which is “in the direction in which the channel area [highlighted

orange below] extends.” According to *Kurashina*, “[t]he **data lines** 6a extend linearly but have **wide-width portions** 6a’ . . . at portions intersecting the scan lines 3a.” *Id.*, ¶[0055]. The “wide-width portions” (6a’) are a “broad portion,” as claimed, because they are relatively broader than another portion of the data line.

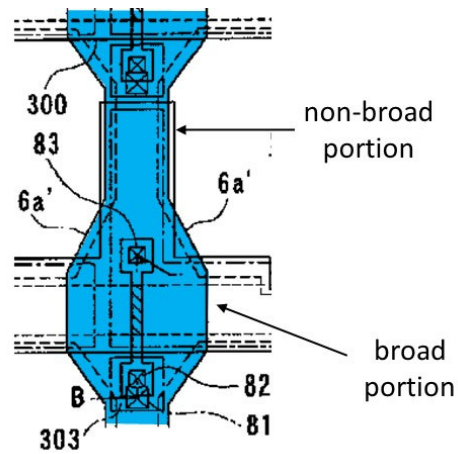


Kurashina, Fig. 3 (annotated)

126. Notably, *Kurashina* teaches to provide a broad portion of the data line for much the same reason as the later '079 patent—i.e., to protect the TFT channel against light leakage. According to *Kurashina*, the broad portions “block light advancing from the liquid-crystal layer 50 side (the direction perpendicular to the paper plane) of the TFT array substrate 10 in each pixel portion.” *Kurashina*, ¶[0055]. As a result of this design, the broad portion of *Kurashina*’s **data line** “overlaps the **thin-film transistor**” (30), such that the data line blocks light (**red arrows**, added below to Figure 4) from reaching the TFT and channel area.



Kurashina, Fig. 4



Kurashina, Fig. 3

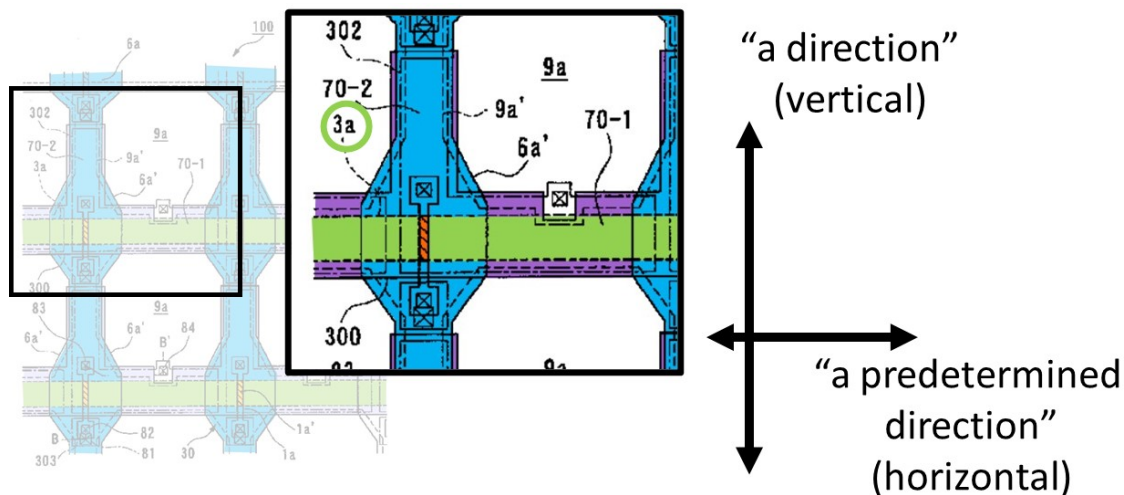
127. The portion of *Kurashina*'s data line that is *not* wide/broad and does *not* overlap the transistor is a “non-broad portion that does not overlap the thin-film transistor,” as illustrated in Figure 3 (above at right). The broad portion of *Kurashina*'s **data line** (6a') is wider than the non-broad portion and, thus, meets the claim requirement of a “broad-width portion” under the plain and ordinary meaning and as that term is purportedly defined in the '079 patent specification. *See* Section VII above. Accordingly, *Kurashina* provides every feature of element 2[c].

2[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;

128. The *Kurashina* reference does not specifically discuss the width(s) of its scanning line; however, the component appears to be depicted as having a

uniform width—i.e., without a “broad-width portion.” See *Kurashina*, Fig. 3. Nonetheless, in my opinion, it would have been obvious over *Kurashina* in view of *Sato* to provide 2[d].

129. In *Kurashina*, the “**data lines** 6a and the **scan lines** 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a.” *Kurashina*, ¶[0054]. More specifically, as illustrated below, the scanning line extends horizontally—i.e., “in the predetermined direction”—and intersects the (vertical) **data line** and the **channel area of the thin film transistor**, as claimed.



Kurashina, Fig. 3 (annotated)

130. In the figure above, the **scan line** of *Kurashina* appears to be depicted as having a uniform width, and *Kurashina* does not describe providing the scan line

with a broad-width portion. Nonetheless, it is my opinion that providing the scan line with a relatively broad-width portion in a portion facing the channel area of the TFT—a feature well known in the art at the time—would have been obvious in view of *Sato*.

131. Preliminarily, I note that a scanning line with a “broad-width portion” was exceedingly well-known, as evidenced by the examiner identifying no fewer than *four references* teaching the feature during prosecution of the ’079 patent and its priority parent. *See* Section VI.B above (discussing the examiner’s application of *Onisawa*, *Ono*, *Murade-721*, and *Uno*). The applicant never disputed the examiner’s identification of the feature in the prior-art, instead relying on other features to secure allowance. *Id.* The *Sato* reference represents yet another prior-art publication that demonstrates the well-known feature.

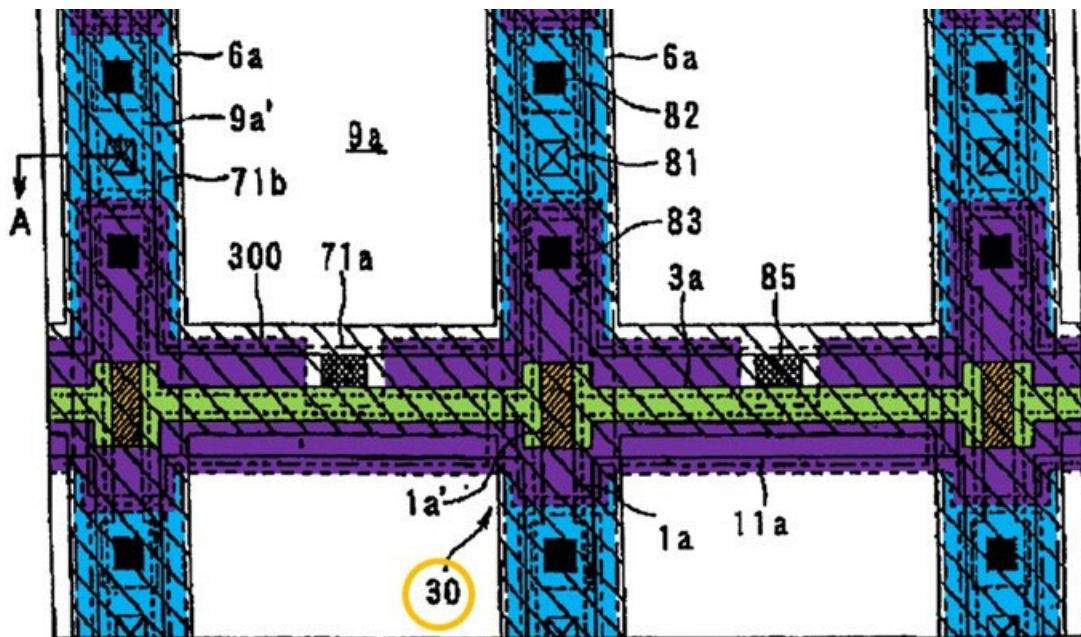
132. *Sato* “relates to the technical field of an electro-optical device of an active matrix drive system, and more particularly, . . . a type having pixel switching thin film transistors.” *Sato*, ¶[0002]. Thus, *Sato* belongs to the same technical field and is analogous art to both *Kurashina* and the ’079 patent. *Compare with Kurashina*, ¶[0002] (discussing related art of “active matrix electro-optical devices using TFTs”) and ’079 patent, 1:12-13 (“invention relates to an electro-optical device capable of performing active matrix drive”). Moreover, both *Kurashina* and

Sato appear to be assigned to the same entity—Seiko Epson—which would motivate POSITA to consider the references together and bolster the POSITA’s conclusion that the references offer compatible teachings.

133. *Sato* also—like *Kurashina*—identifies the need for improved light-shielding “since electro-optical devices are miniaturized and the pixel pitches thereof are greatly narrowed to cope with a recent requirement for enhancing the quality of a displayed image.” *Sato*, ¶[0007]. Further, both *Sato* and *Kurashina* reflect the art’s reluctance to unduly restrict the size of the pixel aperture, which would provide a POSITA with an indication that the design goals of both references are compatible. See *Sato*, ¶¶[0008]-[0009] (purporting to address problem that light shielding makes it “fundamentally difficult to increase the opening ratio of each pixel”); *Kurashina*, ¶¶[0019]-[0020] (selective widening “in the vicinity of the transistor . . . to shield a corner portion of the pixel electrode” makes it “possible to block light” while making the pixel opening only “somewhat narrower”).

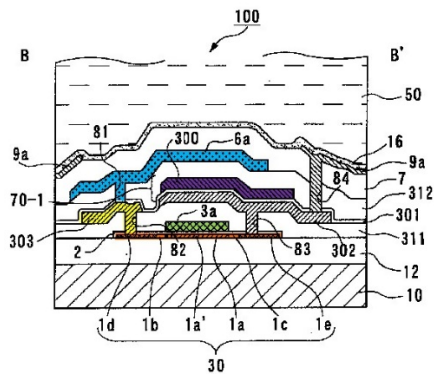
134. *Sato*’s design includes the same general structures as *Kurashina*, including a **data line** (6a) and **scanning line** (3a) intersecting to form the channel of a **TFT** (30, including **channel region** 1a’), as well as a **capacitor line** 300, as illustrated below. *Sato*, ¶¶[0090]-[0091] (“pixel switching TFTs 30, each of which has a scanning line 3a as a gate electrode in each channel region a’ . . . disposed at

the positions where the scanning lines 3a intersect the data lines 6a”), [0094] (“capacitance line 300 extends along each scanning line 3a in a striped shape, and the portion thereof overlapping a TFT 30 projects upward and downward [vertically] in FIG. 2”). Similarly to *Kurashina*, *Sparato*’s **capacitor line** 300 has portions protruding along the **data line** in a manner similar to *Kurashina. Sato*, ¶[0094].

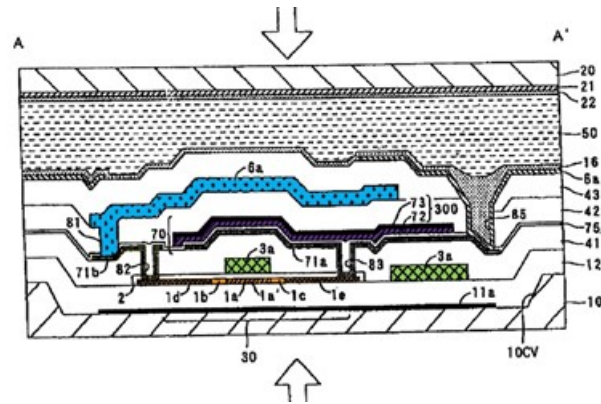


Sato, Fig. 2 (annotated)

135. In addition, *Sato* arranges its **data line** (6a), **scanning line** (3a), **TFT** (30), and **capacitor line** (300) in a manner similar to *Kurashina*, as illustrated below.



Kurashina, Fig. 4 (annotated)



Sato, Fig. 3 (annotated)

136. *Sato* teaches that “the **scanning lines** 3a are widened at portions where they act as the gate electrodes.” *Sato*, ¶[0091]. Thus, similarly to the prior-art references applied during prosecution of the '079 patent and its parent application, *Sato* reflects the art’s understanding that a scanning line must have a certain minimum dimension at the gate area, even if other portions of the scanning line are narrowed to improve pixel pitch and aperture ratio. The **scanning line** of *Sato* thus has a “broad-width portion in a portion facing the channel area of the thin-film transistor,” while the remainder of the scanning line is “a narrow width portion in another portion,” as claimed.

137. *Kurashina* and *Sato* are each analogous art to the '079 patent, at least because each “is from the same field of endeavor,” namely active-matrix drive electro-optical devices such as for LCD displays. *Compare Kurashina*, ¶[0054] (“plurality of transparent pixel electrodes 9a . . . provided in a matrix shape in a pixel

portion on the TFT array substrate”) *with Sato*, ¶[0004] (“pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed in each of a plurality of pixels that are formed in a matrix”) *and* ’079 patent, Abstract (“electro-optical device of the present invention includes pixel electrodes, TFTs . . . and scanning lines and data lines connected to the TFTs”).

138. In addition, *Kurashina* and *Sato* both address problems of light leakage that might otherwise negatively impact TFT channel performance. *Compare Kurashina*, ¶¶[0052] (portions of data line “formed with a wide width in the vicinities of the TFTs 30 . . . and made to serve as light-shielding layers against the incidence of light from the corner portions of the pixel electrodes 9a”) and [0054] (data lines “block light” from reaching TFT) *with Sato*, ¶[0116] (“As a result” of using the data line and capacitance line to block light, “the characteristics of the TFT 30 are hardly deteriorated by light leakage, and a very high light resistant property can be obtained”). In this respect, again, both references address the same problem(s) as the ’079 patent, albeit much earlier. *See* ’079 patent, 23:29-30 (“thus the light leak current can be reduced or minimized”). As is evident from *Kurashina* and *Sato*, it was well-known at the relevant time that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel. A POSITA

would thus consider references such as *Sato* to be pertinent when implementing an active-matrix drive system such as *Kurashina*.

139. In my opinion, it would have been obvious and straightforward to a POSITA at the relevant time (before December 2002) to implement *Kurashina*'s design with the narrow scanning line having a widened gate portion as taught by *Sato*. Indeed, *Sato* specifically teaches that its device "is very advantageous by simply arranging the electro-optical device, and simplifies a manufacturing process thereof." *Sato*, ¶¶[0026], [0028]. Moreover, in my opinion, the art understood that "simply changing the patterning shape when the capacitor lines and the data lines are formed"—as would be required to implement *Sato* with *Kurashina*—would be a relatively straightforward modification, and "has the advantage of making formation possible even without providing any special process." *Kurashina*, ¶[0022]. A POSITA would recognize that the benefits of *Sato*'s narrow scanning line with a wide gate portion would be additive to the design of *Kurashina*, because the combination would result in a higher-density pixel configuration with larger pixel apertures, which would improve image quality. Further, in my opinion, combining *Kurashina* with *Sato* would yield a "scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the

channel area of the thin-film transistor and a narrow width portion in another portion,” just as the claim requires.

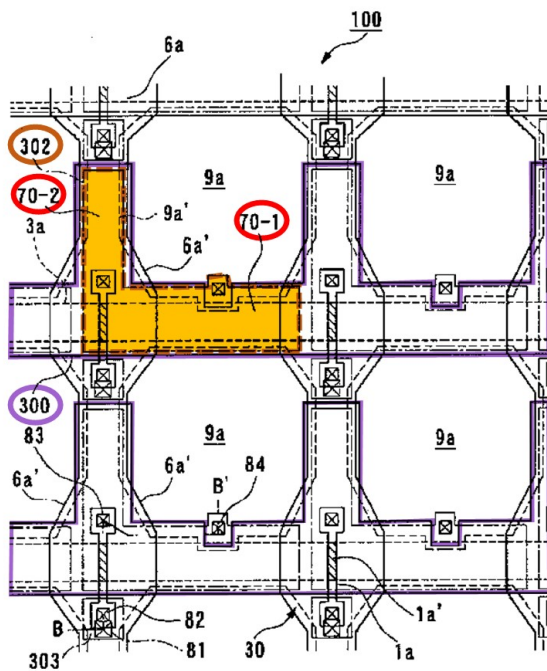
140. It is also my opinion that combining the teachings of *Kurashina* and *Sato* would have required no more than ordinary skill because the combination would have been a simple modification of the scanning line, which is an already-existing component, in a straightforward manner to achieve predictable results. For the reasons discussed above, the combination of references would have had a reasonable expectation of success given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Sato* could be integrated into *Kurashina*’s device. In other words, modifying *Kurashina*’s scanning line according to *Sato*’s teachings would be a straightforward and predictable improvement to *Kurashina*’s device.

141. Thus, in my opinion, *Kurashina* and *Sato* render obvious claim element 2[d].

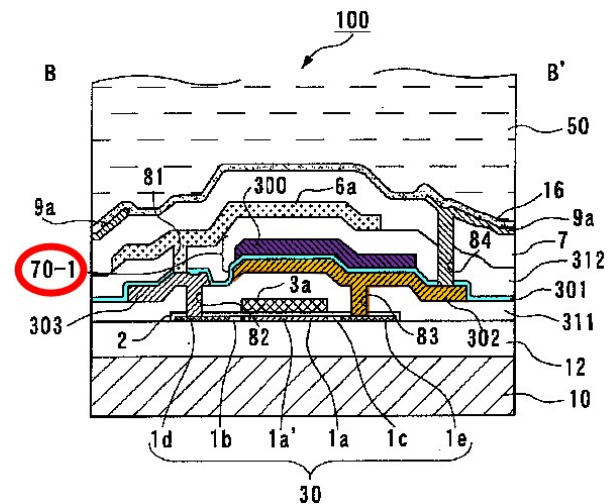
2[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and

142. *Kurashina* discloses 2[e]. *Kurashina* discloses “**storage capacitors**” (70-1 and 70-2) that ensure capacitance and “stabilize the display

screen,” which it illustrates in Figures 3 (below, left) and 4 (below, right).
Kurashina, ¶[0059]. According to *Kurashina*, “the **capacitor lines 300**, together with the L-shaped **drain electrode 302** [illustrated in plan view below at left],” together with “interposed **insulating films**” (301) “form **storage capacitors 70-1**.”
Kurashina, ¶[0058].



Kurashina, Fig. 3 (annotated)



Kurashina, Fig. 4 (annotated)

143. As a fundamental matter of electronics, well understood by a POSITA, a storage capacitor is a device used to store an electrical charge, and consists of two conductors separated by an insulator or dielectric material. Ex. 1025 [Nilsson] at 4 (book page 174); Ex. 1029 [Kaplan Dictionary] at 3 (book page 92 (“capacitor”).

As in the example of *Kurashina*, the **capacitor line** 300 and the **drain electrode** 302 act as conductors, and the **insulating film** 301 serves as the dielectric insulating layer between the conductors, such that a fixed voltage potential difference is created between them.

144. In *Kurashina*, the **drain electrode** 302 represents the potential of the pixel because the pixel 9a connects to **drain electrode** 302 via contact hole 84, as illustrated in Figure 4 (above, right). *Kurashina*, ¶[0032] (describing FIG. 2), ¶[0060] (“FIG. 3 . . . structure is exactly the same” as in FIG. 2).³ In other words, the **drain electrode** 302 forms the first electrode of the storage capacitor and is a “pixel-potential capacitor electrode,” as required by the claim.

145. Further, to create a storage capacitor (as *Kurashina* discloses), a fixed voltage potential is supplied by the **capacitor line** 300, meaning that the **capacitor line** 300 forms a “fixed-potential capacitor electrode.” *Kurashina*, ¶[0034]. Given a background knowledge of capacitors, a POSITA would generally understand a **capacitor line** to have a fixed potential, given its connection to a constant potential

³ These principles are also explained, for example, in *Sato*, which teaches that “pixel potential side capacitance electrode” is formed by connection between “heavily doped drain region 1e of the TFT 30 (and the pixel electrode 9a).” *Sato*, ¶[0093].

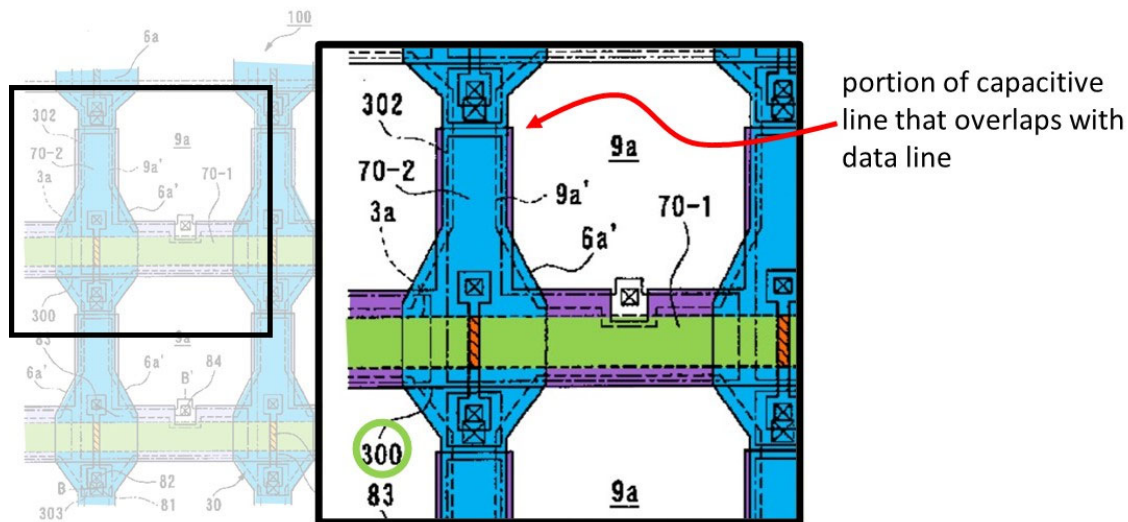
source. *See, e.g., Sato*, ¶[0093] (“part of the capacitance line 300 . . . acts as the fixed potential side capacitance electrode”) and *Takahara*, ¶[0063] (“capacitor line 300 . . . is electrically connected to a constant-potential source, and has a fixed potential”; “constant potential source may be . . . a positive power supply or a negative power supply supplied to a scan-line drive circuit”). Indeed, a later embodiment of *Kurashina* confirms and illustrates the role of the capacitor line as a fixed-potential capacitor electrode, where by example “capacitor electrode 403b having a fixed potential is provided overlapping the scan line 3a, and one end of the capacitor electrode 403b is connected to the capacitor line 404a.” *Kurashina* ¶[0067]. In the above embodiment, the capacitance electrode 403b at a fixed potential is in electrical contact with the capacitance line, and as such, the capacitance line itself is at a fixed potential.

146. Finally, because the **insulating film** 301 is an insulating layer that separates the two electrodes of the capacitor in *Kurashina*, allowing an electric field to build up between the two electrodes rather than allowing a current to pass between them, the insulating film is a “dielectric film.” Ex. 1020 [Dorf] at 3 (book page 15) (“When electrical current flows into a capacitor, a force is established between two parallel plates separated by a dielectric.”); Ex. 1029 [Kaplan Dictionary] at 3-4 (book pages 92 (“capacitor”) and 184 (“dielectric”)); Ex. 1030 [Laplante Dictionary]

at 3 (“dielectric”); *see also Sato*, ¶[0093] (capacitor electrodes “are disposed in confrontation with each other through the dielectric film”). Thus, in my opinion, *Kurashina* provides 2[e].

2[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.

147. *Kurashina* discloses 2[f]. *Kurashina* discloses that “**capacitor lines** 300 overlap the **scan lines** 3a and are provided in the left-right direction in the paper plane along the boundaries of the pixel electrodes 9a.” *Kurashina*, ¶[0057]. Further, the **capacitor lines** 300 have both (i) “substantially linearly extending portions overlapping the **scan lines** 3a” and (ii) “substantially linearly extending portions overlapping the **data lines** 6a.” *Id.*, ¶[0058].



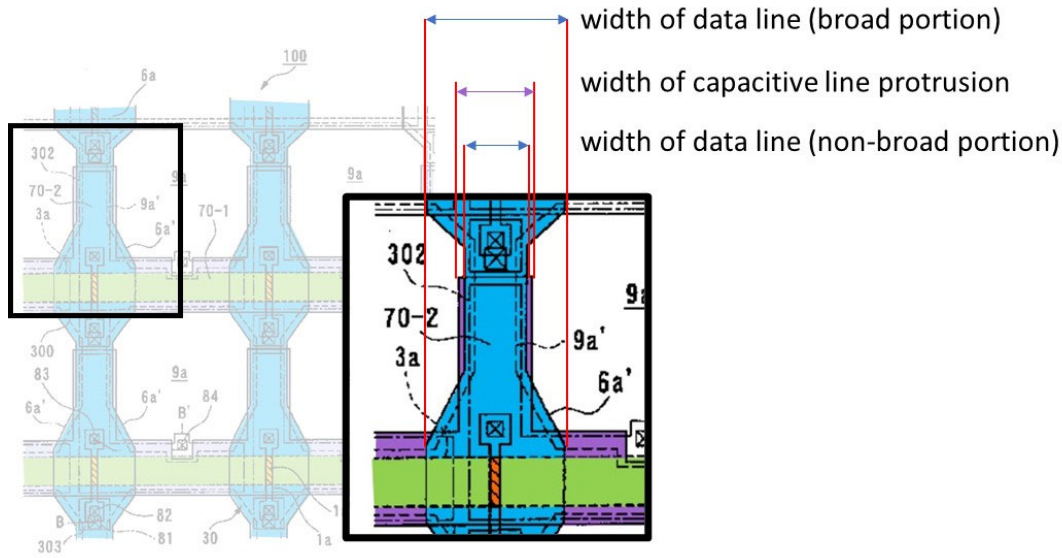
Kurashina, Fig. 3 (annotated)

148. *Kurashina* refers to the horizontal portion of the **capacitor line 300** as the “main line portions, which extend substantially linearly along the **scan line 3a**” and the vertical portions of the **capacitor line 300** as the “**protruding portions**, which protrude in the up-down direction in the paper plane along the **data lines 6a**.” *Kurashina*, ¶[0033]. Although the foregoing text refers specifically to Figure 1, the description applies equally to the analogous components appearing in related Figure 3, as *Kurashina* explains. *Kurashina*, ¶[0053] (“component members having the same functions as in FIG. 1 and FIG. 2 are indicated by the same symbols in FIG. 3 and FIG. 4”).

149. As I discuss above in connection with 2[e], the capacitive line has a portion that “serves as the fixed-potential capacitor electrode of the storage capacitor,” as claimed.

150. The horizontal or “main line portion” of *Kurashina*’s capacitive line is a “portion extending along the scanning line,” i.e., because the scanning line runs in the same direction.

151. The vertical or “protruding portion” of *Kurashina*’s capacitive line is a “portion extending along the data line,” i.e., because the data line runs in the same direction. Moreover, as I illustrate below with annotations added to Figure 3, *Kurashina*’s protruding portion has “a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.” While *Kurashina* may not provide specific dimensions for its components, the reference clearly shows a POSITA that the capacitive line projection is wider than a non-broad portion of the data line.



Kurashina, Fig. 3 (annotated)

152. A POSITA considering implementing a design such as *Kurashina* would understand illustrated relative widths to convey general design information and demonstrate one acceptable design choice. Indeed, I note that *Kurashina* differentiates various embodiments specifically based on the relative widths of components. *Kurashina*, ¶[0052]. For example, in *Kurashina*, “[t]he present second embodiment [Figure 3] differs from the previous first embodiment [Figure 1] in that, instead of forming the capacitor lines 300 with a wide width, the data lines 6a running up and down in the paper plane are formed with a wide width in the vicinities of the TFTs 30, as shown in FIG. 3, and made to serve as light-shielding layers against the incidence of light from the corner portions of the pixel electrodes 9a.” *Id.* From such disclosure, a POSITA would understand (i) *Kurashina*’s figures are

intended to communicate different relative widths (as they specifically illustrate) and (ii) *Kurashina*'s Figure 3 has a data line that is selectively wider than the capacitive line at the TFT portions near the corners of the pixel electrodes *and not at other portions*. Thus, a POSITA would recognize that *Kurashina* teaches 2[f].

153. Accordingly, it is my opinion that *Kurashina* (in view of *Sato* with respect to element 2[d]) provide every limitation of independent claim 2 and, together, render obvious claim 2.

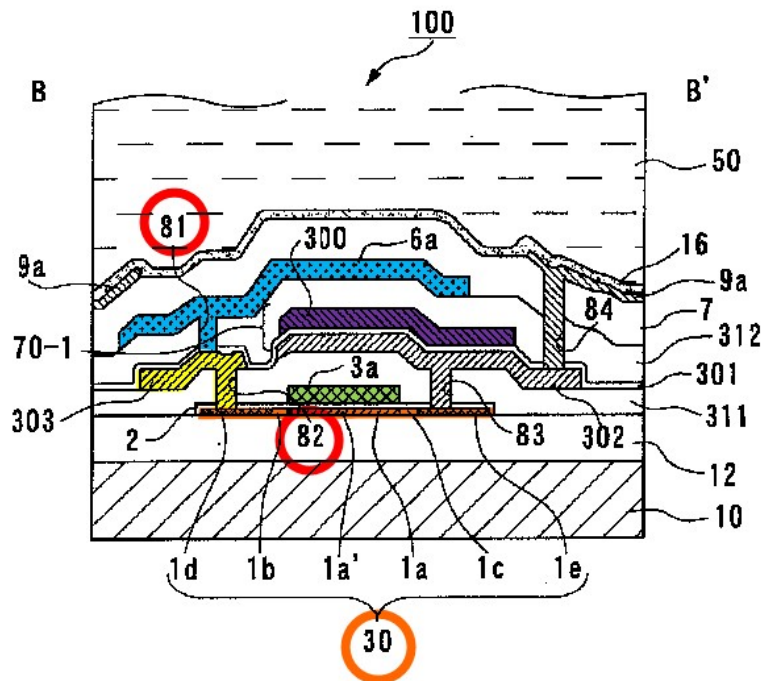
B. Claim 3

3: The electro-optical device according to claim 2, further comprising a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.

154. Claim 3 depends from claim 2 and, thus, incorporates every limitation of claim 2. The combination of *Kurashina* and *Sato* provide those limitations as set forth in the section above. In addition, as explained below, it is my opinion that *Kurashina* discloses the additional limitation of claim 3.⁴

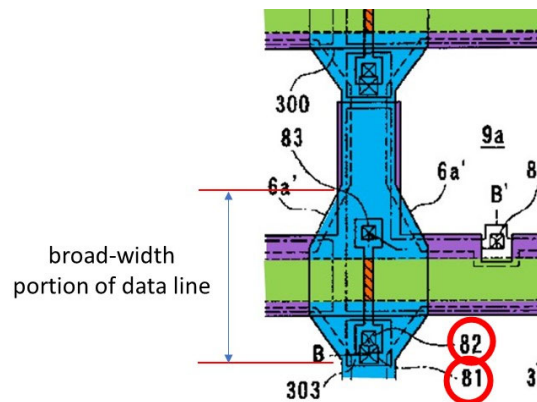
⁴ I have been instructed to assume that claim 3 includes an obvious typographical error, and the claim should be understood as if the word "to" were included between "transistor" and "a portion."

155. According to *Kurashina*, “[t]he **data lines** 6a are electrically connected to the **source electrodes** 303 . . . via the **contact holes** 81.” *Kurashina*, ¶[0055], Fig. 4 (below). Other **contact holes** (82) “electrically connect the **source electrodes** 303 and the high-density source regions 1d of the semiconductor layers 1a” of the **TFT**. *Id.*, ¶[0056]. Thus, because the data line material extends through contact hole 81 to the source electrode, and because the source electrode material extends through contact hole 82 to the TFT, the data line electrically connects to the TFT through contact holes 81 and 82. In other words, *Kurashina* provides the claimed “contact hole that electrically connects the thin-film transistor and the data line.”



Kurashina, Fig. 4 (annotated)

156. *Kurashina* also discloses “the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located,” as claimed. The plan-view illustration of *Kurashina* (Figure 3, below) shows the **data line** 6a being broad—i.e., “broader than the width of the ‘narrow width portion’”—throughout its entire extent from each/either of the **contact holes** (81,82) through the **TFT** (30). In other words, the broad portion is “continuously broad,” as a POSITA would understand that term.



Kurashina, Fig. 3 (annotated)

157. Thus, in my opinion, *Kurashina* in view of *Sato* provides every limitation of claim 3 and, together, renders obvious claim 3, because *Kurashina* provides “a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.”

C. Independent Claim 1

1[pre] An electro-optical device, comprising:

158. *Kurashina* discloses the preamble of claim 1. As I explain above in 2[pre] (§120), *Kurashina* provides an “electro-optical device, comprising.” Because the preamble of claim 1 is identical to claim 2, *Kurashina* provides the preamble of claim 1 for the same reasons.

1[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

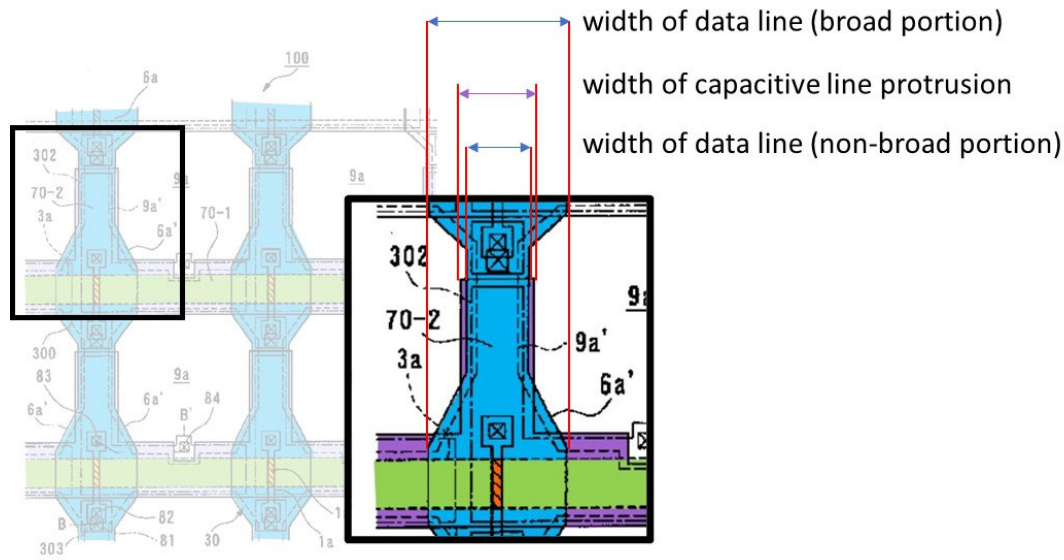
159. *Kurashina* discloses 1[a]. As I explain above in 2[a] (§§121-123), *Kurashina* provides “a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction.” Because 1[a] is identical to 2[a], *Kurashina* provides 1[a] for the same reasons.

1[b] a pixel electrode formed correspondingly to the thin-film transistor;

160. *Kurashina* discloses 1[b]. As I explain above in 2[b] (§124), *Kurashina* provides “a pixel electrode formed correspondingly to the thin-film transistor.” Because 1[b] is identical to 2[b], *Kurashina* provides 1[b] for the same reasons.

1[c] a data line extending in the direction in which the channel area extends, the data line having a broad-width portion that overlaps the channel area in plan view;

161. *Kurashina* discloses 1[c]. As I explain above in 2[c] (§§125-127), *Kurashina* provides “a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor” Limitation 1[c] recites substantially identical structure; therefore, *Kurashina* provides 2[c] for the same reasons. I further note 1[c] specifies that the broad-width portion overlaps the channel area “in plan view,” and the overlap discussed above in §§125-127 (and illustrated in *Kurashina* Figure 3, below) is “in plan view.” See *Kurashina*, ¶[0055] (“data lines 6a extend linearly but have wide-width portions 6a' protruding in the direction of the scan lines 3a (i.e., the left-right direction in the paper plane as seen in plan view) at portions intersecting the scan lines 3a (underlining added)).

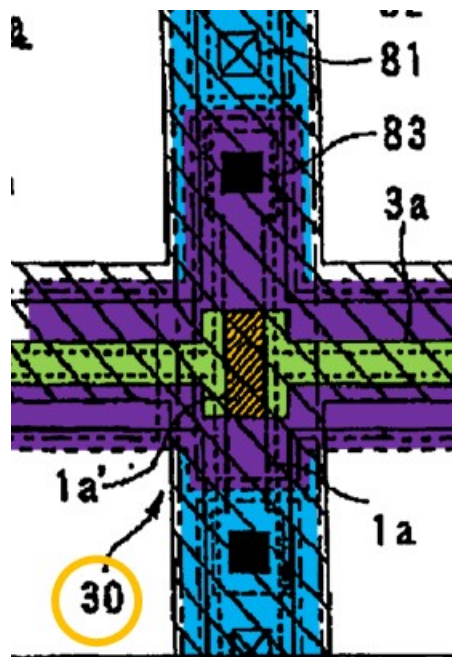


Kurashina, Fig. 3 (annotated)

1[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion;

162. It is my opinion that 1[d] would have been obvious over *Kurashina* in view of *Sato* for the same reasons as 2[d], which I explain above in paragraphs 128-141. Specifically, as I explain above in paragraphs 128-141, the combination of *Kurashina* and *Sato* provides “a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another

portion.” As compared to 2[d], element 1[d] recites that (i) the scanning line has a broad-width portion in a portion “overlapping” (instead of “facing”) the channel area and (ii) the overlap is “in plan view.” Those differences in verbiage, however, make no meaningful difference with respect to the design of *Kurashina* and *Sato*, because as illustrated in Figures 3 and 4 of *Sato* (discussed in ¶¶134-135 above and reproduced below) (i) the broad-width portion of the scanning line is *both* “facing” and “overlapping” the TFT channel and (ii) Figures 3 and 4 show the overlap “in plan view.”



Sato, Fig. 2

163. Accordingly, it is my opinion that *Kurashina* and *Sato* render obvious claim element 1[d].

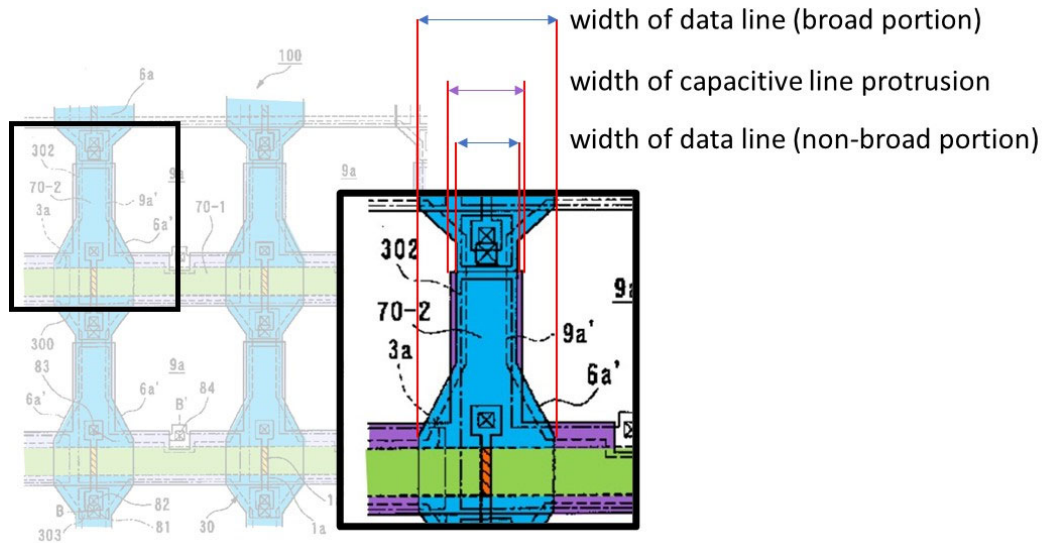
1[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed-potential capacitor electrode;

164. *Kurashina* discloses 1[e]. As I explain above in 2[e] (§§142-146), *Kurashina* provides “a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode.” Because 1[e] is identical to 2[e], *Kurashina* provides 1[e] for the same reasons.

1[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and

165. *Kurashina* discloses 1[f]. As I explain above in 2[f] (§§147-152), *Kurashina* provides “a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width . . . that is wider than the non-broad portion of the data line.” As I discuss in connection with 2[f] and as I illustrate below, the portion of *Kurashina*’s **capacitor line** that extends along the

data line is broader than the non-broad portion of the data line (meaning it is broader than “a width of the data line” as claimed).



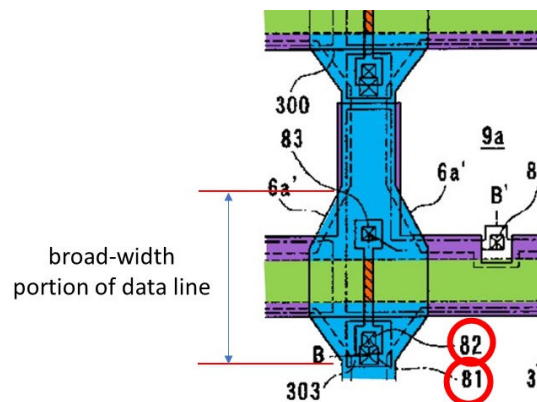
Kurashina, Fig. 3 (annotated)

1[g] a contact hole electrically connecting the data line and the thin film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.

166. *Kurashina* discloses 1[g]. As I explain above in connection with Claim 3 (§§ 154-157), *Kurashina* provides “a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.” Substantively, 1[g] is broader in that it omits the “continuously broad” limitation. As such, the contact hole of 1[g] need only be

positioned “at a portion of the broad-width portion of the data line,” which “extends beyond the channel area in a direction extending from the channel area toward the contact hole.”

167. *Kurashina* discloses this limitation for the same reasons as it discloses Claim 3. As I illustrate below, a portion of the broad width portion of the **data line 6a'** extends beyond the **channel area** in a direction (vertically down) extending from the channel area toward the contact hole. Each **contact hole** (81, 82) is positioned at the foregoing “portion of the broad-width portion of the **data line**,” and thus either contact hole will meet the claim limitation.



Kurashina, Fig. 3 (annotated)

168. In summary, for the reasons set forth above, it is my opinion that *Kurashina* in view of *Sato* provides every limitation of independent claim 1 and, together, the combination renders obvious claim 1.

X. GROUND 2: KURASHINA IN COMBINATION WITH TAKAHARA RENDERS

OBVIOUS CLAIMS 1-3

A. Independent Claim 2

169. As I discuss above in Ground 1, it is my opinion that *Kurashina* discloses every limitation of claim 2, with the possible exception of “the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion,” which is identified herein as element “2[d].” See ¶¶128-141. As set forth above, it is my opinion that *Sato* provides the feature. *Id.* It is also my opinion that *Takahara* (Ex. 1010) provides 2[d] and, as detailed below, a POSITA would have found each of claims 1-3 to be obvious over the combination of *Kurashina* with *Takahara*.

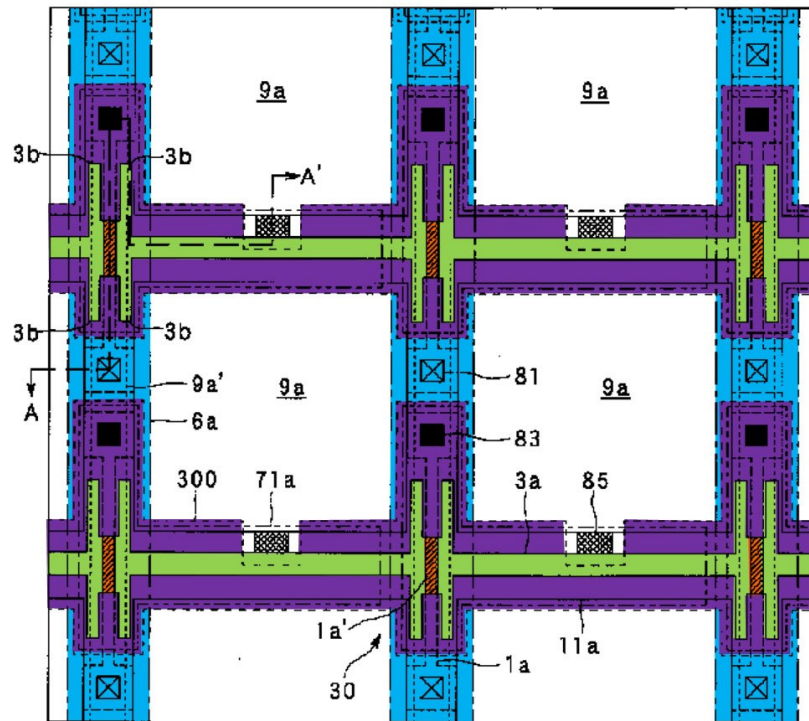
170. Like *Kurashina* and the '079 patent, *Takahara* “pertains to the technical field of active-matrix-drive-type electro-optical devices, and more particularly pertains to a form in which a pixel-switching, thin-film transistor . . . is provided.” *Takahara*, ¶[0001]. Thus, *Takahara* belongs to the same technical field and is analogous art to both *Kurashina* and the '079 patent. *Compare with Kurashina*, ¶[0002] (discussing related art of “active matrix electro-optical devices using TFTs”) and '079 patent, 1:12-13 (“invention relates to an electro-optical device capable of performing active matrix drive”). Moreover, both *Kurashina* and *Takahara* appear to be assigned to the same entity—Seiko Epson—which would motivate POSITA to

consider the references together and bolster the POSITA's conclusion that the references offer compatible teachings.

171. *Takahara* also—like *Kurashina*—addresses the art-recognized need to shield the TFT channel area from incident light, a need that became particularly acute “as higher definition or finer pixel pitch is achieved in electro-optical devices to meet the general demand for higher quality of display images particularly in recent years.” *Takahara*, ¶[0006]. Further, both *Takahara* and *Kurashina* reflect the art's reluctance to unduly restrict the size of the pixel aperture, which would provide a POSITA with an indication that the design goals of both references are compatible. *See Takahara*, ¶¶[0007]-[0008] (cautioning that designs relying on “widened” light-shielding films make it “difficult to increase the aperture percentage of the pixels” and “increase ... internally reflected light and multiply reflected light”); *Kurashina*, ¶¶[0019]-[0020] (selective widening “in the vicinity of the transistor . . . to shield a corner portion of the pixel electrode” makes it “possible to block light” while making the pixel opening only “somewhat narrower”).

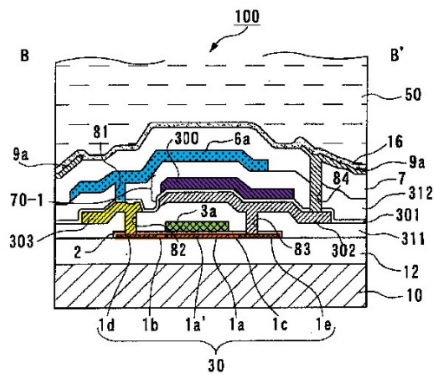
172. *Takahara*'s design includes the same general structures as *Kurashina*, including a “pixel switching TFT 30, in which the scan line 3a is disposed opposing the gate electrode in the channel region 1a', is provided at each location where the scan line 3a and the data line 6a intersect.” *Takahara*, ¶[0054]. *Takahara* further

provides a **capacitor line** 300 with portions protruding along the **data line** in a manner similar to *Kurashina*. *Takahara*, ¶[0058].

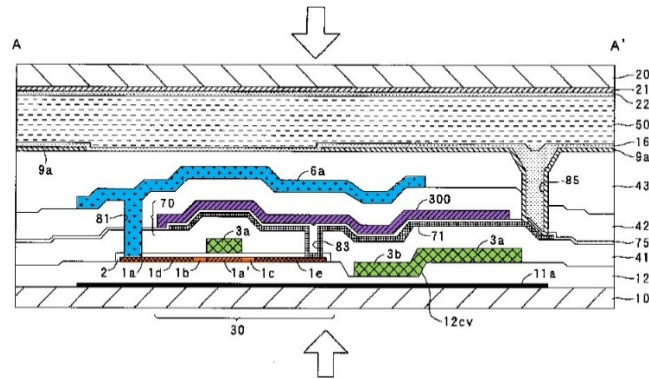


Takahara, Fig. 2 (annotated)

173. In addition, *Takahara* arranges its **data line**, **scanning line**, **TFT**, and **capacitor line** in a manner similar to *Kurashina*, as illustrated below. As illustrated, *Kurashina* differs mainly in its addition of an intervening **source electrode** (303) between the **data line** and **TFT**. In my opinion, however, a POSITA would not consider that difference to be an obstacle in the way of combining the teachings of the two references.



Kurashina, Fig. 4 (annotated)

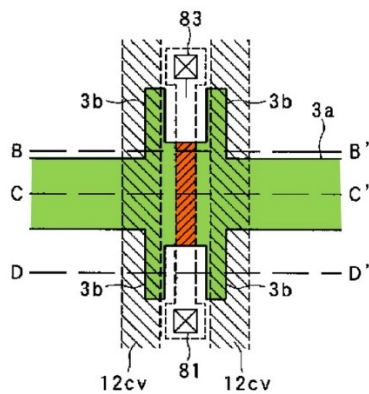


Takahara, Fig. 3 (annotated)

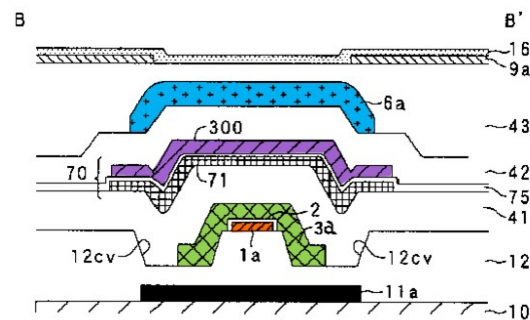
174. *Takahara* teaches that “the **scan line 3a** is formed with a wide width at the location at which it becomes the gate electrode.” *Takahara*, ¶[0053]. Thus, similarly to the prior-art references applied during prosecution of the '079 patent and its parent application, *Takahara* reflects the art’s understanding that a scanning line must have a certain minimum dimension at the gate area, even if other portions of the scanning line are narrowed to improve pixel pitch and aperture ratio. The **scan line** of *Takahara* scanning line thus has a “broad-width portion in a portion facing the channel area of the thin-film transistor,” while the remainder of the scanning line is “a narrow width portion in another portion,” as claimed.

175. In addition, *Takahara*’s scan line has “**protruding portions 3b** , which protrude . . . extending along the data line 6a viewed in plan view,” as illustrated in more detail below (at left) in Figure 4. *Takahara*, ¶[0053]. *Takahara*’s **protruding portions 3b** are provided as an additional way to prevent light leakage from reaching

the TFT. *Takahara*, ¶[0077]. The reference provides further description of the protruding portion in Figure 5 (below at right), which illustrates a cross-section B-B' of the **protruding portion** 3b. *Id.* Because the **protruding portion** of *Takahara*'s scanning line is broader than another portion of the scanning line, and the **protruding portion** is “in a portion facing the channel area of the thin-film transistor,” and the claim limitation is met for this additional reason.



Takahara, Fig. 4 (annotated)



Takahara, Fig. 5 (annotated)

176. *Takahara* teaches several benefits of implementing its **protruding portions** 3b, as the structure protects the **TFT channel** (1a') against “impingement of the incident light advancing obliquely toward the substrate surface of the TFT.” *Takahara*, ¶[0079]. According to *Takahara*, “even if various light-shielding films are provided above and below the **TFT** 30”—e.g., like the overlapping data line layer of *Kurashina*—“oblique light that advances through gaps between them can be

present.” *Id.*, ¶[0082]. Based on those disclosures, a POSITA would understand *Takahara*’s scan line **protruding portions** to achieve desirable improvements in performance. For example, according to *Takahara*, “even under severe conditions such as . . . strong incident light or returning light, [the TFT] can satisfactorily perform switching control of the pixel electrode 9a, and ultimately a bright, high-contrast image can be displayed.” *Takahara*, ¶[0083].

177. *Kurashina* and *Takahara* are each analogous art to the ’079 patent, at least because each “is from the same field of endeavor,” namely active-matrix drive electro-optical devices such as for LCD displays. *Compare Kurashina*, ¶[0054] (“plurality of transparent pixel electrodes 9a . . . provided in a matrix shape in a pixel portion on the TFT array substrate”) with *Takahara*, ¶[0051] (“pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed in each of a plurality of pixels that are formed in a matrix”) and ’079 patent, Abstract (“electro-optical device of the present invention includes pixel electrodes, TFTs . . . and scanning lines and data lines connected to the TFTs”).

178. In addition, *Kurashina* and *Takahara* both address problems of light leakage that might otherwise negatively impact TFT channel performance. *Compare Kurashina*, ¶¶[0052] (portions of data line “formed with a wide width in the vicinities of the TFTs 30 . . . and made to serve as light-shielding layers against the

incidence of light from the corner portions of the pixel electrodes 9a”) and [0054] (data lines “block light” from reaching TFT) *with Takahara*, ¶[0082] (using “capacitor line 300 and the data line 6a” as “light-shielding films against the incident light entering the electro-optical device from above” and “protruding portions 3b, which shield the sides”). In this respect, both references address the same problem(s) as the ’079 patent, albeit much earlier. *See* ’079 patent, 23:29-30 (“thus the light leak current can be reduced or minimized”). As is evident from *Kurashina* and *Takahara*, it was well-known at the relevant time that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel. Furthermore, *Takahara*’s design is specifically intended to improve systems having a relatively wide light-shielding layer above the TFT that might otherwise “increase. . . internally reflected light and multiply reflected light.” *Takahara*, ¶[0007]. Although *Kurashina* mitigates internal reflection/refraction by only *partially* widening the data layer at the corner areas above the TFT, those widened portions still could benefit from the additional mitigating measures provided by *Takahara*’s scanning line projections (3b). A POSITA would thus consider references such as *Takahara* to be pertinent when implementing an active-matrix drive system such as *Kurashina*.

179. In my opinion, it would have been obvious and straightforward to a POSITA at the relevant time (before December 2002) to implement *Kurashina*'s design with the scanning line protrusions taught by *Takahara*. Indeed, *Takahara* specifically teaches that its protruding portions can easily be implemented and manufactured. *Takahara*, ¶[0084] (“because the protruding portions 3b are formed integrally from the same film as the scan line 3a, no additional step is needed to form [them]”). *Takahara* also is adaptable to various configurations, as it teaches that different protrusion designs can be used “considering the layout of the lines, elements, and the like around the semiconductor layer 1a.” *Takahara*, ¶[0086]. That flexibility would give the POSITA a reasonable expectation of success in implementing the principles of *Takahara* with the design of *Kurashina*. Moreover, in my opinion, the art understood that “simply changing the patterning shape when the capacitor lines and the data lines are formed”—as would be required to implement *Takahara* with *Kurashina*—would be a relatively straightforward modification and “has the advantage of making formation possible even without providing any special process.” *Kurashina*, ¶[0022]. Moreover, a POSITA would recognize that the benefits of *Takahara*'s light-shielding improvements would be additive to the light-shielding mechanisms already present with *Kurashina*, and providing those improvements would be a simple matter of design choice exercising

ordinary skill. Further, in my opinion, combining *Kurashina* with *Takahara* would yield a “scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion,” just as the claim requires.

180. It is also my opinion that combining the teachings of *Kurashina* and *Takahara* would have required no more than ordinary skill because the combination would have been a simple modification of an existing component (scanning line) in a straightforward manner to achieve predictable results. For the reasons discussed above, the combination of references would have had a reasonable expectation of success given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Takahara* could be integrated into *Kurashina*’s device. In other words, modifying *Kurashina*’s scanning line according to *Takahara*’s teachings would be a straightforward and predictable improvement to *Kurashina*’s device.

181. Thus, in my opinion, *Kurashina* and *Takahara* render obvious claim element 2[d]. And because *Kurashina* provides all the remaining limitations of claim 2, as discussed above in Ground 1, it is my opinion that claim 2 would have been obvious over the combination.

B. Claim 3

182. As I discuss above in connection with Ground 1, *Kurashina* discloses the limitations of claim 3. Accordingly, it is my opinion that the combination of *Kurashina* and *Takahara* renders claim 3 obvious.

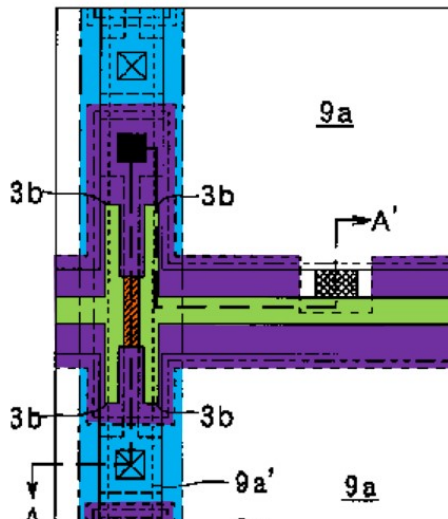
C. Independent Claim 1

183. As I discuss above in Ground 1, it is my opinion that *Kurashina* discloses every limitation of claim 1, with the possible exception of “the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion,” which is identified herein as element “1[d].” See ¶162.

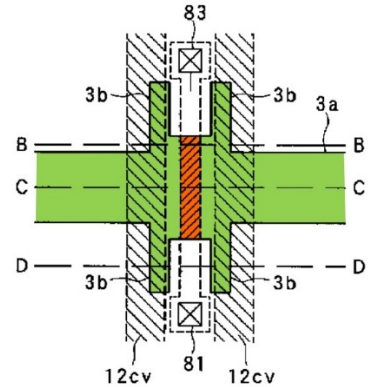
184. It is my opinion that 1[d] would have been obvious over the combination of *Kurashina* and *Takahara* for the same reasons as 2[d], and, as detailed below, a POSITA would have found each of claims 1 to be obvious over the combination.

185. As compared to 2[d], element 1[d] recites that (i) the scanning line has a broad-width portion in a portion “overlapping” (instead of “facing”) the channel area and (ii) the overlap is “in plan view.” Those differences in verbiage, however, make no meaningful difference with respect to the design of *Kurashina* and *Takahara*, because, in my opinion, (i) the broad-width portion of the scanning line

is *both* “facing” and “overlapping” the TFT channel and (ii) Figures 2 and 4 show the overlap “in plan view,” in *Takahara*, as illustrated below.



Takahara, Fig. 2



Takahara, Fig. 4

186. Thus, because the obvious combination of *Kurashina* and *Takahara* provides every limitation of claim 1, it is my opinion that claim 1 would have been obvious to a POSITA.

XI. GROUND 3: MURADE-109 IN COMBINATION WITH MURADE-125 RENDERS OBVIOUS CLAIMS 1-3

187. As detailed below, Murade-109 (Ex. 1011) in combination with Murade-125 (Ex. 1012) provide every feature of claims 1-3 and, in my opinion, a POSITA would have found each claim to be obvious over the combination of references.

188. Listing the same inventor and assignee as the '079 patent but published more than one year *before* the '079 patent was first filed in the United States, *Murade-109* presents an electro-optical device strikingly similar to the design later disclosed in the '079 patent. *Murade-109* depicted each of (i) the scanning line having a “broad-portion,” (ii) the alternately broad and narrow data line, and (iii) the “contact hole” that form the basis for the '079 patent’s claimed design. And although *Murade-109* does not describe a capacitance line projection that is broader than a portion of the data line, that feature was a well-known and obvious design choice. As evidenced, for example, by *Murade-125* (yet another prior-art disclosure from the '079 patent’s inventor) a POSITA would have known and been motivated to provide just such a feature.

A. Independent Claim 2

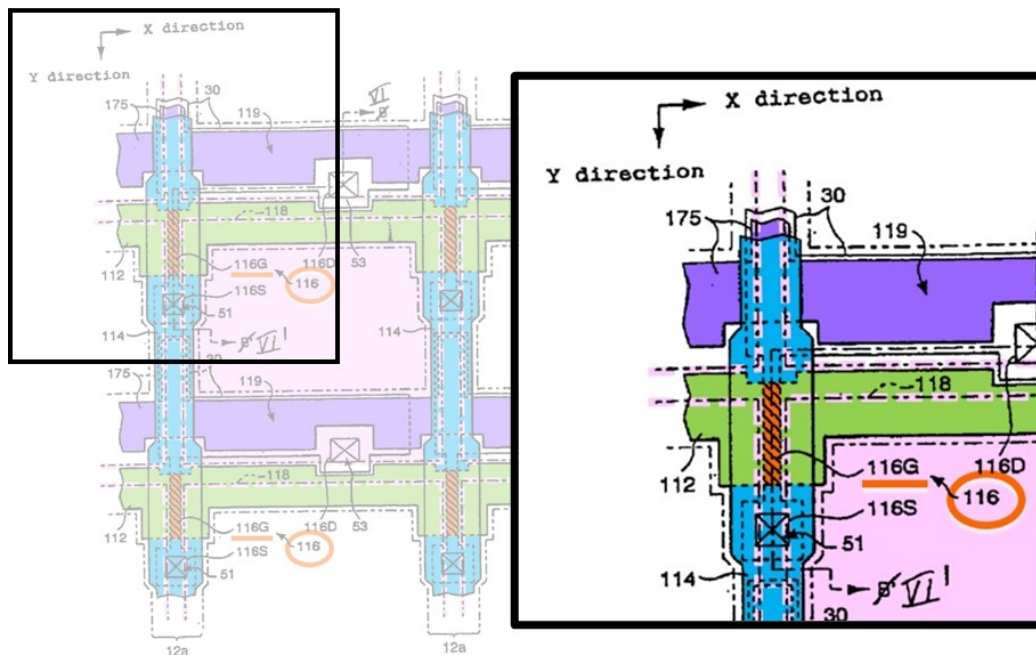
189. In my analysis of the '079 patent claims, I will address independent claim 2 (and its dependent, claim 3) before independent claim 1. Claim 2 is, in some respects, the broader claim because claims 1 and 3 generally include the same or similar elements but add a “contact hole” feature. Thus, it makes logical sense to address claim 2 first.

2[pre] An electro-optical device, comprising:

190. Murade-109 discloses the preamble of claim 2. *Murade-109* discloses an “electro-optical device.” *Murade-109*, Title.

2[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

191. *Murade-109* discloses 2[a]. *Murade-109* discloses the “principal elements” common to a known electro-optical device, “such as the **data line** 114, the **scanning line** 112, the **capacitor line** 175, and the **TFT** 116,” as illustrated below. *Murade-109*, ¶[0135]. *Murade-109*’s TFT includes several regions, including a heavily-doped source region (116S), gate electrode (116G), and heavily-doped drain region (116D). *Murade-109*, ¶[0138]. As *Murade-109* explains, a “portion of the semiconductor layer 30 overlapping the **scanning line** 112 corresponds to a **channel region** 30a.” *Murade-109*, ¶[0138]. “That is,” *Murade-109* continues, “a portion of the scanning line 112 intersecting with the semiconductor layer 30 is used as a **gate electrode** 116G.” *Murade-109*, ¶[0138]. *Murade-109*’s **channel region** 30a (corresponding to the **gate electrode**) is a “channel area” according to the claim.



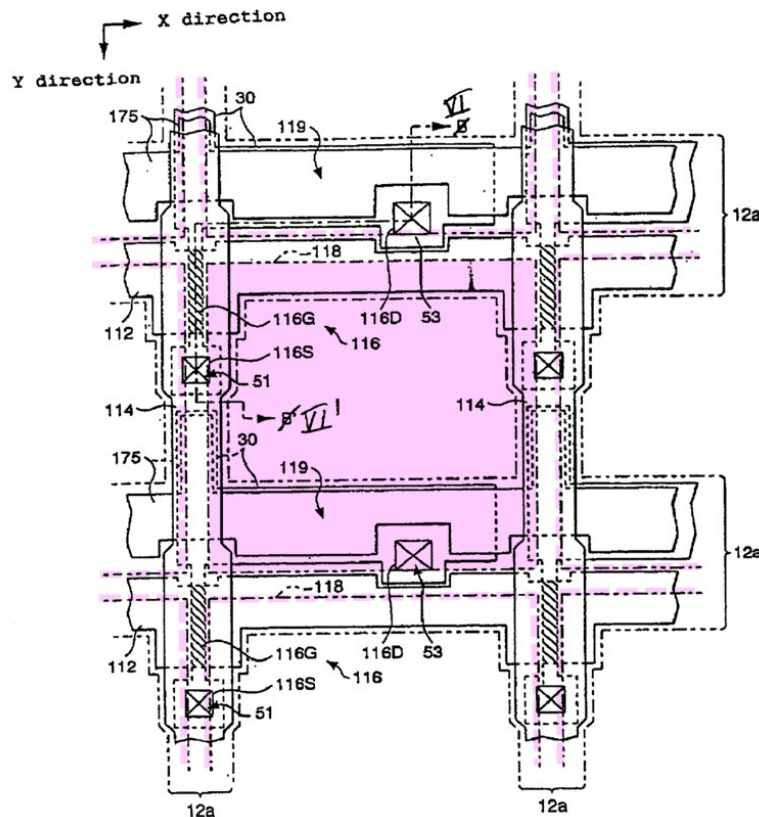
Murade-109, Fig. 5 (annotated)

192. Furthermore, as depicted above, the channel region of the **TFT** (30a, beneath **gate electrode** 116G above) extends in a direction (namely, the “Y direction” depicted on the figure) and intersects a predetermined direction (namely, the “X direction”) that intersects the direction. Thus, the thin-film transistor of *Murade-109* has “a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction,” as required by the claim.

2[b] a pixel electrode formed correspondingly to the thin-film transistor;

193. *Murade-109* discloses 2[b]. In *Murade-109* Figure 5, “the outline of the pixel electrode 118 [is] indicated by a broken line,” as I have highlighted below.

Murade-109, ¶[0134]. In actuality, *Murade-109* depicts several **pixel electrode** in a matrix configuration. In the figure below, the central **pixel electrode** is highlighted with pink highlighting, while the adjacent pixels are indicated by pink dotted lines.



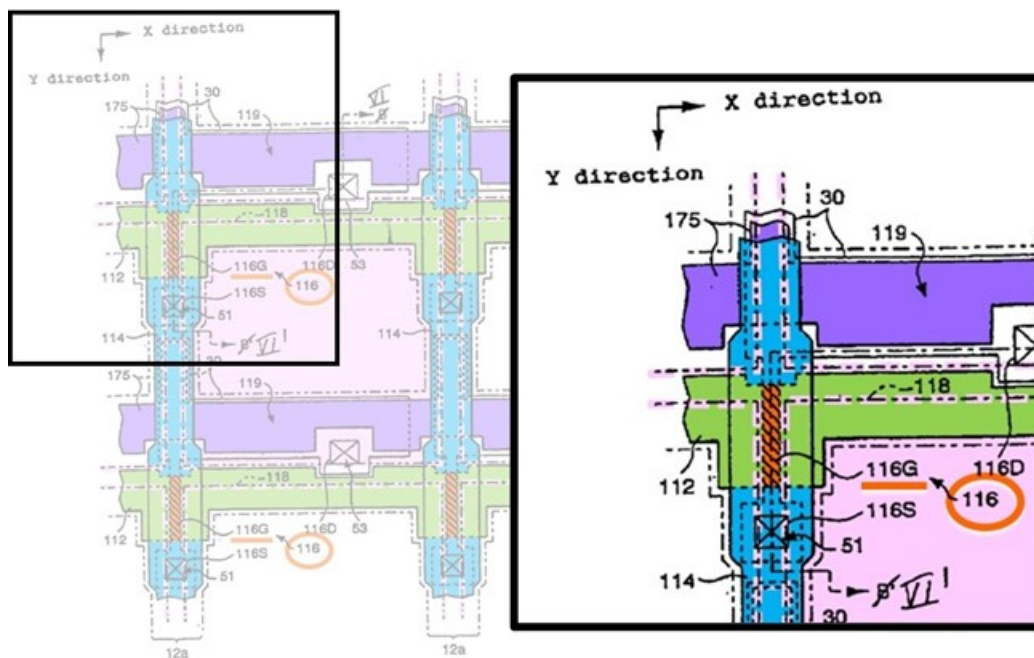
Murade-109, Fig. 5 (annotated)

194. Each **pixel electrode** in *Murade-109* is “formed correspondingly” to a TFT, because each “heavily-doped drain region 116D [of the TFT] is connected to the pixel electrode 118 by a contact hole 53.” *Murade-109*, ¶[0139].

2[c] a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor and a non-broad portion

that does not overlap the thin-film transistor, the broad portion being wider than the non-broad portion;

195. *Murade-109* discloses 2[c]. In *Murade-109*, “[t]he **data line** 114 extends in the Y direction” (vertically), as illustrated below. *Murade-109*, ¶[0137]. As discussed above in connection with 2[a], the **channel area** [30a, beneath gate 116G] also extends in the “Y direction.” See ¶¶191-192.



Murade-109, Fig. 5 (annotated)

196. As shown in the figure above, a “broad portion” of the **data line** “overlaps the thin-film transistor” (which, as discussed above in 2[a], includes the **gate** 116G of **TFT** 116). *Murade-109*’s **data line** also includes other portions that do not overlap the TFT and are narrower than the “broad portions” identified above,

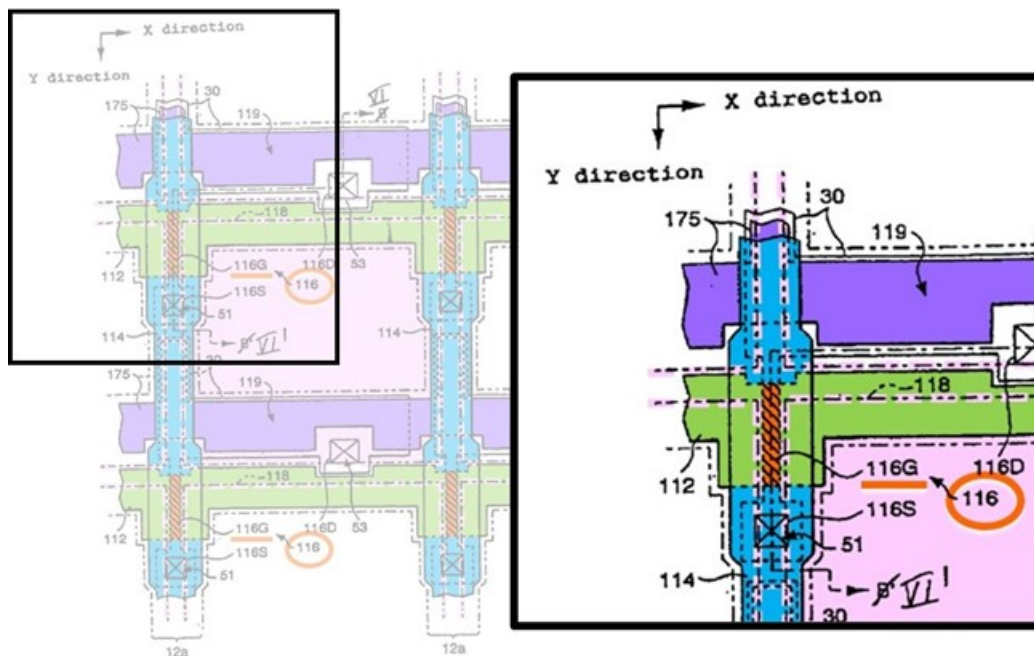
meaning that the broad portion of the **data line** is “wider than the non-broad portion,” as claimed.

197. While *Murade-109* does not provide specific measurements of the broad and non-broad portions of the **data line**, those relative widths would be apparent to a POSITA. (I note that the '079 patent also does not provide specific measurements for the broad and non-broad portions.) A POSITA would understand illustrated changes of shape within a given component (e.g., the changes in width of the **data line** where it overlaps the TFT) to convey general design information, which a POSITA would consider when implementing the disclosed design. Further, a POSITA would recognize that broadening part of the data line as illustrated in *Murade-109* would achieve design benefits, such as the design benefits known from *Kurashina*, which I discuss in ¶¶ 125-127. Thus, a POSITA viewing the reference would recognize that *Murade-109* teaches to provide the data line with a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, as claimed. Exactly how much broader to make the broad portion would be a matter of design choice for a POSITA (and is not specified by the claim in any event).

2[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width

portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;

198. *Murade-109* discloses 2[d]. For reference, “the predetermined direction” is defined above in connection with 2[a] as the horizontal “X direction” in *Murade-109*. According to *Murade-109*, the “scanning line 112 extends in the X direction” and intersects the data line 114 and channel region 30a, which “extend[] in the Y direction.” *Murade-109*, ¶[0137]; see also ¶[0130] (TFTs are “located at the intersections between the first scanning line 112 . . . and the six data lines 114”). The “scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor” is illustrated below.



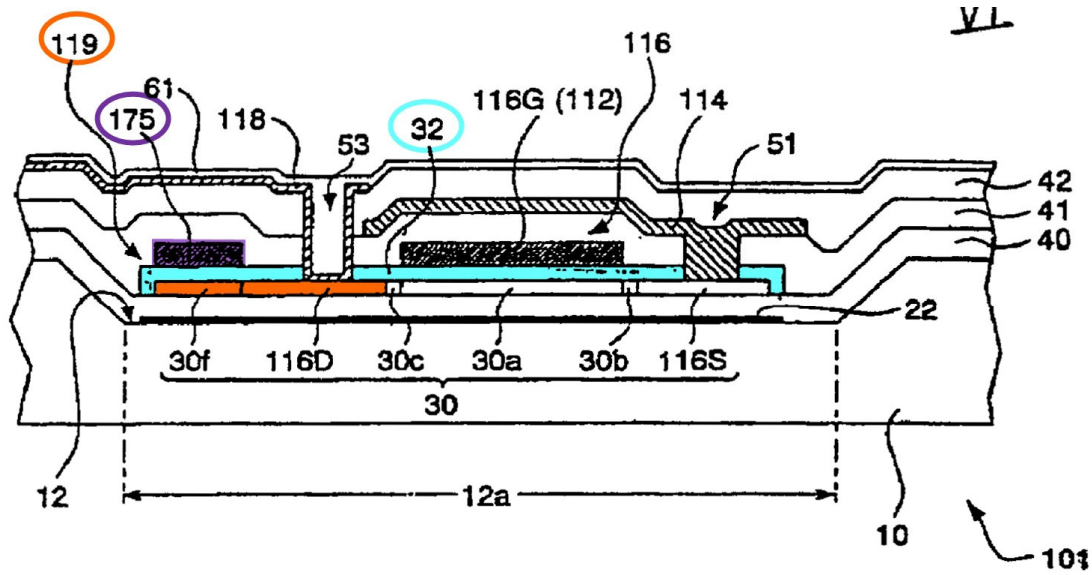
Murade-109, Fig. 5 (annotated)

199. *Murade-109* also illustrates that the **scanning line** alternates between relatively broad and narrow portions. Specifically, the **scanning line** has a “broad-width portion in a portion facing the channel area [**TFT gate 116G** above]” as well as a “narrow width portion in another portion” (i.e., the portions of the scanning line between different TFT areas). As with the data line (discussed above in ¶197), *Murade-109* does not provide specific measurements of the broad and non-broad portions of the **scanning line** (as the ’079 patent also does not provide specific measurements for the broad and non-broad portions). Nonetheless, those qualitative relative widths would be apparent to a POSITA, because a POSITA would understand illustrated changes of shape within a given component (e.g., the changes in width of the **scanning line** where it faces the TFT) to convey general design information, which a POSITA would consider when implementing the disclosed design. Further, a POSITA would recognize that broadening part of the scanning line as illustrated in *Murade-109* would achieve certain design benefits, such as the design benefits known from *Takahara* (which I discuss above in paragraphs 174-175). Thus, a POSITA viewing the reference would recognize that *Murade-109* teaches to provide the scanning line with a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion, as claimed. Exactly how much broader to make the broad portion would be

a matter of design choice for a POSITA (and is not specified by the claim in any event).

2[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and;

200. *Murade-109* discloses 2[e]. As *Murade-109* explains, “[a] portion of the **heavily doped drain region 116D** in the semiconductor layer 30 acts as one electrode of the **storage capacitor 119**. That is, in the **storage capacitor 119**, a **heavily-doped drain region 30f** located under the **capacitor line 175** acts as one electrode, and the **capacitor line 175** itself acts as the other electrode, and the **insulating film 32** formed on the semiconductor layer 30 is interposed between the two electrodes.” *Murade-109*, ¶[0140]. The storage capacitor of *Murade-109* is illustrated in Fig. 6, which I present below.



Murade-109, Fig. 6 (annotated)

201. As a fundamental matter of electronics, well understood by a POSITA, a storage capacitor is a device used to store an electrical charge, and consists of two conductors separated by an insulator or dielectric material. Ex. 1025 [Nilsson] at 4 (book page 174); Ex. 1029 [Kaplan Dictionary] at 3 (book page 92 (“capacitor”)). As in the example of *Murade-109*, the **heavily doped drain region 30f** and the **capacitor line 175** act as conductors/electrodes, and the **insulating film 32** serves as the dielectric insulating layer between the two layers, such that a fixed voltage potential difference is created between them.

202. In *Murade-109*, “[o]ne end of each storage capacitor 119 is connected to the pixel electrode 118 (the drain of the TFT 116). *Murade-109*, ¶[0120]. More specifically, pixel 118 connects to the **heavily doped drain region 116D** (and, by

extension, to the **drain region 30f**) via contact hole 53. By virtue of that connection, the **heavily doped drain region 116D** (including the **drain region 30f**) represents the potential of the pixel. *Murade-109*, ¶[0120]. In other words, the **heavily doped drain region 116D** forms the first electrode of the storage capacitor and is a “pixel-potential capacitor electrode,” as claimed.

203. The **capacitor line 175** serves as the mated electrode in *Murade-109*’s storage capacitor. As *Murade-109* explains, “the other end [of the storage capacitor 119] is connected in common by a **capacitor line 175**.” *Murade-109*, ¶[0120]. The capacitor line supplies a “fixed potential,” as claimed, because “what is required is to apply a constant voltage over time to the capacitor line 175.” *Murade-109*, ¶[0120]. As *Murade-109* explains, the fixed potential may be supplied by a constant voltage from low level side voltage V_{ssY} , “high-level-side voltage V_{ddY} , the voltage LC_{com} , or the like.” Thus, the **capacitor line 175** is a “fixed-potential capacitor electrode.” *See also Murade-109*, ¶¶[0113] (“ V_{ssY} of the power supply, which is the ground potential of [the] storage capacitor . . . is also supplied to the individual pixels via capacitor lines 175”).

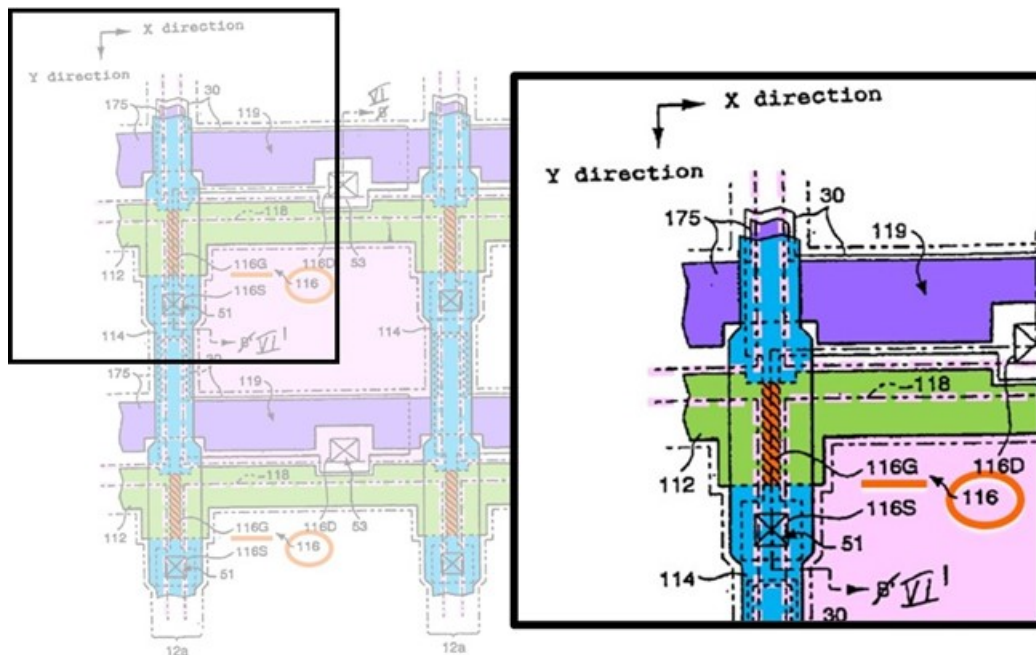
204. Finally, because the **insulating film 32** is an insulating layer that separates the two electrodes of the capacitor in *Murade-109*, allowing an electric field to build up between the two electrodes rather than allowing a current to pass

between them, the insulating film is a “dielectric film.” Ex. 1020 [Dorf] at 3 (book page 15) (“When electrical current flows into a capacitor, a force is established between two parallel plates separated by a dielectric.”); Ex. 1029 [Kaplan Dictionary] at 3-4 (book pages 92 (“capacitor”) and 184 (“dielectric”)); Ex. 1030 [Laplante Dictionary] at 3 (“dielectric”). Indeed, without a dielectric film, the device would not function as a storage capacitor. Accordingly, *Murade-109* provides 2[e].

2[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.

205. The *Murade-109* reference does not specifically describe or illustrate that the portion of the capacitive line extending along the data line has a width broader than a portion of the data line. Nonetheless, in my opinion, it would have been obvious over *Murade-109* in view of *Murade-125* to provide 2[f].

206. In *Murade-109*, “[t]he **capacitor line** 175 extends in the X direction close to and in parallel to the **scanning line** 112, and at the section intersecting with the **data line** 114, the **capacitor line** 175 protrudes (upward in FIG. 5),” as illustrated below. *Murade-109*, ¶[0137].



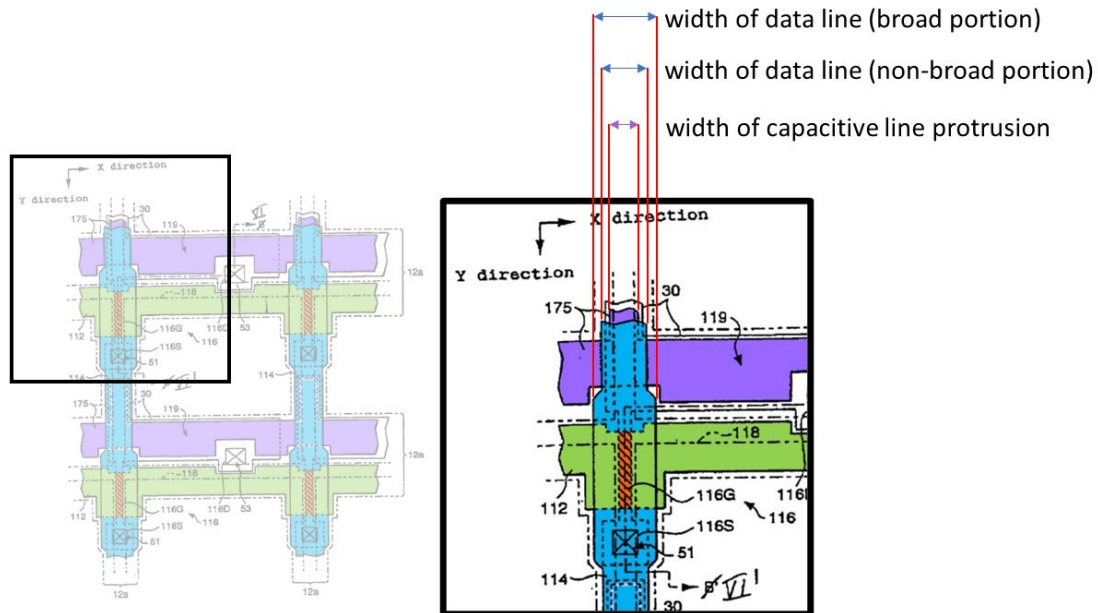
Murade-109, Fig. 5 (annotated)

207. As I discuss above in connection with 2[e] (§§200-204), the **capacitor line** has a portion that “serves as the fixed-potential capacitor electrode of the storage capacitor,” as also required by 2[f].

208. The portion of *Murade-109*’s **capacitive line** extending along the “X direction” is a “portion extending along the **scanning line**.” *Murade-109*, ¶[0137]. In other words, as illustrated above, both the **capacitive line** and the **scanning line** have portions extending horizontally, alongside each other.

209. The protruding portion of *Murade-109*’s **capacitive line** extending along the “Y direction” is a “portion extending along the **data line**”—meaning that both elements extend vertically. *Murade-109*, ¶[0137]. As illustrated below,

Murade-109 illustrates the protruding portion of the **capacitor line** as having “a width that is narrower than the broad portion of the **data line**.”



Murade-109, Fig. 5 (annotated)

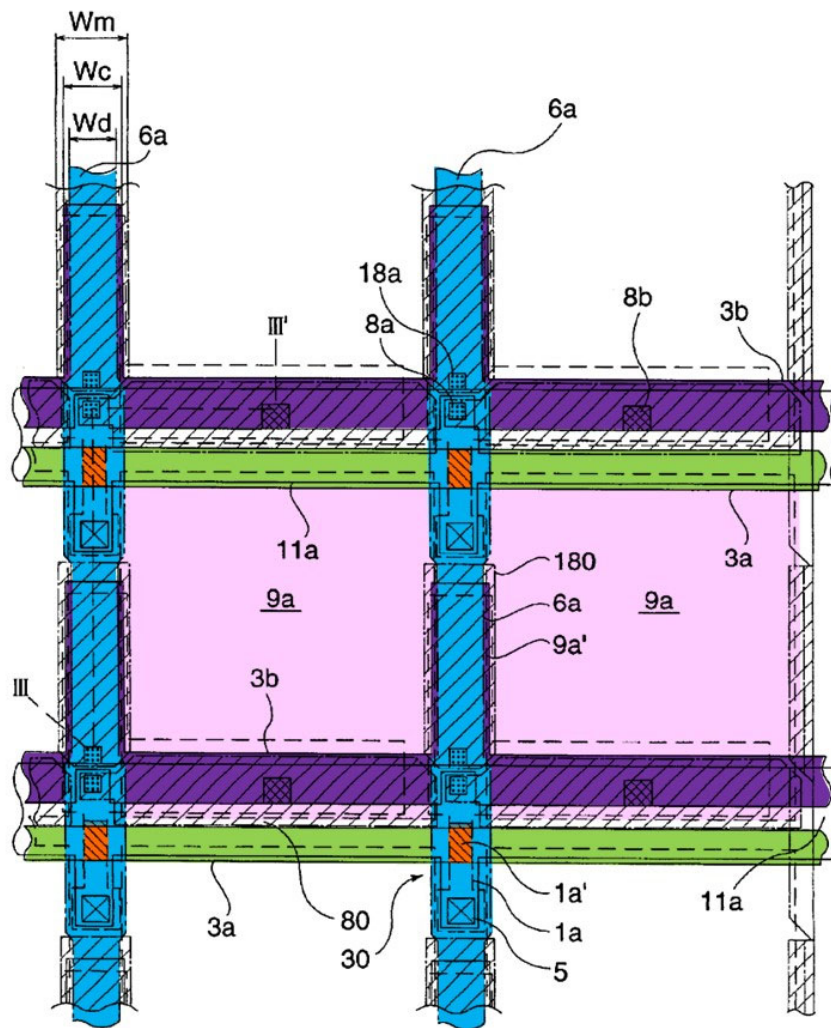
210. In the figure above, the vertical protruding portion of *Murade-109*’s **capacitor line** appears to be depicted as having a width that is *also* narrower than the non-broad portion of the data line. The reference does not describe making the protruding portion wider than the non-broad portion of the data line; however, slightly widening the protruding portion of the **capacitor line** to be wider than the non-broad portion of the **data line** (while still being narrower than the broad portion of the **data line**) would have been obvious in view of *Murade-125*.

211. *Murade-125* “pertains to the technical field of electro-optical devices of active-matrix-driven electro-optical devices, and, in particular [those with] a pixel-switching thin-film transistor (thin-film transistor; hereinbelow, called ‘TFT’ where appropriate) for pixel switching.” *Murade-125*, ¶[0001]. Thus, *Murade-125* belongs to the same technical field and is analogous art to both *Murade-109* and the ’079 patent. Compare with *Murade-109*, ¶[0004] (“active matrix liquid crystal device” with “three-terminal switching element, such as a TFT”) and ’079 patent, Abstract (“electro-optical device of the present invention includes pixel electrodes, TFTs . . . and scanning lines and data lines connected to the TFTs”). Moreover, both *Murade-125* and *Murade-109* name Masao Murade as their inventor and Seiko Epson Corporation as their original assignee⁵—which would motivate a POSITA to consider the references together and bolster the POSITA’s conclusion that the references offer compatible teachings.

212. *Murade-125*’s design includes the same general structures as *Murade-109*, including “a plurality of the transparent pixel electrodes 9a . . . provided in a

⁵ *Murade-125* was submitted in an IDS with the application for the ’079 patent, but, despite sharing an inventor and assignee, *Murade-109* was not. Ex. 1001, Cover Page.

matrix on the TFT-array substrate,” wherein the “**data lines** 6a, the **scan lines** 3a, and the **capacitor lines** 3b are respectively provided along the vertical and horizontal boundaries of the **pixel electrodes** 9a.” *Murade-125*, ¶[0057]. The general configuration of *Murade-125* is illustrated in Fig. 2, below. As illustrated, “the **TFT** 30, in which the **scan line** 3a is disposed opposing the **channel region** 1a’ as a gate electrode is provided at each intersection between the **scan line** 3a and the **data line** 6a.” *Murade-125*, ¶[0057].



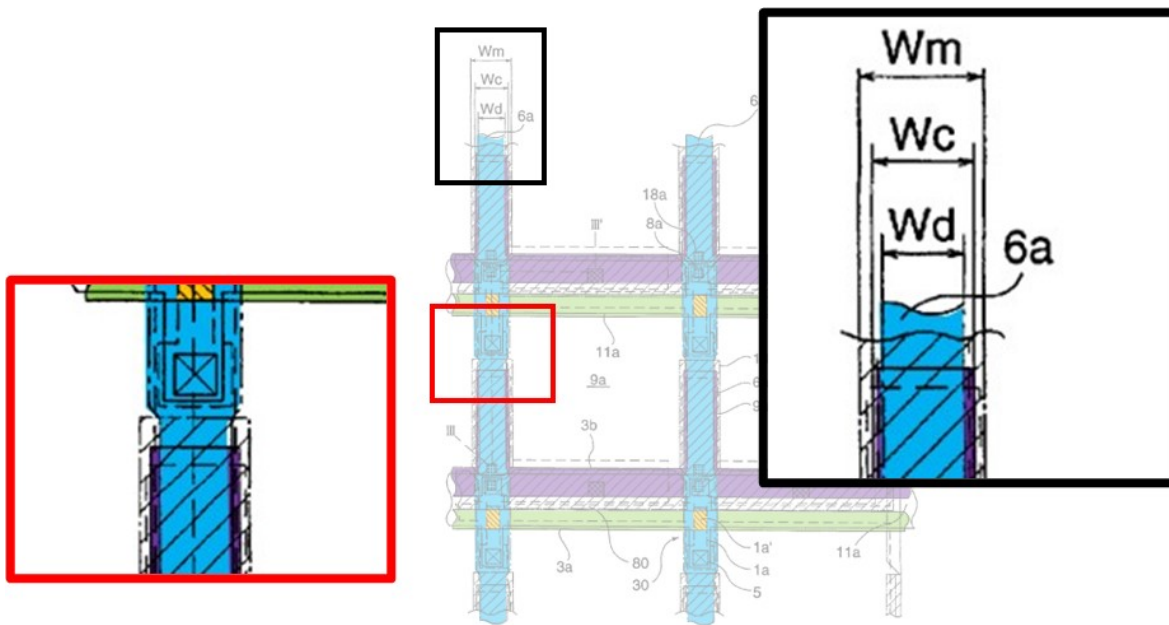
Murade-125, Fig. 2 (annotated)

213. *Murade-125* identifies a “strong general demand for increased display image quality,” and teaches that “to this end, it is extremely important to increase the pixel aperture ratio (i.e., to increase the size of the aperture region of a pixel, through which display light passes, relative to the light-shielding region thereof, through which display light does not pass) while reducing pixel pitch.” *Murade-125*,

¶[0004]. At the same time, however, *Murade-125* cautions that reducing pixel pitch “results in problems such as making it more difficult to incorporate the storage capacitors described above, especially as the pixel pitch is reduced, or to ensure the regions in which the contact holes are to be formed” *Id.*, ¶[0005]. *Murade-125* teaches to address those issues, while simultaneously providing improved light blockage and improved capacitance by making the capacitor electrode wider:

The “**capacitor electrode** further has a portion that extends along the **data line** as seen in plan view, and a width W_d of the **data line**, a width W_c of the **capacitor electrode**, and a width W_m of the portion of the intermediate conductive layer that extends along the data line satisfy the relationship $W_d < W_c < W_m$ at a location along the data line.”

Id., ¶¶[0041], [0094]. Thus, as illustrated in Figure 2 below, *Murade-125* teaches making the protruding portion wider than the non-broad portion of the data line, as required by 2[f].



Murade-125, Fig. 2 (annotated detail)

214. A POSITA further would understand *Murade-125*'s relatively wide capacitor line protruding portion to achieve desirable improvements in performance. According to *Murade-125*, "Al (aluminum) film is typically used as the material of the **data line** [because of] its low wire resistance." *Murade-125*, ¶[0042]. Aluminum, however, is a "reflective film of extremely high reflectivity," meaning that "when a [TFT] is shielded solely by a data line formed from an Al film, projected light or returning light that is oblique to the surface of the substrate is reflected by the inner surface of the data line (i.e., the surface on the side facing the thin-film transistor), causing multiple reflection within the layered structure and ultimately causing the problem in which light reaches the channel region or regions adjacent

thereto.” *Id.* Widening the capacitive line relative to the data line (a) “attenuates multiply reflected light caused by internal reflection as described above” and (b) a “larger storage capacitor can be constructed using the capacitor electrode and the intermediate conductive layer, which are wider than the data line.” *Id.* A POSITA would thus be motivated to implement the reflection-attenuating and capacitor-enhancing features of *Murade-125* with the design of *Murade-109* to achieve improved performance.

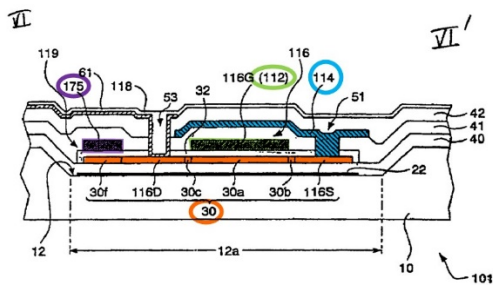
215. I note that a POSITA implementing *Murade-109*’s capacitor line projection with a width wider than the narrow portion of the data line (according to *Murade-125*) would have no motivation to make the capacitor line projection wider than the *broad portion* of the data line and would understand not to do so. In *Murade-109*, the wide portion of the data line does not overlap the capacitor line. Thus, making the capacitor line wider than the broad portion of the data line would add material cost and reduce the aperture of the pixel area *without* achieving the benefit of shielding against internal reflection by that portion of the data line. Further, widening the capacitor line will increase capacitance only to the extent it overlaps its mated electrode (30f), meaning no increase in capacitance would be achieved by unduly increasing the capacitor width significantly beyond the width of the data line portion it overlaps. For that reason, it would have been an obvious and efficient

design choice for a POSITA to make the capacitor line projection wider than the narrow portion of the data line but narrower than the broad portion of the data line.

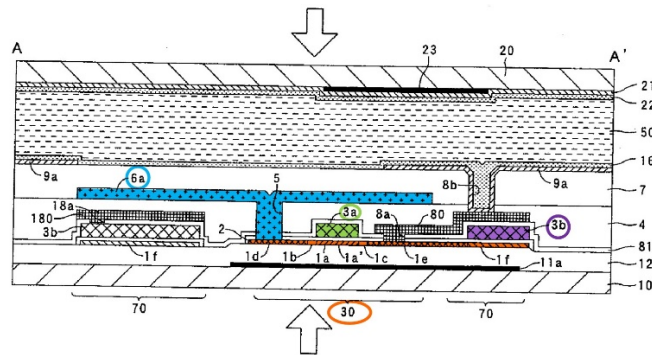
216. *Murade-109* and *Murade-125* are each analogous art to the '079 patent, at least because each “is from the same field of endeavor” of active-matrix drive electro-optical devices, such as may be used for LCD displays. Compare *Murade-109*, ¶[0004] (“active matrix liquid crystal device” with “three-terminal switching element, such as a TFT”) with *Murade-125*, ¶[0001] (“active-matrix-driven electro-optical devices,” particularly those with “a pixel-switching thin-film transistor”) and '079 patent, Abstract (“electro-optical device of the present invention includes pixel electrodes, TFTs . . . and scanning lines and data lines connected to the TFTs”).

217. In addition, *Murade-125* offers improvements to improve display quality, reduce light leakage, and improve capacitance, which a POSITA would recognize as desirable modifications when implementing the design of *Murade-109*. In particular, it was well-known at the relevant time—including from the teachings of *Murade-125*—that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel. A POSITA would thus consider references such as *Murade-125* to be pertinent when implementing an active-matrix drive system such as *Murade-109*.

218. In my opinion, it would have been obvious and straightforward to a POSITA at the relevant time (before December 2002) to implement *Murade-109*'s design with the capacitance line projections taught by *Murade-125*. The references include similar layer structures, with each including a TFT (30 in both), data line (114 in *Murade-109*, 6a in *Murade-125*), scan line (112 in *Murade-109*, 3a in *Murade-125*), and capacitor line (175 in *Murade-109*, 3b in *Murade-125*), as illustrated below. Thus, making the modification would require no more than changing the relative size of existing components such as the data line and capacitive line projection, which were modifications well within the level of ordinary skill in the art at the time.



Murade-109, Fig. 6



Murade-125, Fig. 3

219. Moreover, a POSITA would recognize that the benefits of *Murade-125*'s light-shielding improvements would be additive to the design already present

in *Murade-109*, and providing those improvements would be a simple matter of design choice. Further, in my opinion, the combination of *Murade-109* and *Murade-125* would yield a “a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line,” just as the claim requires.

220. It is also my opinion that combining the teachings of *Murade-109* and *Murade-125* would have required no more than ordinary skill because the combination would have been a simple modification of an existing component (capacitive line and/or data line) in a straightforward manner to achieve predictable results. For the reasons discussed above, the combination of references would have had a reasonable expectation of success given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Murade-125* could be integrated into *Murade-109*'s device. In other words, modifying the relative widths of *Murade-109*'s data line and scanning line according to *Murade-125*'s teachings would be a straightforward and predictable improvement to *Murade-109*'s device.

221. Thus, in my opinion, *Murade-109* and *Murade-125* render obvious claim element 2[f]. Further, because *Murade-109* in view of *Murade-125* provide every limitation of independent claim 2, their combination renders the claim obvious.

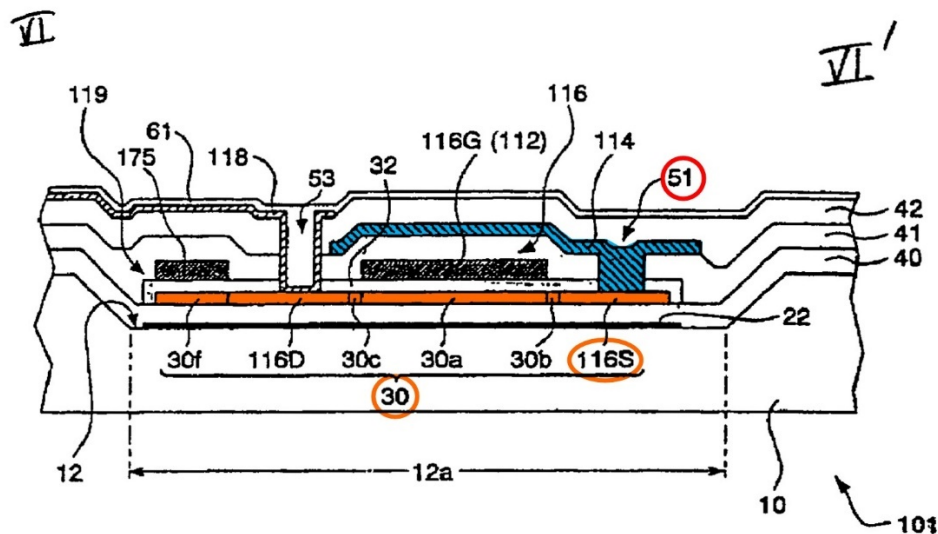
B. Claim 3

3: The electro-optical device according to claim 2, further comprising a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.

222. Claim 3 depends from claim 2 and, thus, incorporates every limitation of claim 2. The combination of *Murade-109* and *Murade-125* provide those limitations as set forth in the section above. In addition, as explained below, it is my opinion that *Murade-109* discloses the additional limitation of claim 3.

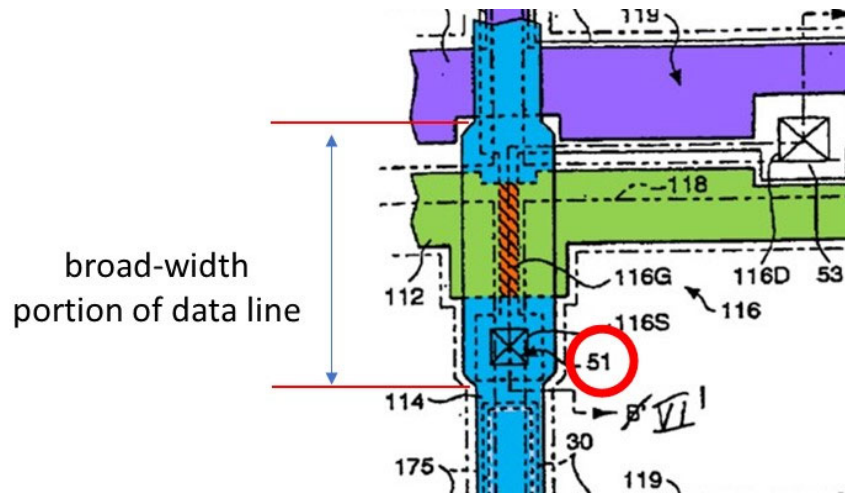
223. According to *Murade-109*, the “**heavily doped source region 116S** is connected to the **data line** by a **contact hole** 51 made through the insulating film 32 and a first interlayer insulating film 41.” *Murade-109*, ¶[0139], Fig. 6 (below). As I explain above in connection with 2[a] (¶¶191), the heavily doped source region 116S is part of the TFT (30). See *Murade-109*, ¶¶[0138], [0163] (“TFT has an LDD structure in which . . . a heavily-doped source region 116S [is] provided”). Thus, because the data line material extends through contact hole 51 to the TFT, the data

line electrically connects to the TFT through contact hole 51. In other words, *Murade-109* provides the claimed “contact hole that electrically connects the thin-film transistor and the data line.”



Murade-109, Fig. 6 (annotated)

224. *Murade-109* also discloses “the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.” The plan-view illustration of *Murade-109* (Figure 5, below) shows the **data line** 114 being broad—i.e., “broader than the width of the ‘narrow width portion’”—throughout its entire extent from a portion that overlaps the **TFT** (30a, beneath gate portion 116G) through to the **contact hole** (51). In other words, the broad portion is “continuously broad,” as a POSITA would understand that term.



Murade-109, Fig. 5 (annotated)

225. Thus, in my opinion, *Murade-109* in view of *Murade-125* provides every limitation of claim 3 and, together, renders obvious claim 3, because *Murade-109* provides “a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.”

C. Independent Claim 1

1[pre] An electro-optical device, comprising:

226. *Murade-109* discloses the preamble of claim 1. As I explain above in 2[pre] (§190) *Murade-109* provides an “electro-optical device, comprising.” Because the preamble of claim 1 is identical to claim 2, *Murade-109* provides the preamble of claim 1 for the same reasons.

1[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

227. *Murade-109* discloses 1[a]. As I explain above in 2[a] (§§191-192), *Murade-109* provides “a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction.” Because 1[a] is identical to 2[a], *Murade-109* provides 1[a] for the same reasons.

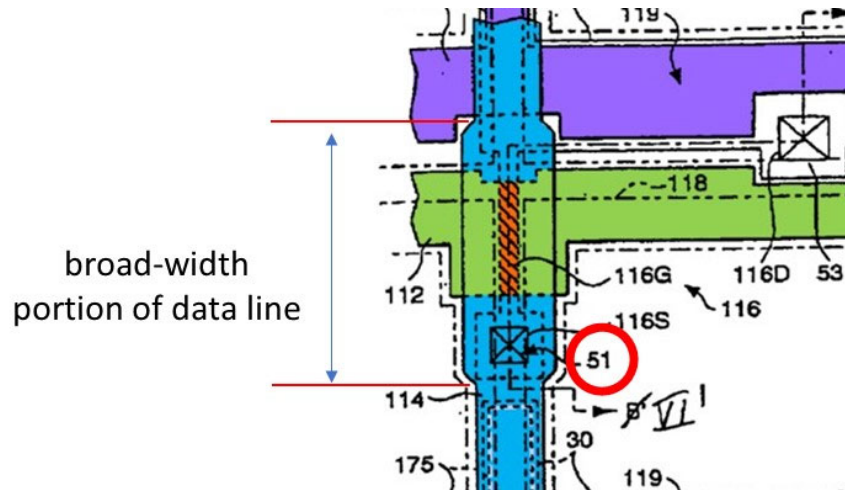
1[b] a pixel electrode formed correspondingly to the thin-film transistor;

228. *Murade-109* discloses 1[b]. As I explain above in 2[b] (§§193-194), *Murade-109* provides “a pixel electrode formed correspondingly to the thin-film transistor.” Because 1[b] is identical to 2[b], *Murade-109* provides 1[b] for the same reasons.

1[c] a data line extending in the direction in which the channel area extends, the data line having a broad-width portion that overlaps the channel area in plan view;

229. *Murade-109* discloses 1[c]. As I explain above in 2[c] (§§195-197), *Murade-109* provides “a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor” Limitation 1[c] recites substantially identical structure; therefore, *Murade-109* provides 2[c] for the same reasons. I further note 1[c] specifies that the broad-width portion overlaps the channel area “in plan view,” and the overlap

discussed above in ¶¶195-197 (and illustrated in *Murade-109* Figure 3, below) is “in plan view.”

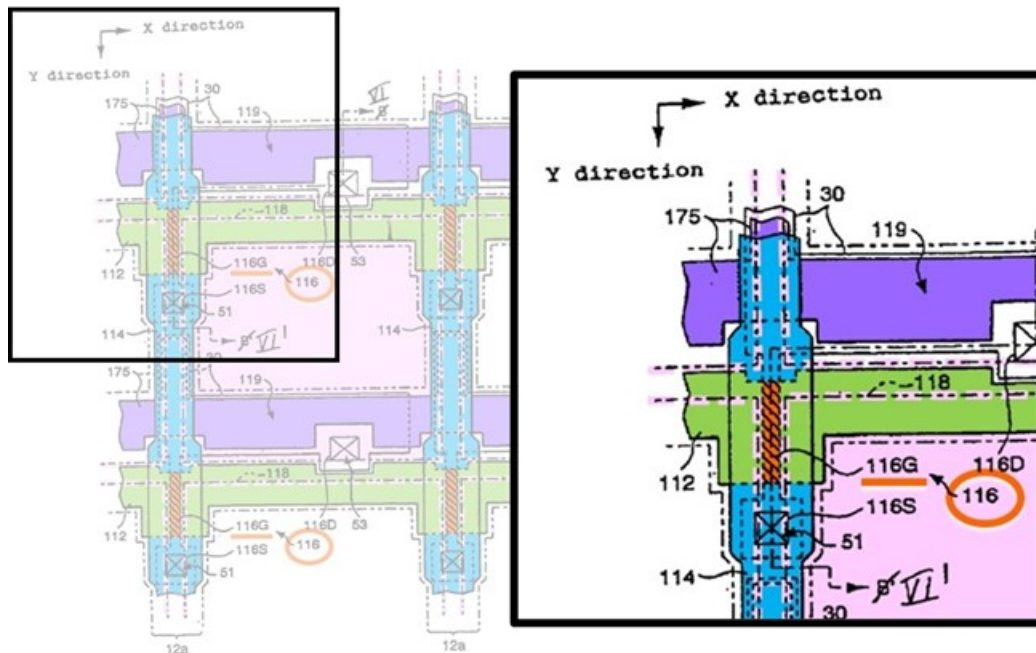


Murade-109, Fig. 5 (annotated)

1[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion;

230. *Murade-109* discloses 1[d]. As I explain above in 2[d] (¶¶198-199), *Murade-109* provides “a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.” As compared to 2[d], element 1[d] recites that (i) the scanning line has a broad-width portion in a portion

“overlapping” (instead of “facing”) the channel area and (ii) the overlap is “in plan view.” Those differences in verbiage, however, make no meaningful difference with respect to the design of *Murade-109*, because as illustrated in Figure 5 of *Murade-109* (discussed in ¶¶198-199 above and reproduced below) (i) the broad-width portion of the scanning line is *both* “facing” and “overlapping” the TFT channel and (ii) Figure 5 shows the overlap “in plan view.”



Murade-109, Fig. 5 (annotated)

1[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential

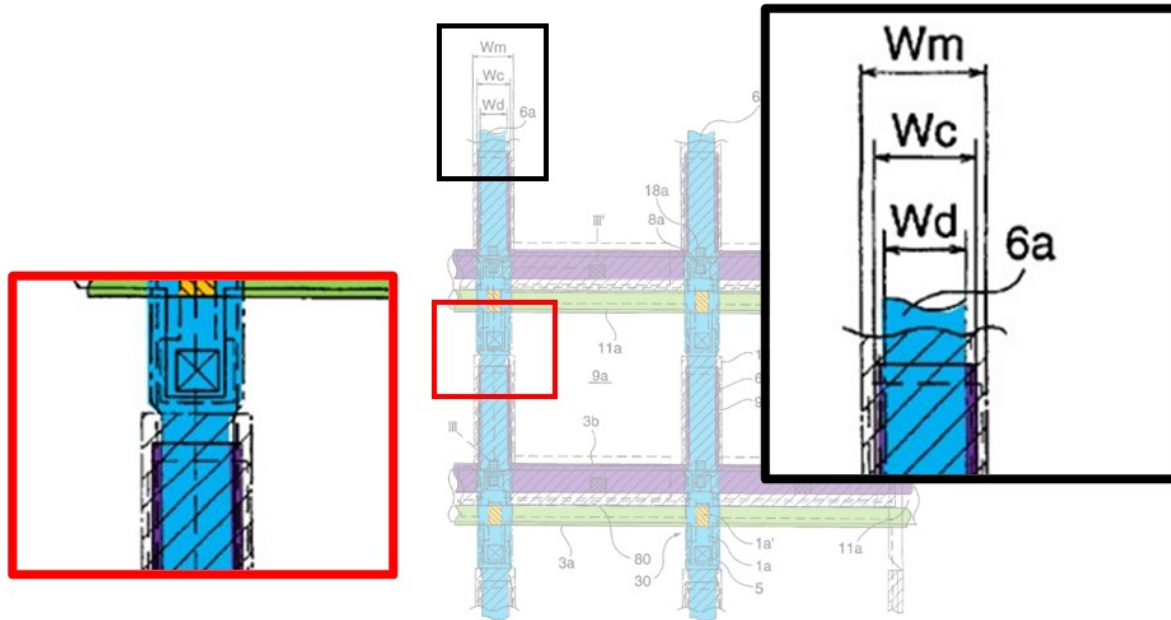
capacitor electrode and the fixed-potential capacitor electrode;

231. *Murade-109* discloses 1[e]. As I explain above in 2[e] (§§200-204), *Murade-109* provides “a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode.” Because 1[e] is identical to 2[e], *Murade-109* provides 1[e] for the same reasons.

1[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and

232. It is my opinion that 1[f] would have been obvious over *Murade-109* in view of *Murade-125* for the same reasons as 2[f], which I explain above in paragraphs 205-221. Specifically, as I explain above in paragraphs 205-221, the combination of *Murade-109* and *Murade-125* provides “a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width . . . that is wider than the non-broad portion of the data line.” As I discuss in

connection with 2[f] and as I illustrate below, the portion of *Murade-125*'s **capacitor line** (width W_c) that extends along the **data line** is broader than the non-broad portion of the data line (width W_d), meaning it is broader than “a width of the data line” as claimed.



Murade-125, Fig. 2 (annotated detail)

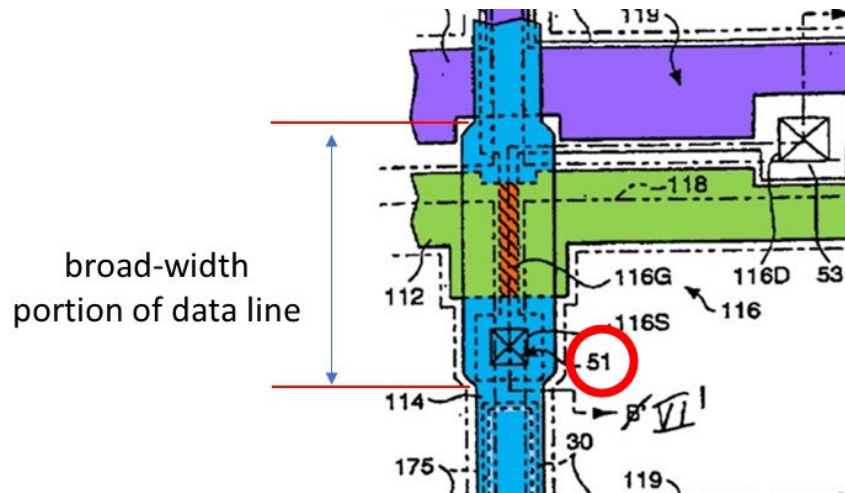
233. Thus, it would have been obvious in the combination of *Murade-109* with *Murade-125* to provide “the portion extending along the data line having a width that is equal to or broader than a width of the data line.”

1[g] a contact hole electrically connecting the data line and the thin film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that

extends beyond the channel area in a direction extending from the channel area toward the contact hole.

234. *Murade-109* discloses 1[g]. As I explain above in connection with Claim 3, *Murade-109* provides “a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.” Substantively, 1[g] is broader in that it omits the “continuously broad” limitation. As such, the contact hole of 1[g] need only be positioned “at a portion of the broad-width portion of the data line,” which “extends beyond the channel area in a direction extending from the channel area toward the contact hole.”

235. *Murade-109* discloses this limitation for the same reasons as it disclosed Claim 3. As I illustrate below, a portion of the broad width portion of the **data line** 114 extends beyond the **channel area of TFT** in a direction (vertically down) extending from the channel area toward the contact hole. The **contact hole** (51) is positioned at the foregoing “portion of the broad-width portion of the **data line**.”



Murade-109, Fig. 5 (annotated)

236. In summary, for the reasons set forth above, it is my opinion that *Murade-109* in view of *Murade-125* provides every limitation of independent claim 1 and, together, the combination renders obvious claim 1.

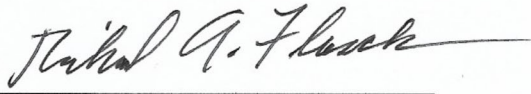
XII. CONCLUSION

237. For the reasons set forth above, I believe claims 1-3 of the '079 patent are unpatentable in view of the prior art. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

Declaration of Richard A. Flasck
U.S. Patent No. 7,502,079

I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 3, 2024

By: 
Richard A. Flasck