

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

Case No. IPR2024-00976
U.S. Patent No. 7,502,079

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,502,079**

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LIST OF EXHIBITS

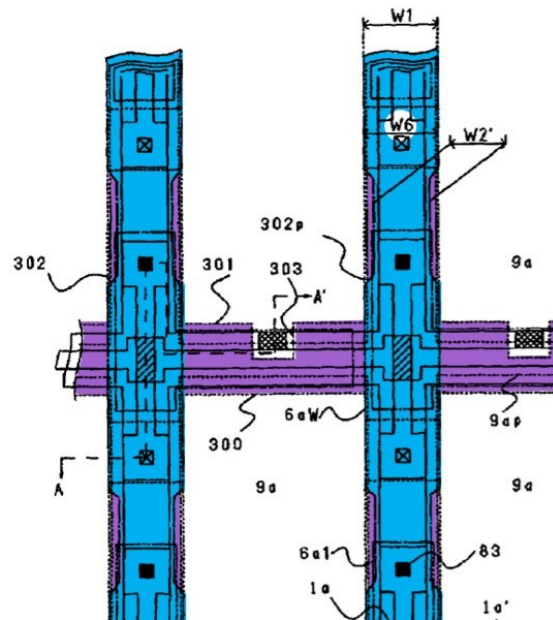
Exhibit	Description
Ex. 1001	U.S. Patent No. 7,502,079 to Murade (“’079 patent”)
Ex. 1002	Declaration of Mr. Richard A. Flasck (“Flasck”)
Ex. 1003	Curriculum Vitae of Mr. Richard A. Flasck
Ex. 1004	Prosecution File History of the ’079 patent
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Ex. 1006	JP-2002-000713 (Jan. 7, 2002) Asserted Foreign Priority Application for the ’079 Patent – Certified Translation, Supporting Declaration, and Original
Ex. 1007	Reserved
Ex. 1008	JP-2002-090721A to Kurashina (“ <i>Kurashina</i> ”) – Certified Translation, Supporting Declaration, and Original
Ex. 1009	U.S. Pub. No. 2002/0014627A1 to Sato (“ <i>Sato</i> ”)
Ex. 1010	JP-2002-158360A to Takahara (“ <i>Takahara</i> ”) – Certified Translation, Supporting Declaration, and Original
Ex. 1011	U.S. Pub. No. 2001/0048109A1 to Murade (“ <i>Murade-109</i> ”)
Ex. 1012	JP-2001-331125A to Murade (“ <i>Murade-125</i> ”) – Certified Translation, Supporting Declaration, and Original
Ex. 1013	U.S. Patent No. 5,668,379 to Ono (“ <i>Ono</i> ”)
Ex. 1014	U.S. Patent No. 5,831,694 to Onisawa (“ <i>Onisawa</i> ”)
Ex. 1015	U.S. Patent No. 6,388,721 to Murade (“ <i>Murade-721</i> ”)
Ex. 1016	U.S. Patent No. 5,748,276 to Uno (“ <i>Uno</i> ”)
Ex. 1017	L.W. MacDonald and A.C. Lowe, Display Systems (1997) (excerpts)

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Ex. 1018	W. den Boer, Active Matrix Liquid Crystal Displays: Fundamentals and Applications (2005) (excerpts) (“den Boer”)
Ex. 1019	S. Lee et al., “Amorphous Silicon Thin Film Transistor Fabricated with a New Copper Dry Etching Method,” Electrochemical Society Proceedings, vol. 2000-31 (2000) (“Lee”)
Ex. 1020	R.C. Dorf, ed., The Electrical Engineering Handbook (2d. Ed. 1997) (excerpts) (“Dorf”)
Ex. 1021	Complaint for Patent Infringement filed in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP, Dkt. 1 (E.D. Tex.) (Nov. 8, 2023), ECF No. 1
Ex. 1022	Docket Control Order in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP, Dkt. 37 (E.D. Tex.) (Apr. 9, 2024)
Ex. 1023	Plaintiff’s Infringement Contentions in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP (E.D. Tex.) (Mar. 11, 2024)
Ex. 1024	Excerpt from Federal Court Management Statistics—Profiles (Dec. 31, 2023), available for download at https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-december-2023 (last accessed June 4, 2024)
Ex. 1025	J.W. Nilsson and S.A. Riedel, Electric Circuits (9th Ed. 2011) (excerpts) (“Nilsson”)
Ex. 1026	R.A. Street, Technology and Applications of Amorphous Silicon (2000) (excerpts) (appearing in Mr. Flasck’s declaration only)
Ex. 1027	J. Kanicki, ed., Amorphous & Microcrystalline Semiconductor Devices, Vol. II: Materials and Device Physics (1992) (excerpts) (appearing in Mr. Flasck’s declaration only)

Exhibit	Description
Ex. 1028	T. Yamazaki, et al., “Color TFT Liquid Crystal Displays” (1996) (excerpts) (appearing in Mr. Flasck’s declaration only)
Ex. 1029	S. Kaplan, Wiley Electrical and Electronics Engineering Dictionary (2004) (excerpts) (appearing in Mr. Flasck’s declaration only)
Ex. 1030	P.A. Laplante, Electrical Engineering Dictionary (2000) (excerpts) (appearing in Mr. Flasck’s declaration only)
Ex. 1031	U.S. Patent No. 6,380,560B1 to Yamazaki (“Yamazaki-560”)

I. PRELIMINARY STATEMENT

Petitioner BOE Technology Group requests *inter partes* review of claims 1-3 of U.S. Patent No. 7,502,079, assigned to Patent Owner 138 East LCD Advancements Limited. The '079 patent addresses “high precision and miniaturization requirements imposed in related art electro-optical devices” with a **data line** (6aW, 6a1) that is partly *broad*er and partly *narrow*er than a **capacitive line** (302, 302p) that it overlaps. *See* Ex. 1001, 23:1-7, Fig. 16 (below).¹

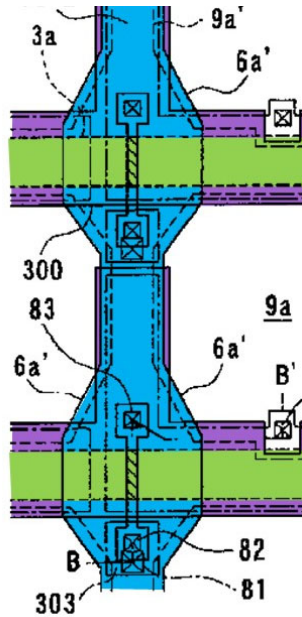


Ex. 1001, Fig. 16

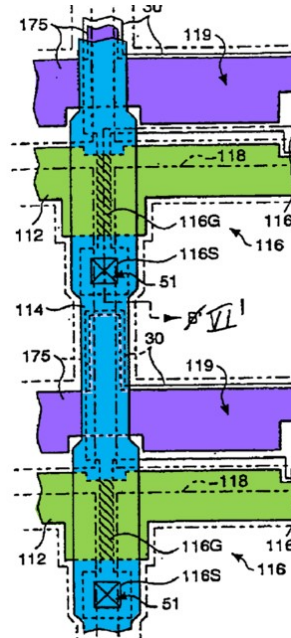
During prosecution, applicant relied on these relative widths to distinguish the prior art. Those features, however, were already well known. For example, both

¹ All colorization and emphasis of text and figures herein has been added.

Kurashina (Ex. 1008) and *Murade-109* (Ex. 1011) disclosed broad/narrow portions in their **data lines** as illustrated below.



Kurashina, Fig. 3



Murade-109, Fig. 5

Because every claimed feature was well-known and obvious, Petitioner requests that the Board institute *inter partes* review and cancel all claims.

II. OVERVIEW OF TECHNOLOGY

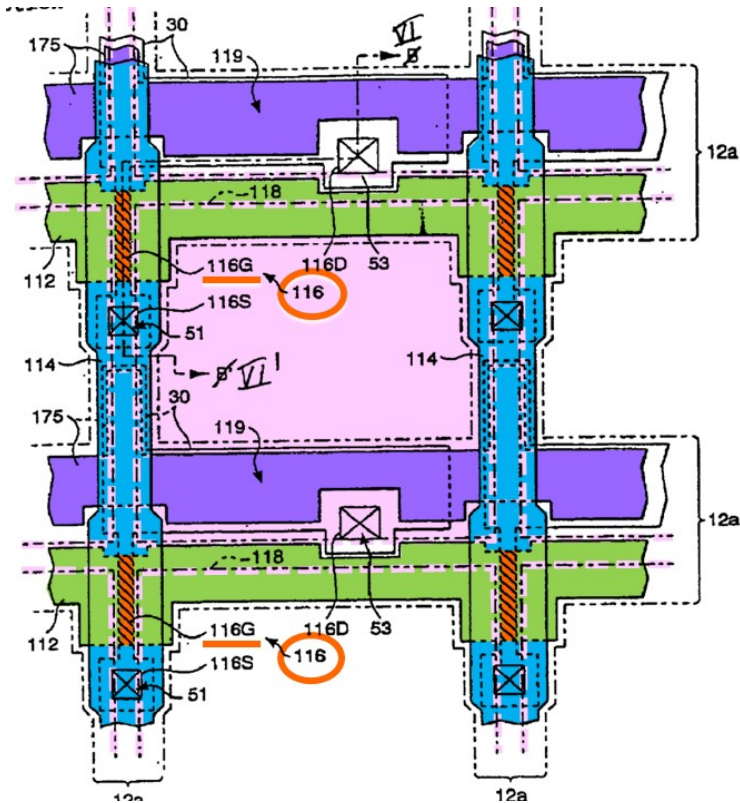
A. Active-Matrix Control of LCD Pixel Displays

Active-matrix drive liquid crystal display (AMLCD) technology comprises an array of color pixels and sub-pixels, each of which is controlled by a thin-film transistor (TFT), and acts as a shutter allowing light to selectively pass through. Flasck ¶59. Before the '079 patent, an AMLCD device was known to have the following basic structure:

[O]ne substrate ... is provided with a plurality of **scanning lines** [112] and a plurality of **data lines** [114] intersecting with each other. At each intersection thereof, a three-terminal switching element, such as a TFT (Thin Film Transistor) [**TFT gate** 116G highlighted below²], and a **pixel electrode** [118] are formed as a set, and peripheral circuits for driving the individual scanning lines and data lines are provided in the periphery of the region (display region) in which these **pixel electrodes** are formed. The other substrate is provided with a transparent counter electrode facing the **pixel electrodes**.

Murade-109, ¶[0004], Fig. 5 (below); Flasck ¶68.

² As illustrated in *Murade-109*, the TFT comprises a heavily-doped source region (116S), gate electrode (116G), and heavily-doped drain region (116D). *Murade-109*, ¶[0138]; Flasck ¶192.



Murade-109, Fig. 5

Signals along the scanning and data lines are used to selectively block or transmit light through individual pixels of the display. Flasck ¶69; *see* Ex. 1001, 1:28-38.

B. Optimization of LCD Pixels for High-Definition Displays

At least by the mid-1990's, the art recognized that the “needs for LCD devices as display units are increasing as information processing devices such as personal computers become smaller in size and lighter in weight and are used more widely.” *Onisawa*, 1:9-12. As such, the art was pushing for “improvement of

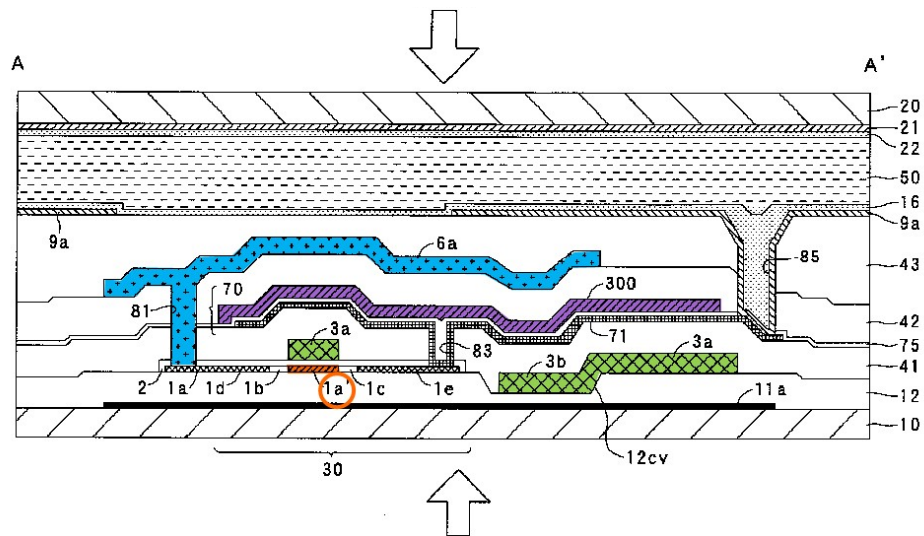
performance such as larger display area, higher resolution, faster response and full color.” *Id.*, 1:12-14; Flasck ¶70.

The art sought to improve resolution and brightness by increasing pixel density (a/k/a reducing “pixel pitch”) and/or the “area of the aperture relative to the area of the complete light valve” (a/k/a “aperture ratio”). Flasck, ¶71; Ex. 1017 at 4. A POSITA understood that narrowing the width of components between the pixels could increase aperture ratio by minimizing light blockage by peripheral components and traces when the pixel is illuminated. Flasck ¶71. *Murade-109* (Fig. 5, above), narrowed portions of the **data line** (114) and **scanning line** (112) between the **pixel electrodes** (118). Flasck ¶71. At the same time, however, portions of the **data line** and **scanning line** forming the TFT require certain minimum dimensions to properly function. Flasck, ¶72 (citing Ex. 1019 at 3; Ex. 1031, 1:45-53). Accordingly, a POSITA understood to form TFT portions broader than the other portions, as shown by *Murade-109* and references like *Sato*, which specifically provided “scanning lines” that are “widened at portions where they act as the gate electrodes.” *Sato*, ¶[0091]; *see also Takahara*, ¶[0053] (scanning line “formed with a wide width at the location at which it becomes the gate electrode”); Flasck, ¶72.

Reducing pixel pitch, however, made it “more difficult to implement sufficient light shielding” to protect the TFT channel against light leakage causing

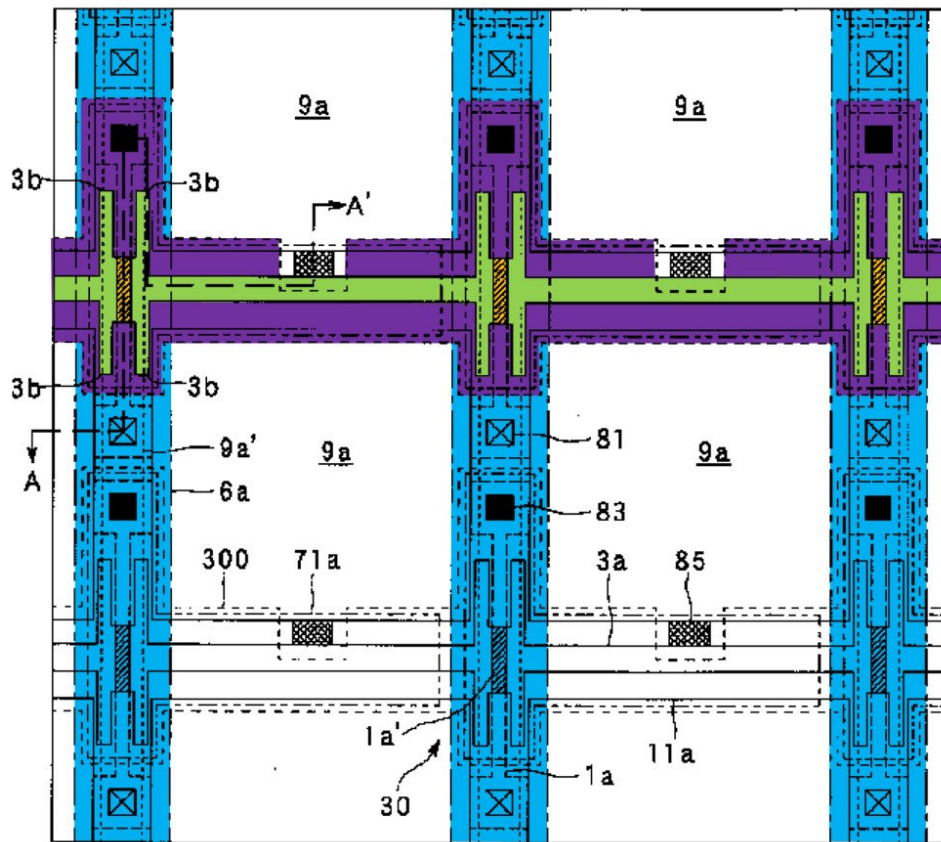
“flicker or the like due to changes in the transistor characteristics of the TFT.”

Takahara, ¶[0006]. To solve that problem, capacitive lines, data lines, and scanning lines were designed to block light leakage. Flasck, ¶75. For example, *Takahara* provided a **capacitor line** and **data line** as “light shielding films” overlapping the **TFT channel** (1a’). *Id.*, ¶[0082], Fig. 3 (below).



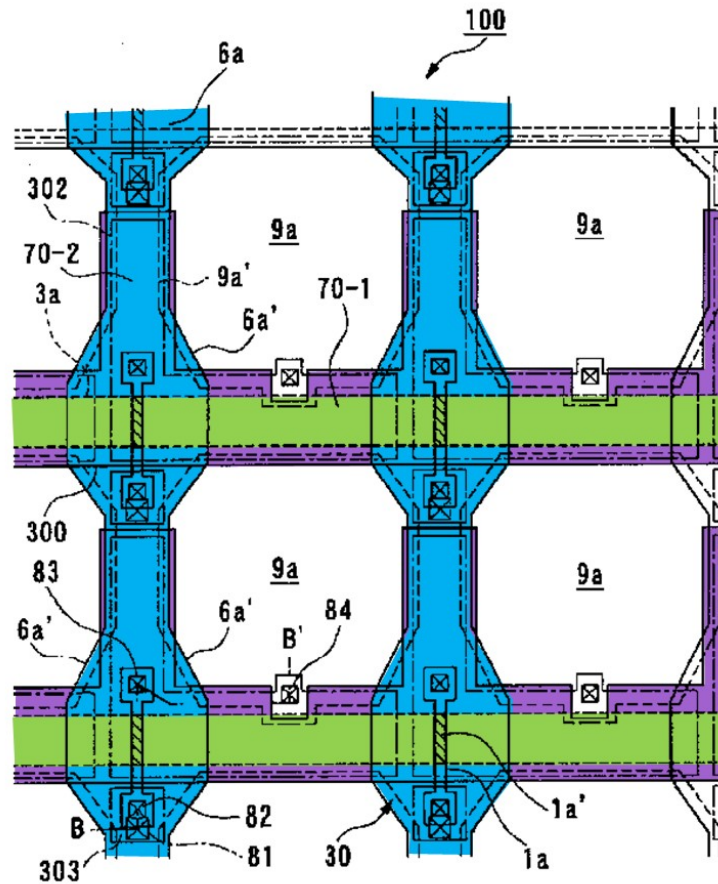
Takahara, Fig. 3

Further, *Takahara*’s **scanning lines** also blocked light, e.g., via “**protruding portions**” (3b) near the TFT gates to improve “the light-shielding performance ... with respect to oblique light that impinges three-dimensionally from various directions.” *Id.*, ¶[0018], Fig. 2 (below).



Takahara, Fig. 2

Light coming from the pixel corners presented another source of light leakage. *Kurashina*, ¶¶[0015]-[0017]; *Flasck*, ¶77. To address that issue, the art provided a **data line** “formed with a wide width in the vicinities of the TFTs 30.” *Kurashina*, ¶[0052], Fig. 3 (below). Such a **data line** varies from a narrow width (narrower than an overlapped portion of the **capacitance line**) to a broad width (wider than the **capacitance line**). *Flasck*, ¶77.



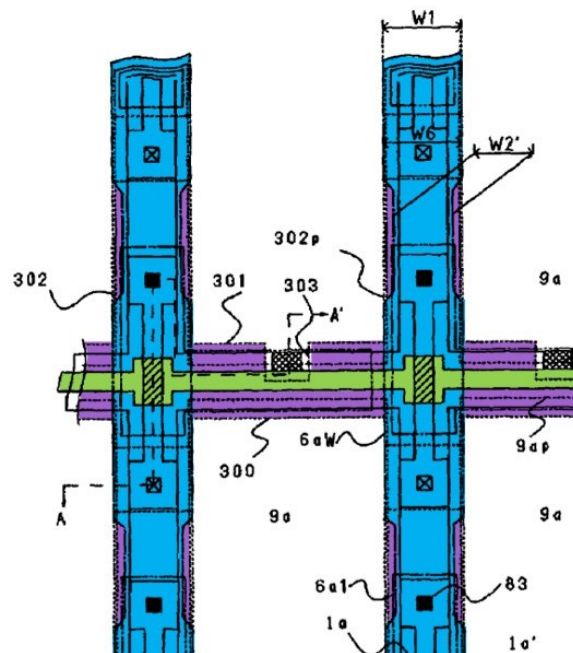
Kurashina, Fig. 3

In summary, the challenges of improving active-matrix controlled electro-optical LCD displays, the related consequences of light leakage (and solutions of using widened portions of the data line, capacitive line, and scanning line for shielding), and the requirement to use a relatively wide/long gate portion were well understood before the '079 patent. Flasck, ¶78.

III. THE '079 PATENT

A. Alleged Invention

The '079 patent addresses technical problems associated with “precisely driving the TFTs [of an electro-optical device] ... while satisfying the high precision and miniaturization requirements imposed in related art electro-optical devices.” Ex. 1001, 1:45-48. The '079 patent addresses this problem by (1) providing a **scanning line** with a “broad width portion as a gate electrode in a portion facing a channel area of the respective thin-film transistor” and (2) forming a **data line** “locally broad” at the portion “overlapping the thin-film transistor” such that “light entered from the upper portion of the thin-film transistor can be more securely prevented or reduced.” Ex. 1001, 2:33-36, 8:66-9:7.



Ex. 1001, Fig. 16

The '079 patent acknowledges that the components of an LCD were known in the prior art. *See* Ex. 1001, 1:28-38; Flasck, ¶79. The '079 patent describes a “third exemplary embodiment,” illustrated above, in which a vertical “**data line** 6a1 includes a broad width portion 6aW of which a portion overlapping the TFT 30 is formed locally broad.” Ex. 1001, 22:65-23:1; Fig. 16.

As illustrated, the width of the data line varies between W2' (narrow portion) to W6 (wide portion). Ex. 1001, 23:1-7. A projection (302p) of the **capacitive line** has a width W1, which is “broader than a width W2” and “almost equal to a width W6 of the broad width portion 6aW in the data line 6a1.” *Id.* As recited in claim 2, $W2' < W1 < W6$. *Id.*; Flasck, ¶81. According to the '079 patent, “since the broad width portion 6aW of the data line 6a1 and the protruded portion 302 of the capacitive line 300 ... exist on the TFT 30, [a] so called ... double light-shielding effect can be obtained” and “thus light leak current [into the TFT] can be reduced or minimized.” Ex. 1001, 23:24-30.

Figure 16 further depicts a horizontal **scanning line** 3a with a broad-width portion at the channel area. Flasck, ¶82; Ex. 1001, 23:11,14:25-30 (describing

similar configuration in Fig. 2).³ According to the patent, this configuration may “simultaneously realize the trade-off requirements in securing the adequate channel length, that is, securing an adequate operation characteristic of the thin-film transistor and the narrowness of the scanning line, required for high precision or miniaturization of the electro-optical devices.” *Id.*, 2:57-3:2.

Independent Claim 2 recites (1) a “**data line** having a broad portion that overlaps the thin-film transistor,” (2) a “**scanning line** having a broad-width portion in a portion facing the channel area of the thin-film transistor,” and (3) a “**capacitive line**” portion with a “width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

Independent Claim 1 recites similar limitations. As set forth herein, the prior art discloses and/or renders obvious every recited feature.

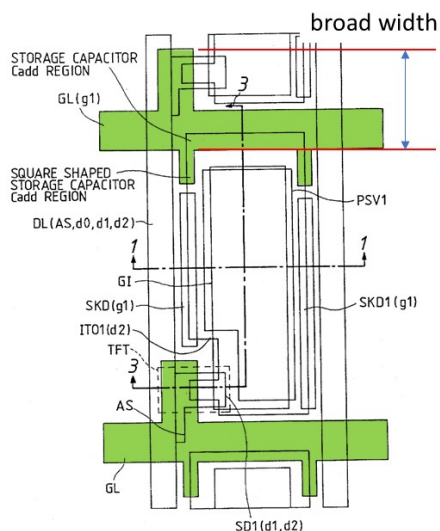
B. Prosecution History

1. Prosecution of Parent ’371 Application

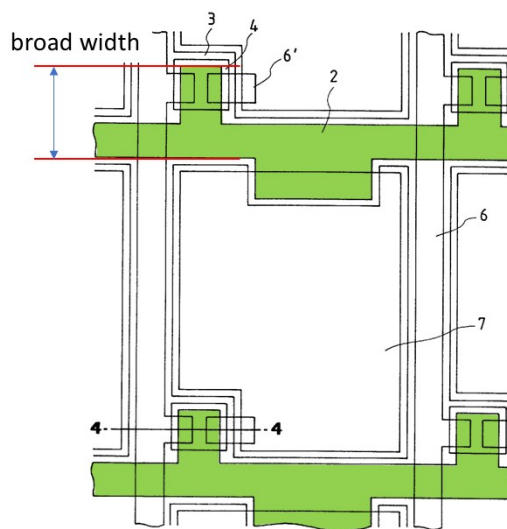
The ’079 patent is a divisional of application no. 10/320,371. Claim 1 of the ’371 application recited a “scanning line having a broad width portion as a gate

³ The ’079 patent uses “reference numerals in FIGS. 16 to 19 [to] indicate the same elements as in FIGS. 1 to 15 ... when they indicate[] substantially equivalent elements.” ’079 patent, 22:61-64.

electrode in a portion facing a channel area of the respective thin-film transistor and a narrow width portion in the other portion.” Ex. 1005 at 157.⁴ The examiner rejected the claim as obvious over *Ono* (Ex. 1013) and *Onisawa* (Ex. 1014), both of which disclosed the claimed scanning line. Ex. 1005 at 133-134.



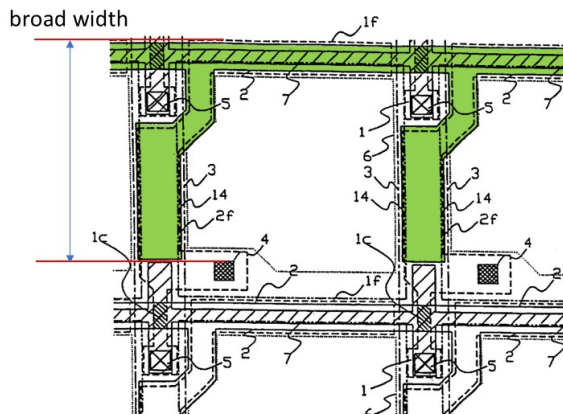
Ono, Fig. 2



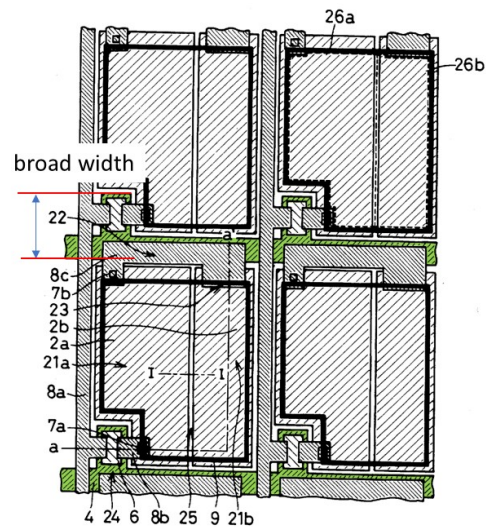
Onisawa, Fig. 3

The examiner later rejected the claims over *Murade-721* (Ex. 1015) and *Uno* (Ex. 1016), which included the same limitation, as illustrated below. Ex. 1005 at 17-19.

⁴ Citations are made to exhibit page numbers, not original page numbers, unless noted otherwise.



Murade-721, Fig. 1 (capacitive line 2 highlighted)



Uno, Fig. 1a (capacitive line 4 highlighted)

Ultimately, the examiner allowed the claims based on the location of the claimed “contact hole.” See Ex. 1005 at 11.

2. Prosecution of '589 Application

The application for the '079 patent was filed on December 1, 2005, as no. 11/290,589, a divisional of the '371 application. Ex. 1004 at 43. Application claims 1-4 were initially rejected as anticipated by *Murade-721* and *Uno*, because both included a “scanning line having a broad width portion.” Ex. 1004 at 34-35.

In response, the applicant canceled claims 1-4 and added new claims 5-7. Ex. 1004 at 27-28. The applicant did not dispute that a “broad width portion” of a scanning line was known. Instead, the applicant purported to distinguish the prior art as failing to disclose (a) “a contact hole ... positioned at a portion of the broad-width portion of the data line” as recited in claim 5 and (b) “a capacitive line [with

a] portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line” as recited in claim 6. *Id.* at 29. In a subsequent interview, the applicant focused on the latter limitation, arguing that *Murade-721* and *Uno* lack a “capacitive line having a ... portion extending along the data line having a width that is equal to or broader than a width of the data line, as recited in claims 5 and 6.” Ex. 1004 at 21. Thereafter, the examiner allowed the claims without further comment. Ex. 1004 at 13.

C. Priority Date

The '079 patent asserts priority to a Japanese patent application—JP-2002-000713—dated January 7, 2002 (“JP-713”). Challenged claims 1-3 of the '079 patent, however, are not entitled to that priority date. Each challenged claim requires a combination of several limitations that were not disclosed in JP-713. *Flasck*, ¶92. Specifically, claim 1 requires (a) a “data line having a broad-width portion that overlaps the channel area” and (b) a “capacitive line having ... a portion extending along the data line [with] a width that is equal to or broader than a width of the data line.” Similarly, claim 2 (and dependent claim 3) requires (a) a “data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor” and (b) a “capacitive line having ... a portion extending along the data line [with] a width that is

narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

JP-713 illustrates only a data line having a *uniform width*—i.e., no “broad portion” or “non-broad portion.” *See, e.g.*, Ex. 1006, Fig. 2 (element 6a), Fig. 5 (element 6a); Flasck, ¶94. Likewise, JP-713 discloses only a capacitive line that is *narrower* than the data line—i.e., not “equal to or broader than a width of the data line” or “wider than the non-broad portion of the data line.” Flasck, ¶94. The accompanying text describes no configuration that would support the features later claimed in the ’079 patent. Flasck, ¶94.

Furthermore, any written description support that the ’079 patent might arguably provide for the claimed features is limited to the “third exemplary embodiment.” Ex. 1001, 22:48-24:15, Figs. 16-19. JP-713, in contrast, includes only Figures 1-10, which correspond to ’079 patent Figs. 1-7 and 20-22.

For the foregoing reasons, the earliest date to which the ’079 patent may arguably claim priority is no earlier than December 16, 2002 (through JP-2002-363864) or December 17, 2002 (through U.S. application no. 10/320,371).

D. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*,

868 F.3d 1014, 1017 (Fed. Cir. 2017). Other than the potential terms identified below, no other terms need construction because the claims read on the asserted art under any construction consistent with *Phillips*. See Flasck, ¶100.

Claim 1 of the '079 patent recites a “data line having a *broad-width portion*” and a “scanning line having a *broad-width portion*.” Claim 2 recites a “data line having a *broad portion*” and a “scanning line having a *broad-width portion*.” Under their plain meaning, the terms “broad-width portion” and “broad portion” are terms of relative size, connoting that the portion is broader than another portion of the subject element. Flasck, ¶101. The '079 patent confirms this interpretation by offering a lexicographic definition of the term “broad width”:

Further, in the present invention, “broad width” means that it is broader than the width of the “narrow width portion,” and “narrow width” means that it is narrower than the width of the “broad width portion”. In short, the broad and narrow degree of “the broad width portion” and the “narrow width portion” is determined in accordance with the relative relationship between them.

Ex. 1001, 3:17-23. Thus, lexicography in the patent is consistent with and confirms the ordinary meaning of “broad width portion” and “broad portion” as *a portion that is broader than another portion of the subject element*. Flasck, ¶103; see *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996) (“[A] patentee is free to be his own lexicographer.”).

IV. STATEMENT OF PRECISE RELIEF REQUESTED

A. Prior Art

Ex. 1008	JP-2002-090721A to Kurashina (“ <i>Kurashina</i> ”)
Ex. 1009	U.S. Pub. No. 2002/0014627A1 to Sato (“ <i>Sato</i> ”)
Ex. 1010	JP-2002-158360A to Takahara (“ <i>Takahara</i> ”)
Ex. 1011	U.S. Pub. No. 2001/0048109A1 to Murade (“ <i>Murade-109</i> ”)
Ex. 1012	JP-2001-331125A to Murade (“ <i>Murade-125</i> ”)

1. *Kurashina* (Ex. 1008)

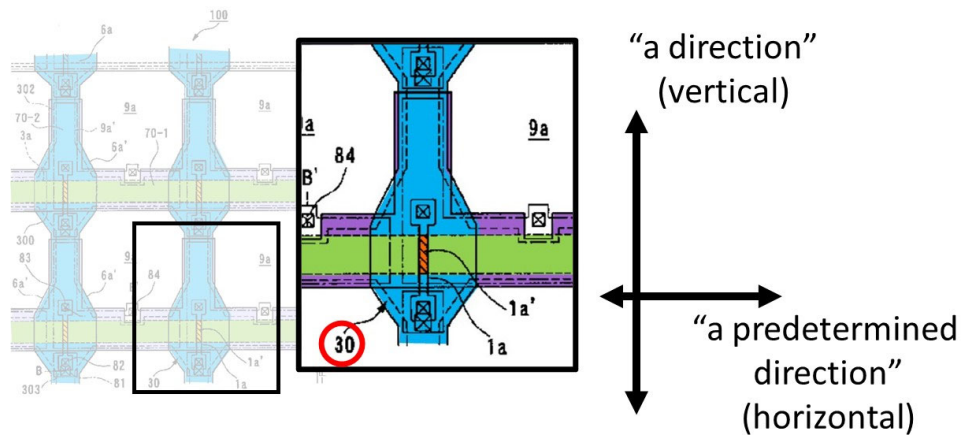
Kurashina published on March 27, 2002, before the earliest date to which the challenged claims may potentially be entitled to priority—i.e., December 16, 2002. Accordingly, *Kurashina* is prior art under at least 35 U.S.C. § 102(a).⁵

Kurashina discloses that “**data lines** 6a and **scan lines** 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a.”

Kurashina, ¶[0054], Fig. 3 (below). “The **data lines** 6a extend linearly but have

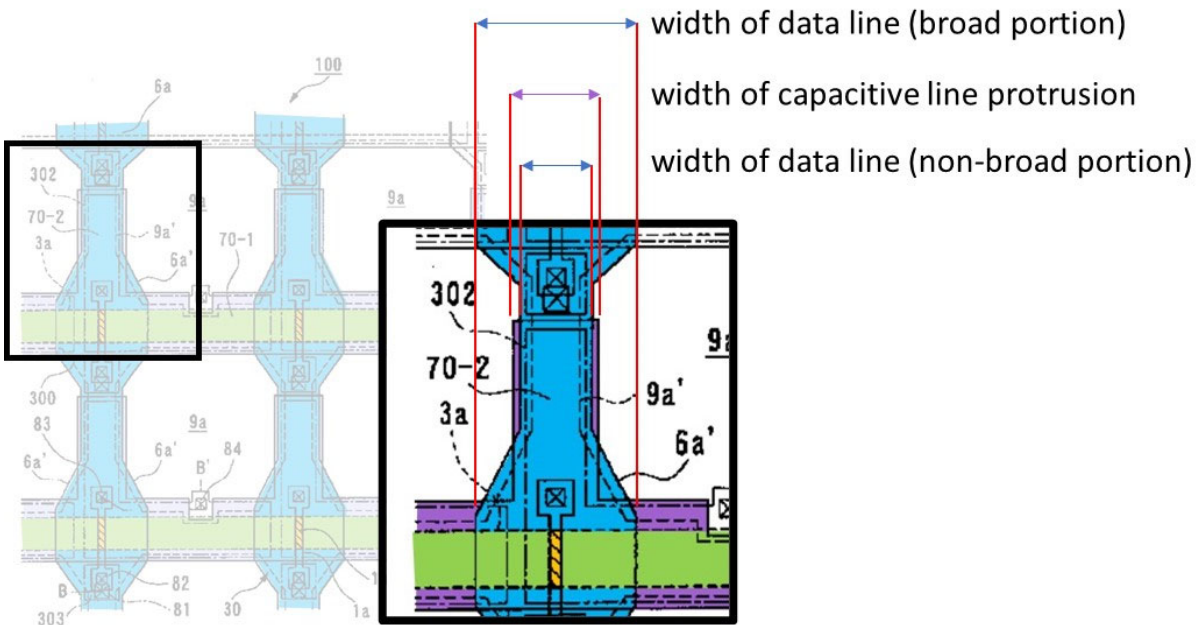
⁵ The application for the ’079 patent was filed on December 1, 2005, and thus is subject to the pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

wide-width portions 6a' protruding in the direction of the **scan lines** 3a (i.e., the left-right direction in the paper plane as seen in plan view) at portions intersecting the scan lines 3a." *Id.*, ¶[0055].



Kurashina, Fig. 3

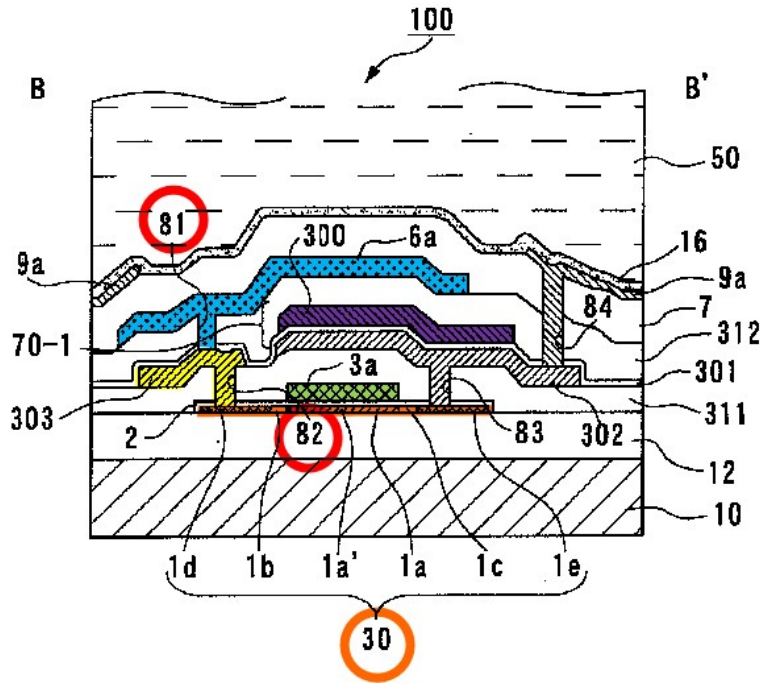
Kurashina's **capacitance line** 300 has a vertical projection that is both *narrower* than the broad portion of the **data line** and *wider* than the non-broad portion of the **data line**, as illustrated below.



Kurashina, Fig. 3

Flasck, ¶107.

Kurashina further illustrates **contact holes** 81, 82 positioned beneath a broad-width portion of the **data line** (6a) that extends from the TFT **channel area** (30) toward the **contact holes**. Flasck, ¶108.



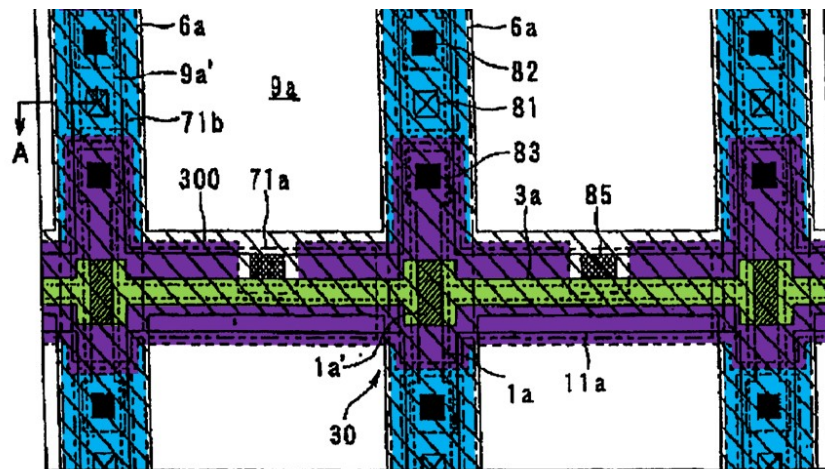
Kurashina, Fig. 4

Kurashina was assigned on its face to Seiko Epson Corporation (“Seiko Epson”), the same assignee on the face of the ’079 patent. *See Kurashina*, Cover. As shown above, *Kurashina* discloses the very features that the applicant relied on to secure allowance of the claims—i.e., a “capacitive line having a ... portion extending along the data line having a width that is equal to or broader than a width of the data line, as recited in [the] claims” and a “contact hole electrically connecting the data line and the thin-film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.” Ex. 1004 at 21, 29. The applicant, however, never submitted

Kurashina during prosecution, and the reference does not appear on the face of the '079 patent. Ex. 1001, Cover.

2. *Sato* (Ex. 1009)

Sato published on February 7, 2002, before the earliest date to which the challenged claims may potentially be entitled to priority—i.e., December 16, 2002. Accordingly, *Sato* is prior art under at least 35 U.S.C. § 102(a). *Sato* discloses “scanning lines 3a [that] are widened at portions where they act as the gate electrodes,” as illustrated below. *Sato*, ¶[0091], Fig. 2.



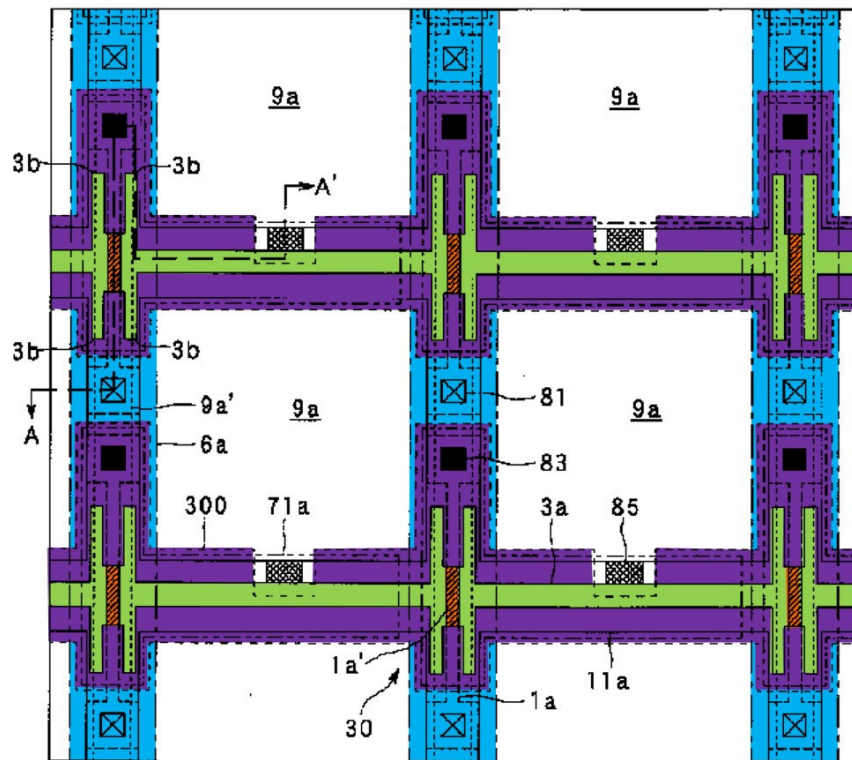
Sato, Fig. 2

Despite being assigned to Seiko Epson, *Sato* was never submitted during prosecution. Ex. 1001, Cover.

3. *Takahara* (Ex. 1010)

Takahara published on May 31, 2002, before the earliest date to which the challenged claims may potentially be entitled to priority—i.e., December 16, 2002.

Accordingly, *Takahara* is prior art under at least 35 U.S.C. § 102(a). *Takahara* discloses “**protruding portions 3b**” of a **scan line 3a**, overlapped by a **data line 6a** as illustrated below. *Takahara*, ¶¶[0053], [0079].



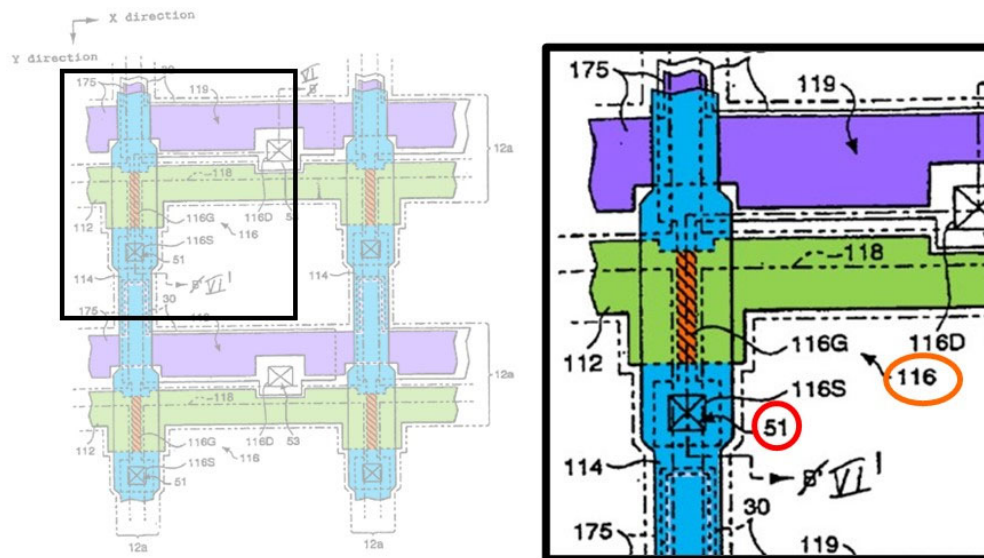
Takahara, Fig. 2

Takahara further teaches to provide **protruding portions 3b** specifically to protect the **TFT channel (1a')** against “incident light advancing obliquely toward the substrate surface of the TFT array substrate 10.” *Id.*, ¶¶[0079]-[0081].

Takahara was assigned on its face to Seiko Epson, but was never submitted during prosecution. Ex. 1001, Cover.

4. *Murade-109* (Ex. 1011)

Murade-109 published on December 6, 2001, more than one year before the earliest date to which the challenged claims may potentially be entitled to priority—i.e., December 16, 2002. Further, *Murade-109* published more than one year before the first U.S. filing date to which the '079 patent claims priority. Thus, *Murade-109* is prior art under at least 35 U.S.C. §§ 102(a) and 102(b). *Murade-109* discloses “principal elements, such as the **data line** 114, the **scanning line** 112, the **capacitor line** 175, and the **TFT** 116,” as illustrated below. *Murade-109*, ¶[0135]; Flasck, ¶111.



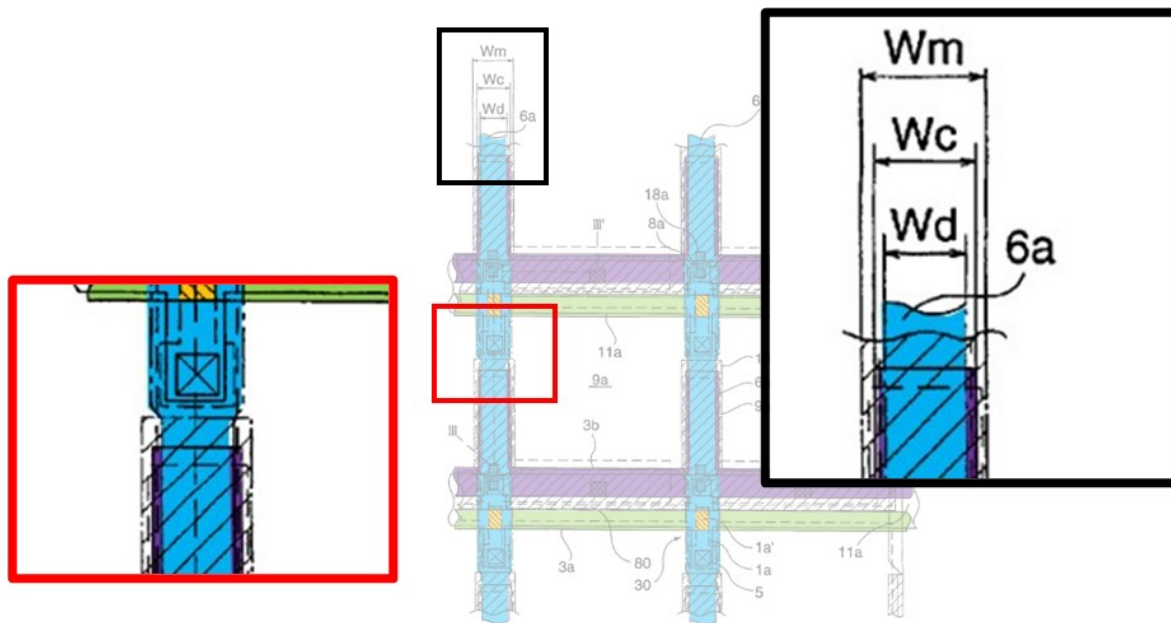
Murade-109, Fig. 5

Murade-109 further illustrates a **contact hole** (51) positioned beneath a broad-width portion of the **data line** (114) that extends from the **channel area** (116, **gate portion** 116G highlighted) toward the **contact hole**. Flasck, ¶111.

Murade-109 was assigned on its face to Seiko Epson and discloses the very feature (appearing in issued claims 1 and 3) that the applicant argued distinguished its claims over the prior art—i.e., a “contact hole electrically connecting the data line and the thin-film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.” Ex. 1004 at 29. *Murade-109*, however, was never submitted during prosecution. Ex. 1001, Cover.

5. *Murade-125* (Ex. 1012)

Murade-125 published on November 30, 2001, more than one year before the earliest date to which the challenged claims may potentially be entitled to priority—i.e., December 16, 2002. Further, *Murade-125* published more than one year before the first U.S. filing date to which the '079 patent claims priority. Thus, *Murade-125* is prior art under at least 35 U.S.C. §§ 102(a) and 102(b). *Murade-125* discloses providing a portion of a **capacitor line** that extends along the **data line**, such that the width (W_c) of the **capacitor line** portion is broader than a non-broad portion of the **data line** (width W_d), as illustrated below.



Murade-125, Fig. 2

As shown above, *Murade-125* discloses the very feature that the applicant argued distinguished its claims over the prior art—i.e., a “capacitive line having a ... portion extending along the data line having a width that is equal to or broader than a width of the data line, as recited in [the] claims.” Ex. 1004 at 21. The applicant *did* submit *Murade-125* during prosecution, and the reference appears on the face of the ’079 patent. Ex. 1001, Cover. The *Murade-125* reference, however, was submitted only in the Japanese language with no English-language abstract or translation. Ex. 1004 at 113. The applicant did not address how its patentability arguments contradicted *Murade-125*, and there is no record demonstrating how (if at all) the examiner considered *Murade-125* in connection with the applicant’s patentability arguments.

B. Grounds of Unpatentability

Claims 1-3 of the '079 patent are challenged in this Petition as unpatentable in view of the following grounds:

Ground	Claims	Statutory Basis	Prior Art
1	1-3	35 U.S.C. § 103	<i>Kurashina</i> (Ex. 1008) in view of <i>Sato</i> (Ex. 1009)
2	1-3	35 U.S.C. § 103	<i>Kurashina</i> (Ex. 1008) in view of <i>Takahara</i> (Ex. 1010)
3	1-3	35 U.S.C. § 103	<i>Murade-109</i> (Ex. 1011) in view of <i>Murade-125</i> (Ex. 1012)

V. LEVEL OF ORDINARY SKILL

A skilled artisan would have had at least a bachelor's degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. *Flasck*, ¶97. Additional education could substitute for professional experience and vice versa. *Id.* For example, a master's degree in electrical engineering, computer science, physics, or a similar field can be a substitute for two years of experience designing semiconductor display devices. *Id.*

VI. CLAIMS 1-3 ARE UNPATENTABLE OVER THE PRIOR ART

The Grounds below present independent Claim 2 before Claims 1 and 3, because Claims 1 and 3 generally include the same elements as Claim 2 but add a “contact hole” feature.

A. Ground 1: Claims 1-3 Are Obvious Over *Kurashina* in View of *Sato*

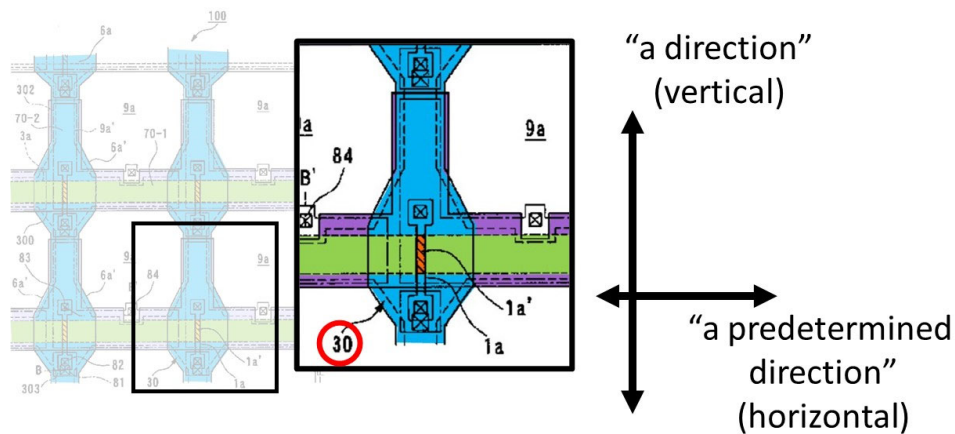
1. Independent Claim 2

a. 2[pre] An electro-optical device, comprising:

Kurashina discloses 2[pre]. *Kurashina* discloses “electro-optical devices” having “increased light-shielding performance in the corner portions of pixel electrodes.” *Kurashina*, ¶¶[0001]; Flasck, ¶120.

b. 2[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

Kurashina discloses 2[a]. *Kurashina* discloses a “pixel-switching TFT [thin-film transistor] 30” having a “channel region 1a’.” See *Kurashina*, ¶¶[0031]-[0032] (describing Figure 1), [0053] (“component members having the same functions as in FIG. 1 and FIG. 2 are indicated by the same symbols in FIG. 3 and FIG. 4”), ¶[0054] (identifying “TFT 30” in Figure 3).

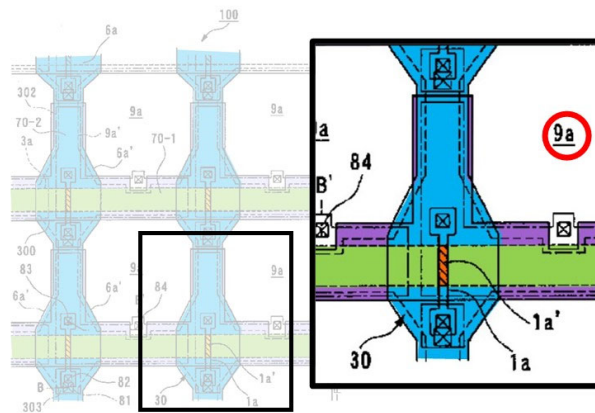


Kurashina, Fig. 3

As illustrated, the channel area extends in a direction (vertical) and intersects a predetermined direction (horizontal) that intersects the direction. Flasck, ¶¶121-122.

c. 2[b] a pixel electrode formed correspondingly to the thin-film transistor;

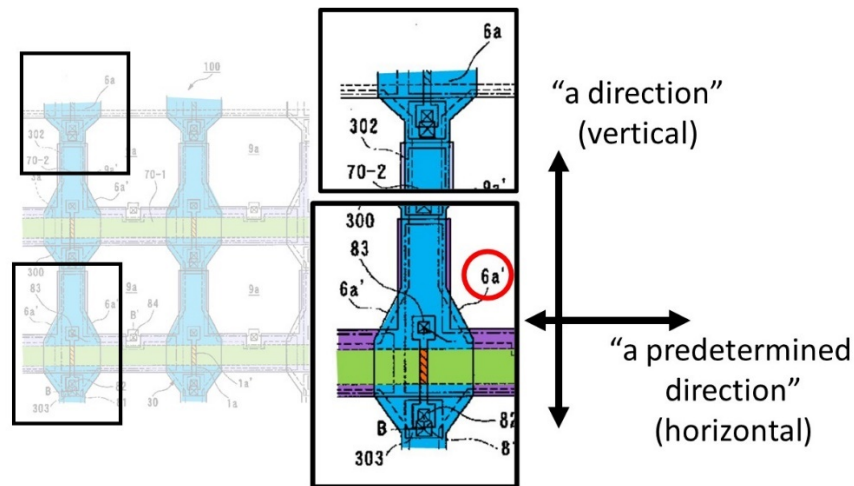
Kurashina discloses 2[b]. *Kurashina* discloses a “plurality of transparent **pixel electrodes** 9a ... provided in a matrix shape in a pixel portion on the TFT array substrate,” as illustrated below. *Kurashina*, ¶[0054]. Further, the pixel electrode is formed correspondingly to the thin-film transistor, as claimed, because “[the] pixel-switching TFT 30, which is for performing switching control of the *corresponding pixel electrode* 9a, is provided in a corner portion of *each of the pixel electrodes* 9a along the corresponding data line 6a.” *Id.* (emphasis added); Flasck, ¶124.



Kurashina, Fig. 3

- d. **2[c] a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, the broad portion being wider than the non-broad portion;**

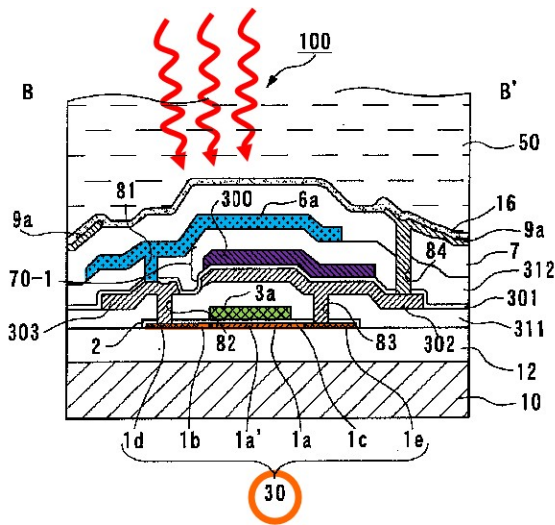
Kurashina discloses 2[c]. *Kurashina* discloses that “**data lines** 6a and the **scan lines** 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a.” *Kurashina*, ¶[0054]. As illustrated below, the data line extends vertically—i.e., “in the direction in which the channel area extends.” *Flasck*, ¶125. According to *Kurashina*, “[t]he **data lines** 6a extend linearly but have **wide-width portions** 6a’ ... at portions intersecting the scan lines 3a.” *Id.*, ¶[0055]. The “wide portions” (6a’) are a “broad portion,” as claimed. *Flasck*, ¶125.



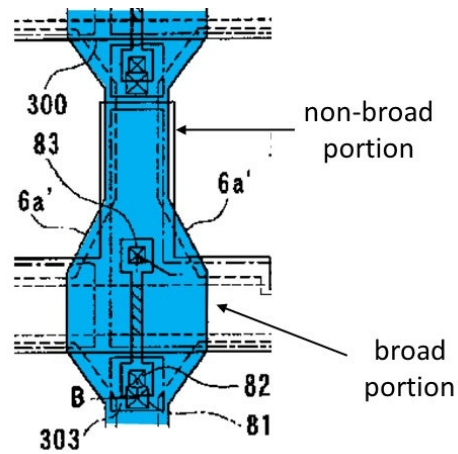
Kurashina, Fig. 3

Kurashina further describes that the broad portions “block light advancing from the liquid-crystal layer 50 side (the direction perpendicular to the paper plane) of the TFT array substrate 10 in each pixel portion.” *Kurashina*, ¶[0055].

This means that, as illustrated in the cross-sectional view of Figure 4 (below, left), the broad portion of the **data line** “overlaps the **thin-film transistor**” (30), as claimed, such that the data line blocks light (**red arrows**, added below) from reaching the TFT and channel area. *Flasck*, ¶126.



Kurashina, Fig. 4



Kurashina, Fig. 3

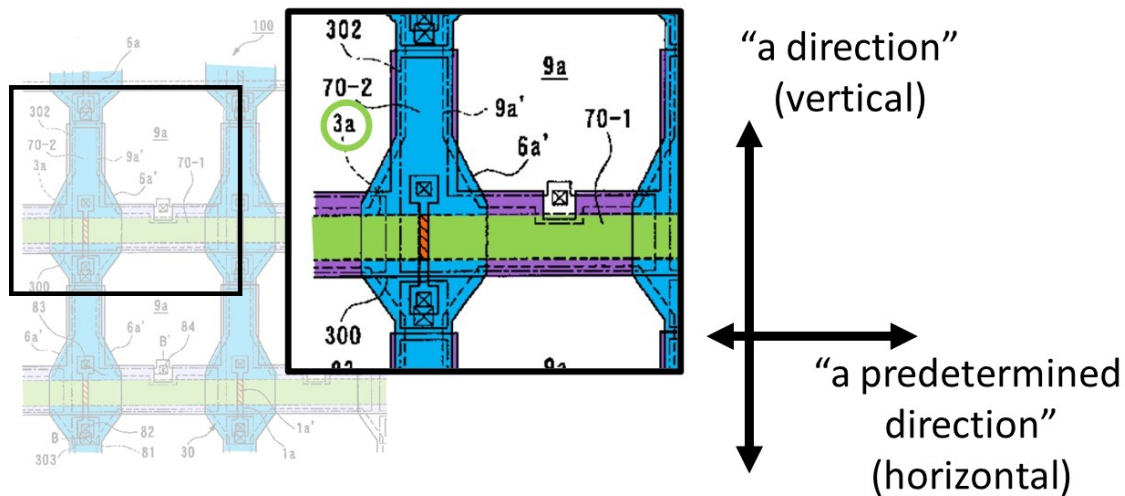
As illustrated in Figure 3, above-right, the portion of *Kurashina*'s data line that is *not* wide/broad and does not overlap the transistor is a "non-broad portion that does not overlap the thin-film transistor." See *Kurashina*, Fig. 3; Flasck, ¶127. The broad portion of *Kurashina*'s **data line** (6a') is wider than the non-broad portion. Flasck, ¶127. Thus, *Kurashina* provides every feature of element 2[c]. Flasck, ¶127.

- e. **2[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;**

It would have been obvious over *Kurashina* in view of *Sato* to provide 2[d].

Kurashina discloses that "**data lines** 6a and the **scan lines** 3a are provided along the vertical and horizontal boundaries, respectively, of the pixel electrodes 9a."

Kurashina, ¶[0054]. As illustrated below, the scan line extends horizontally—i.e., “in the predetermined direction”—and intersects the **data line** and the **channel area of the thin film transistor**, as claimed. Flasck, ¶129.



Kurashina, Fig. 3

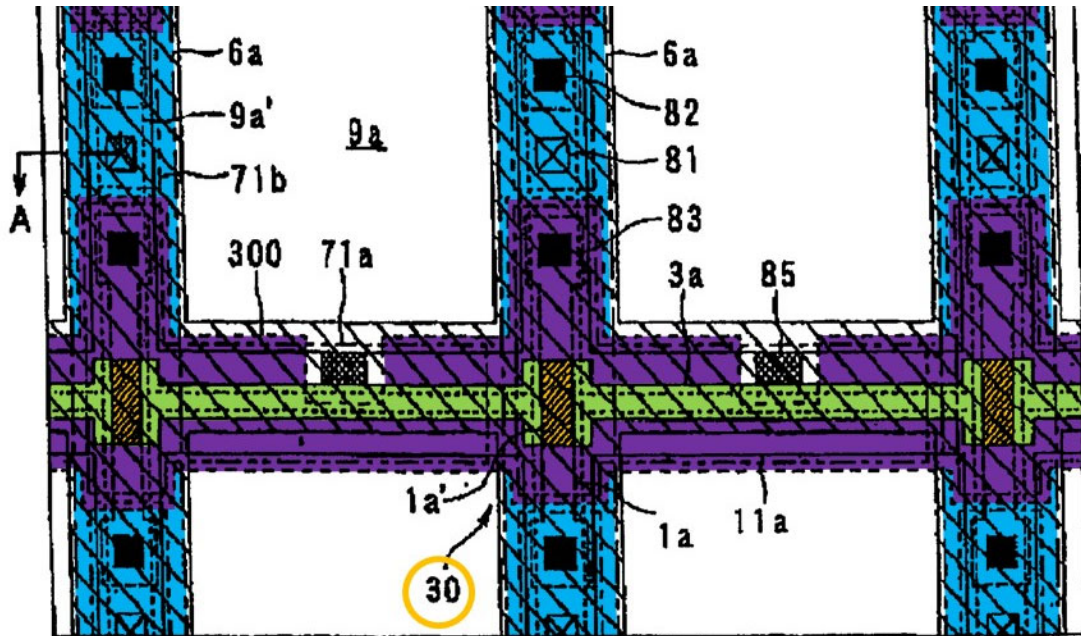
Kurashina does not describe providing the **scan line** with a broad-width portion. Nonetheless, that feature would have been obvious in view of *Sato*. Flasck, ¶130.

Like *Kurashina* (and the '079 patent), *Sato* “relates to the technical field of an electro-optical device of an active matrix drive system, and more particularly, ... a type having pixel switching thin film transistors.” *Sato*, ¶[0002]; Flasck, ¶132. Also, like *Kurashina*, *Sato* addresses the art-recognized need to shield the TFT channel area from incident light—a need that became particularly acute “since electro-optical devices are miniaturized and the pixel pitches thereof are greatly

narrowed to cope with a recent requirement for enhancing the quality of a displayed image.” *Id.*, ¶[0007]; Flasck, ¶133. *Sato* and *Kurashina* further share the concern that any design improvement not unduly reduce the size of the pixel aperture, which, as Mr. Flasck explains, indicates to a POSITA that “the design goals of both references are compatible.” Flasck, ¶133; *compare Sato*, ¶¶[0008]-[0009] (purporting to address problem that light shielding makes it “fundamentally difficult to increase the opening ratio of each pixel”) *with Kurashina*, ¶¶[0019]-[0020] (selective widening “in the vicinity of the transistor ... to shield a corner portion of the pixel electrode” makes it “possible to block light” while making the pixel opening only “somewhat narrower”).

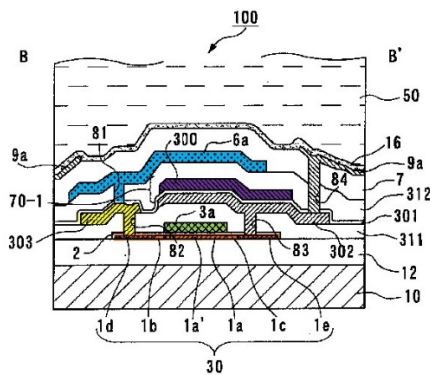
Sato’s design includes the same general structures as *Kurashina*, including a **data line** (6a) and **scanning line** (3a) intersecting to form the channel of a **TFT** (30, including **channel region** 1a’), as illustrated below. *Sato*, ¶¶[0090]-[0091] (“pixel switching TFTs 30, each of which has a scanning line 3a as a gate electrode in each channel region a’ ... disposed at the positions where the scanning lines 3a intersect the data lines 6a”); Flasck, ¶134. A **capacitance line** 300 is also provided, with portions projecting along the **data line** in a manner similar to *Kurashina*. *Sato*, ¶[0094] (“capacitance line 300 extends along each scanning line 3a in a striped shape, and the portion thereof overlapping a TFT 30 projects upward and

downward [vertically] in FIG. 2”); Flasck, ¶134; *see also* Section VI.A.1.g *infra* (discussing configuration of *Kurashina*’s **capacitor line** and protruding portions).

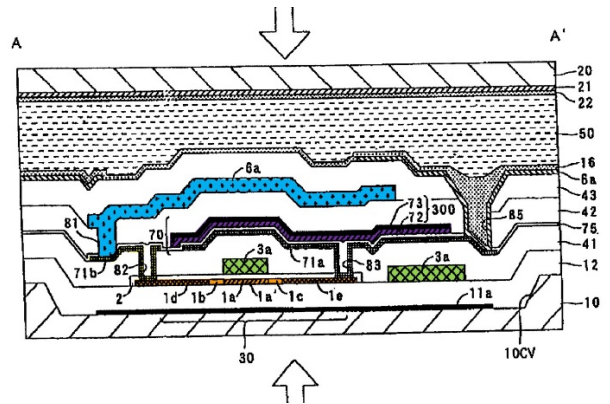


Sato, Fig. 2

Sato and *Kurashina* also layer their **data line** (6a), **scanning line** (3a), **TFT**, and **capacitor line** (300) in a similar fashion, as illustrated below. Flasck, ¶135.

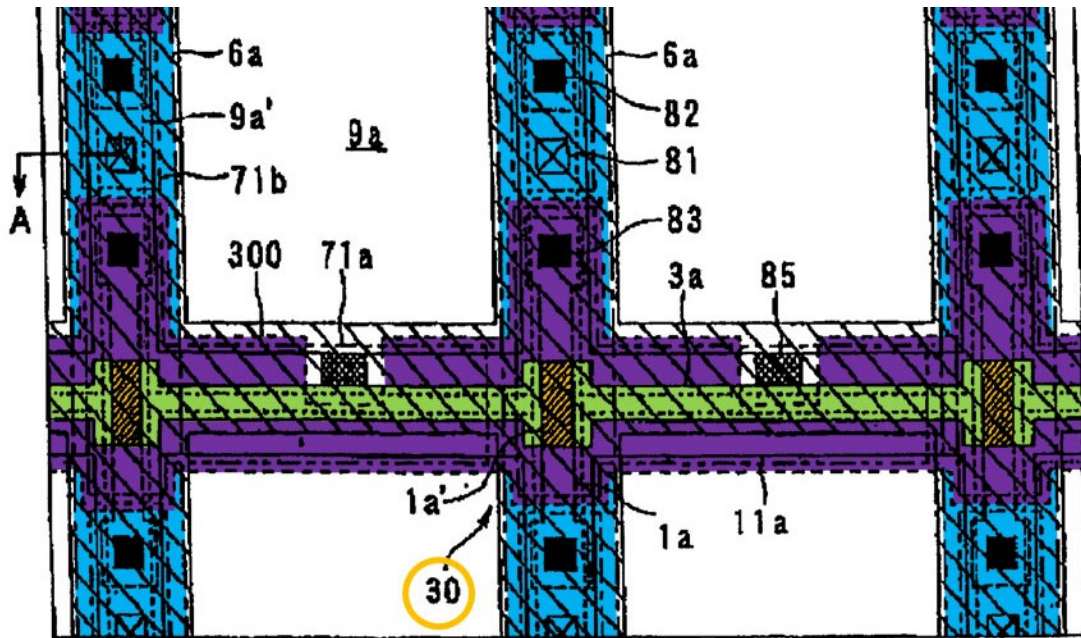


Kurashina, Fig. 4



Sato, Fig. 3

Sato further discloses that “the **scanning lines** 3a are widened at portions where they act as the gate electrodes,” as illustrated below. *Sato*, ¶[0091]. Thus, like the prior art references discussed during prosecution, “*Sato* reflects the art’s understanding that a scanning line must have a certain minimum dimensions at the gate area, even if other portions of the scanning line are narrowed.” Flasck, ¶136. *Sato*’s **scanning line** thus has a “broad-width portion in a portion facing the channel area of the thin-film transistor,” while the remainder of the scanning line is “a narrow width portion in another portion,” as claimed. Flasck, ¶136.



Sato, Fig. 2

Kurashina and *Sato* are each analogous art to the '079 patent, at least because each “is from the same field of endeavor,” namely active-matrix drive electro-optical devices such as for LCD displays. *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1000–01 (Fed. Cir. 2016) (citation omitted); Flasck, ¶137; compare *Kurashina*, ¶[0054] with *Sato*, ¶[0004] and '079 patent, Abstract. Moreover, *Kurashina* and *Sato* both are directed to solving the same or related problems of light leakage that may negatively impact TFT channel performance. Flasck, ¶138; compare *Kurashina*, ¶[0052] (portions of data line “formed with a wide width in the vicinities of the TFTs 30 ... and made to serve as light-shielding layers against the incidence of light from the corner portions of the pixel electrodes 9a”) and [0055] (data lines “block light” from reaching TFT) with *Sato*,

¶[0116] (“As a result” of using the data line and capacitance line to block light, “the characteristics of the TFT 30 are hardly deteriorated by light leakage, and a very high light resistant property can be obtained”) *and* ’079 patent, 23:29-30 (“thus the light leak current can be reduced or minimized”). As Mr. Flasck explains, “it was well-known at the relevant time that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel.” Flasck, ¶138. “A POSITA would thus consider references such as *Sato* to be pertinent when implementing an active-matrix drive system such as *Kurashina*.” Flasck, ¶138.

It would have been obvious and straightforward to implement *Kurashina*’s design with *Sato*’s narrow scanning line having a widened gate portion. Flasck, ¶139. *Sato* teaches that its device “is very advantageous by simply arranging the electro-optical device, and simplifies a manufacturing process thereof.” *Sato*, ¶¶[0026], [0028]; Flasck, ¶139. Moreover, “simply changing the patterning shape when the capacitor lines and the data lines are formed”—to implement *Sato* with *Kurashina*—would be a relatively straightforward modification and “has the advantage of making formation possible even without providing any special process.” *Kurashina*, ¶[0022]; Flasck, ¶139. Further, a POSITA would recognize that the benefits of *Sato*’s narrow scanning line with a wide gate would be “additive to the design of *Kurashina*,” because the combination would result in

improved pixel pitch and aperture ratio, which would improve image quality.

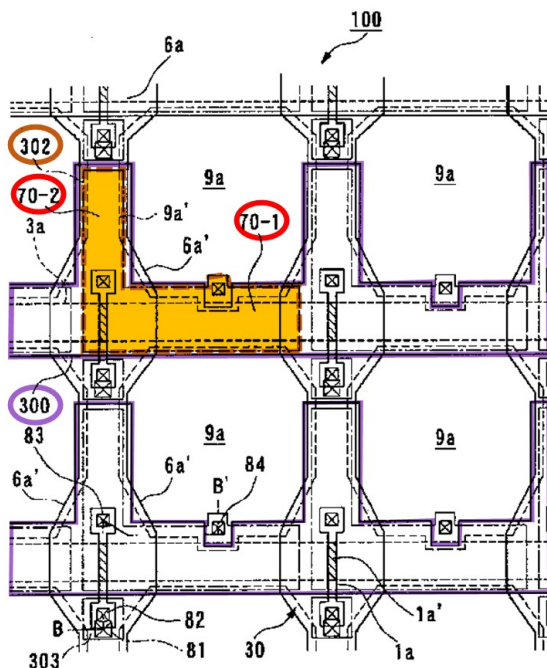
Flasck, ¶139. The combination would yield a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion. Flasck, ¶139.

As Mr. Flasck further explains, “combining the teachings of *Kurashina* and *Sato* would have required no more than ordinary skill because the combination would have been a simple modification of . . . an already existing component, in a straightforward manner to achieve predictable results.” Flasck, ¶140 (further explaining that the combination “would have had a reasonable expectation of success given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Sato* could be integrated into *Kurashina*’s device”). At bottom, both *Kurashina* and *Sato* disclose devices using TFT for active matrix-drive control, and modifying *Kurashina*’s scanning line according to *Sato*’s teachings would be a straightforward and predictable improvement to *Kurashina*’s device. Flasck, ¶140.

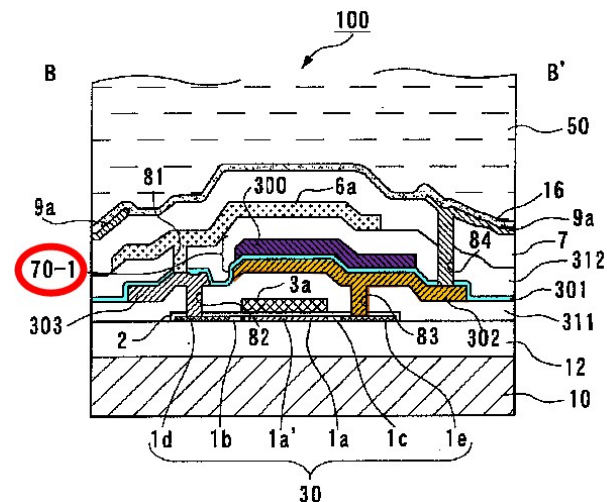
Thus, *Kurashina* and *Sato* render obvious claim element 2[d]. Flasck, ¶141.

- f. 2[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and;

Kurashina discloses 2[e]. In Figures 3-4, *Kurashina* discloses “**storage capacitors**” (70-1 and 70-2) that ensure capacitance and “stabilize the display screen.” *Kurashina*, ¶[0059]. According to *Kurashina*, “the **capacitor lines** 300, together with the L-shaped **drain electrode** 302 [illustrated in plan view below at left],” together with “interposed **insulating films**” (301) “form **storage capacitors** 70-1.” *Kurashina*, ¶[0058].



Kurashina, Fig. 3



Kurashina, Fig. 4

As Mr. Flasck explains, a storage capacitor (e.g., 70-1, 70-2 of *Kurashina*) is defined by two conductors (or electrodes) separated by an insulator (or dielectric)

such that a fixed voltage potential difference is created between them. Flasck, ¶143 (citing Ex. 1025 at 4; Ex. 1029 at 3).

In *Kurashina*, the **drain electrode** 302 represents the potential of the pixel because the pixel 9a connects to **drain electrode** 302 via contact hole 84.

Kurashina, ¶[0032] (describing FIG. 2), ¶[0060] (“FIG. 3 ... structure is exactly the same” as in FIG. 2); Flasck, ¶144; *accord Sato* ¶[0093] (“pixel potential side capacitance electrode” is formed by connection between “heavily doped drain region 1e of the TFT 30 (and the pixel electrode 9a)”). That is, the **drain electrode** 302 forms the first electrode of the storage capacitor and is a “pixel-potential capacitor electrode,” as claimed. Flasck, ¶144.

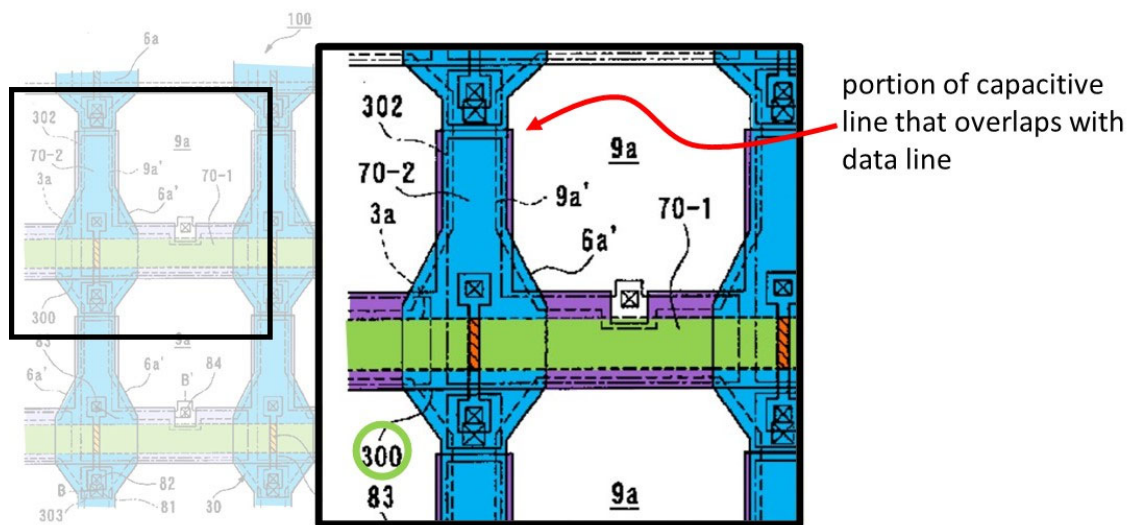
To create a storage capacitor as *Kurashina* discloses, the **capacitor line** 300 supplies a fixed-voltage potential, meaning that the **capacitor line** 300 forms a “fixed-potential capacitor electrode.” *Kurashina*, ¶[0034]; Flasck, ¶145. As Mr. Flasck notes, a POSITA would “generally understand a **capacitor line** to have a fixed potential, given its connection to a constant potential source.” Flasck, ¶145; *citing Sato*, ¶[0093] (“part of the capacitance line 300 ... acts as the fixed potential side capacitance electrode”) and *Takahara*, ¶[0063] (“capacitor line 300 ... is electrically connected to a constant-potential source, and has a fixed potential”; “constant potential source may be ... a positive power supply or a negative power supply supplied to a scan-line drive circuit”). Indeed, “a later embodiment of

Kurashina confirms and illustrates the role of the capacitance line as a fixed-potential capacitor electrode, where by example ‘capacitor electrode 403b having a fixed potential is provided overlapping the scan line 3a, and one end of the capacitor electrode 403b is connected to the capacitor line 404a.’” Flasck, ¶145 (quoting *Kurashina* ¶[0067]). In that later embodiment, the capacitance electrode 403b at a fixed potential is in electrical contact with the capacitance line, and as such, the capacitance line itself is at a fixed potential. *Id.*

Finally, Mr. Flasck explains, because the **insulating film** 301 is an insulating layer that separates the two electrodes of *Kurashina*'s capacitor, allowing the buildup of an electric field between the two electrodes rather than allowing a current to pass between them, the insulating film is a “dielectric film.” Flasck, ¶146 (citing Ex. 1020 at 3); *see also Sato*, ¶[0093] (capacitor electrodes “are disposed in confrontation with each other through the dielectric film”). Accordingly, *Kurashina* provides 2[e]. Flasck, ¶146.

- g. 2[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.

Kurashina discloses 2[f]. In *Kurashina*, “**capacitor lines** 300 overlap the **scan lines** 3a and are provided in the left-right direction in the paper plane along the boundaries of the pixel electrodes 9a.” *Kurashina*, ¶[0057]. Further, the **capacitor lines** 300 have both (i) “substantially linearly extending portions overlapping the **scan lines** 3a” and (ii) “substantially linearly extending portions overlapping the **data lines** 6a.” *Id.*, ¶[0058].



Kurashina, Fig. 3

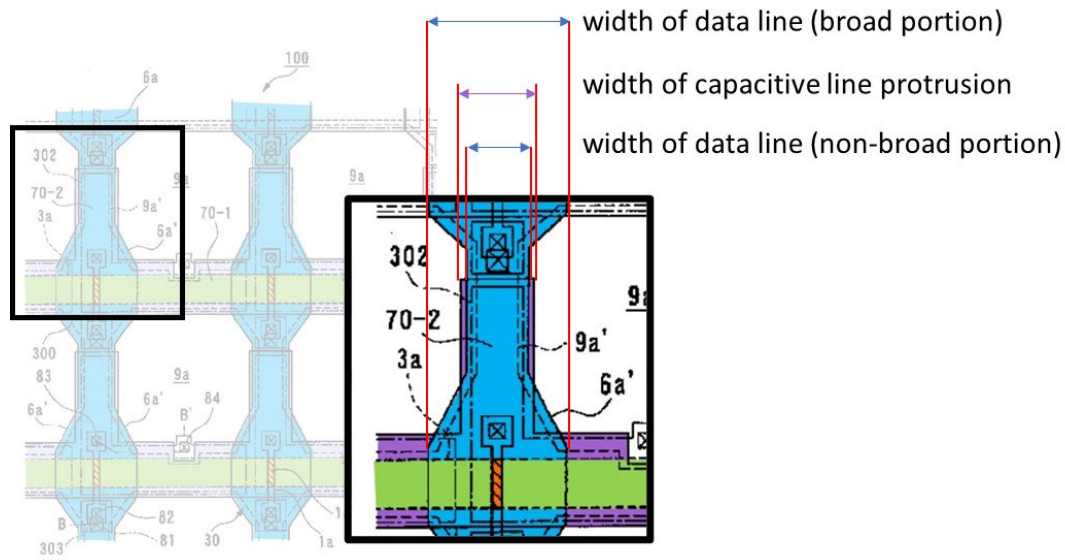
In describing the related embodiment in Figure 1, *Kurashina* refers to the horizontal portion of the **capacitor line** 300 as the “main line portions, which

extend substantially linearly along the **scan lines** 3a” and the vertical portions of the **capacitor line** 300 as the “**protruding portions**, which protrude in the up-down direction in the paper plane along the **data lines** 6a.” *Kurashina*, ¶[0033]; Flasck, ¶148.

As discussed above in connection with 2[e], the capacitive line has a portion that “serves as the fixed-potential capacitor electrode of the storage capacitor,” as claimed. *See* Section VI.A.1.f; Flasck, ¶149.

The horizontal or “main line portion” of *Kurashina*’s capacitive line is a “portion extending along the scanning line.” Flasck, ¶150.

The vertical or “protruding portion” of *Kurashina*’s capacitive line is a “portion extending along the data line.” Flasck, ¶151. Moreover, as illustrated below, the width of *Kurashina*’s protruding portion has “a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.” Flasck, ¶151.



Kurashina, Fig. 3

While prior-art drawings generally may not be assumed to depict specific dimensions, “[d]escription for the purposes of anticipation can be by drawings alone as well as by words.” *In re Mraz*, 455 F.2d 1069, 1072 (C.C.P.A. 1972). In *Mraz*, for example, the court found that a prior-art drawing disclosed claim features by “showing them with great particularity and showing the [features] to have an angularity well within the range recited in appellant’s claims.” *Id.* Thus, the Board has on several occasions found prior-art drawings to visually (even without specific verbiage) depict relative sizes recited in challenged claims. See *Micron Tech., Inc. v. Lone Star Silicon Innovations, LLC*, Institution Decision, IPR2017-01561, 2018 WL 6584977, at *14-*15 (PTAB Dec. 12, 2018) (instituting IPR based on prior art visually depicting claimed “straight sidewalls”); *Innoscence (Zhuhai) Tech. Co., Ltd. v. Efficient Power Conversion Corp.*, Institution Decision,

IPR2023-01384, 2024 WL 1283533, at *15 (PTAB Mar. 26, 2024) (instituting IPR based on prior art visually depicting claimed limitation of “substantially equal widths”); *see also Ex Parte Post*, Appeal No. 2020-005029, Decision on Appeal, 2021 WL 1265136 (PTAB Apr. 2, 2021) (affirming anticipation rejection based on prior-art drawings visually depicting claimed “the first diameter dimension being larger than the second diameter dimension”). Here, *Kurashina* shows a POSITA that the capacitive line projection is wider than a non-broad portion of the data line. Flasck, ¶152.

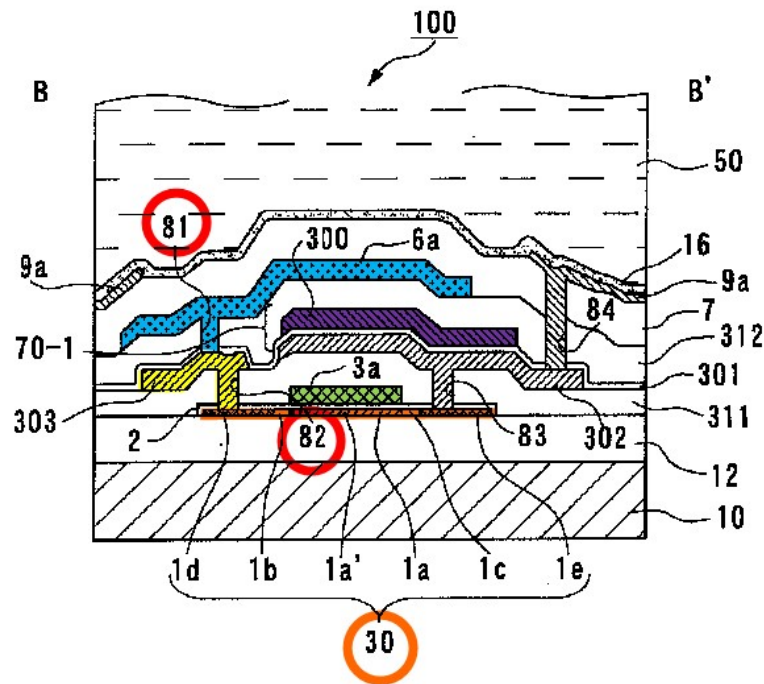
Moreover, Mr. Flasck explains, a POSITA in this field “would understand illustrated relative widths to convey general design information and demonstrate one acceptable design choice,” particularly where *Kurashina* differentiates various embodiments *specifically* based on the relative widths of components. Flasck, ¶152 (discussing *Kurashina*, ¶[0052]). Thus, a POSITA would recognize that *Kurashina* teaches 2[f]. Flasck, ¶152.

For the reasons above, *Kurashina* in view of *Sato* provide every limitation of independent claim 2 and, together, render obvious claim 2. Flasck, ¶153.

2. **Claim 3. The electro-optical device according to claim 2, further comprising a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.**

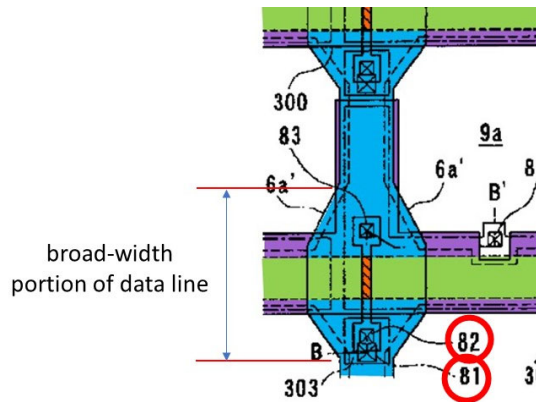
Kurashina discloses the additional features of claim 3.⁶ As discussed in Section VI.A.1, *Kurashina* in view of *Sato* provide the electro-optical device of claim 2, from which claim 3 depends. *Kurashina* discloses that “[t]he **data lines** 6a are electrically connected to the **source electrodes** 303 ... via the **contact holes** 81.” *Kurashina*, ¶[0055], Fig. 4 (below); Flasck, ¶155. Other **contact holes** (82) “electrically connect the **source electrodes** 303 and the high-density source regions 1d of the semiconductor layers 1a” of the **TFT**. *Kurashina*, ¶[0056]; Flasck, ¶155. Thus, as Mr. Flasck explains, the data line electrically connects to the TFT through contact holes 81 and 82. Flasck, ¶155.

⁶ Petitioner assumes for purposes of this proceeding that claim 3 includes an obvious typographical error, and the claim should be understood as if the word “to” were included between “transistor” and “a portion.”



Kurashina, Fig. 4

Kurashina also discloses “the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.” Flasck, ¶156. As illustrated in Figure 3 (below), the **data line** 6a is broad—i.e., “broader than the width of the ‘narrow width portion’”—throughout its entire extent from *either* **contact hole** (81,82) through the **TFT** (30), meaning the broad portion is “continuously broad.” Flasck, ¶156.



Kurashina, Fig. 3

Thus, *Kurashina* in view of *Sato* also provides every limitation of claim 3 and, together, renders obvious claim 3. *Flasck*, ¶157.

3. Independent Claim 1

a. 1[pre] An electro-optical device, comprising:

Kurashina discloses 1[pre] for the same reasons as 2[pre]. *See* Section VI.A.1.a.

b. 1[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

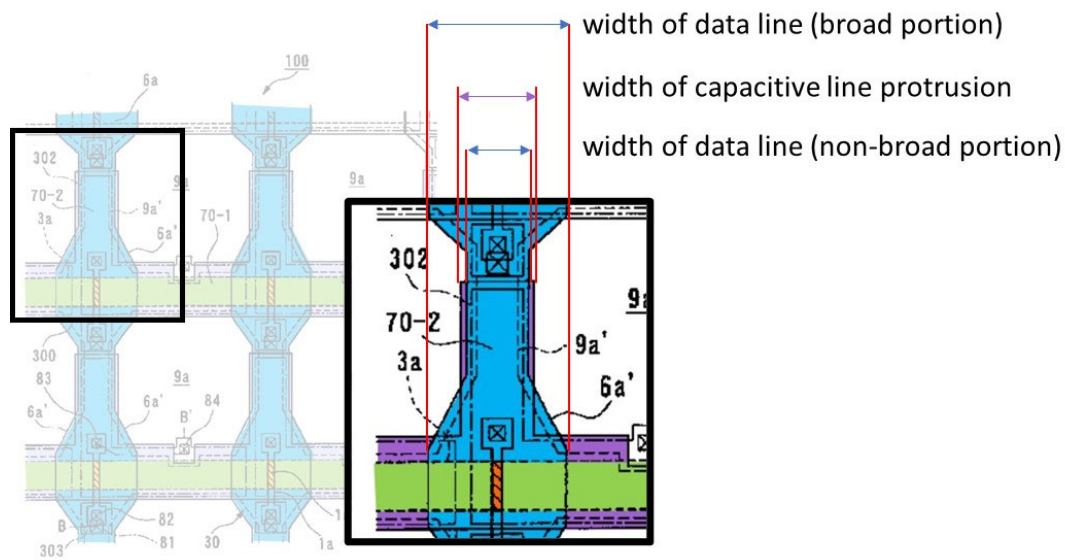
Kurashina discloses 1[a] for the same reasons as 2[a]. *See* Section VI.A.1.b.

c. 1[b] a pixel electrode formed correspondingly to the thin-film transistor;

Kurashina discloses 1[b] for the same reasons as 2[b]. *See* Section VI.A.1.c.

- d. **1[c] a data line extending in the direction in which the channel area extends, the data line having a broad-width portion that overlaps the channel area in plan view;**

Kurashina discloses 1[c] for the same reasons as it discloses 2[c]. *See* Section VI.A.1.d. By comparison, 1[c] adds that the overlap is “in plan view,” which *Kurashina* illustrates. *Flasck*, ¶161.

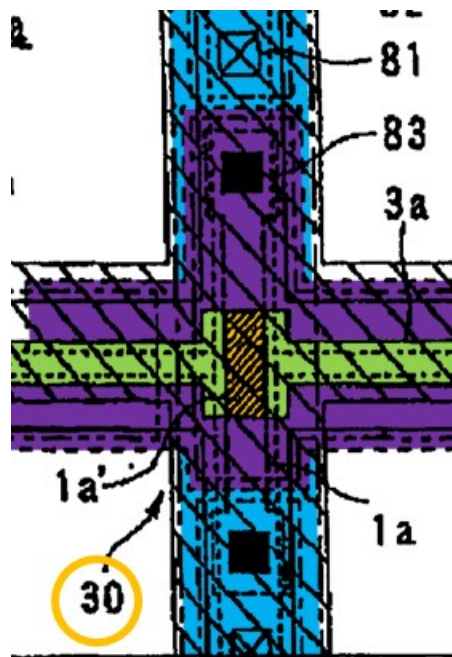


Kurashina, Fig. 3

- e. **1[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion;**

1[d] would have been obvious over *Kurashina* in view of *Sato* for the same reasons as 2[d]. *See* Section VI.A.1.e. As compared to 2[d], element 1[d] recites that (i) the scanning line has a broad-width portion in a portion “overlapping”

(instead of “facing”) the channel area and (ii) the overlap is “in plan view.” As Mr. Flasck explains, “[t]hose differences in verbiage ... make no meaningful difference with respect to the design of *Kurashina* and *Sato*, because ... (i) the broad-width portion of [*Sato*’s] scanning line is *both* ‘facing’ and ‘overlapping’ the TFT channel and (ii) [*Sato*’s] Figure 2 shows the overlap ‘in plan view,’” as illustrated below. Flasck, ¶162.



Sato, Fig. 2

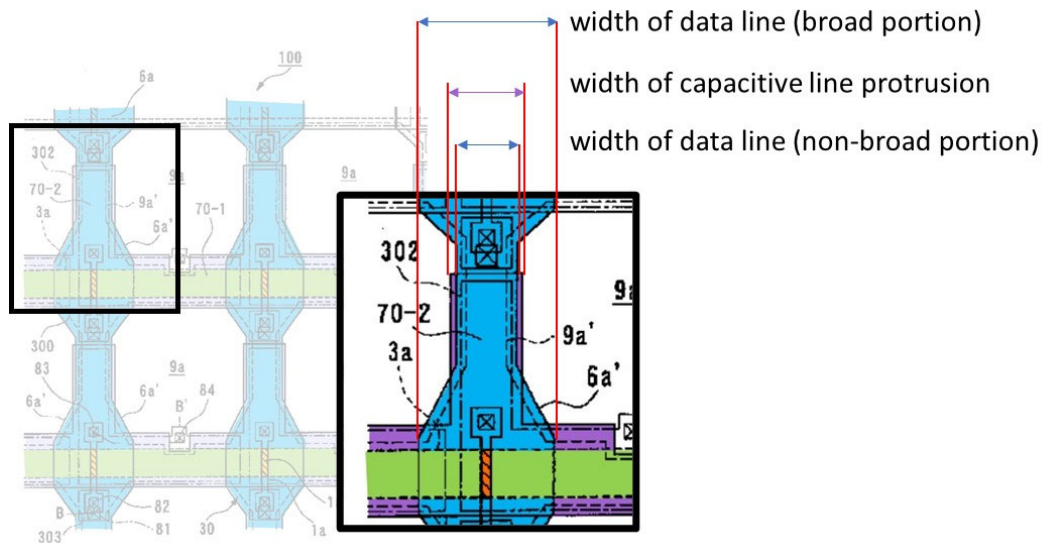
- f. **1[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed-potential capacitor electrode;**

Kurashina discloses 1[e] for the same reasons as it discloses 2[e]. See Section VI.A.1.f; Flasck, ¶164.

- g. **1[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and**

Kurashina discloses 1[f] for the same reasons as it discloses 2[f]. *See*

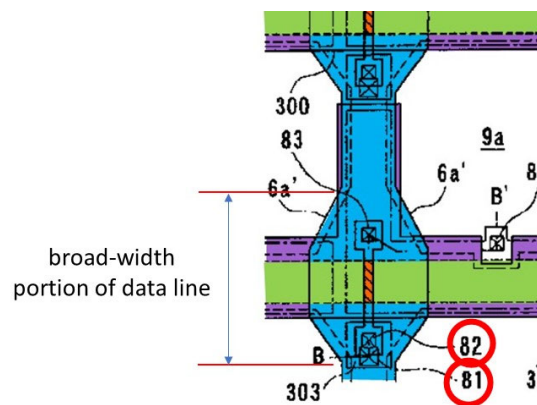
Section VI.A.1.g. As discussed in connection with 2[f] and as illustrated below, the portion of *Kurashina*'s **capacitive line** that extends along the **data line** is broader than the non-broad portion of the data line. The width of the non-broad portion of the data line is “a width of the data line”; therefore, “the portion [of the capacitive line] extending along the data line [has] a width that is equal to or broader than a width of the data line,” as claimed. *Flasck*, ¶165.



Kurashina, Fig. 3

- h. **1[g] a contact hole electrically connecting the data line and the thin film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.**

Kurashina discloses 1[g] for the same reasons as it discloses Claim 3. *See* Section VI.A.2. Mr. Flasck explains that “[s]ubstantively, 1[g] ... omits the ‘continuously broad’ limitation,” meaning that “the contact hole of 1[g] need only be positioned ‘at a portion of the broad-width portion of the data line,’ which ‘extends beyond the channel area in a direction extending from the channel area toward the contact hole.’” Flasck, ¶166. As illustrated below, a portion of the broad width portion of the **data line** 6a’ extends beyond the **channel area** in a direction (vertically down) extending from the channel area toward the contact hole. Flasck, ¶167. Further, each **contact hole** (81, 82) is positioned at the foregoing “portion of the broad-width portion of the **data line**”—either one meets the claim.



Kurashina, Fig. 3

For the reasons above, *Kurashina* in view of *Sato* provide every limitation of independent claim 1 and, together, render obvious claim 1. Flasck, ¶168.

B. Ground 2: Claims 1-3 Are Obvious Over *Kurashina* in View of *Takahara*

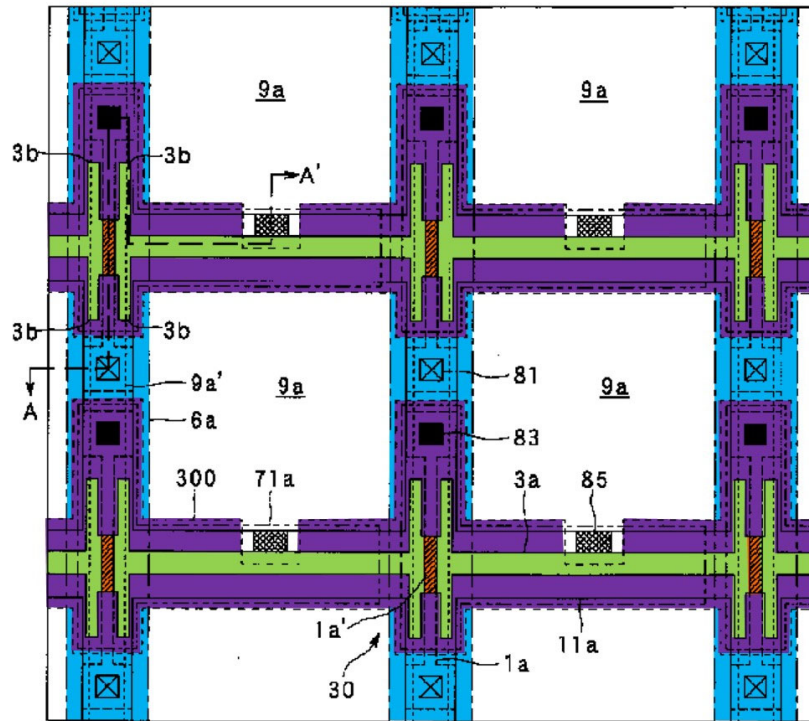
1. Independent Claim 2

As discussed above in Section VI.A.1, *Kurashina* discloses every limitation of claim 2 except, arguably, “the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion,” as required by 2[d]. *See* VI.A.1.e; Flasck, ¶169. *Takahara* provides 2[d]. Flasck, ¶169.

Like *Kurashina* (and the '079 patent), *Takahara* pertains to the “technical field of an electro-optical device ... in which a pixel-switching, thin-film transistor ... is provided.” *Takahara*, ¶[0001]; Flasck, ¶170. Also like *Kurashina*, *Takahara* addresses the art-recognized need to shield the TFT channel area from incident light—a need that became particularly acute “as higher definition or finer pixel pitch is achieved in electro-optical devices to meet the general demand for higher quality of display images particularly in recent years.” *Id.*, ¶ [0006]; Flasck, ¶171. *Takahara* and *Kurashina* further share the concern that any design improvement not unduly reduce the size of the pixel aperture, which, as Mr. Flasck explains, indicates to a POSITA that “the design goals of both references are compatible.”

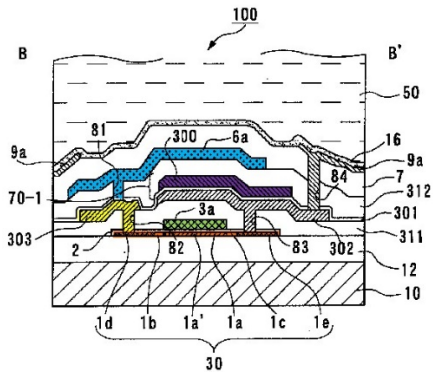
Flasck, ¶171; *compare* *Takahara*, ¶¶[0007]-[0008] (cautioning that “widened” light-shielding films make it “difficult to increase the aperture percentage of the pixels” and “increase ... internally reflected light and multiply reflected light”) *with Kurashina*, ¶¶[0019]-[0020] (selective widening “in the vicinity of the transistor ... to shield a corner portion of the pixel electrode” makes it “possible to block light” while making the pixel opening only “somewhat narrower”).

Takahara’s design includes the same general structures as *Kurashina*, including a “pixel switching TFT 30, in which the scan line 3a is disposed opposing the gate electrode in the channel region 1a' ... where the scan line 3a and the data line 6a intersect.” *Takahara*, ¶[0054]; Flasck, ¶172. A capacitor line 300 is also provided, with portions protruding along the data line as in *Kurashina*. *Takahara*, ¶[0058]; Flasck, ¶172.

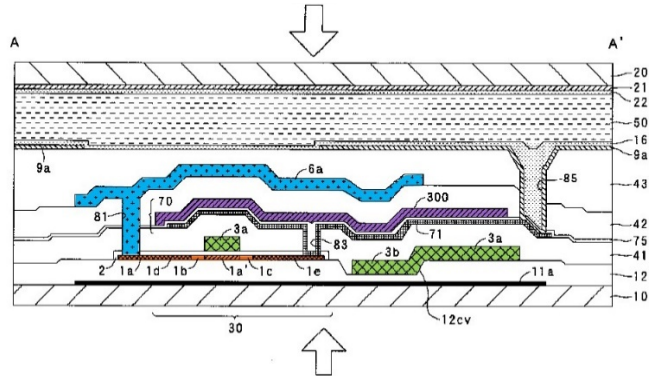


Takahara, Fig. 2

Takahara also layers its **data line**, **scanning line**, **TFT**, and **capacitor line** similarly to *Kurashina*, as illustrated below. Flasck, ¶173. The primary difference is *Kurashina*’s use of an intervening **source electrode** (303) between the **data line** and **TFT**. Flasck, ¶173. According to Mr. Flasck, however, that difference is not “an obstacle” to “combining the teachings of the two references.” *Id.*

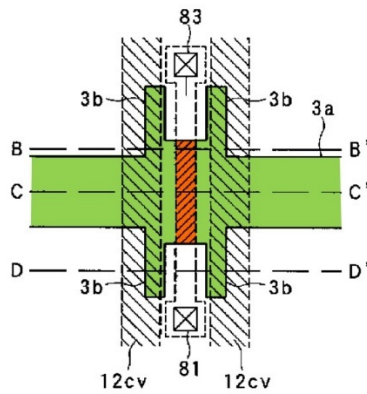


Kurashina, Fig. 4

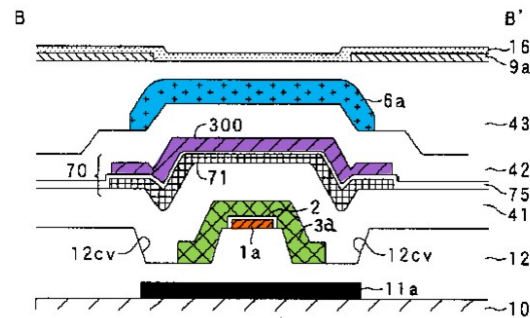


Takahara, Fig. 3

Takahara further discloses that “the **scan line** 3a is formed with a wide width at the location at which it becomes the gate electrode.” *Takahara*, ¶[0053]. Thus, like the prior art applied during prosecution, *Takahara* reflects the art’s understanding that the gate area must have certain minimum dimensions. Flasck, ¶174. *Takahara*’s **scan line** thus has a “broad-width portion in a portion facing the channel area of the thin-film transistor,” while the remainder of the scanning line is “a narrow width portion in another portion,” as claimed. Flasck, ¶174.



Takahara, Fig. 4



Takahara, Fig. 5

In addition, *Takahara*'s scan line has “**protruding portions** 3b, which protrude ... extending along the data line 6a viewed in plan view,” as best illustrated in Figure 4 (above-left). *Takahara*, ¶[0053]. Figure 5 (above-right) further illustrates a cross-section B-B' of the **protruding portions** 3b. *Id.* *Takahara*'s **protruding portion** constitutes *another* “broad-width portion in a portion facing the channel area of the thin-film transistor,” while the remainder of the scanning line is “a narrow width portion in another portion,” as claimed. *Flasck*, ¶174. Thus, *Takahara* provides the claimed feature for this additional reason.

Takahara teaches that **protruding portions** 3b protect the **TFT channel** (1a') against “impingement of the incident light advancing obliquely toward the substrate surface of the TFT.” *Id.*, ¶[0079]. According to *Takahara*, “even if various light-shielding films are provided above and below the **TFT** 30”—e.g.,

like the overlapping data line layer of *Kurashina*—“oblique light that advances through gaps between them can be present.” *Id.*, ¶[0082]; Flasck, ¶176. Thus, a POSITA would understand *Takahara*’s protruding portions to achieve improved performance—e.g., “even under severe conditions such as ... strong incident light or returning light, [the TFT] can satisfactorily perform switching control of the pixel electrode 9a, and ultimately a bright, high-contrast image can be displayed.” *Takahara*, ¶[0083]; Flasck, ¶176.

Kurashina and *Takahara* are each analogous art to the ’079 patent, at least because each “is from the same field of endeavor,” namely active-matrix drive electro-optical devices such as for LCD displays. *Unwired Planet*, 841 F.3d at 1000–01; Flasck, ¶177; *compare Kurashina*, ¶[0054] *with Takahara*, ¶[0051] *and* ’079 patent, Abstract. Moreover, *Kurashina* and *Takahara* both are directed to solving the same or related problems of light leakage that may negatively impact TFT channel performance. Flasck, ¶178; *compare Kurashina*, ¶¶[0052] and [0055] *with Takahara*, ¶[0082] (using “capacitor line 300 and the data line 6a” as “light-shielding films against the incident light entering the electro-optical device from above” and “protruding portions 3b, which shield the sides”) *and* ’079 patent, 23:29-30. As Mr. Flasck explains, “it was well-known at the relevant time that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel.” Flasck, ¶178. Furthermore, *Takahara* notes that its

design may be particularly helpful for systems having a relatively wide light-shielding layer above the TFT that might otherwise “increase ... internally reflected light and multiply reflected light.” *Takahara*, ¶[0007]; Flasck, ¶178. According to Mr. Flasck, “[a]lthough *Kurashina* mitigates internal reflection/refraction by only *partially* widening the data layer at the corner areas above the TFT, those widened portions still could benefit from the additional mitigating measures provided by *Takahara*’s scanning line projections (3b).” Flasck, ¶178. “A POSITA would thus consider references such as *Takahara* to be pertinent when implementing an active-matrix drive system such as *Kurashina*.” Flasck, ¶178.

It would have been obvious and straightforward to a POSITA to implement *Kurashina*’s design with *Takahara*’s widened scanning line portions, and the combination would require no more than ordinary skill. Flasck, ¶179. *Takahara* specifically teaches that its protruding portions can easily be implemented and manufactured. *Takahara*, ¶[0084] (“because the protruding portions 3b are formed integrally from the same film as the scan line 3a, no additional step is needed to form [them]”); *Id.* *Takahara* also teaches that its design is adaptable to various configurations—different protrusion designs can be used “considering the layout of the lines, elements, and the like around the semiconductor layer 1a.” *Takahara*, ¶[0086]. “That flexibility would give the POSITA a reasonable expectation of

success in implementing the principles of *Takahara* with the design of *Kurashina*.” Flasck, ¶179. Moreover, the art understood that “simply changing the patterning shape when the capacitor lines and the data lines are formed”—as would be required to implement *Takahara* with *Kurashina*—would be a relatively straightforward modification and “has the advantage of making formation possible even without providing any special process.” *Kurashina*, ¶[0022]; Flasck, ¶179. As such, Mr. Flask explains, a POSITA reasonably expect success combining the references, “given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Takahara* could be integrated into *Kurashina*’s device.” Flasck, ¶180. A POSITA would recognize that the benefits of *Takahara*’s light-shielding improvements would be “additive to the light-shielding mechanisms already present with *Kurashina*,” and the combination would yield a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion. Flasck, ¶179.

At bottom, both *Kurashina* and *Takahara* disclose devices using TFT for active matrix-drive control, and modifying *Kurashina*’s scanning line according to *Takahara*’s teachings would be a straightforward and predictable improvement to *Kurashina*’s device. Flasck, ¶180.

Thus, *Kurashina* and *Takahara* render obvious claim element 2[d]. Flasck, ¶181. And because *Kurashina* provides all remaining limitations, *Kurashina* in view of *Takahara* provide every limitation of independent claim 2 and, together, render obvious claim 2. *Id.*

2. Claim 3

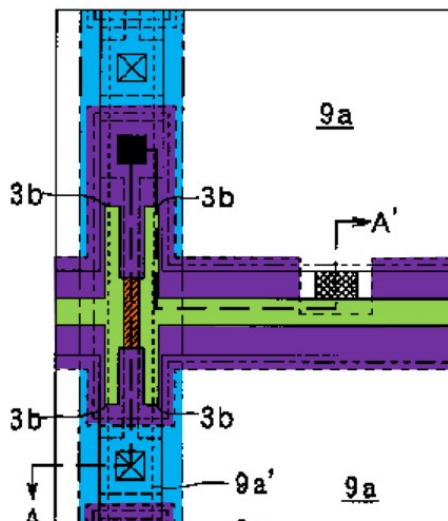
As discussed above in Section VI.A.2, *Kurashina* discloses the additional features of claim 3. Thus, *Kurashina* in view of *Takahara* also provides every limitation of claim 3 and, together, renders obvious claim 3. Flasck, ¶182.

3. Independent Claim 1

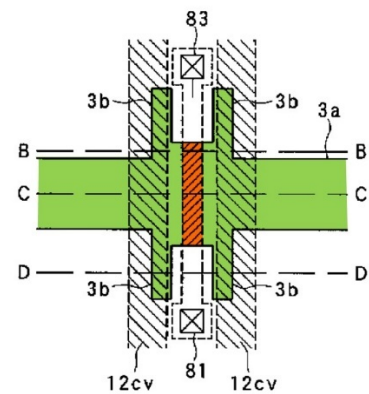
As discussed above in Section VI.A.3, *Kurashina* discloses every limitation of claim 1 except, arguably, “the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion,” as required by 1[d]. *See* VI.A.3.e; Flasck, ¶183.

1[d] would have been obvious over *Kurashina* in view of *Takahara* for the same reasons as 2[d]. *See* Section VI.B.1; Flasck, ¶184. As compared to 2[d], element 1[d] recites that (i) the scanning line has a broad-width portion in a portion “overlapping” (instead of “facing”) the channel area and (ii) the overlap is “in plan view.” As Mr. Flasck explains, “[t]hose differences in verbiage ... make no meaningful difference with respect to the design of *Kurashina* and *Takahara*,

because ... (i) the broad-width portion of [*Takahara*'s] scanning line is *both* 'facing' and 'overlapping' the TFT channel and (ii) [*Takahara*'s] Figures 2 and 4 show the overlap 'in plan view,'" as illustrated below. Flasck, ¶185.



Takahara, Fig. 2



Takahara, Fig. 4

For the reasons above, *Kurashina* in view of *Takahara* provide every limitation of independent claim 1 and, together, render obvious claim 1. Flasck, ¶186.

C. Ground 3: Claims 1-3 Are Obvious Over *Murade-109* in View of *Murade-125*

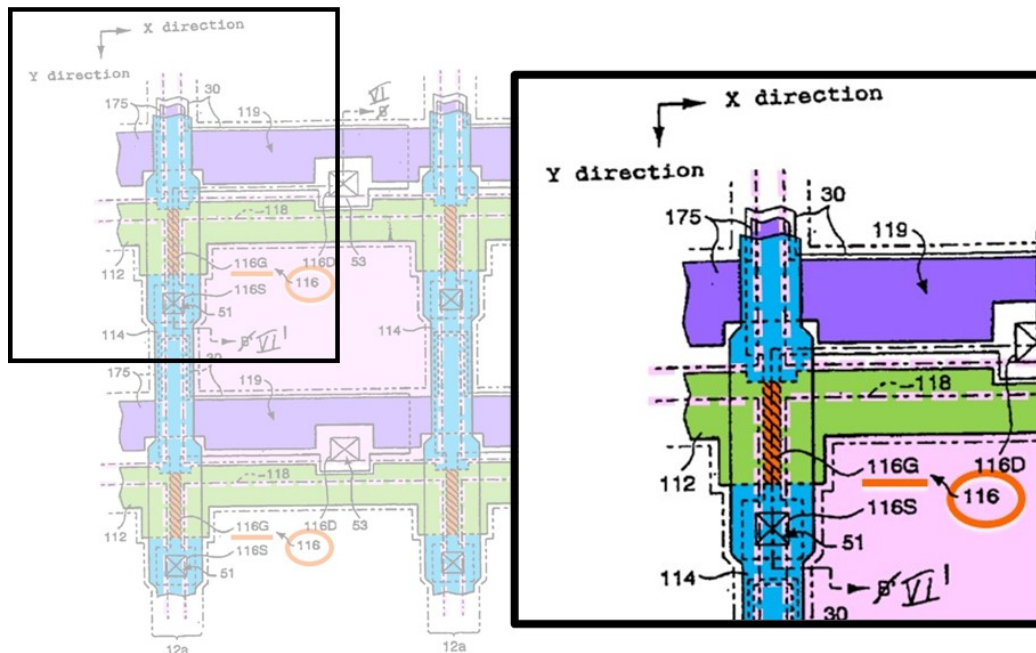
1. Independent Claim 2

a. 2[pre] An electro-optical device, comprising:

Murade-109 discloses 2[pre]. *Murade-109* discloses an "electro-optical device." *Murade-109*, Title; Flasck, ¶190.

- b. 2[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

Murade-109 discloses 2[a]. *Murade-109* discloses “principal elements, such as the **data line** 114, the **scanning line** 112, the **capacitor line** 175, and the **TFT [thin-film transistor]** 116,” as illustrated below. *Murade-109*, ¶[0135]; Flasck, ¶191. “A portion of the semiconductor layer 30 overlapping the **scanning line** 112 corresponds to a **channel region** 30a. That is, a portion of the scanning line 112 intersecting with the semiconductor layer 30 is used as a **gate electrode** 116G.” *Murade-109*, ¶[0138]. *Murade-109*’s **channel region** 30a (corresponding to the **gate electrode**) is a “channel area,” as claimed. Flasck, ¶191.

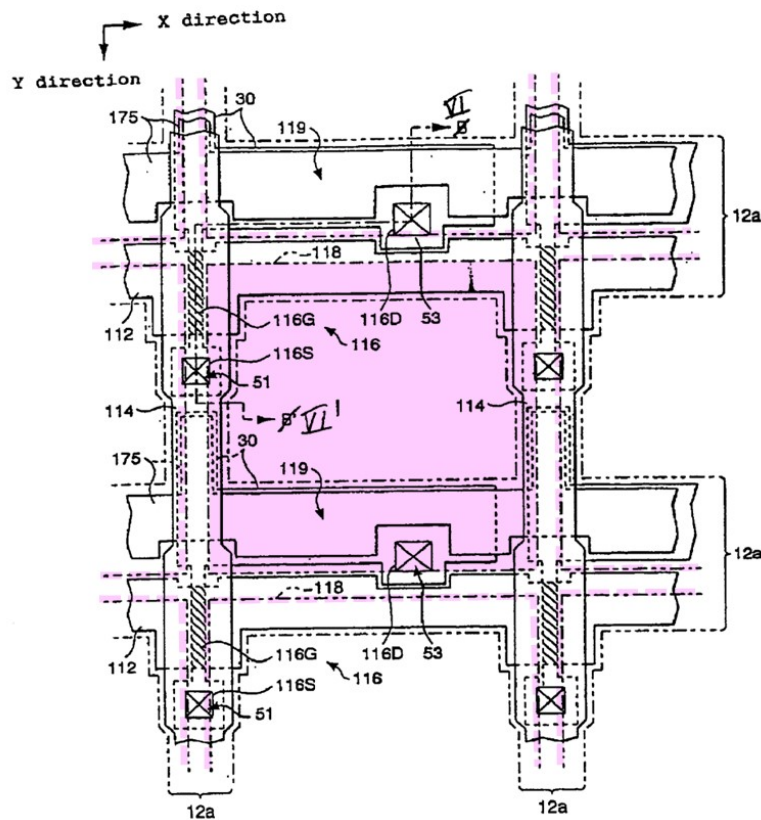


Murade-109, Fig. 5

As illustrated, the channel region of the **TFT** (30a, beneath **gate electrode** 116G) extends in a direction (“Y direction”) and intersects a predetermined direction (“X direction”) that intersects the direction (intersects the “Y direction”). Flasck, ¶192.

c. 2[b] a pixel electrode formed correspondingly to the thin-film transistor;

Murade-109 discloses 2[b]. *Murade-109* illustrates “the outline of the **pixel electrode** 118 ... indicated by a broken line” in Figure 5 below. *Murade-109*, ¶[0134]. Below, the central **pixel electrode** is highlighted pink, and adjacent pixels are indicated by pink dotted lines. Flasck, ¶193.



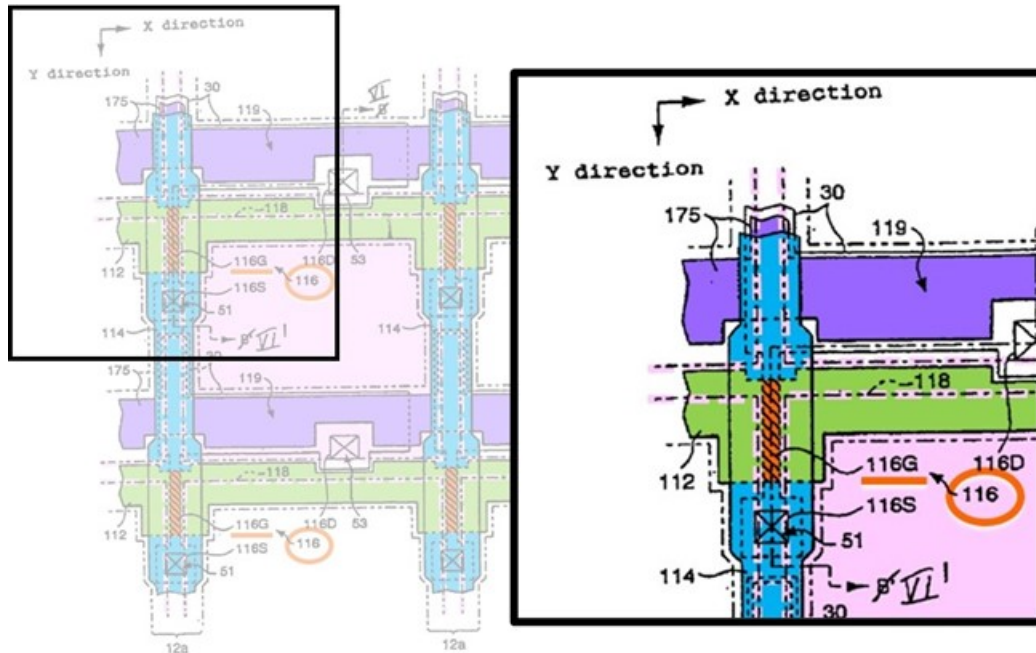
Murade-109, Fig. 5

Each **pixel electrode** in *Murade-109* is formed correspondingly to a TFT, as each “heavily-doped drain region 116D [of the TFT] is connected to the pixel electrode 118 by a contact hole 53.” *Murade-109*, ¶[0139]; Flasck, ¶194.

- d. 2[c] a data line extending in the direction in which the channel area extends, the data line having a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, the broad portion being wider than the non-broad portion;

Murade-109 discloses 2[c]. *Murade-109* discloses that “[t]he **data line 114** extends in the Y direction,” as illustrated below. *Murade-109*, ¶[0137]. The

channel area [30a, beneath gate 116G] also extends in the “Y direction.” See Section VI.C.1.b; Flasck, ¶195.



Murade-109, Fig. 5

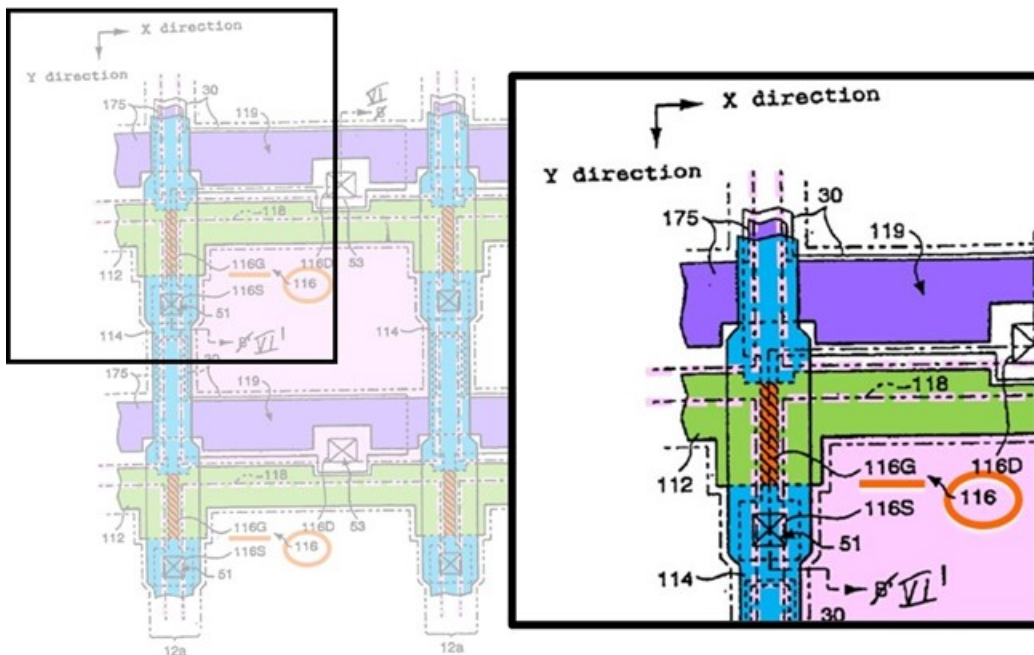
As illustrated above, *Murade-109*’s **data line** includes a “broad portion that overlaps the thin-film transistor” (e.g., **TFT** 116). Flasck, ¶196. Other portions of the data line (not overlapping the TFT) are a “non-broad portion,” and the broad portion is “wider than the non-broad portion,” as claimed. Flasck, ¶196; see *Mraz*, 455 F.2d at 1072 (“anticipation can be by drawings alone as well as words”).

Mr. Flasck explains that a POSITA in this field “would understand illustrated changes of shape within a given component (e.g., the changes in width of the **data line** where it overlaps the TFT) to convey general design information.” Flasck, ¶197. Further, a POSITA would recognize that broadening part of the data

like *Murade-109* would achieve design benefits (e.g., the light-shielding benefits known from *Kurashina*, section VI.A.1.d, *supra*). *Id.* Thus, a POSITA would recognize that “*Murade-109* teaches to provide the data line with a broad portion that overlaps the thin-film transistor and a non-broad portion that does not overlap the thin-film transistor, as claimed.” *Id.*

- e. **2[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;**

Murade-109 discloses 2[d]. *Murade-109* discloses that the “**scanning line** 112 extends in the X direction”—i.e., “in the predetermined direction”—and intersects the **data line** 114 and **channel region** 30a, which “extend[] in the Y direction.” *Murade-109*, ¶[0137]; *see also* ¶[0130] (TFTs are “located at the intersections between the first scanning line 112 ... and the six data lines 114”); Flasck, ¶198.



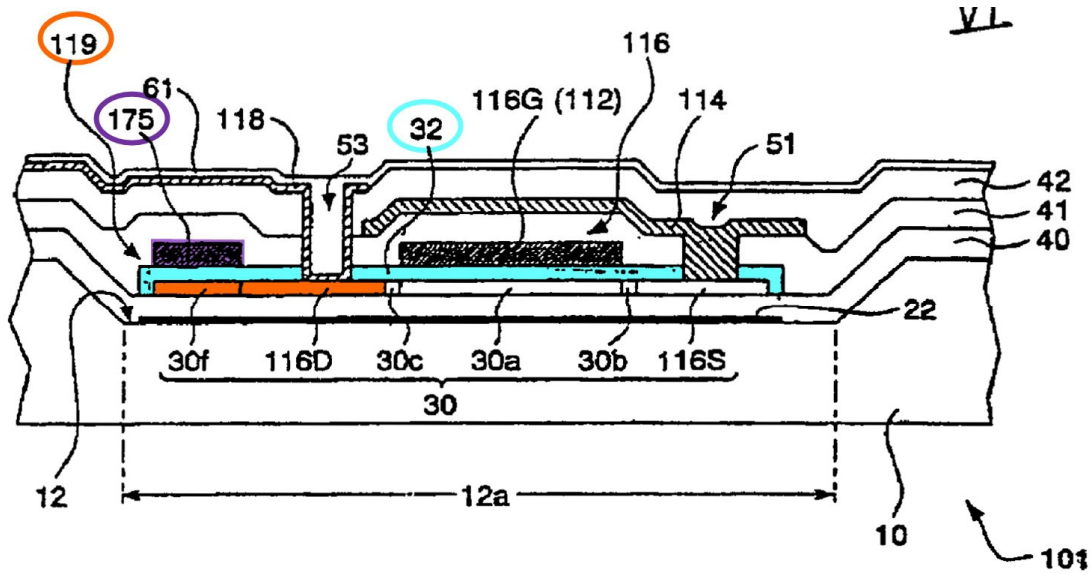
Murade-109, Fig. 5

Murade-109's **scanning line** further has a “broad-width portion in a portion facing the channel area [30a, beneath **TFT gate** 116G above]” and a “narrow width portion in another portion” (i.e., the portions of the scanning line between different TFT areas). Flasck, ¶199; see *Mraz*, 455 F.2d at 1072 (“anticipation can be by drawings alone as well as words”). As Mr. Flasck explains, a POSITA in this field “would understand illustrated changes of shape within a given component (e.g., the changes in width of the **scanning line** where it faces the TFT) to convey general design information.” Flasck, ¶199. Further, “a POSITA would recognize that broadening part of the scanning line as illustrated in *Murade-109* would achieve design benefits” (e.g., certain design benefits known from *Takahara*, section VI.B, *supra*). *Id.* Thus, a POSITA would recognize that “*Murade-109*

teaches to provide the scanning line with a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion, as claimed.” *Id.*

- f. **2[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and;**

Murade-109 discloses 2[e]. *Murade-109* discloses that “[a] portion of the **heavily doped drain region 116D** in the semiconductor layer 30 acts as one electrode of the **storage capacitor 119**. That is, in the **storage capacitor 119**, a **heavily-doped drain region 30f** located under the **capacitor line 175** acts as one electrode, and the **capacitor line 175** itself acts as the other electrode, and the **insulating film 32** formed on the semiconductor layer 30 is interposed between the two electrodes.” *Murade-109*, ¶[0140], Fig. 6 (below); *Flasck*, ¶200.



Murade-109, Fig. 6

Murade-109 explains that “[o]ne end of each storage capacitor 119 is connected to the pixel electrode 118 (the drain of the TFT 116)” —meaning that the **heavily doped drain region 116D** (including the **drain region 30f**) represents the potential of the pixel. *Murade-109*, ¶[0120]; Flasck, ¶202 (explaining that pixel 118 connects to the **heavily doped drain region 116D** (and, by extension, to the **drain region 30f**) via contact hole 53). That is, the **heavily doped drain region 116D** forms the first electrode of the storage capacitor and is a “pixel-potential capacitor electrode,” as claimed. Flasck, ¶202.

Further, “the other end [of the storage capacitor 119] is connected in common by a **capacitor line 175**,” which supplies a *fixed potential* because “what is required is to apply a constant voltage over time to the capacitor line 175.”

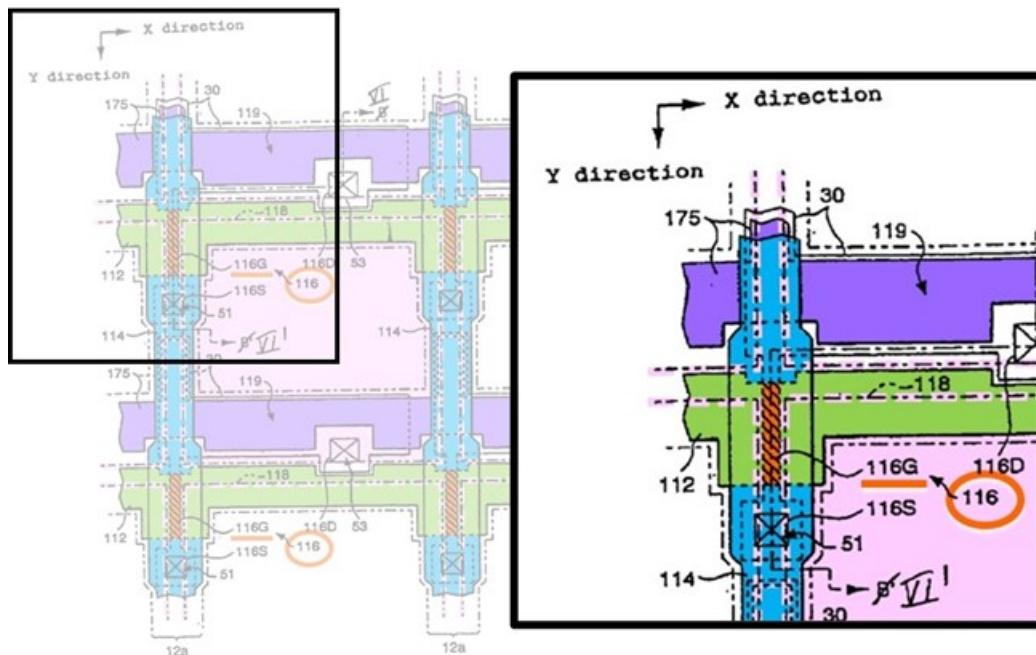
Murade-109, ¶[0120] (constant voltage from low level side voltage V_{ssY} , “high-

level-side voltage VddY, the voltage LCcom, or the like”); Flasck, ¶203. Thus, the **capacitor line** 175 is a “fixed-potential capacitor electrode.” *Id.*; see also *Murade-109*, ¶[0113] (“VssY of the power supply, which is the ground potential of [the] storage capacitor ... is also supplied to the individual pixels via capacitor lines 175”).

Moreover, because the **insulating film** 32 separates the two electrodes of the capacitor, allowing the buildup of an electric field between the two electrodes, the insulating film is necessarily a “dielectric film.” Flasck, ¶204 (citing Ex. 1020 at 3). Accordingly, *Murade-109* provides 2[e]. *Id.*

- g. 2[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.**

2[f] would have been obvious over *Murade-109* in view of *Murade-125*. Flasck, ¶205. In *Murade-109*, “[t]he **capacitor line** 175 extends in the X direction close to and in parallel to the **scanning line** 112, and at the section intersecting with the **data line** 114, the **capacitor line** 175 protrudes (upward in FIG. 5),” as illustrated below. *Murade-109*, ¶[0137]; Flasck, ¶206.

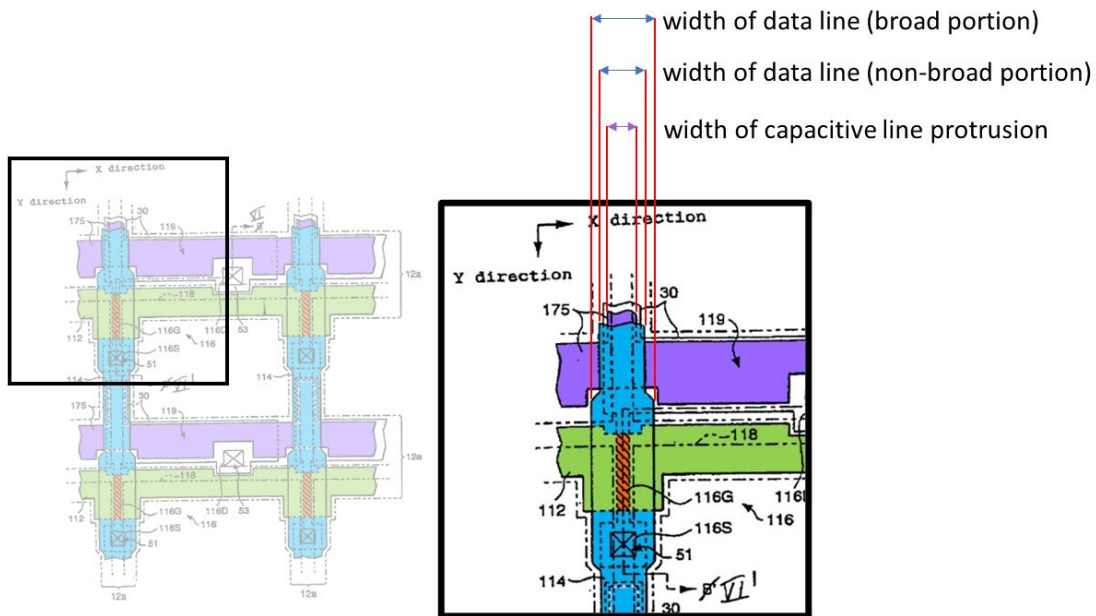


Murade-109, Fig. 5

As discussed above in 2[e], the capacitor line has a portion that “serves as the fixed-potential capacitor electrode of the storage capacitor,” as claimed. *See* Section VI.C.1.f; Flasck, ¶207.

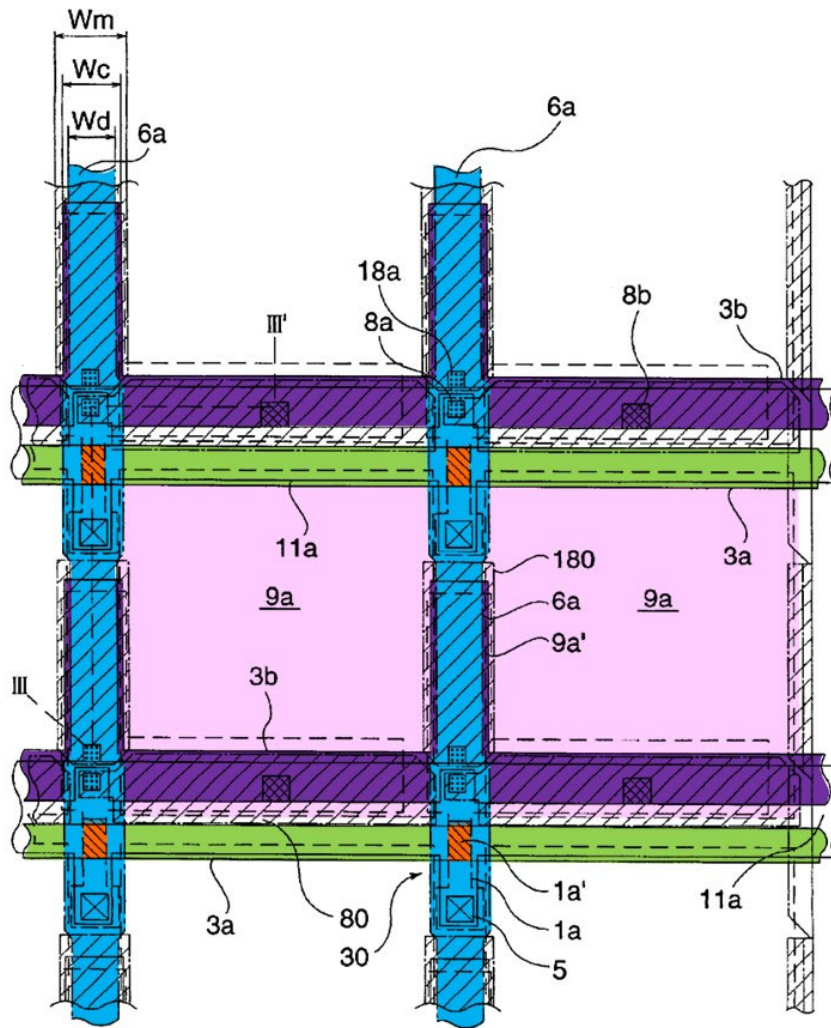
The portion of *Murade-109*’s **capacitive line** extending along the “X direction” is a “portion extending along the **scanning line**.” *Murade-109*, ¶[0137]; Flasck, ¶208.

The protruding portion of *Murade-109*’s **capacitive line** extending along the “Y direction” is a “portion extending along the **data line**.” *Murade-109*, ¶[0137]; Flasck, ¶209. Moreover, as illustrated below, the protruding portion has “a width that is narrower than the broad portion of the **data line**.” *Id.*



Murade-109, Fig. 5

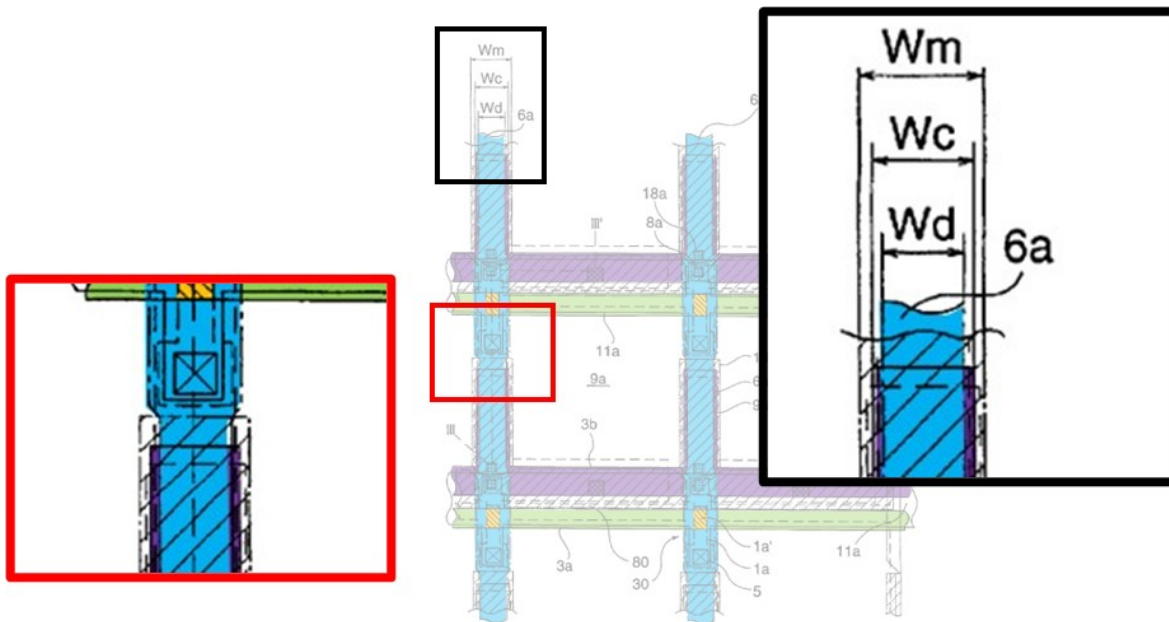
Slightly widening the protruding portion of the **capacitor line** to be wider than the non-broad portion of the **data line** (while still being narrower than the broad portion of the **data line**) would have been obvious in view of *Murade-125*, as explained below. Flasck, ¶210. Like *Murade-109*, *Murade-125* discloses “a plurality of the transparent **pixel electrodes** 9a ... provided in a matrix on the TFT-array substrate,” wherein the “**data lines** 6a, the **scan lines** 3a, and the **capacitor lines** 3b are respectively provided along the vertical and horizontal boundaries of the **pixel electrodes** 9a.” *Murade-125*, ¶[0057], Fig. 2 (below); Flasck, ¶212. As illustrated, “the **TFT** 30, in which the **scan line** 3a is disposed opposing the **channel region** 1a' as a gate electrode is provided at each intersection between the **scan line** 3a and the **data line** 6a.” *Murade-125*, ¶[0057]; Flasck, ¶212.



Murade-125, Fig. 2

Murade-125 identifies a “strong general demand for increased display image quality,” and teaches that “to this end, it is extremely important to increase the pixel aperture ratio (i.e., to increase the size of the aperture region of a pixel, through which display light passes, relative to the light-shielding region thereof, through which display light does not pass) while reducing pixel pitch.” *Murade-125*, ¶[0004]. *Murade-125* cautions, however, that reducing pixel pitch “results in

problems such as making it more difficult to incorporate the storage capacitors described above, especially as the pixel pitch is reduced, or to ensure the regions in which the contact holes are to be formed.” *Id.*, ¶[0005]. To address those issues, as well as to provide improved light blockage and improved capacitance, *Murade-125* teaches a “**capacitor electrode** further has a portion that extends along the **data line** as seen in plan view, and a width W_d of the **data line**, a width W_c of the **capacitor electrode**, and a width W_m of the portion of the intermediate conductive layer that extends along the data line satisfy the relationship $W_d < W_c < W_m$ at a location along the data line.” *Id.*, ¶¶[0041], [0094], Fig. 2; Flasck, ¶213. Thus, *Murade-125* teaches making the protruding portion wider than the non-broad portion of the data line, as required by 2[f]. Flasck, ¶213.



Murade-125, Fig. 2

According to *Murade-125*, **data line** material (typically aluminum) is a “reflective film of extremely high reflectivity,” meaning that “when a [TFT] is shielded solely by a data line formed from an Al film, projected light or returning light that is oblique to the surface of the substrate is reflected by the inner surface of the data line (i.e., the surface on the side facing the thin-film transistor), causing multiple reflection within the layered structure and ultimately causing the problem in which light reaches the channel region or regions adjacent thereto.” *Murade-125*, ¶[0042]. Thus *Murade-125* explains, widening the capacitive line relative to the data line (a) “attenuates multiply reflected light caused by internal reflection as described above” and (b) a “larger storage capacitor can be constructed using the capacitor electrode and the intermediate conductive layer, which are wider than the data line.” *Id.*; Flasck, ¶214. Accordingly, a POSITA would understand *Murade-125*’s capacitor line protruding portion to achieve desirable improvements in performance. Flasck, ¶214.

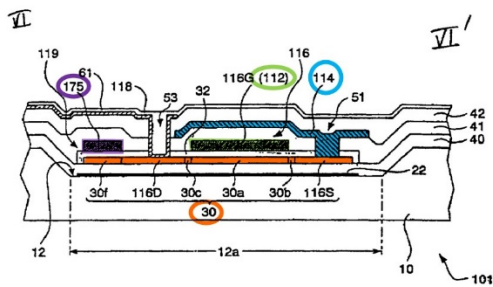
Furthermore, when making *Murade-109*’s capacitor line projection wider than the narrow portion of the data line (as taught by *Murade-125*), a POSITA would *not* make the capacitor line projection wider than the broad portion of the data line. Flasck, ¶215. This is because, in *Murade-109*, the wide portion of the data line does not overlap the capacitor line. *Id.* Thus, making the capacitor line wider than the broad portion of the data line would not achieve either benefit of

increased capacitance or shielding against internal reflection by that portion of the data line and would negatively reduce the aperture of the pixel area. *Id.* Thus, making the capacitor line projection wider than the narrow portion of the data line but narrower than the broad portion of the data line would have been an obvious design choice. *Id.*

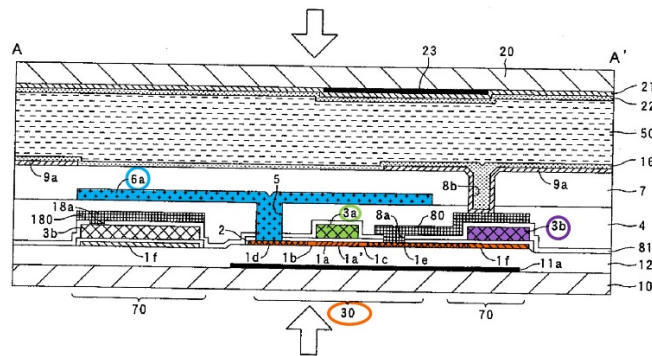
Murade-109 and *Murade-125* are each analogous art to the '079 patent, at least because each “is from the same field of endeavor,” namely active-matrix drive electro-optical devices such as for LCD displays. *Unwired Planet*, 841 F.3d at 1000–01; Flasck, ¶¶211, 216; *compare Murade-109*, ¶[0004] *with Murade-125*, ¶[0001] *and* '079 patent, Abstract. Moreover, *Murade-125* offers additional features to improve display quality, reduce light leakage, and improve capacitance, which a POSITA would recognize as desirable improvements to *Murade-109*. Flasck, ¶217. As Mr. Flasck explains, “it was well-known at the relevant time—including from the teachings of *Murade-125*—that an electro-optical device must be provided with measures to block incident light from reaching the TFT channel.” *Id.* “A POSITA would thus consider references such as *Murade-125* to be pertinent when implementing an active-matrix drive system such as *Murade-109*.” *Id.*

It would have been obvious and straightforward to a POSITA at the relevant time to implement *Murade-109*'s design with the capacitance line projections taught by *Murade-125*. Flasck, ¶218. The references already present similar layer

structures, including **TFT** (30), **data line** (114/6a), **scan line** (112/3a), and **capacitor line** (175/3b), as illustrated below. *Id.* Thus, a POSITA would recognize, for example, that the improvements offered by *Murade-125* may be implemented simply by changing the relative size of existing components (the data line and capacitive line projection), and such modifications were well within the level of ordinary skill. *Id.*



Murade-109, Fig. 6



Murade-125, Fig. 3

Moreover, “a POSITA would recognize that the benefits of *Murade-125*’s light-shielding improvements would be additive to the design already present in *Murade-109*,” and the combination would yield a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line. Flasck, ¶219.

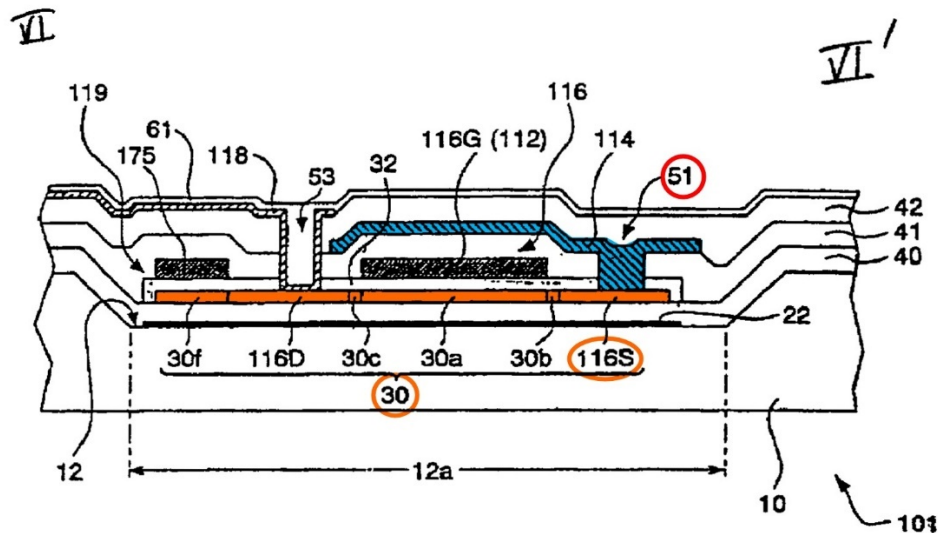
As Mr. Flasck further explains, “combining the teachings of *Murade-109* and *Murade-125* would have required no more than ordinary skill because the combination would have been a simple modification of an existing component (capacitive line and/or data line) in a straightforward manner to achieve predictable results.” Flasck, ¶220 (further explaining that the combination “would have had a reasonable expectation of success given their overall similarities, the particular overlap in functionality and the ease with which the relevant functionality of *Murade-125* could be integrated into *Murade-109*’s device”). At bottom, both *Murade-109* and *Murade-125* disclose devices using TFT for active matrix-drive control, and modifying *Murade-109*’s capacitive line and/or data line according to *Murade-125*’s teachings would be a straightforward and predictable improvement to *Murade-109*’s device. Flasck, ¶220.

Thus, *Murade-109* and *Murade-125* provide claim element 2[f] and render claim 2 obvious. Flasck, ¶221.

2. **Claim 3. The electro-optical device according to claim 2, further comprising a contact hole that electrically connects the thin-film transistor and the data line, the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.**

Murade-109 discloses the additional features of claim 3. As discussed in Section VI.C.1, *Murade-109* in view of *Murade-125* provide the electro-optical

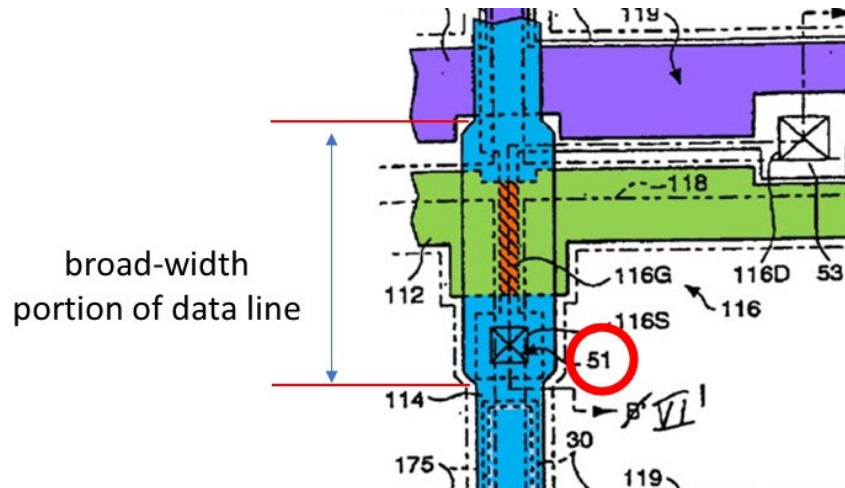
device of claim 2, from which claim 3 depends. *Murade-109* further discloses that “**heavily doped source region 116S** is connected to the **data line** by a **contact hole** 51 made through the insulating film 32 and a first interlayer insulating film 41.” *Murade-109*, ¶[0139], Fig. 6 (below); Flasck, ¶223. As Mr. Flasck explains, the heavily doped source region 116S is part of the TFT (30). Flasck, ¶223; *see Murade-109*, ¶[0163] (“TFT has an LDD structure in which ... a heavily-doped source region 116S [is] provided”).



Murade-109, Fig. 6

Murade-109 also discloses “the data line being continuously broad from the broad portion that overlaps the thin-film transistor [to] a portion where the contact hole is located.” Flasck, ¶224. As illustrated in Figure 5 (below), the **data line** 114 is broad—i.e., “broader than the width of the ‘narrow width portion’”—throughout

its entire extent from a portion that overlaps the TFT (116, including gate portion 116G) through to the **contact hole** (51). *Id.* ¶



Murade-109, Fig. 5

Thus, *Murade-109* in view of *Murade-125* also provides every limitation of claim 3 and, together, renders obvious claim 3. Flasck, ¶225.

3. Independent Claim 1

a. 1[pre] An electro-optical device, comprising:

Murade-109 discloses 1[pre] for the same reasons as 2[pre]. See

Section VI.C.1.a.

b. 1[a] a thin-film transistor having a channel area that extends in a direction and that intersects a predetermined direction that intersects the direction;

Murade-109 discloses 1[a] for the same reasons as 2[a]. See

Section VI.C.1.b.

- c. 1[b] a pixel electrode formed correspondingly to the thin-film transistor;**

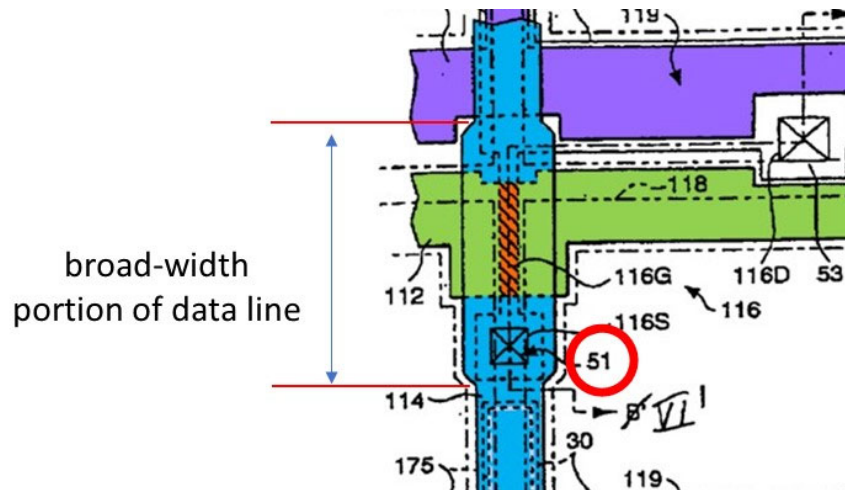
Murade-109 discloses 1[b] for the same reasons as 2[b]. *See*

Section VI.C.1.c.

- d. 1[c] a data line extending in the direction in which the channel area extends, the data line having a broad-width portion that overlaps the channel area in plan view;**

Murade-109 discloses 1[c] for the same reasons as 2[c]. See

Section VI.C.1.d; Flasck, ¶229. As compared to 2[c], 1[c] further specifies that the broad-width portion of the data line overlaps the channel area “in plan view,” which *Murade-109* illustrates in Figure 5 (below). *Id.*



Murade-109, Fig. 5

- e. **1[d] a scanning line extending in the predetermined direction and intersecting the data line and the channel area of the thin-film transistor, the scanning line having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion;**

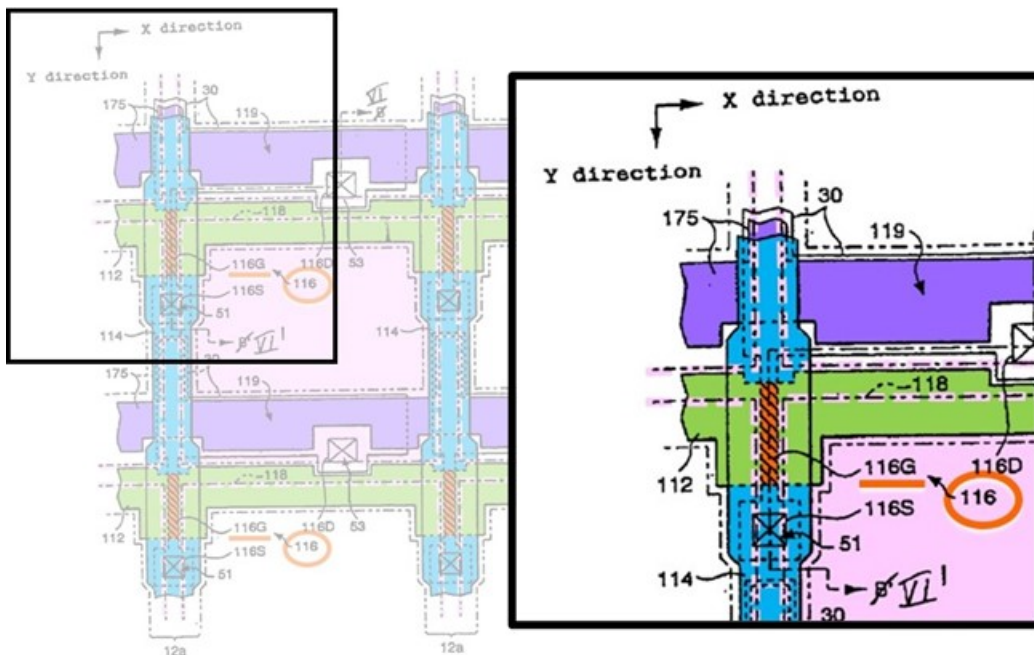
Murade-109 discloses 1[d] for the same reasons as 2[d]. *See*

Section VI.C.1.e; Flasck, ¶230. As compared to 2[d], element 1[d] recites that

(i) the scanning line has a broad-width portion in a portion “overlapping” (instead of “facing”) the channel area and (ii) the overlap is “in plan view.” Flasck, ¶230.

As Mr. Flasck explains, “[t]hose differences in verbiage ... make no meaningful difference with respect to the design of *Murade-109*, because as illustrated in

Figure 5 of *Murade-109* ... (i) the broad-width portion of the scanning line is *both* ‘facing’ and ‘overlapping’ the TFT channel and (ii) Figure 5 shows the overlap ‘in plan view,’” as illustrated below. *Id.*



Murade-109, Fig. 5

- f. **1[e] a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed-potential capacitor electrode;**

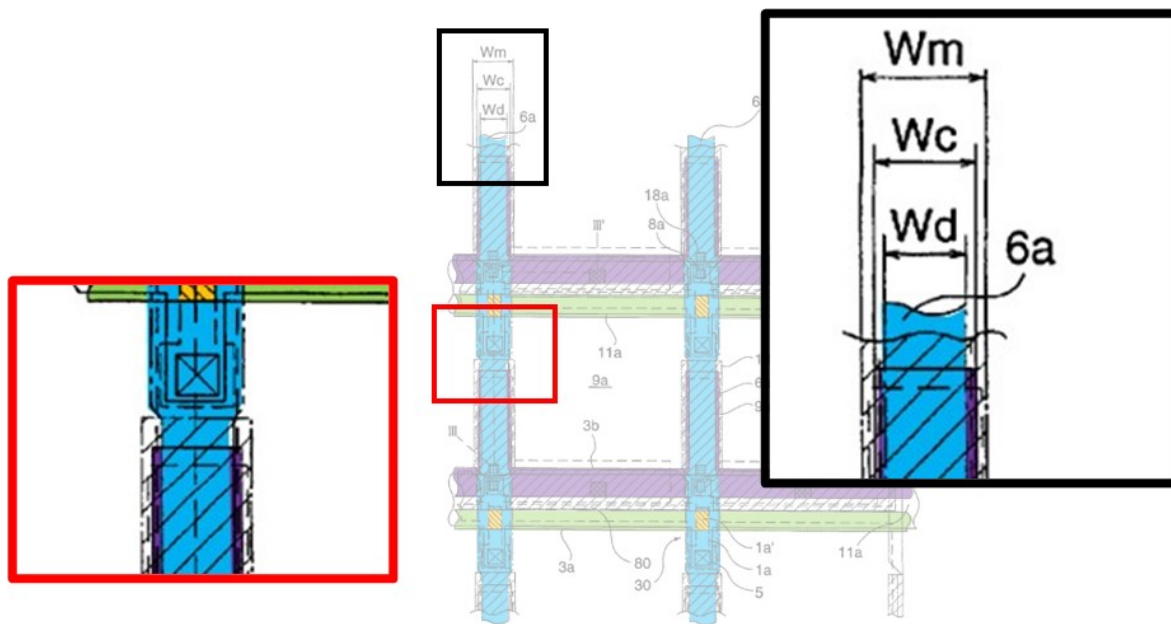
Murade-109 discloses 1[e] for the same reasons as 2[e]. See

Section VI.C.1.f.

- g. **1[f] a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and**

1[f] would have been obvious over *Murade-109* in view of *Murade-125* for the same reasons as 2[f]. See Section VI.C.1.g; Flasck, ¶232. As discussed in

connection with 2[f] and as illustrated below, the portion of *Murade-125*'s **capacitor line** (width W_c) extending along the **data line** is broader than the non-broad portion of the data line (width W_d). Width W_d of *Murade-125* is “a width”; therefore, the “the portion [of the capacitive line] extending along the data line having a width that is equal to or broader than a width of the data line.” Flasck, ¶232.



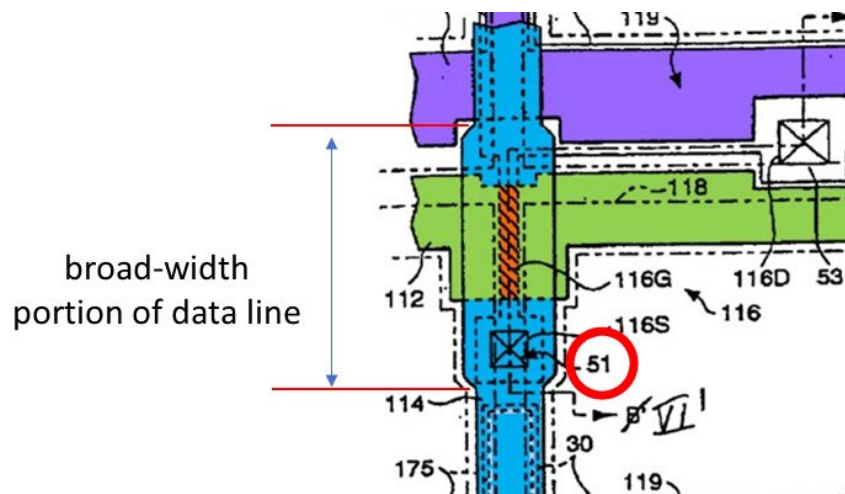
Murade-125, Fig. 2

- h. 1[g] a contact hole electrically connecting the data line and the thin film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.

Murade-109 discloses 1[g] for the same reasons as Claim 3. See Section VI.C.2; Flasck, ¶234. As compared to claim 3, 1[g] omits the

“continuously broad” limitation. The contact hole of 1[g] need only be positioned “at a portion of the broad-width portion of the data line,” which “extends beyond the channel area in a direction extending from the channel area toward the contact hole.” Flasck, ¶234.

As illustrated below, broad width portion of the **data line** (114) extends beyond the **channel area** (30a, beneath gate 116G) in a direction (vertically down) extending from the channel area toward the **contact hole** (51). Flasck, ¶235. Further, the **contact hole** (51) is positioned at the foregoing “portion of the broad-width portion of the **data line**.” *Id.*



Murade-109, Fig. 5

For the reasons above, *Murade-109* in view of *Takahara* provide every limitation of independent claim 1 and, together, render obvious claim 1. Flasck, ¶236.

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office’s interim guidelines dated June 21, 2022 (“Interim Procedures”) require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 6 requires institution because the merits of this Petition are strong. The Petition relies upon materially different and non-cumulative primary references not applied during prosecution of the ’079 patent, which teach the very features the applicant argued during prosecution to be lacking from the prior art.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions less than three months ago, on March 11, 2024. Ex. 1023. *See, e.g., Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 11 (PTAB Mar. 20, 2020) (“[I]t is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding.”); *Coolit Sys., Inc. v. Asetek Danmark A/S*, IPR2021-01195, Paper 10 at 11, 14 (PTAB Dec. 28, 2021) (finding petitioner acted diligently where it filed the petition within five months after PO provided contentions for nine patents). Fact discovery opened only last month, and

the claim construction hearing will not take place until January 2025; therefore, the district court's investment by institution will be nominal. Ex. 1022.

Factor 4 favors institution because this petition challenges claims 1 and 3, which are not involved in the litigation.

Regarding Factors 1, 2, and 5, Patent Owner filed its Complaint against Petitioner on November 8, 2023. Ex. 1021. No stay has been requested, trial is currently scheduled for June 2025, and the current median time-to-trial in the Eastern District of Texas is 21.4 months (Ex. 1024), so trial is projected to occur in August 2025 at the earliest. Ex. 1024. A FWD is anticipated by November 2025. In light of the Board's holistic analysis balancing all the *Fintiv* factors, however, the trial date of the related litigation is not determinative but weighed in concert with the other relevant factors. *See e.g., Netnut Ltd., v. Bright Data Ltd.*, IPR2021-01492, Paper 12 at 9-16 (PTAB March 21, 2022) (instituting review with related litigation trial date six months before final written decision deadline; no stipulation regarding district court arguments made); *Coolit*, Paper 10 at 11, 14 (same by five months; *Sand II* stipulation); *Micron Technology, Inc., v. Vervain, LLC*, IPR2021-01550, Paper 11 at 9-13 (PTAB April 11, 2022) (same by approximately three months).

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under § 325(d)

Neither of the *Advanced Bionics* factors warrant denial of institution. During prosecution, the Examiner did not consider, let alone rely on, the primary references or secondary references *Sato* and *Takahara* asserted herein. *Id.* *Murade-125* was submitted (in Japanese), but there is no record of how (if at all) the examiner squared the applicant's arguments with *Murade-125*'s disclosure of key features applicant argued to secure allowance. *See* Section IV.A.5. As the Board has explained, "the criteria adopted by the Board for denying the petition in *Advanced Bionics* included not only the fact that the art was made of record, but also the fact that it was applied and discussed during prosecution." *Nintendo Co., Ltd. et al. v. Gamevice, Inc.*, IPR2023-00643, Paper 11 at 18-19 (PTAB Nov. 6, 2023). Here, because *Murade-125* was neither applied nor discussed, the record indicates that "the Examiner overlooked [*Murade-125*'s] teachings of the limitations that were the basis for allowing the challenged claims," which constitutes error material to patentability. *See id.* at 19. The Board should not exercise its discretion to deny institution under 35 U.S.C. § 325(d).

VIII. MANDATORY NOTICES

A. Real Parties-in-Interest

The real party-in-interest is BOE Technology Group Co., Ltd.

B. Related Matters

The '079 patent is currently asserted in *Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.*, 2:23-cv-00515 (EDTX). Petitioner is not aware of any other judicial or administrative matter that would affect, or be affected by, a decision in this proceeding.

On its face, the '079 patent purports to claim priority to U.S. Patent Application No. 10/320,371, filed Dec. 17, 2002, since issued as U.S. Patent No. 7,136,117. The '079 patent further claims priority to two foreign applications: JP-2002-000713, filed Jan. 7, 2002, and JP-2002-363864, filed Dec. 16, 2002.

One U.S. patent application purportedly claims priority to the '079 patent or the application for the '079 patent (No. 11/290,589), namely, No. 12/320,647, filed January 30, 2009, since issued as U.S. Patent No. 7,859,603.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the addresses above.

Petitioner consents to electronic service by email at the above email addresses.

IX. GROUNDS FOR STANDING

Petitioner certifies that the '079 patent is available for IPR, and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

X. CONCLUSION

For the reasons above, Petitioner requests institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: June 4, 2024

Respectfully Submitted,

/ Joshua L. Goldberg /
Joshua L. Goldberg
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW contains 13,525 words, excluding the parts of this Petition that are exempted under 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

/ Joshua L. Goldberg /
Joshua L. Goldberg
Reg. No. 59,369

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Petitioner's Power of Attorney, and the associated Exhibits 1001-1006, 1008-1031** were served via overnight courier on June 4, 2024, on the correspondence address of record below indicated in the Patent Office's Patent Center for U.S. Patent No. 7,502,079.

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Dated: June 4, 2024

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