

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. IPR2024-00976
U.S. Patent No. 7,502,079

PATENT OWNER'S PRELIMINARY RESPONSE

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U.S. Patent No. 7,502,079

TABLE OF EXHIBITS

Number	Description
2001	Declaration of E. Fred Schubert, Ph.D.

I. PRELIMINARY STATEMENT

Pursuant to 37 C.F.R. § 42.107, Patent Owner 138 East LCD Advancements Limited (“138 East” or “Patent Owner”) submits its Preliminary Response to the Petition for *Inter Partes* Review of U.S. Patent No. 7,502,079 (“the ’079 patent”). Paper 2 (“Petition” or “Pet.”). Petitioner BOE Technology Group Co., Ltd., challenges the validity of claims 1-3 of the ’079 patent.

The Petition has not established a reasonable likelihood that the asserted references render any of claims 1-3 unpatentable. The asserted references, alone or in combination as presented in the Grounds, do not disclose all limitations of any challenged claim. In particular, in Grounds 1 and 2, the Petition fails to show that Kurashina discloses a capacitor line at least as broad as the data line as claimed, because the drawings on which the Petition relies are not to scale. The Petition further fails to show that Sato or Takahara would motivate a POSA to alter the scan line geometry of Kurashina as claimed, because doing so would be contrary to the express teachings of Kurashina. In Ground 3, the Petition relies on a combination of incompatible references directed to different designs, and fails to show that modifying Murade-109 in view of Murade-125 would result in a capacitor line at least as broad as the data line as claimed. The Board therefore should deny institution for failure to present a likelihood that the Petitioner will prevail on any Ground.

II. THE '079 PATENT

The '079 patent, titled “Electro-optical device and electronic apparatus,” describes arrangements of scan lines, data lines, and capacitive lines in a liquid crystal display device that result in improved optical performance. Broadly, the '079 patent recognizes a need for precision in driving the thin-film transistors (TFTs) connected to the pixel electrodes in the liquid crystal electro-optical device while simultaneously miniaturizing the electro-optical components for a compact design. *Id.*, 1:42-48.

TFTs comprise a semiconductor layer with a channel area; source and drain areas; and a gate electrode covering at least a part of the channel area. *Id.*, 1:49-52. Applying a voltage to the gate electrode causes an electric field to be applied in the channel area, which leads to current flow through the TFT. *Id.*, 1:52-55. The on and off states of the TFTs are therefore controlled by the gate electrode: when a voltage is applied to the gate electrode, the TFT is on, and vice versa. Ex. 2001, ¶34. The gate electrode, in turn, is part of or otherwise connected to the scan line. *Id.*, 1:61-64.

According to the '079 patent, both the length of the channel area in the TFT (the “channel length”) and the arrangement of the gate electrode on the channel area are important factors in determining the characteristics of the TFTs. *Id.*, 1:56-61. The '079 patent describes the importance of arranging the TFT in relation to

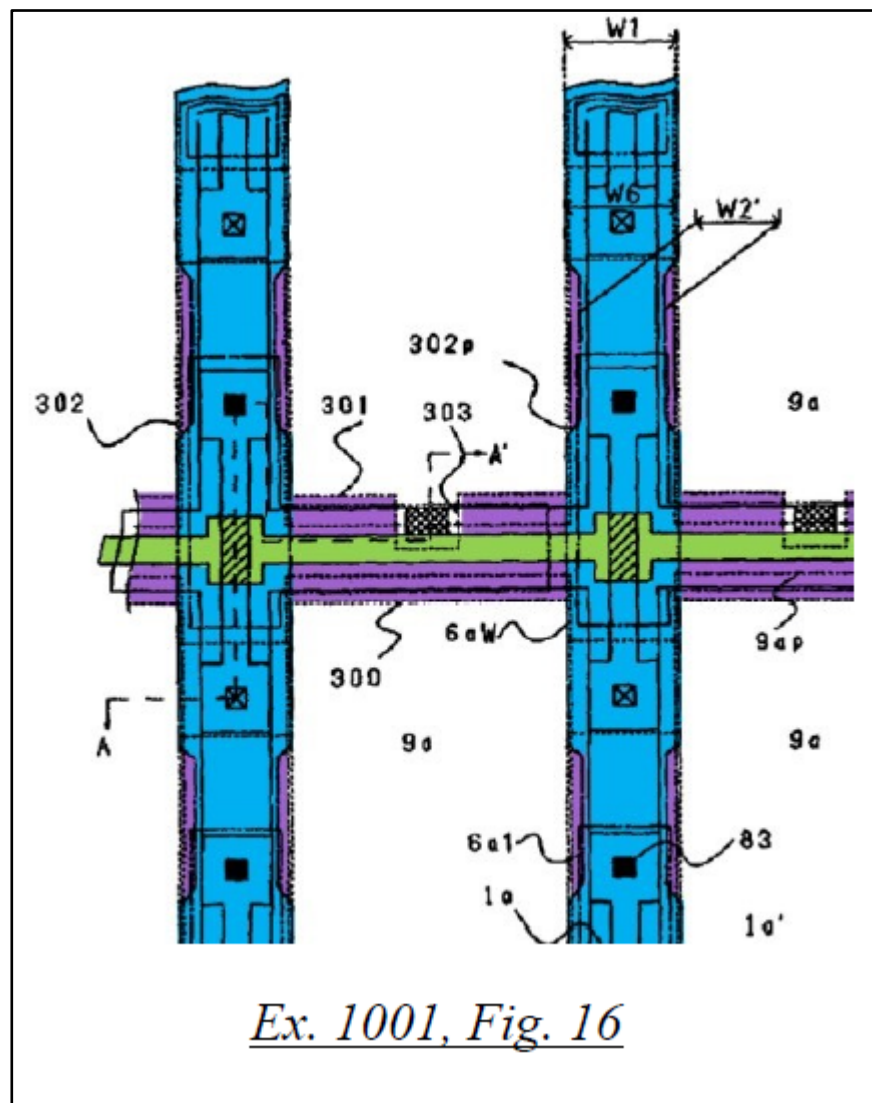
the scanning line so as to achieve precision in driving the TFTs. *Id.*, 1:66-2:4. But the '079 patent also describes detrimental effects associated with light leakage currents, which are generated by light entering the channel area. *Id.*, 2:10-12. According to the '079 patent, the TFTs should be placed as far as possible from light-transmitting areas of the device such as pixel electrodes. *Id.*, 2:12-16. This restriction on TFT placement also restricts the scan line/TFT arrangement, which may compromise precision in operating the device. *Id.*, 2:17-20.

The '079 patent solves these problems by providing scan lines that have broad-width portions where they face the channel area and act as the gate electrode, and that have narrow-width portions elsewhere. *Id.*, 2:42-45. Through this arrangement, the channel areas of the TFTs can be placed far from the pixel corners to protect them from incident light. Yet the channel areas still have adequate length for precision control, while realizing device miniaturization through the narrow scan lines away from the channel areas. *Id.*, 2:50-3:5. Because the broad-width portion of the scan line extends with the channel area, the gate electrode is better formed to the channel, and the electric field can be more precisely applied in the channel area. *Id.*, 3:52-59.

The '079 patent further discloses forming storage capacitors connected to the pixel electrodes by providing capacitive lines that extend along both the scan lines and the data lines. *Id.*, 7:56-67. According to the '079 patent, the portion of

the capacitive line extending along the data line should have a width equal to or broader than that of the data line. *Id.*, 7:63-67. The broader capacitive line not only has a low resistance, but its breadth compared to the data line shields stray light reflecting off the back of the data line that can enter the TFT and contribute to the light leakage current. *Id.*, 8:7-10, 8:29-39.

The above-described features are shown in the annotated excerpt of Figure 16 from the Petition, as reproduced below:



Pet., 9.

Figure 16 depicts the channel areas (1a'), scan lines (9a), data lines (6a) and capacitive lines (300) discussed above. In the particular embodiment shown, the data lines are formed with broad-width portions 6aW that overlap the TFTs; the portions of the capacitive lines overlapping the TFTs are likewise broad, although not as broad as the data lines in those regions. Away from the TFTs, the data lines

are formed with narrow-width portions, and the portions of the capacitive lines in these areas are as broad as, or broader than, the data lines. This geometry provides shielding of stray light reflecting off the back of the data line, as discussed above.

These novel aspects of the '079 patent disclosure, illustrated in the annotated figure above, are also reflected in independent claim 2, which recites as follows:

2. An electro-optical device, comprising:
 - a thin-film transistor having a channel area that extends in
a direction and that intersects a predetermined
direction that intersects the direction;
 - a pixel electrode formed correspondingly to the thin-film
transistor;
 - a data line extending in the direction in which the channel
area extends, the data line having a broad portion
that overlaps the thin-film transistor and a non-
broad portion that does not overlap the thin-film
transistor, the broad portion being wider than the
non-broad portion;
 - a scanning line extending in the predetermined direction
and intersecting the data line and the channel area
of the thin-film transistor, the scanning line having

a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion;

a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed potential capacitor electrode; and

a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.

Id., 26:24-53.

The '079 patent also discloses contact holes 81 that connect the semiconductor layer 1a of the TFT to the data line 6a, as shown in Figure 16 above. *Id.*, 23:56-62. According to the '079 patent, no capacitive line can be

formed here because of the need to connect the data line and semiconductor layer.

Id., 23:59-62. The data line is therefore kept broad from the TFT to the formation position of the contact hole to maintain light shielding performance. *Id.*, 23:66-24:8. This further aspect is reflected in independent claim 1 of the '079 patent, which recites as follows:

1. An electro-optical device, comprising:
 - a thin-film transistor having a channel area that extends in
a direction and that intersects a predetermined
direction that intersects the direction;
 - a pixel electrode formed correspondingly to the thin-film
transistor;
 - a data line extending in the direction in which the channel
area extends, the data line having a broad-width
portion that overlaps the channel area in plan view;
 - a scanning line extending in the predetermined direction
and intersecting the data line and the channel area
of the thin-film transistor, the scanning line having
a broad-width portion in a portion overlapping the
channel area of the thin-film transistor in plan view
and a narrow width portion in another portion;

a storage capacitor including a pixel-potential capacitor electrode, a fixed-potential capacitor electrode, and a dielectric film interposed between the pixel-potential capacitor electrode and the fixed-potential capacitor electrode;

a capacitive line having a portion that serves as the fixed-potential capacitor electrode of the storage capacitor, the capacitive line having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line; and

a contact hole electrically connecting the data line and the thin film transistor, the contact hole being positioned at a portion of the broad-width portion of the data line that extends beyond the channel area in a direction extending from the channel area toward the contact hole.

Id., 25:51-26:23.

Claim 3 depends from claim 2 and adds a contact hole limitation similar to that of claim 1:

3. The electro-optical device according to claim 2, further comprising
a contact hole that electrically connects the thin-film transistor
and the data line, the data line being continuously broad from
the broad portion that overlaps the thin-film transistor a portion
where the contact hole is located.

None of the asserted references or combinations disclose the claimed layouts that deliver the benefits of the '079 inventions.

III. CLAIM CONSTRUCTION

Patent Owner does not believe that any claim terms require express construction to deny institution. Accordingly, the claims should be given their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art. 37 C.F.R. § 100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

Petitioner provides proposed constructions of the terms “broad portion” and “broad-width portion.” Pet., 16. Patent Owner contends that these terms have their plain and ordinary meanings, which would be apparent to a person of ordinary skill in the art and even a layperson. Even under Petitioners’ constructions, however, the

alleged prior art references do not disclose the features claimed in the '079 patent, as discussed further below.

IV. LEGAL STANDARD

The Board may not institute an *inter partes* review unless the Petition demonstrates a reasonable likelihood that the petition would prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

V. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Preliminary Response only, Patent Owner does not dispute the level of skill for a person of ordinary skill in the art (“POSA”), set forth in the Petition. Pet., 26. Patent Owner does not waive, however, any argument regarding the proper level of skill and reserves the right to later advance additional arguments.

VI. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD THAT THE ASSERTED REFERENCES RENDER UNPATENTABLE ANY CHALLENGED CLAIM.

A. The Petition does not establish a reasonable likelihood that Kurashina in view of Sato or Takahara renders obvious claims 1-3 (Grounds 1 and 2).

1. Kurashina: Overview

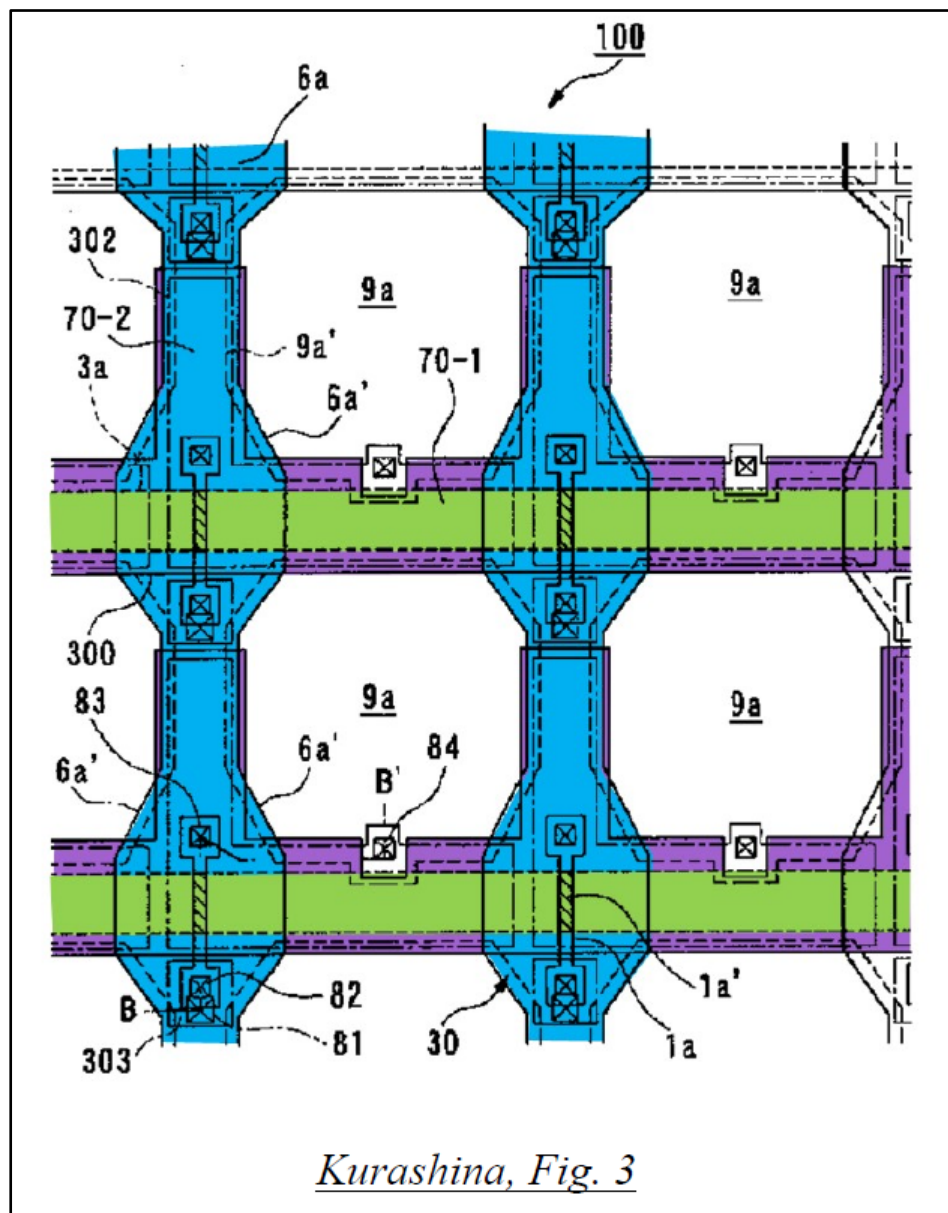
JP-2002-090721A to Kurashina (“Kurashina”) is primarily focused on shielding transistor elements from light leakage currents induced by light emanating from the corner portions of pixels in liquid crystal projector displays.

Ex. 1008 at 1, ¶[0016]. Kurashina recognizes that in “an extremely powerful light source such as a projector,” even light reflecting off the substrate rear-surface side can enter the TFT channel and alter the switching characteristics of the device. *Id.*, ¶[0017]. To solve this problem, Kurashina teaches “a light-shielding film layered between the transistor and the pixel electrode” with “a wide width in the vicinity of the transistor” that “shield[s] a corner portion of the pixel electrode.” *Id.*, ¶[0019].

Kurashina recognizes performance tradeoffs in the disclosed configuration: for instance, Kurashina notes that shielding the corner portions of the pixel electrode narrows its aperture area, which results in less emitted light. *Id.*, ¶[0020]. According to Kurashina, however, the tradeoff is the ability to block light from the pixel electrodes arriving at the TFT from oblique directions, as doing so maintains the switching characteristics of the TFT. *Id.*

Kurashina also teaches using capacitor lines or data lines as the light-shielding films for the corner portions of the pixels. *Id.*, ¶[0021]. Where the light-shielding capacitor lines overlap the scan lines, Kurashina notes, “it is possible to make the width of the capacitor lines take up the entire interval between pixels,” and to thereby “increase storage capacitance.” *Id.*, ¶[0024].

Figure 3 of Kurashina is exemplary of the main aspects taught; the annotated version of Figure 3 below is reproduced from the Petition and is the primary figure discussed therein:



Pet., 8; *see also* Ex. 1008 at 14.

As shown in Figure 3, the capacitor lines 300 “overlap the scan lines 3a and are provided in the left-right direction in the paper plane along the boundaries of the pixel electrodes 9a.” Ex. 1008, ¶[0057]. The capacitor lines further form two sets of storage capacitors: a first set 70-1 formed by the overlap between the L-

shaped drain electrodes 302 and portions of the capacitor lines 300 overlapping the scan lines; and a second set 70-2 formed by the overlap between the drain electrodes 302 and the portions of the capacitor lines 300 overlapping the data lines. *Id.*, ¶[0058]. According to Kurashina, in this way the “spaces apart from the aperture regions . . . are effectively used to increase the storage capacitance of the pixel electrodes 9a,” and the increased storage capacitance is used “to stabilize the display screen.” *Id.*, ¶[0059].

Unlike the '079 patent, therefore—which balances light shielding with miniaturization—Kurashina is primarily concerned with blocking light coming from corner portions of the pixels.

2. The Petition fails to show that Kurashina discloses all limitations of any challenged claim.

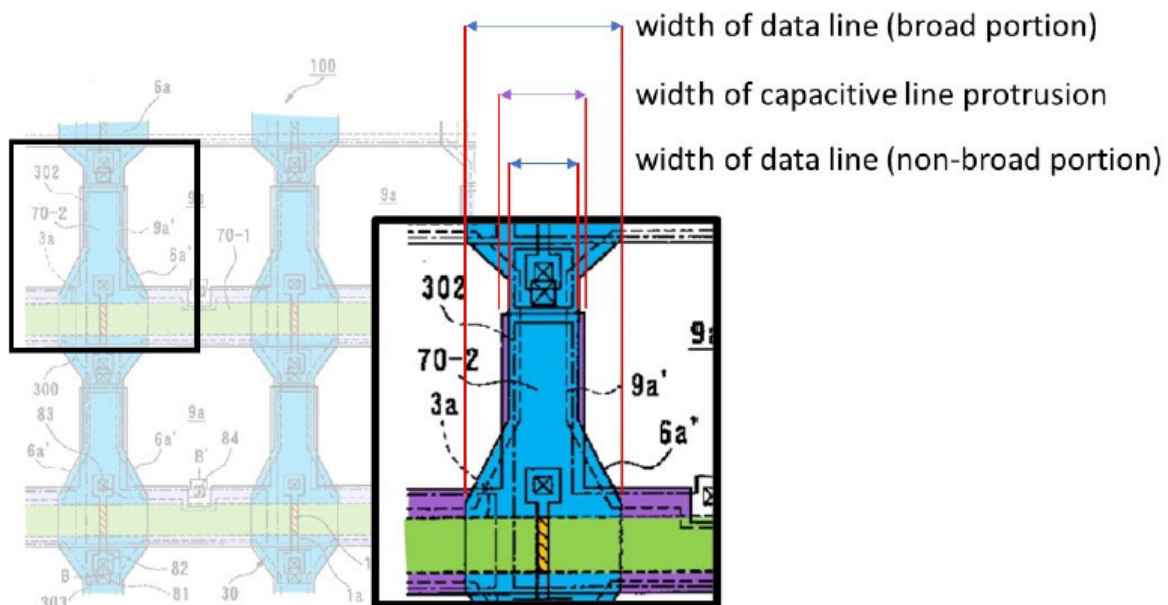
a. Claim 2

- i. The Petition does not show that Kurashina discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”**

The Petition fails to show that Kurashina discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is

narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

The Petitioner’s only cited support for this claim element in Kurashina is Figure 3, which the Petition annotates as follows:



Kurashina, Fig. 3

Pet., 19. Although Kurashina’s written description contains no express disclosure of the relative widths of the data line and capacitive line, the Petition notes that the Board has “on several occasions” relied upon prior art drawings to depict relative sizes. Pet., 44.

The Petition’s reliance on these decisions is misplaced. All of the cases cited in the Petition involve patents that were silent as to the scale of their drawings.

Kurashina, however, expressly states that its figures are not drawn to scale: “Note

that, in the various drawings of the embodiments, the various layers and members are scaled differently, not identically, so that the various layers and various members are large enough to be recognizable in the drawings.” Ex. 1008, ¶[0028].

Figures, like Kurashina’s, that are not drawn to scale are not evidence of actual proportions. *See Hockerson–Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”), *Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005) (“[A]rguments based on drawings not explicitly made to scale in issued patents are unavailing.”); *see also Innoscience (Zhuhai) Tech. Co., Ltd. v. Efficient Power Conversion Corp.*, No. IPR2023-01384, 2024 WL 1283533, at *6 (PTAB Mar. 26, 2024) (declining to construe claims to require particular, relative dimensions where specification included disclaimer “[i]t is to be understood that other embodiments may be employed and that various structural, logical, and electrical changes may be made”); MPEP § 2125 (9th ed. Rev. 07.2022) (“Proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale.”) (citing *Hockerson*).

Petitioner’s cases are further distinguishable on the basis that, unlike here, they involved drawings that showed certain proportions clearly. *E.g., In re Mraz*,

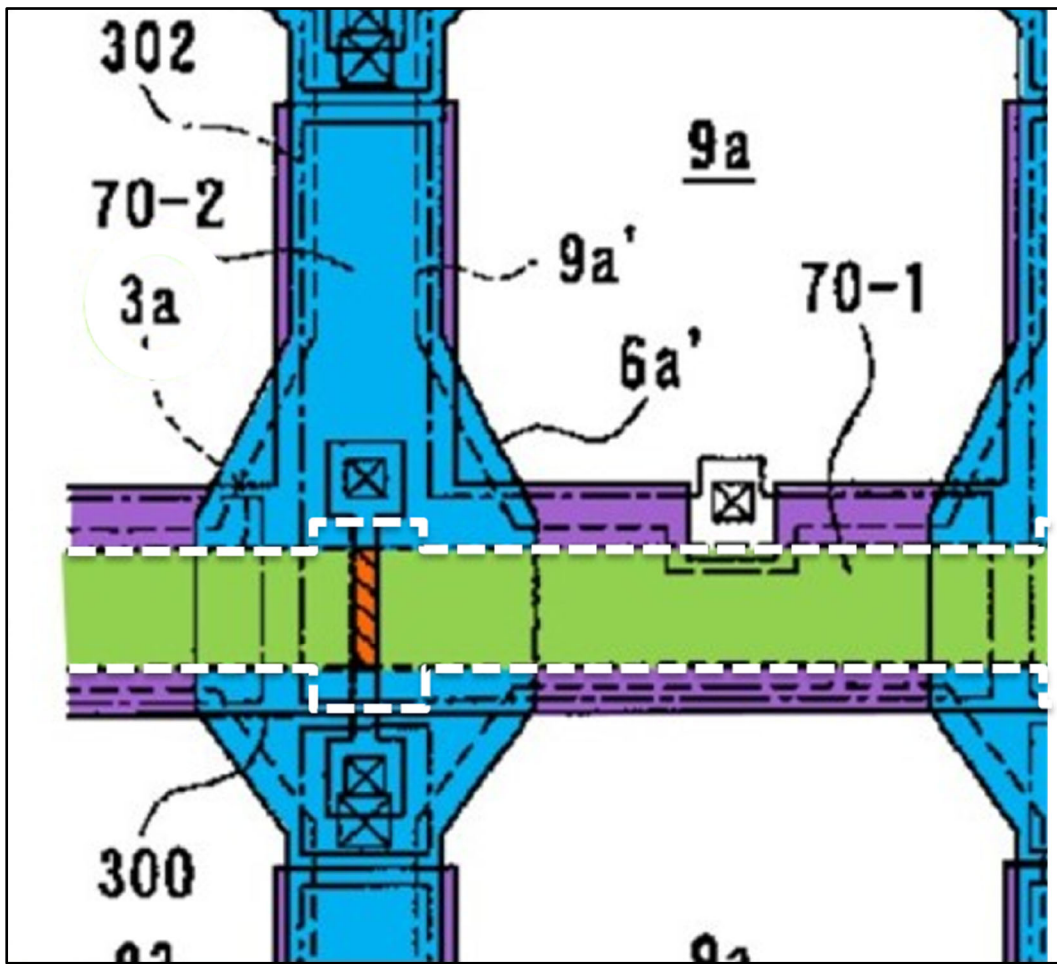
455 F.2d 1069, 1072 (C.C.P.A. 1972) (claim features shown “with great particularity”), *Micron Tech., Inc. v. Lone Star Silicon Innovations, LLC*, No. IPR2017-01561, 2018 WL 6584977, at *14 (PTAB Dec. 12, 2018) (patent figures showed contact holes “with great particularity”) (quoting *Mraz*); *see also Ex Parte Post*, Appeal No. 2020-005029, Decision on Appeal, 2021 WL 1265136 (PTAB Apr. 2, 2021) (“simple observation” of patent figure “clearly reveal[ed]” claimed diameters). Here, by contrast, Kurashina’s capacitive line is drawn only barely wider than the non-broad portion of the data line—a relative width consistent with Kurashina simply drawing the capacitive line “large enough to be recognizable in the drawings,” regardless of its actual proportions. Ex. 1008, ¶[0028]; Ex. 2001, ¶¶52-53.

Kurashina’s disclaimer about scale also undercuts the statement of Mr. Flasck, Petitioner’s expert, that a POSA would understand illustrated relative widths to convey general design information. Pet., 45. A POSA reading Kurashina in view of its express statement that different layers are drawn at different scales would reach the opposite conclusion: that relative widths do not convey general design information, but rather are drawn so as to provide visibility through different layers in plan view. Ex. 1008, ¶[0028]; Ex. 2001, ¶54.

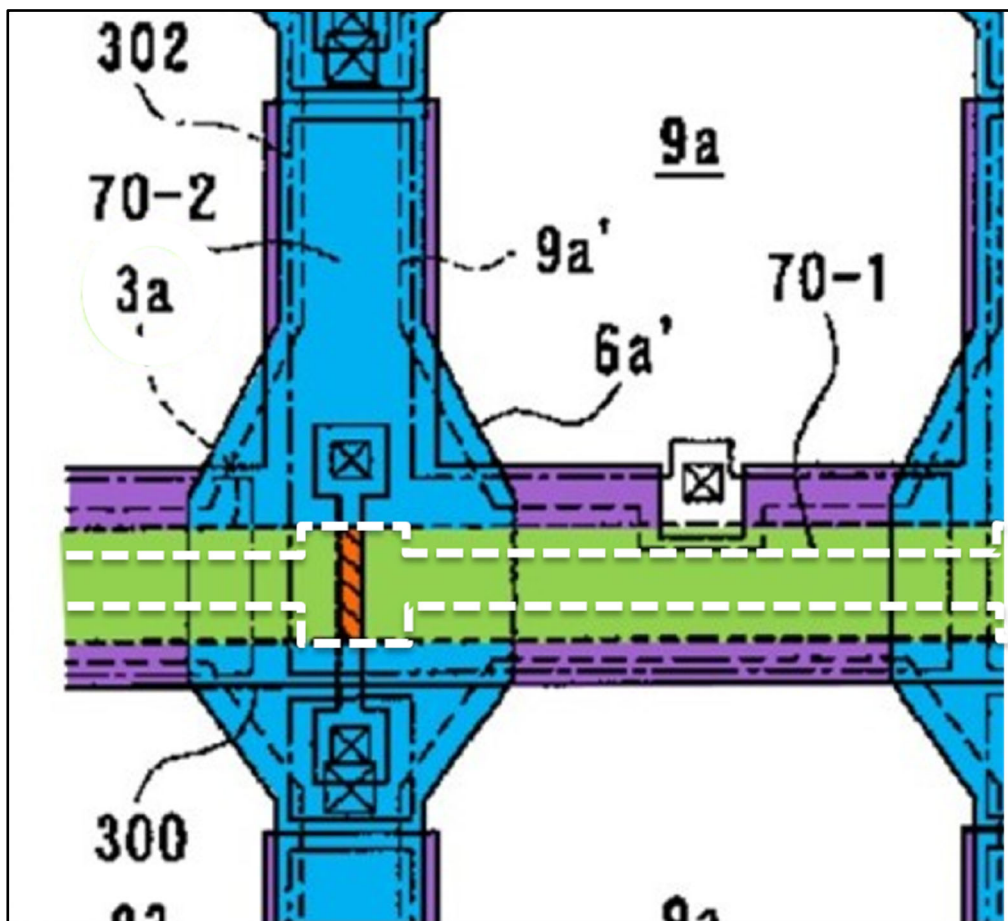
Because Kurashina's drawings are not to scale, the Petition cannot rely on those drawings to show relative sizes. The Petition therefore fails to show that Kurashina teaches this claim element.

- ii. **The Petition does not show that Kurashina in view of Sato discloses “a scanning line . . . having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.”**

The Petition further fails to show that Kurashina in view of Sato discloses “a scanning line . . . having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.” In arguing that the combination of Kurashina and Sato discloses this limitation, the Petition does not say whether a POSA would have been motivated to make the portion of the scan line facing the channel area *broader* or other portions of the scanning line *narrower*. The two possibilities are illustrated in the following two figures, where the dashed white line indicates the borders of the hypothetical scan line.



Ex. 1008, Fig. 3 (dashed white line added to show broader scan line in channel area).

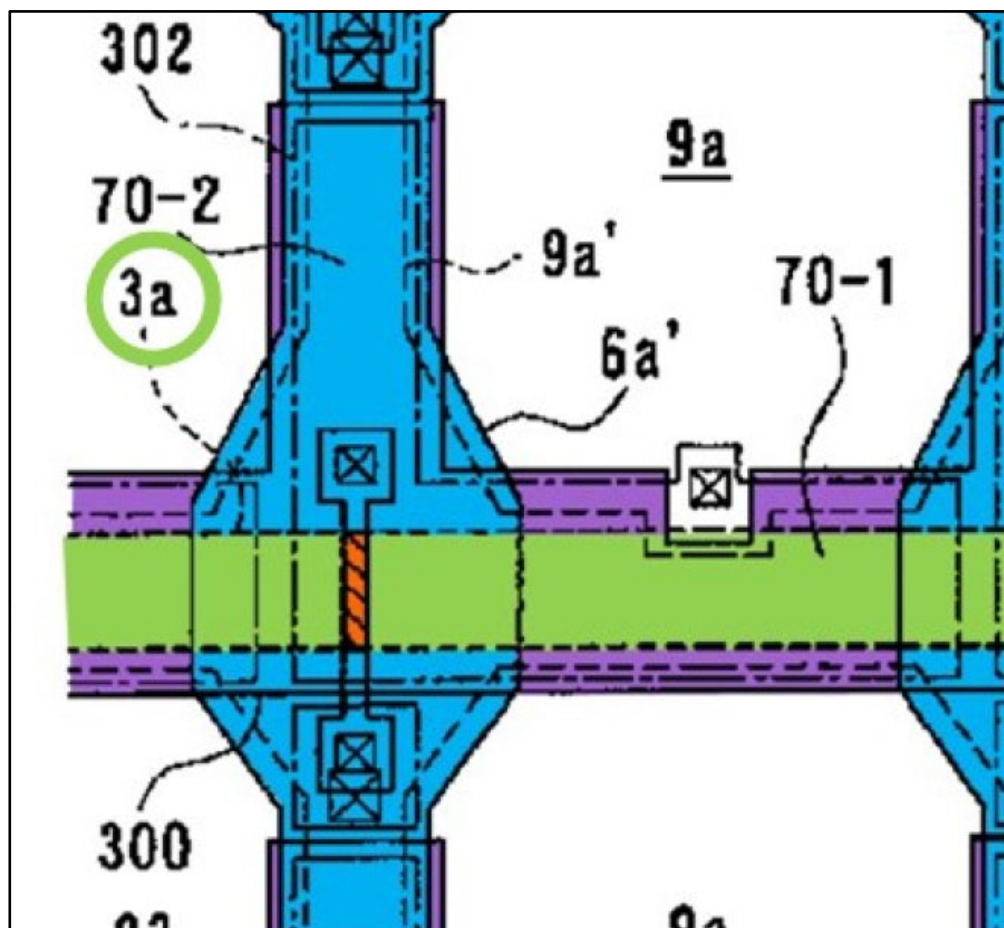


Ex. 1008, Fig. 3 (dashed white line added to show narrower scan line in areas away from channel).

Considering the two cases in turn, however, a POSA would not have been motivated to make either design change in Kurashina. A POSA would not have been motivated to make the portion of Kurashina's scan line facing the channel area broader, because Kurashina's scan line is already sized to the channel area and making it any wider would compromise device performance. And a POSA would not have been motivated to make the portion of Kurashina's scan line in areas away from the channel narrower, because doing so would increase the resistance of

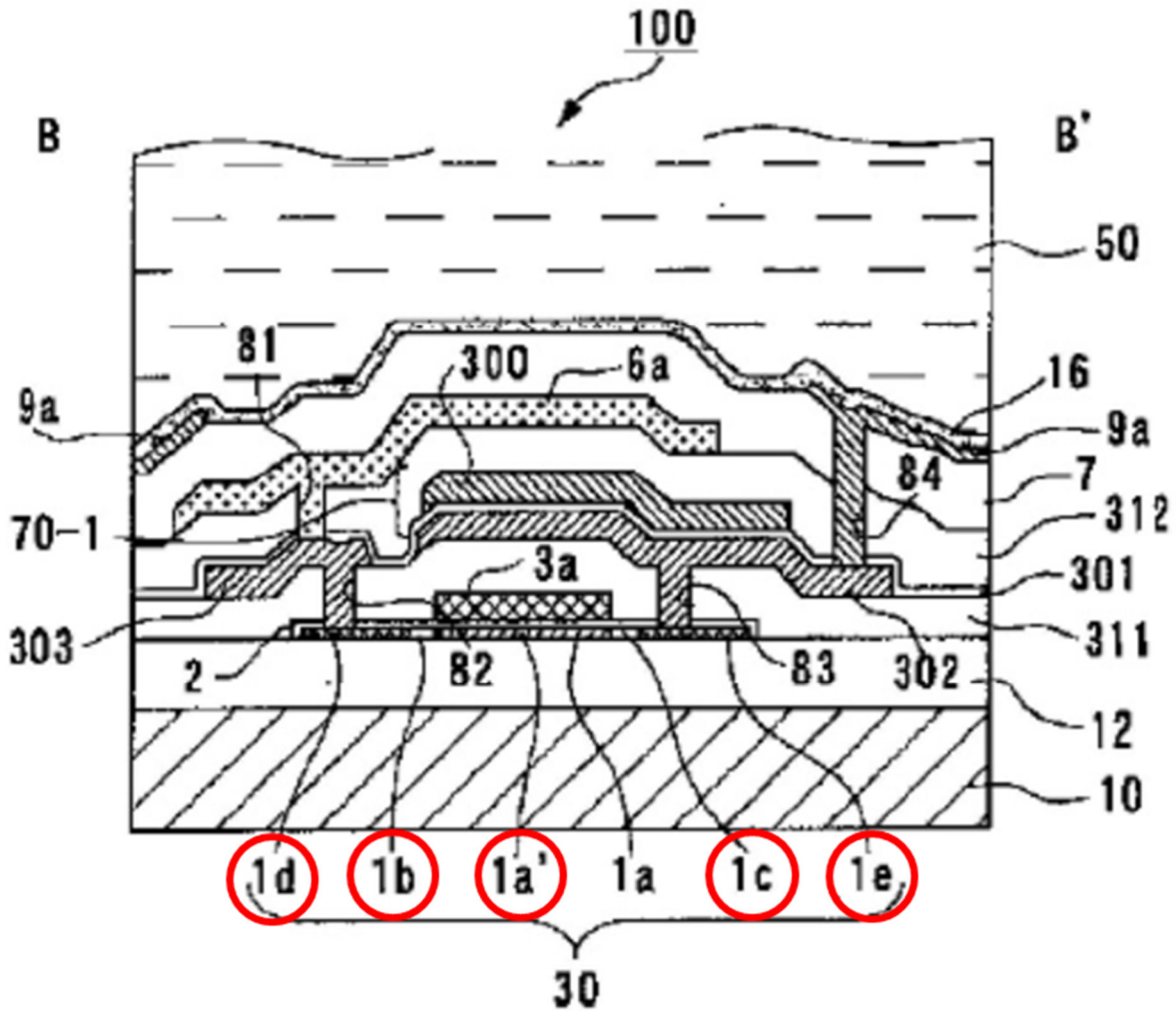
the scan line and reduce the response time of the device, while having no impact on pixel density or aperture ratio. The Petition therefore fails to show that this claim element is disclosed by Kurashina in view of Sato.

A POSA would not have been motivated to make the portion of the scan line facing the channel area broader than portions away from the channel area, as required by the claim element. As shown below in a figure reproduced from the Petition, the channel size in Kurashina (depicted by orange shading) sets the maximum width for the scan line:



Pet., 32. Neither Kurashina nor Sato discloses a scan line that is broader than the channel, and neither the Petition nor Petitioner's expert points to any reason or suggestion in those references that the scan line should be made broader than the channel. Petitioner's expert, Mr. Flasck, opines regarding Sato that "a scanning line must have [] certain minimum dimensions at the gate area, even if other portions of the scanning line are narrowed." Ex. 2001, ¶136; Pet., 35. But Sato, like Kurashina, shows a scan line only as broad as—and not broader than—the channel area. Ex. 2001, ¶¶60-61. Mr. Flasck and Petitioner therefore fail to explain why a POSA would have been motivated to make Kurashina's scan line any broader than shown.

Instead, a POSA would have recognized significant *disadvantages* to broadening Kurashina's scan line beyond the channel area. Widening the scan line would interfere with and modify the access regions of the TFTs—those regions located between the source and gate electrodes and between the gate and drain electrodes. Ex. 2001, ¶63. The access regions include lightly doped regions (source-side LDD region 1b and drain-side LDD region 1c) as well as heavily doped regions (high-density source region 1d and the high-density drain region 1e). *Id.*



Ex. 1008, Fig. 3 (annotations added).

Modifying the width of the gate electrode region (scanning line) would modify the spatial relationships of channel region 1a', source-side LDD region 1b, drain-side LDD region 1c, and heavily doped regions 1d and 1e, thereby degrading the performance of the TFT. Ex. 2001, ¶63. Kurashina teaches away from any design change that would degrade TFT performance. Kurashina describes, for instance, the importance of avoiding light-leakage current in the TFT so that "the switching

characteristics of the TFT do not change” and “a stable and sharp display screen can be obtained.” Ex. 1008, ¶[0060].

In other words, contrary to Petitioner’s suggestion that this modification would have been “simple” and “straightforward” (Pet., 38), the spatial relationships among the regions 1a’, 1b, 1c, 1d, and 1e cannot be modified (for example by widening the scan line and subsequently the gate electrode) without negatively affecting the TFT characteristics, and Kurashina teaches away from any such design change. Further, extending the scanning line would not provide any significant light-shielding benefits to hedge against this degraded performance, because the data line is already made broad over the channel area to keep light out of the TFT. Ex. 1008, ¶[0021]; Ex. 2001, ¶62.

Therefore, in addressing Kurashina in view of Sato, the Petition fails to articulate any reason to make the portion of Kurashina’s scan line that faces the channel area broader than it already is, and doing so would be contrary to the teachings of the primary reference on which the Petition relies.

Petitioner and its expert also fail to show why a POSA would have been motivated to narrow the scan line in areas away from the channel. The Petition refers to “Sato’s narrow scanning line with a wide gate,” and notes that the combination would result in “improved pixel pitch and aperture ratio.” Pet., 37-38. But while Sato has a narrow scan line at least in part to avoid the contact hole at

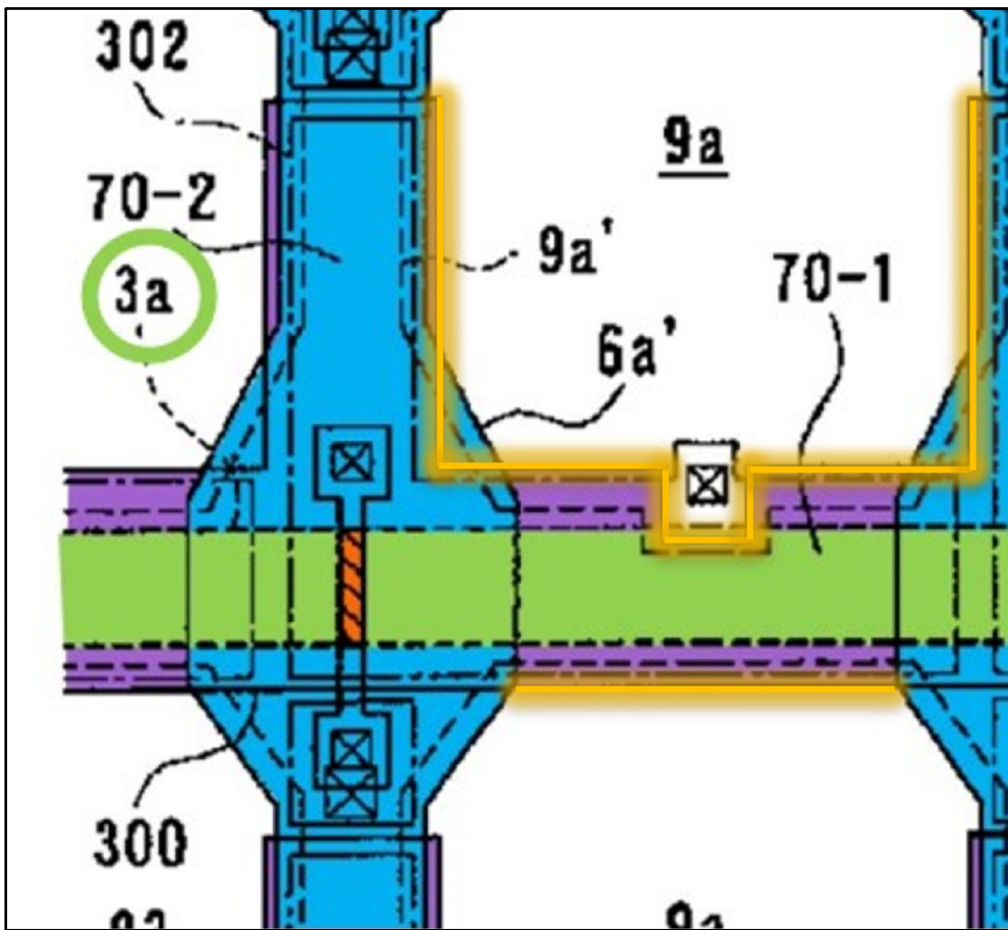
the east/west mid-point of the pixel electrode, Kurashina's corresponding contact hole is further north in the plan view, meaning that Kurashina's scanning line does not have to be narrow to avoid the contact hole. Ex. 2001, ¶65. Further, as discussed below, narrowing Kurashina's scan line in areas away from the channel would have significant disadvantages, while having no effect whatsoever on pixel pitch or aperture ratio, which are set instead by Kurashina's capacitive line.

First, a POSA would have recognized certain disadvantages in narrowing the scan line in areas away from the channel. As explained in the accompanying declaration of Dr. Schubert, narrowing the scan line would increase the resistance of the line between the TFTs. Ex. 2001, ¶66; *see also* Ex. 1001, 8:7-10 (explaining that a broader capacitive line has lower resistance). Just as less water can flow through a narrower pipe of a given length, a thinner wire has fewer electrons to carry current along a given path length. As Dr. Schubert explains, the resistance of the scanning line is inversely proportional to its width, such reducing the width of the scanning line by 50% would double the resistance of the line. Ex. 2001, ¶66. As further explained by Dr. Schubert, increasing resistance in the scanning line would in turn reduce the response time of the TFTs, which is directly proportional to the resistance. *Id.* Slower TFTs mean a slower frame rate in the device. *Id.*

Kurashina teaches away from any design changes that would reduce the response time of the TFTs. For example, Kurashina describes the importance of

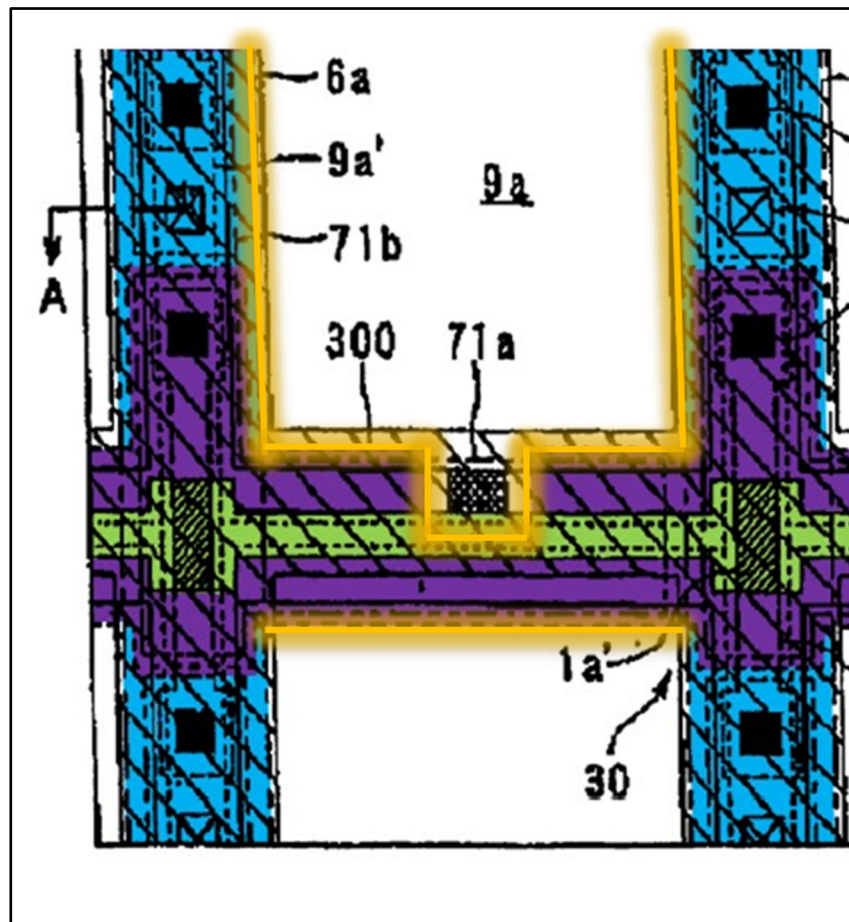
avoiding light-leakage current in the TFT so that “the switching characteristics of the TFT do not change” and “a stable and sharp display screen can be obtained.” Ex. 1008, ¶[0060]. And Kurashina is concerned more broadly with a “projection-type display device having excellent switching characteristics and a yielding a vivid image display.” Ex. 1008, ¶[0117]. Any design change that reduces the response time of the TFTs, such as reducing the width of the scanning line in areas away from the TFTs, would compromise the switching characteristics of the device, which would degrade both stability and sharpness in the display. Ex. 2001, ¶66; Ex. 1008, ¶[0060].

Finally, reducing the width of Kurashina’s scan line in areas away from the channel would not result in “improved pixel pitch and aperture ratio,” as Petitioner alleges. Pet., 38. As shown in the annotated figure below, the aperture ratio of Kurashina’s pixels is set by the protruding portion of the capacitor line (302, depicted with purple shading, with outline depicted in orange), not by the scan line (3a, depicted with green shading). Ex. 2001, ¶68. Any change to pixel pitch or aperture ratio would therefore require adjusting the width of the capacitor line, not the scan line. *Id.*



Ex. 1008, Fig. 3 (annotations added).

Similarly, the aperture ratio of the pixels in Sato is set almost entirely by the capacitor line (300) along top and bottom, and by the data lines (6a) along the sides, as depicted by the orange line below:



Ex. 1009, Fig. 2 (annotations added).

Because the pixel aperture ratio in both Kurashina and Sato is limited by the arrangement of the capacitor line rather than the scan line, nothing in those references would have motivated a POSA to reduce the width of the scan line, as doing so would not have any impact on the pixel aperture ratio. Ex. 2001, ¶70.

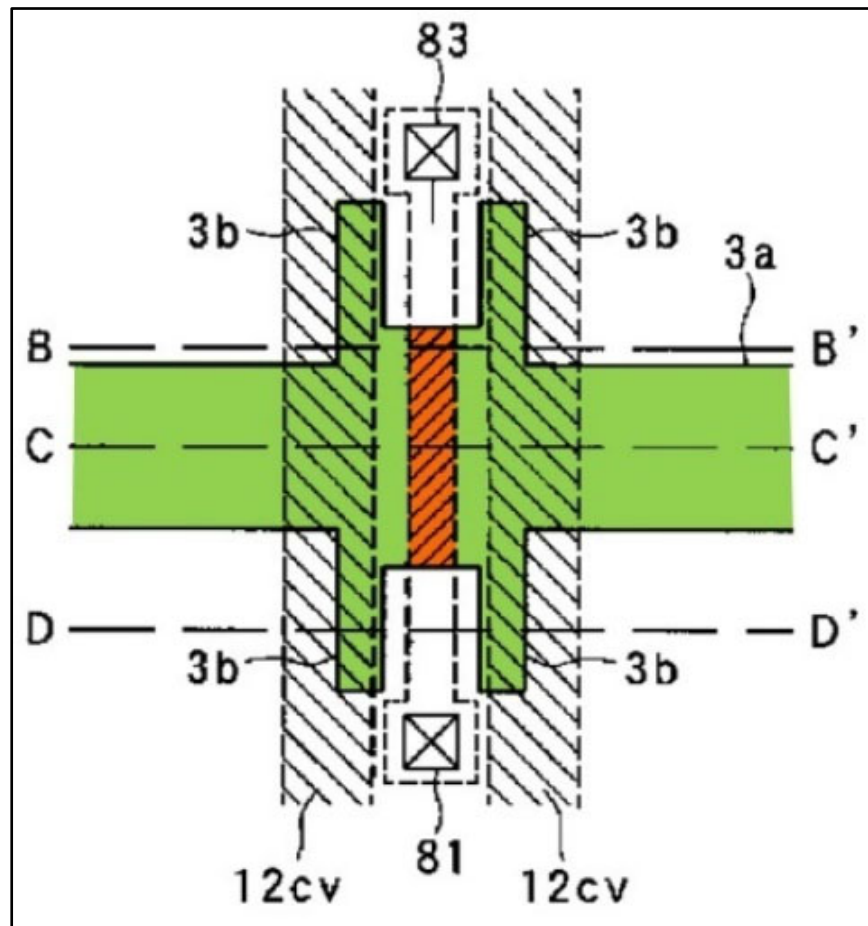
Because the Petition fails to show that a POSA would have been motivated to modify Kurashina's scan line geometry in view of Sato, it further fails to show that Kurashina in view of Sato renders obvious "a scanning line . . . having a

broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.”

iii. The Petition does not show that Kurashina in view of Takahara discloses “a scanning line . . . having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.”

The Petition also fails to show that Kurashina in view of Takahara discloses “a scanning line . . . having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.” The Petition points to two different portions of the scan line 3a in Takahara, alleging that each constitutes the claimed “broad-width portion.” Pet., 56-57. But neither of the Petition’s theories cures critical deficiencies in the purported combination of Kurashina with Takahara.

The Petition points first to Takahara’s disclosure of a “scan line 3a [] formed with a wide width at the location at which it becomes the gate electrode,” and asserts that Takahara therefore teaches the claim element. Pet., 56. But like the scan line in Sato, the wide-width portion of Takahara’s scan line that actually faces the channel area—that portion that functions as the gate electrode—is no wider than the channel area, which is depicted by orange shading in Petitioner’s annotated drawing below:

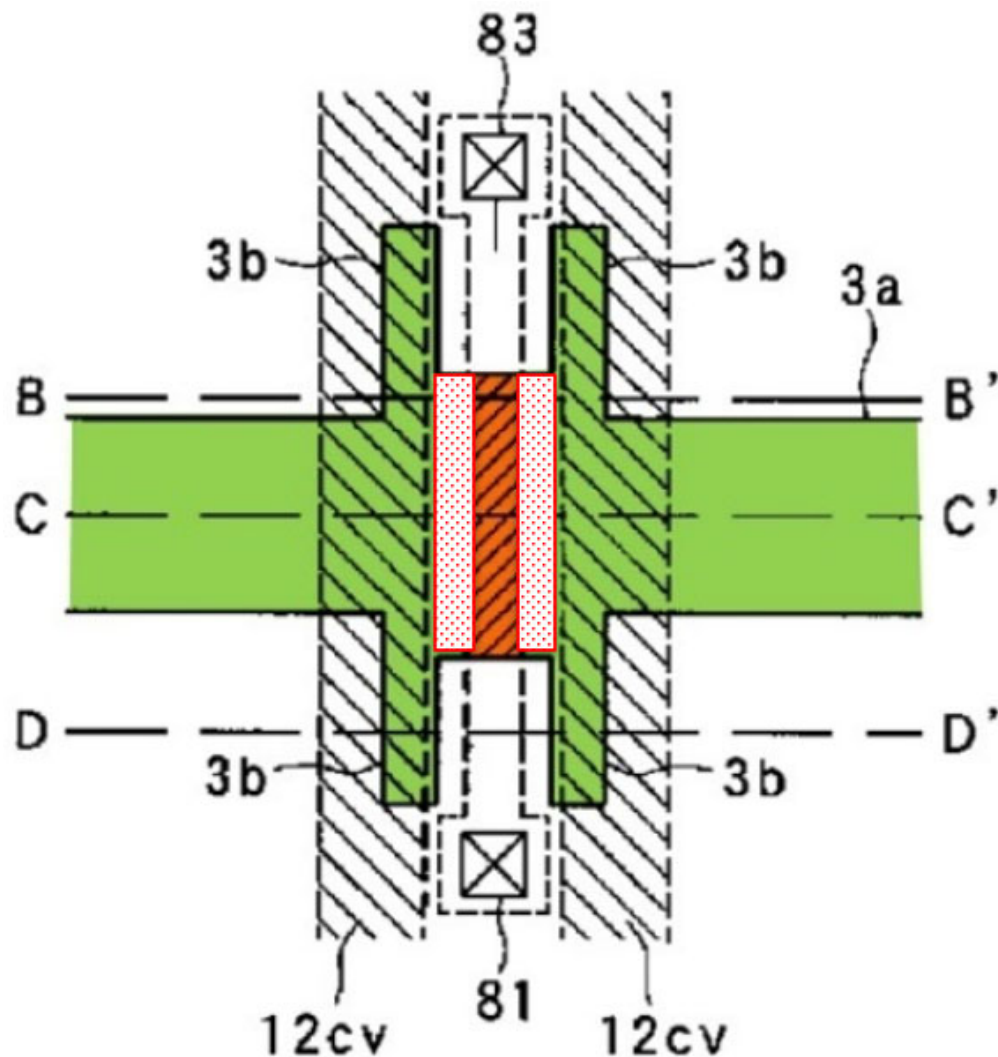


Pet., 57. Indeed, if not for the projecting portions 3b shown in the drawing (and addressed further below), Takahara's scan line would look just like that of Sato.

Because Takahara's scan line—apart from the protruding portions (addressed separately below)—otherwise has the same geometry as Sato's, Kurashina in view of Takahara fails to teach this claim element for the at least the reasons addressed in § VI.A.2.a.ii above. Neither Kurashina nor Takahara discloses a scan line that is broader than the channel in the area facing the channel, and

neither the Petition nor Petitioner's expert points to any reason or suggestion in those references that the scan line should be made broader than the channel.

The Petition then points to Takahara's disclosure of "protruding portions 3b" and asserts that they comprise another broad-width portion of the scan line facing the channel area. Pet., 57. But the Petition errs in this assertion as well, because the broad-width portions of the scan line formed by protruding portions 3b do not face the channel area, as recited by this claim element. Ex. 2001, ¶ 77. Rather, those protruding portions are *displaced* from the channel area by the segments of the scan line depicted by red hatching below:



Ex. 1010, Fig. 6 (annotations added).

Even if Kurashina's scanning line geometry were modified to have Takahara's protruding portions, the portion of Kurashina's scan line that actually faces the channel area would be no wider, because the protruding portions in Takahara do not face the channel area. Ex. 2001, ¶78. Modifying Kurashina's scan line design in view of Takahara would therefore not result in the '079 claim element, which is "a scanning line . . . having a broad-width portion in a portion facing the channel

area of the thin-film transistor and a narrow width portion in another portion.” Ex. 1001, 26:37-40 (emphasis added).

Because the Petition fails to show that a POSA would have been motivated to modify Kurashina’s scanning line geometry in view of Takahara, and further fails to show that modifying Kurashina with Takahara’s protruding portions would result in the claim element, the Petition fails to show that Kurashina in view of Takahara renders obvious “a scanning line . . . having a broad-width portion in a portion facing the channel area of the thin-film transistor and a narrow width portion in another portion.”

b. Claim 3

The Petition fails on dependent claim 3 for at least the same reasons as claim 2, as discussed in section VI.A.2.a.

c. Claim 1

- i. The Petition does not show that Kurashina discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line.”**

The Petition fails to show that Kurashina discloses this limitation for the same reasons discussed above at § VI.A.2.a.i. As compared with claim 2, this claim element recites the portion of the capacitor line extending along the data line

having a width that is “equal to or broader than a width of the data line,” rather than “narrower than the broad portion of the data line” and “wider than the non-broad portion of the data line” as recited in claim 2. But this slight difference in verbiage does not matter: Kurashina expressly states that its drawings are not to scale, so they cannot be relied on to convey any particular dimensions, including those recited here. Ex. 2001, ¶58. The Petition therefore fails to show that Kurashina discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line.”

ii. The Petition does not show that Kurashina in view of Sato or Takahara discloses “a scanning line . . . having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion.”

The Petition fails to show that Kurashina discloses this limitation for the same reasons discussed above at § VI.A.2.a.ii and iii. As noted in the Petition, as compared with claim 2, this claim element recites that the scanning line has a broad-width portion in a portion “overlapping” (instead of “facing”) the channel area and further that the overlap is “in plan view.” Again, these slight differences in verbiage do not alter the analysis from claim 2. Ex. 2001, ¶ 73. The Petition fails

to show that a POSA would have been motivated in view of Sato or Takahara to make Kurashina's scanning line broader near the channel area or narrower away from the channel area. The Petition therefore fails to show that Kurashina in view of Sato or Takahara discloses "a scanning line . . . having a broad-width portion in a portion overlapping the channel area of the thin-film transistor in plan view and a narrow width portion in another portion."

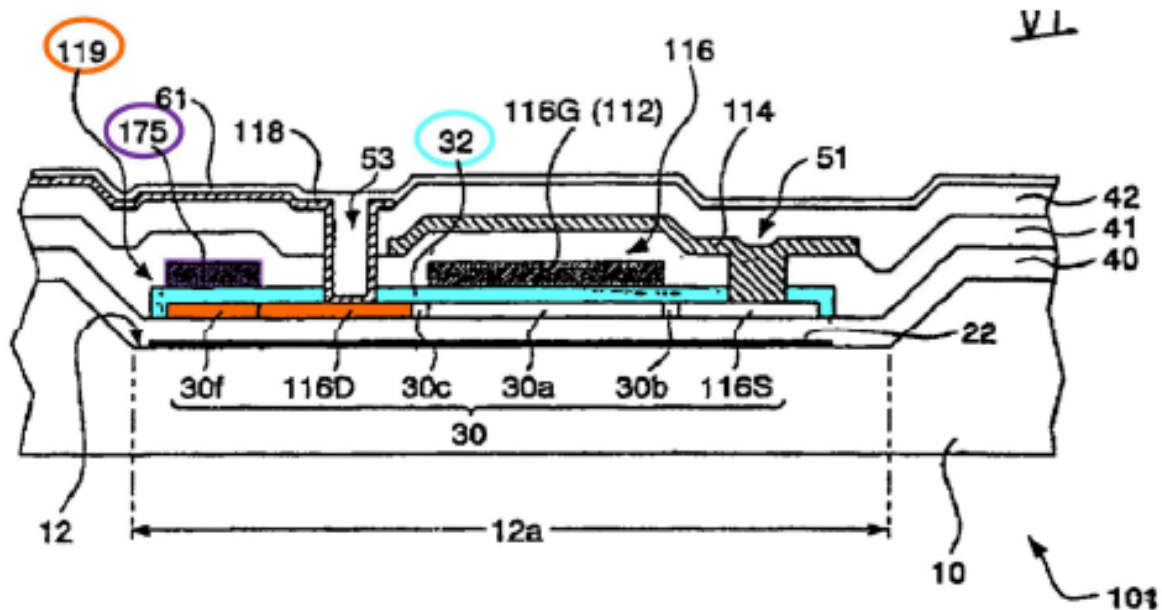
B. The Petition does not establish a reasonable likelihood that Murade-109 in view of Murade-125 renders obvious claims 1-3 (Ground 3).

1. Murade-109 and Murade-125: Overview

U.S. Pub. No. 2001/0048109A1 to Murade ("Murade-109") is primarily concerned with minimizing the difference in levels between two different surfaces of an electro-optical device substrate; this design promotes uniformity in rubbing treatment and an improved display quality. Ex. 1011, ¶¶[0009]-[0011]. Apart from teaching a standard lower light-shielding film (22) to prevent light from entering the TFT (116) from the lower side of the substrate, Murade-109 is not concerned with and does not address preventing light-induced leakage currents in the TFTs.

The annotated Murade-109 Figure 6 from the Petition, shown below, indicates several of the key structures taught. These include a pixel electrode (118), which connects directly to the heavily-doped drain region (116D) through a contact hole (53); a data line (114); a scan line (112), which forms the gate electrode

(116G); a capacitive line (175); a heavily-doped drain region (30f); and an insulating film (32). The capacitive line and heavily-doped drain region, sandwiching the insulating film (32) between them, form a storage capacitor (119) connected to the pixel electrode. Ex. 1011, ¶[0140].

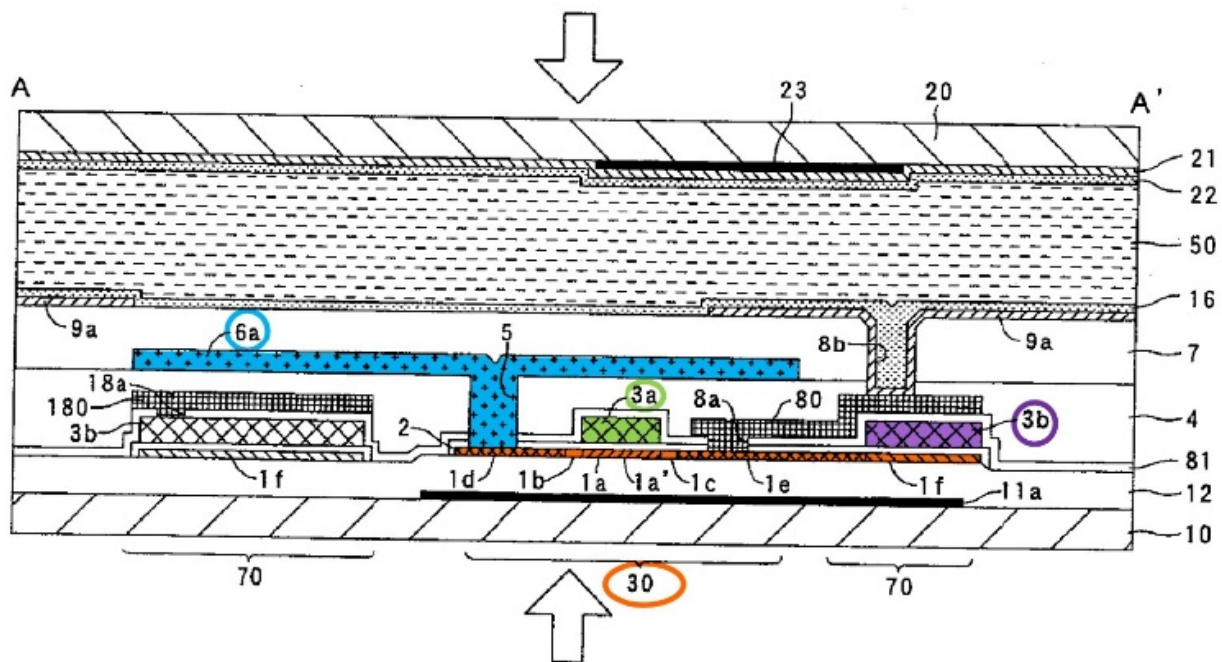


Pet., 70.

Unlike Murade-109, Murade-125 is primarily directed to solving problems caused by intermediate conductive layers, which are provided in certain electro-optical devices to improve conduction between the pixel electrode and the TFT. Ex. 1012, ¶[0001]. According to Murade-125, these intermediate conductive layers result in more layers in the overall structure and more contact holes as well, which leads to alignment irregularities and makes it more difficult to incorporate storage capacitors into the device design. *Id.*, ¶[0005]. Murade-125 teaches connecting the

pixel electrode to the drain region of the semiconductor layer via an intermediate conductive layer, which establishes a good connection using comparatively small contact holes; these smaller contact holes in turn facilitate a larger pixel aperture ratio. *Id.*, ¶[0008].

The annotated Murade-125 Figure 3 from the Petition, shown below, indicates several of the key structures taught. These include a pixel electrode (9a), which connects to the drain region (1e) via a first intermediate conductive layer (80) and contact hole (8a); a data line (6a); a scan line (3a), which forms a gate electrode; a capacitive line (3b); a capacitor electrode (1f) extending from the drain region (1e); a second intermediate conductive layer (180); and first and second interlayer insulating films (81, 2). The capacitor electrode (1f), capacitive line (3b), and second intermediate conductive layer (180), sandwiching the two interlayer insulating films (81, 2), form a large storage capacitor (70).



Pet., 78.

The design of Murade-109 differs substantially from Murade-125 at least in that Murade-109 does not disclose an intermediate conductive layer. While the pixel electrode in Murade-125 connects to the drain via the first intermediate conductive layer 80, the pixel electrode in Murade-109 connects directly to the drain, as previously described, rather than through an intermediate conductive layer.

2. The Petition fails to show that Murade-109 discloses all limitations of any challenged claim.

a. Claim 2

- i. The Petition does not show that Murade-109 in view of Murade-125 discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the**

data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

The Petition fails to show that Murade-109 in view of Murade-125 discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.” A POSA would not have been motivated to widen the capacitive line of Murade-109 in view of any teaching in Murade-125. Further, even if a POSA had widened the capacitive line of Murade-109, they would not have made it broader than the non-broad portion of the data line because the semiconductor layer 30 in Murade-109—the mating electrode for the capacitor line—is itself narrower than the non-broad portion of the data line. The Petition fundamentally misinterprets the teachings of Murade-125 and their applicability to Murade-109 in arguing otherwise. Specifically, the Petition contends that Murade-125 teaches widening the capacitive line relative to the data line for two reasons: (1) to attenuate multiply reflected light caused by internal reflection, and (2) to construct a larger storage capacitor using the capacitor electrode and intermediate conductive layer. Pet., 76. But the Petition is simply

incorrect regarding reason (1), and reason (2) does not apply to Murade-109 and does not result in the claim element.

Regarding reason (1), Murade-125 nowhere teaches making the capacitive line wider than the data line to attenuate multiply reflected light. Instead, Murade-125 teaches making the *intermediate conductive layer* wider than the data line to achieve this two-fold light-shielding purpose: according to Murade-125, the two shielding layers are the data line and the intermediate conductive layer, not the data line and the capacitive line. Murade-125 first discloses the configuration $W_d < W_c < W_m$ at ¶[0041]. Murade-125 then immediately explains that “[a]ccording to this configuration, it becomes possible to provide two-fold shielding against incident light from the opposing substrate [] using the data line and *the intermediate conductive layer*.” Ex. 1012, ¶[0042] (emphasis added). Murade-125 goes on to explain that the intermediate conductive layer is “formed from a low-reflective, high-melting-point metal film or a polysilicon film, thus making it possible to adopt a configuration that attenuates multiply reflected light as described above.” *Id.* And Murade-125 later states that

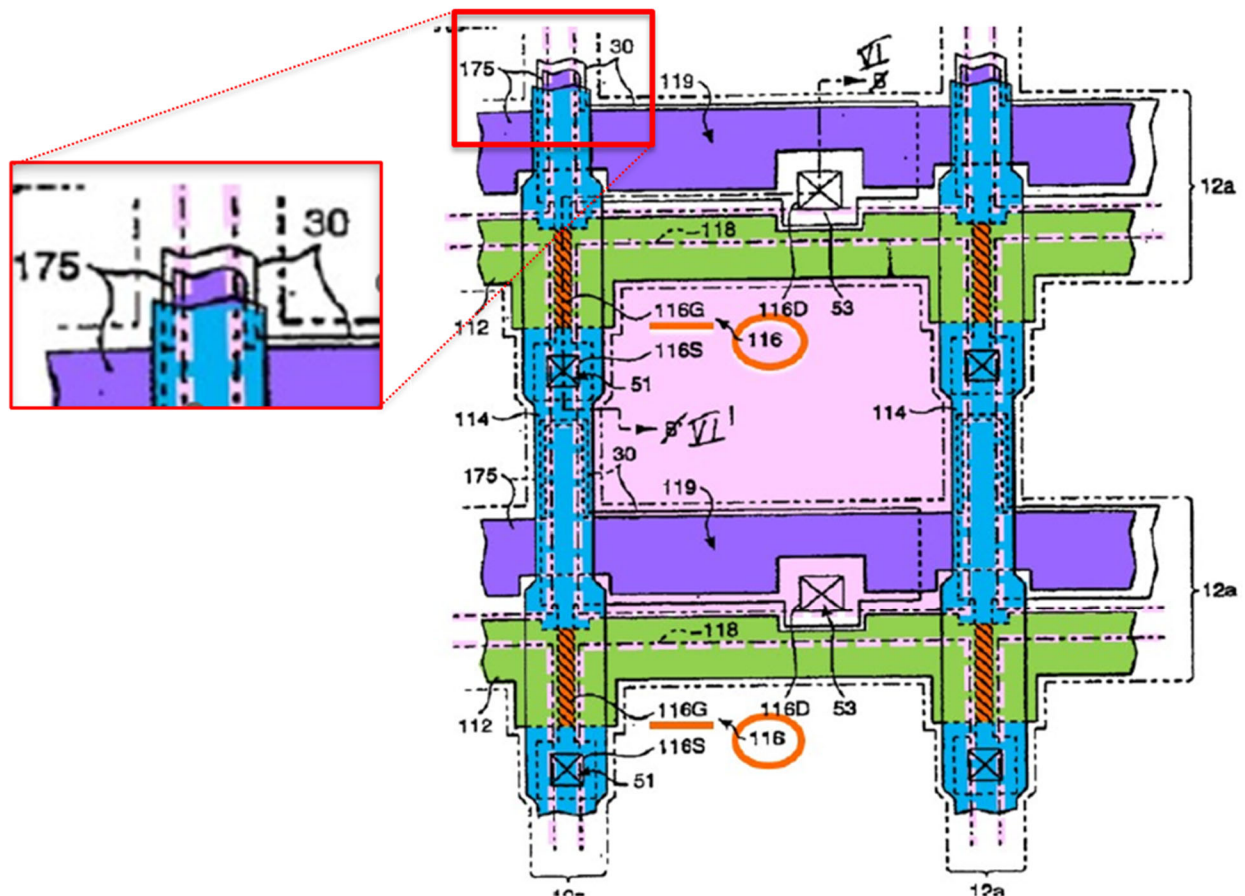
multiply reflected light resulting from internal reflection as described above can be attenuated by forming the first intermediate conductive layer 80 and the second intermediate conductive layer 180 from a low reflectivity refractive metal film or from a polysilicon film, and by

forming the second intermediate conductive layer 180 so as to be wider than the data line 6a ($W_d < W_m$).

Id., ¶ [0094]. Murade-125 therefore teaches using the intermediate conductive layer(s) for improved light shielding. Murade-125 nowhere discloses using the capacitive line as a light shielding layer. The Petition is simply wrong in asserting that Murade-125 teaches widening the capacitive line to attenuate reflected light.

As to reason (2), that a “larger storage capacitor can be constructed using the capacitor electrode and the intermediate conductive layer” (Pet., 76), this logic does not apply to Murade-109 and therefore would not motivate a POSA to modify Murade-109 in any way. As discussed at § VI.B.1, *supra*, Murade-109 does not disclose an intermediate conductive layer. For this reason alone, a POSA would not have been motivated to modify the capacitive line in Murade-109 to create a larger capacitor: it would be impossible to make a larger storage capacitor in Murade-109 out of a capacitive line and an intermediate conductive layer when Murade-109 does not disclose the latter layer.

Further, even if a POSA did broaden the capacitive line in Murade-109, this would not result in the claim element. As shown in Figure 5 of Murade-109, both the protruding portion of the capacitor line 175 and the semiconductor layer 30 are narrower than the non-broad portion of the data line 114:



Ex. 1011, Fig. 5 (annotations and callout added).

Therefore, even if the capacitor line 175 in Murade-109 were broadened to be the same width as the semiconductor layer 30 (the mating electrode in Murade-109), it would still be narrower than the non-broad portion of the data line 114, and the claim limitation “the portion [of the capacitor line] extending along the data line having a width that is . . . wider than the non-broad portion of the data line” would not be met.

Further, a POSA would not have been motivated to broaden the capacitor line beyond the width of the semiconductor layer. This design change would not provide any more capacitance in Murade-109 because capacitance comes only from the regions of the capacitor line and semiconductor layer 30 that overlap. Ex. 2001, ¶98. Indeed, both the Petition and Petitioner's expert make this same point in arguing that a POSA would not have been motivated to make the capacitor line projection wider than the broad portion of the data line. Ex. 2001, ¶98; Pet., 76-77. Yet both Petitioner and its expert fail to apply the same logic in considering areas of the device containing the non-broad portions of the data line, erroneously concluding that a POSA would have been motivated to make Murade-109's capacitor line broader in those regions. Ex. 2001, ¶98. Here, making the capacitor line in Murade-109 broader than the semiconductor layer 30—its “mated electrode”—would provide no additional capacitance, and a POSA therefore would not have been motivated to make this design change in Murade-109. *Id.*

Finally, a POSA would not have been motivated to make the semiconductor layer 30 in Murade-109 broader in accordance with the capacitor line 175. While broadening the intermediate conductive layer (and capacitor line) beyond the data line in Murade-125 provided light shielding benefits, the same does not translate to Murade-109. A broader semiconductor layer 30 would not provide any light shielding—indeed, it is the semiconductor layer itself that must be shielded from

stray light to reduce light-induced leakage currents. Ex. 2001, ¶99. Further, broadening the semiconductor layer 30 would increase its area, which would make it even more susceptible to stray light and the light-induced leakage currents that result. *Id.* Again, in view of the incompatibility in designs between Murade-109 and Murade-125, even if a POSA did modify Murade-109 by widening the capacitor line, they would not have arrived at the claim element because they would not have had any reason to make the capacitor line broader than the data line. *Id.*

At best, then, Murade-125 teaches (1) shielding light that reflects off the data line by using a wider intermediate conductive layer, and (2) making a larger storage capacitor by widening both the intermediate conductive layer and the capacitor line relative to the data line. Ex. 1012, ¶[0042]. But to the extent these teachings of Murade-125 improve device performance, as the Petition alleges (Pet., 76), those improvements would not extend to Murade-109. Ex. 2001, ¶100. The two references are incompatible because Murade-109 does not have an intermediate conductive layer. *Id.* Because Murade-109 would not realize the benefits of any design change based on Murade-125, a POSA would not have been motivated to carry these aspects of Murade-125's design over to Murade-109. *Id.* And even if a POSA did broaden the capacitor line in Murade-109 to increase capacitance, it would not result in the claim element because the capacitor line

would still be narrower than the non-broad portion of the data line, as shown in Figure 5 of Murade-109, above. *Id.*, ¶101.

The Petition therefore fails to show that Murade-109 in view of Murade-125 discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is narrower than the broad portion of the data line and that is wider than the non-broad portion of the data line.”

b. Claim 3

The Petition fails on dependent claim 3 for at least the same reasons as claim 2, as discussed in § VI.B.2.a.

c. Claim 1

- i. The Petition does not show that Murade-109 in view of Murade-125 discloses “a capacitive line . . . having a portion extending along the scanning line and a portion extending along the data line, the portion extending along the data line having a width that is equal to or broader than a width of the data line.”**

The Petition fails to show that Murade-109 in view of Murade-125 discloses this limitation for the same reasons discussed above at § VI.B.2.a. As compared with claim 2, this claim element recites the portion of the capacitor line extending along the data line having a width that is “equal to or broader than a width of the data line,” rather than “narrower than the broad portion of the data line” and “wider

than the non-broad portion of the data line” as recited in claim 2. But as with Grounds 1 and 2, the slight difference in verbiage between the claims makes no difference here. Ex. 2001, ¶104. A POSA reading Murade-109 in view of Murade-125 would not have been motivated to widen the capacitor line, let alone make it as broad as or broader than the non-broad portion of the data line in Murade-109, for the reasons discussed at § VI.B.2.a. Therefore, a POSA would not have been motivated to make the capacitor line in Murade-109 “equal to or broader than a width of the data line.”

VII. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. § 314 AND *FINTIV*

The Board should exercise its discretion to deny the Petition under *Fintiv* and the Director’s Interim Guidance.¹ The *Fintiv* factors weigh against institution:

- The United States District Court for the Eastern District of Texas has not stayed the parallel proceedings. And no evidence suggests that the district court would grant a stay were the Board to institute; three of six patents-in-suit are not subject to *inter partes* review proceedings.

See AGIS Software Development LLC v. Google LLC, 2:19-CV-

¹ K. Vidal, INTERIM PROCEDURE FOR DISCRETIONARY DENIALS IN AIA POSTGRANT PROCEEDINGS WITH PARALLEL DISTRICT COURT LITIGATION (June 21, 2022), https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

00361-JRG, 2021 WL 465424, at *2 (E.D. Tex. Feb. 9, 2021) (“It has been this Court’s consistent and long established practice to deny motions to stay pending IPR and EPR when the PTAB or PTO have instituted review on less than all asserted claims of all asserted patents because at least one or more originally asserted claims will be unaffected by the outcome of those parallel proceedings and left intact before this Court to be tried.”). Investment in the district court proceedings is ongoing.

- Trial in the district court proceedings will take place on June 2, 2025, more than six months before the Board’s Final Written Decision deadline. Ex. 1022. Median time from filing to trial in the district is 21.6 months as of June 2024, which would push trial only to August 2025, as the Petition notes.² The district court is, under the issued trial date and the estimated time-to-trial, expected to try this case before the Board’s Final Written Decision deadline.
- Issues before the Board are substantially the same as those before the district court. Claim 1 is the only independent claim that is challenged here and not asserted in the district court, and claim 1 is substantially

² https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0630.2024.pdf.

similar to asserted independent claim 2. Petitioner has not submitted a *Sotera* stipulation.

- The Petition has not demonstrated a reasonable likelihood of success, much less a compelling likelihood of success. And the other factors weigh in favor of dismissal. *See CommScope Techs. LLC. v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4 (February 27, 2023) (Precedential) (“I intended for PTAB panels to only consider compelling merits if they first determined that *Fintiv* factors 1–5 favored a discretionary denial.”).

VIII. CONCLUSION

The Petition does not establish a reasonable likelihood that any of the challenged claims are unpatentable. The Board should deny institution.

IPR2024-00976
U.S. Patent No. 7,502,079

Date: September 20, 2024

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

I certify that this Patent Owner's Preliminary Response complies with the word count limit and contains 8,194 words in 14-point Times New Roman font as calculated by the word count feature of Microsoft Office, in compliance with 37 C.F.R. § 42.24(a)(1)(i). This word count is inclusive of all text and footnotes but does not include the table of contents, table of authorities, certificate of service or word count, or appendix of exhibits or claim listing.

Date: September 20, 2024

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CERTIFICATE OF SERVICE

I certify that on September 20, 2024, a copy of Patent Owner's Preliminary Response, including exhibits, was served in its entirety by electronic mail to Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

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