

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

Case No. IPR2024-00977

U.S. Patent No. 9,557,606

**DECLARATION OF ALEX Z. KATTAMIS, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,557,606**

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I. INTRODUCTION

1. I, Dr. Alex Kattamis, submit this declaration to state my opinions on the matter described below. I am over the age of 21 and am competent to make this declaration.

2. I have been retained by counsel for BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”), as an independent expert in this proceeding before the United States Patent and Trademark Office (“USPTO”). I am a salaried employee of Exponent. Exponent charges \$550 per hour for my time plus expenses for work performed in connection with this project, and I am being paid my regular salary for time spent on this project. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case. I have no other interest in this proceeding.

3. I understand that this proceeding involves U.S. Patent No. 9,557,606 (“’606 patent”), and I have been asked to provide my opinions as to the patentability of the claims of the ’606 patent. I understand the application for the ’606 patent was filed on December 16, 2014, and claims priority to an earlier U.S. priority document filed December 12, 2005, and a foreign priority document having a filing date of December 27, 2004.

4. I have been asked to consider the patentability of the claims of the '606 patent based on certain prior art references. I have also been asked to consider the state of the art and prior art available as of December 27, 2004. Based on the prior art discussed in this declaration, it is my opinion that claims 7-13 and 15-20 of the '606 patent are unpatentable for the reasons provided below.

II. EXPERIENCE AND QUALIFICATIONS

5. I believe that I am well qualified to serve as a technical expert in this matter based upon my educational and work experience, and specifically, flat panel display devices, including liquid crystal displays.

6. I received my B.A. in Electrical Engineering from the University of Connecticut in 2002. I received an M.A. and Ph.D. in Electrical Engineering from Princeton University in 2004 and 2007, respectively.

7. At Princeton University my research was focused on designing and fabricating pixel circuits on non-conventional substrates for driving liquid-crystal display and active-matrix organic light emitting diode displays (AMOLEDs). This included the application of semiconductor fabrication techniques including PE-CVD, CVD, and photo-lithography. My work also included the development of nanocrystalline silicon TFTs, which attempted to overcome metastability issues found in traditional amorphous silicon TFTs. I also designed pixel circuits for use in

electrophoretic displays along with the development of the drivers necessary to operate a fully functional display.

8. I am a Principal Engineer in Exponent's Electrical Engineering and Computer Science practice. Throughout my career at Exponent, I have worked extensively on AMOLED and AMLCDs, including driver circuits, and thin-film transistor and pixel architectures. This has included the design of TFT backplanes, waveguides and driver electronics for small and large format displays.

9. I have authored or co-authored 30 articles or conference presentations, including numerous papers and presentations concerning lighting and display technologies. My curriculum vitae (Ex. 1003) lists these articles and conference presentations. Of particular interest may be the following:

- a. Hekmatshoar B, Kattamis AZ, Cherenack K, Wagner S, Sturm JC. A novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels. J Soc Info Disp 2008; 16.
- b. Hekmatshoar B., Kattamis AZ, Cherenack KH, Long K, Chen J-Z, Wagner S, Sturm JC, Rajan K, Hack M. Reliability of active-matrix organic light-emitting-diode arrays with amorphous silicon thin-film transistor backplanes on clear plastic. IEEE Elec Dev Lett 2008; 29.

- c. Kattamis AZ, Giebink N, Cheng I-C, Hong Y, Cannella V, Forrest SR, Wagner S. Active-matrix organic light emitting display employing two thin film transistor a-Si:H Pixels on flexible stainless steel foil. J Soc Info Disp 2006; 15:433-437.
- d. Kattamis AZ, Cheng I-C, Long K, Hekmatshoar B, Cherenack K, Wagner, S, Sturm JC, Venugopal S, Loy DE, O'Rourke SM, Allee DR. Amorphous silicon thin film transistor backplanes deposited at 200°C on clear plastic. IEEE J Disp Tech 2006; 2:304-308.
- e. Hekmatshoar B, Cherenack K, Long K, Kattamis AZ, Wagner S, Sturm JC. AMOLED reliability with a-Si TFT's in normal vs. inverted TFT/OLED integration scheme. 66th Dev Res Conf 2008; 243-244.
- f. B. D'Andrade and A.Z. Kattamis, "*Flexible active-matrix organic light emitting displays*," Silicon Valley Engineering Council J 2009; 1:18-21.
- g. B. Hekmatshoar, A.Z. Kattamis, et al., "*Highly stable amorphoussilicon thin-film transistors on clear plastic*." Appl Phys Lett 2008; 93:032103-1-3.

10. Since 2013, I have served as an expert witness in several patent disputes (district court cases, ITC hearings, IPRs and PGRs). Most of these matters involved LCD, active matrix, and/or flat panel displays. I have testified in district court and before the ITC.

11. I am a licensed Professional Engineer in the State of Connecticut, the State of Georgia, the Commonwealth of Massachusetts, the State of New Jersey, the State of New York, the Commonwealth of Pennsylvania, the State of Rhode Island, and the State of Texas. I am also designated a Model Law Engineer by the National Council of Examiners for Engineering.

12. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), which is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.

13. Based on my education, professional experience, scholarly books and publications, I am an expert in the relevant field of the '606 patent and have been an expert in this field since before the earliest claimed priority date of the '606 patent. I am familiar with how a person having ordinary skill in the art (what I will call the "POSITA" later) would have understood and used the terminology found in the '606 patent as of its earliest claimed priority date.

III. MATERIALS CONSIDERED

14. In forming my opinions, I reviewed the '606 patent, its prosecution history and references cited by the Examiner during prosecution, the materials cited in the List of Exhibits below, and the materials cited throughout my declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,557,606 ("the '606 patent")

Exhibit	Description
Ex. 1002	File History of U.S. Patent No. 9,557,606
Ex. 1005	U.S. Patent Application Publication No. 2003/0174271 to <i>Fujikawa</i> (“ <i>Fujikawa</i> ”)
Ex. 1006	U.S. Patent Application Publication No. 2004/0257504 to Kang et al. (“ <i>Kang</i> ”)
Ex. 1007	JP 2003-280030 to Ikeguchi
Ex. 1008	Certified Translation of JP 2003-280030 to Ikeguchi (“ <i>Ikeguchi</i> ”)
Ex. 1009	U.S. Patent No. 7,138,304 to Hirai
Ex. 1010	U.S. Patent No. 6,930,745 to Miyazaki et al. (“ <i>Miyazaki</i> ”)
Ex. 1011	U.S. Patent Application Publication No. 2005/0122466 to Tanaka et al. (“ <i>Tanaka</i> ”)
Ex. 1012	U.S. Patent No. 7,235,415 to Mikoshiba
Ex. 1013	Kamiya, Hiroyuki et al., “ <i>Development of One Drop Fill Technology for AM-LCDs</i> ,” 1354 SID 01 Digest 56.3 (2001)
Ex. 1014	Yamada, S. et al., “ <i>A New Production of Large size TFT-panel by ‘LC-Dropping Method,’</i> ” 1350 SID 01 Digest 56.2 (2001)
Ex. 1015	Wright, Stephen L., “ <i>IBM 9.2-Megapixel Flat-panel Display: Technology and Infrastructure</i> ,” IBM Research Report, RC22363 (W0203-023) (March 8, 2002)
Ex. 1016	den Boer, Willem, “ <i>Active Matrix Liquid Crystal Displays, Fundamentals and Applications</i> ” (2005)
Ex. 1017	U.S. Patent No. 6,466,294 to Yamagishi et al.
Ex. 1018	U.S. Patent No. 6,724,448 to Nakahara

Exhibit	Description
Ex. 1019	Excerpts from Exhibit F1, Longitude Licensing Limited's Infringement Contentions Chart for U.S. Patent No. 9,557,606 in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP (E.D. Tex.)
Ex. 1024	Certified Translation of JP 2004-226654 to Iwai
Ex. 1025	JP 2004-226654 to Iwai

IV. LEGAL STANDARDS

15. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

16. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

17. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

18. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 7-13 and 15-20 of the '606 patent from the perspective of a person of ordinary skill in the art at the '606 patent's earliest claimed priority date in 2004, as described in more detail below.

19. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means "more likely than not."

20. In forming my opinions and considering the subject matter of the '606 patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

21. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims.

22. I understand that a claimed invention is only patentable when it is new, useful, and non-obvious in light of the "prior art." That is, the invention, as defined by the claims of the patent, must not be anticipated by or rendered obvious by the prior art.

A. Level of Ordinary Skill in the Art

23. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

24. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Claim Construction

25. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of one of ordinary skill in the art at the time of the alleged invention.

26. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claim terms are generally not limited by the embodiments described in the specification.

27. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

C. Prior Art

28. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

D. Anticipation

29. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have

been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

E. Obviousness

30. I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

31. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

32. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to

assume that the date of invention for the December 27, 2004. My opinions would not change if I assumed a later date of invention.

33. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

34. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

35. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of

success—in achieving the claimed invention by combining prior art references.

36. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

37. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in

the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

38. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

39. I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '606 patent.

40. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. OVERVIEW OF TECHNOLOGY

A. The Liquid Crystal Display (“LCD”)

41. A liquid-crystal display (“LCD”) consists of a liquid-crystal (“LC”) layer separated by two electrodes. *See, e.g.*, ’606 patent at 1:23-27 (explaining that liquid crystal devices typically comprise “a pair of substrates with a liquid crystal layer interposed therebetween”) Depending on the electrical potential applied across the LC via these electrodes, light is blocked or transmitted. There are two dominant methods to address the pixels in LCDs: passive matrix and active matrix.

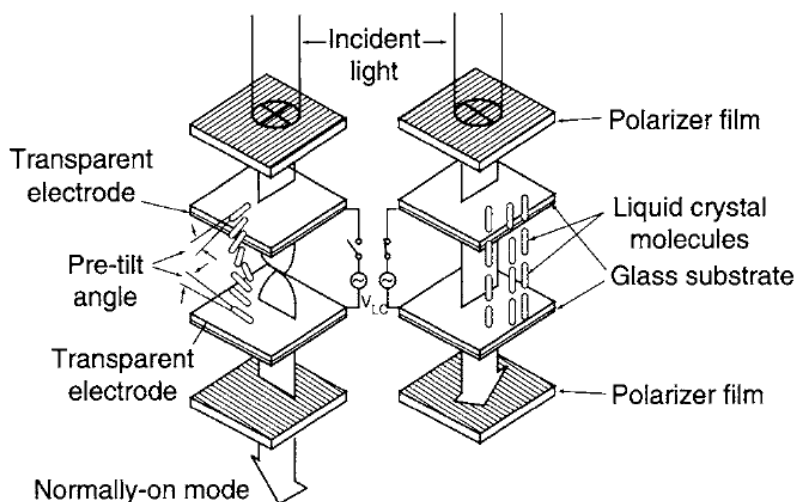


Figure 1.10: Operation of twisted nematic (TN) LC cell.

See Ex. 1016¹ at 22, Fig. 1.10.

¹ Citations for the exhibit are to the page numbers stamped in the exhibit.

1. Passive Matrix LCDs

42. In passive matrix LCDs, each pixel is connected to a data electrode and a scan electrode. This sets the voltage across the LC at each individual pixel:

To obtain LCDs with more picture elements (or pixels), a matrix approach is used. In passive matrix LCDs, the conductive transparent electrodes are patterned as stripes perpendicular to each other on the two opposing substrates (Fig. 1.13). This allows a dot matrix with M rows and N columns (i.e., MxN pixels), to be addressed by M+N external connections. The price to pay for this approach is that the voltage across each pixel is no longer independently controlled. At any time, only one row of pixels is selected and receives data from the column drivers. The data information supplied to the other rows of pixels can, however, modify the average voltage on the pixel.

See Ex. 1016 at 24.

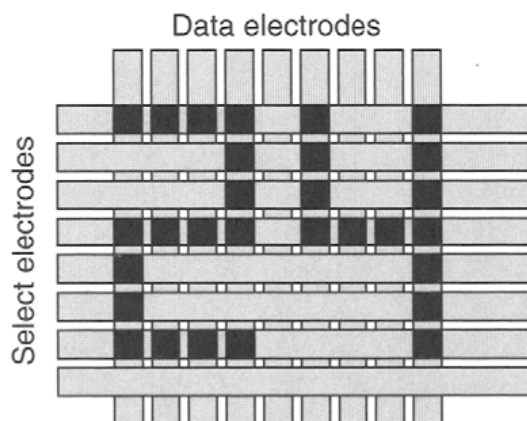


Figure 1.13: Passive matrix addressing.

See Ex. 1016 at 25, Fig. 1.13.

2. Active Matrix LCDs and Thin Film Diodes

43. Active matrix LCDs (“AMLCDs”) add a semiconductor switch to each pixel. This allows the voltage to be set at each pixel. *See* Ex. 1016 at 29 (“By adding a semiconductor switch at each pixel, the drawbacks of multiplexing in a passive matrix are eliminated. In the active matrix configuration, the voltage at each pixel and therefore its transmission and gray level can be accurately controlled.”).

44. Thin film diodes (i.e., “TFDs”) could instead be used as two-terminal switches to apply voltage to each pixel:

Instead of a three-terminal TFT, a two-terminal switch or thin film diode (TFD) may be used at each pixel in an AMLCD. There are several ways to implement TFD LCDs. A TFD in this context can be either a rectifying diode or a bi-directional diode, also called a metal-insulator-metal (MIM) diode or a nonlinear resistor. The bi-directional diode has very low current at voltages below about 5 V and starts conducting when a voltage above 10-15 V of either positive or negative polarity is applied.

* * *

The basic circuit and drive scheme of a single TFD LCD are shown in Fig. 2.23. In diode displays, the data lines are ITO stripes on the color plate [counter substrate], as in passive matrix STN LCDs.

See Ex. 1016 at 49-50.

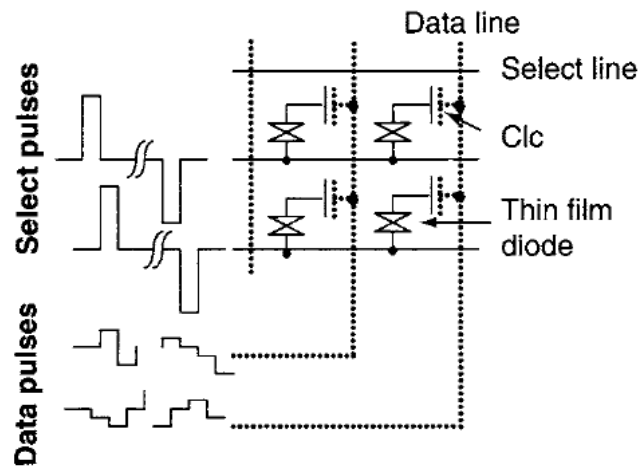


Figure 2.23: Circuit and drive waveforms of a thin film diode LCD.

See Ex. 1016 at 51, Fig. 2.23. This well-known structure is also discussed in the '606 patent in embodiments one to six. '606 patent at 14:45-37:25 (embodiments one to six).

45. For a TFD, data lines must be connected on the counter substrate across the LC layer, which is different from the case for TFT AMLCDs. In TFT AMLCDs, the data and select lines are positioned on the active-matrix substrate. The counter substrate contains a single common electrode:

In a TFT-based AMLCD (Fig. 2.3), both select and data lines are on the active matrix substrate, along with the pixel electrode and storage capacitor. The counter-electrode of each LC pixel capacitor, indicated by the dotted line, is a single common transparent electrode on the opposite substrate (which usually also has color filters). This common electrode is shared by all pixels in the array.

See Ex. 1016 at 29-30.

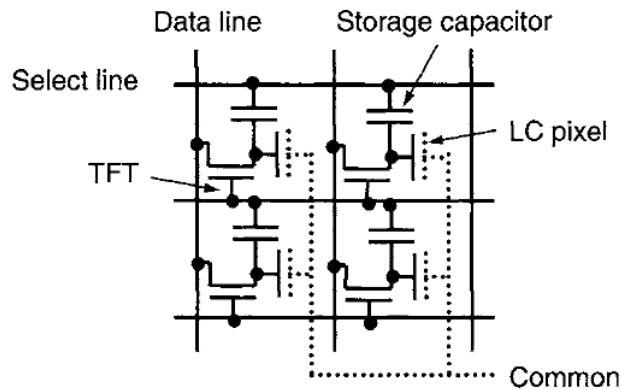


Figure 2.3: Circuit diagram for four pixels in an active matrix LCD.

See Ex. 1016 at 32, Fig. 2.3.

46. For all AMLCDs, connections are needed from the substrate containing the active elements (pixel array) to the common electrode on the counter substrate. This can be accomplished by conductive dots that connect the common electrode of the counter substrate to the pixel array. See Ex. 1016 at 81 (“conductive dots will serve to short the ITO common electrode on the color plate to metal pads on the TFT array plate, so that the Vcom voltage can be applied to the color plate through pads on the TFT array plate”).

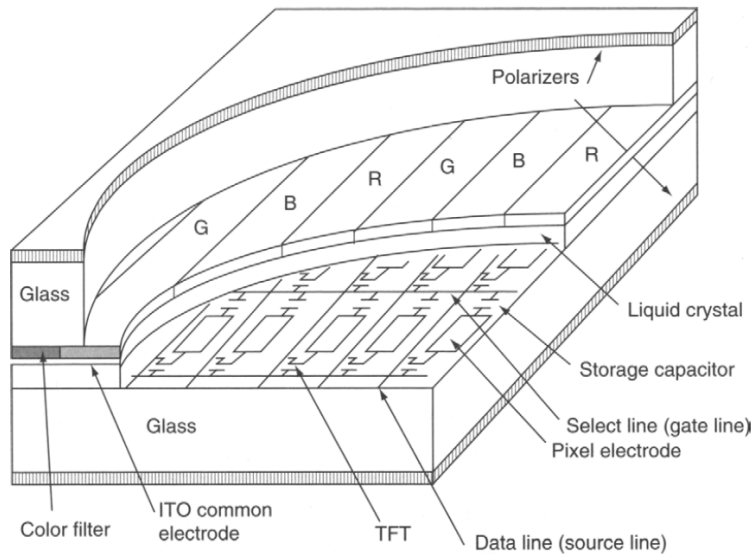


Figure 3.1: Cutout view of a TFT LCD.

See Ex. 1016 at 56, Fig. 3.1.

B. Filling Techniques

47. Traditionally, the LC layer in an LCD was pushed into the void between the substrate containing the pixel array and the counter substrate using a vacuum fill technique:

An injection hole or fill port is left open in the glue seal to allow filling of the assembly with LC fluid. The filling process takes place in a vacuum chamber. A stack of LC assemblies is evacuated in a vacuum chamber to a pressure below 1 Torr (Fig. 3.22). The glue seal openings are then dipped into LC fluid and the chamber is backfilled with N₂ gas. This forces the LC fluid to enter the narrow cell in a process that can take, for large displays, many hours to complete.

See Ex. 1016 at 81.

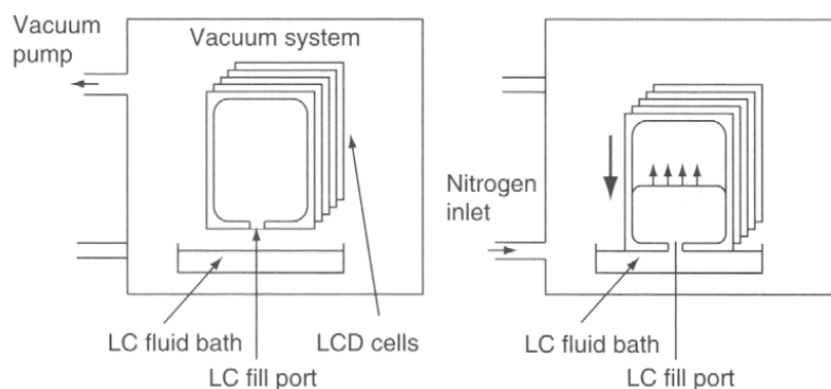


Figure 3.22: Filling of LC cells through fill ports by nitrogen backfill in a vacuum system.

See Ex. 1016 at 82, Fig. 3.22.

48. At least by 2001, researchers were developing a technique to deposit the LC that did not require the slow process of vacuum filling. See, e.g., Ex. 1013. This new technique applied LC via a dispenser and was termed drop filling or one-drop fill:

The drop-filling process provides a dramatic reduction in the filling time from more than 24 hours to a few minutes for large displays used in LCD televisions and monitors.

See Ex. 1016 at 83.

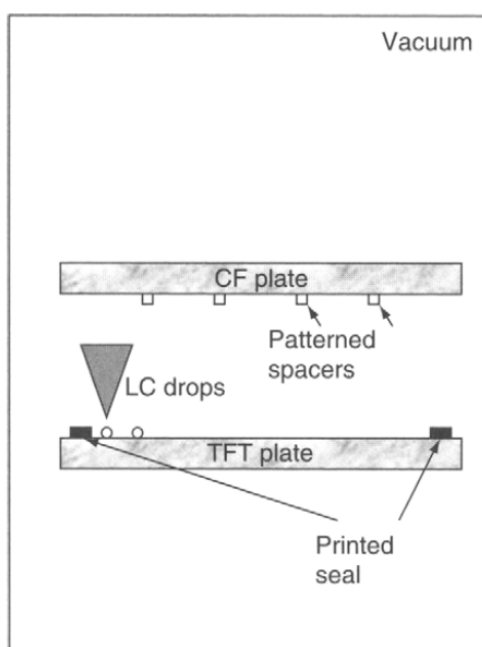


Figure 3.24: Newer LC assembly techniques using patterned spacers and LC drop filling.

See Ex. 1016 at 83, Fig. 3.24.

49. In 2001, IBM and Panasonic developed a one drop fill method for use by display manufacturers:

We have developed an ODF [one drop fill] technology for TFT-LCDs and 22" IPS-mode LCD panel with 4-sided TAB bonding. It has been successfully fabricated in a manufacturing environment. Simplifying the cell process and reducing the fabrication time has been demonstrated with high usage efficiency of the LC material.

See Ex. 1013 at 1357.

Prototype versions of the 9.2 Mpixel display have been produced using a liquid crystal "one-drop fill" process combined with a new process

for liquid crystal alignment which does not require rubbing. In this process, an ion-beam is used to chemically alter the surface of a thin diamond-like carbon layer to align the liquid crystal. These technological improvements combine to improve performance and reduce manufacturing cost.

See Ex. 1015 at 3.

We manufactured 15inches TFT-panel with this sealant by the LC-Dropping method. We could get uniformity and flicker-less TFT-panel.

Now, we are examining production of the “LC-Dropping method” for the large substrate. We confirmed 3 merits of the LC Dropping method.

See Ex. 1014 at 1353.

50. With the one-drop fill technique, a gap or hole does not need to be kept in the seal, and the seal can be formed contiguously prior to application of the LC. Therefore, the step of sealing a hole in the seal is not necessary:

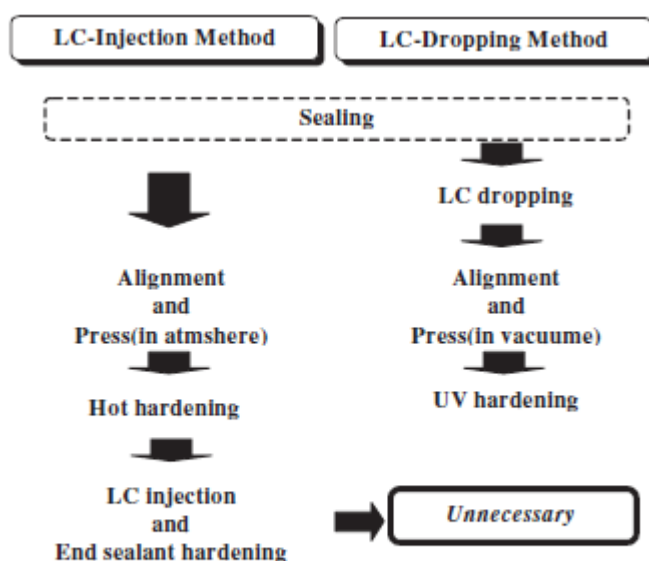


Figure 1. LC-Dropping method and LC-Injection method

See Ex. 1014 at Fig. 1; see also Ex. 1013 at Fig. 1.

C. Sealing and Sealing Materials

51. As mentioned above, the construction of an LCD panel comprises two flat glass panes with associated electronic components and traces disposed on each, with a liquid crystalline material filling the gap between the two glass panes. There is a need for a sealing material then, to retain the liquid crystalline material in the cavity between the two glass panes, and the sealing material is often formulated from a rubber, epoxy, resin, or similar material. To facilitate electrical connection between electrical components on the two glass panes, a conductive material is needed in the vertical plane, and this is sometimes accomplished by applying a conductive paste or other material to the region outside of the seal and connecting to a portion of the

intended substrate that overhangs the sealing portion. This method results in some unused substrate space, which is disfavored, and so another well-known technique involves placing conductive material at points within the seal so that there are several conduction pathways through the seal itself. A drawback to this method is that for displays with a desirably narrow frame, the seal will be narrower:

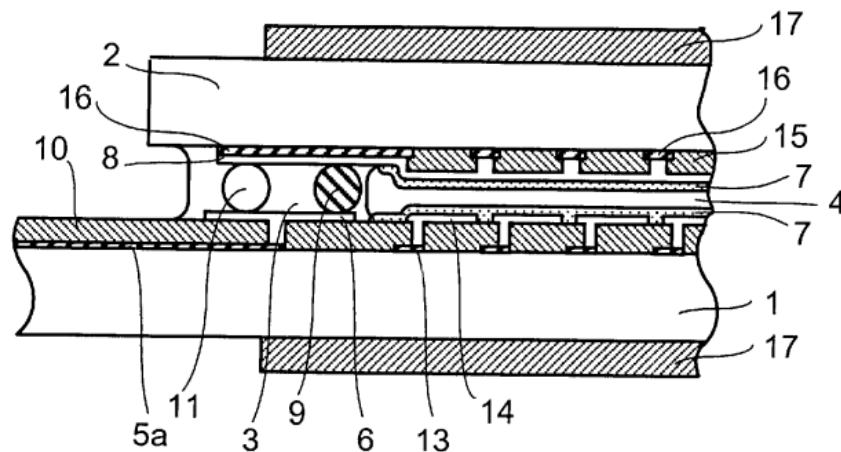
However, making the sealing adhesive strip 3 narrower is limited to a certain minimal width to maintain adhesion strength and moisture resistance. The distance between the end of the display area D and the sealing adhesive 3 is also limited to a certain minimal width because of limitation in application accuracy of the sealing adhesive 3 or disorder in the orientation of liquid crystal at the ends of sealing, or at the ends of an orientation film 7 If the position is too far inside the edge, the conductive paste 18 mixes with the sealing adhesive 3, and may destroy the sealing. To secure an electrical connection, reduction of the area of the conductive paste 18 may also be limited to a certain minimal area.

See Ex. 1017 (Yamagishi) at 1:66-2:14.

52. One of the improvements and simplifications that has been considered is the use of anisotropic conductive material incorporated into the sealing material. This allows the seal to perform multiple purposes, including not only retaining the liquid crystalline material in the cavity between the glass panes, but also facilitating electrical connection between the common electrode on one pane to the appropriate

electronic components on the opposite pane. One commercially available product is known as anisotropic conductive film (ACF), which allows conduction in the z-axis while electrically insulating in the lateral directions, although various epoxies and resins can incorporate conductive particles such that they achieve the same function. This technique has been known since at least 2000. For example, it is described in at least Ex. 1017 and Ex. 1018, that use dispersed conductive particles of particular size to facilitate electrical contact between the two glass panes:

FIG. 2A



See Ex. 1018 (*Nakahara*) at Fig. 2.

53. This anisotropic conductivity allows for the circuit designer to easily connect appropriate components between the two glass panes, provided that there is a trace or other electronic component in a corresponding vertical direction:

The liquid crystal display panel of the present invention further includes a sealing adhesive containing spherical conductors dispersed approximately uniformly at a predetermined concentration along the periphery between the two substrates. The spherical conductors in the sealing adhesive electrically connect the common electrodes on the second substrate and the connecting terminal electrodes on the first substrate.

See Ex. 1017 (Yamagishi) at 2:55-62.

54. In this method, the introduction of an anisotropically conducting seal allows for a more consistent voltage across the plane, where if the connection to the common electrode existed at only the corners of the display for instance, the voltage distribution becomes nonuniform, particularly when the display size increases.

VI. OVERVIEW OF PRIOR ART

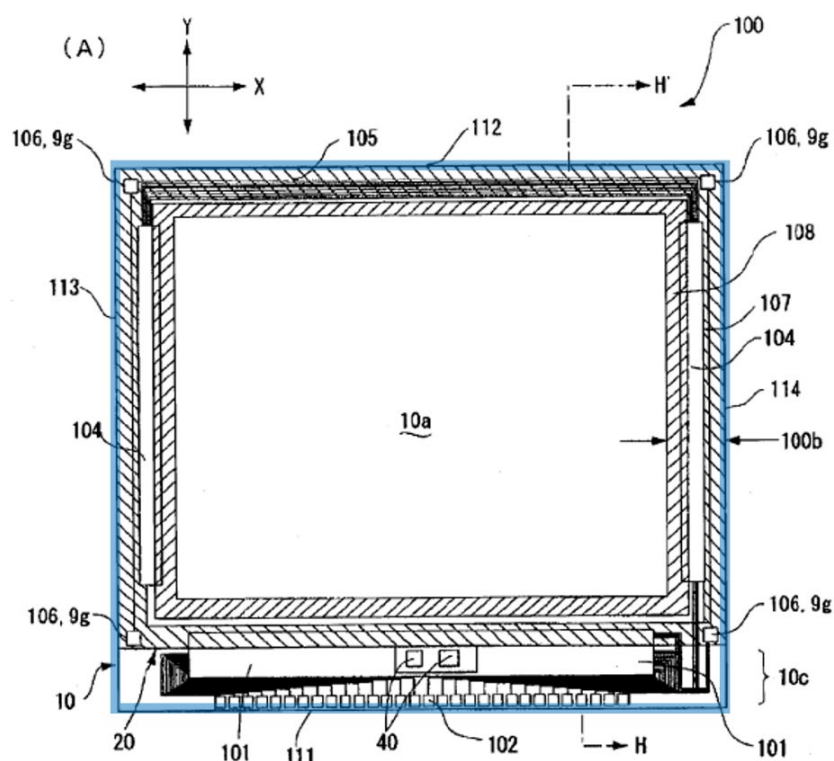
A. Overview of *Fujikawa*

55. U.S. Patent App. Publ. No. 2003/0174271 (“*Fujikawa*”) published on September 18, 2003, from a patent application filed January 27, 2003. I understand *Fujikawa* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e).

56. *Fujikawa* “relates to an electrooptic device,” such as a liquid crystal device, for use in electronic devices like portable computers or telephones. *Fujikawa* at [0002], [0004], [0010]-[0023]. *Fujikawa* explains liquid crystal devices typically comprise a display region 10a and a frame region 100b that lies around the display

region but does not directly contribute to the display. *Fujikawa* at [0010]. When a liquid crystal device is mounted in a portable device, “it is required that the image display region 10a should be large[,] and that the entire display should be small for size reduction of the device.” *Fujikawa* at [0010]. To do this, *Fujikawa* explains the need to “decrease the proportion of the width of the frame region 100b to the total size of the liquid crystal device 100.” *Fujikawa* at [0010]. However, because numerous components (like data line driving circuits, scanning line driving circuits, conductive electrodes, etc.) “are formed around the image display region 10a, the peripheral region” often “cannot be narrowed further.” *Fujikawa* at [0010]. To address this issue, *Fujikawa* discloses a way to “improv[e] the layout of peripheral circuits” to “narrow[]” the peripheral region. *Fujikawa* at [0011]; *see also Fujikawa* at [0012]-[0023].

57. Figure 1A is a plan view of *Fujikawa*’s improved liquid crystal device. *Fujikawa* at [0045]. As shown below in Figure 1A, *Fujikawa*’s liquid crystal device includes a “TFT array substrate 10.” *Fujikawa* at [0046].



Fujikawa at Fig. 1A (TFT array substrate 10 is annotated in blue). *Fujikawa* explains that TFT array substrate 10 has four “substrate edge[s],” 111, 112, 113, and 114. *See Fujikawa* at [0046]. And disposed on TFT array substrate 10 are “a plurality of pixels formed in a matrix[,] so as to constitute the image display region 10a of the liquid crystal device.” *Fujikawa* at [0053]. *Fujikawa* explains that pixels 100a in the image display region are arranged “at a predetermined pitch and in a matrix corresponding to the intersections of a plurality of data lines 6a extending in the Y-direction[,] and a plurality of scanning lines 3a extending in the X-direction.” *Fujikawa* at [0054]. This is shown below in Figure 2 of *Fujikawa*:

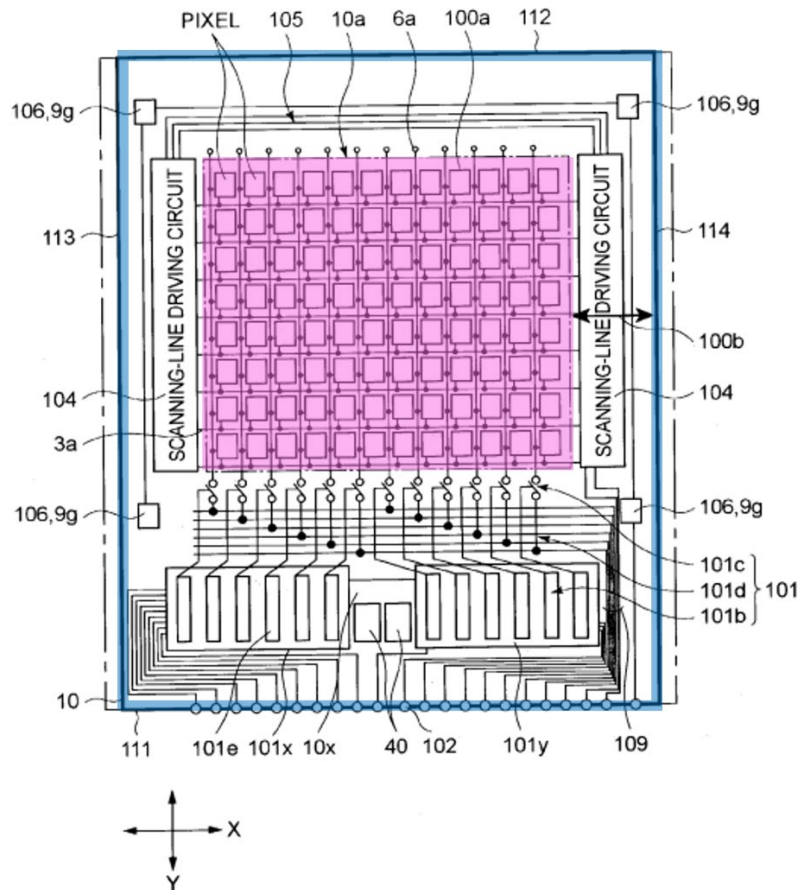


FIG.2

Fujikawa at Fig. 2 (TFT array substrate 10 is annotated in blue and image display region 10a is annotated in pink). Each pixel 100a includes “a pixel electrode 9a and a pixel-switching TFT 30 for controlling the pixel electrode 9a.” *Fujikawa* at [0058], [0061]. The pixel electrodes and the TFTs (which stands for thin film transistor) are shown below in *Fujikawa* Figure 4:

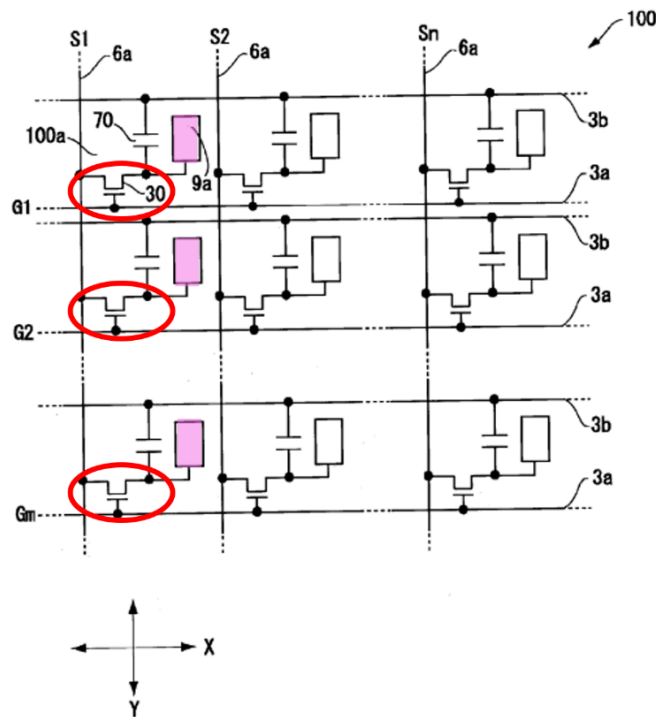
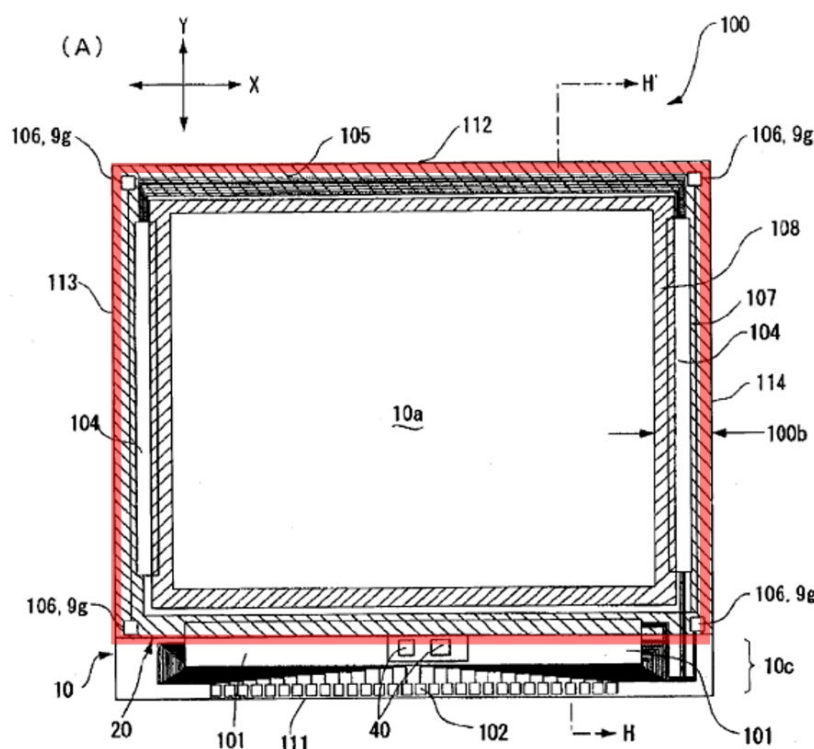


FIG.4

Fujikawa at Fig. 4 (the pixel electrodes are annotated in pink and thin film transistors (TFTs) are annotated in red).

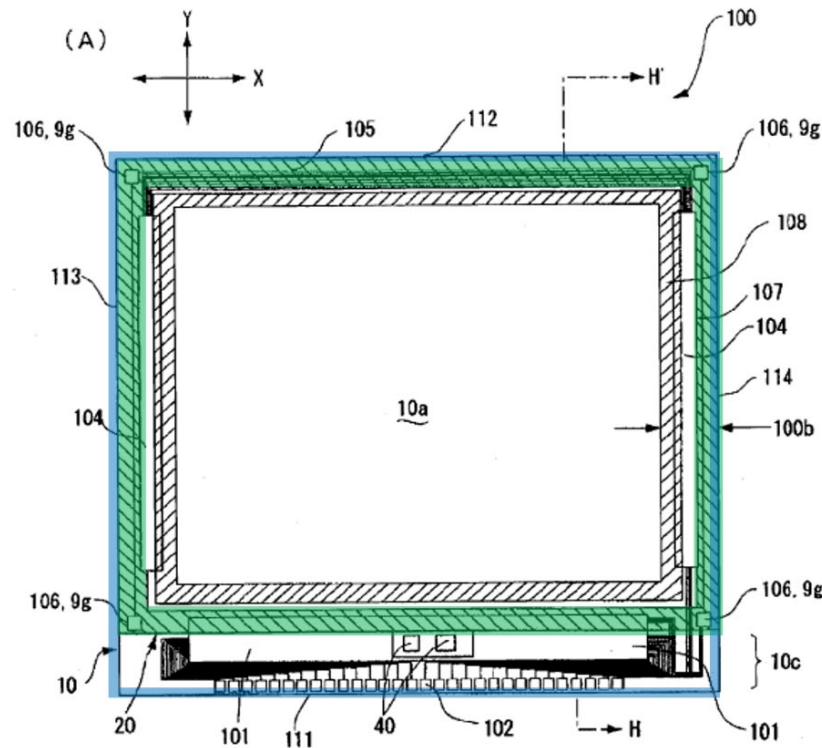
58. *Fujikawa*'s liquid crystal device also includes a "counter substrate 20."

Fujikawa at [0046]. The counter substrate is shown below in Figure 1A:

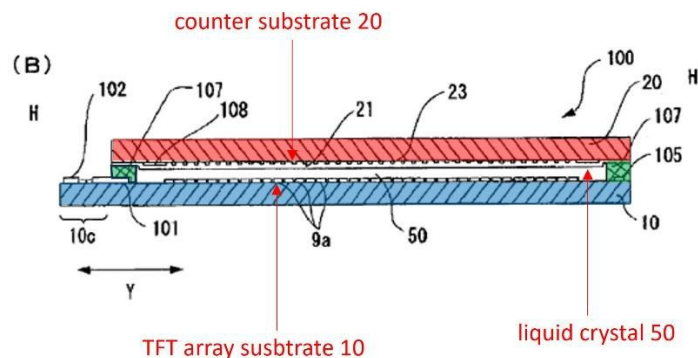


Fujikawa at Fig. 1A (counter substrate 20 is annotated in red). Disposed on counter substrate 20 are “counter electrodes 21.” *Fujikawa* at [0050], [0058], [0079].

59. *Fujikawa* explains that the TFT array substrate 10 and counter substrate 20 are “bonded with a predetermined space therebetween by the sealing material 107,” which is “formed on a TFT array substrate 10 . . . along the edge of a counter substrate 20.” *Fujikawa* at [0046], [0049]. *Fujikawa* explains that sealing material 107 can “be an adhesive made of a photosetting or thermosetting resin for bonding” and also “mixed with a gap material, such as glass fibers or glass beads, that ensures a predetermined distance between the substrates.” *Fujikawa* at [0049].

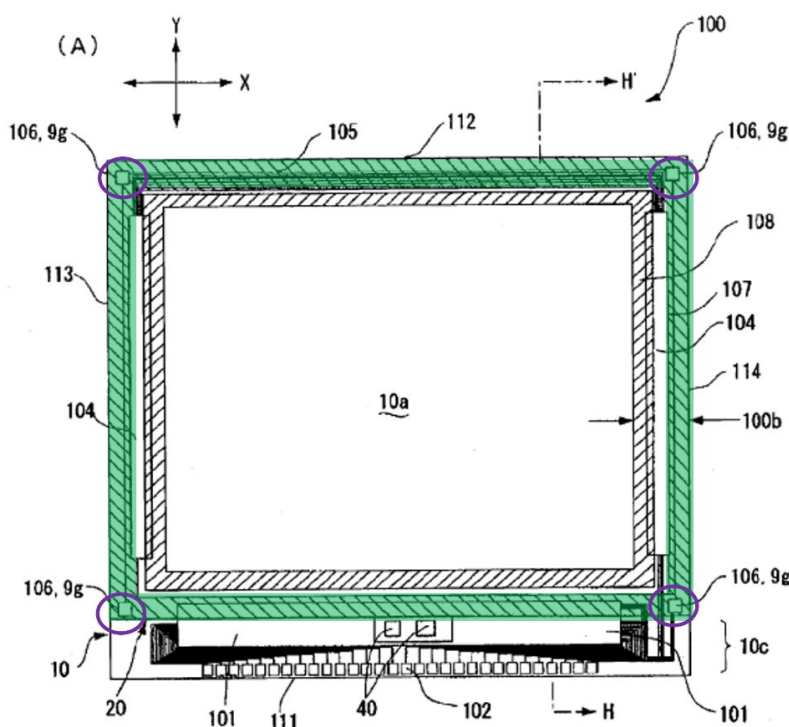


Fujikawa at Fig. 1A (sealing material 107 is annotated in green). *Fujikawa* explains liquid crystal 50 is “held” in the “predetermined space” between the two substrates, as shown below in Figure 1B:



Fujikawa at Fig. 1B (TFT substrate 10 is annotated in blue, counter substrate 20 is annotated in red, and sealing material 107 is annotated in green).

60. *Fujikawa* describes conductive electrodes 9g and conductive materials 106, which *Fujikawa* explains is “formed in areas corresponding to four corners of the counter substrate 20 for electrical continuity between the TFT array substrate 10 and the counter substrate 20.” *Fujikawa* at [0047]. *Fujikawa* explains the “number of conductive electrodes 9g and the like may be appropriately changed.” *Fujikawa* at [0047]. These conductive materials (the conductive electrodes 9g and conductive materials 106) are shown below in Figures 1A and 9:



Fujikawa at Fig. 1A (conductive electrodes 9g and conductive materials 106 are in purple circles and sealing material 107 is annotated in green).

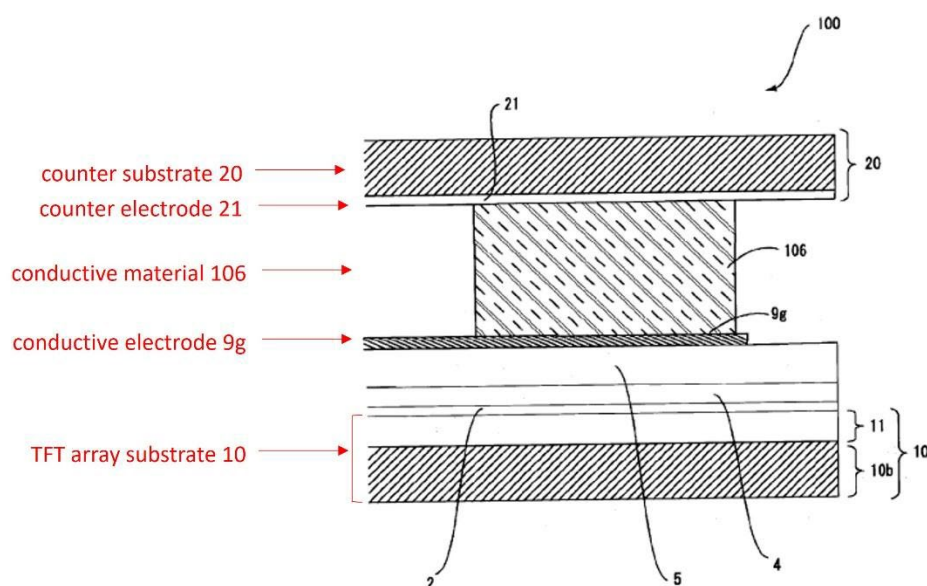


FIG.9

Fujikawa at Fig. 9 (annotated). *Fujikawa* also explains the “plurality of conductive electrodes 9g are formed in the region of the TFT array substrate overlapping with the counter substrate 20, and are electrically connected to the counter electrodes 21 of the counter substrate 20 through the conductive material 106 sandwiched between the substrates.” *Fujikawa* at [0079]. The conductive material 106 “can be made of an epoxy resin adhesive component mixed with conductive particles such as silver powder and gold-plated fiber.” *Fujikawa* at [0079].

B. Overview of *Kang*

61. U.S. Patent Appl. Publ. No. 2004/0257504 (“*Kang*”) published on December 23, 2004, from a patent application filed April 14, 2004. I understand that *Kang* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

62. *Kang* discloses “a liquid crystal display panel capable of preventing air from flowing into an image display part . . . where a thin film transistor array and a color filter substrate are attached to each other.” *Kang* at [0003], [0037]. According to *Kang*, liquid crystal display panels were typically formed by a “vacuum injection method.” *Kang* at [0063]. In a vacuum injection method, an “LCD panel is formed by dipping a liquid crystal injection hole of a liquid crystal display panel into a vacuum chamber filled with liquid crystal.” *Kang* at [0063]. *Kang* explains that the liquid crystal injection hole in the vacuum injection method “is defined as an open region of one side of the seal pattern 506.” *Kang* at [0064]; *Kang* at [0064] (“[A] portion of the seal pattern 506 is formed open so that it functions as a liquid crystal injection hole.”). Liquid crystal is “forced into the liquid crystal display panel by the pressure difference between the inner side and the outer side of the liquid crystal display panel, and can be controlled by varying the degree of the vacuum.” *Kang* at [0063]. Once the panel is filled with the liquid crystal, “the liquid crystal injection hole is sealed.” *Kang* at [0063].

63. *Kang* explains that this vacuum method “has a number of problems.” *Kang* at [0065]. For example, it can “take[] a long time to fill the liquid crystal in the liquid crystal display panel” using a vacuum injection method. *Kang* at [0066]. This is particularly true “as the size of the liquid crystal display panel increases,” making “large-scale maintaining of liquid crystal display panels” using vacuum methods difficult. *Kang* at [0066]. *Kang* also explains that vacuum injection methods also “consume[]” “a large quantity of liquid crystal” and, in turn, increase the “unit price” of the liquid crystal display. *Kang* at [0067]; *Kang* at [0067] (“when the liquid crystal on the container is exposed to air or a specific gas, it reacts with the gas and become degraded” and thus “even if the liquid crystal in the container is used to fill a plurality of the liquid crystal display panels, a large amount of the liquid crystal will still be remaining after the filling process and must be discarded”).

64. To “overcome these problems of the vacuum injection method,” *Kang* notes that a “dropping method” has been “adopted.” *Kang* at [0068]. *Kang* explains that this method includes providing a “seal pattern 506,” which “is formed to have a closed shape that encompasses the outer edge of the image display part in order to prevent the leakage of the liquid crystal from the image display part.” *Kang* at [0070]. The seal pattern 506 “may be formed of various planar shapes depending on a method used to form the liquid crystal layer.” *Kang* at [0062]. Liquid crystal is then dropped directly on the image display part of the substrate (instead of “filled

from the outside”) so the liquid crystal is “uniformly distributed . . . by the pressure generated when” two substrates “are attached to each other.” *E.g.*, *Kang* at [0069]-[0070]. As *Kang* explains, this dropping method reduces both manufacturing time and cost relative to the vacuum injection method. *Kang* at [0071]-[0072].

C. Overview of *Ikeguchi*

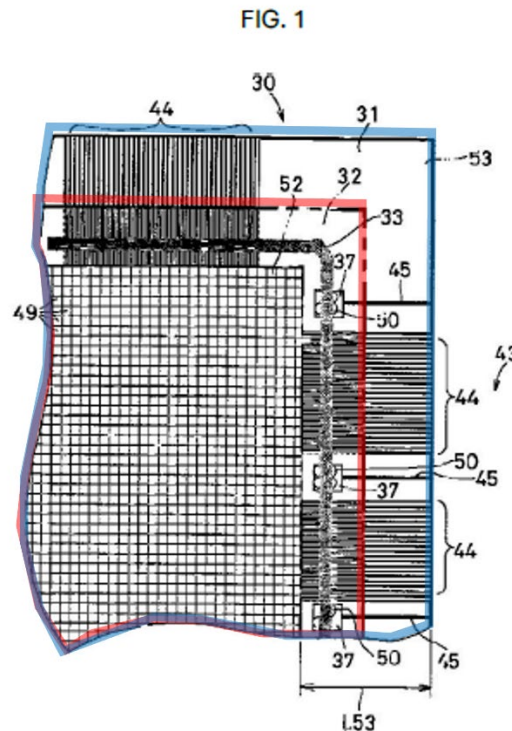
65. JP 2003-280030 (“*Ikeguchi*”) published October 2, 2003.² I understand *Ikeguchi* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (b).

66. *Ikeguchi* discloses a liquid crystal display and a related method for manufacturing such a liquid crystal display device. *Ikeguchi* at [0001]. In particular, *Ikeguchi* “provide[s] a display element in which the non-display region can be made small and reliable conduction” between the substrates “can be achieved.” *Ikeguchi* at [0013]. *Ikeguchi*’s liquid crystal device has “two opposingly disposed electrode substrates” and a bonding material that “bonds the electrode substrates together.” *Ikeguchi* at [0014]. A “conductive material having conductivity is mixed into the bonding material” in part of that bonding material “sandwiched between the inter-substrate conducting-electrode portions.” *Ikeguchi* at [0014]-[0018]. The liquid

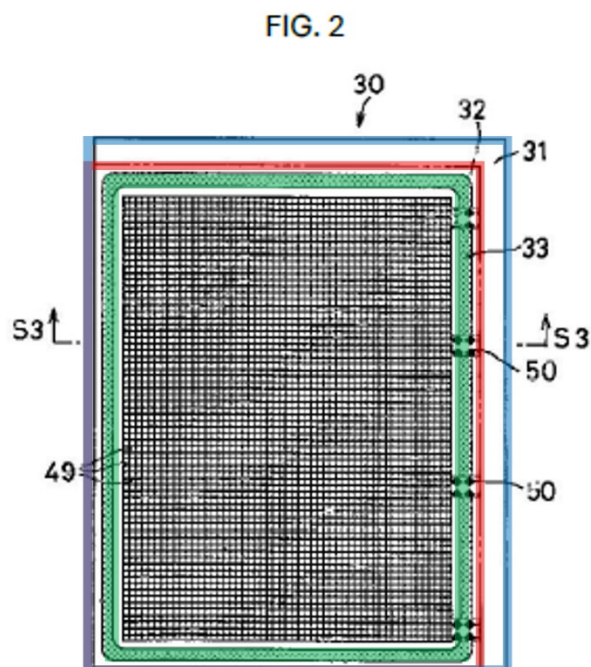
² Citations throughout this Declaration are to the certified translation of *Ikeguchi* that is provided at Ex. 1008.

crystal device includes “inter-substrate electrode portions” that “creat[e] conduction between” the substrates as well. *Ikeguchi* at [0014].

67. Figure 1 of *Ikeguchi* is a “sectional view” of an exemplary embodiment for *Ikeguchi*’s liquid crystal display. *Ikeguchi* at [0027]. As shown in Figure 1, liquid display element 30 includes two electrode substrates, substrate 31 and substrate 32:



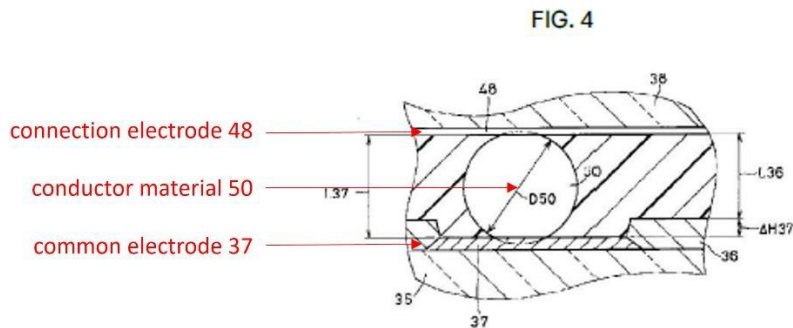
Ikeguchi at Fig. 1 (annotated); *Ikeguchi* at [0027]-[0029]. These two substrates are “disposed and layered spaced apart from each other” and are “bonded together by a sealing material 33 provided in a rectangular closed-loop shape”:



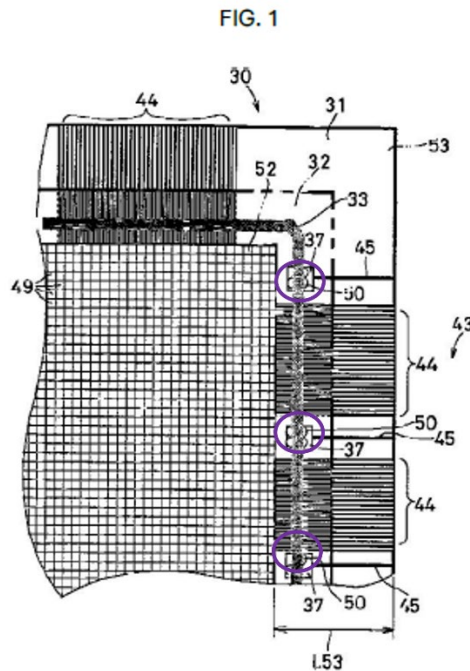
Ikeguchi at Fig. 2 (first substrate is annotated in blue, second substrate is annotated in red, and sealing material is in green); *Ikeguchi* at [0027]-[0030]. “Sealing material 33” is provided between the electrode substrates and “surround[s]” the liquid crystal material 34 in display area 40. *Ikeguchi* at [0027], [0030], [0041].

68. *Ikeguchi* explains it can be necessary to “creat[e] conduction” between the substrates. *Ikeguchi* at [0037]. And a “conducting portion” can be provided to do this. *Ikeguchi* at [0037]. In particular, *Ikeguchi* explains first electrode substrate 31 is provided with a common electrode 37, and the second electrode substrate 32 is provided with a counter electrode 42 and a connection electrode 48. *Ikeguchi* at [0037]. According to *Ikeguchi*, “counter electrode 42 and the connection electrode 48 may be realized by a single electrode.” *Ikeguchi* at [0037]. “[S]ealing material 33

. . . , is sandwiched between the common electrode 37 and the connection electrode 48.” *Ikeguchi* at [0039]. In this location, *Ikeguchi* explains that the sealing material 33 includes conductor material 50 that can comprise “conductive particles in which metal layers are formed on the surfaces of synthetic-resin base particles.” *Ikeguchi* at [0037], [0040], [0042]-[0043].



Ikeguchi at Fig. 4 (annotated). And as shown below, discrete locations of common electrode 37 and conductor material 50 are provided along the sealing region edge:



Ikeguchi at Fig. 1 (annotated). *Ikeguchi* explains that this arrangement allows non-display area 53 to be “made small,” *Ikeguchi* at [0043]-[0044], and obtains a display element 30 having low electrical resistance and “high display quality and stability,” *Ikeguchi* at [0047].

VII. THE '606 PATENT

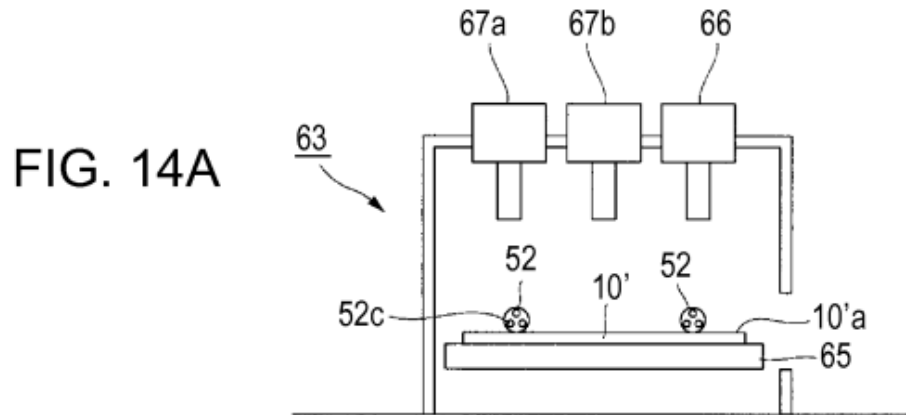
A. Overview of the '606 Patent Specification

69. The '606 patent relates to “a method of manufacturing a liquid crystal device [and] a liquid crystal device.” '606 patent at 1:19-21. As discussed above in the general background of technology section (Section V), the '606 patent similarly explains liquid crystal devices generally comprise “a pair of substrates with a liquid crystal layer interposed therebetween.” '606 patent at 1:23-27. To form liquid crystal

devices, systems would coat a sealant (sealing material) “in a peripheral portion of a surface of one substrate.” ’606 patent at 1:27-29. A “liquid crystal injection hole” would be “formed at a part of the sealant.” ’606 patent at 1:29-31. Spacers would then be placed inside the sealant, and “the other substrate [would be] bonded to the one substrate via the sealant” to form a liquid crystal cell. ’606 patent at 1:31-33. After this “liquid crystal cell is formed,” the cell is vacuumed and “brought back to atmospheric pressure while the liquid crystal injection hole is dipped into a liquid crystal vessel” so that “the liquid crystal cell is filled with liquid crystal by means of a pressure difference . . . and surface tension.” ’606 patent at 1:33-41. As *Kang* explains (Section VI.B), the ’606 patent also recognizes that these vacuum injection methods can “take[] an extremely long time.” ’606 patent at 1:41-45. As such, and again like *Kang* explains (Section VI.B), the ’606 patent sought to use a “dropping assembly method” instead, which would reduce manufacturing time and avoid using a plug to seal the liquid crystal injection hole. ’606 patent at 1:46-3:58, 3:62-10:41, 18:36-19:27, 22:36-31:17.

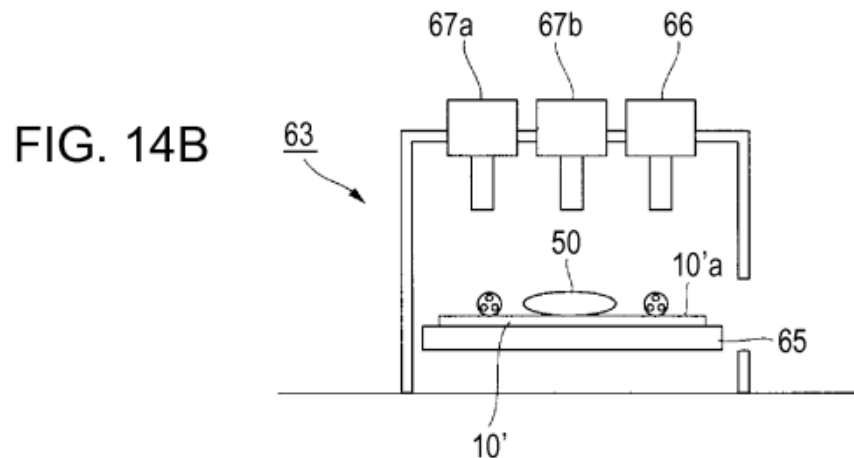
70. The dropping assembly method described in the ’606 patent includes well-known steps for a one-drop fill method. Section V.B. First, the ’606 patent describes preparing a first substrate 10’ and a second substrate 20’. ’606 patent at 18:46-19:15, 22:41-45. The first substrate 10’ is loaded onto a substrate load/unload unit, and the “sealing materials are coated on” the first substrate to form a continuous

“ring-shaped portion.” ’606 patent at 22:46-61, 22:64-65, 23:5-24:36, Figs. 14A, 17A-17B. This is shown, for example, in Figure 14A from the ’606 patent below:



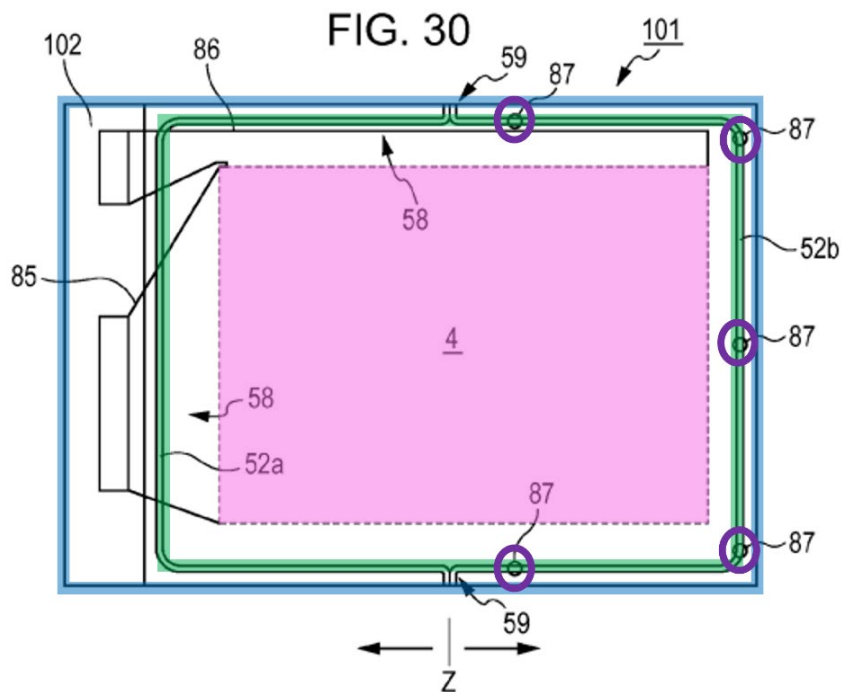
’606 patent at Fig. 14A. “Liquid crystal 50 is dropped in the ring-shaped portion.”

’606 patent at 25:6-15. This is shown for example in Figure 14B from the ’606 patent below:



'606 patent at Fig. 15C. The resulting liquid crystal device (formed from the bonded first and second substrates) is then unloaded from the load/unload unit. '606 patent at 27:25-37; '606 patent at 27:38-28:54. According to the '606 patent, and as likewise explained in *Kang*, this well-known method reduces the leakage of liquid crystal and improves the “reliability of the liquid crystal device.” '606 patent at 29:17-25; '606 patent at 29:25-31:17.

71. An exemplary liquid crystal device is shown in Figure 30 of the '606 patent:



'606 patent at Fig. 30 (annotated), 38:26-67. As shown, the liquid crystal device includes a TFT substrate 102 (blue), data relaying wires 85, gate relaying wires 86,

ring-shaped portion 58, which includes both the conductive sealing member 52b and the insulating sealing member 52a (green), image display region 4 (pink), and dot conductive portions 87 (purple). '606 patent at 38:26-67. The '606 patent discloses the "TFT substrate 102 is electrically connected to the counter substrate via the dot conductive portions 87." '606 patent at 37:67-38:3.

B. Overview of the Prosecution History of the '606 Patent

72. I have reviewed the prosecution history of the application that led to the '606 patent. Ex. 1002. Below, I summarize certain events in the prosecution of the '606 patent.

73. The '606 patent is a continuation of Application No. 14/571,729 ("the '729 application"), which issued as U.S. Patent No. 9,459,498. '606 patent at Related U.S. Application Data. The '729 application is a divisional of Application No. 11/301,086, which issued as U.S. Patent No. 9,599,861. '606 patent at Related U.S. Application Data.

74. The application that led to the '606 patent was filed on December 16, 2014, with a request for prioritized examination, Ex. 1002 at 1-208, that was granted, Ex. 1002 at 305. The Examiner issued a first Office Action, wherein the Examiner explained the "application contains claims directed to" multiple patentably distinct species, and required the Applicant to "elect a single disclosed species." Ex. 1002 at 310-315. In response, the Applicant elected the embodiment in Figure 30 as covered

by the claims and made an amendment to claim 13 to resolve a typographical error.
Ex. 1002 at 317-327.

75. The Examiner then issued a second Office Action, rejecting the claims as obvious over U.S. Patent No. 6,930,745 (“*Miyazaki*,” Ex. 1010), and U.S. Patent Application Publ. No. 2005/0122466 (“*Tanaka*,” Ex. 1011). Ex. 1002 at 331-343. The Examiner submitted *Miyazaki* disclosed every claim element, but was “silent” regarding whether the first substrate “includes a protruding portion which protrudes over the second substrate in the plan-view . . . and a plurality of conductive portions.” Ex. 1002 at 333-341. The Examiner reasoned the claims would have been obvious in view of *Tanaka*. Ex. 1002 at 333-341.

76. In response, the Applicant amended the then-pending claims. Ex. 1002 at 359-369. Among other things, the Applicant amended the claims to require: (1) the active elements to be “thin film transistors disposed on the first substrate”; (2) the common electrode “disposed on the second substrate”; and (3) “dot conductive points.” Ex. 1002 at 359-369. The Applicant then argued *Miyazaki* failed to disclose each of these features. Ex. 1002 at 370-373. With respect to “dot conductive points,” the Applicant argued *Miyazaki* discloses its “conductive portion” “is an area, not a dot.” Ex. 1002 at 371. And it argued that *Tanaka* failed to remedy this deficiency in *Miyazaki*. Ex. 1002 at 371.

77. The Examiner then issued a final rejection. Ex. 1002 at 376-392. The Examiner found *Miyazaki* was silent as to, among other things, the claimed “plurality of conductive portions being dot conductive points.” Ex. 1002 at 380-381, 385, 387-388. According to the Examiner, this limitation would have been obvious in view of *Tanaka*. Ex. 1002 at 380-381, 385, 387-388. As the Examiner submitted:

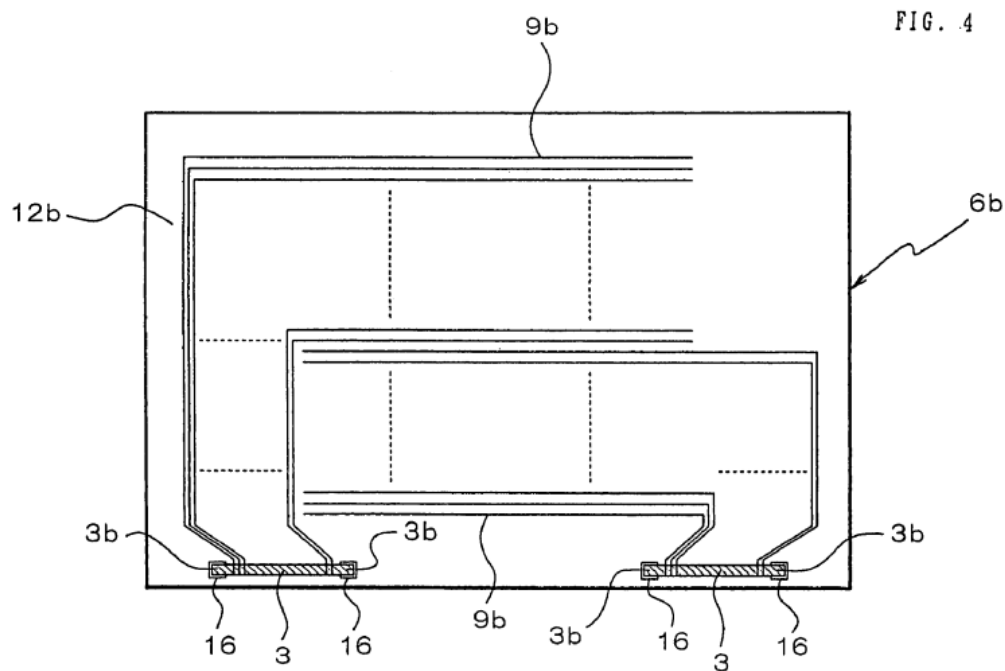
[I]t would have been obvious to one having ordinary skill in the art at the time the invention was made to have dot conductive points, since it has been held that the configuration of the claimed shape of the opening was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the claimed shape of the opening was significant. The application has not provided any criticality for the shape of the conductive points to be a dot.

Ex. 1002 at 378-379 (internal citation omitted).

78. The Applicant initiated an examiner interview to discuss the rejection, but no agreement was reached. Ex. 1002 at 394-395. The Applicant then submitted a request for continued examination, and proposed further amendments. Ex. 1002 at 397-414. The Applicant amended the claims to require, among other things, (i) the seal member not “protrud[e] from the second substrate in the plan-view,” and (ii) a “plurality of wiring lines” that “extend onto the protruding region,” and that do not

“connect[] to the dot conductive points.” Ex. 1002 at 401-410. The Applicant argued neither *Miyazaki* nor *Tanaka* disclosed such limitations. Ex. 1002 at 411-414.

79. The Examiner issued another Office Action, again submitting that the claims would have been obvious over *Miyazaki* and *Tanaka*. Ex. 1002 at 432-449. As to the “dot conductive points,” the Examiner submitted *Miyazaki* (Figures 1-5, 16) discloses a device where the first substrate includes “a plurality of conductive of portions (3b), the plurality of conductive portions being a plurality of dot conductive points and the plurality of wiring lines extend onto the protruding region . . . (11a and 3b).” Ex. 1002 at 434. For convenience, *Miyazaki* Figure 4 and the conductive portions 3b are shown below:



Ex. 1010 (*Miyazaki*) at Fig. 4. The Examiner continued, submitting that to the extent *Miyazaki* is silent regarding “dot conductive points,” such a limitation would have nevertheless been obvious over *Tanaka*. Ex. 1002 at 437-439, 441-443, 445-446.

80. The Applicant initiated a second examiner interview to discuss the rejection, but no agreement was reached. Ex. 1002 at 454-455. The Applicant then proposed additional amendments to the claims, including requiring the claimed “seal member” to be “formed continuously around the entire display region without the use of a plug.” Ex. 1002 at 457-468.³ The Applicant argued *Miyazaki* and *Tanaka* require a “plug” and thus do not disclose this limitation. Ex. 1002 at 457-468. The Examiner agreed. Ex. 1002 at 480-489. In the Notice of Allowability, the Examiner explained that the prior art failed to disclose a “seal member” “formed continuously around the entire display region without the use of a plug.” Ex. 1002 at 486-488. The ’606 patent issued on January 31, 2017. ’606 patent at Date of Patent.

C. Person of Ordinary Skill in the Art

81. I am informed that patentability must be analyzed from the perspective of “one of ordinary skill in the art” in the same field as the ’606 patent at the time of the invention. I am also informed that several factors are considered in assessing the

³ The Applicant also added new claim 21, but cancelled that claim before issuance. Ex. 1002 at 467-467, 484.

level of ordinary skill in the art, including (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the field.

82. In my opinion, a person of ordinary skill in the art (what is termed the “POSITA”) pertinent to the ’606 patent as of its earliest priority date would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional relevant work experience can compensate for less education, and *vice versa*. For example, a Master’s degree in electrical engineering, computer science, physics, or a similar field can substitute for two years of experience designing semiconductor display devices, including LCD displays. My analysis regarding the ’606 patent has been based on the perspective of one ordinary skill in the art as of the priority date of the ’606 patent.

83. I am also familiar with the knowledge of the person of ordinary skill in the art as of the priority date of the ’606 patent. I am able to opine on how the person of ordinary skill in the art would have understood the disclosure and claims of the ’606 patent, the disclosures of the prior art, the motivation to combine the prior art, and what combinations would have been obvious to one of ordinary skill in the art.

VIII. CLAIM CONSTRUCTION OF TERMS OF THE '606 PATENT

84. As I discussed above, I have been informed that for purposes of *inter-partes* reviews, the standard for claim construction of terms within the claims of the patent is the same as that applied in federal district court litigation.

85. I have been asked to assume that the claim terms generally have their plain and ordinary meaning to a person skilled in the art in light of the specification and the prosecution history. I expect to respond in the event Patent Owner proposes, or the Board adopts, a different construction.

IX. SUMMARY OF OPINIONS ON UNPATENTABILITY

86. Claims 7-13 and 15-20 of the '606 patent are unpatentable based on the following combinations of prior art, in my opinion:

Ground	Challenge Presented
1	<i>Fujikawa</i> (Ex. 1005) discloses claims 7-13 and 20
2	<i>Fujikawa</i> (Ex. 1005) renders obvious claims 7-13 and 15-20
3	<i>Fujikawa</i> (Ex. 1005) and <i>Kang</i> (Ex. 1006) render obvious claims 7-13 and 15-20
4	<i>Fujikawa</i> (Ex. 1005) and <i>Ikeguchi</i> (Ex. 1008) render obvious claims 7-13 and 15-20

Ground	Challenge Presented
5	<i>Fujikawa</i> (Ex. 1005), <i>Kang</i> (Ex. 1006), and <i>Ikeguchi</i> (Ex. 1008) render obvious claims 7-13 and 15-20

**X. FUJIKAWA ANTICIPATES CLAIMS 7-13 AND 20 (GROUND 1) AND/OR
RENDERS OBVIOUS CLAIMS 7-13 AND 15-20 (GROUND 2)**

A. Independent Claim 7

1. 7[pre]: “*A display device, comprising:*”⁴

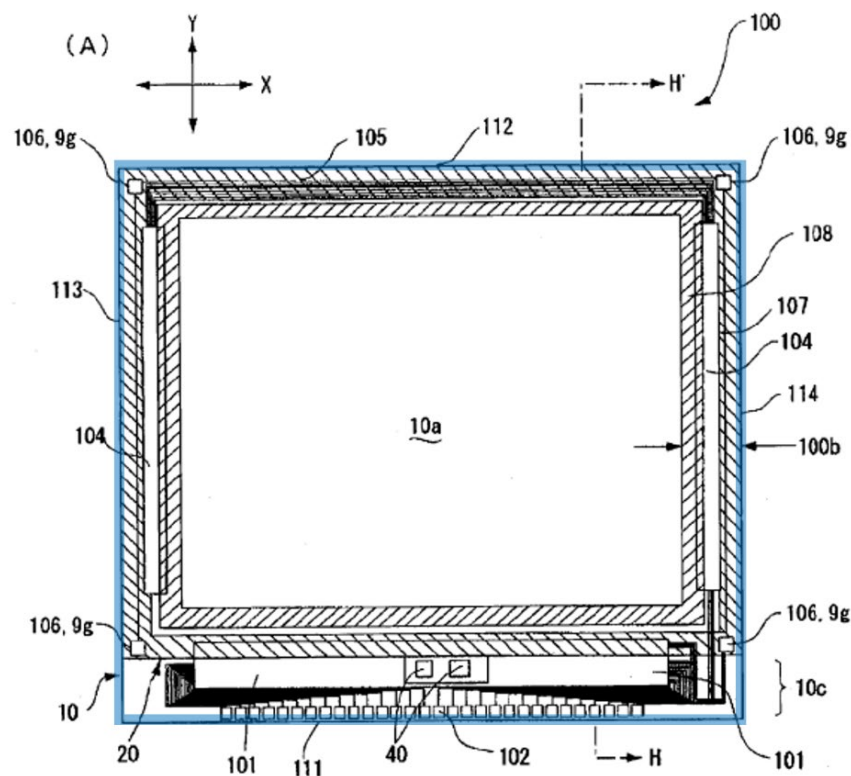
87. To the extent that the preamble is limiting, *Fujikawa* discloses it, in my opinion. *Fujikawa* “relates to an electrooptic device,” such as a liquid crystal device, for use in electronic devices, such as portable computers or telephones. *Fujikawa* at [0002], [0004], [0010]-[0023]. *Fujikawa*’s liquid crystal device includes a display region 10a that comprises a plurality of pixels 100a. *E.g.*, *Fujikawa* at [0046]-[0051], [0054]-[0058]. This liquid crystal device is a “***display device***,” as claimed. *Fujikawa* at [0051] (liquid crystal device 100 and display device 100), [0004] (explaining that electrooptic devices, like liquid crystal devices, “have attracted attention as display sections in electronic devices”).

⁴ The relevant claim language is bolded and italicized throughout my analysis.

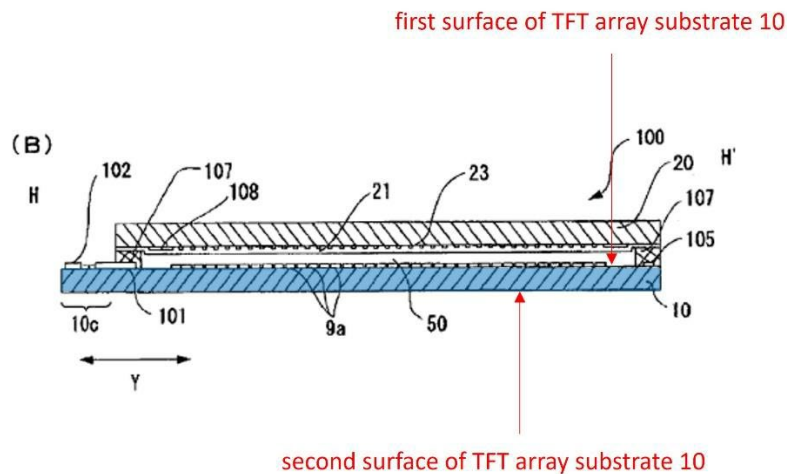
2. 7[a]: “a first substrate including a pixel region and a seal region which is defined around the pixel region on a first surface of the first substrate,”

88. In my opinion, *Fujikawa* discloses this limitation.

89. First, *Fujikawa* discloses its improved liquid crystal device (“*display device*”) includes a “TFT array substrate 10.” *Fujikawa* at [0046]. This is shown in Figure 1A of *Fujikawa* below:



Fujikawa at Fig. 1A (TFT array substrate 10 annotated in blue). TFT array substrate 10 is the claimed “*first substrate*.” And as shown in Figure 1B below, TFT substrate 10 includes a “*first surface*” (top) and a second surface (bottom):



Fujikawa at Fig. 1B (annotated).

90. Second, *Fujikawa* discloses TFT array substrate 10 (“**first substrate**”) includes a “**pixel region**,” as claimed. Specifically, *Fujikawa* discloses that disposed on TFT array substrate 10 is “a plurality of pixels formed in a matrix so as to constitute the image display region 10a of the liquid crystal device.” *E.g.*, *Fujikawa* at [0053]. The pixels 100a are arranged “at a predetermined pitch and in a matrix corresponding to the intersections of a plurality of data lines 6a extending in the Y-direction and a plurality of scanning lines 3a extending in the X-direction.” *Fujikawa* at [0054]. This is shown below in Figure 2:

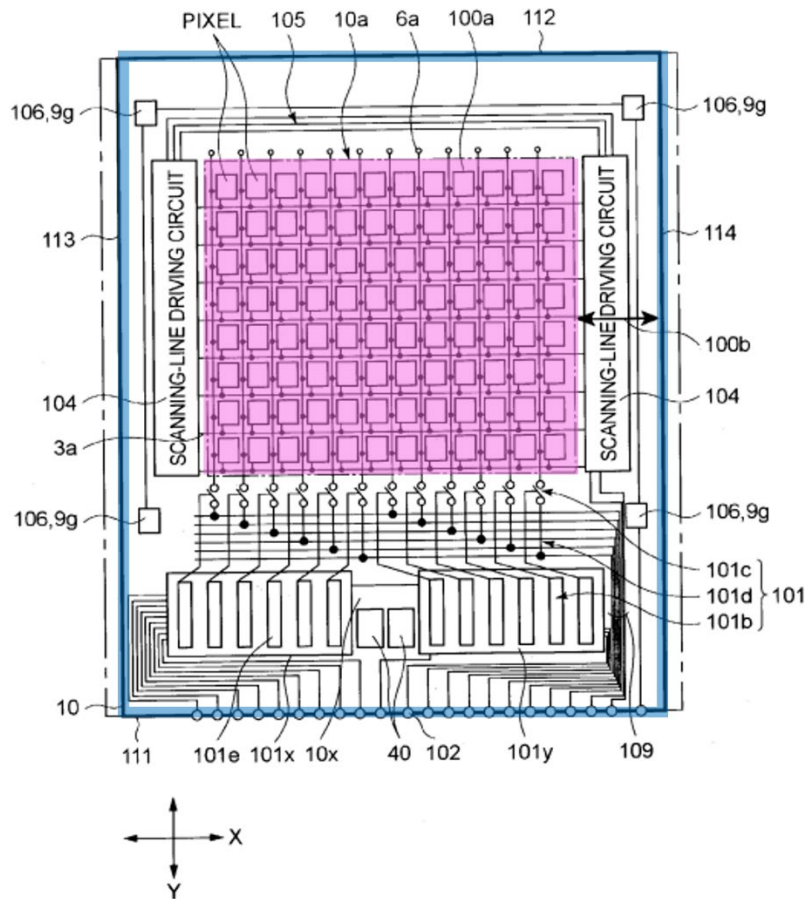
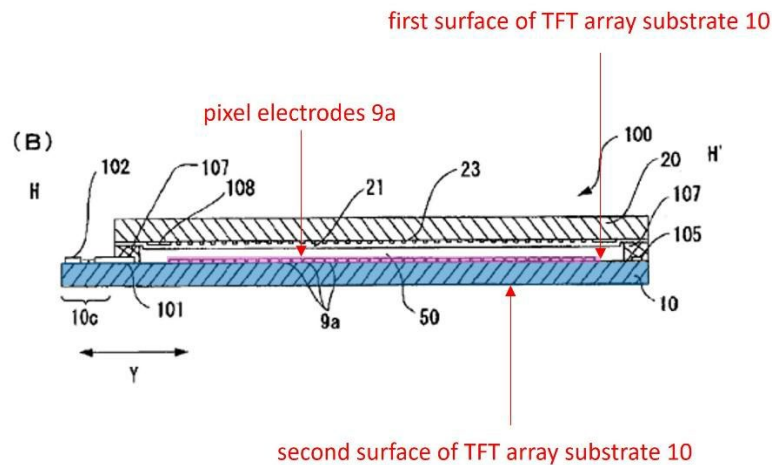


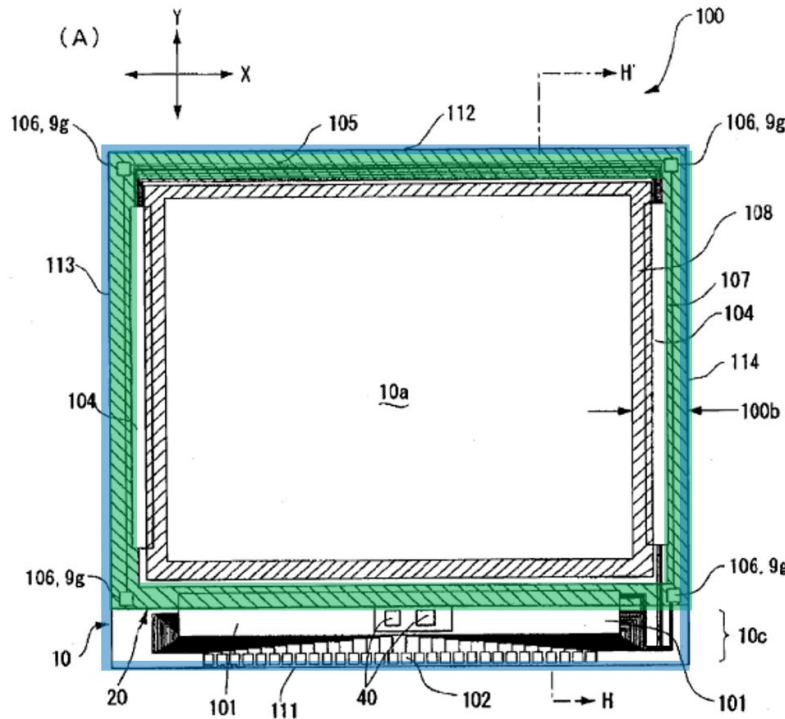
FIG.2

Fujikawa at Fig. 2 (image display region 10a in pink and TFT array substrate 10 is in blue). Each pixel 100a includes “a pixel electrode 9a and a pixel-switching TFT 30 for controlling the pixel electrode 9a.” *Fujikawa* at [0058], [0061]. The matrix of pixels on TFT array substrate 10 is the “*pixel region*.” And as shown in Figure 1B below, the pixel region is on the first surface of TFT array substrate 10:



Fujikawa at Fig. 1B (annotated).

91. Finally, *Fujikawa* discloses “***a seal region.***” *Fujikawa* discloses that its liquid crystal device comprises a TFT array substrate 10 and a counter substrate 20. *Fujikawa* at [0046]. These two substrates are “bonded” to each other “by the sealing material 107.” *Fujikawa* at [0046]. *Fujikawa* highlights this sealing material 107 in Figure 1A and explains it comprises “an area shaded by downward-slanting lines”:

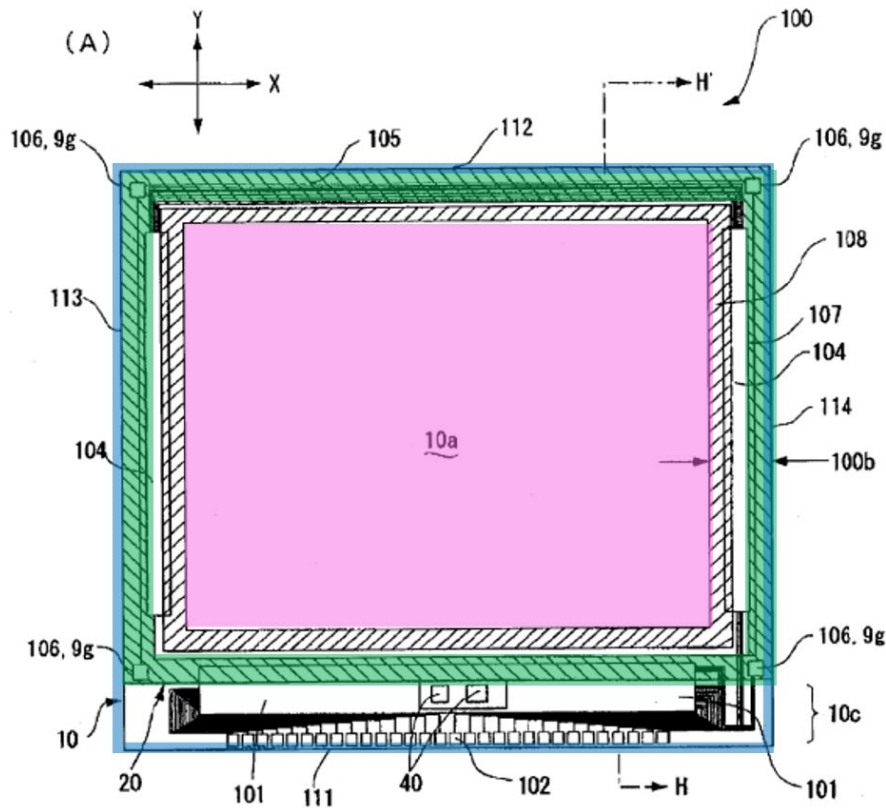


Fujikawa at Fig. 1A (sealing material 107 annotated in green, TFT array substrate 10 annotated in blue). *Fujikawa* explains that the sealing material 107 is “formed on a TFT array substrate 10” and “along the edge of a counter substrate 20.” *Fujikawa* at [0046]. According to *Fujikawa*, the sealing material “can be an adhesive made of a photosetting or thermosetting resin for bonding” and “mixed with a gap material, such as glass fibers or glass beads, that ensures a predetermined distance between the substrates.” *Fujikawa* at [0049]. The sealing material is in a “**sealing region**,” as claimed.

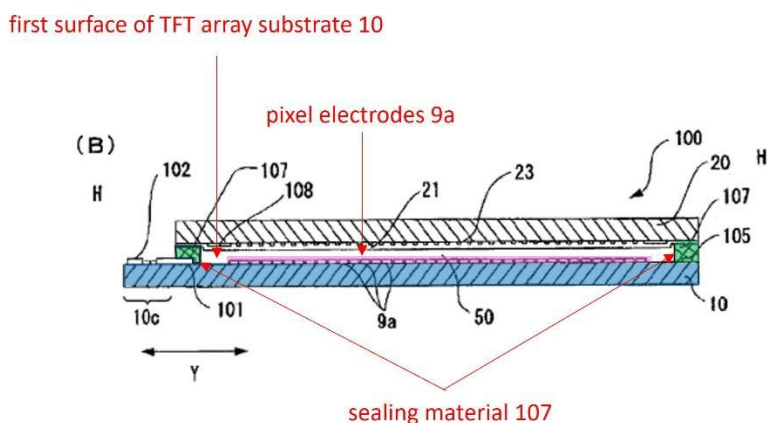
92. Moreover, this “**seal region**” is “**defined around the pixel region on a first surface of the first substrate.**” As noted above, *Fujikawa* explains display area

10a of the liquid crystal device comprises “a plurality of pixels formed in a matrix.”

Fujikawa at [0053]. This pixel region 10a is shown below in Figure 1A:



Id. at Fig. 1A (annotated). As illustrated above, the seal region (green) is defined around the perimeter of the pixel region (pink). This is also shown in Figure 1B, below:

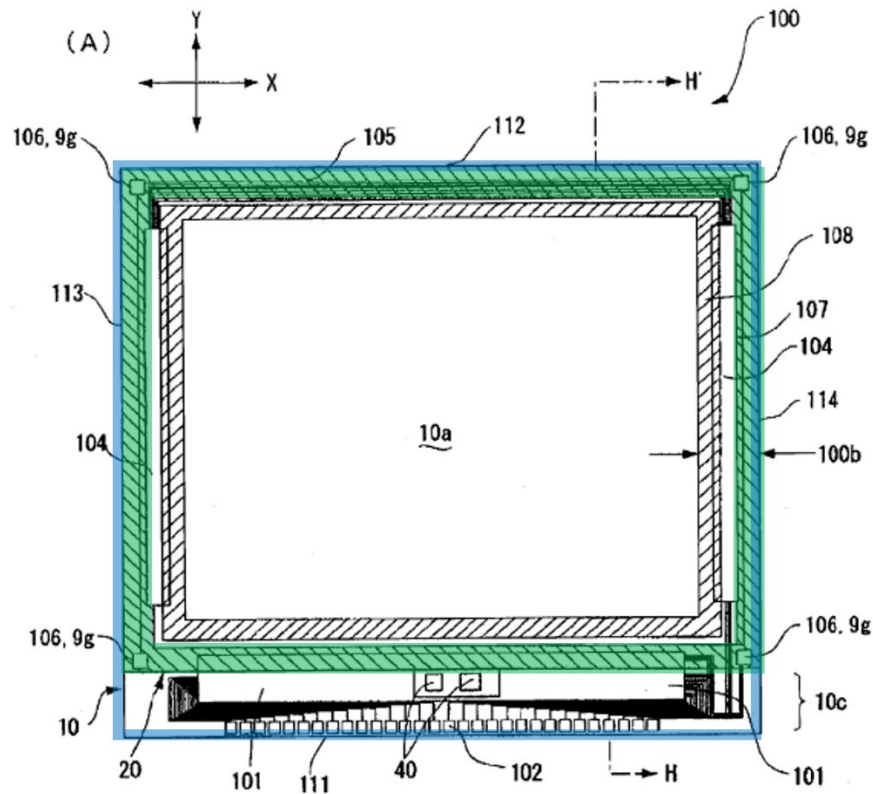


Fujikawa at Fig. 1B (annotated). As shown in this cross-section view above, the seal region (green) is defined on either side of the pixel region (pink). And, as discussed, both the pixel region and the seal area are formed on the “***first surface of the first substrate.***”

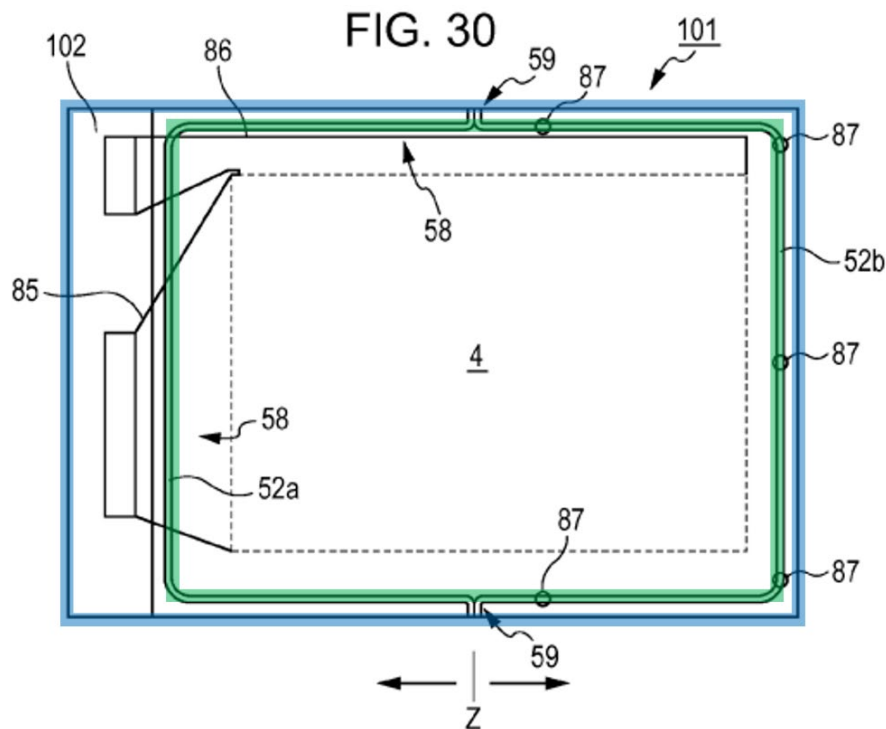
3. 7[b]: “***the pixel region including a plurality of pixels and a plurality of active elements, and the seal region forming a rectangular ring shape, wherein the active elements are thin film transistors disposed on the first substrate; and***”

93. In my opinion, *Fujikawa* discloses this limitation.

94. First, *Fujikawa* discloses its seal region “***form[s] a rectangular ring shape.***” *Fujikawa* discloses sealing material 107 is formed “along the edge of a counter substrate 20” around image display region 10a. *Id.*; e.g., *Fujikawa* at [0046]. This is shown in Figure 1A, which depicts sealing material 107 in the rectangular ring “area shaded by downward-slanting lines”:



Fujikawa at Fig. 1 A (annotated); *see Fujikawa* at [0046]. This is substantially similar to the rectangular ring shape seal region in Figure 30 of the '606 patent:



'606 patent at Fig. 30 (annotated).

95. Second, *Fujikawa* discloses its “*pixel region includ[es] a plurality of pixels and a plurality of active elements . . . wherein the active elements are thin film transistors disposed on the first substrate.*” As discussed, *Fujikawa* discloses its image display region 10a (“*pixel region*”) comprises “a plurality of pixels formed in a matrix” on TFT array substrate 10 (“*first substrate*”). *Fujikawa* at [0053]. This is shown below in Figure 2:

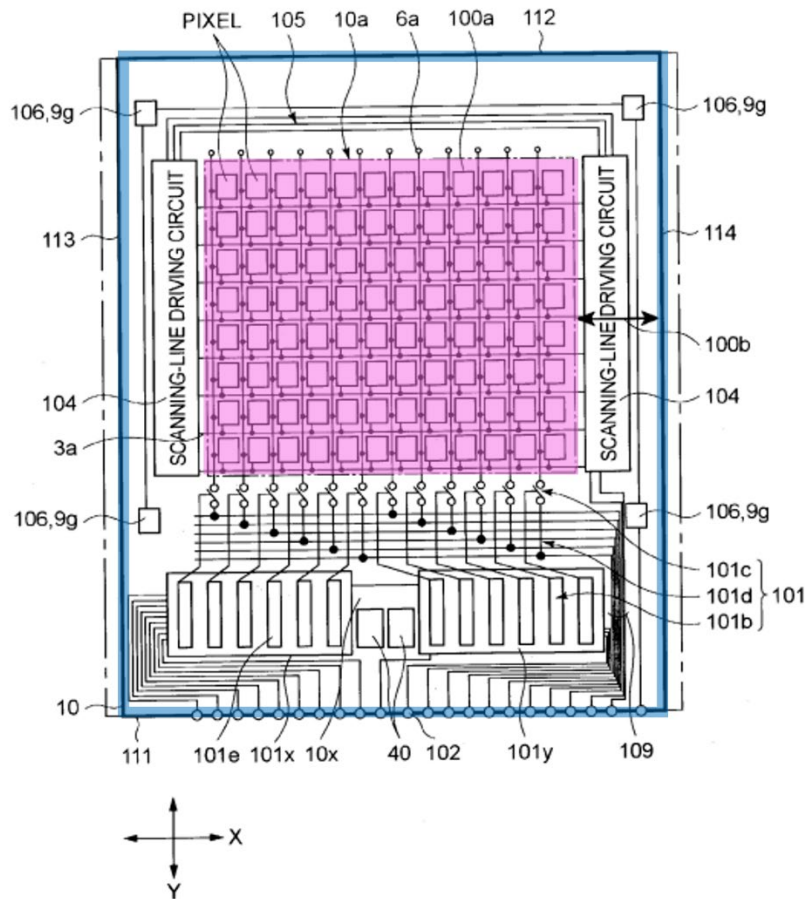


FIG.2

Fujikawa at Fig. 2 (image display region 10a in pink). *Fujikawa* further explains that each pixel in this plurality of pixels has “a pixel electrode 9a and a pixel-switching TFT 30,” “TFT” standing for “thin film transistor,” likewise formed on TFT array substrate 10. *Fujikawa* at [0058], [0061]. The pixel electrodes and TFTs are shown below in Figure 4:

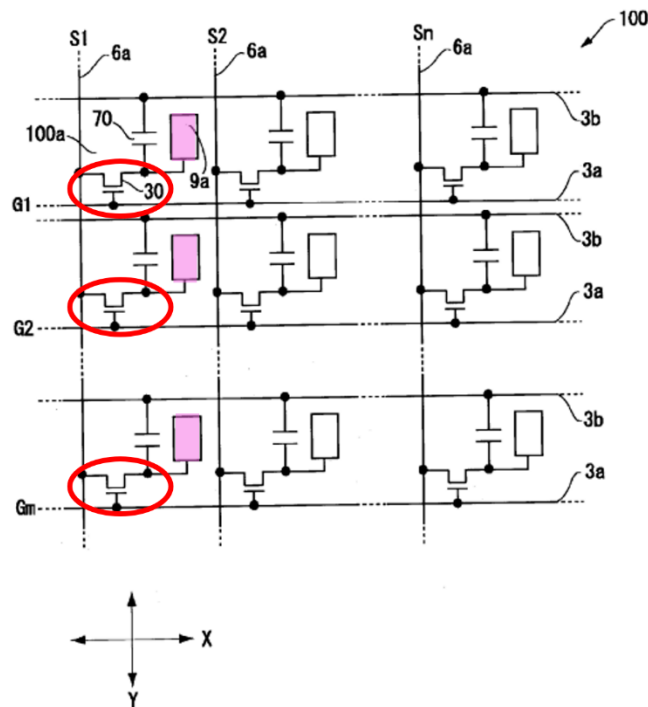


FIG.4

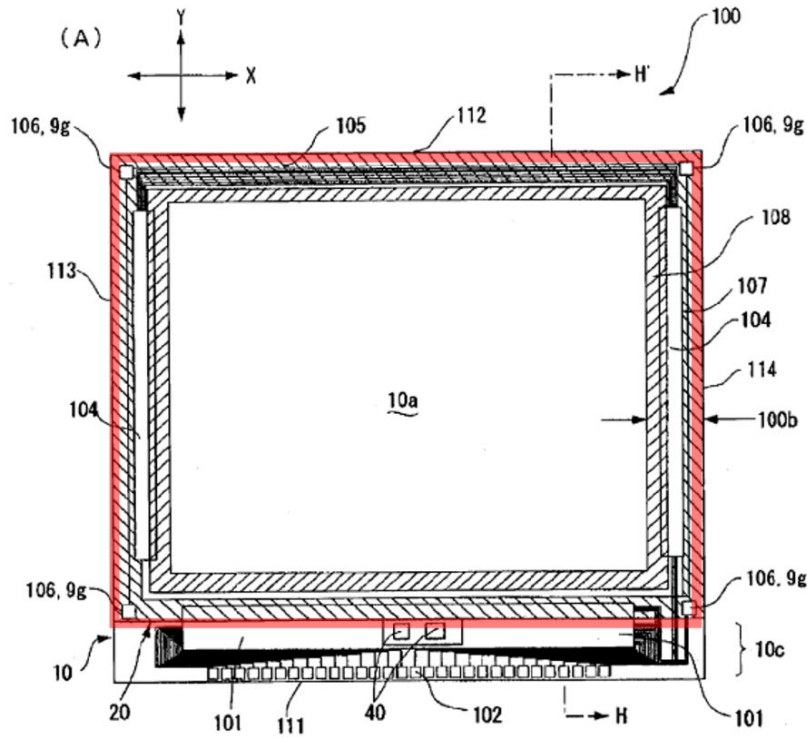
Fujikawa at Fig. 4 (exemplary pixel electrodes in pink, thin film transistors (TFTs) in red), [0050], [0053], [0058].

4. 7[c]: “a second substrate including a common electrode on a second surface; and”

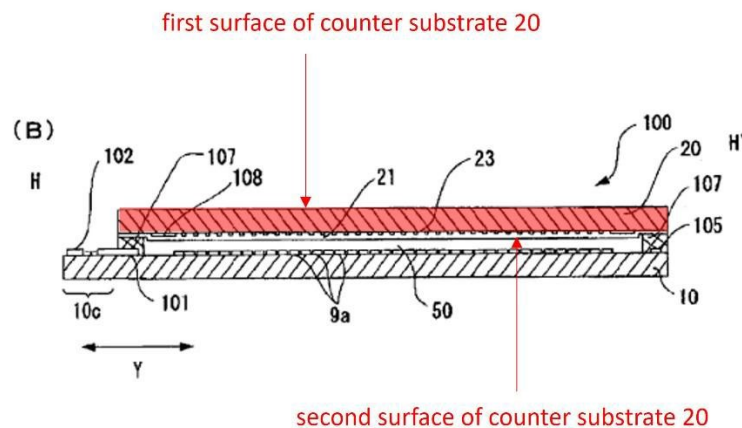
96. In my opinion, *Fujikawa* discloses this limitation.

97. As discussed, *Fujikawa* discloses a liquid crystal device comprising a TFT array substrate 10 (“**first substrate**”) “bonded” to counter substrate 20 “with a predetermined space therebetween by the sealing material 107.” *Fujikawa* at [0046],

[0049]. Counter substrate 20 is the claimed “*second substrate*,” and is shown below in Figure 1A:



Id. at Fig. 1A (counter substrate 20 is in red). Counter substrate 20 has a first surface (top) and a “*second surface*” (bottom), as shown below:



Fujikawa at Fig. 1B (annotated). *Fujikawa* explains disposed on “counter substrate 20” are the “counter electrodes 21.” *Fujikawa* at [0050], [0058], [0079]. A POSITA would have understood counter electrodes 21 are the claimed “*common electrode*” for a “constant voltage [is] supplied to the counter electrodes of the counter substrate 20” (*Fujikawa* at [0008]), and, as shown in Figure 1B (above) and Figure 9 (below), counter electrodes 21 are on the “*second surface*” (bottom) of counter substrate 20:

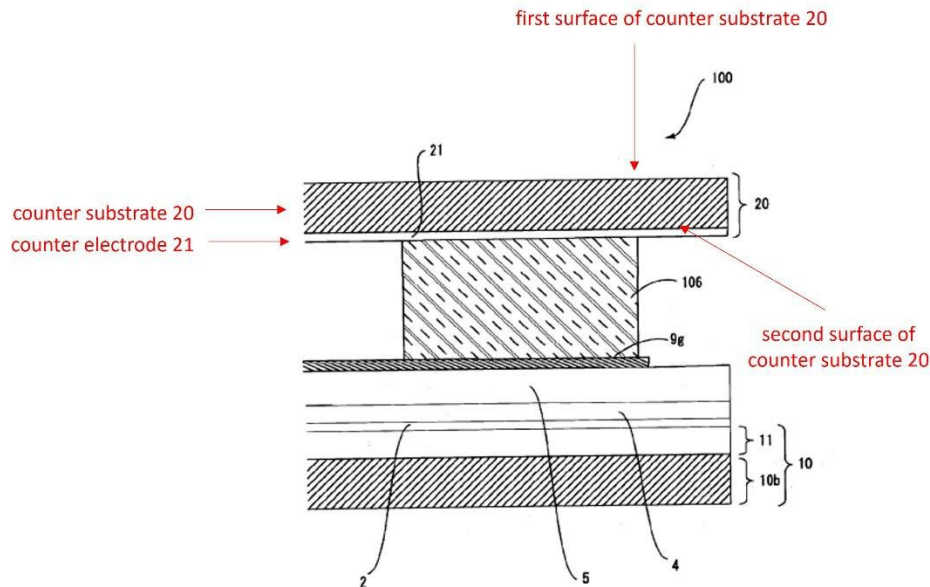


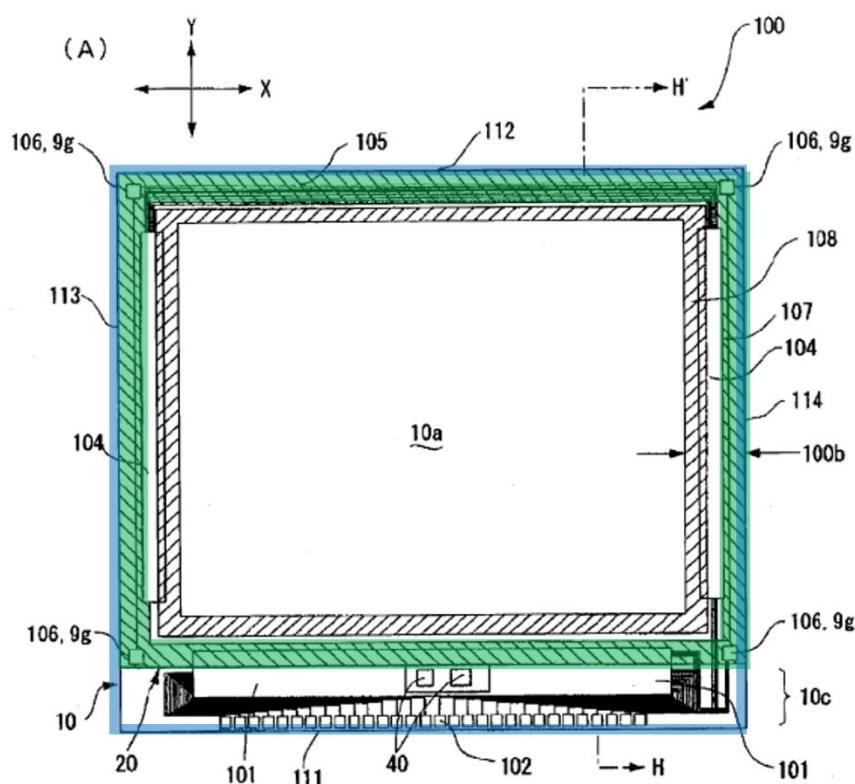
FIG.9

Fujikawa at Fig. 9 (annotated).

5. **7[d]: “a seal member bonding the first substrate and the second substrate so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels,”**

98. In my opinion, *Fujikawa* discloses this limitation.

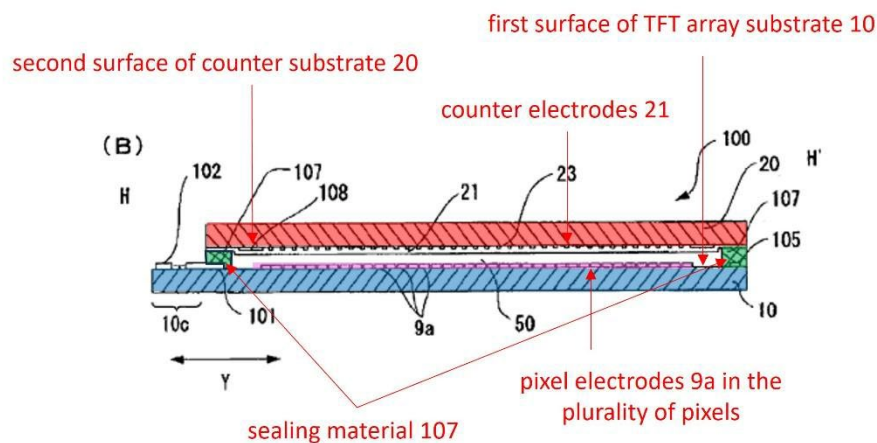
99. As discussed, *Fujikawa* discloses its liquid crystal device comprises a TFT array substrate 10 and a counter substrate 20. *Fujikawa* at [0046]. These two substrates are “bonded” “by the sealing material 107.” *Fujikawa* at [0046]; *see also* *Fujikawa* at [0004] (explaining TFT array substrate 10 and counter substrate 20 are “bonded with a sealing material 107”). *Fujikawa* depicts this sealing material 107 in Figure 1A:



Fujikawa at Fig. 1A (sealing material 107 annotated in green and TFT array substrate 10 annotated in blue). *Fujikawa* explains the sealing material 107 is “formed on a TFT array substrate 10” and “along the edge of a counter substrate 20.” *Fujikawa* at [0046]. According to *Fujikawa*, sealing material 107 “can be an adhesive made of a

photosetting or thermosetting resin for bonding” and “mixed with a gap material, such as glass fibers or glass beads, that ensures a predetermined distance between the substrates.” *Fujikawa* at [0049]. Sealing member 107 is a “***seal member bonding the first substrate and the second substrate,***” as claimed.

100. Moreover, as shown in Figure 1B, sealing member 107 bonds the TFT array substrate 10 and counter substrate 20 “*so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels.*”

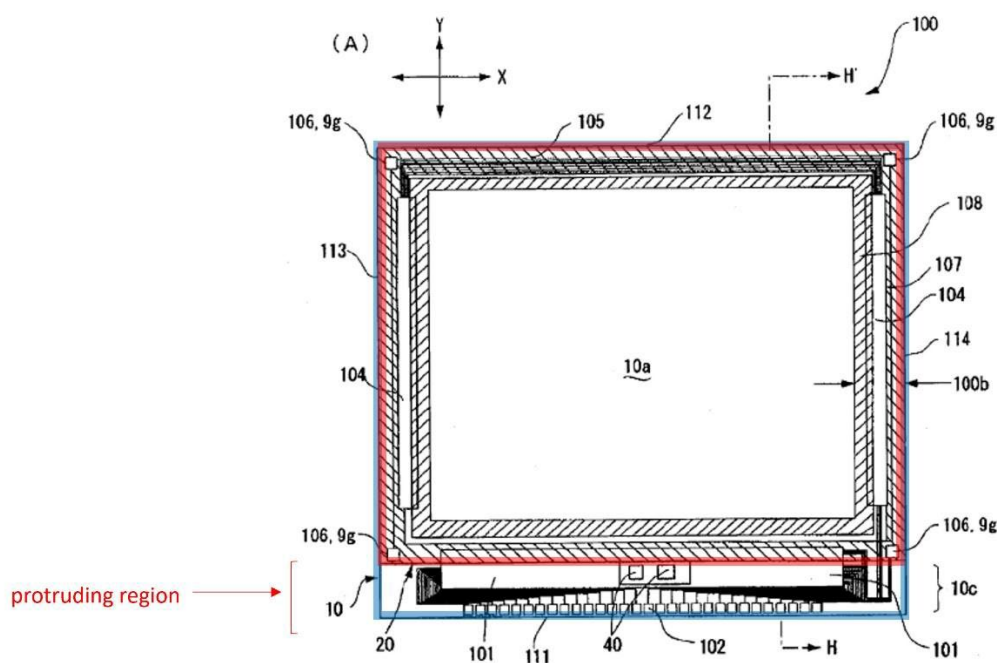


Fujikawa at Fig. 1B (annotated). As shown above, the first surface (top) of the TFT array substrate 10 is facing the second surface (bottom) of the counter substrate 20. And, in this arrangement, counter electrodes 21 are disposed opposite the plurality of pixels 9a.

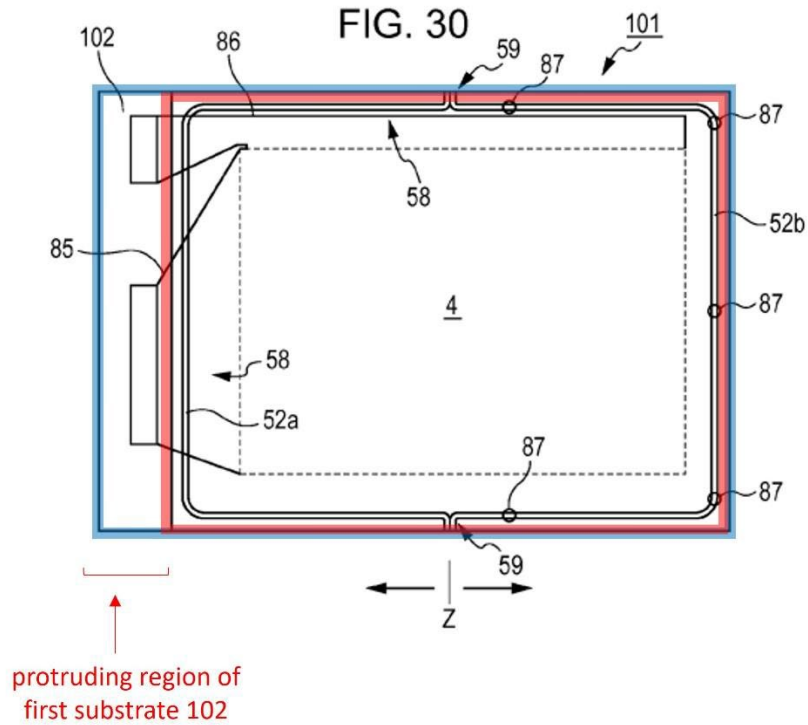
6. 7[e]: “*wherein the first substrate includes a protruding region which protrudes over the second substrate in a plan-view of the first substrate,*”

101. In my opinion, *Fujikawa* discloses this limitation.

102. Figure 1A of *Fujikawa* is a “plan view of a liquid crystal device” that shows the described invention “from the side of the counter substrate [20],” that is looking from the top down onto the top surface of TFT array substrate 10:



Fujikawa at Fig. 1A (annotated), [0045]. As shown in this plan view of the first substrate, TFT array substrate 10 is annotated in blue (“**first substrate**”), and counter substrate 20 is annotated in red (“**second substrate**”). TFT array substrate 10 is larger than counter substrate 20; it extends beyond the counter substrate 20 to include a “**protruding region.**” Indeed, *Fujikawa* describes region 10c as an “extended portion of the TFT array substrate 10 that *protrudes* from the edge of the counter substrate 20.” *Fujikawa* at [0009] (emphasis added); *Fujikawa* at [0046]. This is substantially similar to the protruding region in Figure 30 of the ’606 patent:

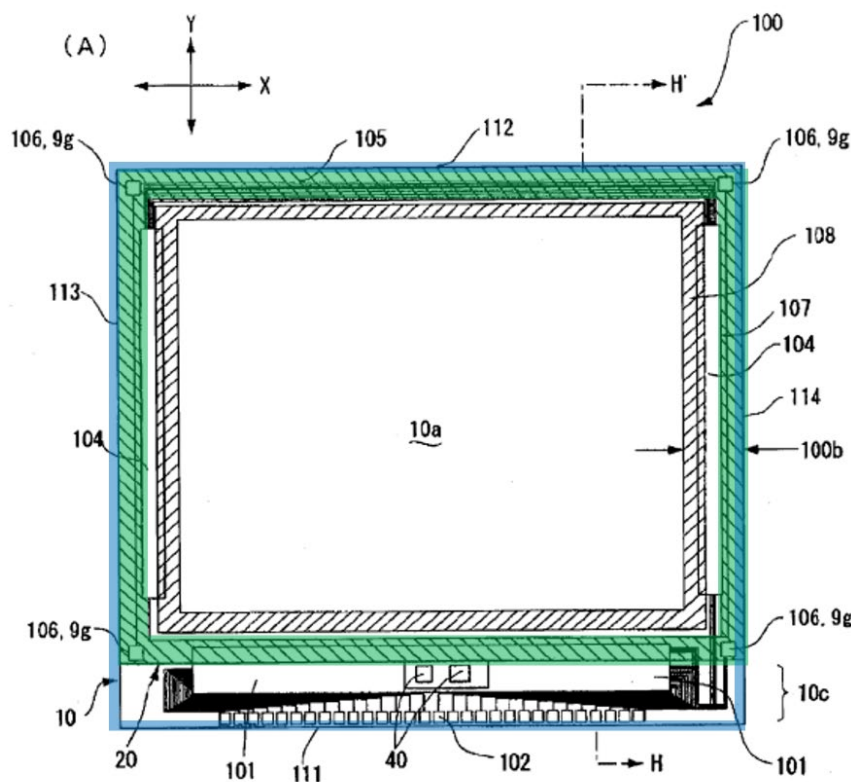


'606 patent at Fig. 30 (annotated).

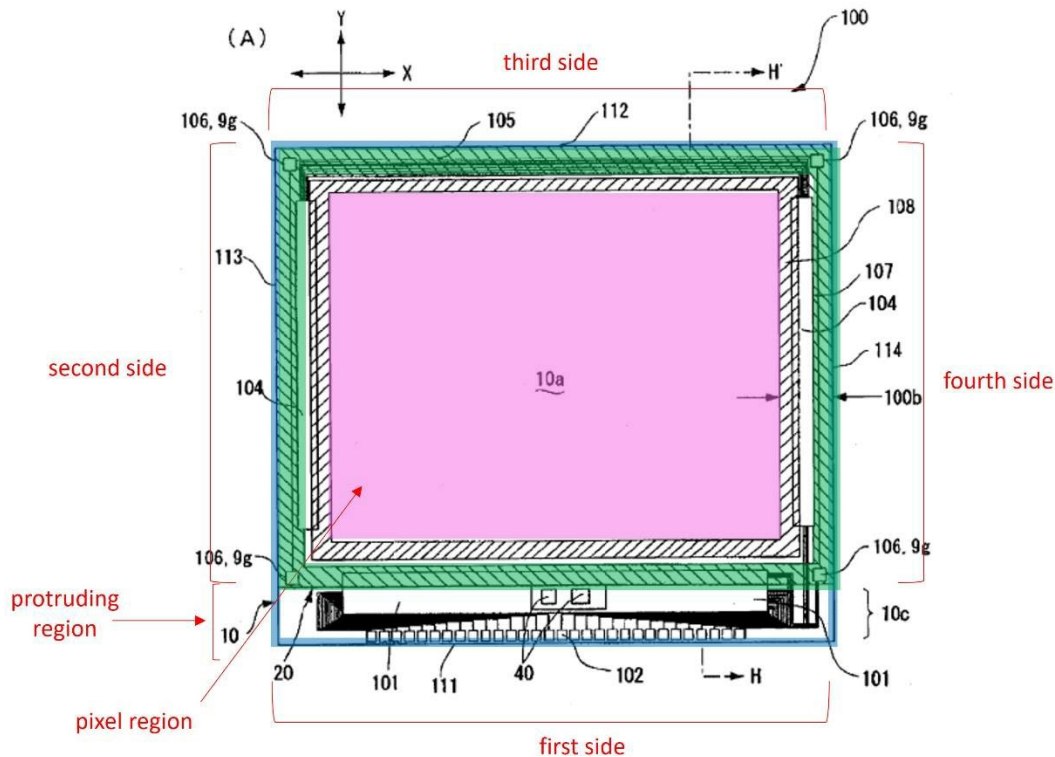
7. 7[f]: “the seal region includes a first side, a second side, a third side and a fourth side, the first side is positioned between the pixel region and the protruding region, and opposed to the third side, and the second side is opposed to the fourth side,”

103. In my opinion, *Fujikawa* discloses this limitation.

104. As discussed, the area containing sealing material 107 has a rectangular ring shape. Section X.A.3. This is shown below in Figure 1A:



Fujikawa at Fig. 1A (seal annotated in green). As *Fujikawa* explains that the TFT array substrate 10 has four “substrate edge[s],” 111, 112, 113, and 114 (*Fujikawa* at [0046]), so too does the rectangular ring shaped seal have four sides. And as shown below, the “***first side***” of the seal area sits between the protruding region of the first substrate (Section X.A.6) and the pixel region (Section X.A.2):

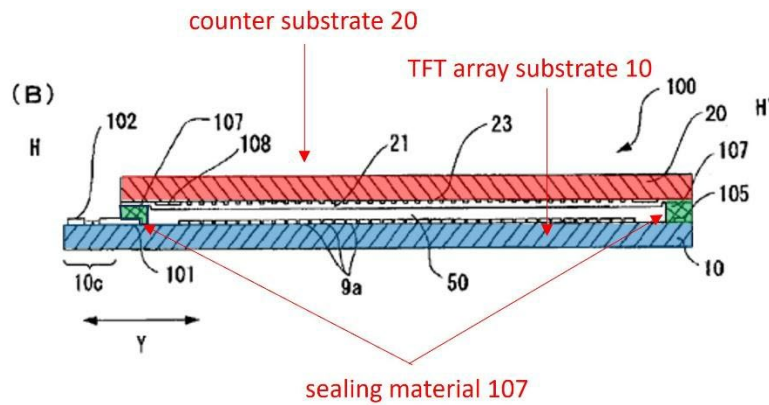


Fujikawa at Fig. 1A (annotated). The “**third side**” of the seal region is “**opposed to**” the “**first side**” (opposite sides of pixel region 10a), and the “**second side**” of the seal region is “**opposed to**” the “**fourth side**,” as claimed.

8. 7[g]: “***the seal member is disposed between the first substrate and the second substrate,***”

105. In my opinion, *Fujikawa* discloses this limitation.

106. As *Fujikawa* explains, sealing material 107 (“***seal member***”) is “formed on a TFT array substrate 10 . . . along the edge of a counter substrate 20.” *Fujikawa* at [0046], [0049]. And as shown in Figure 1B, the sealing material 107 is sandwiched between TFT substrate 10 and counter substrate 20 and is, thus, “***disposed between***” the two substrates:

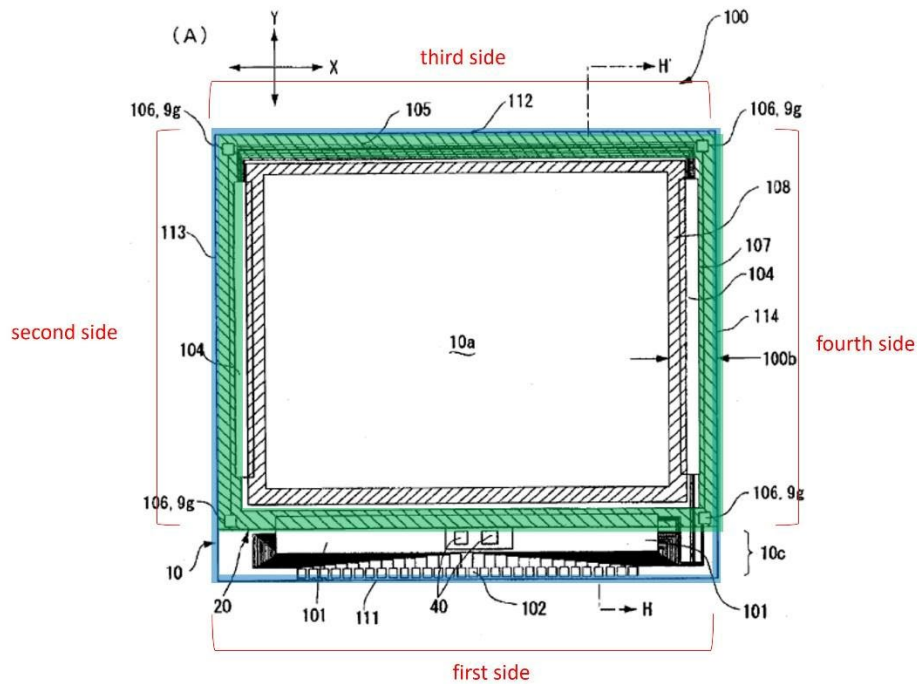


Fujikawa at Fig. 1B (annotated cross-sectional view).

9. 7[h]: “and positioned on the first side, the second side, the third side and the fourth side continuously, forms a closed-ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate, and is formed continuously around the entire pixel region without the use of a plug,”

107. In my opinion, *Fujikawa* discloses this limitation.

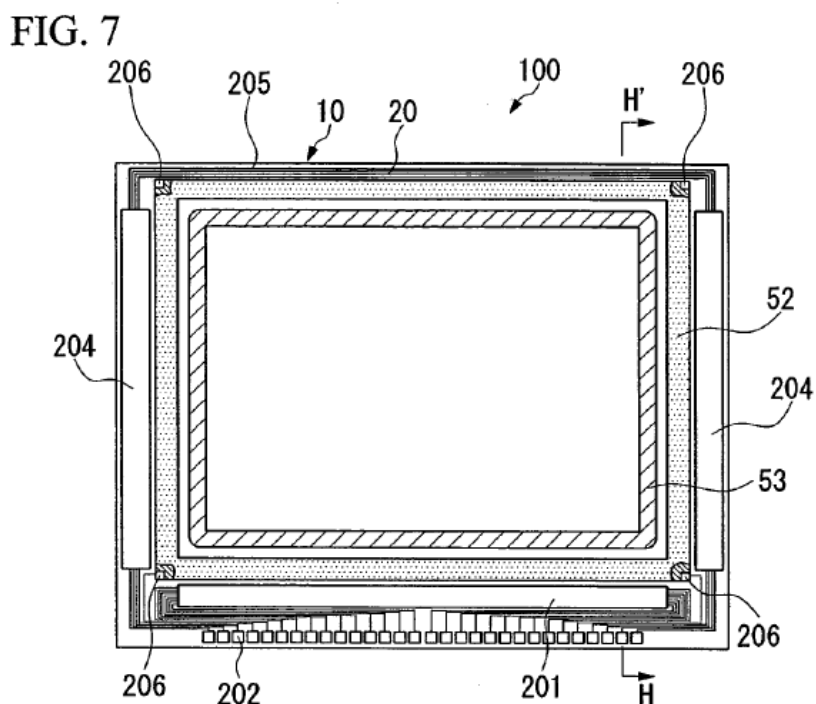
108. As discussed, *Fujikawa* discloses sealing material 107 (“*seal member*”) fills the entire “area shaded by downward-slanting lines” in the plan view of Figure 1A:



Fujikawa at Fig. 1A (sealing material 107 green); *Fujikawa* at [0046], [0049]. As shown above, sealing material 107 is positioned on all four sides of the rectangular “*seal region*” (*first, second, third, fourth*), as claimed.

109. A POSITA would have understood that, looking at this plan view in *Fujikawa*, the sealing material 107 is positioned “*continuously*” in a “*closed-ring shape*” along those four sides “*around the entire pixel region without the use of a plug.*” Several prior art references show a similar design and state that such design does not “include a liquid crystal inlet” and thus does not include a plug. *See, e.g.*, Ex. 1009 at Figs. 7-8, 18:36-44 (explaining in similar design “sealant 52 is formed in the shape of a frame which is closed in a region within the substrate surface, does

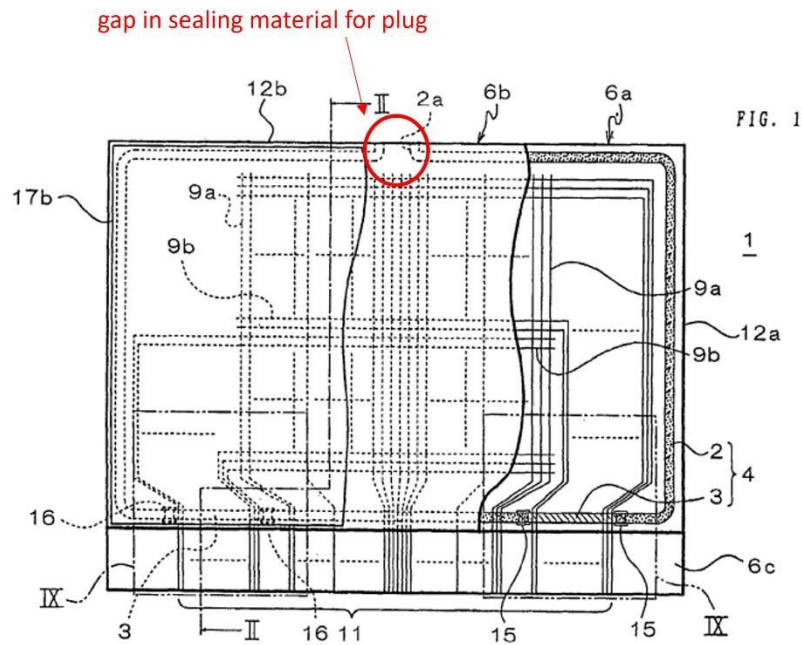
not include a liquid crystal inlet”); Ex. 1012 at Figs. 9-10, 23:12-21 (same). This is shown below in Ex. 1009, for example:



Ex. 1009 at Fig. 7; *see also Ikeguchi* at [0027]-[0029] (explaining the two substrates bonded together by a sealing material provided in a rectangular closed-loop shape”).

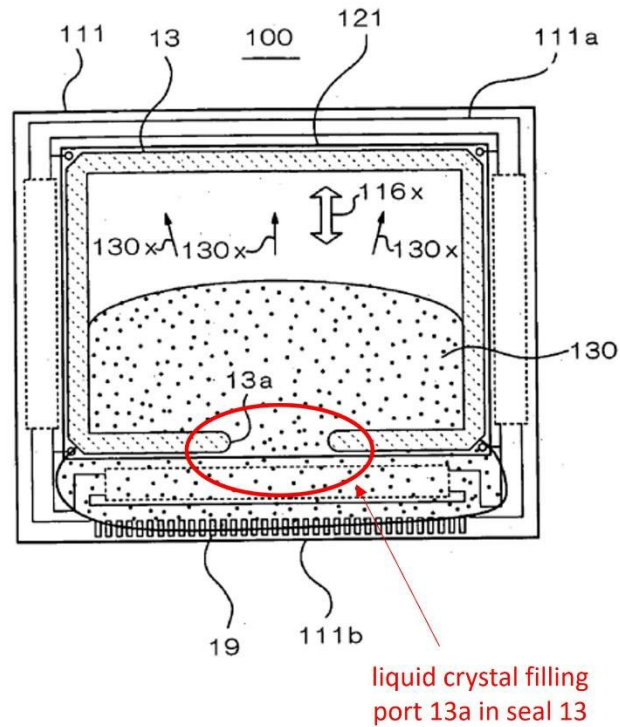
110. The sealing material 107 fills the entire rectangular ring-shaped area shaded by the downward-slanting lines that represent the “*seal region*” in Figure 1A of *Fujikawa*. *Fujikawa* at [0046], [0049], Fig. 1A. If a gap was contemplated and a plug required, the plan view would show as much. This can be seen, for example, in the *Miyazaki* and *Tanaka* references overcome during prosecution, where a gap is illustrated in the sealing material to allow the liquid crystal to fill the display, and a

plug would be used to fill that gap after filling. *E.g.*, Ex. 1010 (*Miyazaki*) at Fig. 1 (showing gap in the sealing material where plug would be used); Ex. 1011 (*Tanaka*) at Fig. 1, 3 (showing gap in the sealing material where plug would be used).



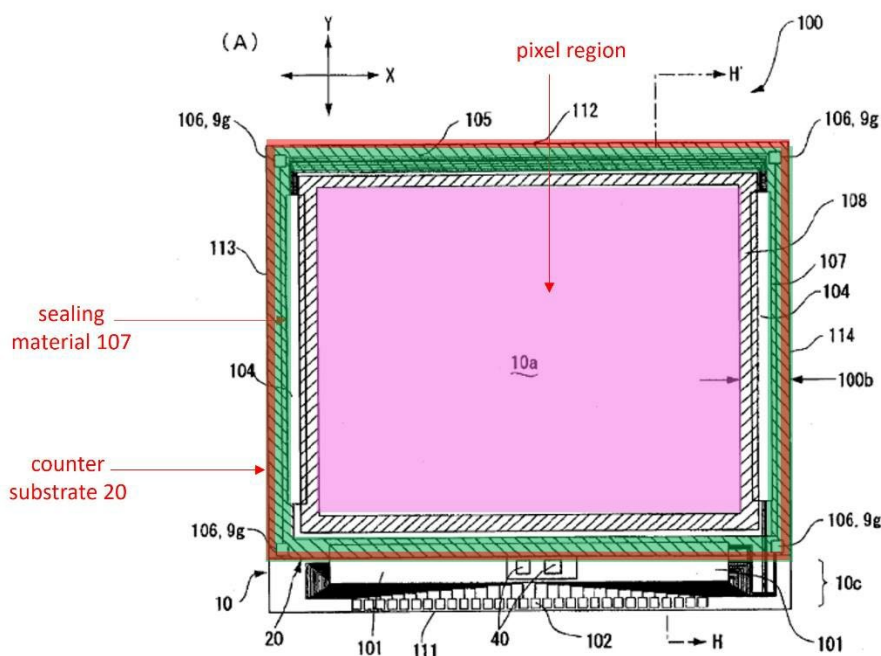
Ex. 1010 (*Miyazaki*) at Fig. 1 (annotated).

FIG. 1



Ex. 1011 (*Tanaka*) at Fig. 1.

111. Finally, *Fujikawa* discloses the sealing material 107 “*forms a closed ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate*”:



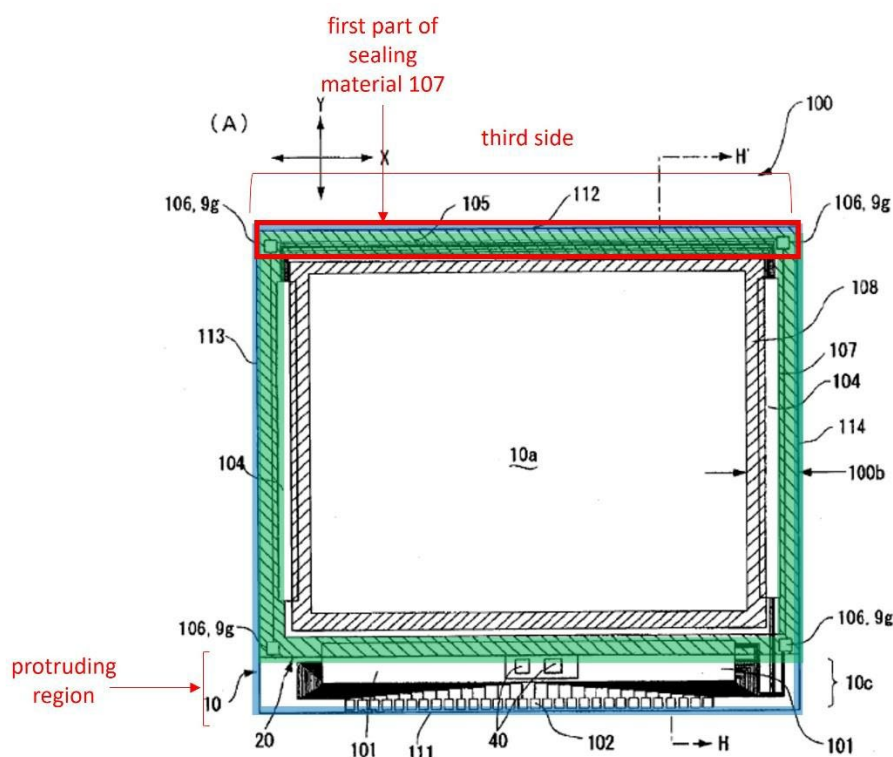
Fujikawa at Fig. 1A (annotated plan view). As shown above, image display area 10a with a plurality of pixels (“**pixel region**”) is “**positioned**” within sealing material 107 (“**seal member**”), and it does not “**protrud[e] from the second substrate in the plan-view of the first substrate.**”

10. 7[i]: “**a first part of the seal member disposed on the third side which is opposed to the protruding region with respect to the pixel region includes a plurality of conductive particles,**”

112. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

113. *Fujikawa* discloses “**a first part of the seal member disposed on the third side which is opposed to the protruding side with respect to the pixel region,**” as claimed. As discussed for limitations 7[f] and 7[h], *Fujikawa* discloses a third side

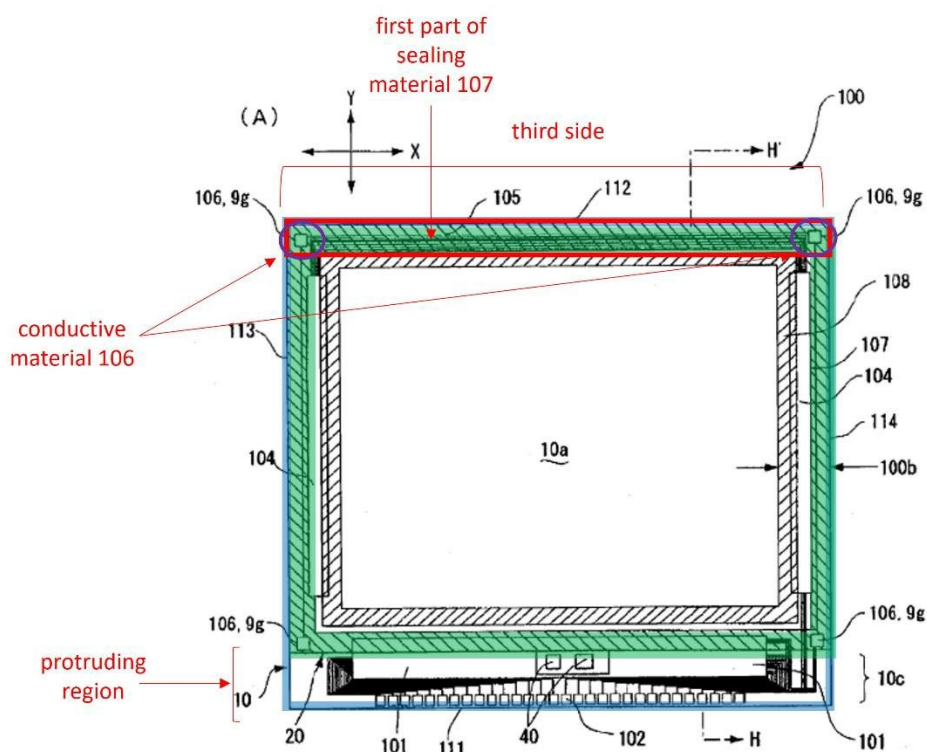
of a seal region (“area shaded by downward-slanting lines”) opposite the protruding region of TFT array substrate 10 relative image display region 10a (“*pixel region*”) that comprises sealing material 107 (“*seal member*”). Sections X.A.7, X.A.9. This is shown below in Figure 1A:



Fujikawa at Fig. 1A (annotated). The “***first part***” of sealing material 107 along the third side of the seal region (annotated above) extends from “edge” 113 of TFT array substrate 10 to “edge” 114 of TFT array substrate 10.

114. *Fujikawa* discloses or at least renders obvious the “***first part***” of that seal member on the third side of the pixel region “***includes a plurality of conductive particles.***” *Fujikawa* explains in sealing member 107 are “conductive materials 106

corresponding to the four corners of the counter substrate 20.” *Fujikawa* at [0047]. Conductive materials 106 electrically connect conductive electrodes 9g to counter electrodes 21 on counter substrate 20. *Fujikawa* at [0079]. “Conductive material 106 can be made of an epoxy resin adhesive component mixed with conductive particles such as silver powder and gold-plated fiber.” *Fujikawa* at [0079]. The conductive particles in conductive material 106 are the “*conductive particles*” in the claim. And as shown in Figure 1A below, there are “*a plurality*” of conductive materials 106, each comprising a plurality of conductive particles, in the “*first part*” of the sealing material 107 on the third side of the seal region:



Fujikawa at Fig. 1A (annotated). *Fujikawa* thus discloses “***a plurality of conductive particles***” in a “***first part***” of the seal member.

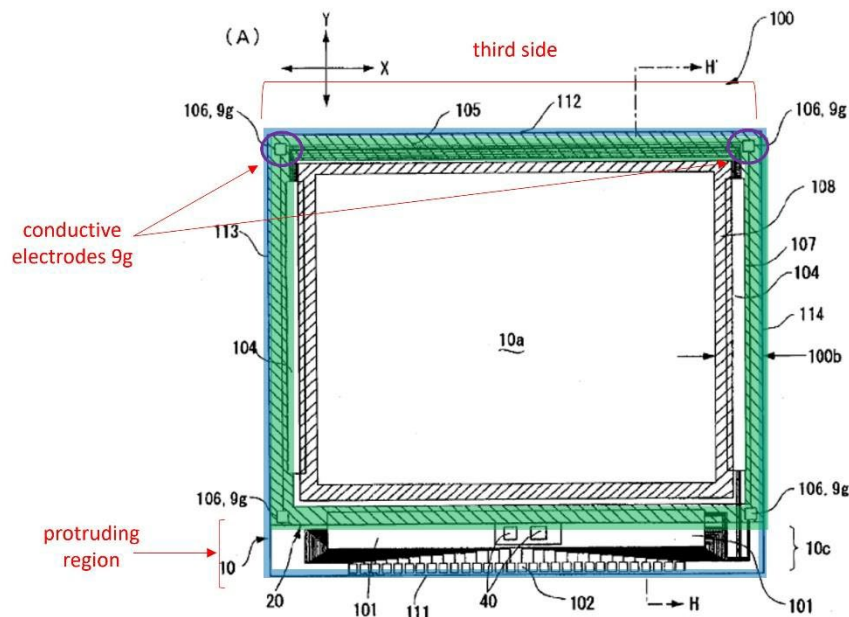
115. To the extent additional conductive particles are required, it would have been obvious to include more, for *Fujikawa* discloses that the “number of conductive electrodes 9g, and the like may be appropriately changed,” and the POSITA would have understood that “the like” refers at least to conductive materials 106. *Fujikawa* at [0047]. A POSITA would have been motivated to include additional conductive materials 106 with the corresponding plurality of conductive particles therein in the first part of the seal member to improve electrical connectivity between the first and second substrates by virtue of connecting the conductive electrodes 9g to counter electrodes 21 on counter substrate 20 (if additional conductive electrodes 9g are required, Section X.A.11). As discussed in Section V.C and elsewhere, additional points of electrical contact vertically from the common electrode are beneficial for retaining a stable voltage spatially across the common electrode. As a display scales to larger sizes, connecting to the common electrode at the corners of the display does not allow for a stable voltage across the electrode as the pixel voltages are varied at different times across the display; it can result in a large impedance in the connection to the common electrode because of the large resistance of a few narrow electrical connections. The introduction of additional electrical connections beyond just those in the corners will shorten the distance between those common electrode connections

at the edges of the display, decreasing spatial voltage variability. Several examples, including those discussed in Section V.C, have introduced conductive material into the seal material to afford conductivity over most of the seal rather than introducing a conductive material at individual gaps in the seals, decreasing overall resistance of the connection to the common electrode while reducing voltage variation across the common electrode. A POSITA would have understood that the additional regions of conductive material and, in turn, the consequent greater number of conductive particles would result in a more stable common electrode with a comparatively lower impedance. The examples discussed incorporate the dispersed conductive particles in a manner where the conductivity is realized only in the z-direction (the direction normal to both glass panes or substrates) by way of design, and the seal retains its otherwise electrically insulating characteristics in the lateral directions to allow for circuit design flexibility. A POSITA would have had a reasonable expectation of success in making such a modification, in my opinion. *Fujikawa* at [0047] (noting “number of conductive electrodes 9g, and the like may be appropriately changed”).

11. 7[j]: “*a plurality of dot conductive points are disposed on the third side of the first substrate, all of the plurality of the dot conductive points are electrically connected to the common electrode, and*”

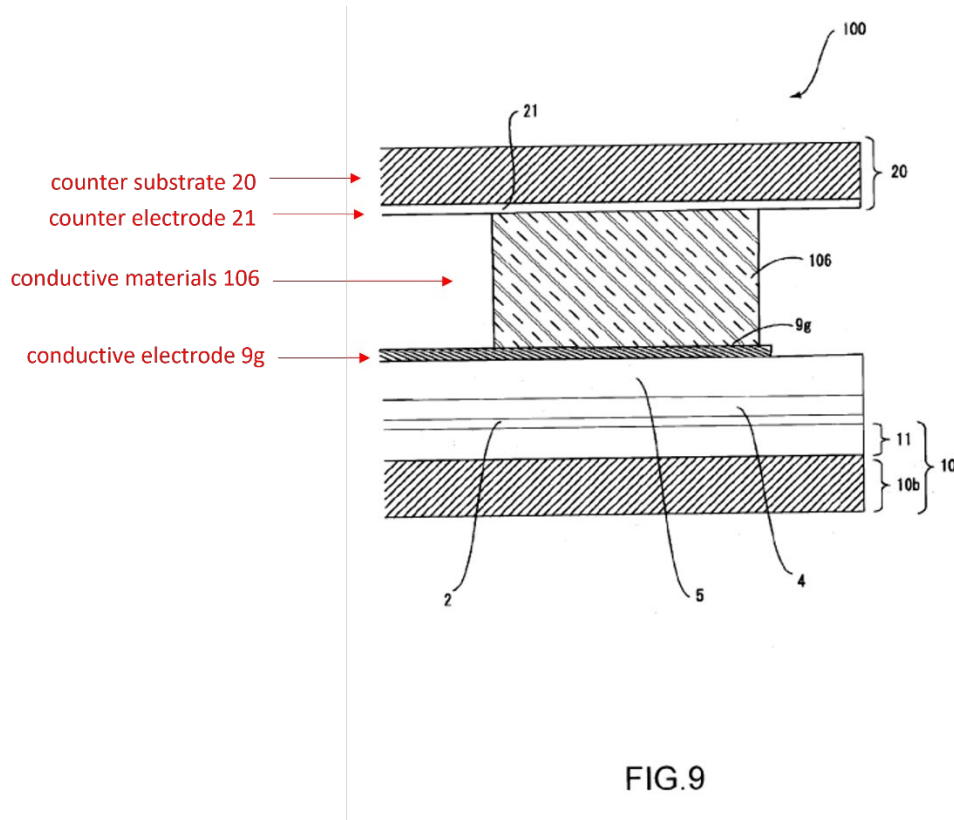
116. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

117. *Fujikawa* discloses “**a plurality of dot conductive points**” “**disposed on the third side of the first substrate**” that are “**electrically connected to the common electrode.**” *Fujikawa* discloses conductive electrodes 9g “are formed in the region of the TFT array substrate 10 overlapping with the counter substrate 20.” *Fujikawa* at [0079]. *Fujikawa* discloses “conductive electrode 9g and conductive materials 106 corresponding to the four corners of the counter substrate 20.” *Fujikawa* at [0047]. The conductive electrodes 9g along the “third side” of the TFT array substrate are annotated below in Figure 1A:



Fujikawa at Fig. 1A (annotated). In my opinion, conductive electrodes 9g are the claimed “**dot conductive points.**” ’606 patent at 38:46-52. *Fujikawa* further explains these conductive electrodes 9g are “electrically connected to the counter electrodes

21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates.” *Fujikawa*, [0079]. This is shown below, for example, in Figure 9:



Fujikawa at Fig. 9 (annotated). *Fujikawa* accordingly discloses “a **plurality of dot conductive points . . . disposed on the third side of the first substrate**” “**electrically connected to the common electrode.**”

118. To the extent additional dot conductive points are required by the claim, it would have been obvious to add more because *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa* at [0047]. A POSITA would have been motivated to include additional dot conductive points on the third side to improve the electrical connectivity between substrates. As

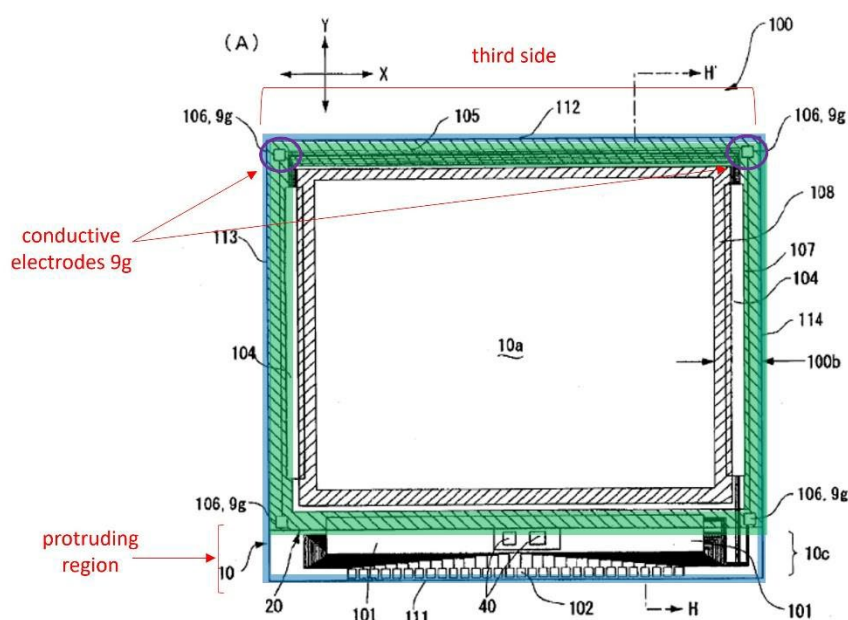
discussed above in Section V.C and elsewhere, having additional points of electrical contact vertically from the common electrode is beneficial for retaining a stable voltage spatially across the common electrode. As the display scales to larger sizes, connecting to the common electrode at the corners of the display does not allow for a stable voltage across the electrode as pixel voltages are varied at different times across the display, and additionally can result in a large impedance in the connection to the common electrode because of the large resistance of a few narrow electrical connections. Introducing additional electrical connections beyond the corners will shorten the distance between those common electrode connections at the edges of the display, decreasing spatial voltage variability. A variety of examples, including those discussed in Section V.C, have introduced conductive material into the seal material to afford conductivity over most of the seal rather than just introducing a conductive material at individual gaps in the seals, decreasing overall resistance of the connection to the common electrode while reducing voltage variation across the common electrode. The additional regions of conductive material, and the associated greater number of conductive particles, would result in a more stable common electrode with a comparatively lower impedance. The examples discussed above incorporate the dispersed conductive particles in a manner where the conductivity is realized only in the z-direction (direction normal to both panes or substrates) by way of design, and the seal retains its otherwise electrically insulating characteristics in

the lateral directions to allow for circuit design flexibility. A POSITA would have had a reasonable expectation of success in making this modification, in my opinion. *Fujikawa* at [0047] (noting “number of conductive electrodes 9g, and the like may be appropriately changed”).

12. 7[k]: “each of the plurality of the dot conductive points are spaced part from each other”

119. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

120. As discussed, *Fujikawa* discloses or renders obvious “***a plurality of dot conductive points.***” Section X.A.11. And as shown in Figure 1A, below, these “***dot conductive points***” (“conductive electrodes 9g”) are also “***spaced apart from each other,***” as claimed:



Fujikawa at Fig. 1A (annotated).

13. 7[1]: “*wherein the first substrate includes a plurality of wiring lines that connect to the plurality of active elements, and the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points.*”

121. In my opinion, *Fujikawa* discloses this limitation.

122. *Fujikawa* discloses “terminals 102” formed “along a substrate edge 111 of the TFT array substrate 10.” *Fujikawa* at [0055]. “A plurality of lines 109 . . . are routed from these terminals 102” on the first substrate (*id.*) and provide signals to the data line driving circuit 101 (*see, e.g., Fujikawa* at [0007]). *Fujikawa* explains that the “data line driving circuit 101 is [also] formed along a substrate edge 111 so as to overlap with a part of the s[e]aling material 107.” *Fujikawa* at [0046]. This data line driving circuit 101 includes “shift register circuits 101b, sample hold circuits 101c, . . . [and] image signal lines 101d.” *Fujikawa* at [0056]-[0057]. *Fujikawa* explains sample hold circuits 101c are “in a one-to-one correspondence with the data lines 6a.” *Fujikawa* at [0057]. To that end, *Fujikawa* discloses a “plurality of data lines 6a” on TFT array substrate 10 (“**first substrate**”) “electrically connected to a source of the TFT 30” (“**active element**”) to supply the “pixel signal.” *Fujikawa* at [0054]. This is shown below in Figure 4:

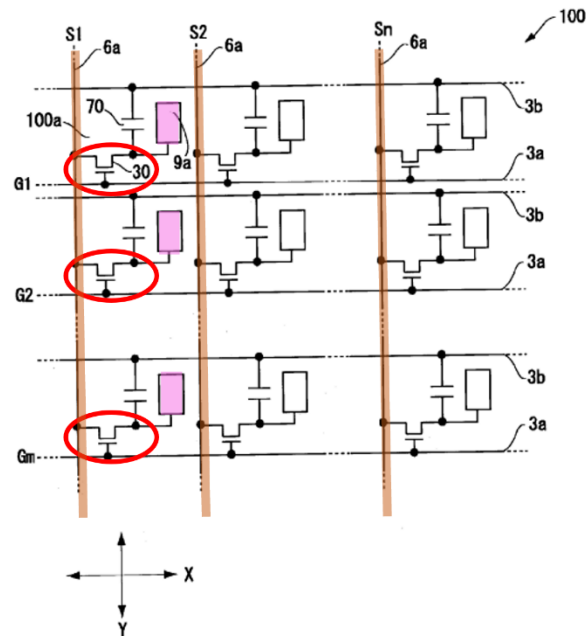


FIG.4

Fujikawa at Fig. 4. *Fujikawa* thus discloses “***the first substrate includes a plurality of wiring lines that connect to the plurality of active elements.***” Each wiring line in *Fujikawa* comprises three line segments, i.e., data line 6a, image signal line 101d, and line 109. The wiring lines may be enabled or disabled depending on control signals provided to shift registers 101b. When a shift register 101b outputs an enabling signal, the corresponding hold circuit 101c (a switch) is closed; and as a result, the corresponding data line 6a, signal line 101d, and line 109 are all directly connected so data signals on the corresponding terminal 102 are provided directly to the corresponding pixel electrodes in the display region. Further, *Fujikawa* discloses

these lines (as shown in Figure 2) “*extend onto the protruding region across the seal member without connecting to the dot conductive points*”:

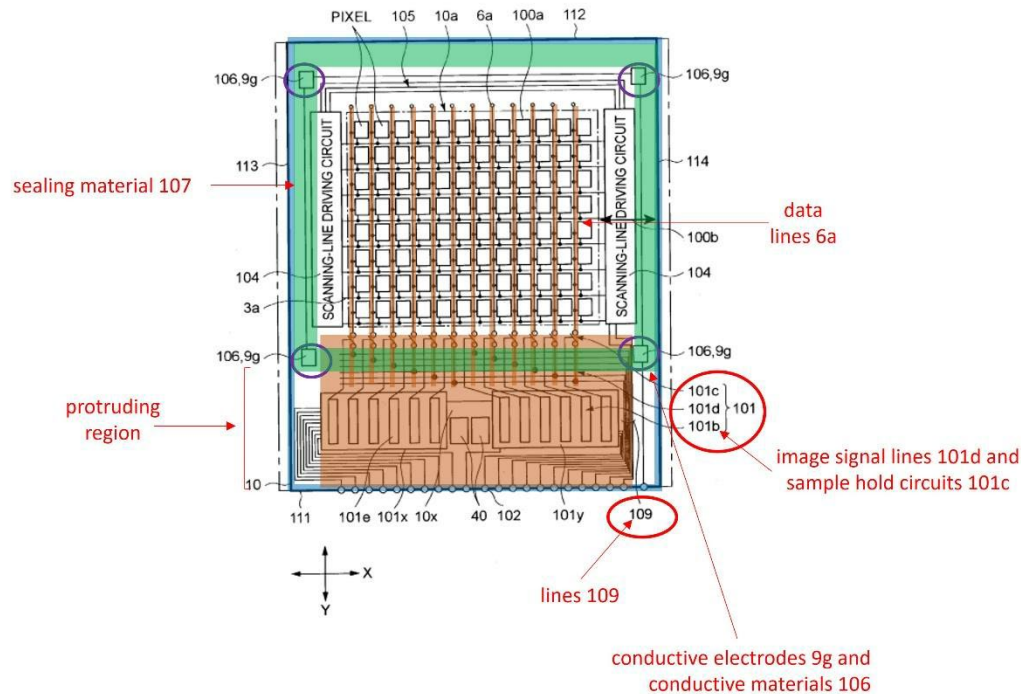


FIG.2

Fujikawa at Fig. 2. A POSITA would have understood these lines would extend from the pixel display region across the sealing member to provide “pixel signals” to pixel electrodes in the display region without connecting to the dot conductive points.

B. Dependent Claim 8

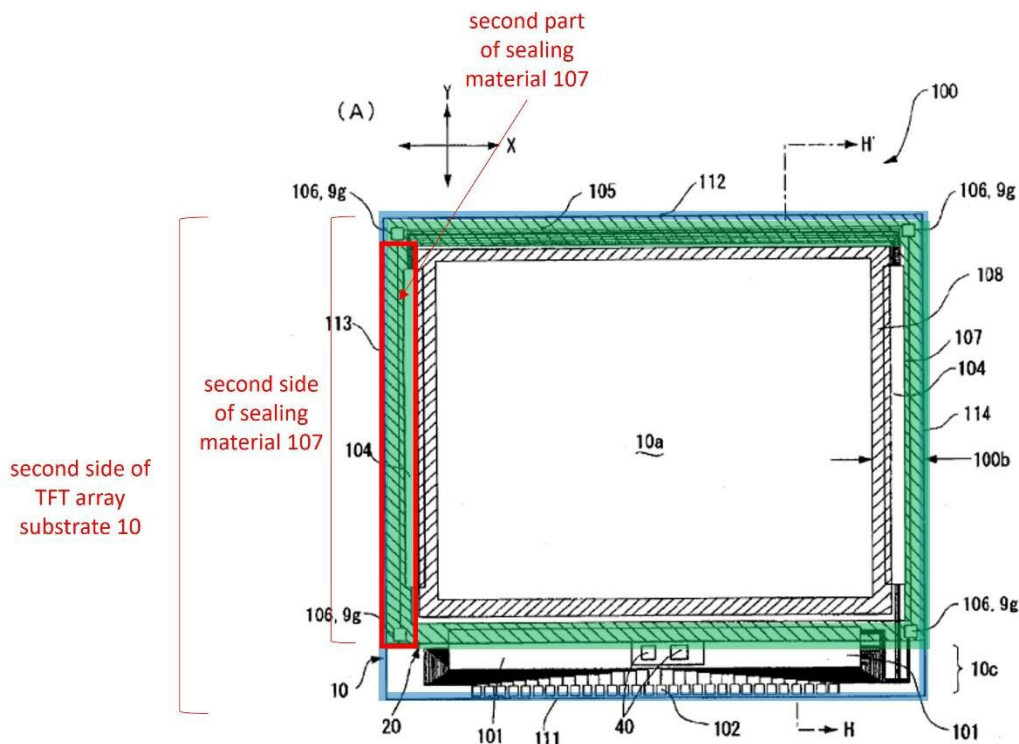
1. 8[pre]: “*The display device, according to claim 7*”

123. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 7, in my opinion. Section X.A.

2. 8[a]: “*wherein the first substrate includes a first conductive point on the second side and the seal member includes a second part of the seal member on the second side,*”

124. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

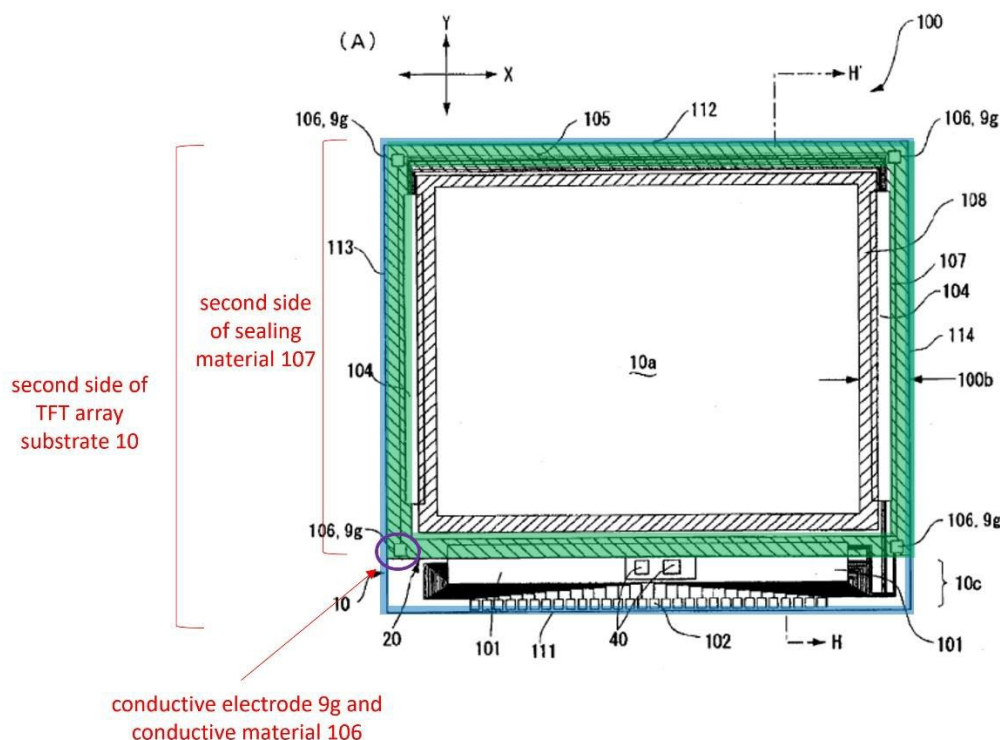
125. First, *Fujikawa* discloses a “*second side*” of the “*first substrate*”:



Fujikawa at Fig. 1A (annotated). *Fujikawa* also discloses a “*second part of the seal member on the second side,*” as shown above.

126. Second, as discussed, *Fujikawa* discloses or at least renders obvious a first conductive point on the second side of the first substrate. See Sections X.A.11-X.A.12. For example, *Fujikawa* discloses conductive electrode 9g and conductive

material 106 at the bottom left corner of TFT array substrate 10 in Figure 1A, which is on the second side of the first substrate.



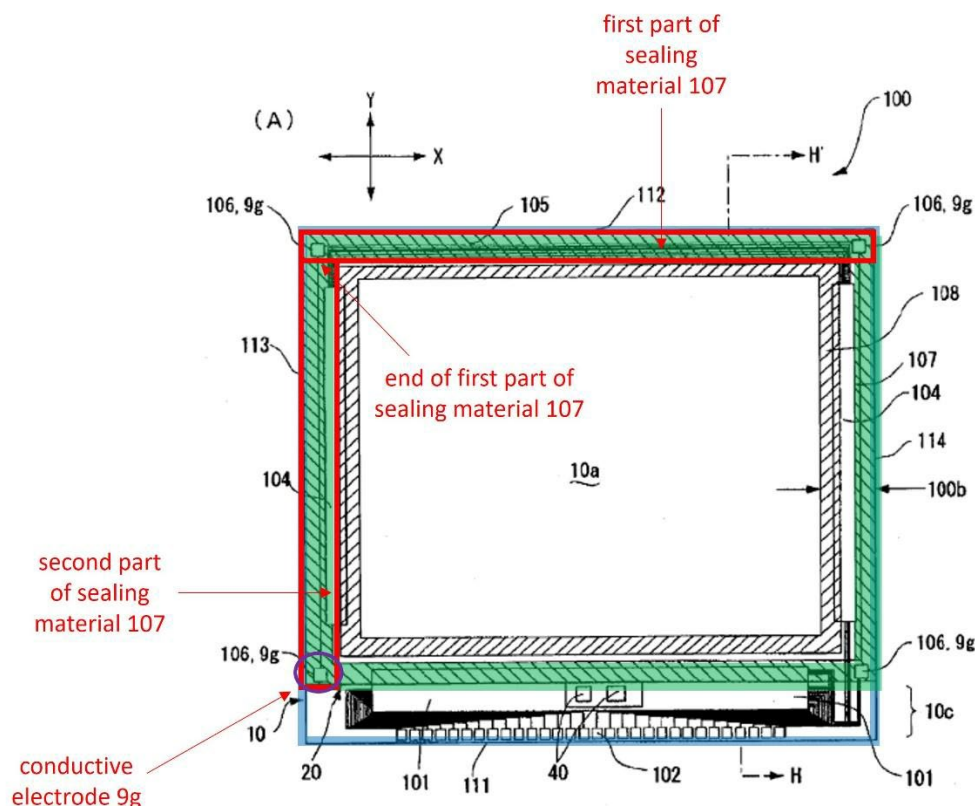
Fujikawa, Fig. 1A (annotated). The conductive electrode 9g in the bottom left corner is the “***first conductive point***” on the second side of the first substrate. It would have also been obvious to include a plurality of conductive points on the second side of the first substrate, for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed,” the conductive electrodes 9g disclosing the claimed conductive points. *Fujikawa*, [0047]; Sections X.A.11-X.A.12.

3. 8[b]: “the second part of the seal member extends from one end of the first part of the seal member over the first conductive point on the second side, and the second part of

*the seal member includes a plurality of conductive particles,
and,”*

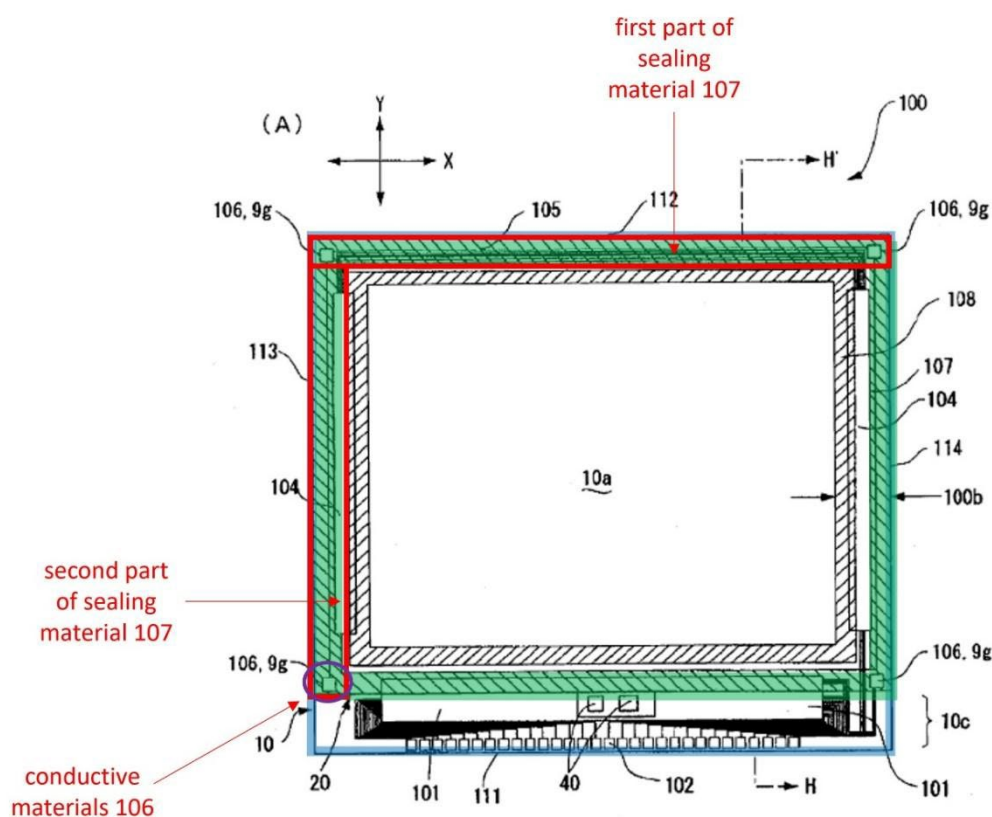
127. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

128. First, as discussed in the previous section for limitation 8[a], *Fujikawa* discloses a “**second part**” of the “**seal member**” (sealing material 107). *See* Section X.B.2. And as discussed above for limitation 7[i], *Fujikawa* also discloses a “**first part**” of that “**seal member**” (sealing material 107). *See* Section X.A.10. As shown below, the “**second part**” of the “**seal member extends from one end of the first part of the seal member over the first conductive point on the second side,**” as claimed:



Fujikawa at Fig. 1A (annotated).

129. Second, as discussed above, *Fujikawa* also discloses or at least renders obvious a plurality of conductive particles in the second part of the seal member. Section X.A.10. For example, *Fujikawa* Figure 1A discloses conductive electrode 9g and conductive material 106 at the bottom left corner of TFT array substrate 10:



Fujikawa at Fig. 1A (annotated). The conductive particles in conductive material 106 of sealing material 107 in the bottom left corner are the claimed “***plurality of conductive particles.***” It would have also been obvious to include a plurality of conductive particles in the second part of the seal member as *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed,”

and the POSITA would have understood that “the like” refers at least to conductive materials 106. *Fujikawa* at [0047]; Section X.A.10.

4. **8[c]: “wherein the first conductive point is electrically connected to the common electrode.”**

130. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

131. As discussed for limitation 7[j], *Fujikawa* discloses each conductive electrode 9g (“**conductive point**”) is “electrically connected to the counter electrodes 21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates.” *Fujikawa* at [0079]; Section X.A.11. This is shown below in Figure 9:

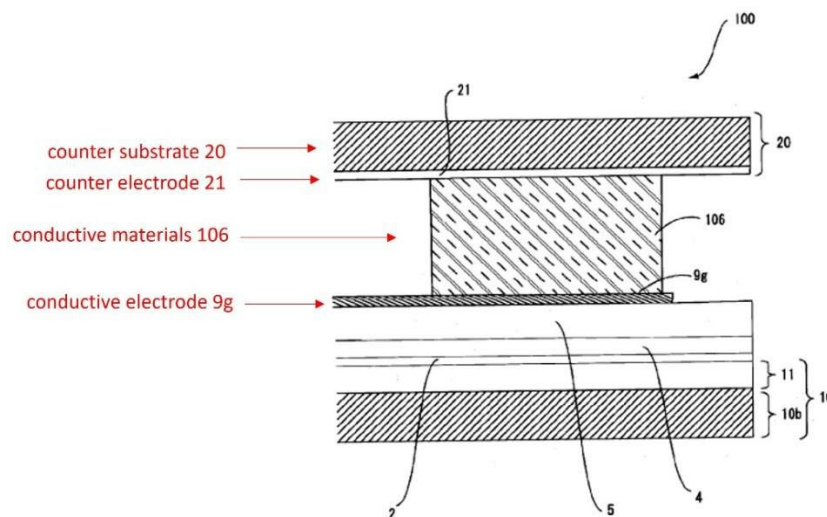


FIG.9

Fujikawa at Fig. 9 (annotated).

C. Dependent Claim 9

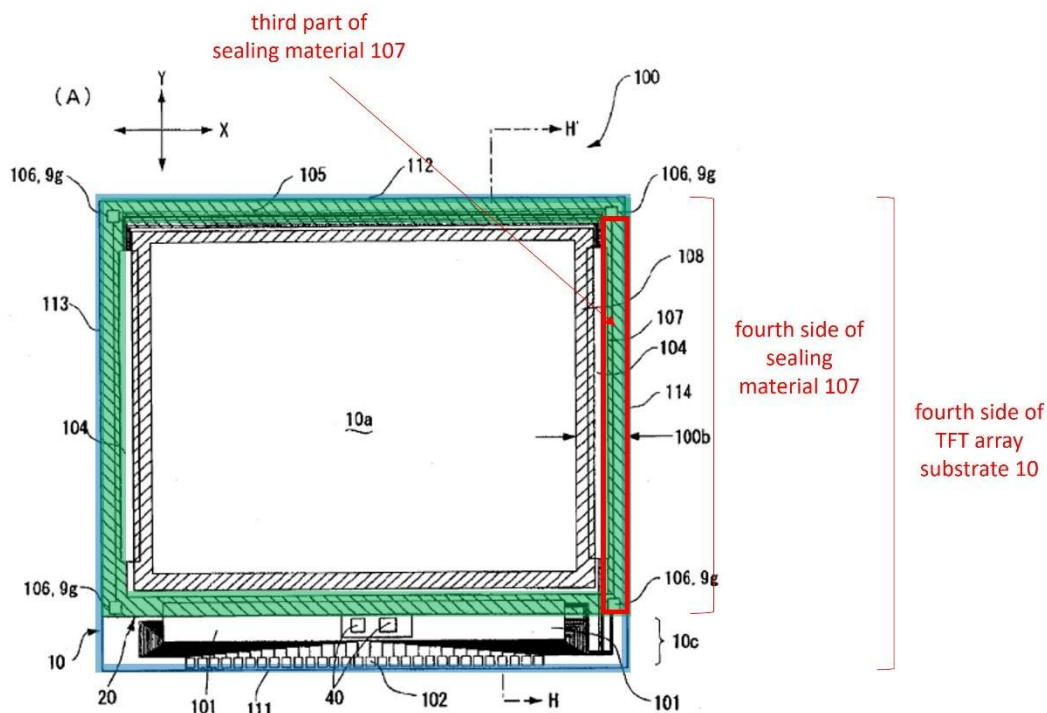
1. 9[pre]: “The display device, according to claim 8”

132. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 8, in my opinion. Section X.B.

2. 9[a]: “wherein the first substrate includes a second conductive point on the fourth side and the seal member includes a third part of the seal member on the fourth side,”

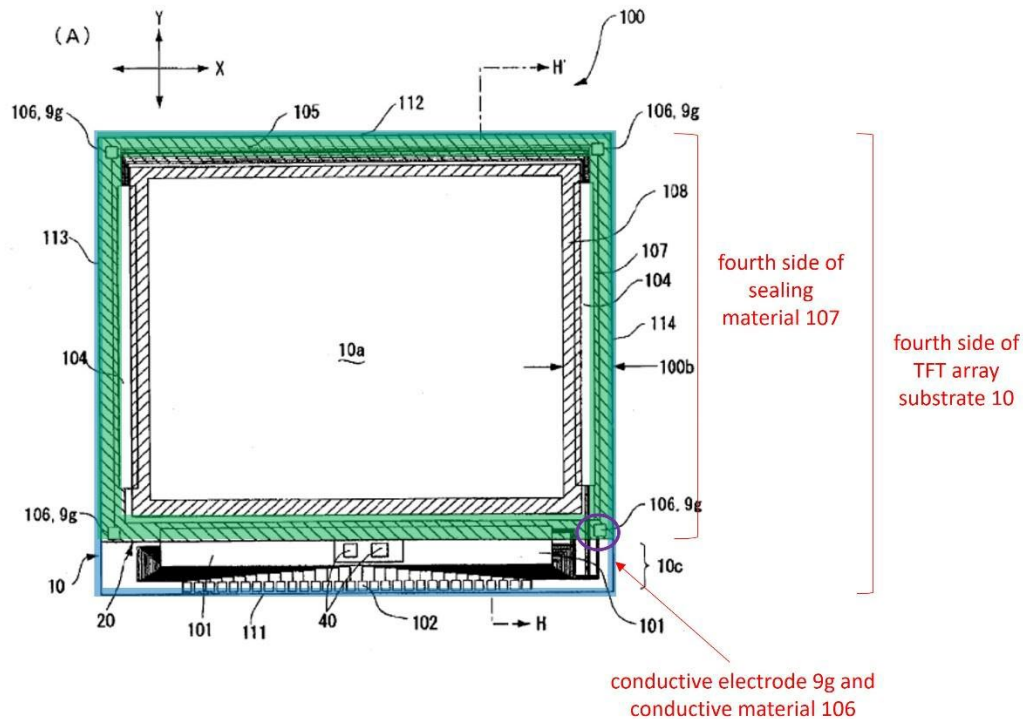
133. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

134. First, *Fujikawa* discloses a “fourth side” of the “first substrate”:



Fujikawa at Fig. 1A (annotated). *Fujikawa* also discloses a “third part of the seal member on the fourth side,” as shown above.

135. Second, as discussed, *Fujikawa* discloses or at least renders obvious a second conductive point on the fourth side. Sections X.A.11-X.A.12. *Fujikawa* discloses conductive electrode 9g at the bottom right corner of TFT array substrate 10 in Figure 1A:



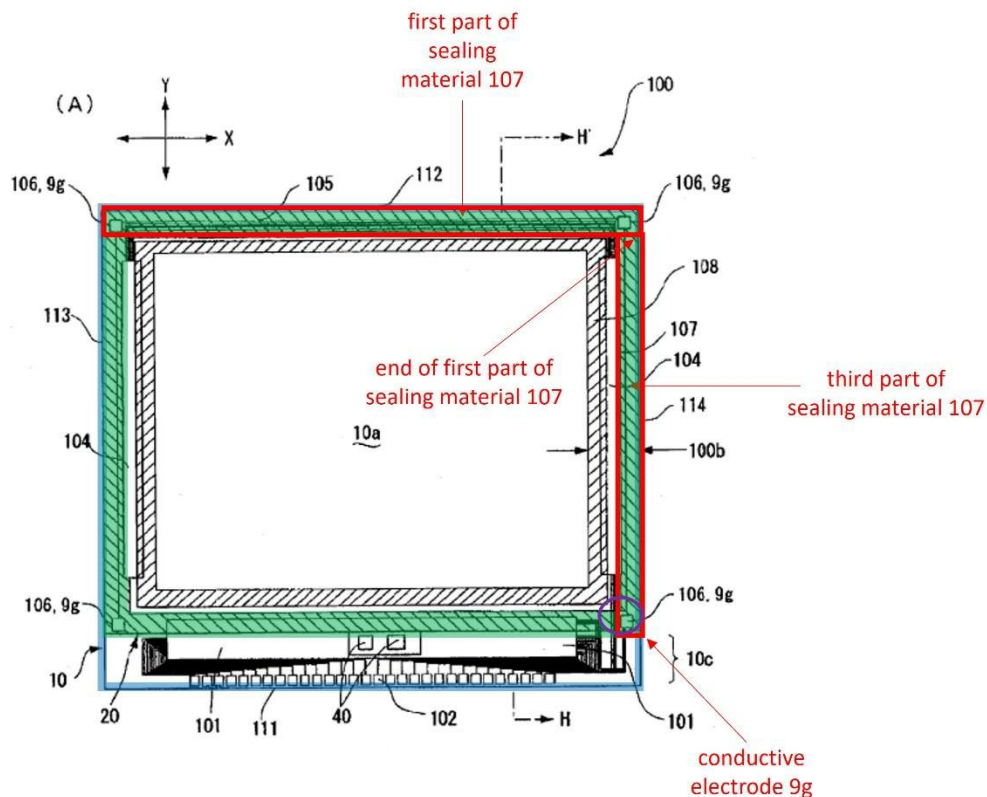
Fujikawa at Fig. 1A (annotated). The conductive electrode 9g in the bottom right corner is the “*second conductive point*” on the fourth side of the first substrate. It would have also been obvious to include a plurality of conductive points along the fourth side of the first substrate since *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed,” the conductive electrodes

9g disclosing the claimed conductive points. *Fujikawa*, [0047]; Sections X.A.10-X.A.12.

3. 9[b]: “*the third part of the seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side, and the third part of the seal member includes a plurality of conductive particles, and*”

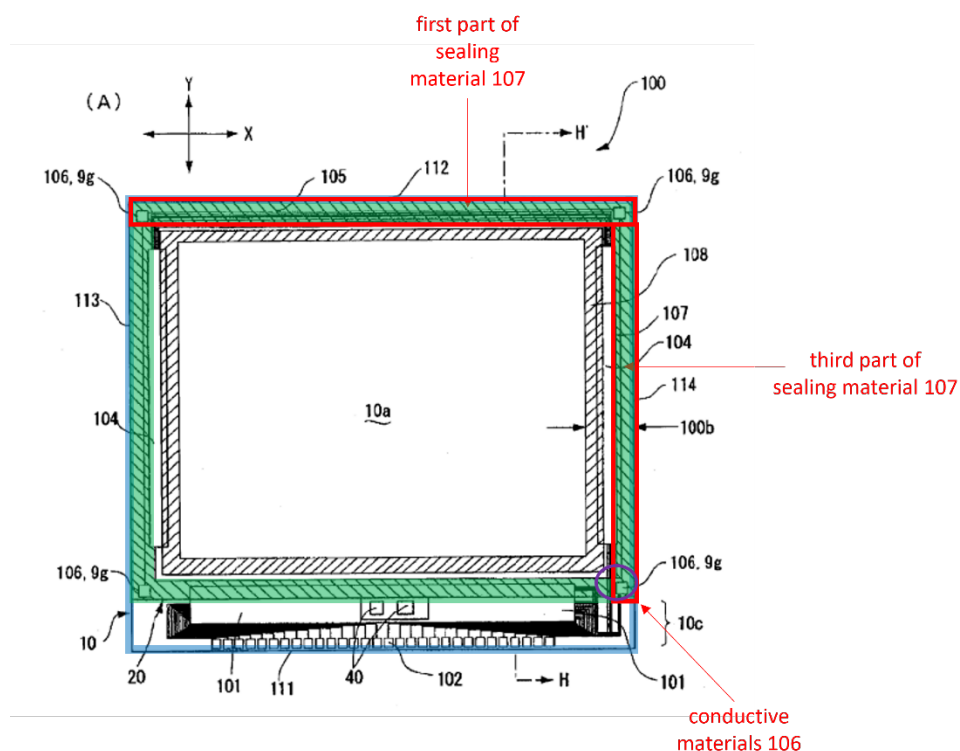
136. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

137. First, as discussed for limitation 9[a], *Fujikawa* discloses a “*third part*” of the “*seal member*” (sealing material 107). Section X.C.2. And as discussed above for limitation 7[i], *Fujikawa* discloses a “*first part*” of the “*seal member*” (sealing material 107). Section X.A.10. As shown below in *Fujikawa*, the “*third part*” of the “*seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side,*” as claimed:



Fujikawa at Fig. 1A (annotated).

138. Second, as discussed above, *Fujikawa* also discloses or at least renders obvious a plurality of conductive particles in the third part of the sealing material. Section X.A.10. For example, *Fujikawa* Figure 1A discloses conductive electrode 9g and conductive material 106 at the bottom right corner of TFT array substrate 10:



Fujikawa at Fig. 1A (annotated). The conductive particles in conductive material 106 of sealing material 107 in the bottom right corner are the claimed “**plurality of conductive particles**.” It would have also been obvious to include a plurality of conductive particles in the third part of the seal member because *Fujikawa* discloses that the “number of conductive electrodes 9g, and the like may be appropriately changed,” and the POSITA would have understood that “the like” refers at least to conductive materials 106. *Fujikawa* at [0047]; Section X.A.10.

4. 9[c]: “**wherein the second conductive point is electrically connected to the common electrode.**”

139. In my opinion, *Fujikawa* discloses or at least renders obvious this claim limitation.

140. As discussed for limitation 7[j], *Fujikawa* discloses each conductive electrode 9g (including the “*second conductive point*”) is “electrically connected to the counter electrodes 21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates.” *Fujikawa*, [0079]; Section X.A.11. This is shown below in Figure 9:

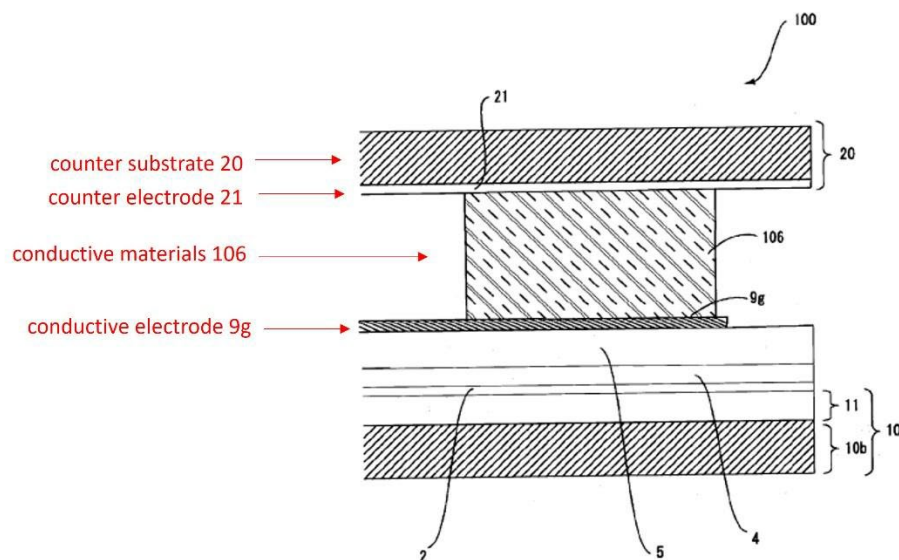


FIG.9

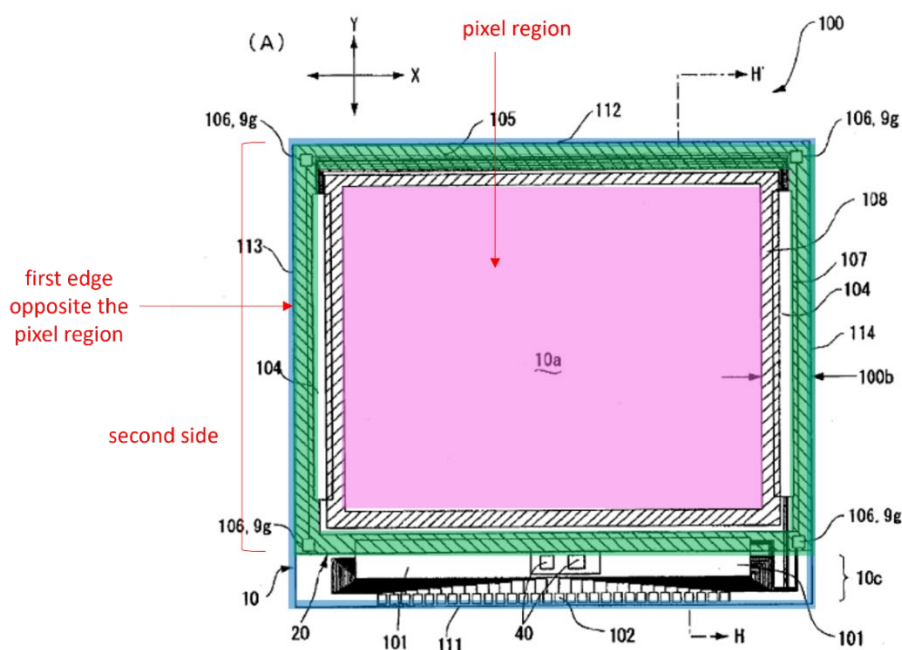
Fujikawa at Fig. 9 (annotated).

D. Dependent Claim 10

1. “*The display device, according to claim 7, wherein the seal member extends to a first edge of the seal region opposite to the pixel region on the second side.*”

141. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 7, in my opinion. Section X.A.

142. Moreover, in my opinion, *Fujikawa* discloses this additional limitation of claim 10. As shown in Figure 1A below, the sealing material 107 fills the entire “area shaded by downward-slanting lines” in the plan view of Figure 1A:



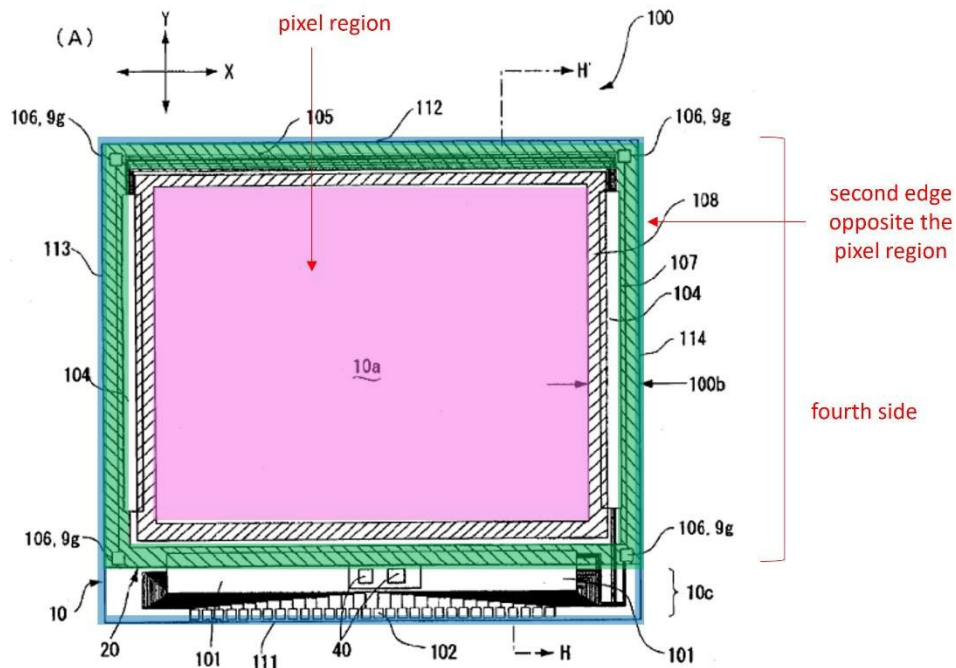
Fujikawa at Fig. 1A (annotated). The sealing material thus “*extends to a first edge of the seal region opposite to the pixel region on the second side.*” *Fujikawa* at [0046], [0049].

E. Dependent Claim 11

1. “*The display device according to claim 10, wherein the seal member extends to a second edge of the seal region opposite to the pixel region on the fourth side.*”

143. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 10, in my opinion. Section X.D.

144. Moreover, in my opinion, *Fujikawa* discloses this additional limitation of claim 11. As shown in Figure 1A below, the sealing material 107 fills the entire “area shaded by downward-slanting lines” in the plan view of Figure 1A:



Fujikawa at Fig. 1A (annotated). The sealing material “*extends to a second edge of the seal region opposite to the pixel region on the fourth side.*” *Fujikawa*, [0046], [0049].

F. Dependent Claim 12

1. “An electronic device comprising the display device according to claim 7.”

145. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 7, in my opinion. Section X.A.

146. Moreover, *Fujikawa* discloses the additional limitation recited in claim 12, in my opinion. *Fujikawa* discloses its liquid crystal device (the claimed “**display device**”) can be used in electronic devices, like portable computers and telephones (“**electronic device**”). *Fujikawa* at [0002], [0004], [0010]-[0023]; *see also Fujikawa* at [0023] (“An electrooptic device of the present invention can be used to form a display section in an electronic device such as a portable computer or a portable telephone.”). Such an electronic device is shown below in Figures 17A and 17B:

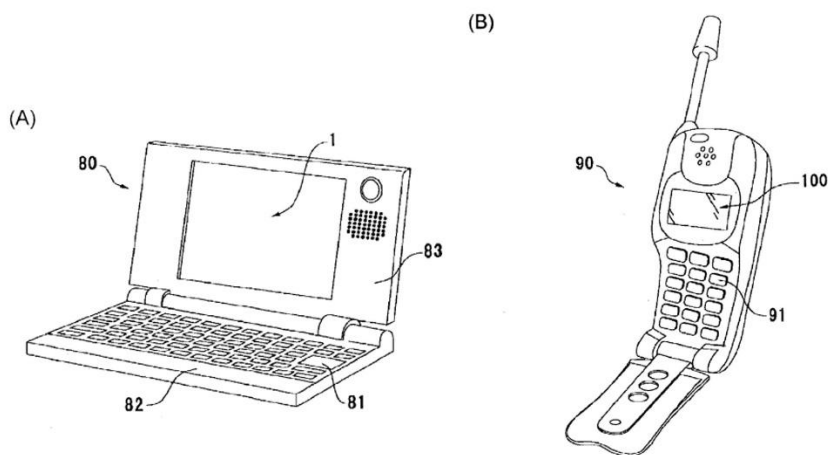


FIG.17

Fujikawa at Figs. 17A-17B (combined), [0041], [0106]-[0107].

G. Independent Claim 13

1. 13 ``` : “A display device, comprising:” ```

147. This preamble is substantially similar to the preamble in claim 7. *See* Section X.A.1. If the preamble is limiting, it is my opinion that *Fujikawa* discloses it for the same reasons discussed above. Section X.A.1.

2. **13[a]: “a first substrate including a plurality of pixel electrodes, a plurality of active elements and a plurality of wiring elements that connect to the plurality of active elements, wherein the plurality of active elements are thin film transistors disposed on the first substrate;”**

148. In my opinion, *Fujikawa* discloses this limitation.

149. As discussed for limitation 7[a], *Fujikawa* discloses a “**first substrate**” in TFT array substrate 10. Section X.A.2; *Fujikawa* at [0046], Figs. 1A-1B.

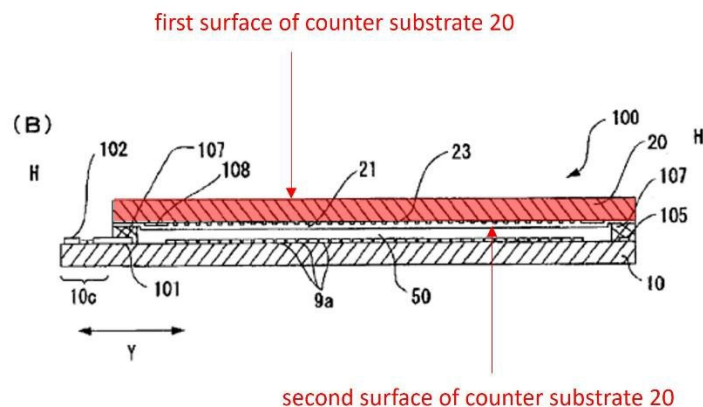
150. As discussed for limitation 7[a] and 7[b], *Fujikawa* discloses a pixel region comprising a plurality of pixels disposed on TFT array substrate 10. Sections X.A.2-X.A.3; *Fujikawa*, [0053], [0058], [0061]. As discussed above for limitation 7[b], *Fujikawa* further discloses that its plurality of pixels has “a pixel electrode 9a and a pixel-switching TFT 30.” Section X.A.3; *Fujikawa*, [0053], [0058], [0061]. *Fujikawa* thus discloses disposed on TFT array substrate 10 (“**first substrate**”) is “**a plurality of pixel electrodes**” and “**a plurality of active elements**” where “**the active elements are thin film transistors.**” See Sections X.A.2-X.A.3; *Fujikawa*, [0053], [0058], [0061].

151. As discussed for limitation 7[l], *Fujikawa* discloses a “**plurality of wiring elements**” on TFT array substrate 10 that “**connect to the plurality of active elements**” (TFT). Section X.A.13.

3. 13[b]: “a second substrate including a common electrode, wherein the common electrode is disposed on the second substrate;”

152. In my opinion, *Fujikawa* discloses this limitation.

153. As discussed above for limitation 7[c], *Fujikawa* discloses the “**second substrate**” in counter substrate 20. Section X.A.4; *Fujikawa*, [0046], [0049], Figs. 1A-1B. And as also discussed for limitation 7[c], *Fujikawa* discloses a “**common electrode . . . disposed on the second substrate**” in counter electrodes 21 disposed on the bottom of counter substrate 20. Section X.A.4; *Fujikawa*, [0050], [0058], [0079], Figs. 1B, 9. These are shown in Figures 1B and 9, below:



Fujikawa at Fig. 1B (annotated).

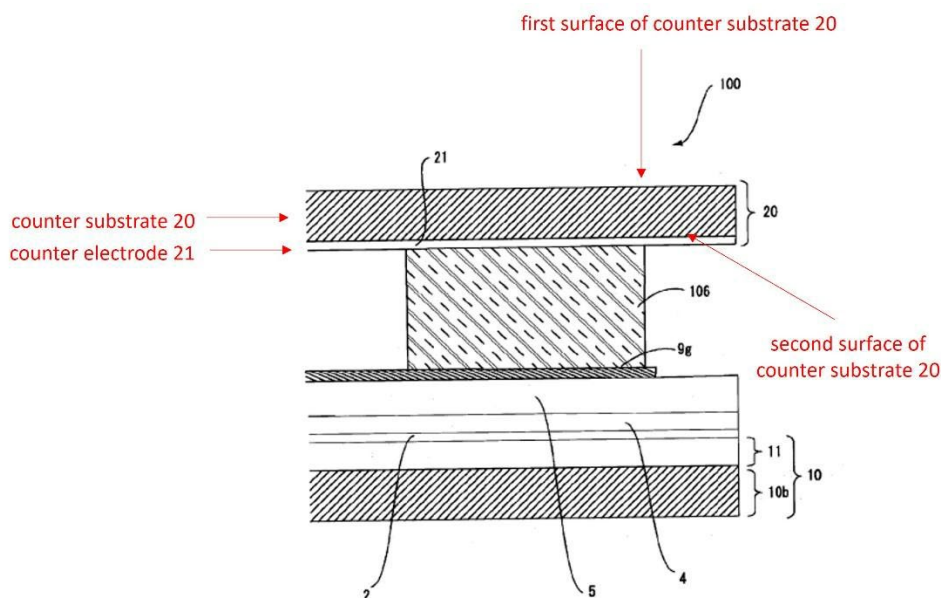


FIG.9

Fujikawa at Fig. 9 (annotated).

4. 13[c]: “*a display region in which the plurality of pixel electrodes and the plurality of active elements are aligned in a plan-view of the first substrate;*”

154. In my opinion, *Fujikawa* discloses this limitation.

155. As discussed for limitations 7[a] and 7[b], *Fujikawa* discloses a pixel region (image display region 10a) (“***display region***”) disposed on a first substrate. Sections X.A.2-X.A.3. This pixel/display region includes a plurality of pixels comprising a plurality of pixel electrodes and TFTs (“***active elements***”). *Fujikawa* at [0053]-[0054], [0058], [0061]; Sections X.A.2-X.A.3. The pixel electrodes and TFTs in the display region can be seen below in Figure 4:

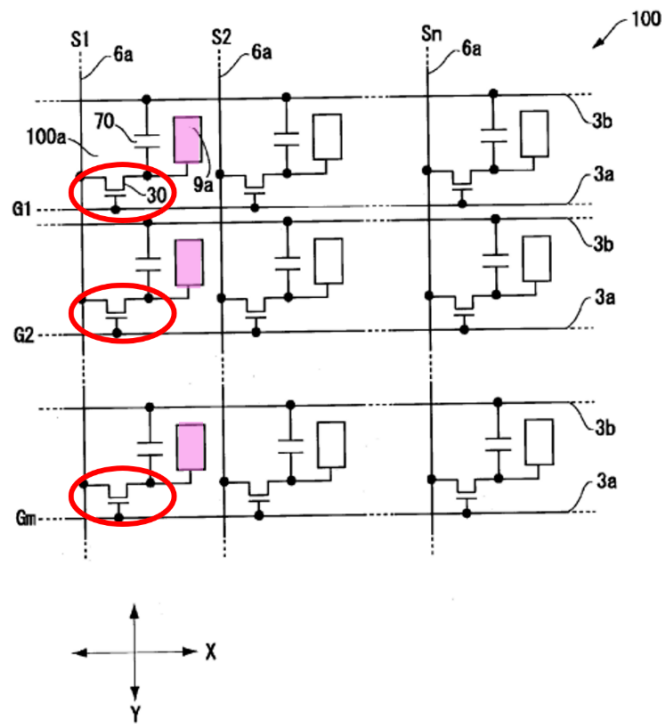


FIG.4

Fujikawa at Fig. 4 (exemplary pixel electrodes in pink, thin film transistors (TFTs) in red). And the pixel electrodes and TFTs in pixels 100a in the “*display region*” are “*aligned in a plan view of the first substrate,*” as shown in Figure 2:

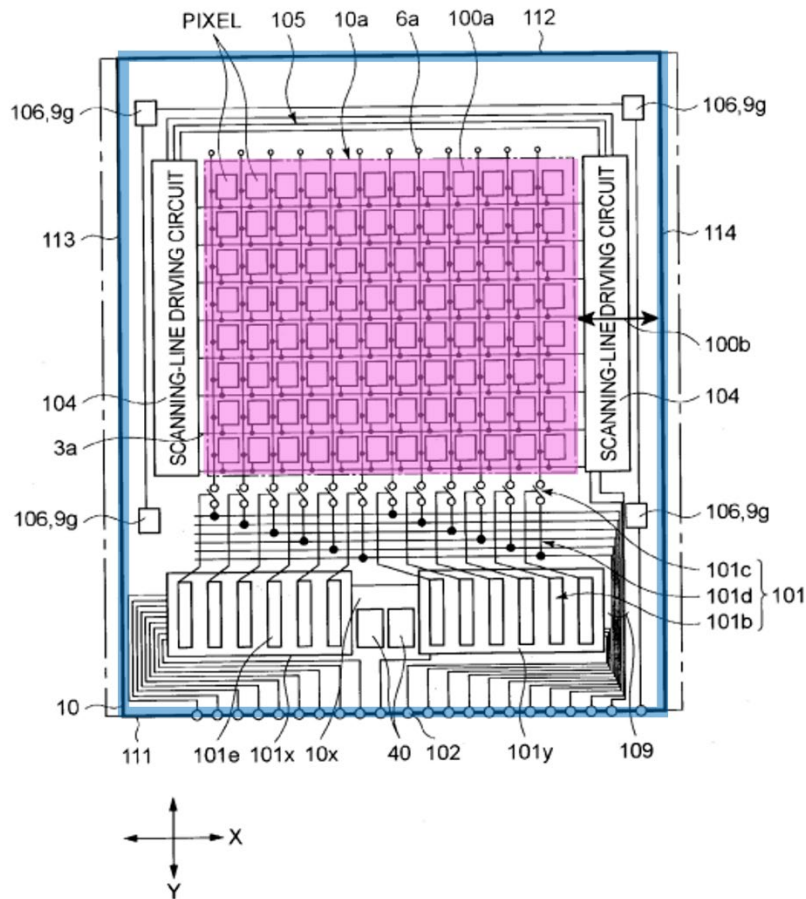


FIG.2

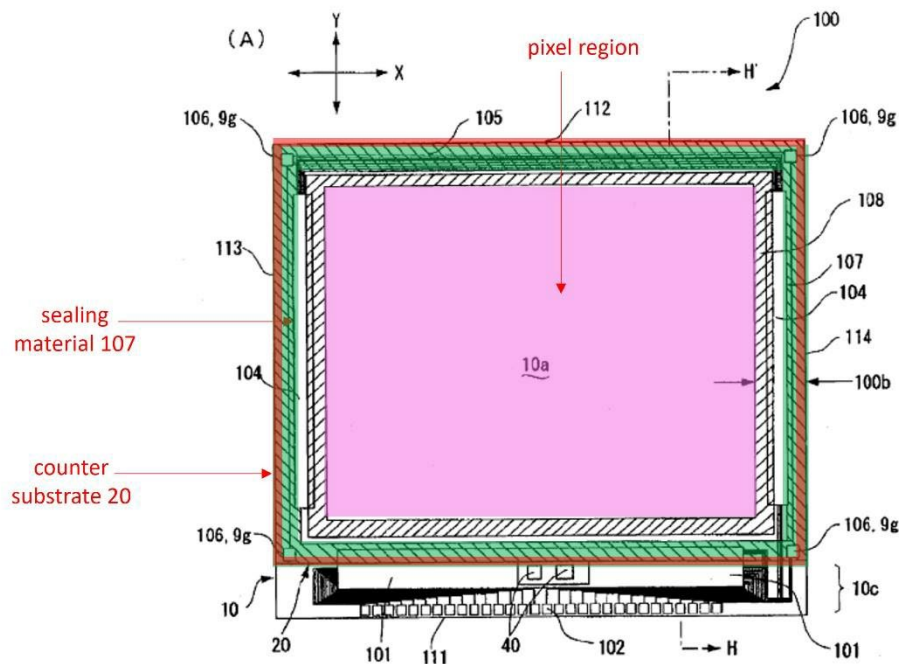
Fujikawa at Fig. 2 (annotated).

5. 13[d]: “a seal region positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed;”

156. In my opinion, *Fujikawa* discloses this limitation.

157. As discussed for limitation 7[a], *Fujikawa* discloses a “**seal region**” of sealing material 107 in the “area shaded by downward-slanting lines” in Figure 1A. Section X.A.2; *Fujikawa*, [0046], [0049], Figs. 1A-1B.

158. As discussed for limitation 7[h], *Fujikawa* discloses a “**seal region**” comprising sealing material 107 (“**seal member**”) “**positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed.**” Section X.A.9. This is shown, for example, in Figure 1A:



Fujikawa at Fig. 1A (annotated).

6. 13[e]: ***“a seal member being disposed in the seal region and bonding the first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes,”***

159. In my opinion, *Fujikawa* discloses this limitation.

160. As discussed for limitation 7[d], *Fujikawa* discloses sealing material 107 (“***a seal member***”) disposed in the “area shaded by downward-slanting lines” in Figure 1A (“***the seal region***”). Section X.A.5. And as explained for limitation 7[d], *Fujikawa* discloses sealing material 107 “***bond[s] the first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes.***” Section X.A.5; *Fujikawa*, [0046], [0049], Figs. 1A-1B.

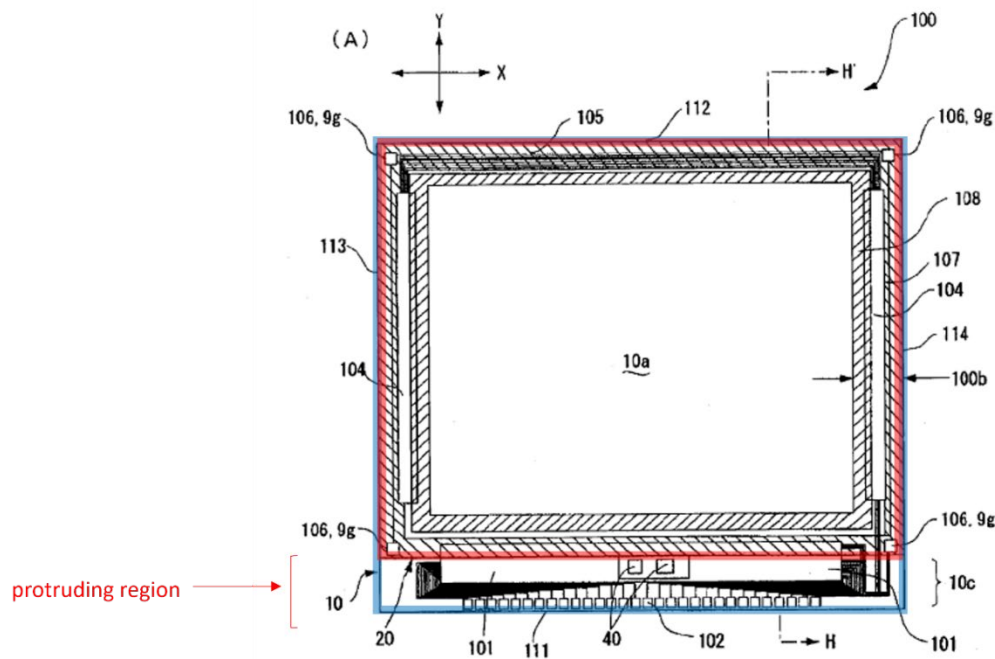
7. 13[f]: ***“the seal member forming a closed-ring shape in which the display region is positioned without protruding from the second substrate in the plan-view of the first substrate, the seal member is disposed between the first substrate and the second substrate, and the seal member is formed continuously around the entire display region without the use of a plug;”***

161. This limitation is substantially similar to limitation 7[h]. See Section X.A.9. For the reasons discussed above, *Fujikawa* discloses this limitation in my opinion. Section X.A.9; Section X.G.4 (discussing “***display region***” in limitation 13[c] is the same as “***pixel region***” discussed in limitation 7[a]).

8. 13[g]: ***“wherein the first substrate includes a protruding region which protrudes over the second substrate in the plan-view of the first substrate and a plurality of conductive portions,”***

162. In my opinion, *Fujikawa* discloses this limitation.

163. First, as discussed above in limitation 7[e], *Fujikawa* discloses the “**first substrate includes a protruding region which protrudes over the second substrate in the plan-view.**” Section X.A.6. This is shown in Figure 1A below:



Fujikawa at Fig. 1A (annotated).

164. Second, *Fujikawa* discloses “[m]ultiple terminals 102 made of a metal film . . . , such as an ITO film, are formed along the substrate edge 111 of the TFT array substrate.” *Fujikawa* at [0055]. A “constant voltage” and “driving signals are input thereto.” *Fujikawa* at [0055]. “A plurality of lines 109 made of, for example, a low-resistance metal film, . . . for driving a scanning-line driving circuit 104 and data-line driving circuits 101, are routed from these terminals 102.” *Fujikawa* at [0055]. These elements are shown below:

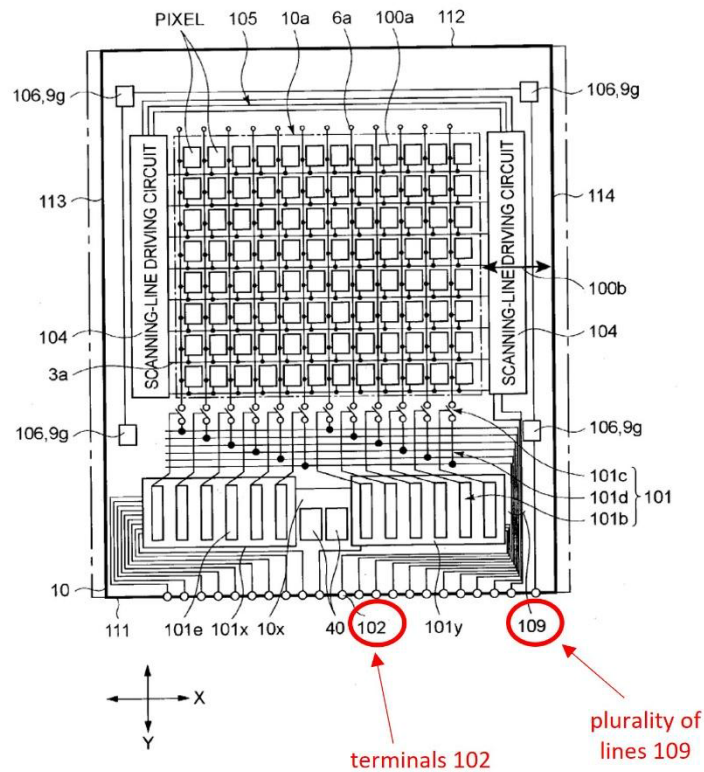


FIG.2

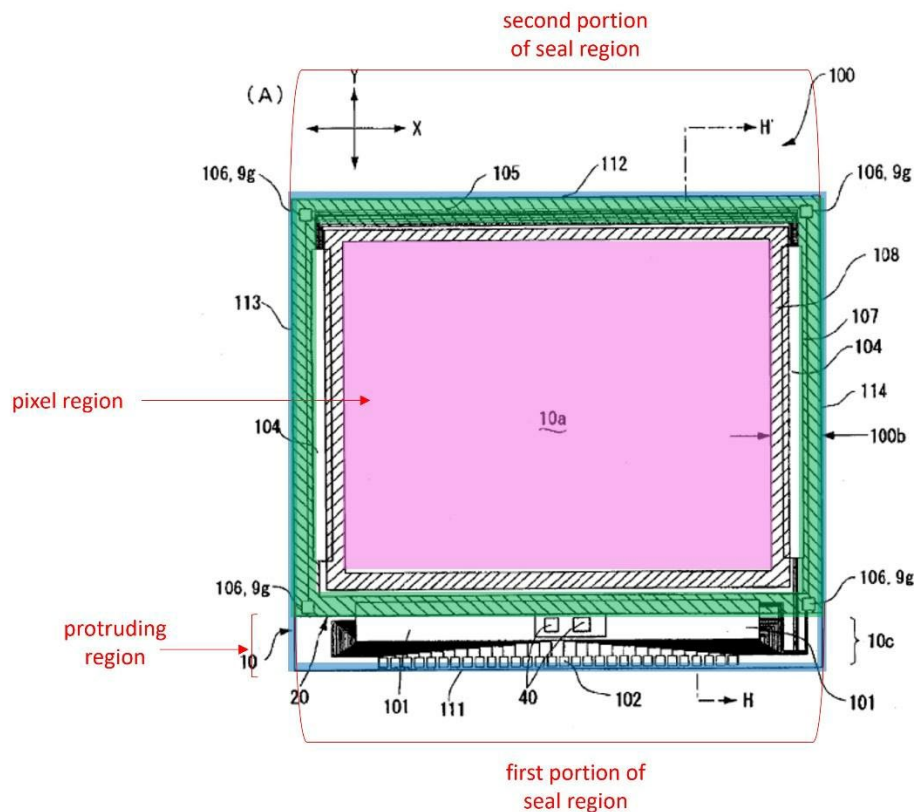
Fujikawa at Fig. 2. *Fujikawa* thus discloses “***first substrate includes . . . a plurality of conductive portions***” in “terminals 102.”

9. 13[h]: “***the seal region includes a first portion and a second portion, the first portion is positioned at least between the display region and the protruding region, and the second portion is positioned at least opposite to the protruding region with respect to the display region, and***”

165. In my opinion, *Fujikawa* discloses this limitation.

166. As discussed above for limitation 7[b], *Fujikawa* discloses a seal region that forms a rectangular ring shape around image display area 10a. Section X.A.3.

This seal region comprising sealing material 107 includes at least a “*first portion*” and a “*second portion.*” As shown below in *Fujikawa* Figure 1A, the “*first portion is positioned at least between the display region and the protruding region*” and the “*second portion is positioned at least opposite to the protruding region with respect to the display region,*” as claimed:

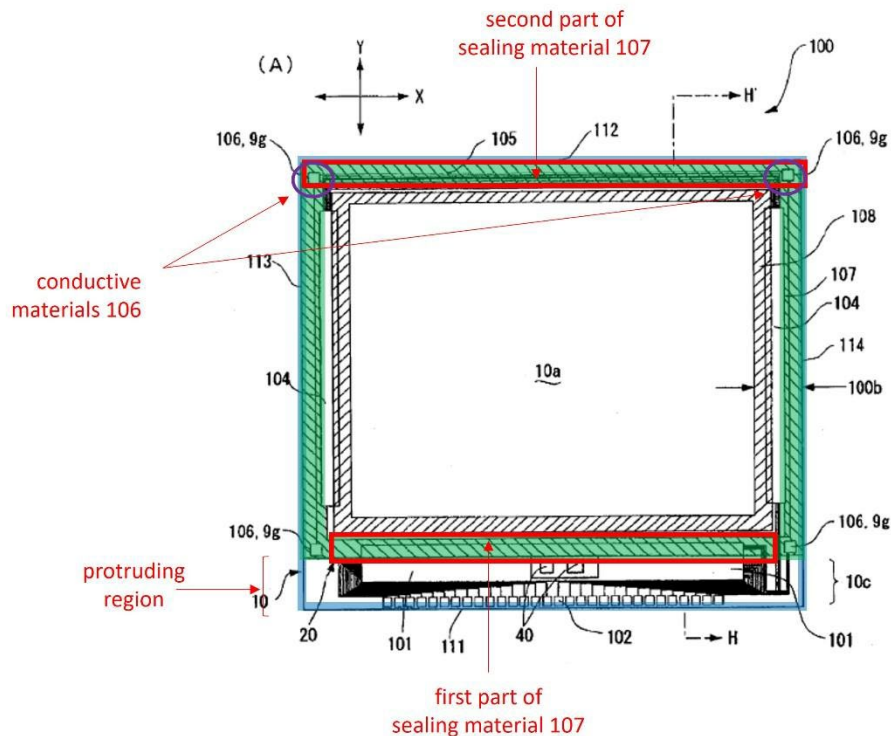


Fujikawa at Fig. 1A (annotated).

10. 13[i]: “the seal member includes a first part and a second part, the first part of the seal member is positioned on the first portion and the second part of the seal member is positioned

on the second portion, and the second part of the seal member includes a plurality of conductive particles”

167. This limitation is substantially similar to limitation 7[i]. See Section X.A.10. As shown in Figure 1A below, the sealing material includes “***a first part***” and “***a second part***”:



Fujikawa at Fig. 1A (annotated). And for the reasons discussed for limitation 7[i], *Fujikawa* discloses or renders obvious “***the second part of the seal member includes a plurality of conductive particles.***” Section X.A.10; *Fujikawa*, [0047].

11. 13[j]: “***a plurality of dot conductive points are disposed on the second portion of the first substrate, all of the plurality of dot***

conductive points are electrically connected to the common electrode,”

168. This limitation is substantially similar to limitation 7[j]. *See* Section X.A.11. As explained above, *Fujikawa* discloses or at least renders obvious this limitation in my opinion. Section X.A.11; *Fujikawa* at [0047].

12. 13[k]: “each of the plurality of the dot conductive points are spaced apart from each other, and”

169. This limitation is substantially similar to limitation 7[k]. *See* Section X.A.12. As explained above, *Fujikawa* discloses or at least renders obvious this limitation in my opinion. Section X.A.12; *Fujikawa* at [0047].

13. 13[l]: “the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points.”

170. This limitation is substantially similar to limitation 7[l]. *See* Section X.A.13. As explained, *Fujikawa* discloses this limitation in my opinion. Section X.A.13; *Fujikawa* at [0047].

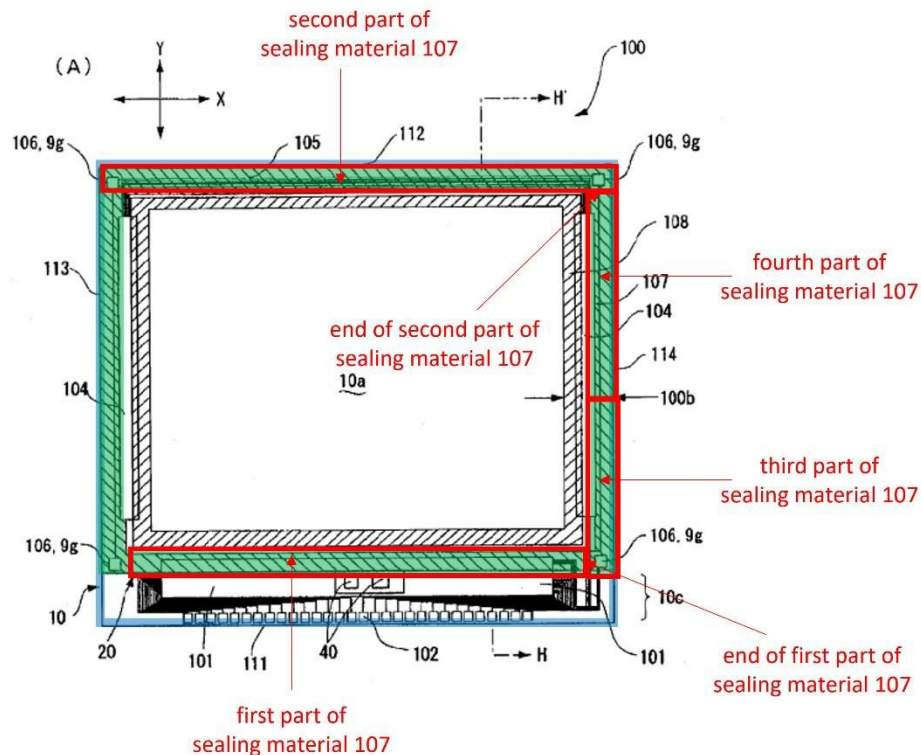
H. Dependent Claim 15

1. “The display device, according to claim 13, wherein the seal member further includes a third part and a fourth part, the third part of the seal member extends from one end of the first part, and the fourth part of the seal member extends from one end of the second part and includes a first plurality of conductive particles.”

171. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 13. Section X.G. Moreover, *Fujikawa* at least renders obvious

the additional limitation in claim 15 in my opinion.

172. First, as discussed for limitations 7[b] and 7[d], *Fujikawa* discloses a seal region that forms a rectangular ring shape around the image display area 10a that comprises sealing material 107 (“*seal member*”). See Sections X.A.3, X.A.5. Under Patent Owner’s apparent interpretation of this claim limitation in district court, *Fujikawa* discloses a “*third part of the seal member extends from one end of the first part*” and a “*fourth part of the seal member extends from one end of the second part,*” as claimed:



Fujikawa at Fig. 1A (annotated); Ex. 1019 at 3-4.⁵

173. Second, as discussed above for limitation 7[i], *Fujikawa* at least renders obvious “***a first plurality of conductive particles***” along the seal member, including in the “***fourth part of the seal member.***” Section X.A.10; *Fujikawa*, [0047].

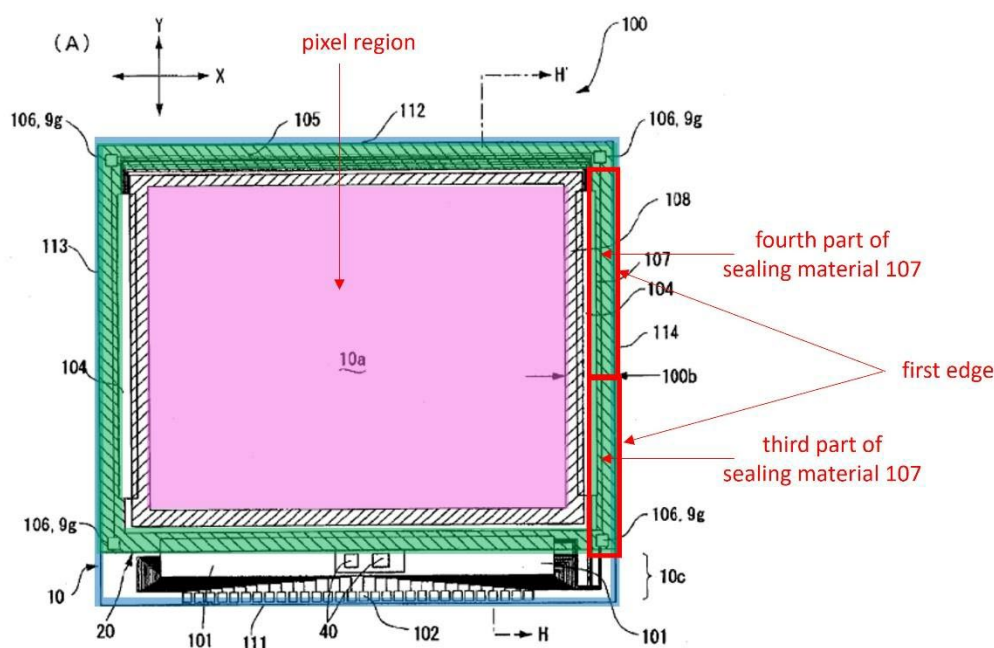
I. Dependent Claim 16

1. “***The display device, according to claim 15, wherein the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region.***”

174. As discussed above, *Fujikawa* discloses or renders obvious a display device according to claim 15. Section X.H. Moreover, *Fujikawa* also discloses or at least renders obvious this additional limitation in claim 16 in my opinion.

175. As discussed for claim 15, *Fujikawa* discloses at least a “***third part***” and “***fourth part***” of the seal member. Section X.H. Under Patent Owner’s apparent interpretation of this limitation in the district court litigation, and as shown in Figure 1A, *Fujikawa* discloses that “***the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region,***” as claimed:

⁵ Citations for the exhibit are to the page numbers stamped in the exhibit.



Fujikawa at Fig. 1A (annotated); Ex. 1019 at 4-5.

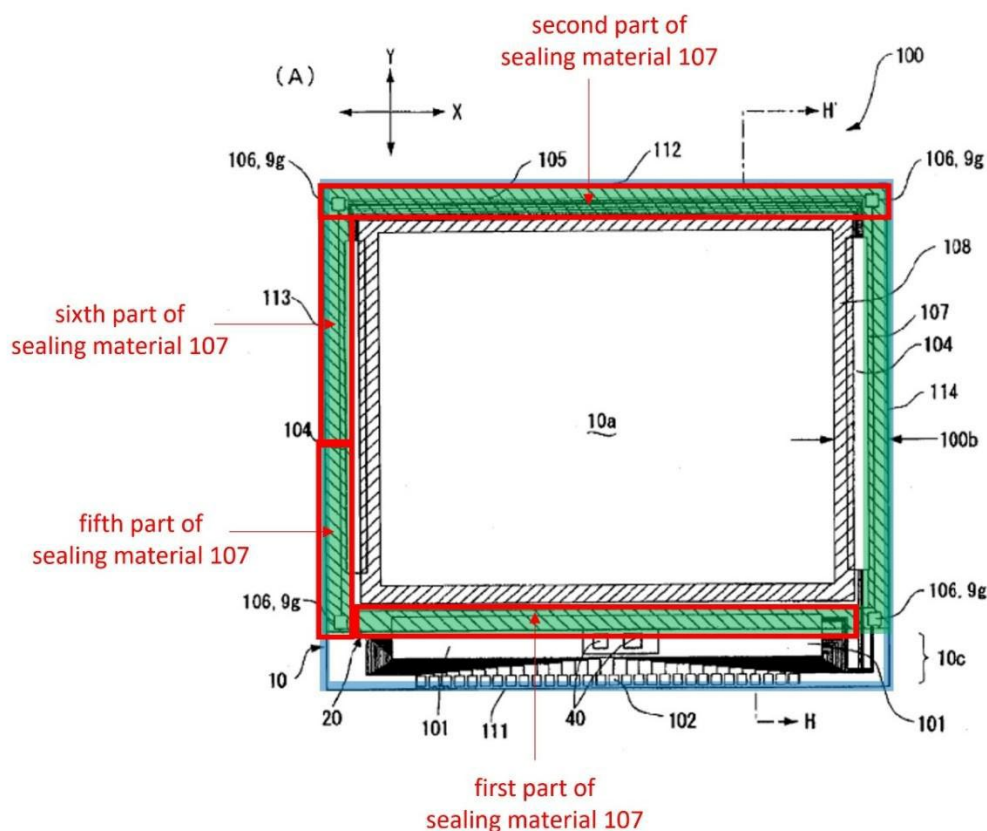
J. Dependent Claim 17

1. *“The display device, according to claim 16, wherein the seal member further includes a fifth part and a sixth part, the fifth part of the seal member extends from another end of the first part, and the sixth part of the seal member extends from another end of the second part and includes a second plurality of conductive particles, and the fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region.”*

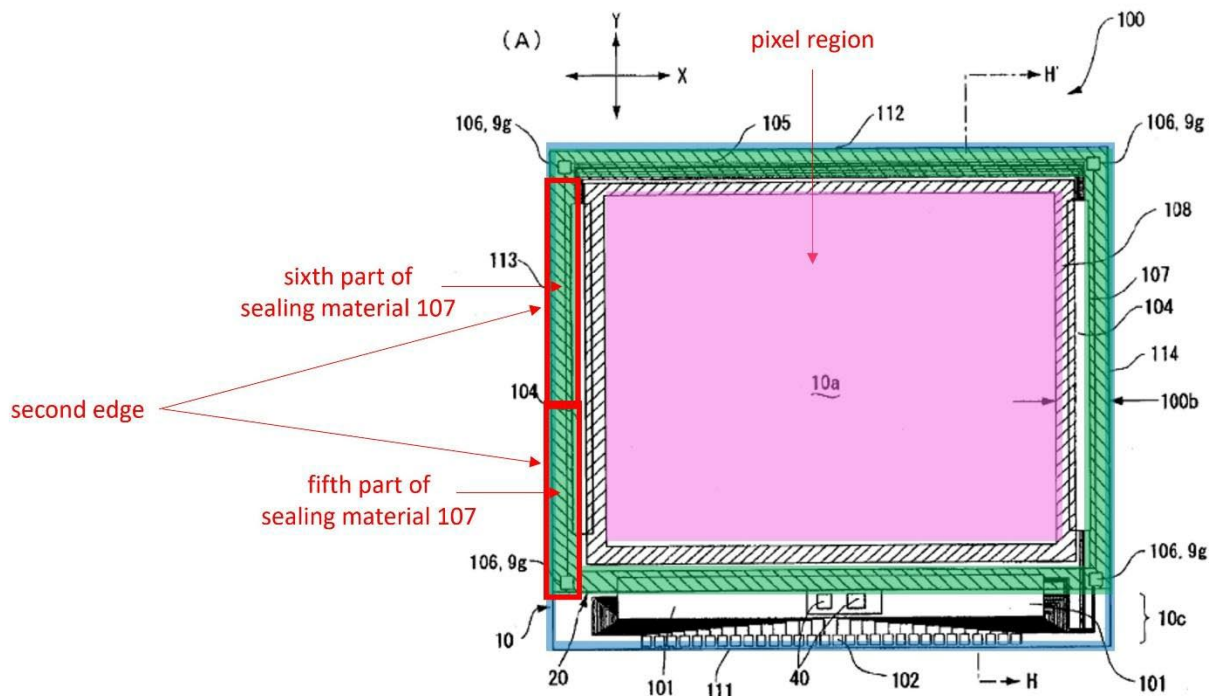
176. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 16. Section X.I. Moreover, *Fujikawa* at least renders obvious the additional limitation in claim 17 in my opinion.

177. First, as discussed for limitations 7[b] and 7[d], *Fujikawa* discloses a seal region that forms a rectangular ring shape around the image display area 10a

comprising sealing material 107 (“*seal member*”). Sections X.A.3, X.A.5. Under Patent Owner’s apparent interpretation of this claim limitation in the district court litigation, *Fujikawa* discloses sealing material 107 includes at least includes a “*fifth part*” that “*extends from another end of the first part*” and also a “*sixth part*” that “*extends from another end of the second part*”:



Fujikawa at Fig. 1A (annotated); Ex. 1019 at 5-7. Moreover, under Patent Owner’s apparent interpretation of this limitation in the district court litigation, and as shown below, the “***fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region,***” as claimed:



Fujikawa at Fig. 1A; Ex. 1019 at 5-7.

178. Second, as discussed above for limitation 7[i], *Fujikawa* at least renders obvious “*second plurality of conductive particles*” along the seal member, including in the “*sixth part of the seal member.*” Section X.A.10; *Fujikawa* at [0047].

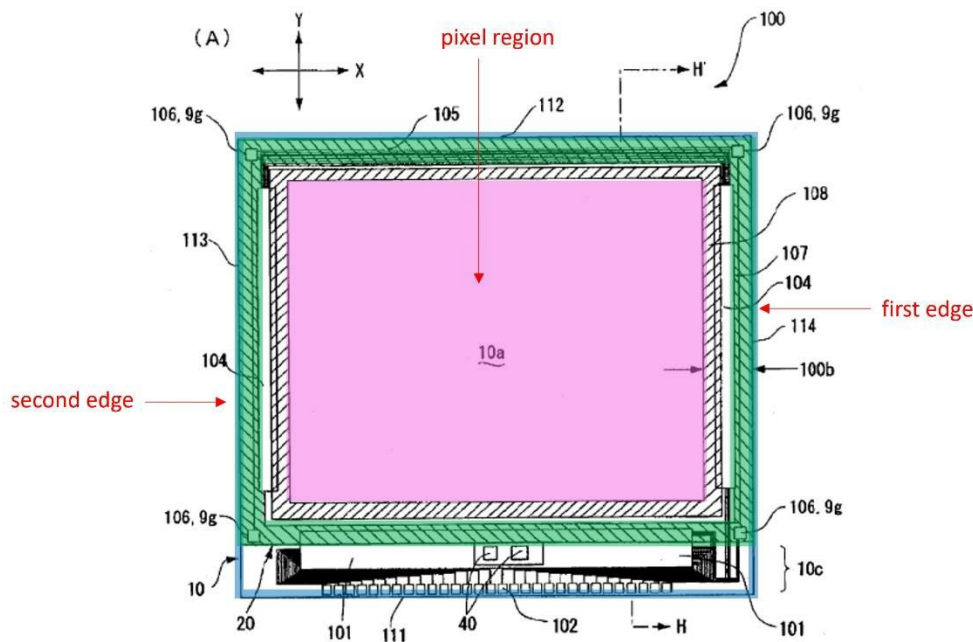
K. Dependent Claim 18

1. “*The display device, according to claim 17, wherein the first edge of the seal region is positioned opposite to the second edge of the seal region with respect to the display region.*”

179. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 17. Section X.J. Moreover, *Fujikawa* discloses this additional limitation in claim 18 in my opinion.

180. As discussed for claims 16 and 17, *Fujikawa* discloses a “*first edge of*

the seal region” and “second edge of the seal region.” Sections X.I-X.J. As shown in Figure 1A, these edges are “positioned opposite” each other “with respect to the display region”:



Fujikawa at Fig. 1A (annotated).

L. Dependent Claim 19

1. 19[pre]: “*The display device, according to claim 18,*”

181. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 18. Section X.K.

2. 19[a]: “*wherein the first substrate further includes a first conductive point and a second conductive point, different from the plurality of conductive points, and the first conductive point, the second conductive point and the*”

plurality of conductive points are disposed apart from each other, and”

182. This limitation is substantially similar to claim limitations 7[j], 7[k], 13[j], and 13[k], and claims 8 and 9. Sections X.A.11-X.A.12, X.G.11-X.G.12, X.B, X.C. For the reasons discussed above, *Fujikawa* discloses or at least renders obvious this limitation. Sections X.A.11-X.A.12, X.G.11-X.G.12, X.B, X.C.

3. **19[b]: “*the first conductive point is electrically connected to the common electrode through the first plurality of conductive particles and the second conductive point is electrically connected to the common electrode through the second plurality of conductive particles.*”**

183. This limitation is substantially similar to limitations 7[i], 7[j], 7[k], 13[i], 13[j], and 13[k], and claims 8, 9, 15, and 17. *See* Sections X.A.10-X.A.12, X.G.10-X.G.12, X.B, X.C, X.H, X.J. For the reasons above, *Fujikawa* discloses or at least renders obvious this limitation. *See* Sections X.A.10-X.A.12, X.G.10-X.G.12, X.B, X.C, X.H, X.J.

M. Dependent Claim 20

1. **“*An electronic device comprising the display device according to claim 13.*”**

184. As discussed, *Fujikawa* discloses or renders obvious a display device according to claim 13. Section X.G. Moreover, in my opinion, *Fujikawa* discloses the additional limitation in claim 20, for the reasons discussed above with respect to claim 12. Section X.F.

XI. FUJIKAWA AND KANG RENDER OBVIOUS CLAIMS 7-13 AND 15-20
(GROUND 3)

A. Independent Claim 7

1. 7[pre]-7[g]

Element	Claim Language
7[pre]	<i>A display device, comprising</i>
7[a]	<i>a first substrate including a pixel region and a seal region which is defined around the pixel region on a first surface of the first substrate</i>
7[b]	<i>the pixel region including a plurality of pixels and a plurality of active elements, and the seal region forming a rectangular ring shape, wherein the active elements are thin film transistors disposed on the first substrate; and</i>
7[c]	<i>a second substrate including a common electrode on a second surface; and</i>
7[d]	<i>a seal member bonding the first substrate and the second substrate so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels</i>
7[e]	<i>wherein the first substrate includes a protruding region which</i>

Element	Claim Language
	<i>protrudes over the second substrate in a plan-view of the first substrate</i>
7[f]	<i>the seal region includes a first side, a second side, a third side and a fourth side, the first side is positioned between the pixel region and the protruding region, and opposed to the third side, and the second side is opposed to the fourth side</i>
7[g]	<i>the seal member is disposed between the first substrate and the second substrate</i>

185. As discussed above, it is my opinion that *Fujikawa* discloses each of these limitations. See Sections X.A.1-X.A.8.

2. 7[h]

Element	Claim Language
7[h]	<i>and positioned on the first side, the second side, the third side and the fourth side continuously, forms a closed-ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate, and is formed continuously around the entire pixel region without the use of a</i>

Element	Claim Language
	<i>plug</i>

186. As discussed above, *Fujikawa* discloses this limitation. Section X.A.9. Alternatively, to the extent *Fujikawa* does not expressly disclose this feature, it is my opinion that it would have been obvious to a POSITA in view of *Kang*.

187. *Kang* discloses a dropping method that provides a marked improvement over previous vacuum injection methods for creating a liquid crystal display. Section VI.B; *Kang* at [0068]-[0072]; '606 patent at 1:23-61 (acknowledging drop method was a well-known improvement over vacuum method). According to *Kang*, vacuum methods that use a hole to inject liquid crystal from the outside and then seal that hole with a plug were costly and slow. *Kang* at [0066]-[0067]. To avoid this problem, *Kang* discloses a “dropping” method where a “seal pattern” is “formed to have a closed shape that encompasses the outer edge of the image display part” on a first substrate. *Kang* at [0070]. Liquid crystal is then dropped onto the “display part”—rather than “filled from the outside” using a plug. *Kang* at [0069], [0070]. According to *Kang*, the “seal pattern” used in this method necessarily has a “closed shape . . . to prevent the leakage of the liquid crystal.” *Kang* at [0070], [0062] (explaining seal pattern 506 “may be formed of various planar shapes”).

188. A POSITA would have been motivated to combine *Fujikawa* and *Kang* to achieve such an improved liquid crystal display device. As an initial matter, *Fujikawa* and *Kang* are analogous art to the '606 patent. They are both in the same field of endeavor as each other and as the '606 patent. The '606 patent relates to a method of manufacturing a liquid crystal device (and resulting liquid crystal device). Section VII.A; '606 patent at 1:19-21. It discloses a dropping method of forming a liquid display device to avoid the cost and time associated with vacuum methods, as the '606 patent admits was well-known. *E.g.*, '606 patent at 1:23-3:58, 3:62-10:41, 18:36-19:27, 22:36-31:17. The resulting liquid display device has a seal member with a closed-ring shape that is formed around the pixel display area continuously without the use of a plug. *See, e.g.*, '606 patent at claims 7, 13. So too does *Kang* disclose using a closed-shape seal during “dropping” to create a liquid crystal device without the use of a plug. *Kang* at [0068]-[0072]. *Kang* explains that the seal pattern “may be formed of various planar shapes.” *Kang* at [0062]. And *Fujikawa* discloses a liquid crystal device with a rectangular ring shape seal member that surrounds a display area and “h[o]ld[s]” liquid crystal. *Fujikawa*, [0046], [0049].

189. A POSITA would have been motivated to use a dropping method and position *Fujikawa*'s sealing material 107 “*continuously*” in a “*closed-ring shape*” along the four sides of the seal region “*around the entire pixel region without the use of a plug.*” As described in the background section, the technique of depositing

liquid crystal material via drop fill was well known at the time, and a POSITA would have known this technique could be used, offering well-known benefits over existing vacuum injection methods, and would not require the use of a plug in *Fujikawa*. A POSITA would have been aware of the advantages of using a drop fill method which include reduced liquid crystal fill time. Ex. 1014 at 1353. Indeed, a POSITA would have understood using *Kang*'s dropping assembly would reduce time of manufacture and limit liquid crystal waste. *See, e.g., Kang* at [0065]-[0072]. A POSITA would have looked to a reference like *Kang* to improve the manufacture and design of the liquid crystal device in *Fujikawa* and ensure no liquid crystal leaks out of the display area. *E.g., Kang* at [0070].

190. A POSITA would have had a reasonable expectation of success using such a method with *Fujikawa*'s liquid crystal device. Using *Kang*'s dropping method and forming a seal pattern with a closed ring shape would be applying a known manufacturing method to improve a similar device in the same way to achieve the entirely predictable result of a liquid crystal display device with no "leakage of the liquid crystal." *Kang* at [0070]; '606 patent at 1:46-61 (admitting drop methods were known in the art to be alternative to vacuum injection methods, successfully forming seal without an injection hole in the background of the art section). It would require no more than ordinary skill to provide the rectangular seal region in *Fujikawa* using *Kang*'s drop method to create a closed-ring structure as contemplated by the claims,

for *Kang* discloses that seal patterns can “be formed of various planar shapes” using its methods. *Kang* at [0062].

191. The drop filling method has indeed been used to dramatically reduce the time required to produce and manufacture LCDs. For instance, as discussed in Section V.B, the drop filling method has been shown to decrease the time required to fill the LCD with liquid crystalline material from approximately one day to a few minutes. The ability to directly place liquid crystalline material where it is desired, rather than waiting for a vacuum within the cavity to draw liquid crystalline material in allows for the direct control of display fabrication and straightforward production. There would be a reasonable expectation of success in implementing this technique, as the method for creating the seal itself would likely use a similar drop or printing technique to dispense the material. The drop filling technique additionally removes the need for the plug that the vacuum fill technique requires, thus removing a step in the production process.

3. 7[i]-7[k]

Element	Claim Language
7[i]	<i>a first part of the seal member disposed on the third side which is opposed to the protruding region with respect to the pixel region includes a plurality of conductive particles</i>

Element	Claim Language
7[j]	<i>a plurality of dot conductive points are disposed on the third side of the first substrate, all of the plurality of the dot conductive points are electrically connected to the common electrode, and</i>
7[k]	<i>each of the plurality of the dot conductive points are spaced part from each other</i>

192. As discussed, *Fujikawa* discloses or renders obvious these limitations. See Sections X.A.10-X.A.12.

4. 7[l]

Element	Claim Language
7[l]	<i>wherein the first substrate includes a plurality of wiring lines that connect to the plurality of active elements, and the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points</i>

193. As discussed, *Fujikawa* discloses this limitation. See Sections X.A.13.

B. Dependent Claims 8-9

Element	Claim Language
8[pre]	<i>The display device, according to claim 7</i>

Element	Claim Language
8[a]	<i>wherein the first substrate includes a first conductive point on the second side and the seal member includes a second part of the seal member on the second side</i>
8[b]	<i>the second part of the seal member extends from one end of the first part of the seal member over the first conductive point on the second side, and the second part of the seal member includes a plurality of conductive particles, and</i>
8[c]	<i>wherein the first conductive point is electrically connected to the common electrode</i>
9[pre]	<i>The display device, according to claim 8</i>
9[a]	<i>wherein the first substrate includes a second conductive point on the fourth side and the seal member includes a third part of the seal member on the fourth side</i>
9[b]	<i>the third part of the seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side, and the third part of the seal member includes a plurality of conductive particles, and</i>

Element	Claim Language
9[c]	<i>wherein the second conductive point is electrically connected to the common electrode</i>

194. As discussed, *Fujikawa* discloses or renders obvious the additional limitations in these claims. See Sections X.B-X.C.

C. Dependent Claims 10-12

Element	Claim Language
10	<i>The display device, according to claim 7, wherein the seal member extends to a first edge of the seal region opposite to the pixel region on the second side</i>
11	<i>The display device according to claim 10, wherein the seal member extends to a second edge of the seal region opposite to the pixel region on the fourth side</i>
12	<i>An electronic device comprising the display device according to claim 7</i>

195. As discussed, *Fujikawa* discloses the additional limitations in these claims. See Sections X.D-X.F.

D. Independent Claim 13

1. 13[pre]-13[c]

Element	Claim Language
13[pre]	<i>A display device, comprising</i>
13[a]	<i>a first substrate including a plurality of pixel electrodes, a plurality of active elements and a plurality of wiring elements that connect to the plurality of active elements, wherein the plurality of active elements are thin film transistors disposed on the first substrate</i>
13[b]	<i>a second substrate including a common electrode, wherein the common electrode is disposed on the second substrate</i>
13[c]	<i>a display region in which the plurality of pixel electrodes and the plurality of active elements are aligned in a plan-view of the first substrate</i>

196. As discussed above, *Fujikawa* discloses these limitations. See Sections X.G.1-X.G.4.

2. 13[d]

Element	Claim Language
13[d]	<i>a seal region positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed</i>

197. As discussed above for limitation 7[h], it is my opinion that *Fujikawa* and *Kang* render obvious a “*seal region*” comprising sealing material 107 (“*seal member*”) that is “*positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed.*”

Section XI.A.2.

3. 13[e]

Element	Claim Language
13[e]	<i>a seal member being disposed in the seal region and bonding the first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes</i>

198. As discussed, *Fujikawa* discloses this limitation. Section X.G.6.

4. 13[f]

199. As discussed above for limitation 7[h], it is my opinion that *Fujikawa* and *Kang* render obvious this limitation. Section XI.A.2.

Element	Claim Language
13[f]	<i>the seal member forming a closed-ring shape in which the display region is positioned without protruding from the second substrate in the plan-view of the first substrate, the seal member is disposed between the first substrate and the second substrate, and the seal member is formed continuously around the entire display region without the use of a plug</i>

5. 13[g]-13[h]

Element	Claim Language
13[g]	<i>wherein the first substrate includes a protruding region which protrudes over the second substrate in the plan-view of the first substrate and a plurality of conductive portions</i>
13[h]	<i>the seal region includes a first portion and a second portion, the first portion is positioned at least between the display region and the protruding region, and the second portion is positioned at least opposite to the protruding region with respect to the display region, and</i>

200. As discussed, *Fujikawa* discloses this limitation. See Sections X.G.8-X.G.9.

6. 13[i]-13[k]

Element	Claim Language
13[i]	<i>the seal member includes a first part and a second part, the first part of the seal member is positioned on the first portion and the second part of the seal member is positioned on the second portion, and the second part of the seal member includes a plurality of conductive particles</i>
13[j]	<i>a plurality of dot conductive points are disposed on the second portion of the first substrate, all of the plurality of dot conductive points are electrically connected to the common electrode</i>
13[k]	<i>each of the plurality of the dot conductive points are spaced apart from each other, and</i>

201. As discussed, *Fujikawa* discloses or renders obvious these limitations.
See Sections X.G.10-X.G.12.

7. 13[l]

Element	Claim Language
13[l]	<i>the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive</i>

Element	Claim Language
	<i>points</i>

202. As discussed, *Fujikawa* discloses this limitation. See Section X.G.13.

E. Dependent Claim 15

Element	Claim Language
15	<i>The display device, according to claim 13, wherein the seal member further includes a third part and a fourth part, the third part of the seal member extends from one end of the first part, and the fourth part of the seal member extends from one end of the second part and includes a first plurality of conductive particles</i>

203. As discussed, *Fujikawa* at least renders obvious the additional limitation in claim 15. See Section X.H.

F. Dependent Claim 16

Element	Claim Language
16	<i>The display device, according to claim 15, wherein the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region</i>

204. As discussed, *Fujikawa* discloses or at least renders obvious the

additional limitation in claim 16. *See* Section X.I.

G. Dependent Claim 17

Element	Claim Language
17	<i>The display device, according to claim 16, wherein the seal member further includes a fifth part and a sixth part, the fifth part of the seal member extends from another end of the first part, and the sixth part of the seal member extends from another end of the second part and includes a second plurality of conductive particles, and the fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region</i>

205. As discussed, *Fujikawa* at least renders obvious the additional limitation in claim 17. *See* Section X.J.

H. Dependent Claim 18

Element	Claim Language
18	<i>The display device, according to claim 17, wherein the first edge of the seal region is positioned opposite to the second edge of the seal region with respect to the display region</i>

206. As discussed, *Fujikawa* discloses the additional limitation in claim 18.

See Section X.K.

I. Dependent Claim 19

Element	Claim Language
19[pre]	<i>The display device, according to claim 18</i>
19[a]	<i>wherein the first substrate further includes a first conductive point and a second conductive point, different from the plurality of conductive points, and the first conductive point, the second conductive point and the plurality of conductive points are disposed apart from each other, and</i>
19[b]	<i>the first conductive point is electrically connected to the common electrode through the first plurality of conductive particles and the second conductive point is electrically connected to the common electrode through the second plurality of conductive particles</i>

207. As discussed, *Fujikawa* discloses or renders obvious the additional limitations in claim 19. See Section X.L.

J. Dependent Claim 20

Element	Claim Language
20	<i>An electronic device comprising the display device according to</i>

Element	Claim Language
	<i>claim 13</i>

208. As discussed, *Fujikawa* discloses the additional limitation in claim 20.

See Section X.M.

XII. FUJIKAWA AND IKEGUCHI RENDER OBVIOUS CLAIMS 7-13 AND 15-20
(GROUND 4)

A. Independent Claim 7

1. 7[pre]-7[a]

Element	Claim Language
7[pre]	<i>A display device, comprising</i>
7[a]	<i>a first substrate including a pixel region and a seal region which is defined around the pixel region on a first surface of the first substrate</i>

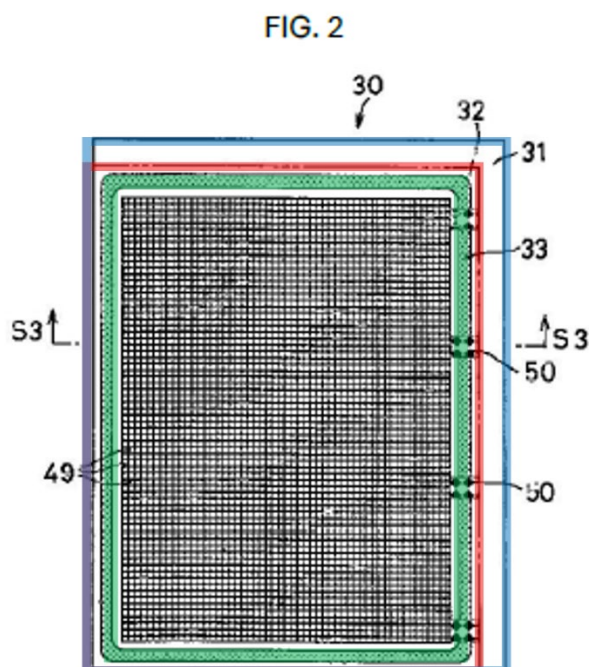
209. As discussed above, it is my opinion that *Fujikawa* discloses each of these limitations. See Sections X.A.1-X.A.2.

2. 7[b]

Element	Claim Language
7[b]	<i>the pixel region including a plurality of pixels and a plurality of active elements, and the seal region forming a rectangular ring</i>

Element	Claim Language
	<i>shape, wherein the active elements are thin film transistors disposed on the first substrate; and</i>

210. As discussed above, *Fujikawa* discloses this limitation. Section X.A.3. Alternatively, it is my opinion that the seal region having “*a rectangular ring shape*” would have been obvious over *Ikeguchi*. *Ikeguchi* discloses two substrates “disposed and layered spaced apart” and “bonded together by a sealing material 33 provided in a rectangular closed-loop shape.” *Ikeguchi*, [0027], [0030], [0039]. This is shown below:



Ikeguchi at Fig. 2 (annotated). A POSITA would have been motivated to use such a

rectangular seal region to match the shapes of the substrates and pixel region, and in turn reduce the amount of sealing material used. Furthermore, given the commonly used rectangular shape in display applications, a seal, the main purpose of which is to retain liquid crystalline material in the cavity between two opposing substrates, would therefore desirably follow the shape of the portions where liquid crystalline material resides. Having the seal occupy a space that is different from the region containing active components of the display (i.e., the pixels and TFTs) would result in wasted liquid crystalline material as well as wasted space, which is a valuable commodity in display applications. In my opinion, a POSITA would have had a reasonable expectation of success implementing this well-known seal region shape in *Fujikawa's* device.

3. 7[c]-7[h]

Element	Claim Language
7[c]	<i>a second substrate including a common electrode on a second surface; and</i>
7[d]	<i>a seal member bonding the first substrate and the second substrate so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels</i>
7[e]	<i>wherein the first substrate includes a protruding region which</i>

Element	Claim Language
	<i>protrudes over the second substrate in a plan-view of the first substrate</i>
7[f]	<i>the seal region includes a first side, a second side, a third side and a fourth side, the first side is positioned between the pixel region and the protruding region, and opposed to the third side, and the second side is opposed to the fourth side</i>
7[g]	<i>the seal member is disposed between the first substrate and the second substrate</i>
7[h]	<i>and positioned on the first side, the second side, the third side and the fourth side continuously, forms a closed-ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate, and is formed continuously around the entire pixel region without the use of a plug</i>

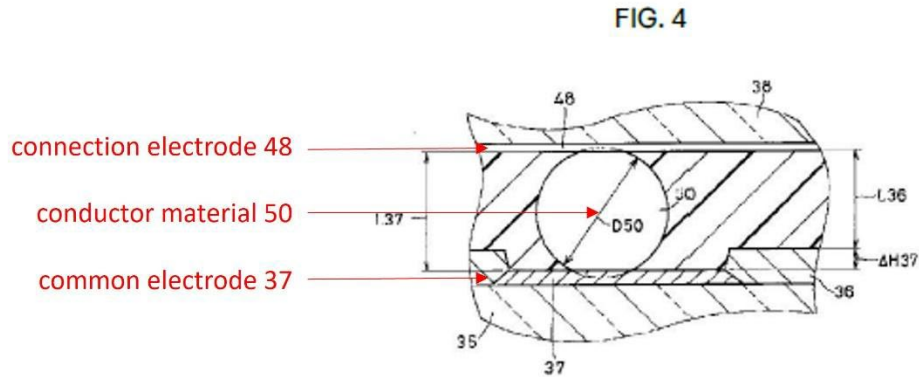
211. As discussed above, it is my opinion *Fujikawa* discloses each of these limitations. See Sections X.A.4-X.A.9.

4. 7[i]

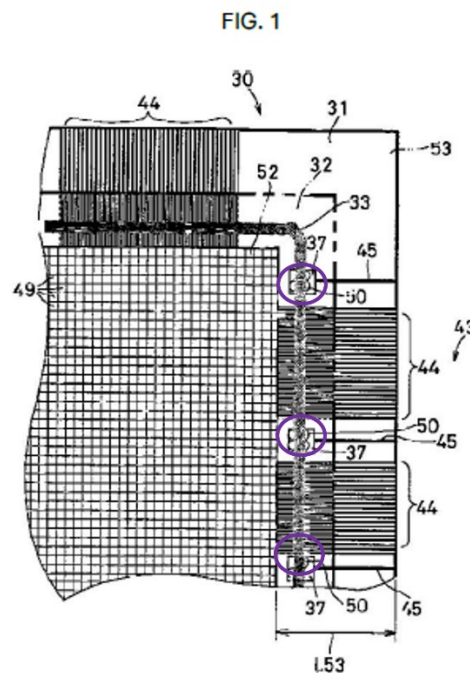
Element	Claim Language
7[i]	<i>a first part of the seal member disposed on the third side which is opposed to the protruding region with respect to the pixel region includes a plurality of conductive particles</i>

212. As discussed above, *Fujikawa* discloses or at least renders obvious this limitation. *See supra* Section X.A.10; *Fujikawa* at [0047]. Alternatively, it would have been obvious to have additional conductive particles (with more conductive electrodes 9g, *see* Section XII.A.5) in *Fujikawa*'s design in view of *Ikeguchi*.

213. *Ikeguchi* discloses a liquid crystal display device that reduces the non-display area while achieving reliable conduction between substrates and improved display quality and stability. *Ikeguchi* at [0013], [0047]. *Ikeguchi*'s improved device includes two electrode substrates (31, 32) bonded together using a sealing material 33. *Ikeguchi* at [0027]-[0030], [0042]. The sealing material 33 is mixed with a conductive material to facilitate electrical connectivity between substrates. *Ikeguchi* at [0015]-[0018], [0037], [0039]-[0040], [0042]-[0043]. In particular, the conductor material 50 in sealing material 33 can comprise "conductive particles in which metal layers are formed on the surfaces of synthetic-resin base particles." *Ikeguchi* at [0037], [0040], [0042]-[0043]. This is shown in Figure 4 below:



Ikeguchi at Fig. 4 (annotated). As *Ikeguchi* illustrates in Figure 1, numerous, discrete locations of conductor material 50 can be provided along the sealing region:



Ikeguchi at Fig. 1 (annotated); *Ikeguchi* at [0045]. Like the conductive particles in conductive material 106 in *Fujikawa*, conductor material 50 in *Ikeguchi* discloses

the claimed “*conductive particles*.” *Fujikawa* Figure 9 and *Ikeguchi* Figure 4 are provided side-by-side below:

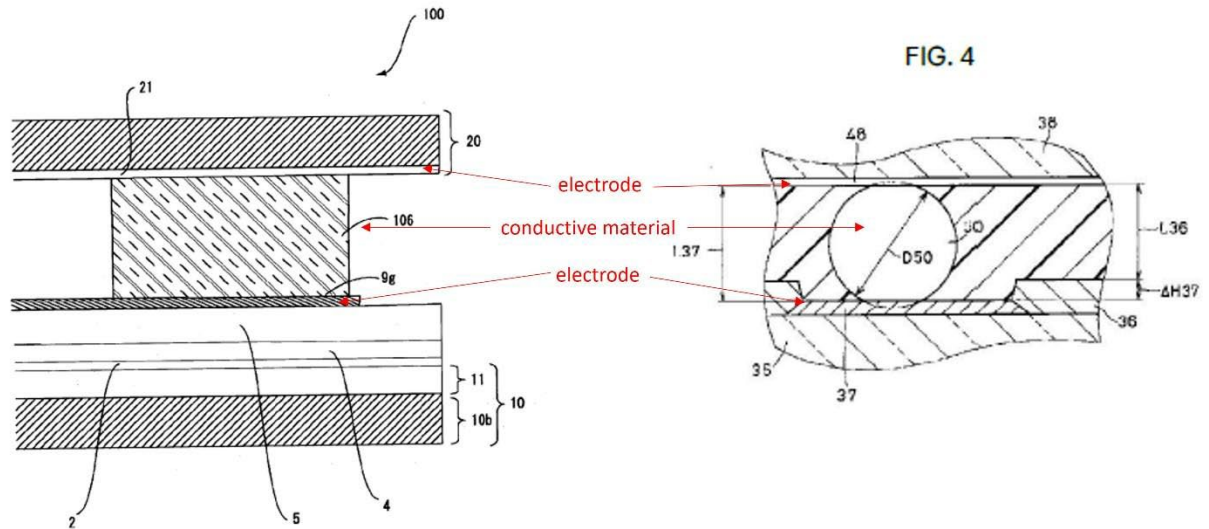


FIG.9

Fujikawa at Fig. 9 (left); *Ikeguchi* at Fig. 4 (right).

214. A POSITA would have been motivated to combine *Fujikawa* and *Ikeguchi* to provide a plurality of conductive particles in the seal member along the first side of the seal member, as claimed. As an initial matter, *Fujikawa* and *Ikeguchi* are analogous art to the '606 patent. *Fujikawa* and *Ikeguchi* are in the same field of endeavor as each other and the '606 patent. As noted above, the '606 patent relates to a method of manufacturing a liquid crystal device (and the resulting liquid crystal device). Section VII.A; '606 patent at 1:19-21. It discloses a liquid crystal device

that includes a seal member having a plurality of conductive particles and a plurality of dot conductive points separated from each other to electrically connect two substrates. *See, e.g.*, '606 patent at 38:26-67, Fig. 30. So too does *Fujikawa* disclose an improved liquid crystal display device with a plurality of “[c]onductive electrodes 9g and conductive materials 106 . . . in areas corresponding to four corners of the counter substrate for electrical continuity” for the substrates and to reduce the non-display area. *See, e.g., Fujikawa*, [0010]-[0011], [0047], [0079], Figs. 1A, 9. And, *Ikeguchi* likewise discloses a plurality of common electrodes 37 and plurality of conductor materials 50 in sealing material 33 to provide reliable conduction between substrates and reduce the non-display area. *Ikeguchi*, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047].

215. A POSITA would have been motivated to have additional conductive particles in *Fujikawa*’s sealing material 107 (“*seal member*”) in view of *Ikeguchi* to further reduce non-display area, achieve reliable conduction between substrates, and improve display quality and stability. As discussed above, *Fujikawa* discloses that, in existing devices, a “frame region” that “does not directly contribute to the display” is often too large. *Fujikawa* at [0010]. As a result, *Fujikawa* aims to “decrease the proportion of the width of the frame region,” and in turn, increase the relative image display region, while keeping the liquid crystal device small. A POSITA would have looked to references like *Ikeguchi*, that solve a similar problem, and would have

been motivated to implement its improvements (multiple conductive particles in the seal material) in *Fujikawa*'s design to reduce the non-display area, achieve "reliable conduction," and improve display quality and stability. *Ikeguchi* at [0013], [0037], [0039]-[0040], [0042]-[0043], [0047]. Indeed, *Ikeguchi* explains, with its design, a "non-display region 53 in which the sealing material 33, the common electrode 37, the connection electrode, and the conductive material 50 are disposed can thus be made small." *Ikeguchi* at [0043].

216. Moreover as discussed above in Section V.C and elsewhere, additional points of electrical contact vertically from the common electrode are beneficial for retaining a stable voltage spatially across the common electrode. As the display scales to larger sizes, simply connecting to the common electrode at the corners of the display does not allow for a stable voltage across the electrode as pixel voltages are varied at different times across the display, and additionally can result in a large impedance in the connection to the common electrode because of the large resistance of only a few narrow electrical connections. The introduction of additional electrical connections beyond the corners will shorten the distance between those common electrode connections at the edges of the display, decreasing the spatial voltage variability. A variety of examples, including those discussed in Section V.C, have introduced conductive material into the seal material to afford conductivity over most of the seal rather than introducing a conductive material at individual gaps in

the seals, decreasing overall resistance of the connection to the common electrode while simultaneously reducing voltage variation across the common electrode. The additional regions of conductive material, and the associated greater number of conductive particles, would therefore result in a more stable common electrode with a comparatively lower impedance. The examples discussed above incorporate the dispersed conductive particles in a manner where the conductivity is realized only in the z-direction (the direction normal to both glass panes or substrates) by way of design, and the seal retains its otherwise electrically insulating characteristics in the lateral directions to allow for circuit design flexibility.

217. In my opinion, a POSITA would have done this with a reasonable expectation of success. Adding additional conductive particles along the side of *Fujikawa*'s sealing material 107 would have been the simple use of a known design to improve a similar device in the same way to achieve a predictable result (namely, a liquid crystal display device with improved conductivity and reduced non-display area). It would have required no more than ordinary skill to provide additional conductive particles along the side of *Fujikawa*'s sealing material. And a POSITA would have understood doing so would not frustrate *Fujikawa*'s existing design, while offering the known benefits described above. *Fujikawa* at [0047] ("number of conductive electrodes 9g, and the like may be appropriately changed").

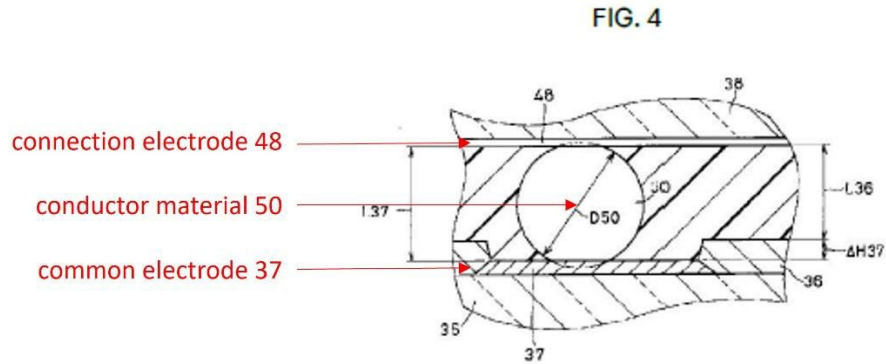
5. 7[j]

Element	Claim Language
7[j]	<i>a plurality of dot conductive points are disposed on the third side of the first substrate, all of the plurality of the dot conductive points are electrically connected to the common electrode, and</i>

218. As discussed above, *Fujikawa* discloses or at least renders obvious this limitation. *See supra* Section X.A.11; *Fujikawa* at [0047]. Alternatively, it would have been obvious to have additional dot conductive points in *Fujikawa*’s design in view of *Ikeguchi*.

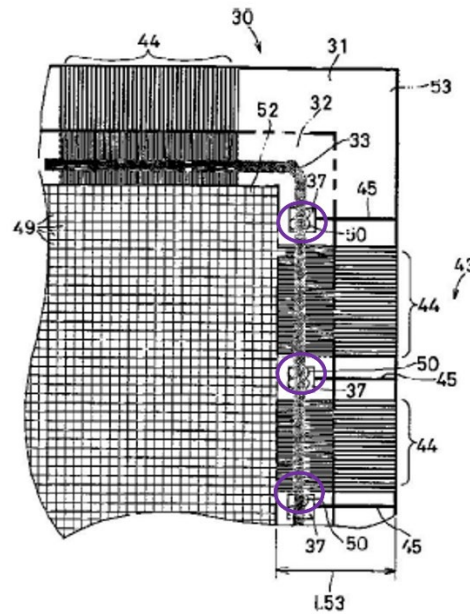
219. *Ikeguchi* discloses an improved liquid crystal device that reduces non-display area while achieving reliable conduction between substrates and improving display quality and stability. *E.g.*, *Ikeguchi* at [0013], [0043], [0047]. *Ikeguchi*’s improved display device includes two electrode substrates (31, 32) bonded together using a sealing material 33. *Ikeguchi* at [0027]-[0030], [0042]. *Ikeguchi* explains it is needed to electrically connect the substrates and discloses a “conducting portion” to do so. *Ikeguchi* at [0037]. This conducting portion includes common electrode 37 on the first substrate, connection electrode 48 on the second substrate, and conductor material 50 in the seal material 33 “sandwiched” in between the two electrodes. *Ikeguchi* at [0037] (“counter electrode 42 and the connection electrode 48 may be

realized by a single electrode”), [0039], [0040], [0042]-[0043]. This is shown below in Figure 4:



Ikeguchi at Fig. 4 (annotated). And as *Ikeguchi* shows in Figure 1 below, numerous, discrete locations of common electrode 37 and conductor material 50 along the side of the substrate can be provided:

FIG. 1



Ikeguchi at Fig. 1 (annotated). Like the conductive electrodes 9g in *Fujikawa*, the common electrode 37 in *Ikeguchi* is the claimed “***dot conductive points.***” *Fujikawa* Figure 9 and *Ikeguchi* Figure 4 are provided side-by-side below:

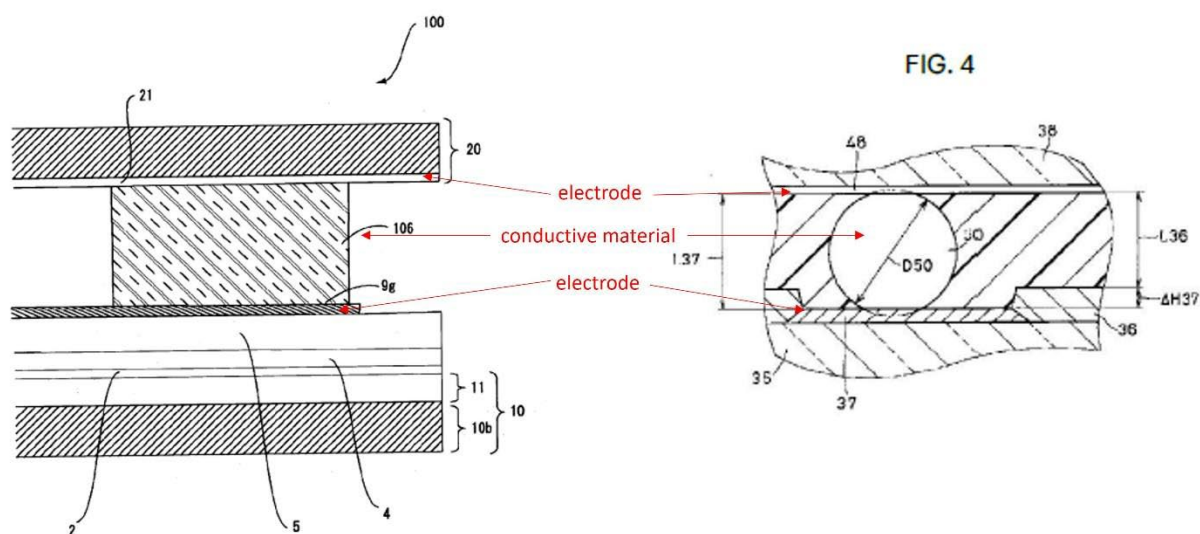


FIG.9

Fujikawa at Fig. 9 (left); *Ikeguchi* at Fig. 4 (right).

220. A POSITA would have been motivated to combine *Fujikawa* and *Ikeguchi* to provide a plurality of dot conductive points along the side of the first substrate. As an initial matter, *Fujikawa* and *Ikeguchi* are analogous art to the '606 patent. *Id.* *Fujikawa* and *Ikeguchi* are in the same field of endeavor as each other and as the '606 patent. As noted, the '606 patent relates to a method of manufacturing a liquid crystal device (and the resulting liquid crystal device). *See* Section VII.A; '606 patent at 1:19-21. It discloses a liquid crystal device that includes a seal member having a plurality of conductive particles and a plurality of dot conductive points separated from each other to electrically connect two substrates. *See, e.g.,* '606

patent at 38:26-67, Fig. 30. So too does *Fujikawa* disclose an improved liquid crystal display device with a plurality of “[c]onductive electrodes 9g and conductive materials 106 . . . in areas corresponding to four corners of the counter substrate for electrical continuity” for the substrates and to reduce the non-display area. *See, e.g., Fujikawa*, [0010]-[0011], [0047], [0079], Figs. 1A, 9. *Ikeguchi* likewise discloses a plurality of common electrodes 37 and plurality of conductor materials 50 in sealing material 33 to provide reliable conduction between substrates and reduce the non-display area. *Ikeguchi*, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047].

221. A POSITA would have been motivated to provide additional dot conductive points along the side of *Fujikawa*’s first substrate in view of *Ikeguchi* to further reduce non-display area, achieve reliable conduction between the substrates, and improve display quality and stability. As noted, *Fujikawa* discloses, in existing liquid display devices, the “frame region” that “does not directly contribute to the display” is too large. *Fujikawa* at [0010]. *Fujikawa* thus strives to “decrease the proportion of the width of the frame region,” and in turn, increase the relative image display region, while keeping the liquid crystal display device small. *Id.* A POSITA would have looked to references like *Ikeguchi*, that solve a similar problem, and would have been motivated to implement its improvements (multiple dot conductive points along the edge of the first substrate) in *Fujikawa*’s design to reduce non-display area, achieve reliable conduction, and improve display quality and stability.

Ikeguchi, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047]. Indeed, *Ikeguchi* explains, with its design, a “non-display region 53 in which the sealing material 33, the common electrode 37, the connection electrode, and the conductive material 50 are disposed can thus be made small.” *Ikeguchi* at [0043].

222. Moreover as discussed above in Section V.C and elsewhere, additional points of electrical contact vertically from the common electrode are beneficial for retaining a stable voltage spatially across the common electrode. As the display scales to larger sizes, simply connecting to the common electrode at the corners of the display does not allow for a stable voltage across the electrode as pixel voltages are varied at different times across the display, and additionally can result in a large impedance in the connection to the common electrode because of the large resistance of only a few narrow electrical connections. The introduction of additional electrical connections beyond the corners will shorten the distance between those common electrode connections at the edges of the display, decreasing the spatial voltage variability. A variety of examples, including those discussed in Section V.C, have introduced conductive material into the seal material to afford conductivity over most of the seal rather than introducing a conductive material at individual gaps in the seals, decreasing overall resistance of the connection to the common electrode while simultaneously reducing voltage variation across the common electrode. The additional regions of conductive material, and the associated greater number of

conductive particles, would therefore result in a more stable common electrode with a comparatively lower impedance. The examples discussed above incorporate the dispersed conductive particles in a manner where the conductivity is realized only in the z-direction (the direction normal to both glass panes or substrates) by way of design, and the seal retains its otherwise electrically insulating characteristics in the lateral directions to allow for circuit design flexibility.

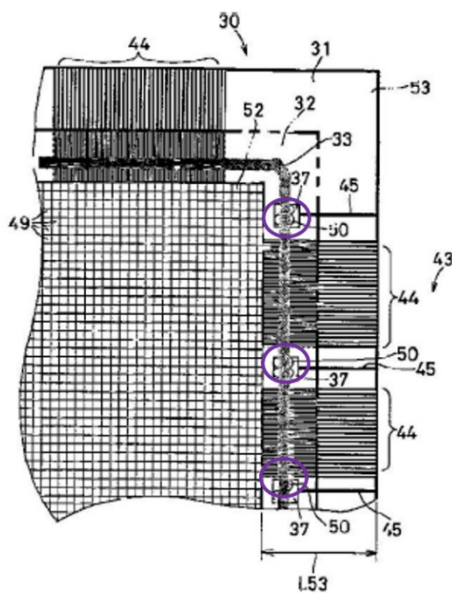
223. In my opinion, a POSITA would have done so with a reasonable expectation of success. Adding additional dot conductive points along the side of *Fujikawa's* first substrate would have been the simple use of a known design to improve a similar device in the same way to achieve a predictable result (namely, a liquid crystal display device with improved conductivity and reduced non-display area). It would have required no more than ordinary skill to add more dot conductive points along the side of *Fujikawa's* TFT array substrate 10. And the POSITA would have understood that doing so would not have frustrated *Fujikawa's* existing design, while offering known benefits discussed above. *Fujikawa*, [0047] (“number of conductive electrodes 9g, and the like may be appropriately changed”).

6. 7[k]

Element	Claim Language
7[k]	<i>each of the plurality of the dot conductive points are spaced part from each other</i>

224. As discussed above, *Fujikawa* discloses or at least renders obvious this limitation, in my opinion. Sections X.A.12. Alternatively, to the extent *Fujikawa* is modified in view of *Ikeguchi* to have additional plurality of conductive particles and dot conductive points (Sections XII.A.4-XII.A.5), this limitation would have been obvious in view of *Fujikawa* and *Ikeguchi*. Indeed, as shown in Figure 1, numerous, discrete locations of common electrode 37 and conductor material 50 can be “*spaced apart from each other*”:

FIG. 1



Ikeguchi at Fig. 1.

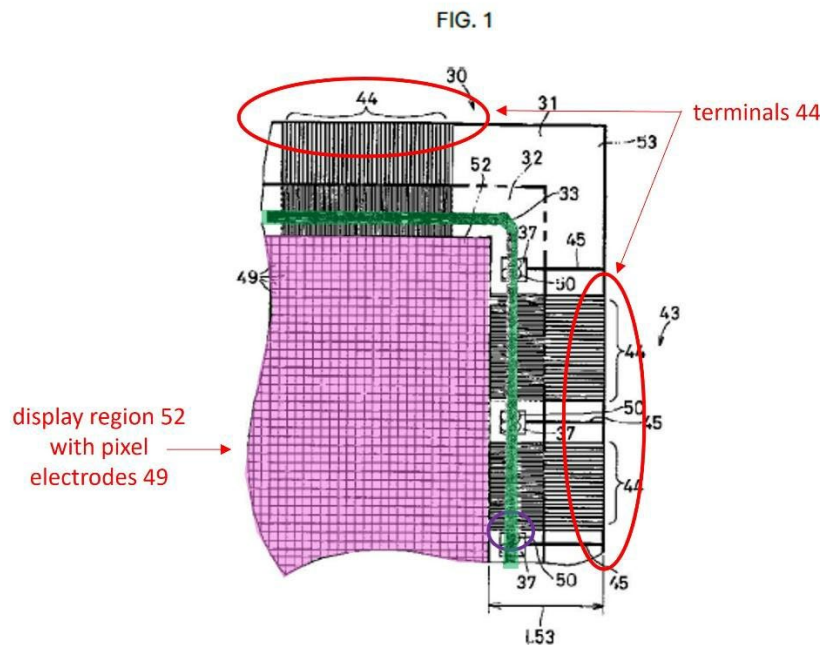
7. 7[1]

Element	Claim Language
7[1]	<i>wherein the first substrate includes a plurality of wiring lines that connect to the plurality of active elements, and the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points</i>

225. As discussed, *Fujikawa* discloses this limitation. See Sections X.A.13. In the event Patent Owner argues that *Fujikawa*'s data lines can only include lines 6a, it would have been obvious to have the wiring lines “*extend onto the protruding*

region across the seal member” in view of Ikeguchi.

226. *Ikeguchi* discloses a driver integrated circuit that drives the display. *Ikeguchi* at [0031]-[0032]. The drive integrated circuit comprises input terminals 44 located on a “one-side edge” of first electrode substrate 31 outside *Ikeguchi*’s seal material 33, as shown in Figure 1:



Ikeguchi at Fig. 1 (annotated), [0035] (explaining that terminals 44 “formed in the portions thereof protruding outward from the second electrode substrate”). *Ikeguchi* explains these terminals in the driver integrated circuit are “electrically connected to” the TFTs in the pixel electrodes in the display region 52 “via connection lines.” *Ikeguchi* at [0034]; *Ikeguchi* at [0033]-[0035]. A POSITA would have understood the “connection lines” extend from the TFTs in the display region, across the seal

material, out to the terminals in the protruding regions to “electrically connect[]” the TFTs and the driver integrated circuit. A POSITA would have been motivated to implement such a design in *Fujikawa*. The driver integrated circuit can be within the sealing region or outside the sealing region. It would have been the simple selection of a known design to obtain a predictable result to have the driver integrated circuit outside the seal region and in turn have the wires that connect that circuit to the TFTs in the display area cross the seal region. *See, e.g.*, Ex. 1025 at Fig. 1, [0017]-[0019]. A POSITA would have reasonably expected this modification would be successful, for it would require no more than ordinary skill to implement.

B. Dependent Claim 8

1. 8[pre]

Element	Claim Language
8[pre]	<i>The display device, according to claim 7</i>

227. As discussed above, *Fujikawa* and *Ikeguchi* render obvious claim 7. *See* Section XII.A.

2. 8[a]-8[c]

Element	Claim Language
8[a]	<i>wherein the first substrate includes a first conductive point on the second side and the seal member includes a second part of the seal</i>

Element	Claim Language
	<i>member on the second side</i>
8[b]	<i>the second part of the seal member extends from one end of the first part of the seal member over the first conductive point on the second side, and the second part of the seal member includes a plurality of conductive particles, and</i>
8[c]	<i>wherein the first conductive point is electrically connected to the common electrode</i>

228. As discussed, *Fujikawa* discloses or renders obvious these limitations. Sections X.B.2-X.B.4. Alternatively, a POSITA would have been motivated to have a plurality of conductive points and plurality of conductive particles on the second side of the first substrate to reduce the non-display area, achieve reliable conduction between two substrates (which would include a decreased impedance), and improve display quality and stability (by improving the spatial uniformity across the common electrode) in view of *Ikeguchi*. See Sections XII.A.4-XII.A.6. A POSITA would have had a reasonable expectation of success doing so. Sections XII.A.4-XII.A.6.

C. Dependent Claim 9

1. 9[pre]

Element	Claim Language
9[pre]	<i>The display device, according to claim 8</i>

229. As discussed above, *Fujikawa* and *Ikeguchi* render obvious claim 8. *See*

2. 9[a]-9[c]

Element	Claim Language
9[a]	<i>wherein the first substrate includes a second conductive point on the fourth side and the seal member includes a third part of the seal member on the fourth side</i>
9[b]	<i>the third part of the seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side, and the third part of the seal member includes a plurality of conductive particles, and</i>
9[c]	<i>wherein the second conductive point is electrically connected to the common electrode</i>

230. As discussed, *Fujikawa* discloses or renders obvious these limitations. Sections X.C.2-X.C.4. Alternatively, a POSITA would have been motivated to have a plurality of conductive points and plurality of conductive particles on the fourth

side of the first substrate to reduce the non-display area, achieve reliable conduction between two substrates (which would include a decreased impedance), and improve display quality and stability (by improving the spatial uniformity across the common electrode) in view of *Ikeguchi*. Sections XII.A.4-XII.A.6. And a POSITA would have had a reasonable expectation of success doing so. Sections XII.A.4-XII.A.6.

D. Dependent Claims 10-12

Element	Claim Language
10	<i>The display device, according to claim 7, wherein the seal member extends to a first edge of the seal region opposite to the pixel region on the second side</i>
11	<i>The display device according to claim 10, wherein the seal member extends to a second edge of the seal region opposite to the pixel region on the fourth side</i>
12	<i>An electronic device comprising the display device according to claim 7</i>

231. As discussed, *Fujikawa* discloses the additional limitations in these claims. See Sections X.D-X.F.

E. Independent Claim 13

1. 13[pre]-13[h]

Element	Claim Language
13[pre]	<i>A display device, comprising</i>
13[a]	<i>a first substrate including a plurality of pixel electrodes, a plurality of active elements and a plurality of wiring elements that connect to the plurality of active elements, wherein the plurality of active elements are thin film transistors disposed on the first substrate</i>
13[b]	<i>a second substrate including a common electrode, wherein the common electrode is disposed on the second substrate</i>
13[c]	<i>a display region in which the plurality of pixel electrodes and the plurality of active elements are aligned in a plan-view of the first substrate</i>
13[d]	<i>a seal region positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed</i>
13[e]	<i>a seal member being disposed in the seal region and bonding the</i>

Element	Claim Language
	<i>first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes</i>
13[f]	<i>the seal member forming a closed-ring shape in which the display region is positioned without protruding from the second substrate in the plan-view of the first substrate, the seal member is disposed between the first substrate and the second substrate, and the seal member is formed continuously around the entire display region without the use of a plug</i>
13[g]	<i>wherein the first substrate includes a protruding region which protrudes over the second substrate in the plan-view of the first substrate and a plurality of conductive portions</i>
13[h]	<i>the seal region includes a first portion and a second portion, the first portion is positioned at least between the display region and the protruding region, and the second portion is positioned at least opposite to the protruding region with respect to the display region, and</i>

232. As discussed above, *Fujikawa* discloses these limitations. See Sections X.G.1-X.G.9.

2. 13[i]-13[k]

Element	Claim Language
13[i]	<i>the seal member includes a first part and a second part, the first part of the seal member is positioned on the first portion and the second part of the seal member is positioned on the second portion, and the second part of the seal member includes a plurality of conductive particles</i>
13[j]	<i>a plurality of dot conductive points are disposed on the second portion of the first substrate, all of the plurality of dot conductive points are electrically connected to the common electrode</i>
13[k]	<i>each of the plurality of the dot conductive points are spaced apart from each other, and</i>

233. These limitations are substantially similar to limitations 7[i], 7[j], and 7[k]. Sections X.G.10-X.G.12. For the reasons above, it is my opinion *Fujikawa* and *Ikeguchi* render obvious these limitations. Sections XII.A.4-XII.A.6.

3. 13[I]

Element	Claim Language
13[I]	<i>the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points</i>

234. This limitation is substantially similar to limitation 7[I]. *See* Section X.G.13. As discussed, *Fujikawa* and *Ikeguchi* render obvious this limitation. Section XII.A.7.

F. Dependent Claim 15

Element	Claim Language
15	<i>The display device, according to claim 13, wherein the seal member further includes a third part and a fourth part, the third part of the seal member extends from one end of the first part, and the fourth part of the seal member extends from one end of the second part and includes a first plurality of conductive particles</i>

235. For the reasons identified for limitations 7[b], 7[d], and 7[i], *Fujikawa* and *Ikeguchi* render obvious the additional limitation in claim 15. *See* Sections X.H, X.A.3, X.A.5, X.A.10, XII.A.2, XII.A.4.

G. Dependent Claim 16

Element	Claim Language
16	<i>The display device, according to claim 15, wherein the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region</i>

236. As discussed above, *Fujikawa* discloses or at least renders obvious the additional limitation in claim 16. See Section X.I.

H. Dependent Claim 17

Element	Claim Language
17	<i>The display device, according to claim 16, wherein the seal member further includes a fifth part and a sixth part, the fifth part of the seal member extends from another end of the first part, and the sixth part of the seal member extends from another end of the second part and includes a second plurality of conductive particles, and the fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region</i>

237. For the reasons identified for limitations 7[b], 7[d], and 7[i], *Fujikawa* and *Ikeguchi* render obvious the additional limitation in claim 17. See Sections X.J,

X.A.3, X.A.5, X.A.10, XII.A.2, XII.A.4.

I. Dependent Claim 18

Element	Claim Language
18	<i>The display device, according to claim 17, wherein the first edge of the seal region is positioned opposite to the second edge of the seal region with respect to the display region</i>

238. *Fujikawa* discloses the additional limitation in claim 18. Section X.K.

J. Dependent Claim 19

1. 19[pre]

Element	Claim Language
19[pre]	<i>The display device, according to claim 18</i>

239. *Fujikawa* and *Ikeguchi* render obvious claim 18. Sections XII.I.

2. 19[a]-19[b]

Element	Claim Language
19[a]	<i>wherein the first substrate further includes a first conductive point and a second conductive point, different from the plurality of conductive points, and the first conductive point, the second conductive point and the plurality of conductive points are</i>

Element	Claim Language
	<i>disposed apart from each other, and</i>
19[b]	<i>the first conductive point is electrically connected to the common electrode through the first plurality of conductive particles and the second conductive point is electrically connected to the common electrode through the second plurality of conductive particles</i>

240. For the reasons identified in limitations 7[i], 7[j], 7[k], 13[i], 13[j], and 13[k], and claims 8, 9, 15, and 17, *Fujikawa* and *Ikeguchi* render obvious these additional limitations in claim 19. Sections X.L.2-X.L.3, XII.A.4-XII.A.6, XII.B-XII.C, XII.E.2, XII.F, XII.H.

K. Dependent Claim 20

Element	Claim Language
20	<i>An electronic device comprising the display device according to claim 13</i>

241. *Fujikawa* discloses the additional limitation in claim 20. Section X.M.

XIII. FUJIKAWA, KANG, AND IKEGUCHI RENDER OBVIOUS CLAIMS 7-13 AND 15-20 (GROUND 5)

242. For the reasons discussed above in Ground 3 and Ground 4, *Fujikawa*, *Kang*, and *Ikeguchi* render obvious claims 7-13 and 15-20. Sections XI, XII. *Kang*

and *Ikeguchi* disclose different limitations (as noted), and a proposed modification in view of *Ikeguchi* would not impact proposed modifications in view of *Kang*, and vice versa. It would have been obvious to a POSITA to modify *Fujikawa* in view of both *Kang* and *Ikeguchi* to arrive at the claimed invention. Sections XI, XII.

XV. CONCLUSION

243. For the reasons above, it is my opinion that claims 7-13 and 15-20 of the '606 Patent would have been obvious in view of the prior art.

244. In signing this declaration, I understand it will be filed as evidence in contested cases before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I understand I may be subject to cross-examination in this case, and that any cross-examination will take place in the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

245. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that those statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 6, 2024

By: 

Alex Z. Kattamis, Ph.D., P.E.