

Filed: June 6, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case No. 2024-00977
U.S. Patent No. 9,557,606

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,557,606**

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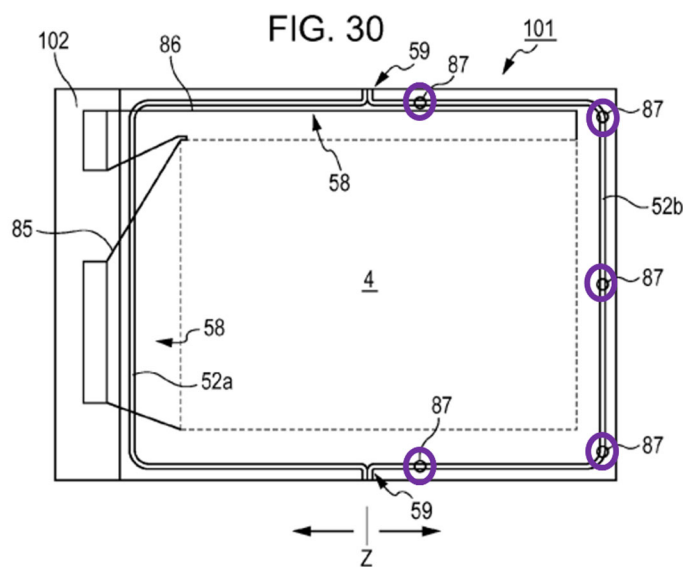
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Ex. 1001	U.S. Patent No. 9,557,606 (“the ’606 patent”)
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Ex. 1004	Declaration of Dr. Alex Kattamis (“Decl.”)
Ex. 1005	U.S. Patent Application Publication No. 2003/0174271 to <i>Fujikawa</i> (“ <i>Fujikawa</i> ”)
Ex. 1006	U.S. Patent Application Publication No. 2004/0257504 to Kang et al. (“ <i>Kang</i> ”)
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Ex. 1015	Wright, Stephen L., “ <i>IBM 9.2-Megapixel Flat-panel Display: Technology and Infrastructure</i> ,” IBM Research Report, RC22363 (W0203-023) (March 8, 2002)

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Ex. 1016	den Boer, Willem, “ <i>Active Matrix Liquid Crystal Displays, Fundamentals and Applications</i> ” (2005)
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Ex. 1020	Complaint for Patent Infringement filed in <i>Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.</i> , 2:23-cv-00515-JRG-RSP, Dkt. 1 (E.D. Tex.) (Nov. 8, 2023), ECF No. 1
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Ex. 1023	Excerpt from Federal Court Management Statistics—Profiles (Dec. 31, 2023), <i>available at</i> https://www.uscourts.gov/sites/default/files/fcms_na_distprofile1231.2023_0.pdf (last accessed May 26, 2024)
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I. Preliminary Statement

Petitioner BOE Technology Group requests *inter partes* review of claims 7-13 and 15-20 of U.S. Patent No. 9,557,606. The '606 patent relates to liquid crystal devices and methods of manufacture. During prosecution, the Applicant sought to capture the idea of “dot conductive points”:



'606 patent at Fig. 30, 38:26-67. But the Examiner repeatedly found conductive points in the prior art. Section III.B. The Applicant then sought to limit the claims to devices made according to a one-drop fill method. *Id.* at 1:46-3:58, 3:62-10:41, 18:36-19:27, 22:36-31:17. But this method was well known at the time; it did not provide a novel, patentable feature. Decl. ¶¶ 41-54. Petitioner requests the Board institute review and cancel claims 7-13 and 15-20.

II. Overview of Technology

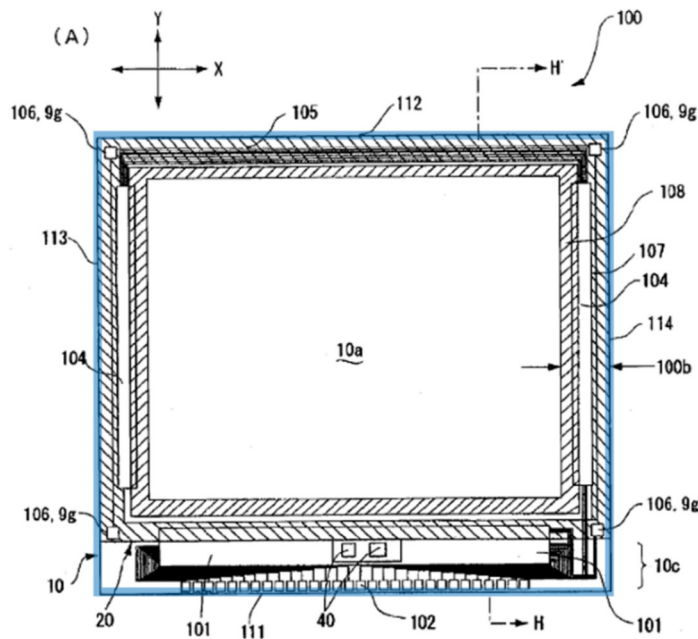
A. *Fujikawa*

U.S. Patent Application Publication No. 2003/0174271 (“*Fujikawa*”) published September 18, 2003, from an application filed January 27, 2003.

Fujikawa is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), (e).

Fujikawa “relates to an electrooptic device,” such as a liquid crystal device, for use in electronic devices like portable computers or telephones. *Fujikawa*, [0002], [0004], [0010]-[0023]. *Fujikawa* explains liquid crystal devices typically comprise a display region 10a and a frame region 100b that lies around the display region but does not directly contribute to the display. *Id.* at [0010]. When a liquid crystal device is in a portable device, “it is required that the image display region 10a should be large and that the entire display should be small.” *Id.* at [0010]. To achieve this, *Fujikawa* “decrease[s] the proportion of the width of the frame region 100b to the total size of the liquid crystal device 100.” *Id.* However, because many components (driving circuits, conductive electrodes, etc.) “are formed around the image display region 10a, the peripheral region” often “cannot be narrowed.” *Id.* To address this, *Fujikawa* seeks to “improv[e] the layout of peripheral circuits” to “narrow[]” this peripheral region. *Id.* at [0011]; *id.* at [0012]-[0023]; Decl. ¶ 56.

Figure 1A is a plan view of *Fujikawa*’s device. *Fujikawa*, [0045]. As shown, *Fujikawa*’s device includes “TFT array substrate 10.” *Id.* at [0046].



Id. at Fig. 1A; Decl. ¶ 57.¹ TFT array substrate 10 has four “substrate edge[s]”—111, 112, 113, 114. *Fujikawa*, [0046]. Disposed on TFT array substrate 10 are “a plurality of pixels formed in a matrix so as to constitute the image display region 10a.” *Id.* at [0053]. The pixels 100a are arranged “in a matrix corresponding to the intersections of a plurality of data lines 6a extending in the Y-direction and a plurality of scanning lines 3a extending in the X-direction.” *Id.* at [0054]. This is shown below:

¹ Annotations added unless otherwise noted.

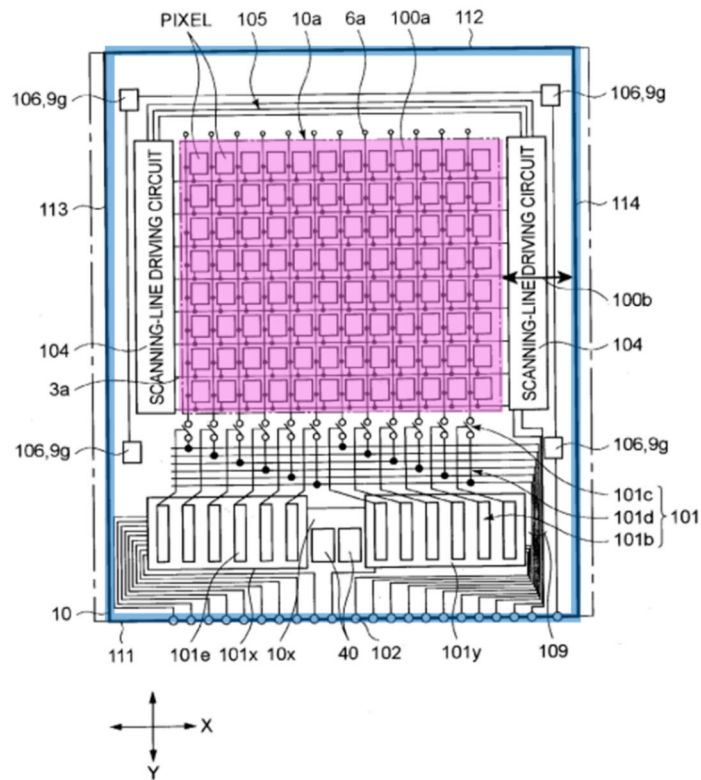


FIG.2

Id. at Fig. 2; Decl. ¶ 57. Each pixel 100a includes “a pixel electrode 9a and a pixel-switching TFT 30 for controlling the pixel electrode 9a.” *Fujikawa*, [0058], [0061].

This is shown below:

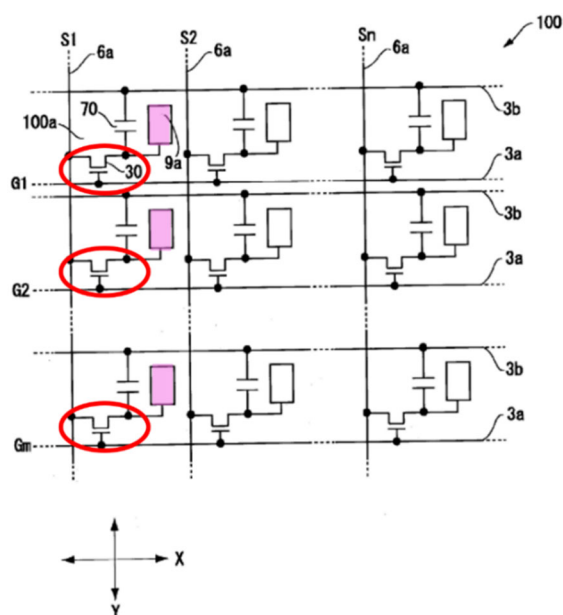
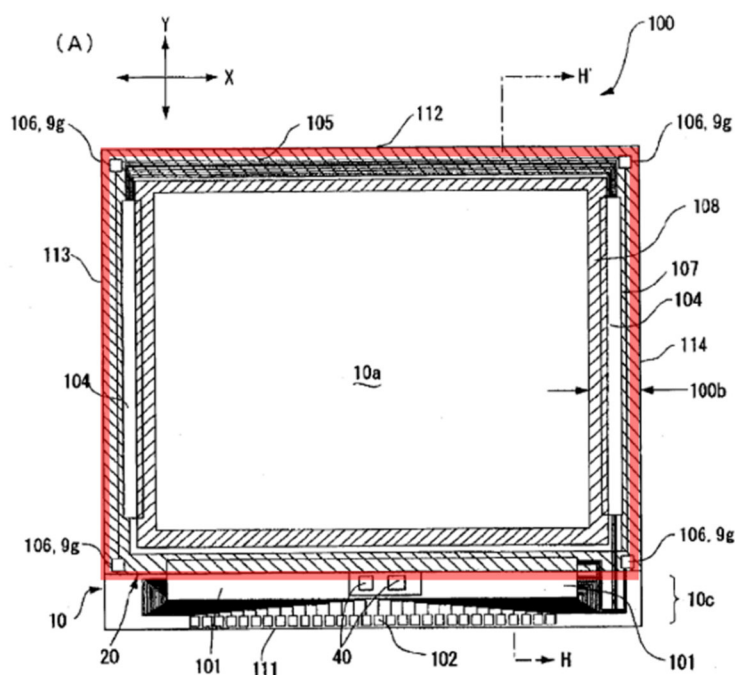


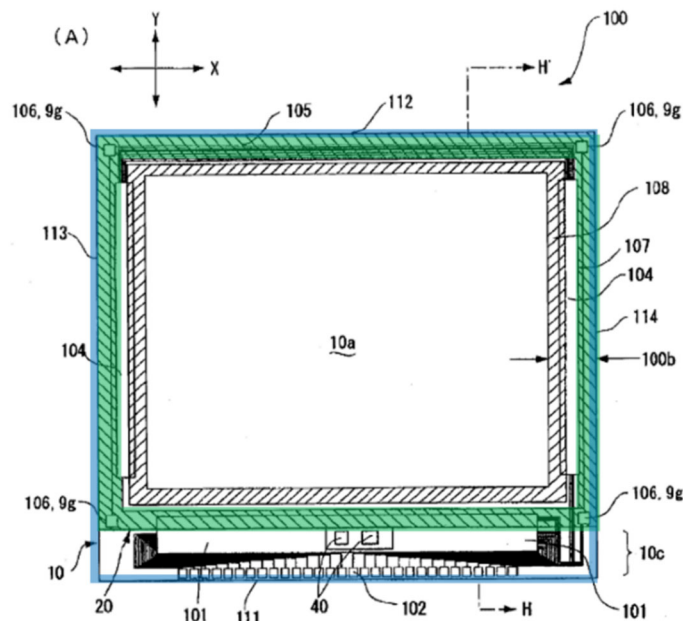
FIG. 4

Id. at Fig. 4. *Fujikawa*'s device also includes “**counter substrate 20.**” *Id.* at [0046].

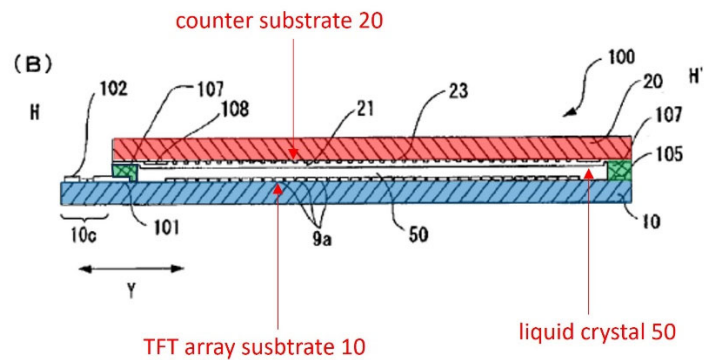


Id. at Fig. 1A. Disposed on counter substrate 20 are “counter electrodes 21.” *Id.* at [0050], [0058], [0079]; Decl. ¶ 58.

Fujikawa explains that the TFT array substrate 10 and counter substrate 20 are “bonded with a predetermined space therebetween by the sealing material 107” “formed on a TFT array substrate 10 . . . along the edge of a counter substrate 20.” *Fujikawa*, [0046], [0049]. The sealing material 107 could “be an adhesive made of a photosetting or thermosetting resin for bonding” and “mixed with a gap material, such as glass fibers or glass beads.” *Id.* at [0049].

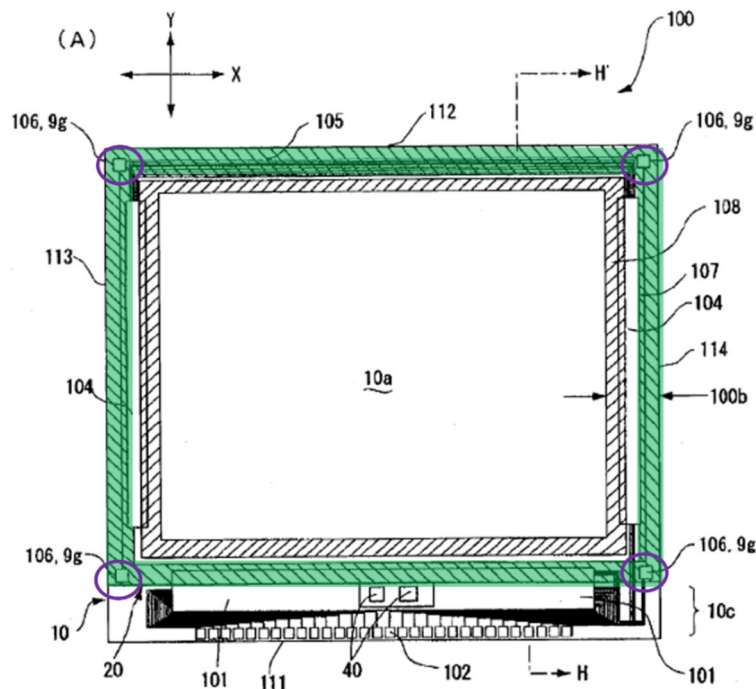


Id. at Fig. 1A; Decl. ¶ 59. Liquid crystal 50 is “held” in the “predetermined space” between the substrates:



Fujikawa at Fig. 1B; Decl. ¶ 59.

Fujikawa also describes a “plurality” of **conductive electrodes 9g** and **conductive materials 106** “formed in areas corresponding to four corners of the counter substrate 20 for electrical continuity between the **TFT array substrate 10** and the **counter substrate 20**.” *Fujikawa*, [0047], [0079].



Id. at Fig. 1A; Decl. ¶ 60. The “plurality of **conductive electrodes 9g** . . . are

electrically connected to the counter electrodes 21 of the counter substrate 20 through the conductive material 106 sandwiched between the substrates.”

Fujikawa, [0079]. The conductive material 106 “can be made of an epoxy resin adhesive component mixed with conductive particles such as silver powder and gold-plated fiber.” *Id.*

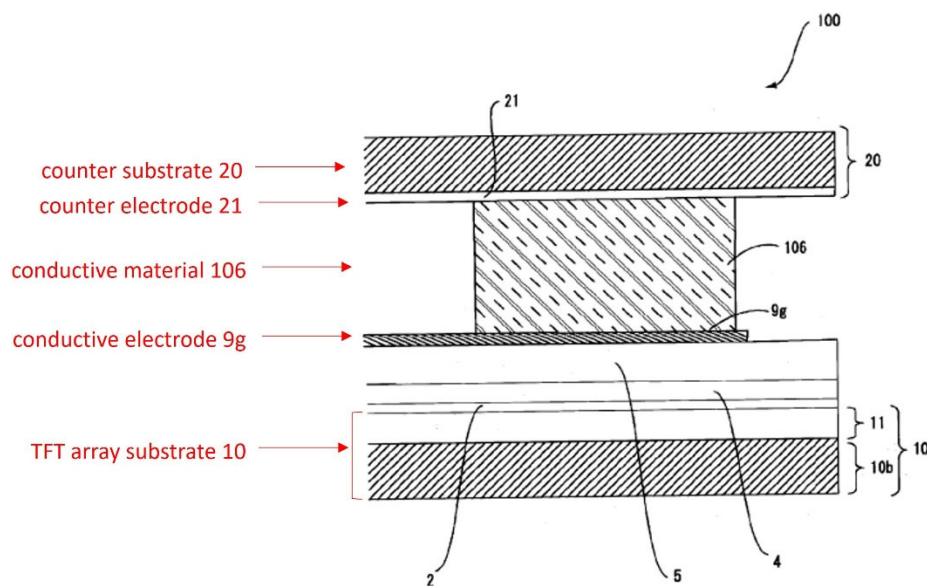


FIG.9

Id. at Fig. 9. *Fujikawa* explains the “number of conductive electrodes 9g and the like may be appropriately changed.” *Id.* at [0079]; Decl. ¶ 60.

B. *Kang*

U.S. Patent Application Publication No. 2004/0257504 (“*Kang*”) published December 23, 2004, from an application filed April 14, 2004. *Kang* is prior art

under at least pre-AIA 35 U.S.C. §§ 102(a), (e).

Kang discloses “a liquid crystal display panel.” *Kang*, [0003], [0037]. Liquid crystal display panels can be formed by a known “vacuum injection method.” *Id.* at [0063]. In a vacuum injection method, “a liquid crystal injection hole of a liquid crystal display panel” is “dipp[ed]” “into a container in a vacuum chamber filled with liquid crystal.” *Id.* Liquid crystal will be “forced into the liquid crystal display panel by the pressure difference between the inner side and the outer side of the liquid crystal display panel.” *Id.* Once filled, “the liquid crystal injection hole is sealed.” *Id.*; Decl. ¶ 62.

Kang explains, however, this vacuum method “has a number of problems.” *Kang*, [0065]. For example, it can “take[] a long time to fill the liquid crystal in the liquid crystal display panel.” *Id.* at [0066]. It also “consumes” “a large quantity of liquid crystal,” increasing the “unit price” of the display. *Id.* at [0067]; Decl. ¶ 63.

To “overcome these problems,” *Kang* notes that a “dropping method” has been “adopted.” *Kang*, [0068]. This method provides a “seal pattern 506” “formed to have a closed shape that encompasses the outer edge of the image display part in order to prevent the leakage of the liquid crystal from the image display part.” *Id.* at [0070]. Liquid crystal is then dropped on the image display part of the substrate (instead of “filled from the outside”) so the liquid crystal is “uniformly distributed . . . by the pressure generated when the” two substrates “are attached to each other.”

Id. at [0069]-[0070]. As *Kang* explains, this reduces manufacturing time and cost relative the vacuum injection method. *Id.* at [0071]-[0072]; Decl. ¶ 64.

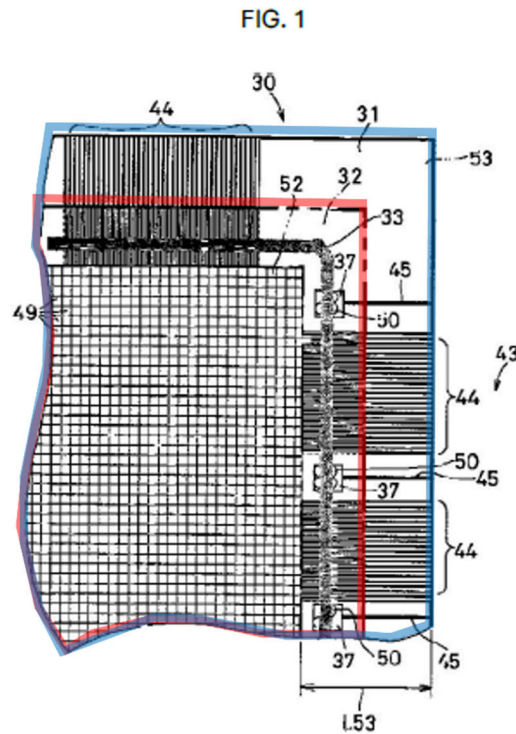
C. *Ikeguchi*²

JP 2003-280030 (“*Ikeguchi*”) published October 2, 2003. *Ikeguchi* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b).

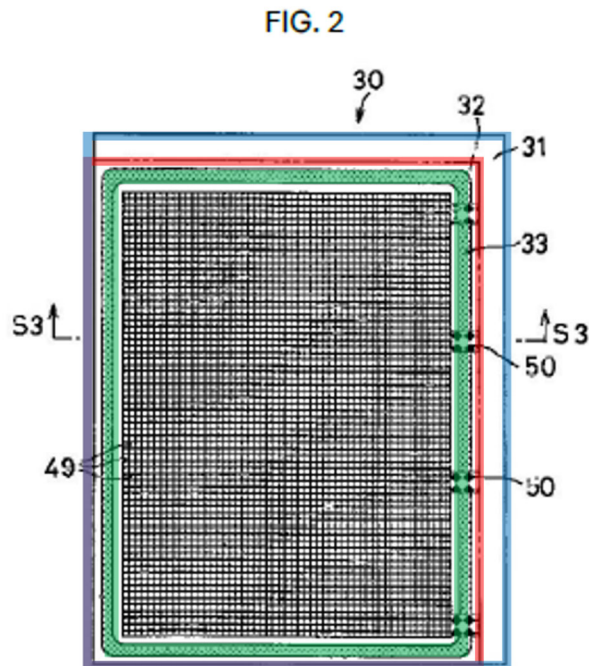
Ikeguchi discloses a liquid crystal display and its method for manufacture. *Ikeguchi*, [0001]. *Ikeguchi* “provide[s] a display element in which the non-display region can be made small and reliable conduction” between the substrates “can be achieved.” *Id.* at [0013]. It teaches “two opposingly disposed electrode substrates” and a bonding material that “bonds the electrode substrates together.” *Id.* at [0014]. A “conductive material having conductivity is mixed into the bonding material” in part of that bonding material “sandwiched between the inter-substrate conducting-electrode portions.” *Id.* at [0014]-[0018]. The “inter-substrate conducting-electrode portions” “creat[e] conduction between” the substrates. *Id.* at [0014]; Decl. ¶ 66.

Figure 1 illustrates an exemplary liquid display element 30 comprising two substrates:

² Citations are to the certified translation of JP 2003-280030.



Ikeguchi, Fig. 1, [0027]-[0030]; Decl. ¶ 67. These two substrates are “bonded together by a **sealing material 33** provided in a rectangular closed-loop shape”:

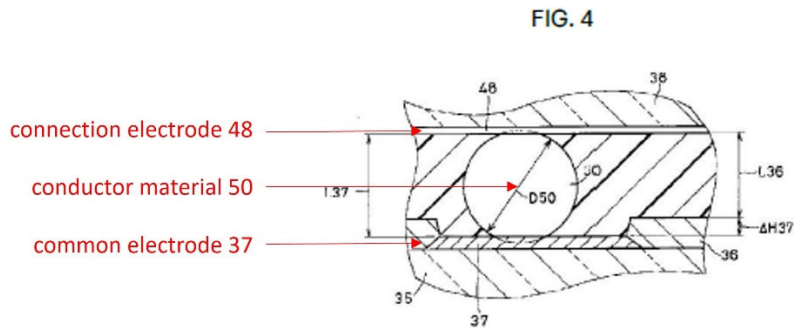


Ikeguchi, Fig. 2, [0027]-[0030]. Sealing material 33 lies between the substrates and “surround[s]” liquid crystal 34 in the display area. *Id.* at [0027], [0030], [0041]; Decl. ¶ 67.

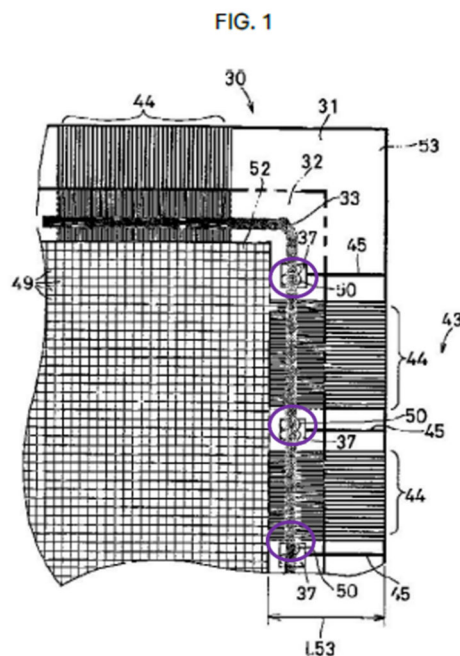
Ikeguchi explains it can be necessary to “creat[e] conduction” between the substrates. *Ikeguchi*, [0037]. A “conducting portion” is provided to do this. *Id.* The conducting portion includes a common electrode 37 formed on the first electrode substrate 31, and a transparent counter electrode 42 and connection electrode 48 formed on the second electrode substrate 32. *Id.* “[C]ounter electrode 42 and the connection electrode 48 may be realized by a single electrode.” *Id.*; Decl. ¶ 68.

“[S]ealing material 33 . . . is sandwiched between the common electrode 37 and the connection electrode 48.” *Ikeguchi*, [0039]. There, sealing material 33

includes **conductor material 50**, which can be “conductive particles in which metal layers are formed on the surfaces of synthetic-resin base particles.” *Id.* at [0037], [0040], [0042]-[0043]. This is shown below:



Id. at Fig. 4; Decl. ¶ 68. And as shown in Figure 1, numerous, discrete locations of **common electrode 37** and **conductor material 50** can be provided along the seal:



Ikeguchi, Figs. 1, 2. This arrangement allows the non-display area to be “made small,” *id.* at [0043]-[0044], and obtains a display element with low electrical resistance and “high display quality and stability,” *id.* at [0047]. Decl. ¶ 68.

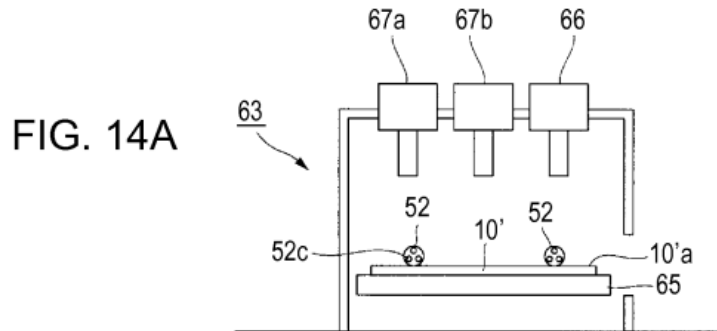
III. The ’606 Patent

A. Specification

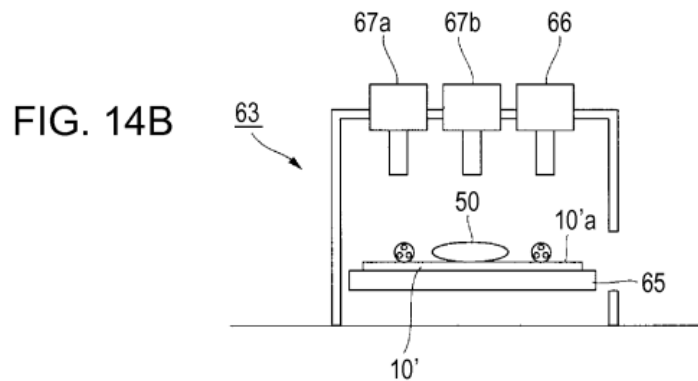
The ’606 patent relates to “a method of manufacturing a liquid crystal device [and] a liquid crystal device.” ’606 patent at 1:19-21. To form such devices, prior systems would coat a sealant “in a peripheral portion of a surface of one substrate.” *Id.* at 1:27-29. A “liquid crystal injection hole” would then be “formed at a part of the sealant.” *Id.* at 1:29-31. Spacers would be placed inside the sealant, and “the other substrate [would be] bonded to the one substrate via the sealant.” *Id.* at 1:31-33. After this “cell is formed,” it is vacuumed and “brought back to atmospheric pressure while the liquid crystal injection hole is dipped” so “the liquid crystal cell is filled with liquid crystal by means of a pressure difference” and surface tension. *Id.* at 1:33-41. Like *Kang*, the ’606 patent recognizes these methods can “take[] an extremely long time.” *Id.* at 1:41-45. As such, and again like *Kang*, the ’606 patent sought to use a “dropping assembly method,” which would reduce manufacturing time and avoid the use of a plug. *Id.* at 1:46-3:58, 3:62-10:41, 18:36-19:27, 22:36-31:17; Decl. ¶ 69.

The method in the ’606 patent includes preparing two substrates. ’606 patent

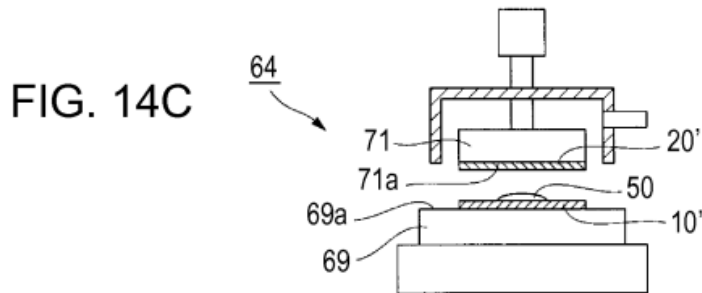
at 18:46-19:15, 22:41-45. The first is loaded onto a substrate load/unload unit and “sealing materials are coated” to form a continuous “ring-shaped portion.” *Id.* at 22:46-61, 22:64-65, 23:5-24:36, Figs. 14A, 17A-17B.



Id. at Fig. 14A. “Liquid crystal 50 is [then] dropped in the ring-shaped portion.” *Id.* at 25:6-15.

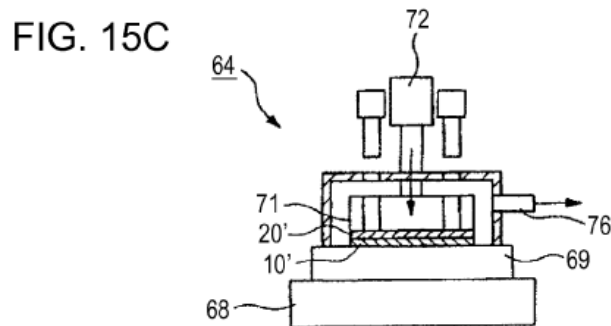


Id. at Fig. 14B. Next, the second substrate is loaded. *Id.* at 25:25-30.



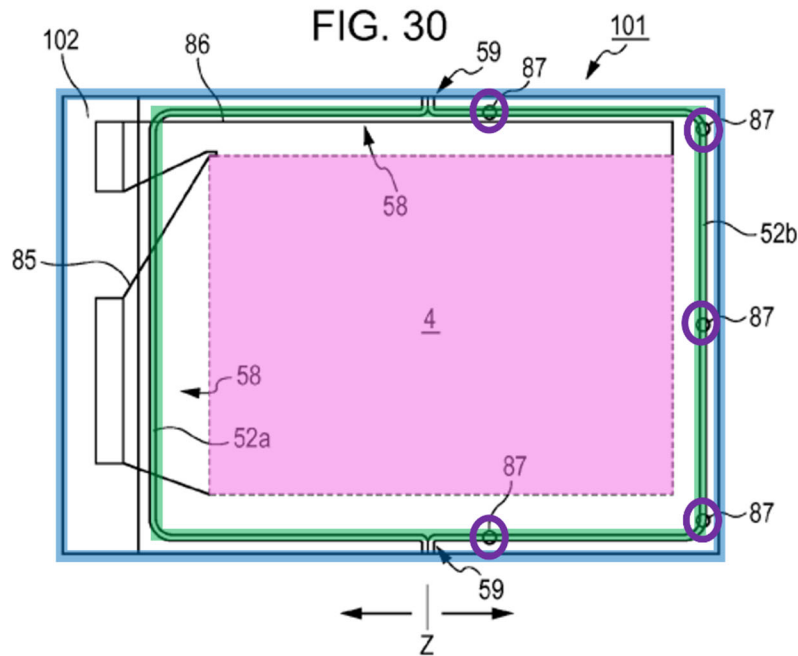
Id. at Fig. 14C. And the substrates are brought together and bonded to each other.

Id. at 26:29-27:24, 28:55-29:16.



Id. at Fig. 15C. The resulting device (formed from the first and second substrates) is unloaded from the load/unload unit. *Id.* at 27:25-37; *see id.* at 27:38-28:54. The '606 patent explains that this well-known method reduces leakage of liquid crystal and improves reliability. *Id.* at 29:17-25, 29:25-31:17; Decl. ¶ 70.

An exemplary liquid crystal device is shown in Figure 30:



'606 patent at Fig. 30, 38:26-67. The liquid crystal device includes TFT substrate 102, data relaying wires 85, gate relaying wires 86, ring-shaped portion 58 with conductive sealing member 52b and insulating sealing member 52a, image display region 4, and dot conductive portions 87. *Id.* at 38:26-67. "TFT substrate 102 is electrically connected to the counter substrate via the dot conductive portions 87." *Id.* at 37:67-38:3; Decl. ¶ 71.

B. Prosecution History

The application that led to the '606 patent was filed on December 16, 2014. Ex. 1002 at 1-208, 305. In response to an Office Action requiring the Applicant to "elect a single disclosed species," the Applicant elected the embodiment in Figure

30. *Id.* at 310-315, 317-327; Decl. ¶¶ 72-74.

The Examiner issued a number of Office Actions repeatedly rejecting the claims over U.S. Patent No. 6,930,745 (“*Miyazaki*,” Ex. 1010), and U.S. Patent Application Publ. No. 2005/0122466 (“*Tanaka*,” Ex. 1011). *Id.* at 331-343, 379-392, 432-449; Decl. ¶¶ 75-79. The Applicant amended the claims several times, including to add “plurality of dot conductive points.” Ex. 1002 at 359-373, 397-414. The Applicant argued *Miyazaki* and *Tanaka* failed to render obvious these features. *Id.* The Examiner disagreed.

After a second Examiner interview (*id.* at 454-455), the Applicant amended the claims to require the “seal member” be “formed continuously around the entire display region without the use of a plug.” *Id.* at 457-468. The Examiner allowed the claims. *Id.* at 480-489; Decl. ¶ 80.

C. Claim Construction

Claims need to be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). No terms require construction because the claims encompass the prior-art mappings under any reasonable construction consistent with the *Phillips* standard. 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

IV. Level of Ordinary Skill

A person of ordinary skill in the art (“POSITA”) as of the earliest priority date of the ’606 patent would have had at least a Bachelor’s degree in electrical engineering, computer science, physics, or a similar field and at least two years of experience designing semiconductor display devices, including LCD displays. Additional relevant work experience can compensate for less education, and *vice versa*. For example, a Master’s degree in electrical engineering, computer science, physics, or a similar field can substitute for two years of experience designing semiconductor display devices, including LCD displays. Decl. ¶¶ 81-83.

V. Statement of Precise Relief Requested

Petitioner requests review and cancellation of claims 7-13 and 15-20 under the following grounds:

Ground	Claims	References	Statutory Basis
1	7-13, 20	<i>Fujikawa</i>	102
2	7-13, 15-20	<i>Fujikawa</i>	103
3	7-13, 15-20	<i>Fujikawa, Kang</i>	103

Ground	Claims	References	Statutory Basis
4	7-13, 15-20	<i>Fujikawa, Ikeguchi</i>	103
5	7-13, 15-20	<i>Fujikawa, Kang, Ikeguchi</i>	103

VI. *Fujikawa* Anticipates Claims 7-13 and 20 (Ground 1) and/or Renders Obvious Claims 7-13 and 15-20 (Ground 2)

A. Independent Claim 7

1. 7[pre]: “*A display device, comprising:*”³

To the extent the preamble is limiting, *Fujikawa* discloses it. Decl. ¶ 87.

Fujikawa “relates to an electrooptic device,” such as a liquid crystal device, for use in electronic devices. *Fujikawa*, [0002], [0004], [0010]-[0023]. *Fujikawa*’s liquid crystal device includes, among other things, a display region 10a comprising a plurality of pixels 100a. *E.g., id.* at [0046]-[0051], [0054]-[0058]. This liquid crystal device is a “***display device***,” as claimed. Decl. ¶ 87; *Fujikawa*, [0004], [0051] (display device 100).

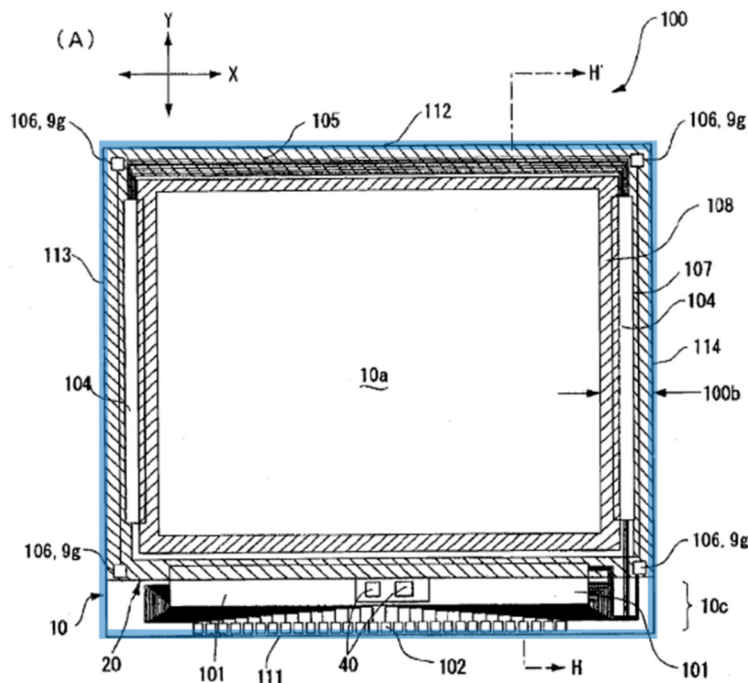
2. 7[a]: “*a first substrate including a pixel region and a seal region which is defined around the pixel region on a first*

³ Claim language is bold and italicized.

surface of the first substrate,”

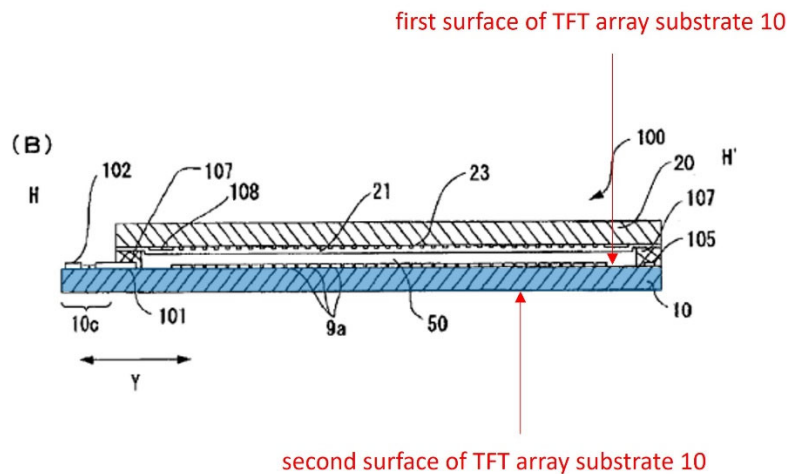
Fujikawa discloses this limitation. Decl. ¶¶ 88-92.

First, *Fujikawa* discloses its liquid crystal device (“*display device*”) includes
“TFT array substrate 10.” *Fujikawa*, [0046].



Id. at Fig. 1A. TFT array substrate 10 is the claimed “*first substrate*.” Decl. ¶ 89.

And as shown in Figure 1B, it includes a “*first surface*” (top) and second surface (bottom):



Fujikawa at Fig. 1B.

Second, *Fujikawa* discloses TFT array substrate 10 (“*first substrate*”) has a “*pixel region*.” Decl. ¶ 90. Specifically, *Fujikawa* discloses that disposed on TFT array substrate 10 is “a plurality of pixels formed in a matrix so as to constitute the image display region 10a.” *Fujikawa*, [0053]. The pixels 100a are arranged “in a matrix corresponding to the intersections of a plurality of data lines 6a extending in the Y-direction and a plurality of scanning lines 3a extending in the X-direction.” *Id.* at [0054].

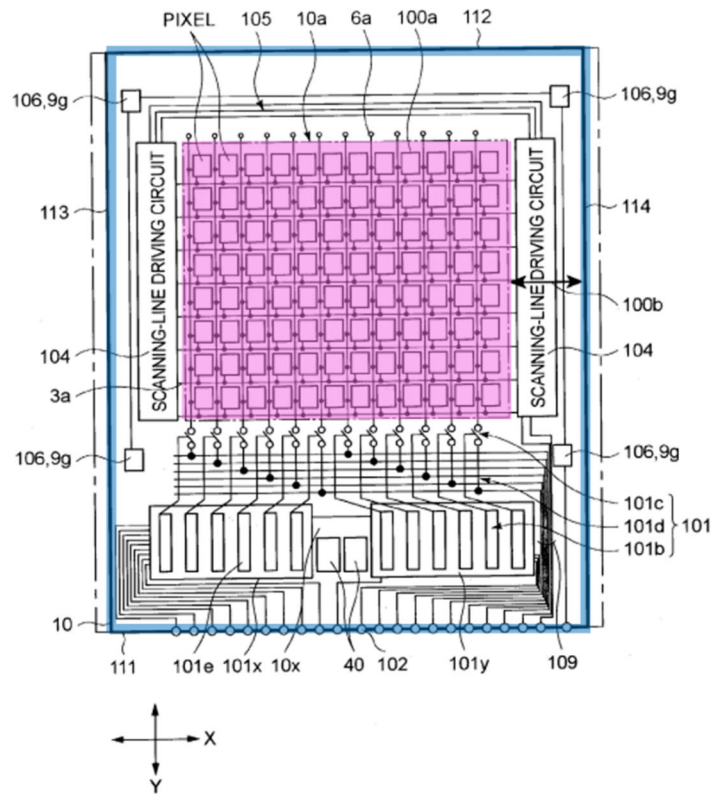
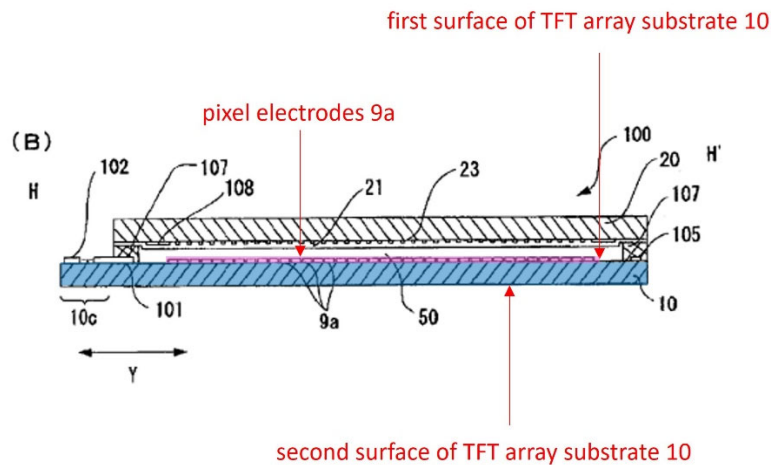


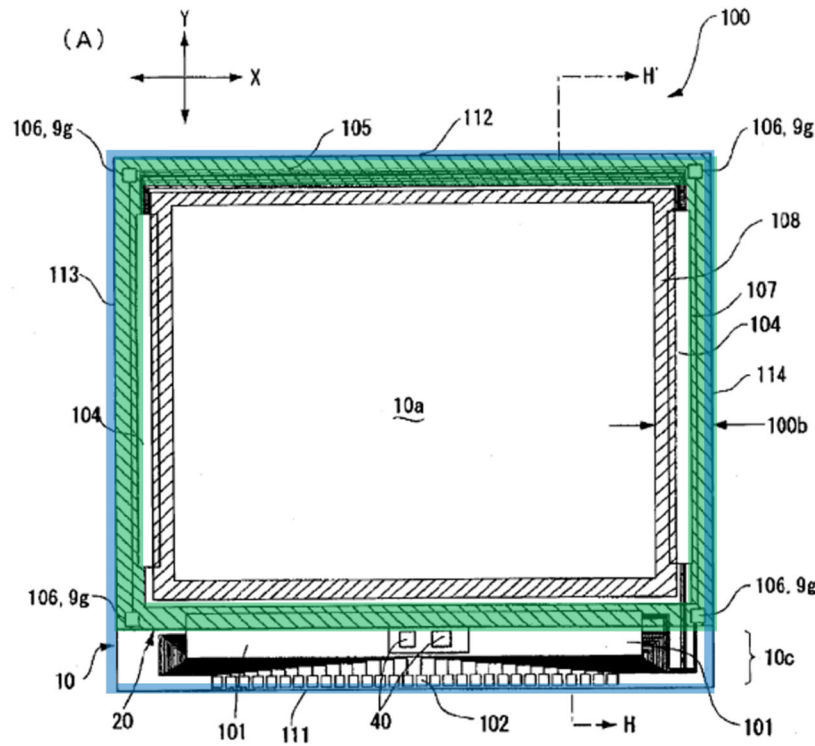
FIG.2

Id. at Fig. 2. Each pixel 100a includes “a pixel electrode 9a and a pixel-switching TFT 30 for controlling the pixel electrode 9a.” *Id.* at [0058], [0061]. The matrix of pixels constitutes the “*pixel region*.” Decl. ¶ 90. As shown in Figure 1B, the pixel region is on the first surface of TFT array substrate 10:



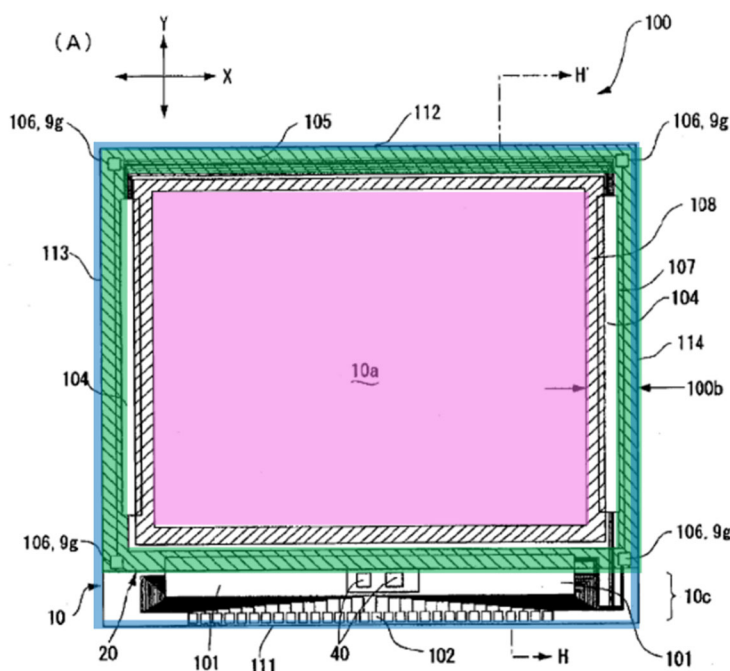
Fujikawa at Fig. 1B.

Finally, *Fujikawa* discloses “*a seal region.*” Decl. ¶ 91. *Fujikawa* discloses its liquid crystal device comprises TFT array substrate 10 and counter substrate 20. *Fujikawa*, [0046]. These two substrates are “bonded” together by sealing material 107, “formed on a TFT array substrate 10” “along the edge of a counter substrate 20.” *Id.* at [0046], [0049].

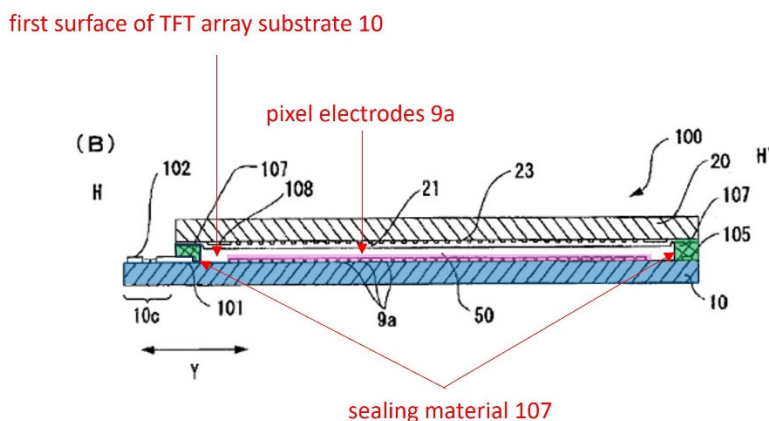


Id. at Fig. 1A. Sealing material 107 is in a “sealing region,” shown in Figure 1A comprising “an area shaded by downward-slanting lines.” *Id.* at [0046].

Moreover, this “seal region” is “defined around the pixel region on a first surface of the first substrate.” Fujikawa explains display area 10a comprises “a plurality of pixels.” *Id.* at [0053].



Id. at Fig. 1A. And as shown above in Figure 1A and below in Figure 1B, the seal region (green) is defined around the pixel region (pink), both of which are formed on the “***first surface of the first substrate.***” Decl. ¶ 92.



Fujikawa at Fig. 1B.

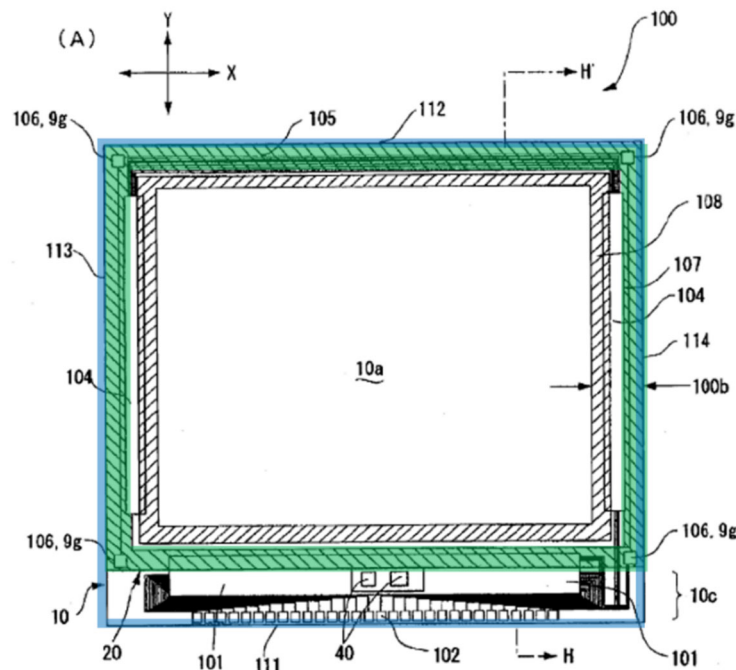
3. 7[b]: “the pixel region including a plurality of pixels and a plurality of active elements, and the seal region forming a

rectangular ring shape, wherein the active elements are thin film transistors disposed on the first substrate; and

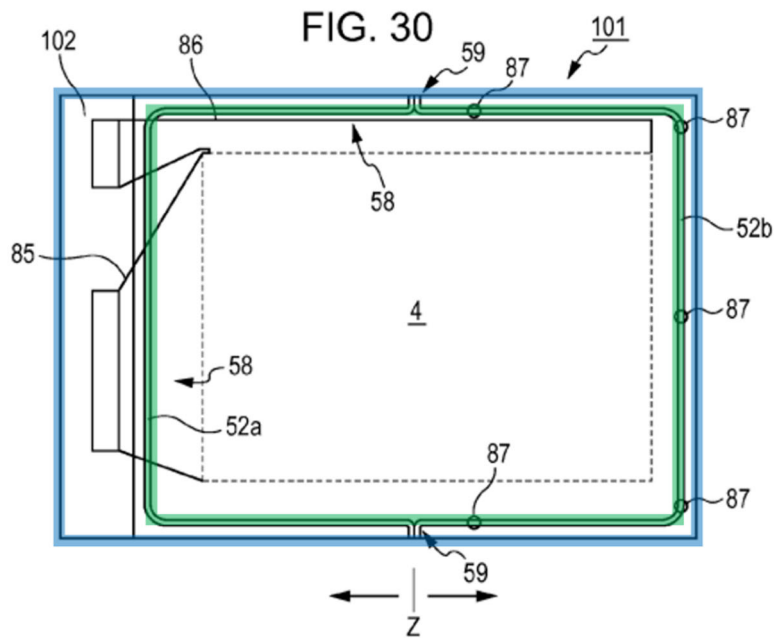
Fujikawa discloses this limitation. Decl. ¶¶ 93-95.

First, *Fujikawa* discloses its seal region “***form[s] a rectangular ring shape.***”

Id. ¶ 94. *Fujikawa* discloses sealing material 107 is formed “along the edge of a counter substrate 20” around image display region 10a. *Id.*; e.g., *Fujikawa*, [0046]. This is shown in Figure 1A, which depicts **sealing material 107** in the rectangular ring “area shaded by downward-slanting lines”:



Fujikawa at Fig. 1A; *id.* at [0046]. This is similar to the **seal region** in Figure 30 of the '606 patent:



'606 patent at Fig. 30; Decl. ¶ 94.

Second, *Fujikawa* discloses its “*pixel region including a plurality of pixels and a plurality of active elements . . . wherein the active elements are thin film transistors disposed on the first substrate.*” Decl. ¶ 95. Image display region 10a (“*pixel region*”) comprises “a plurality of pixels formed in a matrix” on TFT array substrate 10 (“*first substrate*”). *Fujikawa*, [0053].

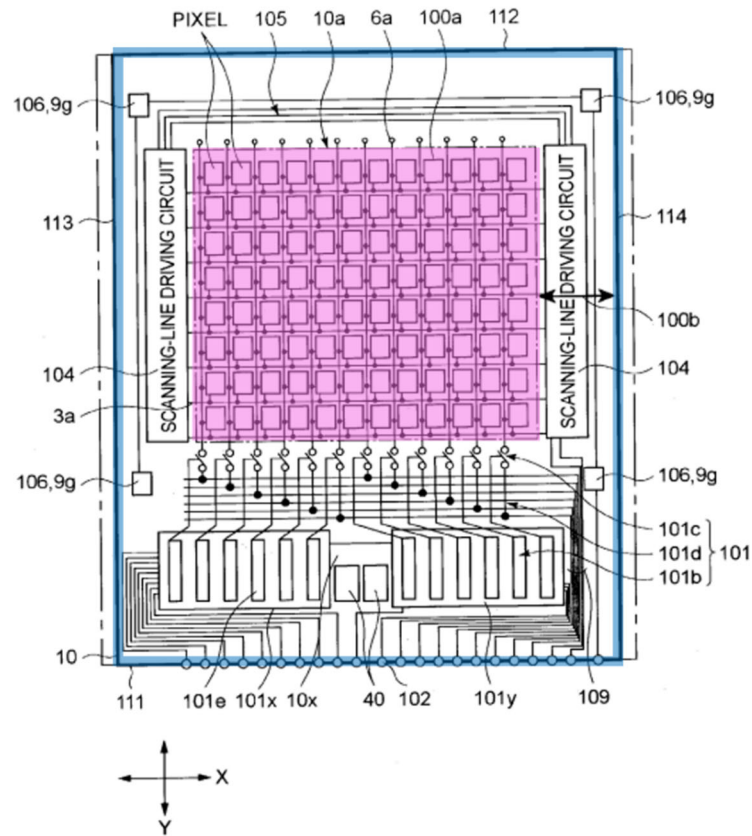


FIG.2

Id. at Fig. 2. Each pixel includes “a pixel electrode 9a and a pixel-switching TFT 30.” *Id.* at [0058], [0061]; Decl. ¶ 95.

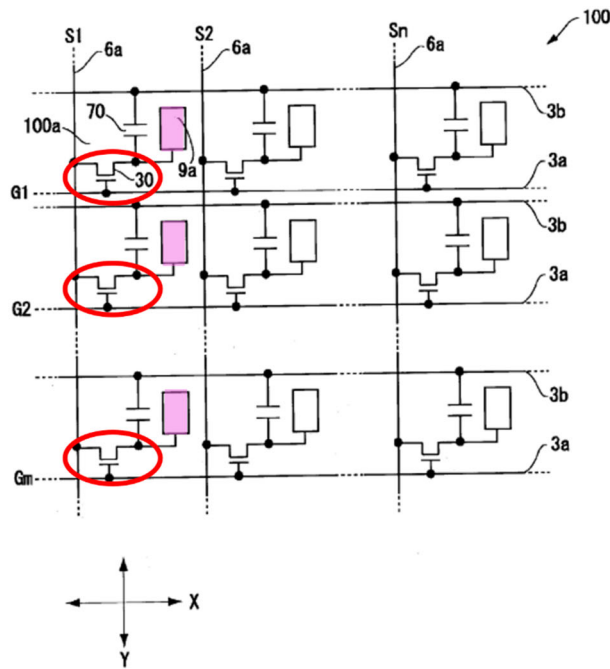
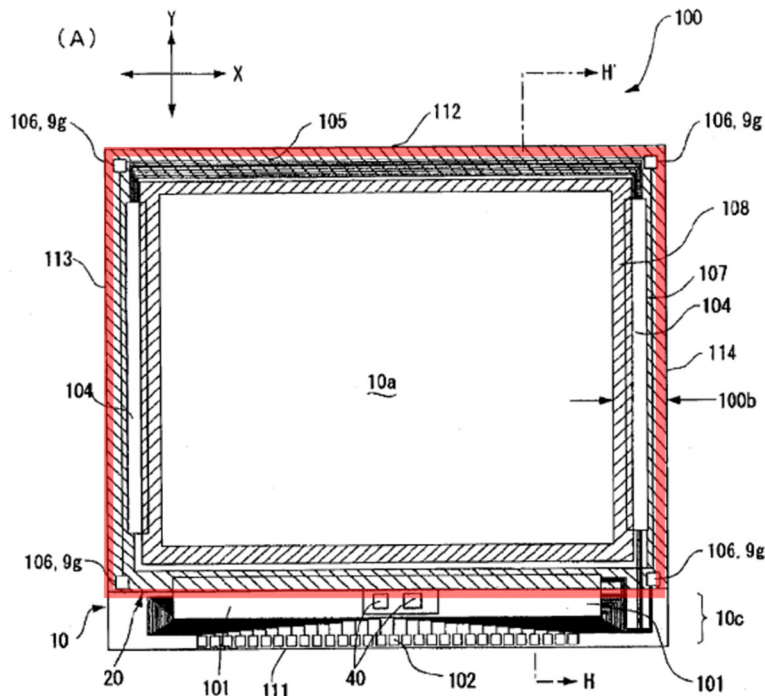


FIG.4

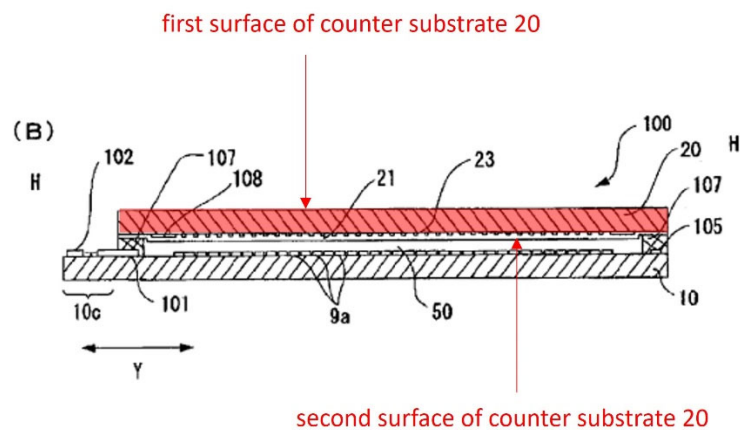
Fujikawa at Fig. 4, [0050], [0053], [0058].

4. 7[c]: “a second substrate including a common electrode on a second surface; and”

Fujikawa discloses this limitation. Decl. ¶¶ 96-97. *Fujikawa* discloses a TFT array substrate 10 (“first substrate”) “bonded” to counter substrate 20 “by the sealing material 107.” *Fujikawa*, [0046], [0049]. Counter substrate 20 is the “second substrate”:

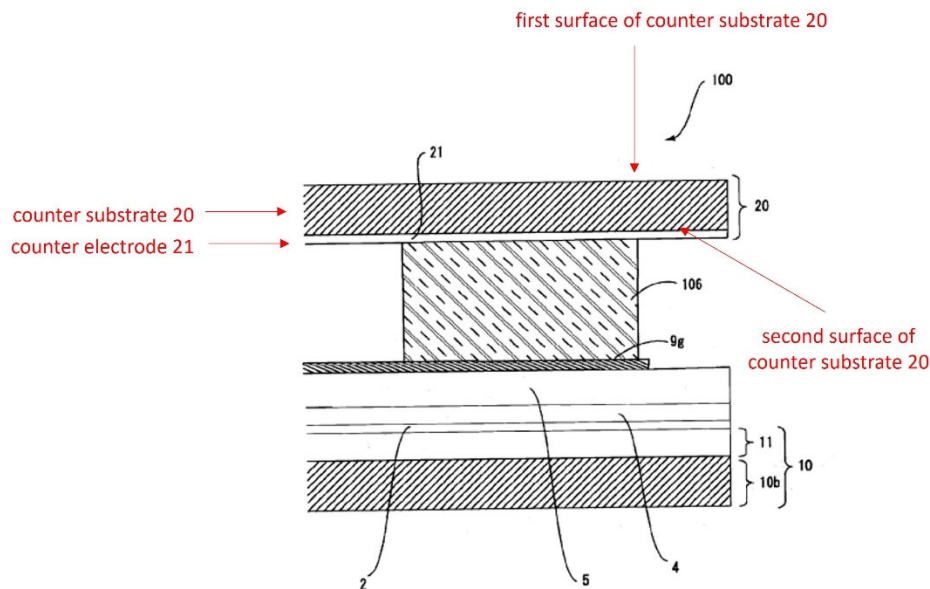


Id. at Fig. 1A; Decl. ¶ 97. **Counter substrate 20** includes a first surface (top) and “*second surface*” (bottom):



Fujikawa at Fig. 1B. Disposed on “counter substrate 20” are “counter electrodes 21.” *Id.* at [0050], [0058], [0079]. A POSITA would have understood that counter electrodes 21 are the claimed “*common electrode*” because a “constant voltage [is]

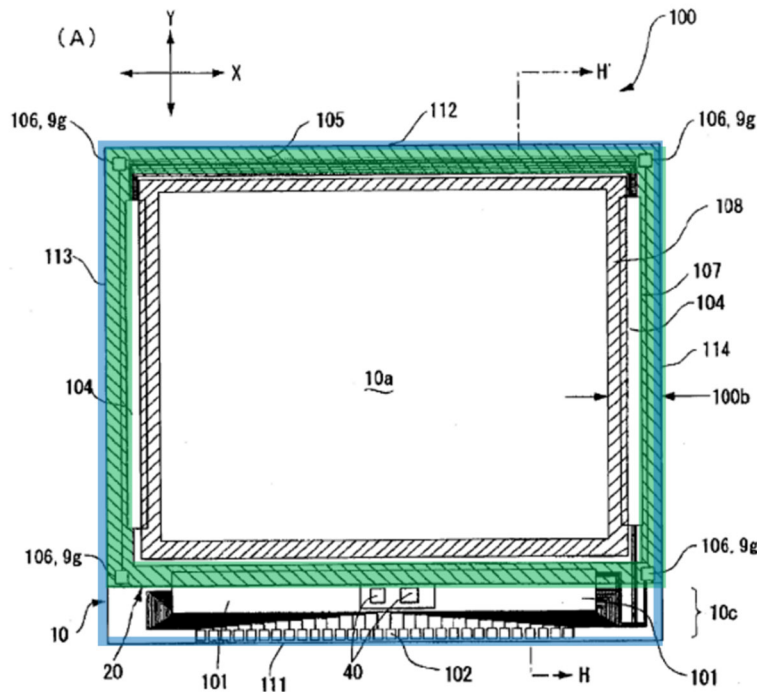
supplied to the counter electrodes of the counter substrate 20” (*id.* at [0008]), and as shown in Figures 1B (above) and 9 (below), they are on the “*second surface*” of counter substrate 20:



Id. at Fig. 9; Decl. ¶ 97.

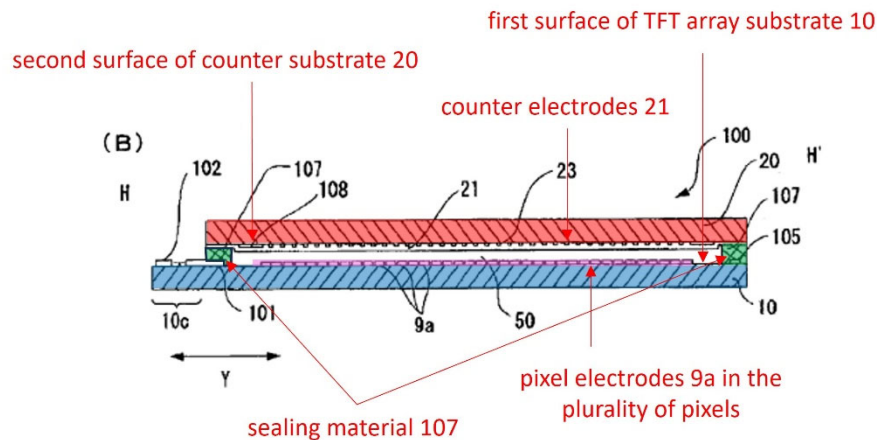
5. 7[d]: “a seal member bonding the first substrate and the second substrate so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels,”

Fujikawa discloses this limitation. Decl. ¶¶ 98-100. *Fujikawa* discloses TFT array substrate 10 and counter substrate 20 “bonded” together by sealing material 107. *Fujikawa*, [0046], [0004].



Id. at Fig. 1A. Sealing material 107 is “formed on a TFT array substrate 10” and “along the edge of a counter substrate 20.” *Id.* at [0046]. It “can be an adhesive made of a photosetting or thermosetting resin for bonding” and “mixed with a gap material, such as glass fibers or glass beads.” *Id.* at [0049]. Sealing member 107 is a “*seal member bonding the first substrate and the second substrate.*” Decl. ¶ 99.

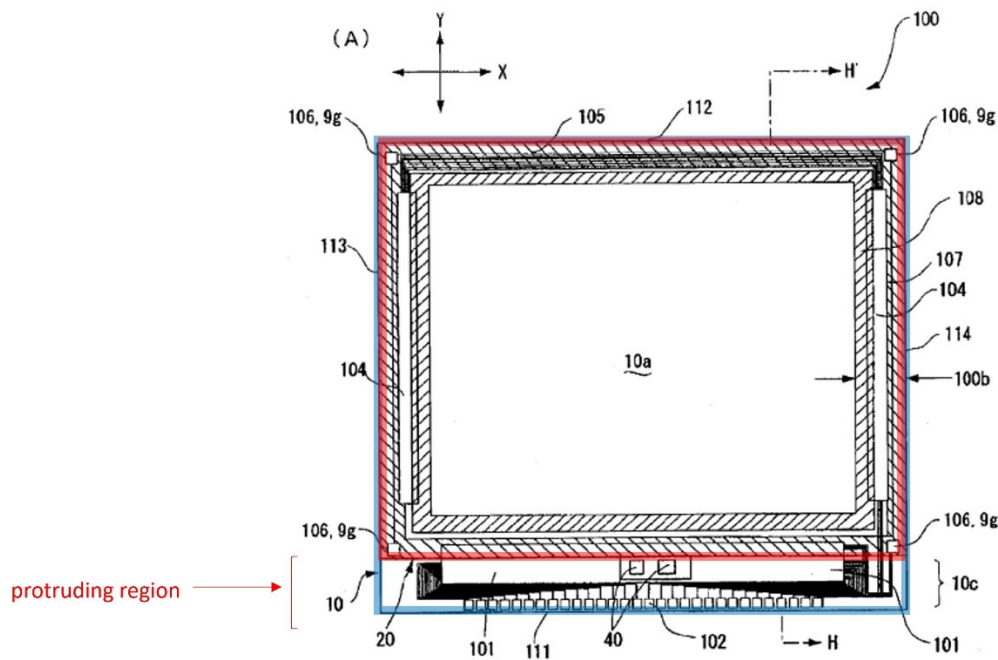
Moreover, sealing member 107 bonds the TFT array substrate 10 and counter substrate 20 “*so that the first surface faces the second surface and the common electrode is disposed opposite to the plurality of pixels.*” Decl. ¶ 100.



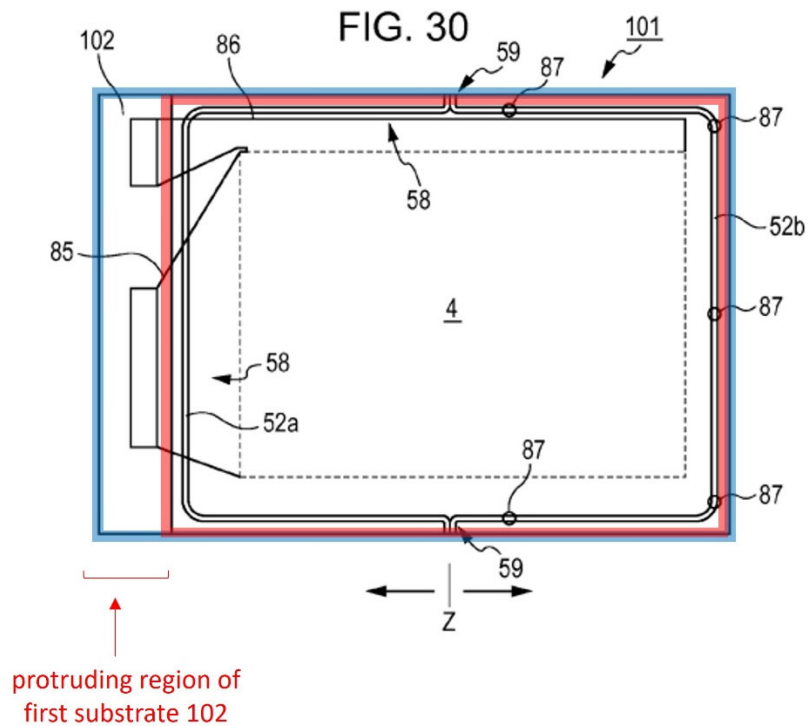
Fujikawa at Fig. 1B. As shown, the first surface (top) of the TFT array substrate 10 is facing the second surface (bottom) of counter substrate 20. Decl. ¶ 100. And, in this arrangement, counter electrodes 21 are disposed opposite a plurality of pixels. *Id.*

6. 7[e]: “wherein the first substrate includes a protruding region which protrudes over the second substrate in a plan-view of the first substrate,”

Fujikawa discloses this limitation. Decl. ¶¶ 101-102. Figure 1A of *Fujikawa* is a “plan view” “from the side of the counter substrate”:



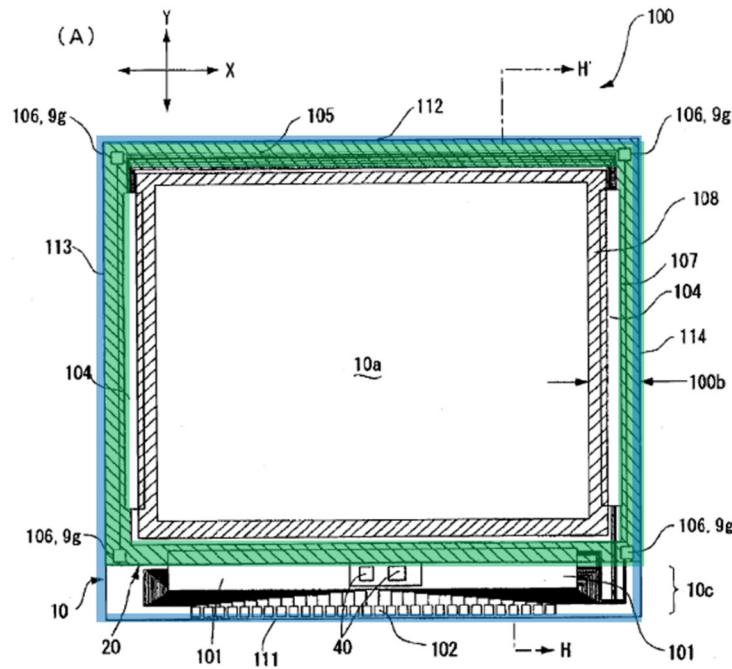
Fujikawa at Fig. 1A, [0045]. In this plan view, TFT array substrate 10 extends beyond counter substrate 20 to include a “*protruding region*.” Decl. ¶ 102. Indeed, region 10c is the “extended portion of the TFT array substrate 10 that *protrudes* from the edge of the counter substrate 20.” *Fujikawa*, [0009] (emphasis added); *id.* at [0046]. This is similar to the protruding region in Figure 30 of the ’606 patent:



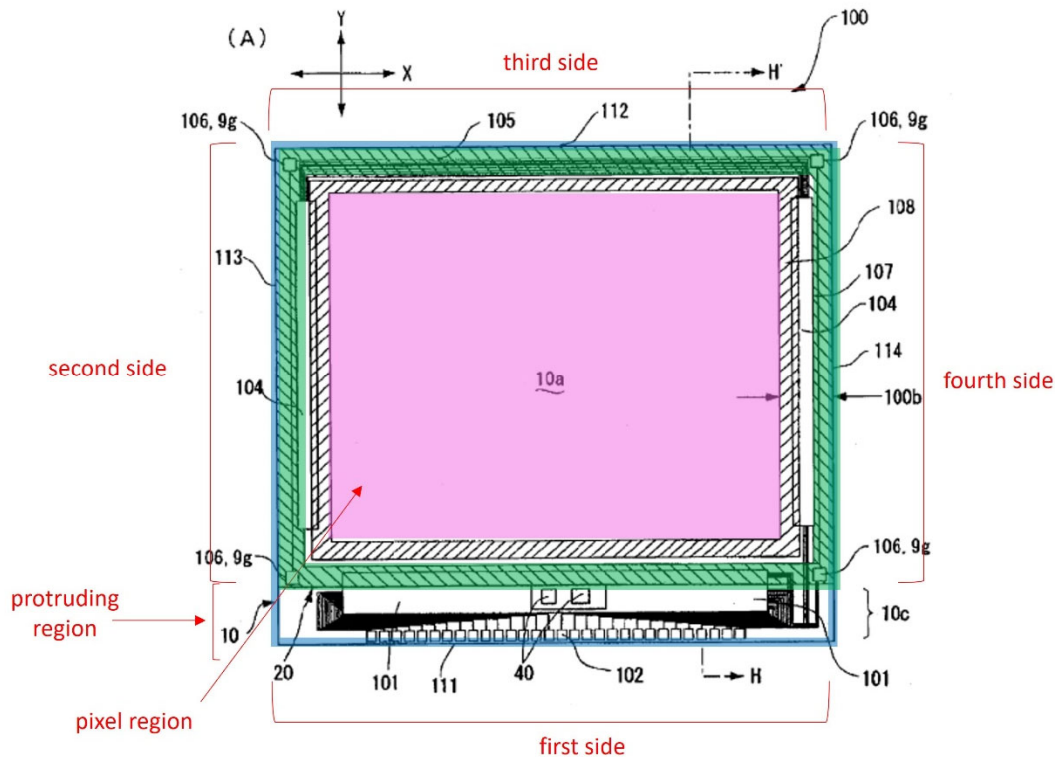
'606 patent at Fig. 30; Decl. ¶ 102.

7. 7[f]: “the seal region includes a first side, a second side, a third side and a fourth side, the first side is positioned between the pixel region and the protruding region, and opposed to the third side, and the second side is opposed to the fourth side,”

Fujikawa discloses this limitation. Decl. ¶¶ 103-104. The area that contains sealing material 107 comprises a rectangular ring shape. Section VI.A.3.



Fujikawa at Fig. 1A. As *Fujikawa* explains that the TFT array substrate 10 has four “substrate edge[s],” (*id.* at [0046]), so too does the rectangular ring shaped seal area have four sides. Decl. ¶ 104. And as shown below, the “*first side*” of the seal area is between the protruding region of the first substrate (Section VI.A.6) and the pixel region (Section VI.A.2):

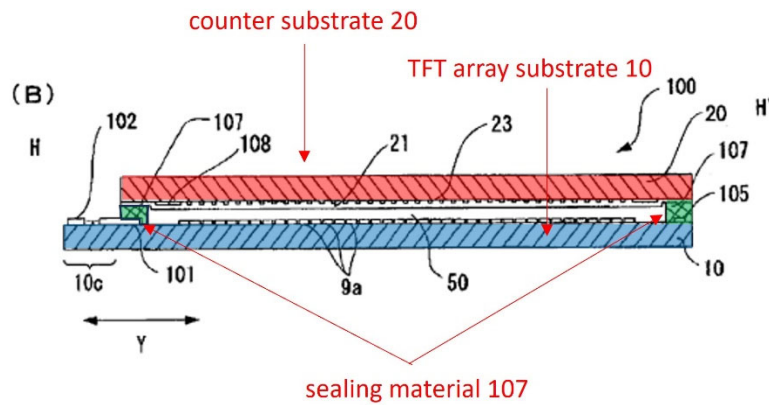


Id. at Fig. 1A; Decl. ¶ 104. The “**third side**” of the seal area is opposed from the “**first side**,” and the “**second side**” of the seal area is opposed the “**fourth side**.”

Decl. ¶ 104.

8. 7[g]: “the seal member is disposed between the first substrate and the second substrate”

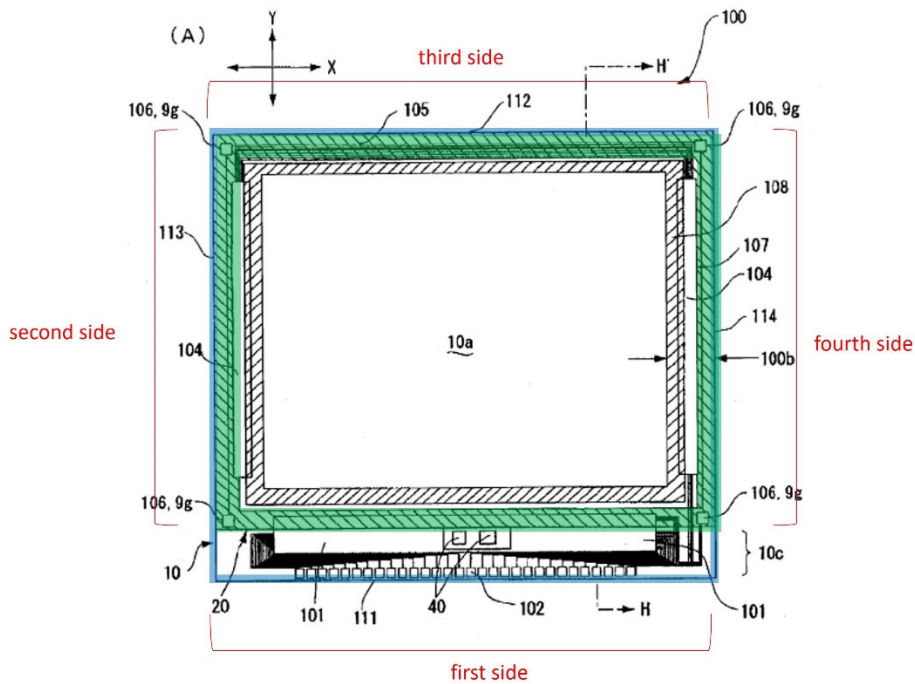
Fujikawa discloses this limitation. Decl. ¶¶ 105-106. **Sealing material 107** (“*seal member*”) is “formed on a **TFT array substrate 10** . . . along the edge of a **counter substrate**.” *Fujikawa*, [0046], [0049]. **Sealing material 107** is sandwiched between these substrates, “*disposed between*” the two:



Id. at Fig. 1B; Decl. ¶ 106.

9. 7[h]: “and positioned on the first side, the second side, the third side and the fourth side continuously, forms a closed-ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate, and is formed continuously around the entire pixel region without the use of a plug,”

Fujikawa discloses this limitation. Decl. ¶¶ 107-111. *Fujikawa* discloses sealing material 107 (“*seal member*”) fills the “area shaded by downward-slanting lines” in the plan view of Figure 1A:

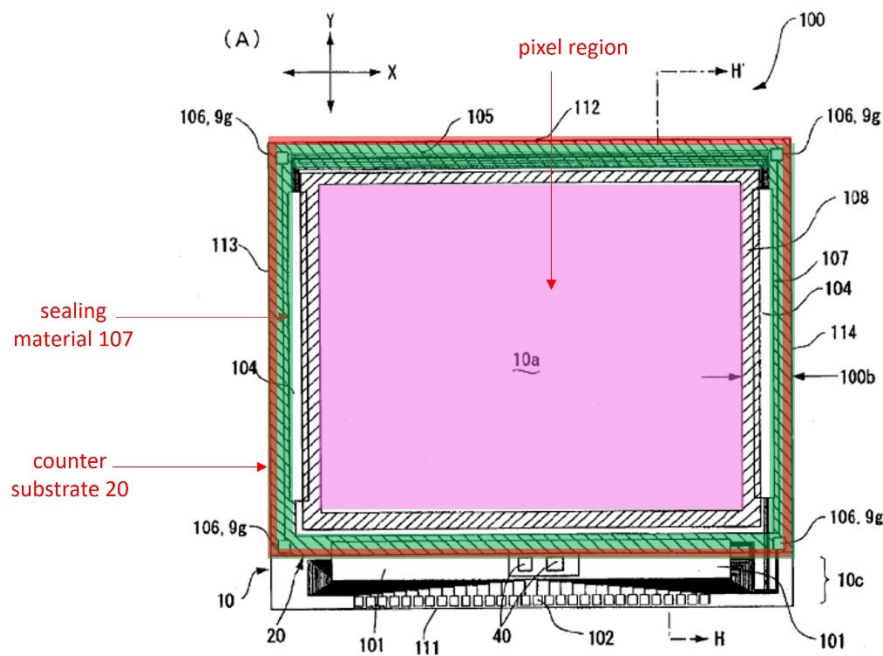


Fujikawa at Fig. 1A; *id.* at [0046], [0049]. As shown above, **sealing material 107** is positioned on all four sides of the “*seal region*.” Decl. ¶ 108.

A POSITA would have understood, looking at this plan view in *Fujikawa*, that the **sealing material 107** is positioned “*continuously*” in a “*closed-ring shape*” along those four sides “*around the entire pixel region without the use of a plug.*” *Id.* ¶ 109; Section VI.A.3; Ex. 1009 at Figs. 7-8, 18:36-44 (explaining in a similar design “sealant 52 is formed in the shape of a frame which is closed in a region within the substrate surface, does not include a liquid crystal inlet”); Ex. 1012 at Figs. 9-10, 23:12-21 (same); *Ikeguchi* at [0027]-[0029]. Indeed, **sealing material 107** fills the entire rectangular ring-shaped area shaded by the downward-slanting lines that represent the “*seal region*” in Figure 1A. *Fujikawa*, [0046], [0049], Fig.

1A. If a gap was contemplated, or a plug required, the plan view would expressly reflect as much. Decl. ¶¶ 109-110; *Miyazaki*, Fig. 1 (gap in seal where plug used); *Tanaka*, Figs. 1, 3 (same).

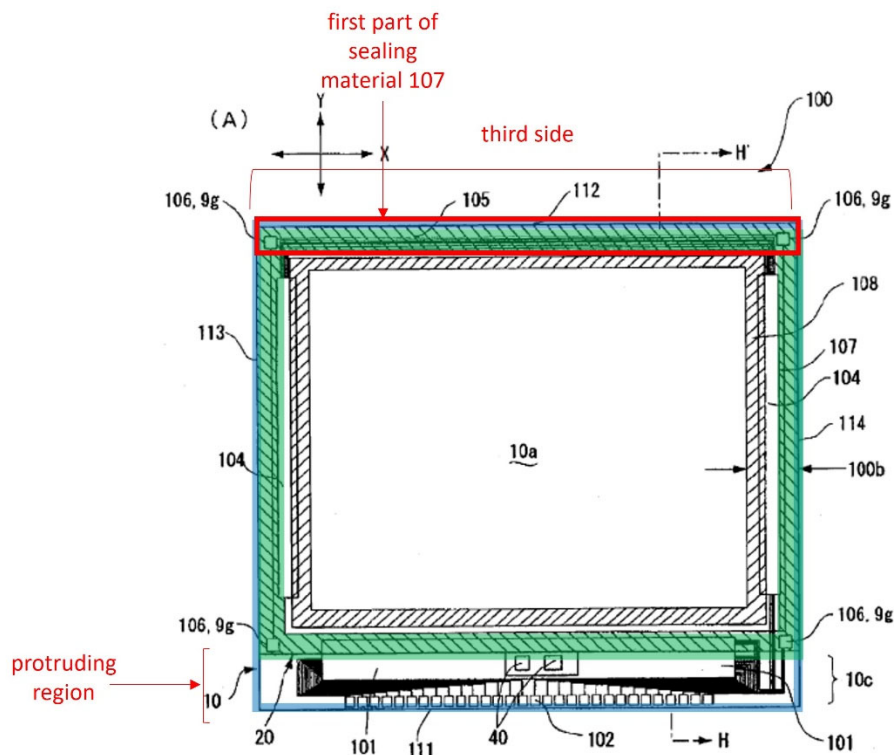
Moreover, *Fujikawa* discloses the [sealing material 107](#) “*forms a closed ring shape in which the pixel region is positioned without protruding from the second substrate in the plan-view of the first substrate*”:



Fujikawa at Fig. 1A. Image display area 10a (“*pixel region*”) is “*positioned*” in sealing material 107 (“*seal member*”) and does not “*protrud[e] from the second substrate in the plan-view.*” Decl. ¶ 111.

10. 7[i]: “a first part of the seal member disposed on the third side which is opposed to the protruding region with respect to the pixel region includes a plurality of conductive particles,”

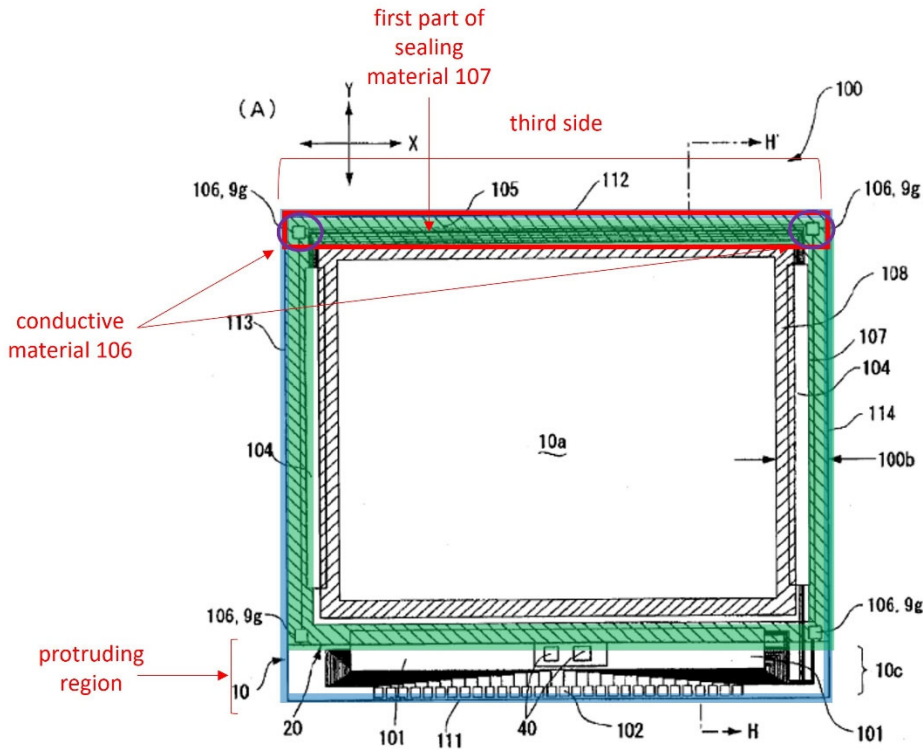
Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 112-115. *Fujikawa* discloses “a first part of the seal member disposed on the third side[,] which is opposed to the protruding side with respect to the pixel region.” Decl. ¶ 113. As discussed for limitations 7[f] and 7[h] (Sections VI.A.7, VI.A.9), *Fujikawa* discloses a third side of a seal region opposite the protruding region of TFT array substrate 10 relative to image display region 10a (“*pixel region*”) that comprises sealing material 107 (“*seal member*”):



Fujikawa at Fig. 1A. The “*first part*” of sealing material 107 along the third side of

the seal region extends from edge 113 to edge 114 of TFT array substrate 10. Decl. ¶ 113.

Fujikawa discloses or at least renders obvious the “***first part***” of that seal member “***includes a plurality of conductive particles.***” Decl. ¶ 114. Within sealing member 107 are “conductive materials 106 corresponding to the four corners of the counter substrate 20.” *Fujikawa*, [0047]. The conductive materials 106 electrically connect conductive electrodes 9g to counter electrodes 21 on counter substrate 20. *Id.* at [0079]. “Conductive material 106 can be made of an epoxy resin adhesive component mixed with conductive particles such as silver powder and gold-plated fiber.” *Id.* The conductive particles in conductive material 106 are the “***conductive particles***” in the claim. Decl. ¶ 114. As shown below, there are “***a plurality***” of conductive materials 106, comprising a plurality of conductive particles, in the “***first part***” of the sealing material 107:

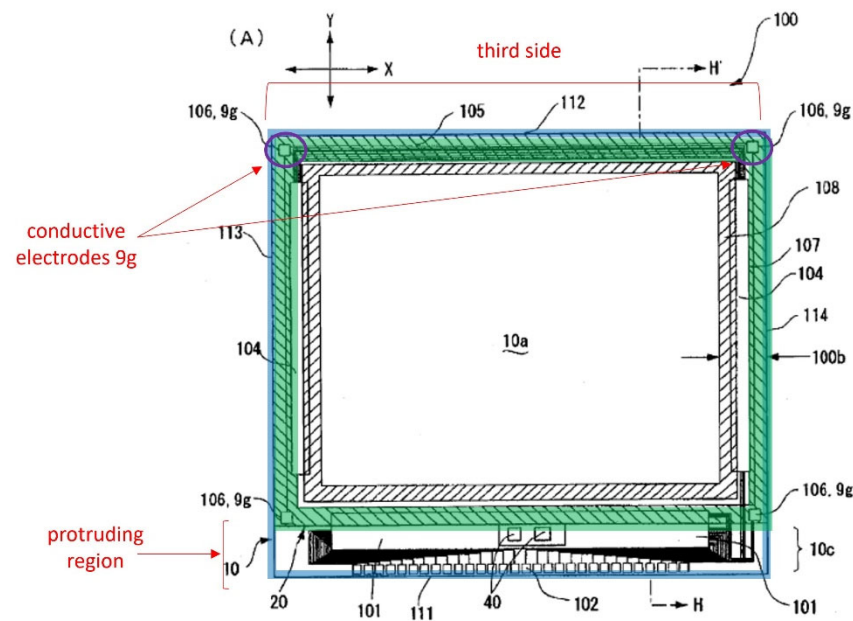


Fujikawa at Fig. 1A; Decl. ¶ 114. To the extent additional conductive particles are required, it would have been obvious to include more, for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 115. A POSITA would have been motivated to have additional conductive materials 106 with the corresponding plurality of conductive particles therein in the first part of the seal member to improve connectivity between the first and second substrates by virtue of connecting the conductive electrodes 9g to counter electrodes 21 (if additional conductive electrodes 9g are required, Section VI.A.11). Decl. ¶ 115. A POSITA would have understood that having more points of electrical contact would retain a stable voltage across the

common electrode and reduce impedance. *Id.* And a POSITA would have had a reasonable expectation of success in implementing such a design in *Fujikawa*. *Id.*

11. 7[j]: “a plurality of dot conductive points are disposed on the third side of the first substrate, all of the plurality of the dot conductive points are electrically connected to the common electrode, and”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 116-118. *Fujikawa* discloses conductive electrodes 9g “formed in the region of the TFT array substrate 10 overlapping with the counter substrate 20.” *Fujikawa*, [0079], [0047]; Decl. ¶ 117. The conductive electrodes 9g on the “third side” of the TFT array substrate are annotated below:



Fujikawa at Fig. 1A. Conductive electrodes 9g are the claimed “dot conductive points.” Decl. ¶ 117; ’606 patent at 38:46-52. *Fujikawa* explains these conductive

electrodes 9g are “electrically connected to the counter electrodes 21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates.”

Fujikawa, [0079].

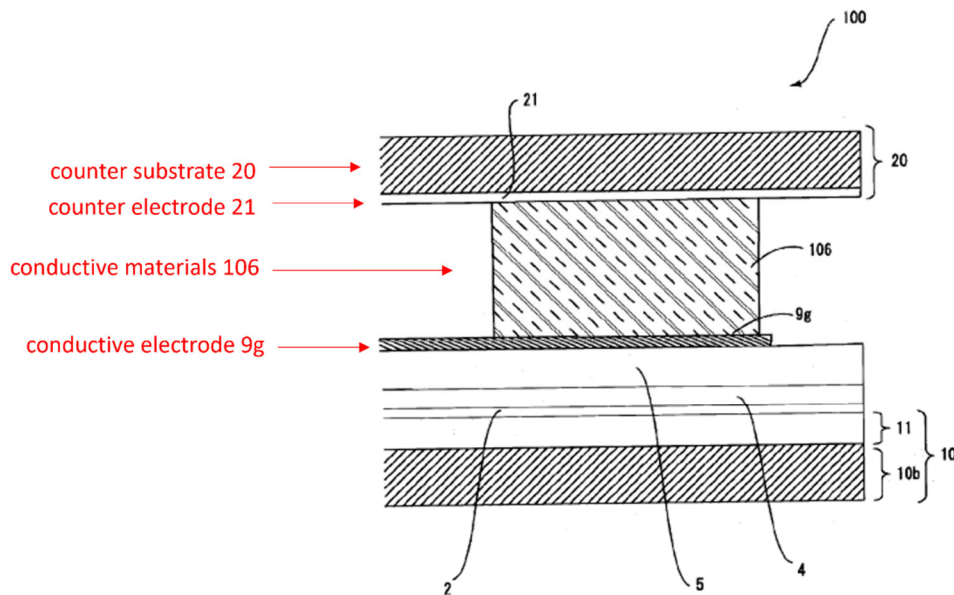


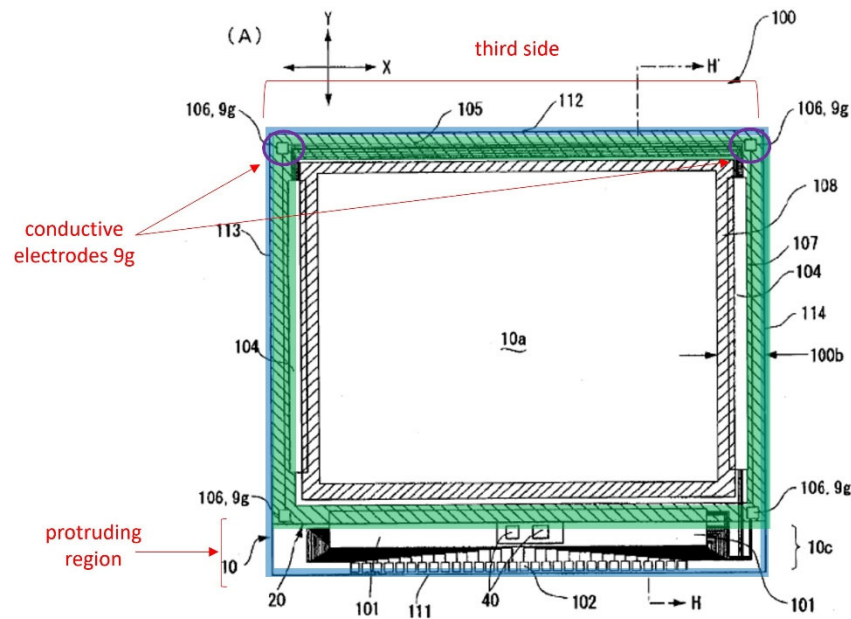
FIG.9

Id. at Fig. 9. *Fujikawa* discloses “a plurality of dot conductive points . . . disposed on the third side of the first substrate” and “electrically connected to the common electrode.” Decl. ¶ 117. To the extent additional conductive points are required, it would have been obvious to include more, for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 118. A POSITA would have been motivated to include additional conductive points on the third side to improve the electrical connectivity between

the first and second substrates. Decl. ¶ 118. A POSITA would have understood having more points of electrical contact would retain a stable voltage across the common electrode and reduce impedance. *Id.* And a POSITA would have had a reasonable expectation of success in doing so. *Id.*

12. 7[k]: “each of the plurality of the dot conductive points are spaced part from each other,”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 119-120. *Fujikawa* discloses or at least renders obvious a plurality of **conductive electrodes 9g** (“*plurality of dot conductive points*”), and as shown below, they are “*spaced apart from each other*”:



Fujikawa at Fig. 1A.

13. 7[l]: “wherein the first substrate includes a plurality of wiring lines that connect to the plurality of active elements, and the

plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points.”

Fujikawa discloses this limitation. Decl. ¶¶ 121-122.

Fujikawa discloses “terminals 102” formed “along a substrate edge 111 of the TFT array substrate 10.” *Fujikawa*, [0055]. “A plurality of lines 109 . . . are routed from these terminals 102” on the first substrate (*id.*) and provide signals to the data line driving circuit 101 (*see, e.g., id.* at [0007]). *Fujikawa* explains that the “data line driving circuit 101 is [also] formed along a substrate edge 111 so as to overlap with a part of the s[e]aling material 107.” *Fujikawa*, [0046]. This data line driving circuit 101 includes “shift register circuits 101b, sample hold circuits 101c, . . . [and] image signal lines 101d.” *Id.* at [0056]-[0057]. *Fujikawa* explains sample hold circuits 101c are “in a one-to-one correspondence with the data lines 6a.” *Id.* at [0057]. To that end, *Fujikawa* discloses a “plurality of data lines 6a” on TFT array substrate 10 (“*first substrate*”) that are “electrically connected to a source of the TFT 30” (“*active element*”) to supply the “pixel signal.” *Id.* at [0054]. This is shown below in Figure 4:

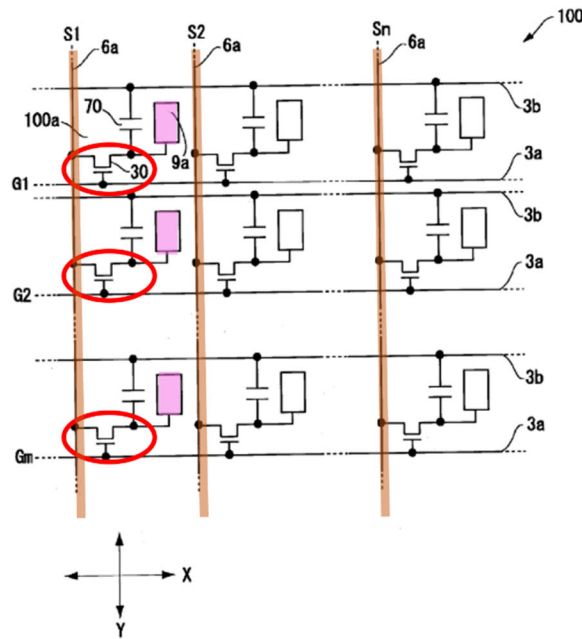


FIG. 4

Id. at Fig. 4. *Fujikawa* thus discloses “***the first substrate includes a plurality of wiring lines that connect to the plurality of active elements.***” Each wiring line in *Fujikawa* comprises three line segments, i.e., **data line 6a**, **image signal line 101d**, and **line 109**. Decl. ¶ 122. The wiring lines may be enabled or disabled depending on control signals provided to **shift registers 101b**. *Id.* When a **shift register 101b** outputs an enabling signal, the corresponding **hold circuit 101c** (a switch) is closed; and as a result, the corresponding **data line 6a**, **signal line 101d**, and **line 109** are all directly connected so data signals on the corresponding terminal 102 are provided directly to the corresponding pixel electrodes in the display region. *Id.* Further,

Fujikawa discloses these lines (as shown in Figure 2) “***extend onto the protruding region across the seal member without connecting to the dot conductive points***”:

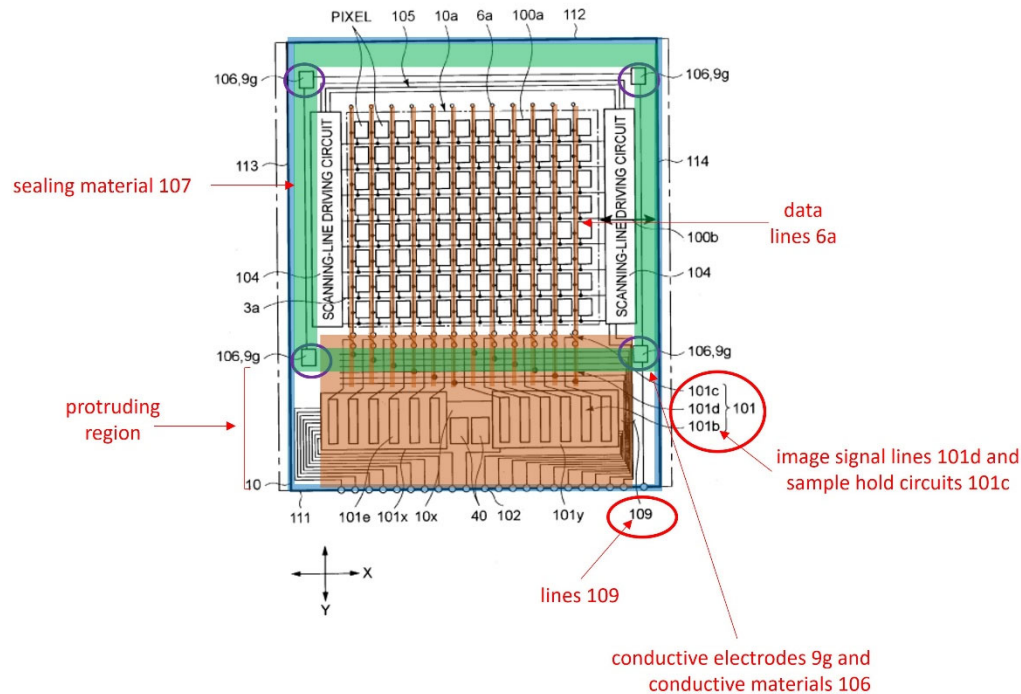


FIG.2

Fujikawa at Fig. 2; Decl. ¶ 122. A POSITA would have understood these lines would extend from the pixel display region across the sealing member to provide “pixel signals” to pixel electrodes in the display region without connecting to the dot conductive points. Decl. ¶ 122.

B. Claim 8

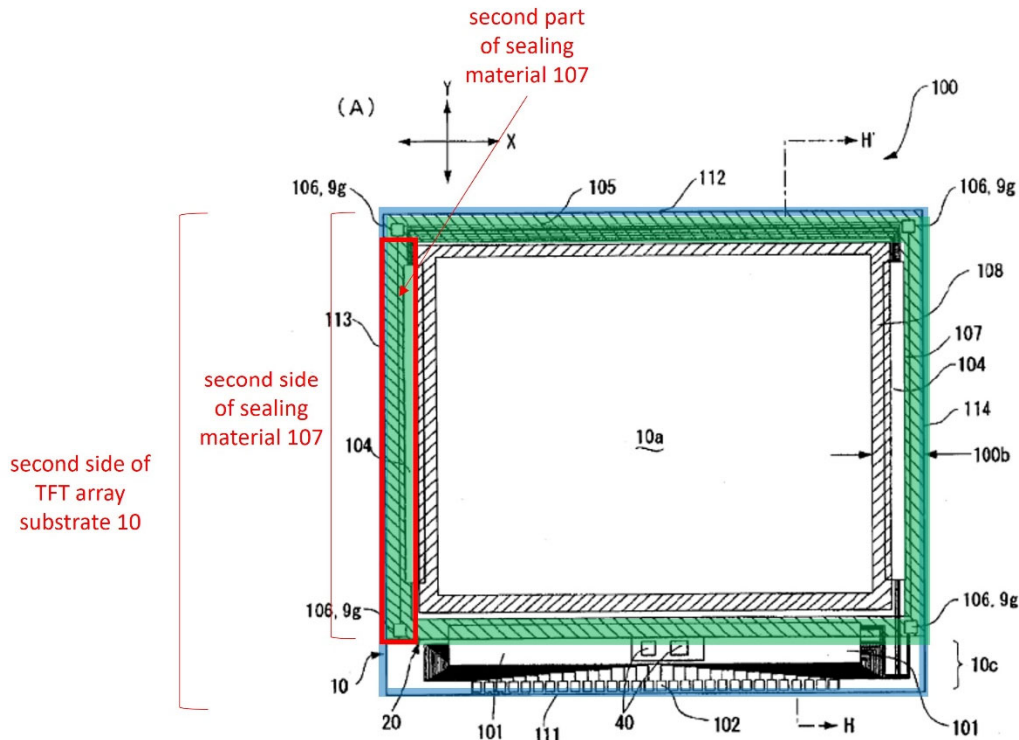
1. 8[pre]: “*The display device, according to claim 7,*”

Fujikawa discloses or renders obvious claim 7. Section VI.A; Decl. ¶¶ 87-123.

2. 8[a]: “*wherein the first substrate includes a first conductive point on the second side and the seal member includes a second part of the seal member on the second side,*”

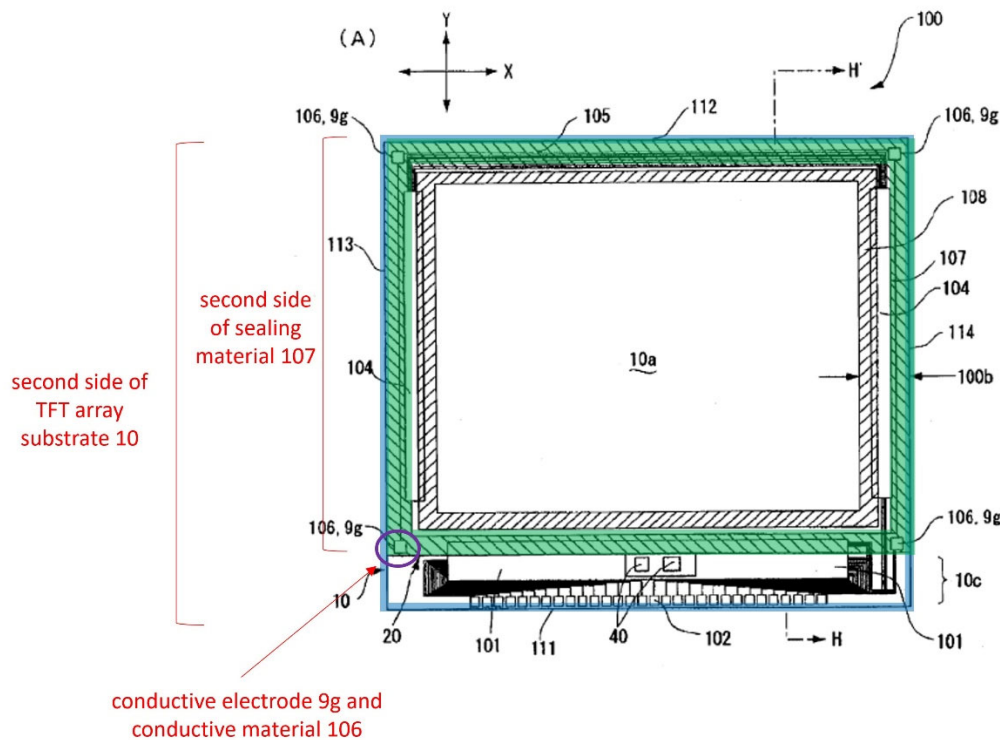
Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 124-

126. First, *Fujikawa* discloses a “*second side*” of the “*first substrate*”:



Fujikawa at Fig. 1A; Decl. ¶ 125. *Fujikawa* also discloses a “*second part of the seal member on the second side,*” as shown. Decl. ¶ 125.

Second, *Fujikawa* discloses or at least renders a first conductive point on the second side of the first substrate. See Sections VI.A.10-VI.A.12; Decl. ¶ 126. For example, *Fujikawa* discloses **conductive electrode 9g and conductive material 106** at the bottom left corner of **TFT array substrate 10**. Decl. ¶ 126.



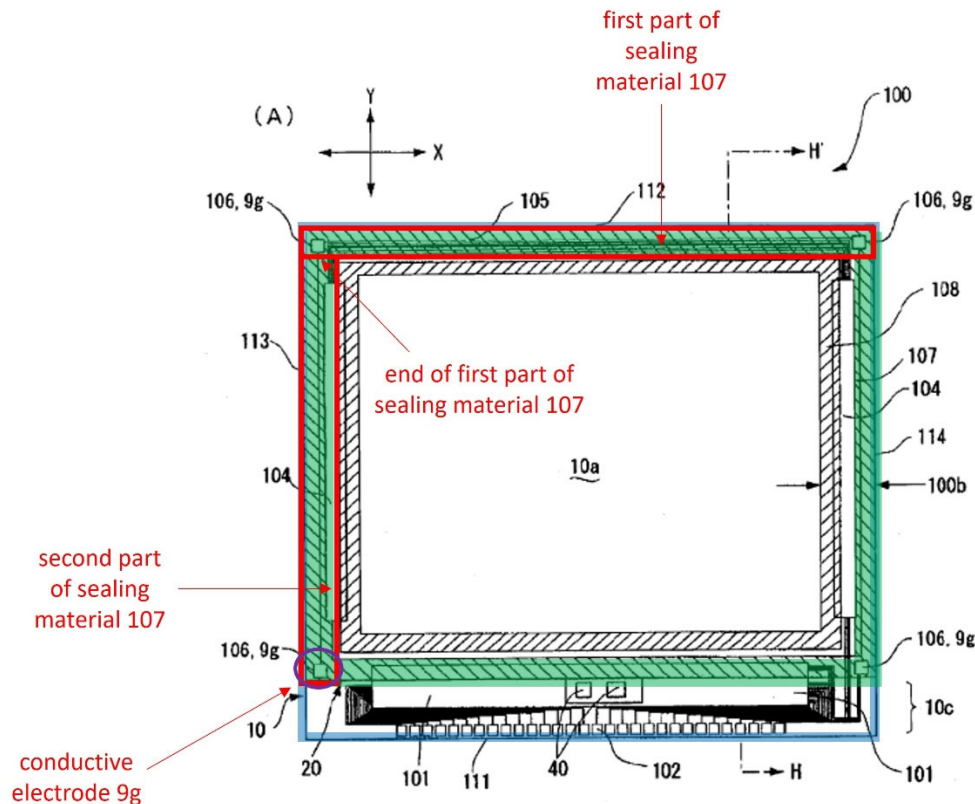
Fujikawa, Fig. 1A. This **conductive electrode 9g** is the claimed “*first conductive point*” on a second side of the first substrate. Decl. ¶ 126. It would have also been obvious to include a conductive point along the second side of the first substrate for *Fujikawa* discloses that the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 126; Sections VI.A.10-VI.A.12.

3. 8[b]: “*the second part of the seal member extends from one end of the first part of the seal member over the first conductive point on the second side, and the second part of the seal member includes a plurality of conductive particles, and*”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 127-

129.

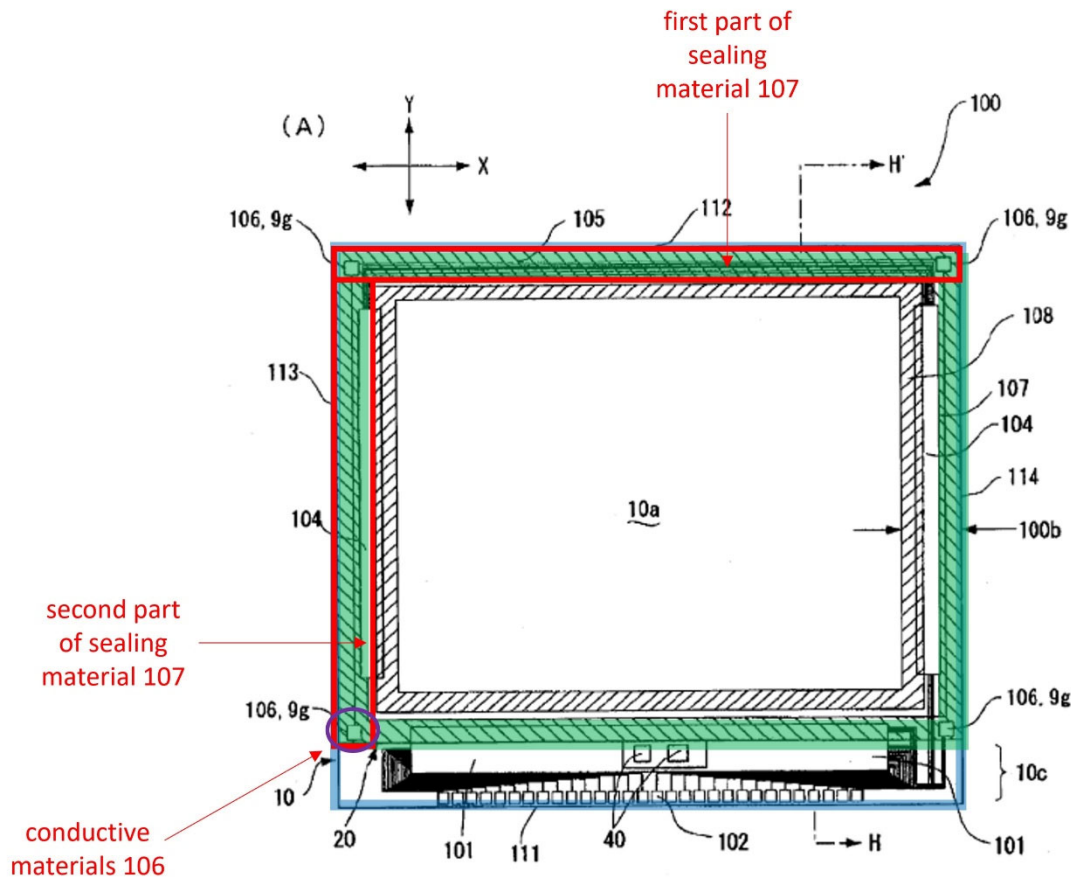
First, as discussed for limitation 8[a], *Fujikawa* discloses a “*second part*” of the “*seal member*” (sealing material 107). Section VI.B.2; Decl. ¶ 128. And as discussed for limitation 7[i], it also discloses a “*first part*” of the “*seal member*” (sealing material 107). Section VI.A.10; Decl. ¶ 128. As shown, the “*second part*” of the “*seal member extends from one end of the first part of the seal member over the first conductive point on the second side*”:



Fujikawa at Fig. 1A.

Second, *Fujikawa* discloses or at least renders obvious a plurality of conductive particles in the second part of the seal member. Sections VI.A.10-

VI.A.12; Decl. ¶ 129. For example, *Fujikawa* Figure 1A discloses conductive electrode 9g and **conductive material 106** at the bottom left corner of TFT array substrate 10. Decl. ¶ 129.



Fujikawa, Fig. 1A. The **conductive particles in conductive material 106** of **sealing material 107** are a “*plurality of conductive particles.*” Decl. ¶ 129. It would have also been obvious to include a plurality of conductive particles in the second part of the seal member for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 129; Sections VI.A.10-VI.A.12.

4. 8[c]: “*wherein the first conductive point is electrically connected to the common electrode.*”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 130-131.

As discussed above for limitation 7[j], **conductive electrode 9g** (“*first conductive point*”) is “electrically connected to the counter electrodes 21 of the counter substrate 20 through conductive material 106,” as shown below. *Fujikawa*, [0079]; Section VI.A.11; Decl. ¶ 131.

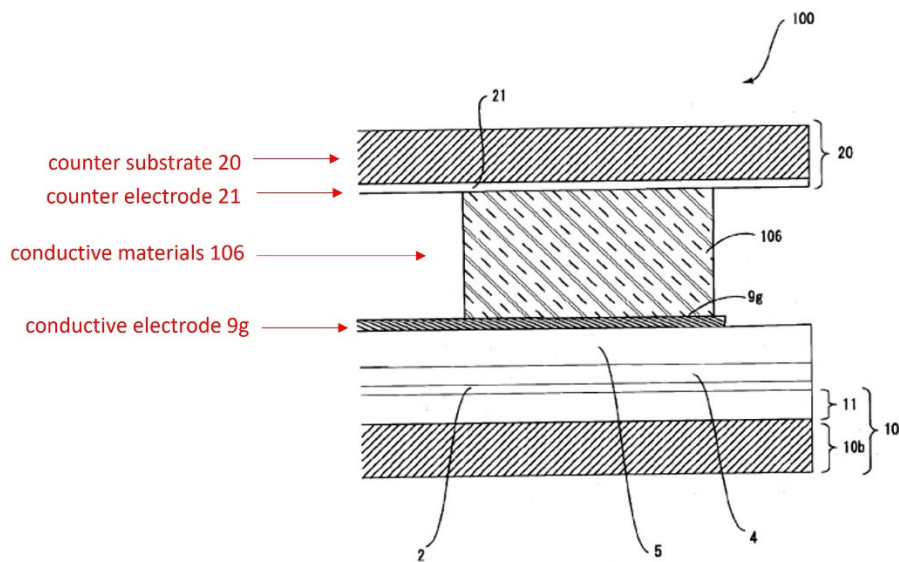


FIG.9

Id. at Fig. 9.

C. Claim 9

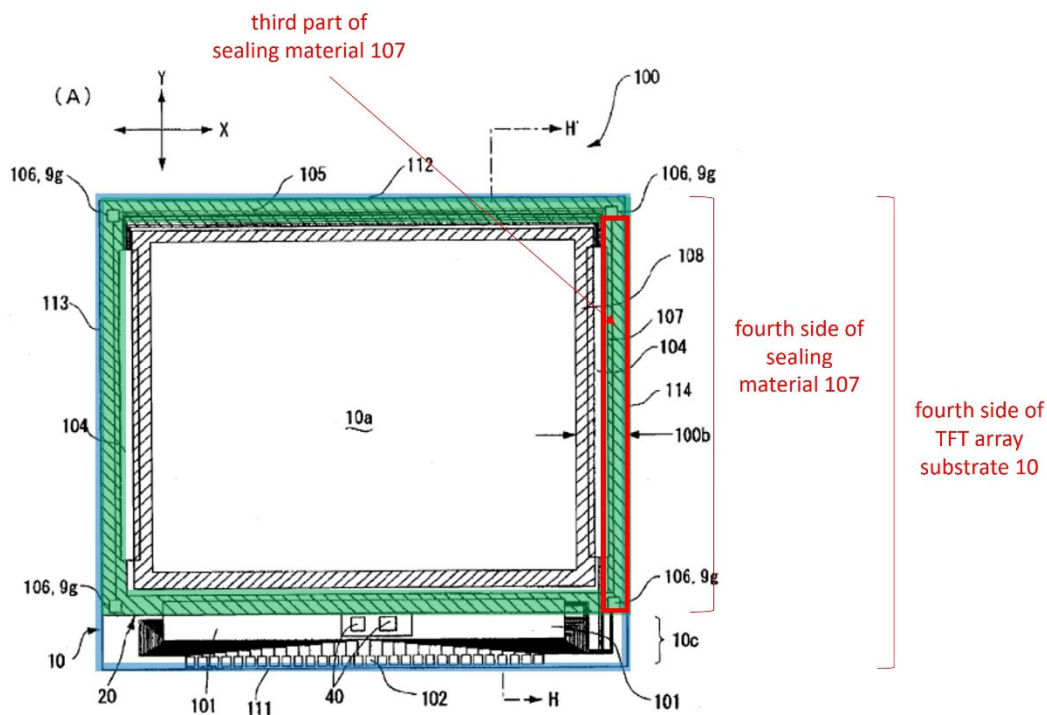
1. 9[pre]: “The display device, according to claim 8,”

Fujikawa discloses or renders obvious claim 8. Section VI.B; Decl. ¶ 132.

2. 9[a]: “wherein the first substrate includes a second conductive point on the fourth side and the seal member includes a third part of the seal member on the fourth side,”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 133-

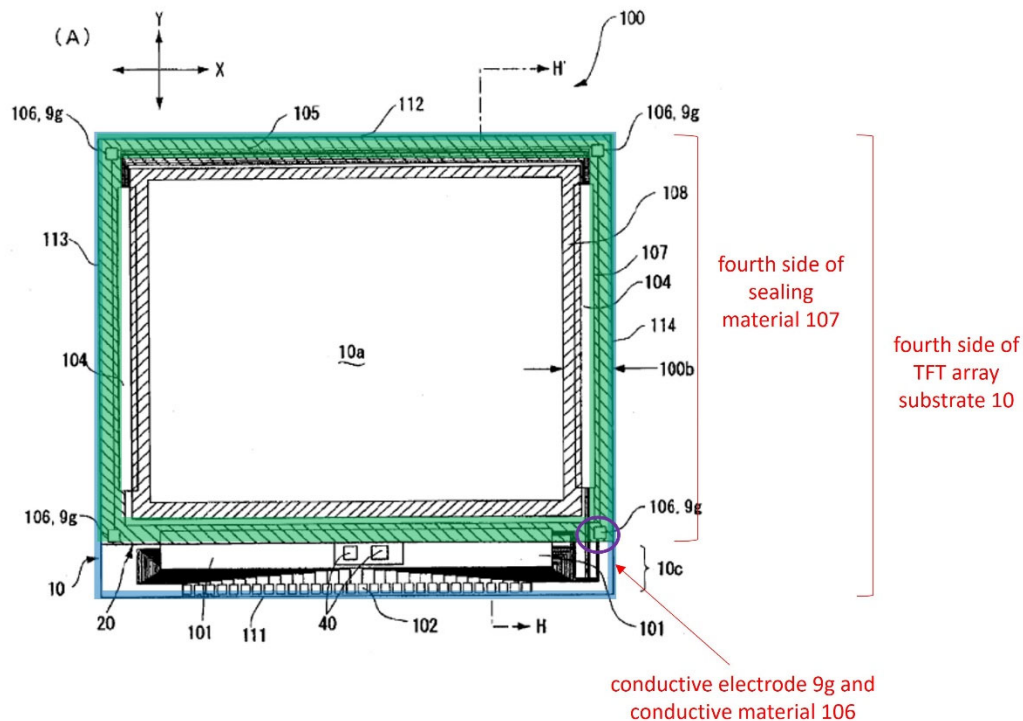
135. First, *Fujikawa* discloses a “*fourth side*” of the “*first substrate*”:



Fujikawa at Fig. 1A; Decl. ¶ 134. *Fujikawa* also discloses a “*third part of the seal member on the fourth side*,” as shown. Decl. ¶ 134.

Second, *Fujikawa* discloses or at least renders obvious a second conductive point on the fourth side. *See* Sections VI.A.10-VI.A.12; Decl. ¶ 135. For example,

Fujikawa discloses **conductive electrode 9g** at the bottom right corner of **TFT array substrate 10** in Figure 1A, as shown below. Decl. ¶ 135.



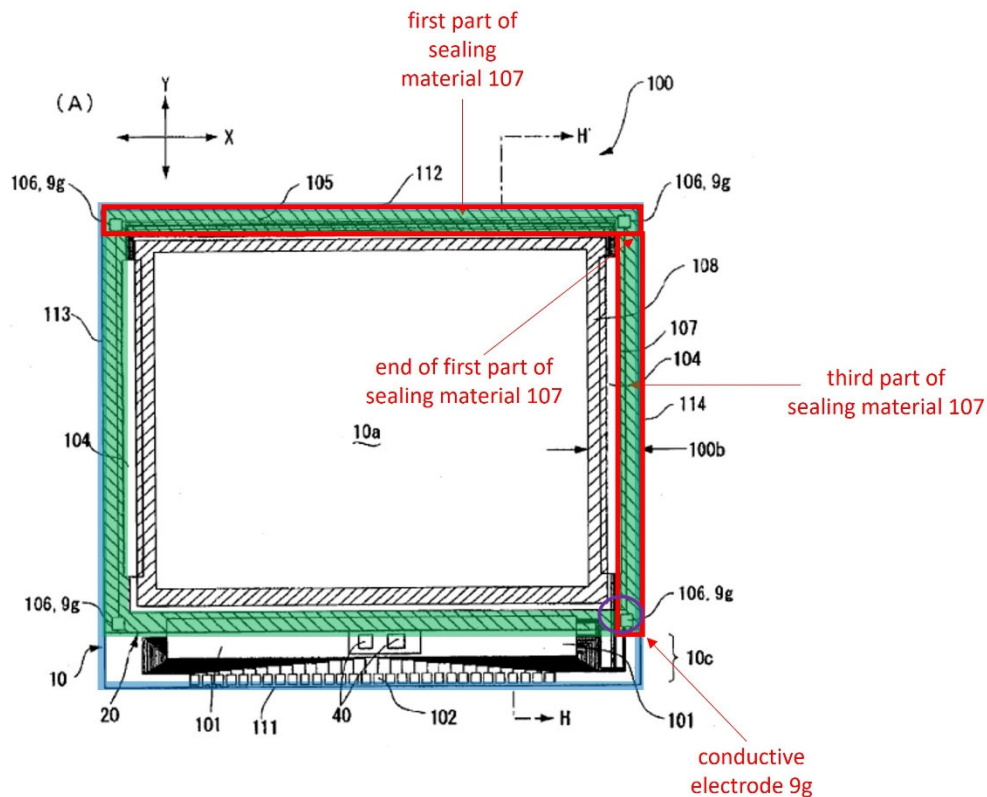
Fujikawa, Fig. 1A. This **conductive electrode 9g** is the “*second conductive point*” on the fourth side of the first substrate. Decl. ¶ 135. It would have likewise been obvious to include a conductive point along the fourth side of the first substrate for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 135; Sections VI.A.10-VI.A.12.

3. **9[b]: “the third part of the seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side, and the third part of the seal member includes a plurality of conductive particles, and”**

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 136-

138.

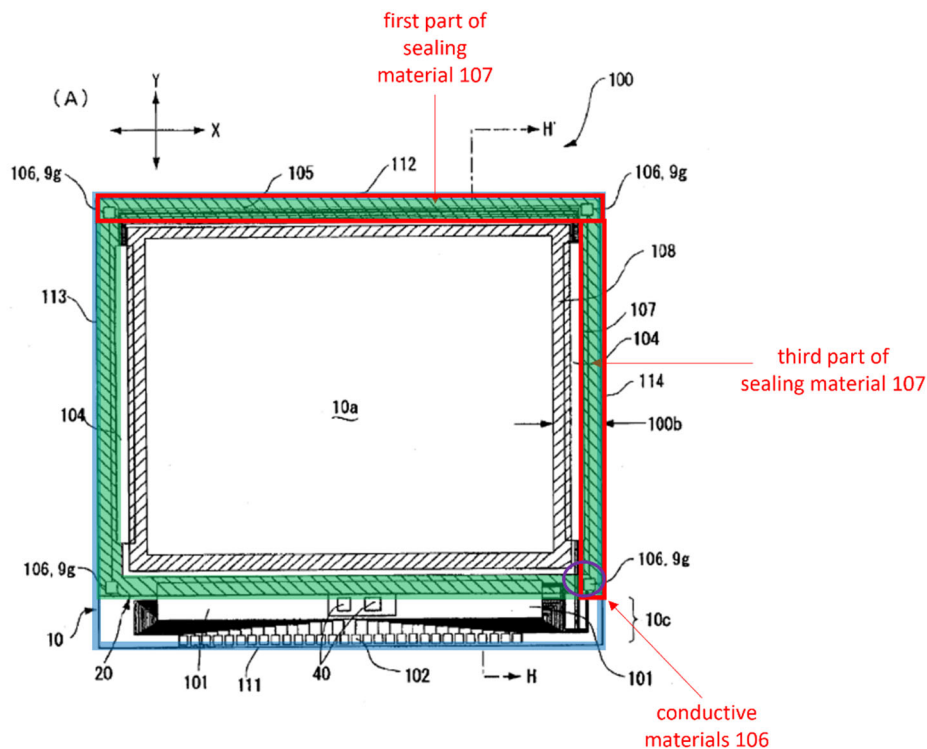
First, as discussed for limitation 9[a], *Fujikawa* discloses a “*third part*” of the “*seal member*” (sealing material 107). Section VI.C.2; Decl. ¶ 137. And as discussed for limitation 7[i], it also discloses a “*first part*” of the “*seal member*” (sealing material 107). Section VI.A.10; Decl. ¶ 137. As shown, the “*third part*” of the “*seal member extends from another end of the first part of the seal member over the second conductive point on the fourth side*”:



Fujikawa at Fig. 1A.

Second, *Fujikawa* discloses or at least renders obvious a plurality of conductive particles in the third part of the sealing member. Sections VI.A.10-

VI.A.12; Decl. ¶ 138. For example, *Fujikawa* Figure 1A discloses conductive electrode 9g and conductive material 106 at the bottom right corner of TFT array substrate 10. Decl. ¶ 138.



Fujikawa, Fig. 1A. The conductive particles in conductive material 106 of sealing material 107 are the “*plurality of conductive particles*.” Decl. ¶ 138. It would have also been obvious to include a plurality of conductive particles in the third part of the seal member for *Fujikawa* discloses the “number of conductive electrodes 9g, and the like may be appropriately changed.” *Fujikawa*, [0047]; Decl. ¶ 138; see Sections VI.A.10-VI.A.12.

4. 9[c]: “*wherein the second conductive point is electrically connected to the common electrode.*”

Fujikawa discloses or at least renders obvious this limitation. Decl. ¶¶ 139-140. As discussed for limitation 7[j], every **conductive electrode 9g** (“*second conductive point*”) is “electrically connected to the counter electrodes 21 of the counter substrate 20 through conductive material 106.” *Fujikawa*, [0079]; Section VI.A.11; Decl. ¶ 140.

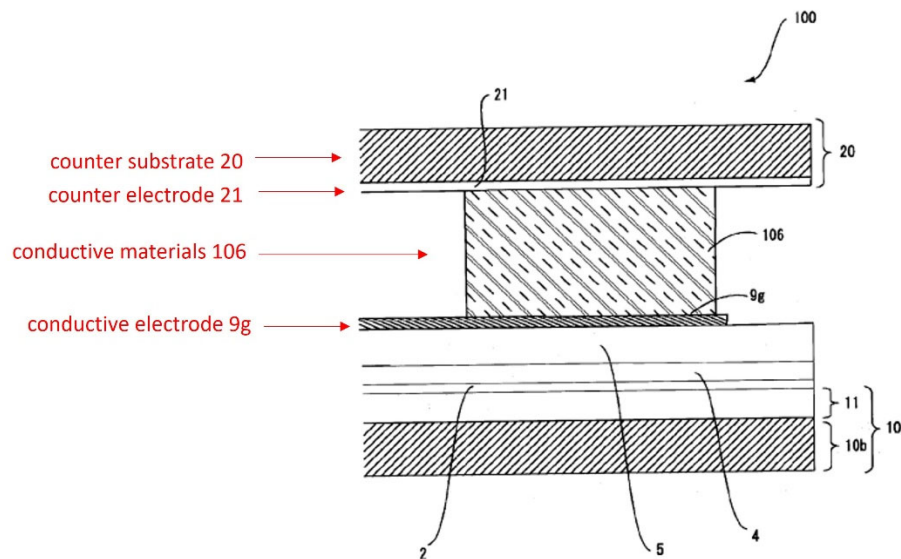
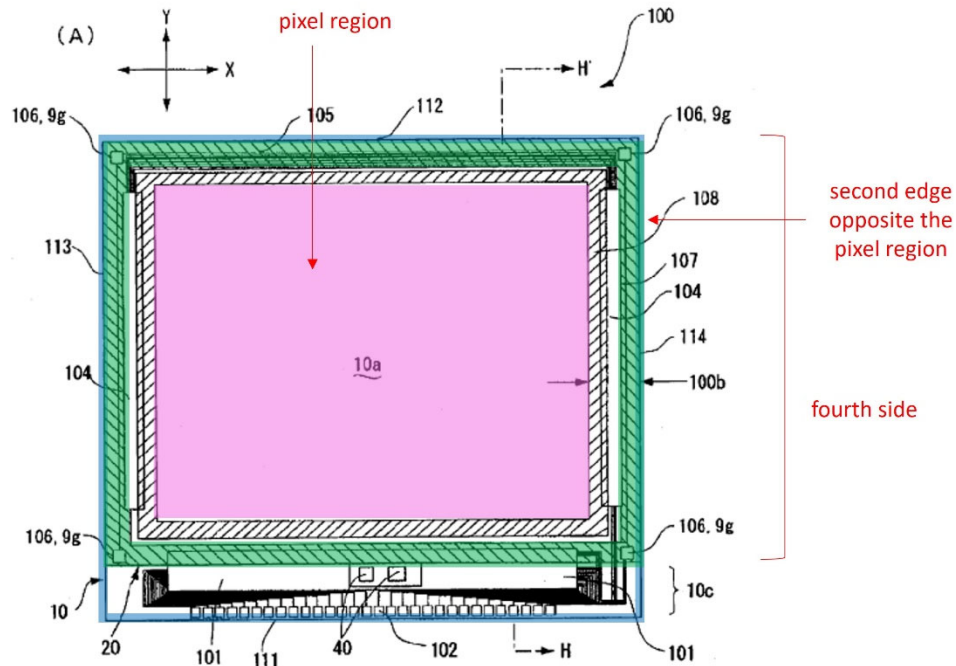


FIG.9

Id. at Fig. 9.

The **sealing material 107** fills the entire “area shaded by downward-slanting lines” in Figure 1A, “*extend[ing] to a second edge of the seal region opposite to the pixel region on the fourth side*”:



Fujikawa at Fig. 1A [0046], [0049]; Decl. ¶ 144.

F. Claim 12

1. “An electronic device comprising the display device according to claim 7.”

Fujikawa discloses or renders obvious a display device according to claim 7. Section VI.A; Decl. ¶ 145. Further, *Fujikawa* discloses this additional limitation in claim 12. Decl. ¶ 146. *Fujikawa* discloses its liquid crystal display device (“**display device**”) can be used in electronic devices, like portable computers and telephones (“**electronic device**”):

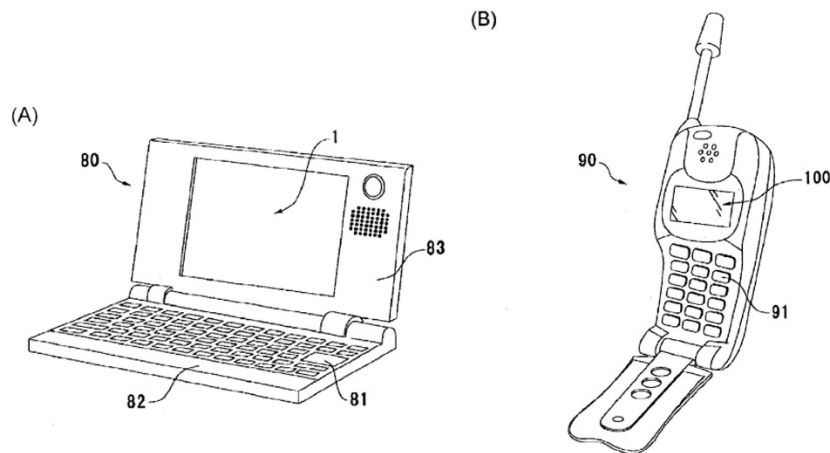


FIG. 17

Fujikawa at Figs. 17A-17B (combined), [0002]-[0004], [0010]-[0023], [0041], [0106]-[0107].

G. Claim 13

1. 13[pre]: “A display device, comprising:”

This preamble is substantially similar to the preamble in claim 7. Section VI.A.1; Decl. ¶ 147. If the preamble is limiting, *Fujikawa* discloses it. Section VI.A.1; Decl. ¶ 147.

2. 13[a]: “a first substrate including a plurality of pixel electrodes, a plurality of active elements and a plurality of wiring elements that connect to the plurality of active elements, wherein the plurality of active elements are thin film transistors disposed on the first substrate;”

Fujikawa discloses this limitation. Decl. ¶¶ 148-151.

As discussed for limitation 7[a], *Fujikawa* discloses a “**first substrate**” in TFT array substrate 10. Section VI.A.2; *Fujikawa*, [0046], Figs. 1A-1B; Decl.

¶ 149.

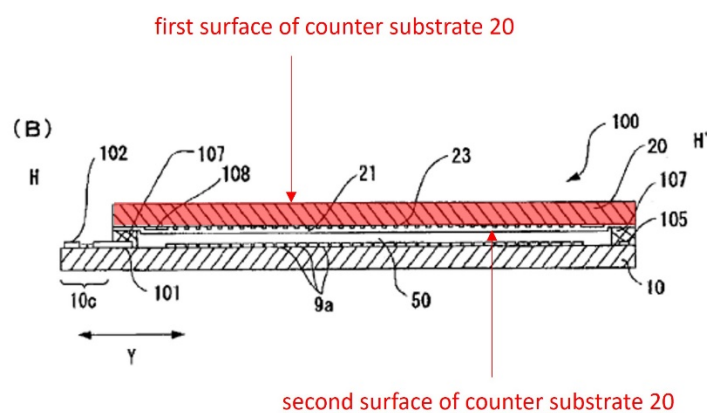
As discussed for limitations 7[a] and 7[b], *Fujikawa* discloses a pixel region with a plurality of pixels on TFT array substrate 10. Sections VI.A.2-VI.A.3. As discussed for limitation 7[b], each pixel has “a pixel electrode 9a and a pixel-switching TFT 30.” Section VI.A.3; *Fujikawa*, [0053], [0058], [0061]. *Fujikawa* discloses disposed on TFT array substrate 10 (“*first substrate*”) is “*a plurality of pixel electrodes*” and “*a plurality of active elements*” where “*the active elements are thin film transistors.*” Sections VI.A.2-VI.A.3; Decl. ¶ 150.

And as discussed above for limitation 7[1], *Fujikawa* discloses a “*plurality of wiring elements*” on the TFT array substrate 10 that “*connect to the plurality of active elements.*” See Section VI.A.13; Decl. ¶ 151.

3. 13[b]: “*a second substrate including a common electrode, wherein the common electrode is disposed on the second substrate;*”

Fujikawa discloses this limitation. Decl. ¶¶ 152-153.

As discussed for limitation 7[c], *Fujikawa* discloses the “*second substrate*” in counter substrate 20. Section VI.A.4; Decl. ¶ 153. *Fujikawa* likewise discloses a “*common electrode . . . disposed on the second substrate*” in counter electrodes 21 disposed on the bottom of counter substrate 20. Section VI.A.4; *Fujikawa*, [0050], [0058], [0079], Figs. 1B, 9; Decl. ¶ 153. These are shown below:



Fujikawa at Fig. 1B.

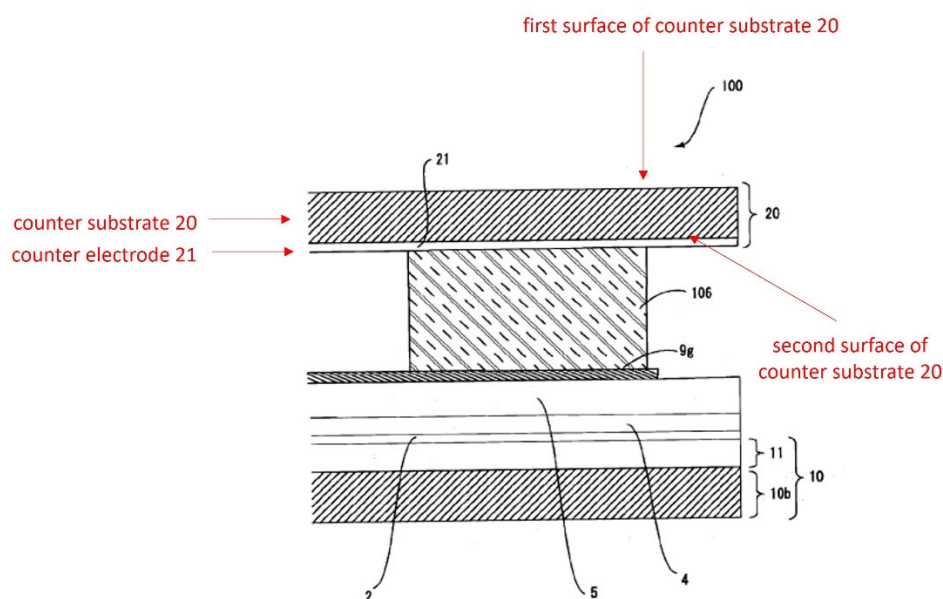


FIG.9

Id. at Fig. 9.

4. 13[c]: “a display region in which the plurality of pixel electrodes and the plurality of active elements are aligned in a plan-view of the first substrate;”

Fujikawa discloses this limitation. Decl. ¶¶ 154-155.

As discussed for limitations 7[a] and 7[b], *Fujikawa* discloses a pixel region (image display region 10a) (“*display region*”) on a first substrate that includes a plurality of pixels comprising pixel electrodes and TFTs (“*active elements*”). Decl. ¶ 155; *Fujikawa*, [0053]-[0054], [0058], [0061]; Sections VI.A.2-VI.A.3; The pixel electrodes and TFTs can be seen below:

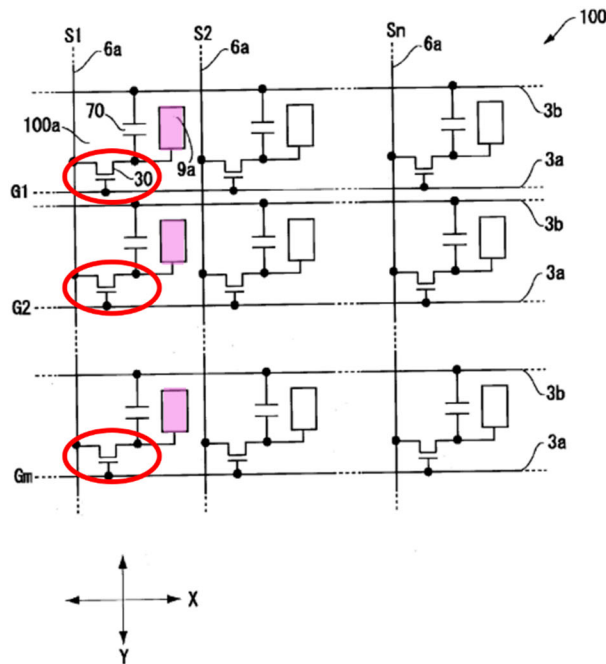


FIG.4

Fujikawa at Fig. 4. The pixel electrodes and TFTs in pixels 100a in the “*display region*” are “*aligned in a plan view of the first substrate,*” as shown in Figure 2:

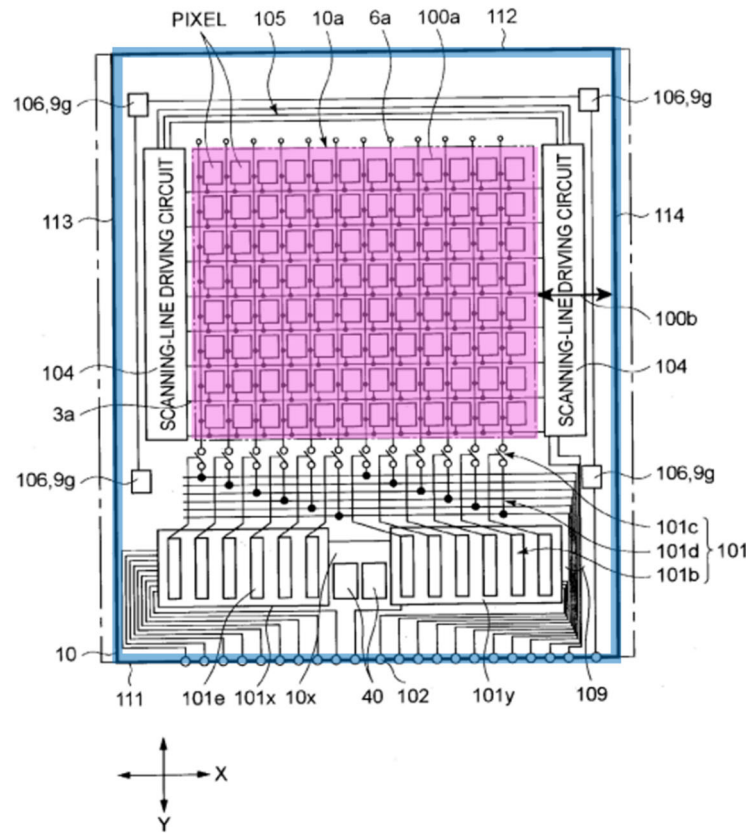


FIG.2

Fujikawa at Fig. 2; Decl. ¶ 155.

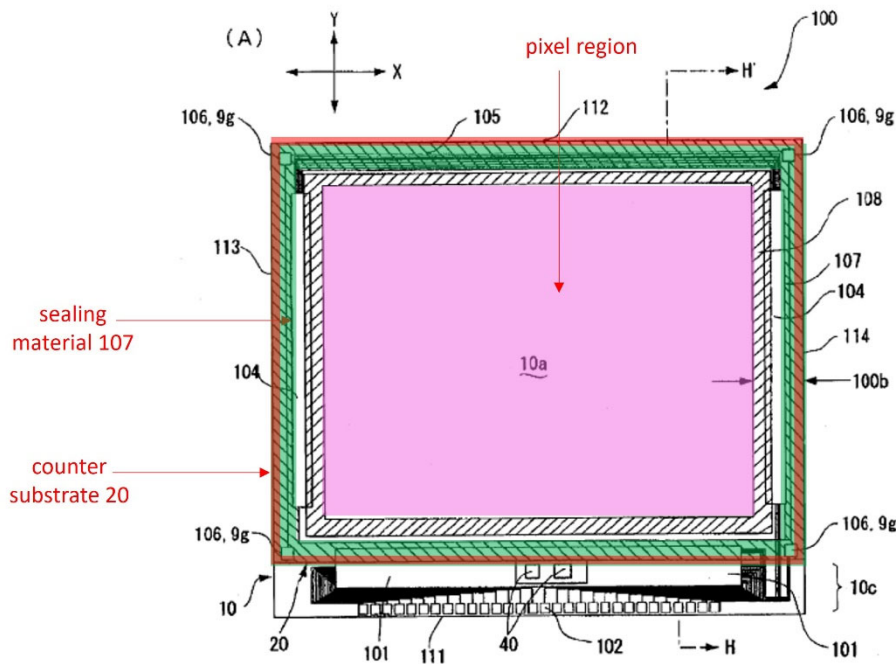
5. 13[d]: *“a seal region positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed;”*

Fujikawa discloses this limitation. Decl. ¶¶ 156-158.

As discussed for limitation 7[a], *Fujikawa* discloses a “**seal region**” of **sealing material 107** in the “area shaded by downward-slanting lines” in Figure 1A.

Section VI.A.2; *Fujikawa*, [0046], [0049], Figs. 1A-1B; Decl. ¶¶ 157.

As discussed for limitation 7[h], this “*seal region*” comprising **sealing material 107** (“*seal member*”) is “*positioned around the display region in the plan-view of the first substrate and forming a closed-ring shape in which the display region is disposed,*” as shown below. Section VI.A.9; Decl. ¶ 158.



Fujikawa at Fig. 1A.

6. 13[e]: “*a seal member being disposed in the seal region and bonding the first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes,*”

Fujikawa discloses this limitation. Decl. ¶¶ 159-160.

As discussed for limitation 7[d], *Fujikawa* discloses **sealing material 107** (“*seal member*”) in the “area shaded by downward-slanting lines” in Figure 1A (“*the seal region*”). *See supra* Section VI.A.5; Decl. ¶ 160. And as explained for

limitation 7[d], **sealing material 107** “*bond[s] the first substrate and the second substrate so that the common electrode faces the plurality of pixel electrodes.*”

See *supra* Section VI.A.5; Decl. ¶ 160; *Fujikawa*, [0046], [0049], Figs. 1A-1B.

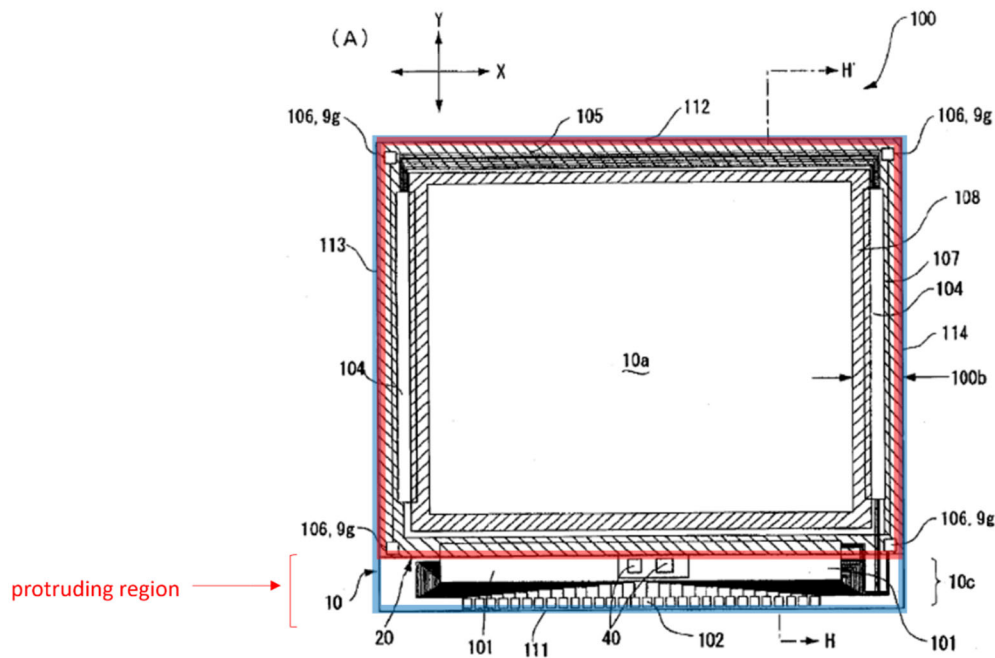
7. 13[f]: “*the seal member forming a closed-ring shape in which the display region is positioned without protruding from the second substrate in the plan-view of the first substrate, the seal member is disposed between the first substrate and the second substrate, and the seal member is formed continuously around the entire display region without the use of a plug;*”

This limitation is substantially similar to limitation 7[h]. Section VI.A.9; Decl. ¶ 161. For the reasons discussed above, *Fujikawa* discloses this limitation. Section VI.A.9; Decl. ¶ 161; Section VI.G.4 (“*display region*” in limitation 13[c] same as “*pixel region*” in limitation 7[a]).

8. 13[g]: “*wherein the first substrate includes a protruding region which protrudes over the second substrate in the plan-view of the first substrate and a plurality of conductive portions,*”

Fujikawa discloses this limitation. Decl. ¶¶ 162-164.

First, as discussed in limitation 7[e], *Fujikawa* discloses the “*first substrate includes a protruding region which protrudes over the second substrate in the plan-view.*” Section VI.A.6; Decl. ¶ 163. This is shown below:



Fujikawa at Fig. 1A; Decl. ¶ 163.

Second, *Fujikawa* discloses “[m]ultiple terminals 102 made of a metal film . . . , such as an ITO film, are formed along a substrate edge 111 of the TFT array substrate.” *Fujikawa* at [0055]. A “constant voltage” and “driving signals are input thereto.” *Id.* “A plurality of lines 109 made of, for example, a low-resistance metal film, . . . for driving a scanning-line driving circuit 104 and data-line driving circuits 101, are routed from these terminals 102.” *Id.* These elements are shown below:

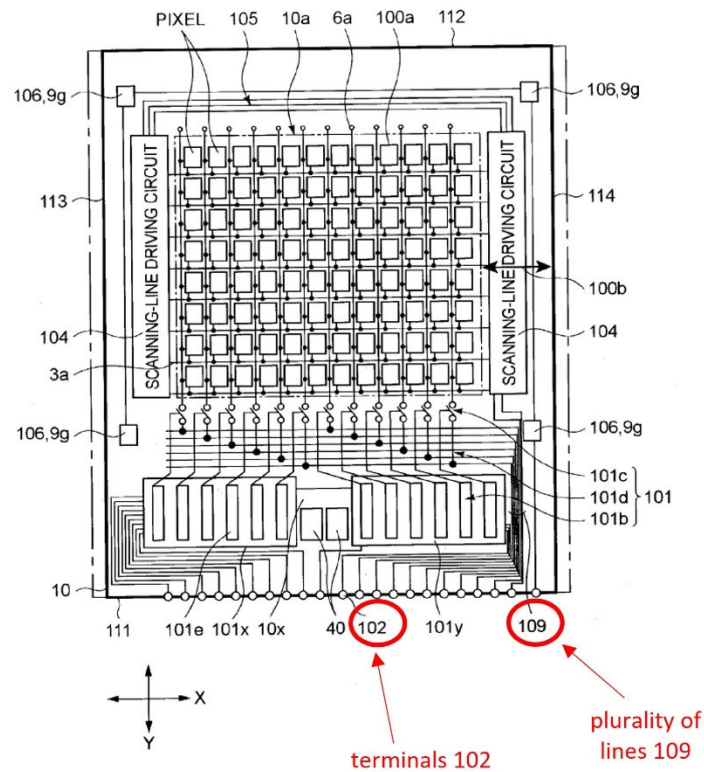


FIG.2

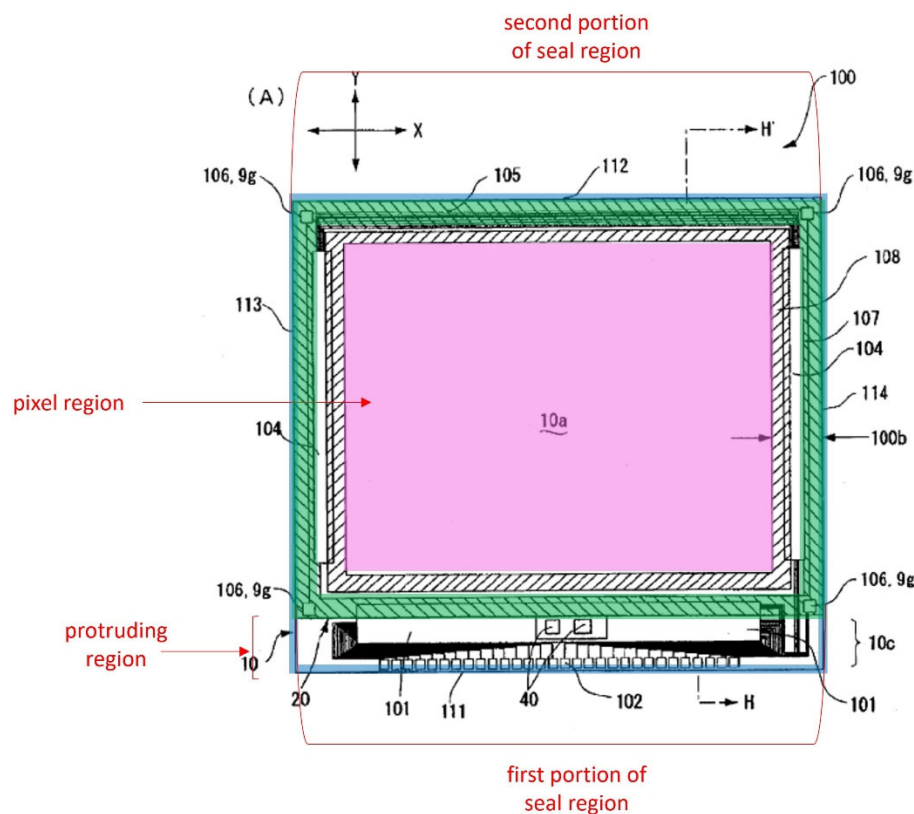
Id. at Fig. 2. *Fujikawa* thus discloses “***the first substrate includes . . . a plurality of conductive portions***” in “terminals 102.” Decl. ¶ 164.

9. 13[h]: “***the seal region includes a first portion and a second portion, the first portion is positioned at least between the display region and the protruding region, and the second portion is positioned at least opposite to the protruding region with respect to the display region, and***”

Fujikawa discloses this limitation. Decl. ¶¶ 165-166.

As discussed for limitation 7[b], *Fujikawa* discloses a seal region that forms a rectangular ring shape around **image display area 10a**. Section VI.A.3; Decl.

¶ 166. This seal region with **sealing material 107** includes at least a “*first portion*” and “*second portion.*” Decl. ¶ 166. As shown in Figure 1A, the “*first portion is positioned at least between the display region and the protruding region*” and the “*second portion is positioned at least opposite to the protruding region with respect to the display region*”:

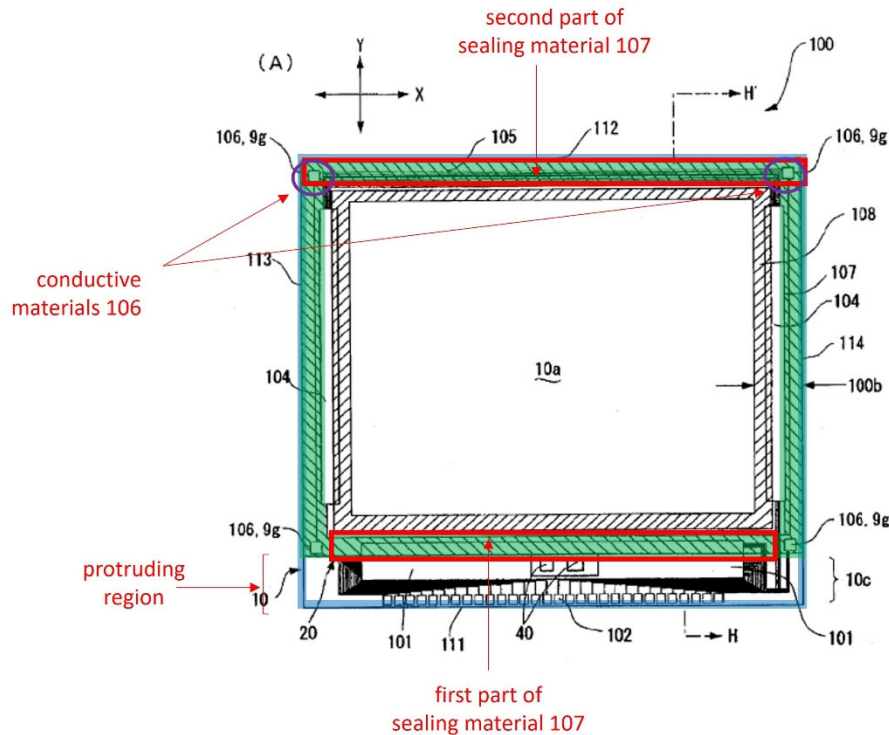


Fujikawa at Fig. 1A; Decl. ¶ 166.

10. 13[i]: “*the seal member includes a first part and a second part, the first part of the seal member is positioned on the first portion and the second part of the seal member is positioned on the second portion, and the second part of the seal member includes a plurality of conductive particles,*”

This limitation is substantially similar to limitation 7[i]. Section VI.A.10;

Decl. ¶ 167. As shown below, the sealing material includes “*a first part*” and “*a second part*”:



Fujikawa at Fig. 1A; Decl. ¶ 167. And for the reasons discussed for limitation 7[i], *Fujikawa* discloses or renders obvious “*the second part of the seal member includes a plurality of conductive particles.*” Decl. ¶ 167; Section VI.A.10; *Fujikawa*, [0047].

11. 13[j]: “*a plurality of dot conductive points are disposed on the second portion of the first substrate, all of the plurality of dot conductive points are electrically connected to the common electrode,*”

This limitation is substantially similar to limitation 7[j]. Section VI.A.11; Decl. ¶ 168. As explained above, *Fujikawa* discloses or at least renders obvious

this limitation. Section VI.A.11; Decl. ¶ 168; *Fujikawa*, [0047].

12. 13[k]: “*each of the plurality of the dot conductive points are spaced apart from each other, and*”

This limitation is substantially similar to limitation 7[k]. Section VI.A.12; Decl. ¶ 169. As explained above, *Fujikawa* discloses or at least renders obvious this limitation. Section VI.A.12; Decl. ¶ 169; *Fujikawa*, [0047].

13. 13[l]: “*the plurality of wiring lines extend onto the protruding region across the seal member without connecting to the dot conductive points.*”

This limitation is substantially similar to limitation 7[l]. Section VI.A.13; Decl. ¶ 170. As explained, *Fujikawa* discloses this limitation. Section VI.A.13; Decl. ¶ 170.

H. Claim 15

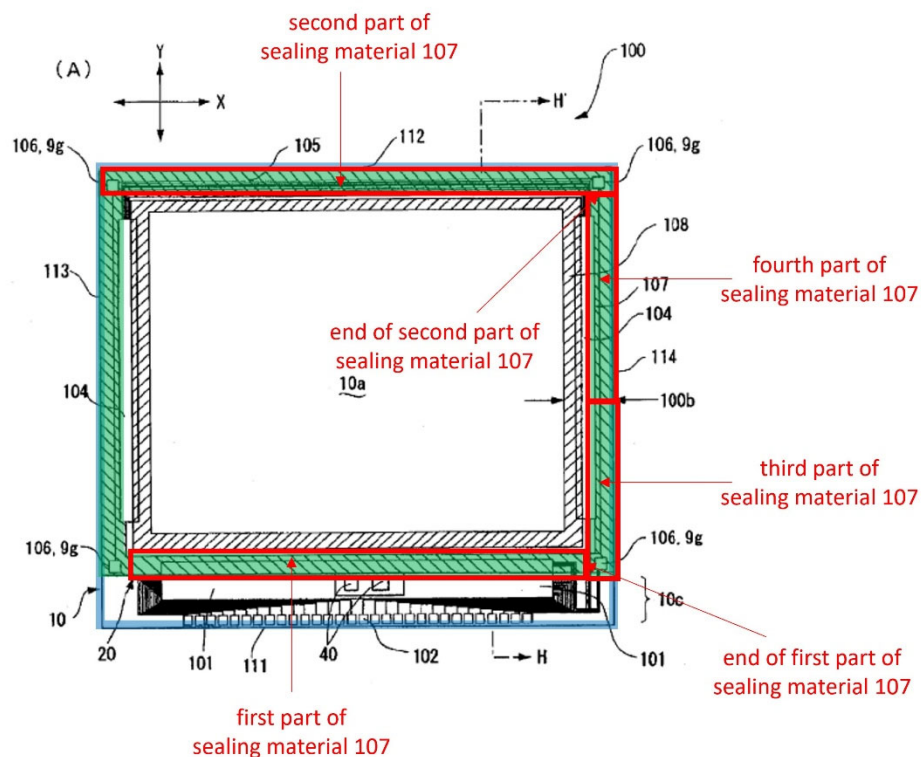
1. “*The display device, according to claim 13, wherein the seal member further includes a third part and a fourth part, the third part of the seal member extends from one end of the first part, and the fourth part of the seal member extends from one end of the second part and includes a first plurality of conductive particles.*”

Fujikawa discloses or renders obvious a display device according to claim 13. Section VI.G; Decl. ¶ 171. Moreover, *Fujikawa* at least renders obvious the additional limitation in claim 15. Decl. ¶ 171.

First, as discussed for limitations 7[b] and 7[d], *Fujikawa* discloses a seal region that forms a rectangular ring shape around the **image display area 10a** that

comprises **sealing material 107** (“*seal member*”). Sections VI.A.3, VI.A.5; Decl.

¶ 172. Under Patent Owner’s apparent interpretation of this limitation in the district court litigation, *Fujikawa* discloses **sealing material 107** includes at least a “*third part*” that “*extends from one end of the first part*” and “*fourth part*” that “*extends from one end of the second part*”:



Fujikawa at Fig. 1A; Decl. ¶ 172; Ex. 1019⁴ at 2-4.

Second, as discussed for limitation 7[i], *Fujikawa* at least renders obvious “*a first plurality of conductive particles*” along the seal member, including in a “*fourth part of the seal member.*” Section VI.A.10; Decl. ¶ 173; *Fujikawa*, [0047].

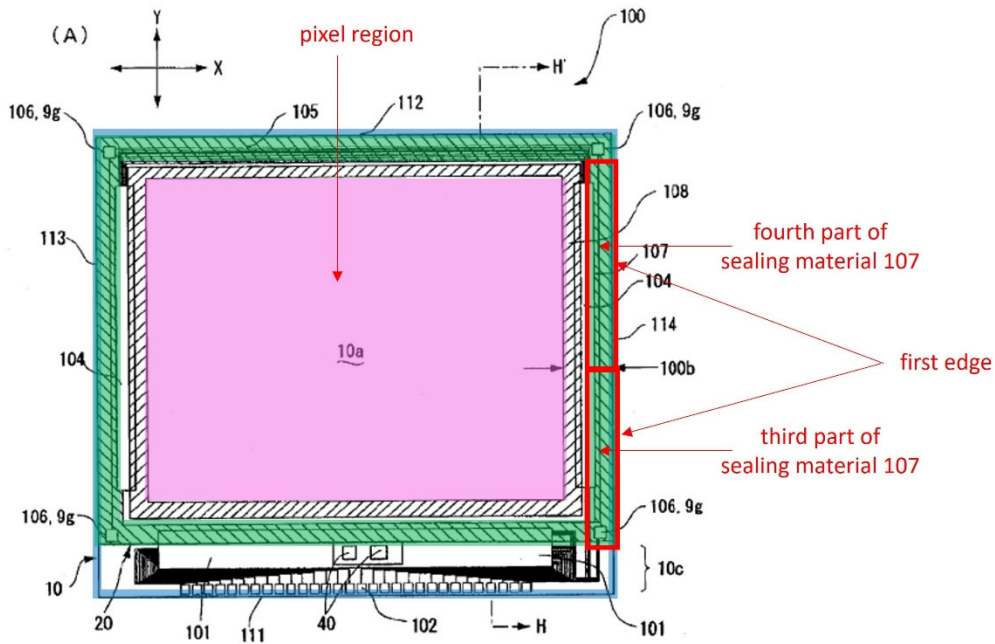
⁴ Citations correspond to the page number stamped on the exhibit.

I. Claim 16

1. ***“The display device, according to claim 15, wherein the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region.”***

Fujikawa discloses or renders obvious a display device according to claim 15. Section VI.H; Decl. ¶ 174. *Fujikawa* also discloses or at least renders obvious the additional limitation in claim 16. Decl. ¶ 174.

As discussed for claim 15, *Fujikawa* discloses a “*third part*” and a “*fourth part*” of the seal member. Section VI.H; Decl. ¶ 175. Under Patent Owner’s apparent interpretation of this limitation in the district court litigation, and as shown in Figure 1A, *Fujikawa* discloses “*the third part and the fourth part are connected and extend to a first edge of the seal region opposite to the display region*”:



Fujikawa at Fig. 1A; Decl. ¶ 175; Ex. 1019 at 4-5.

J. Claim 17

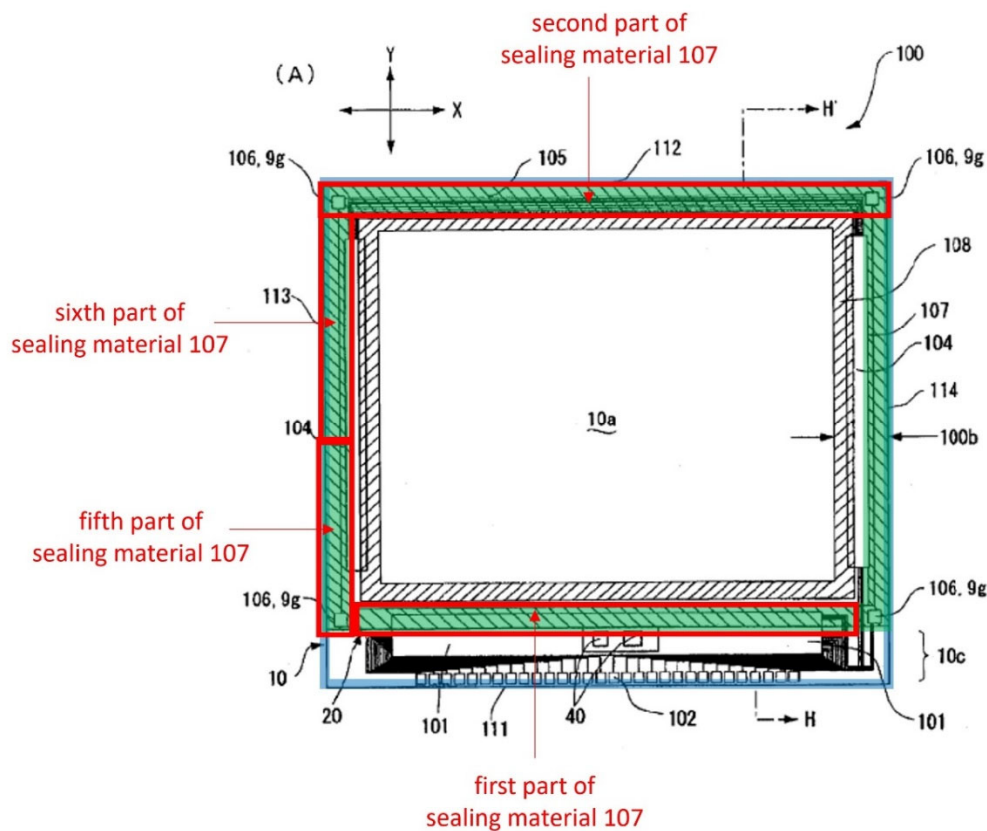
1. *“The display device, according to claim 16, wherein the seal member further includes a fifth part and a sixth part, the fifth part of the seal member extends from another end of the first part, and the sixth part of the seal member extends from another end of the second part and includes a second plurality of conductive particles, and the fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region.”*

Fujikawa discloses or renders obvious a display device according to claim 16. Section VI.I; Decl. ¶ 176. Moreover, *Fujikawa* at least renders obvious the additional limitation in claim 17. Decl. ¶ 176.

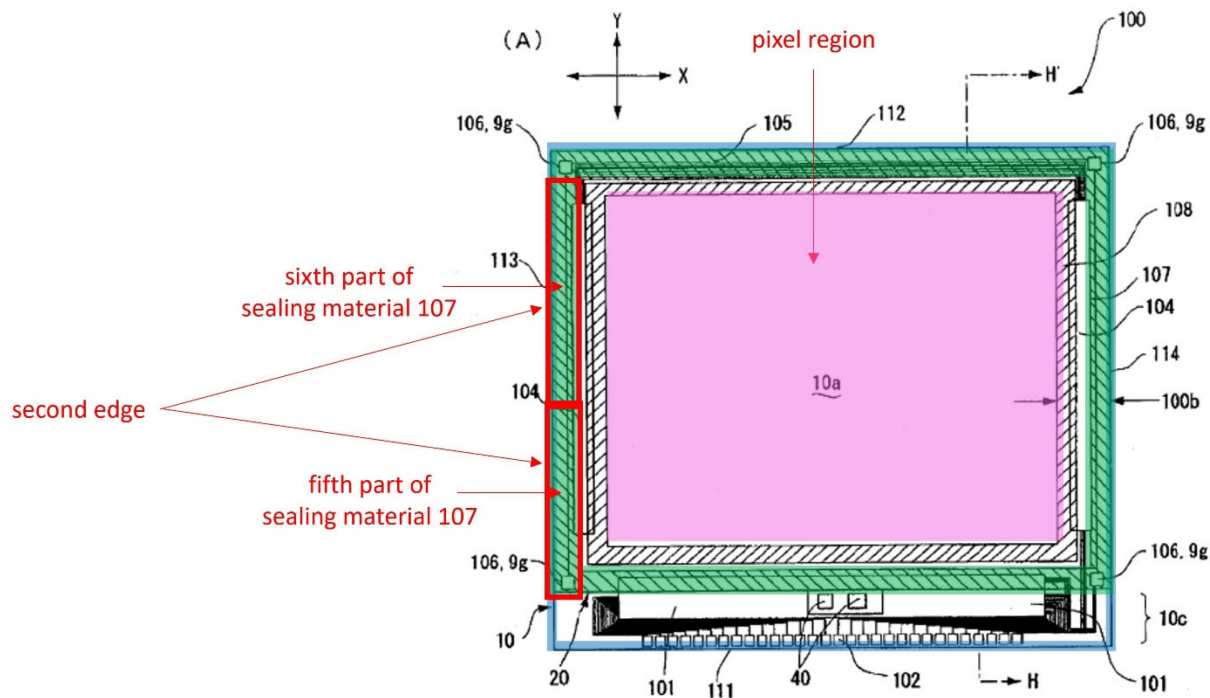
First, as discussed for limitations 7[b] and 7[d], *Fujikawa* discloses a seal region that forms a rectangular ring shape around the image display area 10a that

comprises **sealing material 107** (“*seal member*”). Sections VI.A.3, VI.A.5; Decl.

¶ 177. Under Patent Owner’s apparent interpretation of this limitation in the district court litigation, *Fujikawa* discloses **sealing material 107** includes at least includes a “*fifth part*” that “*extends from another end of the first part*” and “*sixth part*” that “*extends from another end of the second part*”:



Fujikawa at Fig. 1A; Decl. ¶ 177; Ex. 1019 at 5-7. Further, under Patent Owner’s apparent interpretation of this limitation in the district court litigation, and as shown below, the “*fifth part and the sixth part are connected and extend to a second edge of the seal region opposite to the display region*”:



Fujikawa at Fig. 1A; Decl. ¶ 177; Ex. 1019 at 5-7.

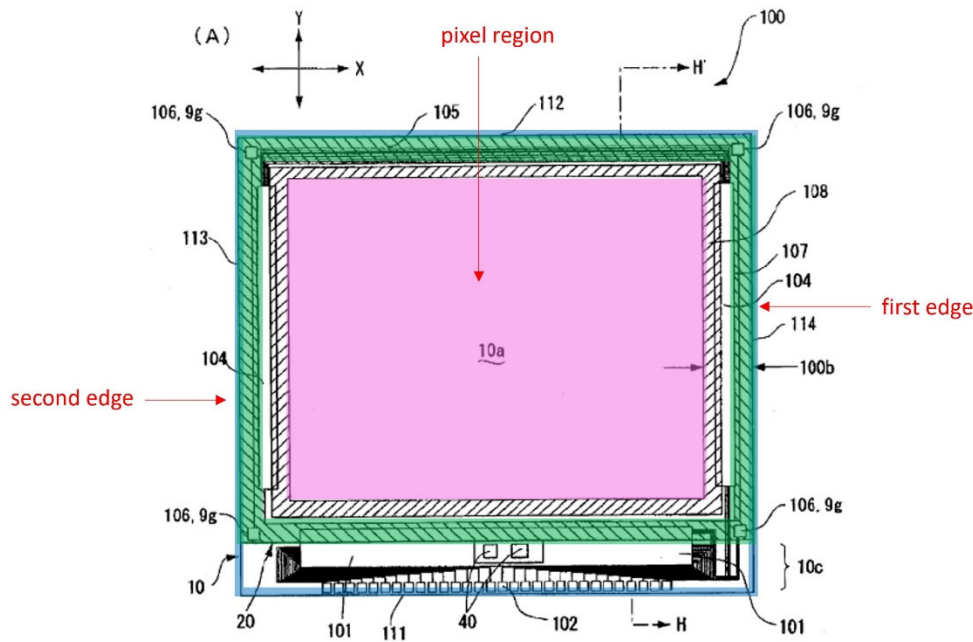
Second, as discussed for limitation 7[i], *Fujikawa* at least renders obvious “*a second plurality of conductive particles*” along the seal member, including in the “*sixth part of the seal member.*” Section VI.A.10; Decl. ¶ 178; *Fujikawa*, [0047].

K. Claim 18

1. *“The display device, according to claim 17, wherein the first edge of the seal region is positioned opposite to the second edge of the seal region with respect to the display region.”*

Fujikawa discloses or renders obvious a display device according to claim 17. Section VI.J; Decl. ¶ 179. *Fujikawa* also discloses the additional limitation of claim 18. Decl. ¶ 179. As discussed for claims 16 and 17, *Fujikawa* discloses a “*first edge of the seal region*” and a “*second edge of the seal region.*” Sections

VI.I-VI.J; Decl. ¶ 180. As shown in Figure 1A, the edges are “*positioned opposite*” each other “*with respect to the display region*”:



Fujikawa at Fig. 1A; Decl. ¶ 180.

L. Claim 19

1. 19[pre]: “*The display device, according to claim 18,*”

Fujikawa discloses or renders obvious a display device according to claim

18. Section VI.K; Decl. ¶ 181.

2. 19[a]: “wherein the first substrate further includes a first conductive point and a second conductive point, different from the plurality of conductive points, and the first conductive point, the second conductive point and the plurality of conductive points are disposed apart from each other, and”

This limitation is substantially similar to limitations 7[j], 7[k], 13[j], and

13[k], and claims 8 and 9. Sections VI.A.11-VI.A.12, VI.G.11-VI.G.12, VI.B-VI.C; Decl. ¶ 182. For the reasons discussed above, *Fujikawa* discloses or at least renders obvious this limitation. Sections VI.A.11-VI.A.12, VI.G.11-VI.G.12, VI.B. VI.C; Decl. ¶ 182.

3. **19[b]: “*the first conductive point is electrically connected to the common electrode through the first plurality of conductive particles and the second conductive point is electrically connected to the common electrode through the second plurality of conductive particles.*”**

This limitation is substantially similar to limitations 7[i], 7[j], 7[k], 13[i], 13[j], and 13[k], and claims 8, 9, 15, and 17. Sections VI.A.10-VI.A.12, VI.G.10-VI.G.12, VI.B-VI.C, VI.H, VI.J; Decl. ¶ 183. For the reasons discussed above, *Fujikawa* discloses or at least renders obvious this limitation. Sections VI.A.10-VI.A.12, VI.G.10-VI.G.12, VI.B-VI.C, VI.H, VI.J; Decl. ¶ 183.

M. Claim 20

1. **“*An electronic device comprising the display device according to claim 13.*”**

Fujikawa discloses or renders obvious a display device according to claim 13. See Section VI.G; Decl. ¶ 187. Moreover, *Fujikawa* discloses the additional limitation in claim 20, for the reasons discussed above in claim 12. Section VI.F; Decl. ¶ 184.

**VII. *Fujikawa* In View of *Kang* Renders Obvious Claims 7-13 and 15-20
(Ground 3)**

A. Independent Claim 7

1. 7[pre]-7[g]

Fujikawa discloses these limitations. Sections VI.A.1- VI.A.8; Decl. ¶ 185.

2. 7[h]

Fujikawa discloses this limitation. Section VI.A.9; Decl. ¶ 186.

Alternatively, this limitation would have been obvious to a POSITA in view of *Kang*. Section II.B; Decl. ¶ 186.

Kang discloses a dropping method that provides a marked improvement over vacuum methods for creating a liquid crystal display. Section II.B; *Kang* at [0068]-[0072]; '606 patent at 1:23-61 (admitting dropping method known improvement over vacuum method in background of the invention). According to *Kang*, vacuum methods that use a hole to inject liquid crystal from the outside and seal that hole with a plug were costly and slow. *Kang* at [0066]-[0067]. To avoid this problem, *Kang* discloses a “dropping” method where a “seal pattern” is “formed to have a closed shape that encompasses the outer edge of the image display part” on a first substrate. *Id.* at [0070]. Liquid crystal is dropped onto the “display part,” rather than “being filled from the outside” using a plug. *Id.* at [0069], [0070]. According to *Kang*, the “seal pattern” in this method has a “closed shape . . . to prevent the external leakage of the liquid crystal.” *Id.* at [0070]; *id.* at [0062] (seal 506 “may

be formed of various planar shapes”); Decl. ¶ 187.

A POSITA would have been motivated to combine *Fujikawa* and *Kang* to achieve such an improved liquid crystal display device. Decl. ¶ 188 As an initial matter, *Fujikawa* and *Kang* are analogous art to the ’606 patent. *Id.* They are both in the same field of endeavor as each other and as the ’606 patent. *Id.* The ’606 patent relates to a method of manufacturing a liquid crystal device (and resulting liquid crystal device). Section III.A; ’606 patent at 1:19-21. It discloses a dropping method of forming a liquid display device to avoid the cost and time associated with existing vacuum methods, as the ’606 patent admits was well known. ’606 patent at 1:23-3:58, 3:62-10:41, 18:36-19:27, 22:36-31:17. The resulting liquid display device has a seal member with a closed-ring shape that is formed around the pixel display area without the use of a plug. *Id.*, cls., 7, 13. So too does *Kang* disclose using a closed-shape seal pattern and a “dropping method” to create a liquid crystal device without the use of a plug. *Kang* at [0068]-[0072]. *Kang*’s seal pattern “may be formed of various planar shapes.” *Id.* at [0062]. Last, *Fujikawa* discloses a liquid crystal device with a rectangular ring shape seal member that surrounds a display area and “h[o]ld[s]” liquid crystal. *Fujikawa*, [0046], [0049].

A POSITA would have been motivated to use *Kang*’s dropping method and position *Fujikawa*’s sealing material 107 “*continuously*” in a “*closed-ring shape*” “*around the entire pixel region without the use of a plug.*” Decl. ¶¶ 189, 191. As

discussed, vacuum injection and dropping were the two known methods for liquid crystal filling. *Id.* As expressly explained in *Kang*, a POSITA would have known using *Kang*'s dropping method would have benefits when compared to the existing vacuum injection methods, such as reducing manufacture time and waste. *Kang* at [0065]-[0072]. Moreover, using the one drop method would allow for more direct control of display fabrication. Decl. ¶ 191. A POSITA would have looked to a reference like *Kang* to improve the manufacture and design of *Fujikawa*'s device and ensure no liquid crystal leaks out of the display to improve the resulting liquid crystal display. *Kang* at [0070]; Decl. ¶ 188; *see Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1379-81 (Fed. Cir. 2023) (known solution to known problem sufficient motivation); *KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) ("if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious").

A POSITA would have had a reasonable expectation of success using such a method with *Fujikawa*'s liquid crystal device. Using *Kang*'s dropping method and forming a seal pattern with a closed ring shape would simply be applying a known manufacturing method to improve a similar device in the same way to achieve the entirely predictable result of a liquid crystal display device with no "leakage of the liquid crystal." *Kang* at [0070]; '606 patent at 1:46-61 (drop methods were known

to be alternative to vacuum injection, successfully forming seal without injection hole, in the background of the invention section); Decl. ¶ 190. It would require no more than ordinary skill to provide the rectangular seal region in *Fujikawa* using *Kang*'s drop method to create a closed-ring structure as claimed, for *Kang* teaches seal patterns can "be formed of various planar shapes" using its methods. *Kang* at [0062]; Decl. ¶¶ 190-191.

3. 7[i]-7[k]

Fujikawa discloses or renders obvious these limitations. Sections VI.A.10-VI.A.12; Decl. ¶ 192.

4. 7[l]

Fujikawa discloses this limitation. Section VI.A.13; Decl. ¶ 193

B. Dependent Claims 8-9

Fujikawa discloses or renders obvious the additional limitations in claims 8 and 9. Sections VI.B-VI.C; Decl. ¶ 194.

C. Dependent Claims 10-12

Fujikawa discloses the additional limitations in claims 10-12. Sections VI.D-VI.F; Decl. ¶ 195.

D. Independent Claim 13

1. 13[pre]-13[c]

Fujikawa discloses these limitations. Sections VI.G.1-VI.G.4; Decl. ¶ 196.

2. 13[d]

As discussed for limitation 7[h] in Ground 3, *Fujikawa* and *Kang* render obvious this limitation. Section VII.A.2; Decl. ¶ 197.

3. 13[e]

Fujikawa discloses this limitation. Sections VI.G.6; Decl. ¶ 198.

4. 13[f]

As discussed for limitation 7[h] in Ground 3, *Fujikawa* and *Kang* render obvious this limitation. Section VII.A.2; Decl. ¶ 199.

5. 13[g]-13[h]

Fujikawa discloses these limitations. Sections VI.G.8-VI.G.9; Decl. ¶ 200.

6. 13[i]-13[k]

Fujikawa discloses or renders obvious these limitations. Sections VI.G.10-VI.G.12; Decl. ¶ 201

7. 13[l]

Fujikawa discloses this limitation. Section VI.G.13; Decl. ¶ 202.

E. Dependent Claim 15

Fujikawa at least renders obvious the additional limitation in claim 15. Section VI.H; Decl. ¶ 203.

F. Dependent Claim 16

Fujikawa discloses or at least renders obvious the additional limitation in claim 16. Section VI.I; Decl. ¶ 204.

G. Dependent Claim 17

Fujikawa at least renders obvious the additional limitation in claim 17.

Section VI.J; Decl. ¶ 205.

H. Dependent Claim 18

Fujikawa discloses the additional limitation in claim 18. Section VI.K; Decl. ¶ 206.

I. Dependent Claim 19

Fujikawa discloses or renders obvious the additional limitations in claim 19. Section VI.L; Decl. ¶ 207.

J. Dependent Claim 20

Fujikawa discloses the additional limitation in claim 20. Section VI.M; Decl. ¶ 208.

VIII. *Fujikawa* In View of *Ikeguchi* Renders Obvious Claims 7-13 and 15-20 (Ground 4)

A. Independent Claim 7

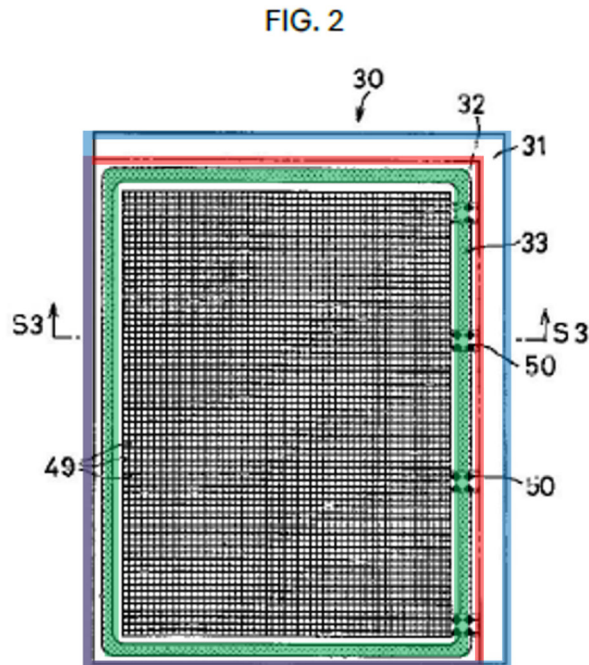
1. 7[pre]-7[a]

Fujikawa discloses these limitations. Sections VI.A.1-VI.A.2; Decl. ¶ 209.

2. 7[b]

As discussed above, *Fujikawa* discloses this limitation. *See supra* Section VI.A.3; Decl. ¶ 210. Alternatively, the seal region having “*a rectangular ring shape*” would have been obvious over *Ikeguchi*. Decl. ¶ 210. *Ikeguchi* discloses

two substrates “disposed and layered spaced apart” and “bonded together by a sealing material 33 provided in a rectangular closed-loop shape.” *Ikeguchi*, [0027], [0030], [0039]. This is shown below:



Id. at Fig. 2; Decl. ¶ 210. A POSITA would have been motivated to have a rectangular seal region to match the shapes of the substrates and pixel region, and in turn reduce the amount of sealing material used. Decl. ¶ 210. Indeed, rectangular shapes were common in display applications and using a differently shaped sealing region would waste space and liquid crystal material. *Id.* A POSITA would have had a reasonable expectation of success implementing this well-known shape in *Fujikawa*’s device. *Id.*

3. 7[c]-7[h]

Fujikawa discloses these limitations. Sections VI.A.4-VI.A.9; Decl. ¶ 211.

4. 7[i]

As discussed, *Fujikawa* discloses or at least renders obvious this limitation. Section VI.A.10; *Fujikawa*, [0047]; Decl. ¶ 212. Alternatively, it would have been obvious to have additional conductive particles (with additional conductive electrodes 9g, *infra* Section VIII.A.5) in *Fujikawa*'s design in view of *Ikeguchi*. Decl. ¶ 212.

Ikeguchi discloses an improved liquid crystal device that reduces non-display area while achieving reliable conduction and improved display quality and stability. *Ikeguchi* at [0013], [0043], [0047]. The device includes substrates (31, 32) bonded with sealing material 33. *Id.* at [0027]-[0030], [0042]. The sealing material 33 is mixed with a conductive material to facilitate connectivity between substrates. *Id.* at [0015]-[0018], [0037], [0039]-[0040], [0042]-[0043]. Conductor material 50 in sealing material 33 can comprise "conductive particles in which metal layers are formed on the surfaces of synthetic-resin base particles." *Id.* at [0037], [0040], [0042]-[0043]. This is shown below:



particles.” Decl. ¶ 213. *Fujikawa* Figure 9 and *Ikeguchi* Figure 4 are provided side-by-side below:

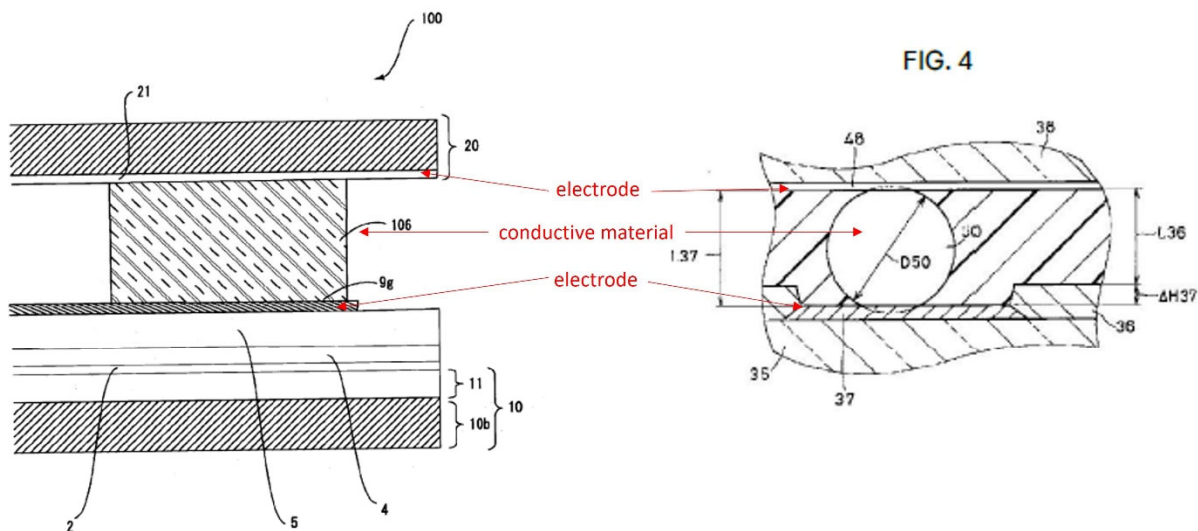


FIG.9

Fujikawa, Fig. 9 (left); *Ikeguchi*, Fig. 4 (right); Decl. ¶ 213.

A POSITA would have been motivated to combine *Fujikawa* and *Ikeguchi* to provide a plurality of conductive particles in the seal member along the first part of the seal member. Decl. ¶ 214. As an initial matter, *Fujikawa* and *Ikeguchi* are analogous art to the '606 patent. *Id.* They are in the same field of endeavor as each other and the '606 patent. *Id.* The '606 patent relates to a method of manufacturing a liquid crystal device (and the resulting liquid crystal device). Section III.A; '606 patent at 1:19-21. It discloses a liquid crystal device that includes a seal member

having a plurality of conductive particles and a plurality of dot conductive points separated from each other to electrically connect substrates. '606 patent at 38:26-67, Fig. 30. So too does *Fujikawa* disclose an improved liquid crystal display device with a plurality of conductive electrodes 9g and conductive materials 106 to reduce non-display area. *Fujikawa*, [0010]-[0011], [0047], [0079], Figs. 1A, 9. And *Ikeguchi* also discloses a plurality of common electrodes 37 and conductor materials 50 within sealing material 33 to reduce the non-display area and provide reliable conduction between electrode substrates. *Ikeguchi*, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047].

A POSITA would have been motivated to provide additional conductive particles in *Fujikawa*'s sealing material 107 ("*seal member*") in view of *Ikeguchi* to further reduce non-display area, achieve reliable conduction between the two substrates, and improve display quality and stability. Decl. ¶¶ 215-216. As noted, *Fujikawa* discloses, in existing devices, the "frame region" that "does not directly contribute to the display" is often too large. *Fujikawa* at [0010]. As such, *Fujikawa* strives to "decrease the proportion of the width of the frame region," and in turn, increase the relative image display region, while keeping the liquid crystal display device small. *Id.* A POSITA would have looked to references like *Ikeguchi* that try to solve a similar problem and would have been motivated to implement *Ikeguchi*'s improvements (multiple conductive particles in seal material) in *Fujikawa*'s design

to reduce non-display area, achieve reliable conduction, and improve the display quality and stability. Decl. ¶ 215; *Ikeguchi*, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047]; *Intel*, 61 F.4th at 1379-81; *KSR*, 550 U.S. at 417. Indeed, *Ikeguchi* explains, with its design, a “non-display region 53 in which the sealing material 33, the common electrode 37, the connection electrode, and the conductive material 50 are disposed can thus be made small.” *Ikeguchi*, [0043]. A POSITA would have understood having more points of electrical contact would retain a stable voltage across the common electrode and reduce impedance, while also reducing non-display area. Decl. ¶ 216.

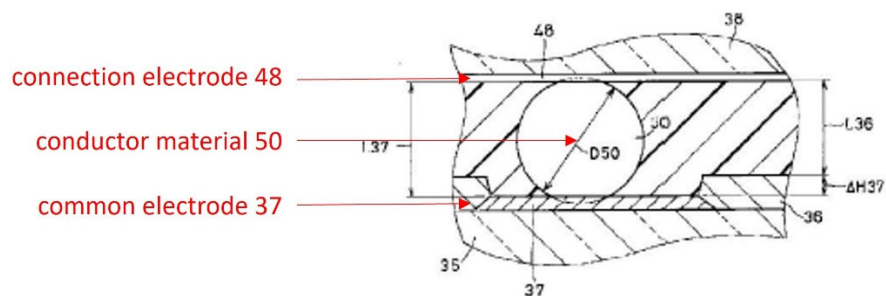
A POSITA would have done so with a reasonable expectation of success. Decl. ¶ 217. Adding additional conductive particles along the side of *Fujikawa*’s sealing material 107 would have been the simple use of a known design to improve a similar device in the same way to achieve a predictable result (namely, a liquid crystal display device with improved conductivity and reduced non-display area). *Id.* It would have required no more than ordinary skill to add additional conductive particles along the side of *Fujikawa*’s sealing material 107. *Id.* And the POSITA would have understood doing so would not frustrate *Fujikawa*’s existing design, while offering the known benefits discussed above. *Id.*; see also, e.g., *Fujikawa*, [0047] (“number of conductive electrodes 9g, and the like may be appropriately changed”).

5. 7[j]

As discussed, *Fujikawa* discloses or at least renders obvious this limitation. Section VI.A.11; *Fujikawa*, [0047]; Decl. ¶ 218. Alternatively, it would have been obvious to have additional dot conductive points in *Fujikawa*'s design in view of *Ikeguchi*. Decl. ¶ 218.

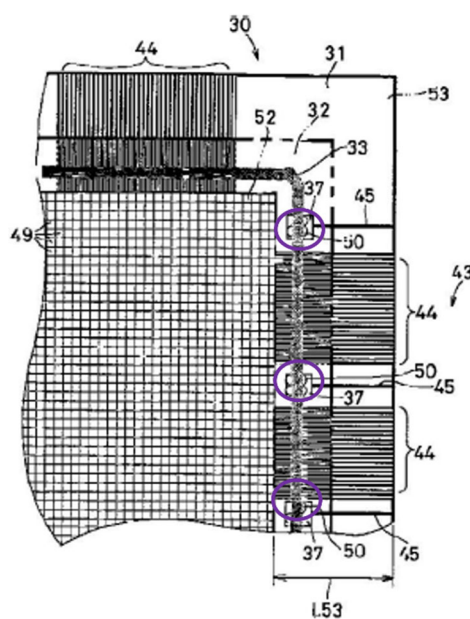
Ikeguchi discloses a liquid crystal device that reduces the non-display area while achieving reliable conduction between the substrates and improved display quality and stability. *Ikeguchi* at [0013], [0043], [0047]. *Ikeguchi*'s device includes two substrates (31, 32) bonded using a sealing material 33. *Id.* at [0027]-[0030], [0042]. *Ikeguchi* explains it is necessary to electrically connect the substrates and discloses a "conducting portion" to do so. *Id.* at [0037]. This conducting portion comprises common electrode 37 on the first substrate, connection electrode 48 on the second substrate, and the conductor material 50 located in the seal material 33 "sandwiched" in between the two electrodes. *Id.* at [0037] ("counter electrode 42 and the connection electrode 48 may be realized by a single electrode"), [0039], [0040], [0042]-[0043]. This is shown below:

FIG. 4



Id. at Fig. 4. And as *Ikeguchi* shows in Figure 1, numerous, discrete locations of common electrode 37 and conductor material 50 along the side of the substrate can be provided:

FIG. 1



Id. at Fig. 1. Like the conductive electrodes 9g in *Fujikawa*, common electrodes 37

in *Ikeguchi* are the claimed “*dot conductive points*.” Decl. ¶ 219. *Fujikawa* Figure 9 and *Ikeguchi* Figure 4 are provided side-by-side below:

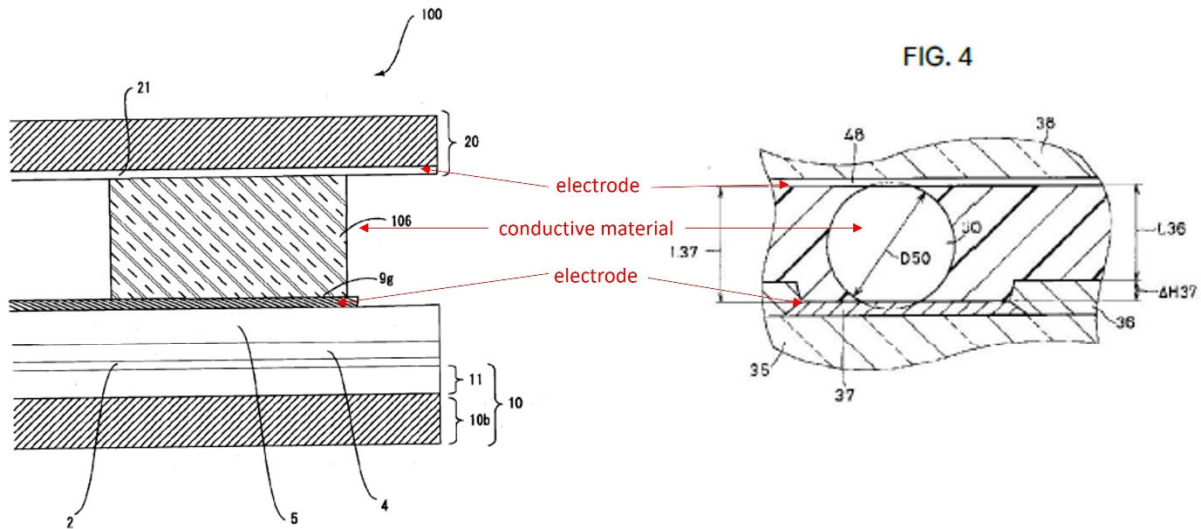


FIG.9

Fujikawa, Fig. 9 (left); *Ikeguchi*, Fig. 4 (right).

A POSITA would have been motivated to combine *Fujikawa* and *Ikeguchi* to provide a plurality of dot conductive points along the side of the first substrate. Decl. ¶¶ 220-222. As an initial matter, and as discussed in Section VIII.A.4, both *Fujikawa* and *Ikeguchi* are analogous art to the '606 patent. Decl. ¶ 220

A POSITA would have been motivated to provide additional dot conductive points along the side of *Fujikawa*'s first substrate in view of *Ikeguchi* to further reduce non-display area, achieve reliable conduction between the two substrates,

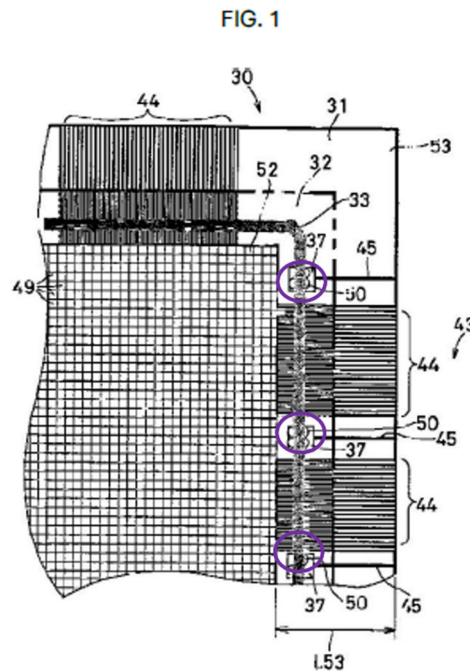
and improve display quality and stability. Decl. ¶¶ 221-222. As noted, *Fujikawa* discloses that, in existing liquid display devices, the “frame region” that “does not directly contribute to the display” is too large. *Fujikawa* at [0010]. *Fujikawa* thus strives to “decrease the proportion of the width of the frame region,” and in turn, increase the relative image display region, while keeping the liquid crystal display device small. *Id.* A POSITA would have looked to references like *Ikeguchi*, that try to solve a similar problem, and would have been motivated to also implement its improvements (multiple dot conductive points along the edge of the first substrate) in *Fujikawa*’s design to reduce the non-display area, achieve reliable conduction, and improve display quality and stability. Decl. ¶ 221; *Ikeguchi*, [0013], [0037], [0039]-[0040], [0042]-[0043], [0047]; *Intel*, 61 F.4th at 1379-81; *KSR*, 550 U.S. at 417. Indeed, *Ikeguchi* explains, with its design, a “non-display region 53 in which the sealing material 33, the common electrode 37, the connection electrode, and the conductive material 50 are disposed can thus be made small.” *Ikeguchi*, [0043]. A POSITA would have understood having more points of electrical contact would retain a stable voltage across the common electrode and reduce impedance, while also reducing non-display area. Decl. ¶ 222.

A POSITA would have done so with a reasonable expectation of success. Decl. ¶ 223. Adding additional dot conductive points along the side of *Fujikawa*’s first substrate would have been the simple use of a known design to improve a

similar device in the same way to achieve a predictable result (namely, a liquid crystal display device with improved conductivity and reduced non-display area). *Id.* It would have required no more than ordinary skill to add more dot conductive points along the side of *Fujikawa*'s TFT array substrate 10. *Id.* And the POSITA would have understood that doing so would not have frustrated *Fujikawa*'s existing design, while offering the known benefits discussed above. *Id.*; *Fujikawa*, [0047] (“number of conductive electrodes 9g and the like may be appropriately changed”).

6. 7[k]

As discussed, *Fujikawa* discloses or at least renders obvious this limitation. Section VI.A.12; Decl. ¶ 224. Alternatively, to the extent *Fujikawa* is modified in view of *Ikeguchi* to have additional conductive particles and dot conductive points (Sections VIII.A.4-VIII.A.5), this limitation would have been obvious in view of *Fujikawa* and *Ikeguchi*. Decl. ¶ 224. As shown in Figure 1, discrete locations of the common electrode 37 and conductor material 50 can be “*spaced apart from each other*”:

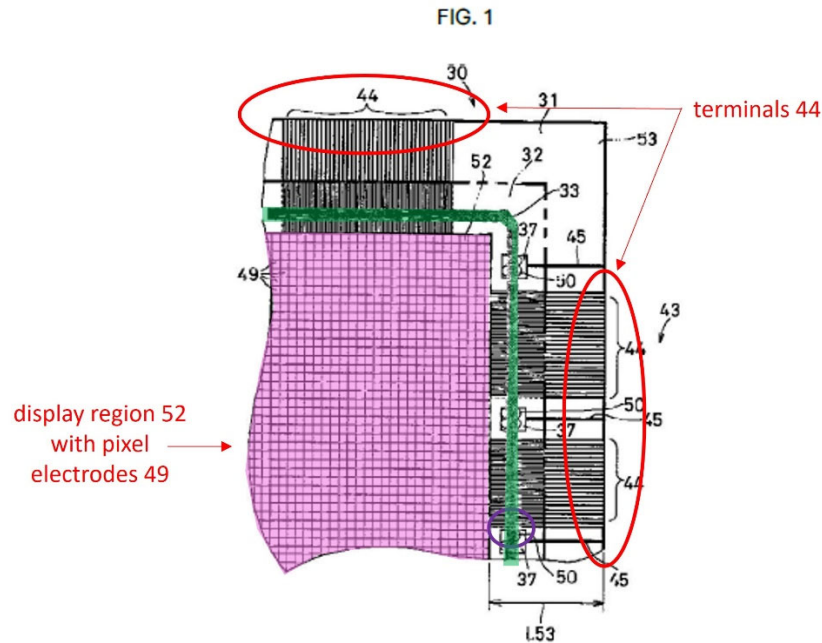


Ikeguchi at Fig. 1.

7. 7[I]

As discussed, *Fujikawa* discloses this limitation. *See supra* Section VI.A.13; Decl. ¶ 225. In the event Patent Owner argues that *Fujikawa*'s data lines can only include lines 6a, it would have been obvious to have the wiring lines “***extend onto the protruding region across the seal member***” in view of *Ikeguchi*. Decl. ¶ 225.

Ikeguchi discloses a driver integrated circuit that drives the display. *Ikeguchi* at [0031]-[0032]. The drive integrated circuit comprises input terminals 44 located on a “one-side edge” of first electrode substrate 31 outside *Ikeguchi*'s seal material 33:



Id. at Fig. 1, [0035] (explaining that terminals 44 “formed in the portions thereof protruding outward from the second electrode substrate”). *Ikeguchi* explains these terminals in the driver integrated circuit are “electrically connected to” the TFTs in the pixel electrodes in the display region 52 “via connection lines.” *Id.* at [0034]; *see also id.* at [0033]-[0035]. A POSITA would have understood the “connection lines” extend from the TFTs in the display region, across the seal material, out to the terminals in the protruding regions to “electrically connect[]” the TFTs and the driver integrated circuit. *See Decl.* ¶ 226. A POSITA would have been motivated to implement such a design in *Fujikawa*. *Id.* The driver integrated circuit can be either within the sealing region or outside the sealing region. It would have been the simple selection of a known design to obtain a predictable result to have the

driver integrated circuit located outside the seal region and in turn the wires that connect that circuit to the TFTs in the display area cross the seal region. *Id.*; *e.g.*, Ex. 1025 at Fig. 1, [0017]-[0019]; *KSR*, 550 U.S. at 416-418. A POSITA would have reasonably expected that this modification would be successful, for it would require no more than ordinary skill to implement. Decl. ¶ 226.

B. Dependent Claim 8

1. 8[pre]

Fujikawa and *Ikeguchi* render obvious claim 7. Section VIII.A; Decl. ¶ 227.

2. 8[a]-8[c]

As discussed, *Fujikawa* discloses or renders obvious these limitations. Sections VI.B.2-VI.B.4; Decl. ¶ 228. Alternatively, a POSITA would have been motivated to have a plurality of conductive points and a plurality of conductive particles on the second side to reduce non-display area, achieve reliable conduction, and improve display quality and stability in view of *Ikeguchi*. Sections VIII.A.4-VIII.A.6; Decl. ¶ 228. A POSITA would have had a reasonable expectation of success doing so. Sections VIII.A.4-VIII.A.6; Decl. ¶ 228.

C. Dependent Claim 9

1. 9[pre]

Fujikawa and *Ikeguchi* render obvious claim 8. Section VIII.B; Decl. ¶ 229.

2. 9[a]-9[c]

As discussed, *Fujikawa* discloses or renders obvious these limitations.

Sections VI.C.2-VI.C.4; Decl. ¶ 230. Alternatively, a POSITA would have been motivated to have a plurality of conductive points and a plurality of conductive particles on the fourth side to reduce non-display area, achieve reliable conduction, and improve display quality and stability in view of *Ikeguchi*. Sections VIII.A.4-VIII.A.6; Decl. ¶ 230. A POSITA would have had a reasonable expectation of success doing so. Sections VIII.A.4-VIII.A.6; Decl. ¶ 230.

D. Dependent Claims 10-12

Fujikawa discloses the additional limitations recited in claims 10-12.

Sections VI.D-VI.F; Decl. ¶ 231.

E. Independent Claim 13

1. 13[pre]-13[h]

Fujikawa discloses these limitations. Sections VI.G.1-VI.G.9; Decl. ¶ 232.

2. 13[i]-13[k]

These limitations are substantially similar to limitations 7[i], 7[j], and 7[k].

Sections VI.G.10-VI.G.12, VIII.A.4-VIII.A.6; Decl. ¶ 233. For the reasons noted above, *Fujikawa* and *Ikeguchi* render obvious these limitations. Sections VIII.A.4-VIII.A.6; Decl. ¶ 233.

3. 13[l]

Fujikawa and *Ikeguchi* render obvious this limitation. Section VIII.A.7; Decl. ¶ 234.

F. Dependent Claim 15

For the reasons identified for limitations 7[b], 7[d], and 7[i] *Fujikawa* and *Ikeguchi* render obvious the additional limitations in claim 15. Sections VIII.A.2, VIII.A.3, VIII.A.4, VI.H; Decl. ¶ 235.

G. Dependent Claim 16

Fujikawa discloses or at least renders obvious the additional limitation in claim 16. Section VI.I; Decl. ¶ 236.

H. Dependent Claim 17

For the reasons identified for limitations 7[b], 7[d], and 7[i] *Fujikawa* and *Ikeguchi* render obvious the additional limitations in claim 17. Sections VIII.A.2, VIII.A.3, VIII.A.4, VI.J; Decl. ¶ 237.

I. Dependent Claim 18

Fujikawa discloses the additional limitation in claim 18. Section VI.K; Decl. ¶ 238.

J. Dependent Claim 19

1. 19[pre]

Fujikawa and *Ikeguchi* render obvious claim 18. Section VIII.I; Decl. ¶ 239.

2. 19[a]-19[b]

For the reasons identified for limitations 7[i], 7[j], 7[k], 13[i], 13[j], and 13[k], and claims 8, 9, 15, and 17, *Fujikawa* and *Ikeguchi* renders obvious these limitations. Sections VIII.A.4-VII.A.6, VIII.E.2, VIII.B-VIII.C, VIII.F, VIII.H;

Decl. ¶ 240.

K. Dependent Claim 20

Fujikawa discloses the additional limitation in claim 20. Section VI.M; Decl. ¶ 241.

IX. *Fujikawa* In View of *Kang* and *Ikeguchi* Renders Obvious (Ground 5) Claims 7-13 and 15-20

For the reasons discussed in Ground 3 and Ground 4, *Fujikawa*, *Kang*, and *Ikeguchi* render obvious claims 7-13 and 15-20. Sections VII-VIII; Decl. ¶ 242.

X. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office’s interim guidelines dated June 21, 2022 (“Interim Procedures”) require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 6 requires institution because the merits of this Petition are strong. The Petition relies on materially different and non-cumulative primary references not applied during prosecution of the ’606 patent, which teach the very features the Applicant argued to be lacking during prosecution.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions less than three months ago, on March 11, 2024. Ex. 1022. *See, e.g., Fintiv* at 11

(“[I]t is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding.”); *Coolit Sys., Inc. v. Asetek Danmark A/S*, IPR2021-01195, Paper 10 at 11, 14 (PTAB Dec. 28, 2021) (finding petitioner acted diligently where it filed the petition within five months after PO provided contentions for nine patents). Fact discovery opened only last month, and the claim construction hearing will not take place until January 2025; therefore, the district court’s investment by institution will be nominal. Ex. 1021.

Factor 4 favors institution because this petition challenges claim 19, which is not involved in the litigation.

As to Factors 1, 2, and 5, Patent Owner filed its Complaint against Petitioner on November 8, 2023. Ex. 1020. No stay has been requested, trial is scheduled for June 2025, and the current median time-to-trial in the Eastern District of Texas is 21.4 months (Ex. 1023), so trial is projected to occur in August 2025 at the earliest. Ex. 1023. A FWD is anticipated by November 2025. In light of the Board’s holistic analysis balancing all *Fintiv* factors, however, the trial date of the related litigation is not determinative but weighed in concert with the other relevant factors. *See e.g., Netnut Ltd., v. Bright Data Ltd.*, IPR2021-01492, Paper 12 at 9-16 (PTAB March 21, 2022) (instituting review with trial date six months before final written decision deadline; no stipulation made); *Coolit*, Paper 10 at 11, 14 (same by five months;

Sand II stipulation); *Micron Technology, Inc., v. Vervain, LLC*, IPR2021-01550, Paper 11 at 9-13 (PTAB April 11, 2022) (same by approximately three months).

B. Denial of Institution Is Not Warranted Under § 325(d)

No other proceedings involving the '606 patent are currently pending or have been brought before the Office. Additionally, none of *Fujikawa*, *Kang*, or *Ikeguchi* was before the Examiner during prosecution of the '606 patent. Thus, the same or substantially the same prior art or arguments have not been previously presented to the Office and denial of institution is not warranted under § 325(d).

XII. Mandatory Notices

A. Real Parties-in-Interest

The real party-in-interest is BOE Technology Group Co., Ltd.

B. Related Matters

The '606 patent is currently asserted in *Longitude Licensing Ltd. v. BOE Tech. Group Co., Ltd.*, 2:23-cv-00515 (EDTX). The '606 patent was previously asserted in *Longitude Licensing Ltd. v. Sharp Corporation*, 2:23-cv-00165 (EDTX) but that case has since been voluntarily dismissed.

The '606 patent is a continuation of U.S. Patent Application No. 14/571,729 (“the '729 application”), which issued as U.S. Patent No. 9,459,498. '606 patent at Related U.S. Application Data. The '729 application is a divisional of U.S. Patent Application No. 11/301,086, which issued as U.S. Patent No. 9,599,861. *Id.* The '606 patent claims priority to Japanese Patent Application JP 2004-375697. The following patents and applications claim priority to the '606 patent—U.S. Patent Nos. 9,625,76 and 9,557,608, both of which are continuations of the '606 patent.

C. Lead and Back-Up Counsel, and Service Information

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Please address all correspondence to lead and back-up counsel at the addresses shown above. Petitioner consents to electronic service by email.

XIII. Grounds for Standing

Petitioner certifies the '606 patent is available for IPR and Petitioner is not barred or estopped from requesting an IPR challenging the claims on the grounds identified herein.

XIV. Conclusion

For the reasons above, Petitioner has established a reasonable likelihood that the challenged claims are unpatentable. Petitioner requests institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: June 6, 2024

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies the foregoing **Petition for *Inter Partes Review* of U.S. Patent No. 9,557,606** contains 13,935 words, excluding the parts of this Petition that are exempted under 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

Dated: June 6, 2024

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on June 6, 2024, a copy of the foregoing **Petition for *Inter Partes Review* of U.S. Patent No. 9,557,606, Petitioner's Power of Attorney and Designation of Lead and Back-up Counsel, and Exhibits 1001-1025** were served via overnight courier on June 6, 2024, on the correspondence address of record below indicated in the Patent Office's Patent Center for U.S. Patent No. 9,557,606.

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Dated: June 6, 2024

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