

# Design of a Passive UHF RFID Tag for Capacitive Sensor Applications

Kerem Kapucu, Jose Luis Merino Panadés, Catherine Dehollain

Institute of Electrical Engineering, RFIC Research Group

Ecole Polytechnique Fédérale de Lausanne (EPFL)

CH-1015, Lausanne, Switzerland

e-mail: kerem.kapucu@epfl.ch

**Abstract**— In this work, the design of a passive UHF RFID tag for sensor applications is described. The system level design issues are discussed taking into account the possible operation scenarios. Among the blocks in the tag, the emphasis is on the design of the rectifier and the capacitive sensor interface. The three-stage, differential-input rectifier is designed to generate the supply voltage with input levels as low as -13 dBm. The power conversion efficiency of the rectifier is 70%, driving a 30 k $\Omega$  load at -13 dBm source power. The fully-digital capacitive sensor interface designed to operate with a humidity sensor, can work with supply voltages as low as 0.8 V with good linearity and a power consumption of 12  $\mu$ W. The tag is capable of getting linear sensor readout under input power levels as low as -9 dBm. The circuits are implemented in 0.18  $\mu$ m UMC CMOS process.

**Index terms**—Radio frequency identification (RFID), passive RFID, wireless humidity sensor, food quality monitoring, UHF

## I. INTRODUCTION

In recent years there has been a growing interest in radio frequency identification (RFID) systems both in industry and academia. The application of RFID is very popular in many areas such as purchasing and distribution logistics, service industries, etc. [1]. RFID technology replaces the traditional barcodes by providing additional features such as adding sensing capabilities to tags. The addition of sensory capabilities to RFID tags can extend the applications of RFID to environmental monitoring and healthcare applications.

The FlexSmell European Marie-Curie Project ([www.flexsmell.eu](http://www.flexsmell.eu)) is among the efforts to use RFID technology in food quality monitoring. The project focuses on very low cost, ultra-low-power chemical sensing RFID tags to be used for food freshness and quality traceability control. This requires the addition of temperature, humidity and gas sensors on RFID tags.

In this work, the aim is to integrate a capacitive humidity sensor on a passive UHF RFID tag which is to be used in food quality monitoring applications. The emphasis is on the

system level design as well as the design of the rectifier and capacitive sensor interface. Section II will give an overview on the system level design issues. The design of the rectifier is discussed in Section III. In section IV, the capacitive sensor interface is described. Section V discusses the effects of backscattering on the performance of the rectifier and the sensor interface.

## II. SYSTEM DESIGN

In order to select the frequency of the RFID tag, a detailed description of the operation scenario is necessary. For food tracking, a possible operation scenario is as follows: an operator carrying a handheld RFID reader walks through the shelves in a depot. Each box of goods is packed with an RFID tag with sensors, which can detect the spoiled goods to be removed from the inventory. Such an operation scenario requires an interrogation range of 1-1.5 m as well as the capability of reading multiple tags at once. Moreover, the system should be as immune as possible to tag-reader alignment. Finally, the tags should be remotely powered for cost minimization.

The high-frequency (HF) RFID systems that operate at e.g. 13.56 MHz, lack the long interrogation range, since it is hard to transmit power to distances on the order of meters with reasonable sized antennas. For commercial HF RFID systems the operating range is generally limited to a few centimeters [1]. Moreover, the alignment of the tag and the reader is important for good inductive coupling between the tag and the reader coils. Therefore, an ultra-high-frequency (UHF) RFID system is the obvious choice for this project considering the possible operation scenarios. A tag antenna with a broad radiation pattern can generate immunity to tag-reader disorientation. Furthermore, the long range of UHF RFID systems allows for accessing multiple tags at once.

Considering the maximum allowed RF power levels, the 865.6-867.6 MHz ISM band is chosen for the system since it offers the highest allowed reader RF power (2 W e.r.p), which will result in the highest operating range. The design of the system is optimized for 866 MHz.

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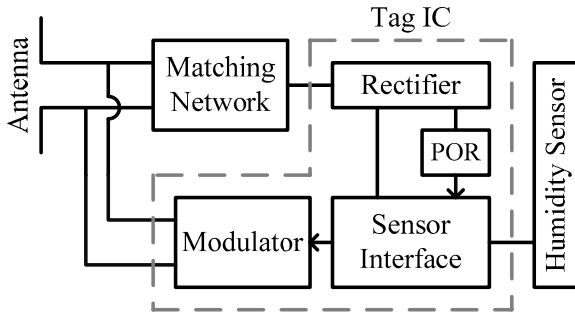


Figure 1. The block diagram of the RFID tag with humidity sensor

The power available at the tag antenna terminals can be calculated using the well-known Friis' transmission equation [2]. For example, for 2 W e.r.p source power at 866 MHz, and 0 dBi tag antenna gain, the available power at the tag antenna terminals is 4 dBm and 0.5 dBm at 1 m and 1.5 m, respectively for perfectly matched tag antenna.

Fig. 1 shows the block diagram of the RFID tag. The tag antenna is an inductively-fed meandered antenna whose impedance is designed to be the complex conjugate of the input impedance of the tag circuit [3]. However, a matching circuitry is added to compensate for the impedance variations between the designed and the manufactured values. The supply voltage is generated by a rectifier. A low-dropout voltage regulator (LDO) is not included in the tag because the capacitive sensor interface is immune to the changes in supply voltage value as discussed in Section IV. When the output of the rectifier settles, the power-on reset (POR) block generates a reset signal for the sensor interface. There is no receiver block in the tag, meaning that the tag will operate without any addressing as soon as enough voltage is generated from the incoming electromagnetic wave.

The tag IC is designed to operate with a capacitive humidity sensor, which has an offset value of 5 pF and a range of 1.5 pF. The value of the capacitance increases from 5 pF to 6.5 pF as the relative humidity increases from 0% to 100%.

### III. RECTIFIER

The RF-to-DC converter of the tag consists of the antenna, the matching network, and the rectifier. In this work, the emphasis is on the design and implementation of the rectifier.

The power conversion efficiency (PCE) of a rectifier is defined as the percentage ratio of the rectifier output power to the rectifier input power [4]. The PCE of a rectifier depends on several parameters such as the circuit topology, the RF input power and frequency, the output load, and the threshold voltages of the diodes (or the diode connected transistors [5]). The threshold voltage of the diodes should be minimized in order to have a high PCE. For this purpose, Schottky diodes are commonly utilized in rectifiers [6].

In this work, the utilization of exotic technology nodes such as silicon on sapphire, and expensive process options such as Schottky diodes are avoided since the aim is to achieve a low-cost system. The rectifier is implemented using

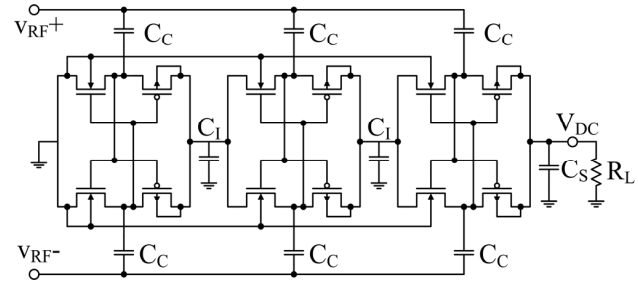


Figure 2. The circuit schematic of the three-stage differential-input rectifier with active threshold cancellation

the MOSFET transistors in UMC 0.18 $\mu$ m technology. However, MOSFETs have higher threshold voltages than Schottky diodes, which results in lower PCEs. Therefore, the active threshold voltage compensation technique proposed in [5] is used, which performs better than the previous static threshold compensation techniques.

The circuit schematic of the three stage rectifier is given in Fig. 2. The rectifier design is optimized at 866 MHz for a maximum load ( $R_L$ ) of 5 k $\Omega$ . The gate widths of the NMOS transistors are designed to be 8  $\mu$ m, whereas the gate lengths are designed to be 240 nm. Keeping a width ratio of 5 between NMOS and PMOS transistors, the gate widths of the PMOS transistors are designed to be 40  $\mu$ m, whereas the gate lengths are designed to be 240 nm. Interstage smoothing capacitors ( $C_I$ ) are 100 fF each, whereas the coupling capacitors ( $C_C$ ) are 1.13 pF. The storage capacitor ( $C_S$ ) at the output is chosen to be 200 pF. The rectifier needs only 4.35  $\mu$ s to achieve the 95% of the final voltage with a -9dBm RF input.

For simulations, perfect impedance matching between the antenna and the rectifier at -5 dBm source power with 10 k $\Omega$  load is assumed and the RF input power is swept keeping the source impedance constant. In other words, the antenna impedance is not changed at each power level to have perfect matching at every step of the input power sweep. This is more realistic since an adaptive impedance matching scheme will not be utilized in the final RFID tag.

The variation in PCE with respect to RF input power levels between -25 dBm and 0 dBm for three different load conditions are shown in Fig. 3(a). As the load resistance increases, the highest PCE is obtained at lower input power levels. The maximum PCE of 70% is achieved for 30 k $\Omega$  load at -13 dBm RF input power, where the output of the rectifier is 0.8 V. This corresponds to a distance of 4.5 m from the reader for 2 W e.r.p source power and a perfectly matched 0 dBi tag antenna. Fig. 3(b) shows the rectifier output voltage with respect to RF input power for four different load conditions. An RF input power of -6 dBm is necessary to generate 1.8 V at the rectifier output for 30 k $\Omega$  load, which corresponds to a distance of 2.8 m from the reader.

The change in the performance of the circuit due to process variations is characterized by means of corner simulations. The power conversion efficiency at 0 dBm input power changes by less than 2% and the 1.8 V output voltage changes by less than 3 mV as a result of simulating the circuit

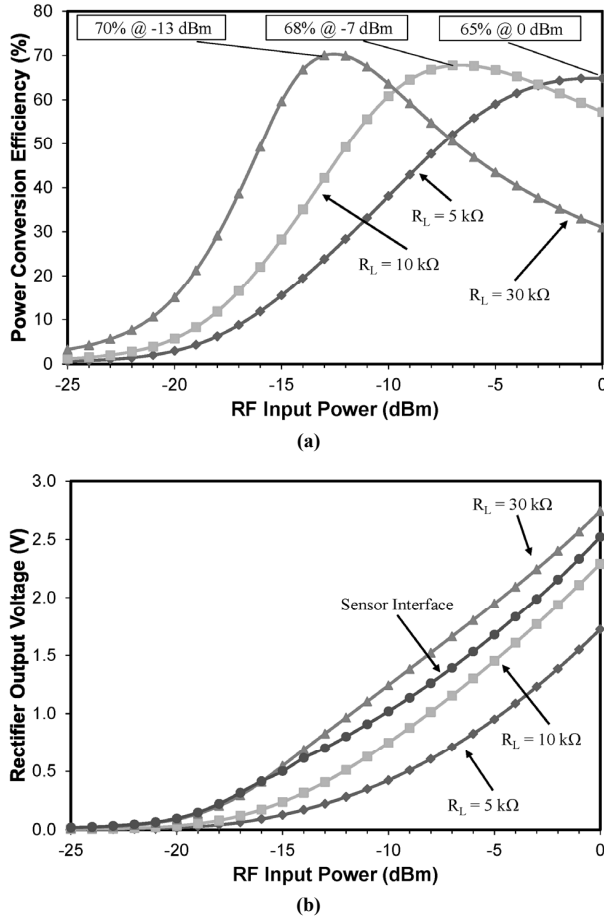


Figure 3. (a) Power conversion efficiency and (b) output voltage of the rectifier as a function of RF input power for different loads

at different technology corners with a  $50 \text{ }\Omega$  power source and fixed matching. The drop in rectifier efficiency in slow-slow corner is less than 10%, for input power levels greater than -5 dBm, whereas the fast-fast corner always results in higher efficiencies.

#### IV. CAPACITIVE SENSOR INTERFACE

The traditional approach for a capacitive sensor interface consists of an analog signal conditioning block such as an instrumentation amplifier and an analog-to-digital converter such as in [7]. In this work, a fully-digital capacitive sensor interface similar to the one proposed in [8] is used. Fig. 4 shows the block diagram of the capacitive sensor interface. The sensor interface is a basic PLL structure consisting of two oscillators and a phase detector. Both oscillators are asymmetrically loaded, five-stage ring oscillators. The sensor oscillator has the capacitive sensor as the load of one of its stages, whereas the digitally controlled oscillator has a switchable capacitive load. The digitally switched capacitive load consists of two capacitors, denoted as  $C_0$  and  $C_m$ . The capacitor  $C_0$ , which refers to the offset value of the sensor, is always connected to the ring oscillator. On the other hand,  $C_m$ ,

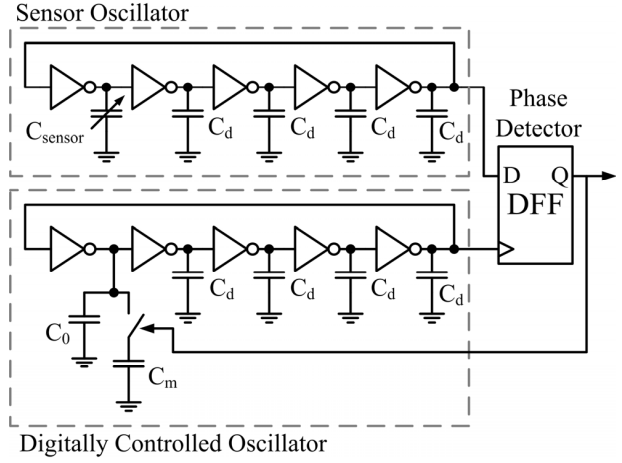


Figure 4. The block diagram of the PLL based capacitive sensor interface

which refers to the change in the sensor capacitance, is connected to and disconnected from the ring oscillator by means of a switch.

The switch is controlled in a feedback manner by the output of the phase detector, which is a pulse train that corresponds to the phase difference between the output signals of the two ring oscillators. It is clear that this structure is a simple PLL due to the feedback loop, and the output of the phase detector is a pulse train whose average value is proportional to the variation in the sensor value.

The capacitor  $C_0$  is selected as 5 pF, which is equal to the offset value of the sensor capacitance and the digitally switched capacitor  $C_m$  is selected to be higher than the range of the sensor capacitance. The selection of the value of  $C_m$  is discussed in Section V. In the physical implementation, the digitally switched load capacitor is implemented as a programmable capacitor, whose value can be trimmed after the chip is manufactured. The dummy load capacitors ( $C_d$ ) at each stage are chosen to be 1 pF.

The phase detector is simply a D Flip-Flop, with the output of the sensor oscillator connected to the data input and the output of the digitally controlled oscillator is connected to the clock input. The output of the phase detector is used as the feedback control signal that switches on and off, the digitally switched load capacitor. Although not shown in the figure, the output of the phase detector is buffered in the physical implementation to obtain a signal with sharper transitions. The control signal is actually a pulse train with a duty cycle that is proportional to the change in the sensor capacitance value [8]. In other words, the average value of the control signal is proportional to the change in the sensor capacitance. In the RFID system, this signal will be modulated and sent to the reader by backscattering.

This architecture has an inherent immunity to supply voltage variations due to the fact that the measurement is done in a differential manner, i.e., the phase difference of two oscillations that are supplied from the same voltage source is measured. This gives an advantage over the absolute

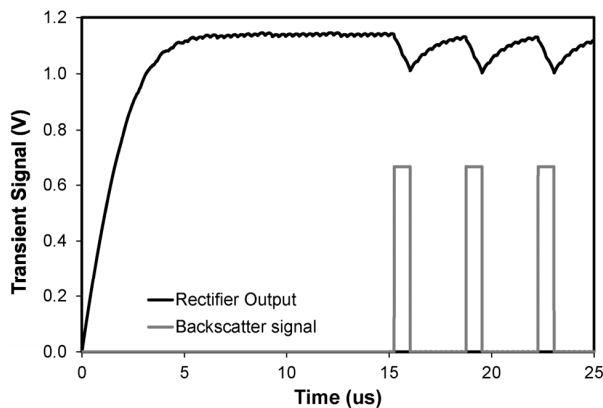


Figure 5. The output of the rectifier and the output of the sensor interface, i.e., the backscatter signal.

frequency measurement methods in terms of power supply rejection.

## V. BACKSCATTERING EFFECTS

The data is sent from the tag to the reader by backscattering, i.e., the antenna inputs are shorted to ground when a digital high level is being sent. This results in a voltage drop at the rectifier output as seen in Fig. 5. As discussed in Section IV, the effect of the supply voltage drop on the capacitive sensor interface circuitry is minimal due to its differential nature, because the sensor oscillator and digital controlled oscillator are affected the same. The rectifier output voltage with respect to input power when the sensor interface is operating is given in Fig. 3b. The rectifier generates a stable supply voltage with input power levels as low as -13 dBm, which corresponds to a distance of 7.1 m from the reader.

The response of the sensor interface is linear with respect to the sensor value, up to half the sensor range for different RF input values and supply voltages as shown in Fig 6. However, the rectifier cannot recover its initial voltage value with a backscattering signal with more than 50% duty-cycle. This reduces the performance of the sensor interface.

The solution to maintain the linearity for all the operating range is to choose the  $C_m$  value to be 3.2 pF, twice the maximum value of  $C_s$ , to keep the duty cycle of the output lower than 50%. By this way, the rectifier output can be kept stable. Of course, there is a trade-off between linearity and sensitivity. With this solution, the sensitivity is reduced, but a highly linear response is obtained for a wide range of RF input power levels.

Using two different input power levels (-5 & -9 dBm) a sensitivity of 0.379 duty cycle per pF is obtained with a  $R^2$  linearity factor of 0.9956. Those results allow determining the value of capacitance by analyzing the average of the

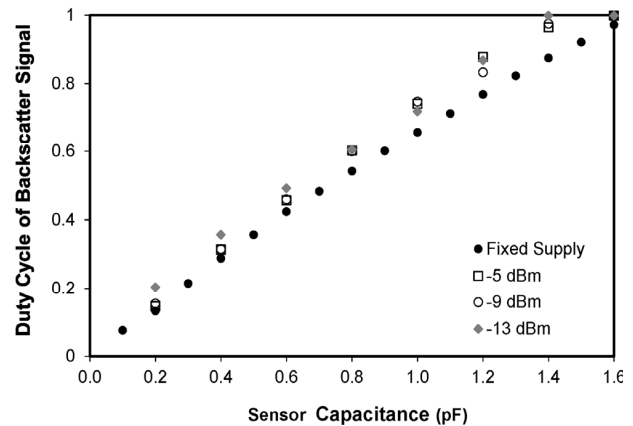


Figure 6. The response of the sensor interface with respect to the sensor value for different RF input power levels. The response is linear up to half the sensor range.

backscatter signal with average and maximum deviances of, respectively, 1.7% and 5.1% of the measured capacitance.

## VI. CONCLUSION

The system level design of a passive UHF RFID tag to be used in sensor applications has been described. The design and implementation of the rectifier and the PLL-based capacitive sensor interface is detailed. It is shown by simulations that the rectifier can reach a maximum PCE of 70% for 30 k $\Omega$  load at -13 dBm RF input power. The fully-digital sensor interface can operate with 0.8 V supply voltage consuming only 12  $\mu$ W. The tag can send linear sensor readout by backscattering at -9 dBm RF input power, which corresponds to a 4.5 m tag-reader distance for 2 W e.r.p source power and 0 dBi tag antenna.

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