

**UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE
PATENT TRIAL AND APPEAL BOARD**

IKEA Supply AG

Petitioner

v.

Everlight Electronics Co., Ltd.,

Patent Owner

U.S. Patent No. 7,554,126 to Higashi *et al.* IPR Case No.: IPR2024-00988

Declaration of Dr. Michael S. Lebby

Regarding U.S. Patent No. 7,554,126

Ex-1003 – Declaration of Dr. Michael S. Lebby Regarding U.S. Patent No. 7,554,126

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1. Introduction and Summary of Opinions

1. My name is Michael S. Lebby. I have been retained as an expert witness by counsel for Petitioners IKEA Supply AG (“IKEA”) in the above captioned proceeding. I have been asked to provide my opinion regarding the validity or invalidity of the U.S. Patent No. 7,554,126 (“the ’126 patent”) purportedly assigned to Patent Owner Everlight Electronics Co., Ltd. (“Everlight”). My analysis in this report relates to claims 1-2 & 4-13 of the ’126 patent (collectively, the “Challenged Claims”).

2. It is my opinion that claims 1, 2, and 5-12 of the ’126 patent are anticipated by Japanese Patent Publication No. 2004103975 (“Terashima”) (Ex-1004).

3. It is my opinion that claims 1, 5-6, 9 and 12 of the ’126 patent are anticipated by United States Patent Application Publication no. US 2004/0159836 (“Sugimoto”).

4. It is my opinion that claims 1, 2, 5, and 7-10 of the ’126 patent are obvious over U.S. Publication No. 2004/0256631 (“Shin”) in view of one or more of what I refer to as the “Thin Film Art” (i.e., Terashima, Sugimoto, U.S. Application Publication No. US 2003/0160259 (“Uemura ’259”), U.S. Application Publication No. US 2004/0149999 (“Uemura ’999”), and U.S. Patent No. 6,333,522 (“Inoue”).

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5. It is my opinion that claim 4 of the '126 patent is obvious over either (i) Terashima; or (ii) Shin and one or more of the Thin Film Art in view of U.S. patent application no. US 2005/0194605 ("Shelton").

6. It is my opinion that claim 5 of the '126 patent is obvious over Terashima in view of Shin, Sugimoto, or Inoue.

7. It is my opinion that claim 6 of the '126 patent is obvious over (i) Terashima; (ii) Shin one or more of the Thin Film Art; or (iii) Sugimoto in view of Shelton and/or the level of ordinary skill in the art.

8. It is my opinion that claim 7 of the '126 patent is obvious over (i) Terashima; (ii) Shin one or more of the Thin Film Art; or (iii) Sugimoto in view of Shelton and/or the level of ordinary skill in the art.

9. It is my opinion that claim 8 of the '126 patent is obvious over (i) Terashima; (ii) Shin one or more of the Thin Film Art; or (iii) Sugimoto in view of Shelton and/or the level of ordinary skill in the art.

10. It is my opinion that claim 11 of the '126 patent is obvious over (i) Sugimoto; or (ii) Shin one or more of the Thin Film Art in view of Terashima and/or the level of ordinary skill in the art.

11. It is my opinion that claim 12 of the '126 patent is obvious over Shin one or more of the Thin Film Art in view of Terashima, Sugimoto, and/or the level of ordinary skill in the art.

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12. It is my opinion that claim 13 of the '126 patent is obvious over (i) Terashima; (ii) Sugimoto; or (iii) Shin plus one or more of the Thin Film Art in view of Shelton and/or the level of ordinary skill in the art.

13. It is my opinion that claims 1, 2, and 4-13 of the '126 patent are obvious over Terashima as applied above in view of one or more of the Thin Film Art minus Terashima and/or the level of ordinary skill in the art.

14. This report contains a statement of the opinions that I have formed regarding the validity/invalidity of the Challenged Claims to date and provides the bases and reasons for my opinions. I have provided my opinion as to the level of skill of a person of ordinary skill in the art (POSITA) and a POSITA's common general knowledge at the time of the alleged invention, which I understand to be 2004 based on the priority claim of the '126 patent. I may offer additional opinions based on further review of materials in this proceeding, including opinions and/or testimony of other experts, including those of Everlight.

15. I am being compensated for my time in connection with this matter at my standard hourly rate of \$450/hour. My compensation is not affected by my opinions or the outcome of this proceeding. I do not have any financial interest in the outcome of this proceeding.

16. I reserve the right to amend and/or supplement my opinions to respond to any declarations, reports, or testimony from any of Everlight's expert(s) or

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witnesses; any briefs or pleadings that Everlight may file; any other filings relating to validity/invalidity of the Challenged Claims, any proposals regarding the level of skill of a POSITA, and/or the interpretation of claim terms that are proposed by Everlight or the Patent Trial and Appeal Board (“the Board”). I also reserve the right to prepare and rely on demonstrative exhibits concerning the opinions and their bases as an aid for trial or to assist the Board in connection with this proceeding.

2. Summary of My Qualifications

2.1 Education, Employment, and Research

17. I am currently the CEO of Lightwave Logic, a company engaged in developing optical polymer modulators for the fiber optic communications industry (including both data communications and telecommunications). I am also the CEO and CTO of Oculi LLC, where I perform expert witness consulting concerning photonics, optoelectronics, semiconductors, and fiber optic equipment technology. I am also currently a technical expert for the Photonics Unit of the European Commission, where I participate in organizing workshops and lectures, evaluating photonics proposals, and advising the European Commission on projects. I was voted the Photonic Integrated Circuits Conference Entrepreneur and Business Leader of the Year in March 2018.

18. A copy of my curriculum vitae (CV) is attached as Exhibit XXXX. As set forth more fully in my CV, over the course of my 40-year career in

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optoelectronics, I have worked in nearly every aspect of optoelectronics, including light-emitting diodes (“LEDs”), LED packaging, and LED fabrication. Accordingly, I have experience and expertise relating to epitaxial wafer growth, LED/device fabrication, implementation of LEDs/devices into packages, and packaging materials such as plastics, metallic-based, semiconductor-based, and ceramic-based. I have also designed LED/device packages (e.g., through-pin, surface mount, flip-chip and various combinations thereof) for printed circuit board mounting. Many of the designed packages were implemented in modules and sub-system/luminaire applications, i.e., fixtures in which LED packages are incorporated. The modules have been fiber-optic, display, lighting, and sensing-based. For example, I have designed optoelectronic devices such as LEDs, laser diodes, photodiodes, and solar cells, with a focus on efficient optical device design that maximizes LED/device performance.

19. I am a chartered engineer in the United Kingdom, which is a status equivalent to a United States professional engineer. I started my career in 1977 at the Ministry of Defense (United Kingdom) in the Royal Electrical and Mechanical Engineer division as a telecommunications apprentice. At the Ministry of Defense, I also studied material and characterization issues of Gallium Arsenide (GaAs) and Indium Phosphide (InP) optoelectronic devices as well as semiconductor device design, fabrication, and characterization, and particularly with materials using III-V

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semiconductors. I also worked on ceramic-based radiofrequency (RF) electronic packaging that included low-temperature co-fired ceramic.

20. I attended the University of Bradford, where I obtained a Bachelors of Engineering (Electrical Engineering), with honors, in 1984, an M.B.A. in 1985, and a Ph.D. (Electrical Engineering) in 1987. My Ph.D. thesis related to the characterization and fabrication of both optoelectronic and electronic semiconductor devices. In 2004, I was awarded a Doctor of Engineering (a Doctorate degree higher than a Ph.D.) from the University of Bradford for my “Technical Contributions to Optoelectronics.” This was only the second time in the University of Bradford’s history that a Doctor of Engineering was granted based on industry experience.

21. At the same time, I attended the University of Bradford and afterward from 1985 to 1989, I worked as a researcher in the Photonics Research Department of AT&T Bell Labs (“Bell Labs”). At Bell Labs, I focused my research on novel device designs using III-V semiconductor material systems that included FETs, bipolar transistors, LEDs, laser diodes, and photodetectors. My research at Bell Labs became the subject of my Ph.D. thesis.

22. After I completed my Ph.D. at the University of Bradford and my work at Bell Labs, I became a Research and Development Manager (“R&D Manager”) in the photonics division of Motorola’s Corporate R&D Labs from 1989 to 1998. My responsibilities at Motorola included research and development of optical

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interconnects, displays, LEDs, and laser devices, as well as the packaging and reliability of mobile product prototypes. While at Motorola, I was the inventor or co-inventor of over 150 utility patents. In 1998, I received a special award from the Chairman of Motorola for exemplary patent accomplishments. At that time, I had the highest number of issued utility patents in the history of Motorola.

23. LEDs, LED packaging, and LED fabrication were an integral part of my work at Motorola. In the early 1990s, full-color LED displays were not viable. Mature LED technologies at the time included Phosphide (Gallium Arsenide Phosphide (GaAsP) and/or Aluminum Indium Gallium Phosphide (AlInGaP)) and Aluminum Gallium Arsenide (AlGaAs)-based LEDs that produced visible red and orange colors with good emission properties. Gallium Phosphide (GaP)-based LEDs that produced a green color had low emission output. Bluewavelength emission LEDs were only available using pure Silicon Carbide (SiC) on Silicon Carbide (SiC) substrate wafers, with extremely low emission output. I worked closely with Motorola's mobile divisions on new and novel display prototypes to research and develop how best to innovate with full color red, green, and blue displays. In the early 1990s, single (red wavelength) and dual (orange and red wavelength) color displays were designed and made into LED packaged prototypes. After consumer testing, it was found that full-color LED displays were more attractive and then a number of alternative technologies were evaluated, such as Liquid Crystal Displays

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(LCDs), organic LEDs (OLEDs), and, in the late 1990s, Gallium Nitride (GaN) and Indium Gallium Nitride (InGaN) materials grown onto Sapphire. I designed packages for these devices, which included standard Transistor Output (TO) cans, over-molded plastic dual in-line (DIL) solutions, and ceramic and semiconductor-based technology.

24. As an R&D Manager at Motorola, I worked on a number of other projects, with a particular interest in miniature displays using technologies such as LEDs, organic LEDs, lasers, and LCDs, as well as technological problems related to package lenses and molding unique and innovative shapes. One of the devices I worked on at Motorola was the Vertical-Cavity Surface-Emitting Laser (“VCSEL”). This device design required special attention to optical efficiency and distributed Bragg reflectors (“DBR”), as well as transparent packaging similar to the approach in LED packaging. I also initiated Motorola’s work in optical interconnect (Optobus™) technology, and I was involved in research and development of the IC chip designs that this parallel interconnect module utilized. In this project, transparent plastics were developed and process over-molded onto standard metallic lead frames for both light-emitting devices (e.g., LEDs, VCSELs) as well as photodetectors, which collect light and convert it into an electronic signal. These transparent lead frame packages were developed in volume production at Motorola.

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25. I also worked on GaAs-based LED opto-couplers, which are optoelectronic packages that optically isolate the LED from a photodetector in a plastic package. These optoelectronic packages are usually designed with either a glass transparent plate or transparent organic polymer positioned between the LED and the photodetector. My work at Motorola also addressed full color display and display electronics composed of red, green, and blue LEDs, and specifically how to package these technologies to allow for high electrical, optical, and thermal performance. I also worked with displays that included large arrays of visible LEDs (i.e., 10,000 LEDs on a chip) and phosphor technology. I also worked on photonics prototypes, which were subject to optimized optical device design and optical/transparent packaging, and consumer products that utilized LEDs in opto-coupler, display, and imager platforms that were all driven using standard electronic ICs and electronic signaling, as well as packages that included transparent plastic packaging varieties where the transparent plastic material was molded to a variety of conventional stamped metallic lead frames and flexible tape automated bonding (TAB) using materials such as Kapton®.

26. In 1998, I left Motorola to join TE Connectivity (previously Tyco Electronics) as Director of Technology and Business Development, where I helped develop technology strategy for optical communications products for the Global

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Optoelectronics Division. My work included designing and characterizing LED- and laser-based packages and modules for customer qualification specifications.

27. In 1999, I joined Intel Capital (“Intel”) as Director of Business Development, and also as a corporate investor. My work at Intel included sourcing, negotiating, and closing private placement equity deals in the optical networking, component, and semiconductor industries. My work at Intel also included investigating the investment in photonic devices, packaging, and modules, as well as LEDs, lasers, and displays. I also was one of the founders of Intel’s silicon photonics division, which worked to establish a fabrication facility in South San Jose to investigate the integration of silicon FET electronics with optoelectronics into the same silicon semiconductor wafer.

28. From 2005 to 2010, I became the Executive Director, President, and CEO of the Optoelectronic Industry Development Association (OIDA), a trade association that represented photonics manufacturers in the fields of fiber optics, display, sensing, defense, aerospace, LED lighting, and motor vehicles. I was responsible for organizing technical conferences, workshops, and forecasts using industry roadmaps that featured LEDs, fiber optics, optics, fiber, optical sensors, displays, and their associated packaging.

29. In 2010, I became the General Manager and CTO of Translucent, Inc., a start-up company that developed and manufactured silicon and rare earth oxide-

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based epitaxial semiconductor wafers. Part of my work there was to help develop novel platforms for the growth of GaN and InGaN onto silicon and the growth of single crystal layers of GaN/InGaN/AlN onto single crystal rare earth oxides for LED fabrication. I also researched various epitaxial semiconductor layer structures for improved LED performance during my time at Translucent.

30. I joined Glyndŵr University from 2013 to 2015 as a Professor of Optoelectronics, where I focused on the design, simulation, and testing of 100G/400G photonic integrated circuits, optoelectronic integrated circuits, laser diodes, optics, and solar cells.

31. From 2013 to 2015, I was also the President and CEO of OneChip Photonics Corporation, where I served as an elected independent board member focusing on the technical and business operational strategy for communications based on InP photonic integrated circuits and optoelectronic integrated circuits.

32. Over the course of my career, I have also given a number of peer-reviewed presentations, speeches, and talks at workshops and conferences, including on optoelectronic devices, optoelectronic components, and packaging technology.

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2.2 Patents

33. I am a named inventor of over 200 issued patents or published patent applications, as set forth more fully in my CV. I am a named inventor of the following exemplary patents relating to LEDs, LED packaging, and LED fabrication:

34. U.S. Patent No. 5,416,870, entitled Optoelectronic interface device and method with reflective surface, issued May 16, 1995;

35. U.S. Patent No. 5,708,280, entitled Integrated electro-optical package and method of fabrication, issued January 13, 1998;

36. U.S. Patent No. 5,358,880, entitled Method of manufacturing closed cavity LED, issued October 25, 1994;

37. U.S. Patent No. 5,563,900, entitled Broad spectrum surface emitting LED, issued October 8, 1996;

38. U.S. Patent No. 5,699,073, entitled Integrated electro-optical package with carrier ring and method of fabrication, issued December 16, 1997;

- U.S. Patent No. 5,741,724, entitled Method of growing gallium nitride on a spinel substrate, issued April 12, 1998;
- U.S. Patent No. 5,739,800, entitled Integrated electro-optical package with LED display chip and substrate with drivers and central opening, issued April 14, 1998;

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- U.S. Patent No. 5,818,404, entitled Integrated electro-optical package, issued October 6, 1998; and
- U.S. Patent No. 7,605,531, entitled Full color display including LEDs with rare earth active areas and different, issued October 20, 2009.

2.3 Publications

39. I have authored or co-authored numerous publications, which are set forth fully in my CV. I am an author or co-author of the below exemplary publications relating to LEDs, LED packaging, and LED fabrication:

- F. Erdem Arkun, Rytis Dargis, Andrew Clark, Robin S. Smith, Michael S. Lebby, Jeffrey M. Leathersich and F. Shahedipour-Sandvik, *Growth of GaN by MOCVD on Rare Earth Oxide on Si(111)*, ECS Transactions, Oct. 31, 2013.
- Rytis Dargis, Andrew Clark, Erdem Arkun, Radek Roucka, David Williams, Robin S. Smith, and Michael S. Lebby, *Epitaxial Si and Gd₂O₃ Heterostructures – Distributed Bragg Reflectors with Stress Management Function for GaN on Si Light Emitting Devices*, ECS Transactions, 2013.

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- F. Erdem Arkun, Rytis Dargis, Robin Smith, David Williams, Andrew Clark, Michael S. Lebby, *Integrated High Reflectivity Silicon Substrates for GaN LEDs*, Physica Status Solidi, Jan. 13, 2012.
- David Williams, Andrew Clark, Erdem Arkun, Aleta Jamora, Gary Vosters, Michael S. Lebby, *Silicon Light Emitting Device Based on Rare Earth Oxide Superlattice*, 7th IEEE International Conference on Group IV Photonics, Beijing, China, Sep. 2010.
- Wenbin Jiang, Michael S. Lebby, *Packaging of Optical Components and Systems*, Wiley Encyclopedia of Electrical Electronics and Engineering, 27 Dec., 1999.
- Wenbin Jiang, Michael S. Lebby, *Semiconductor Laser and Light Emitting Diode Fabrication*, Handbook of Fiber Optic Data Communication, February 2002.

2.4 Prior Testimony

40. I have previously served as a testifying expert witness in patent cases as set forth more fully in my CV. I have been recognized as an expert in the LED field including LED packaging in numerous jurisdictions and by the USPTO in invalidity proceedings including:

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- *Jiaxing Super Lighting Electric Appliance Co., LTD and Obert Inc. v. Current Lighting Solutions, LLC d/b/a GE Current.*, No. 6-22-CV-00534-ADA (W.D. Tx Filed 16th Sep 2022);
- *LG Electronics Inc., v. TCL Electronics Holdings Ltd. (f/k/a TCL § Multimedia Technology Holdings, Ltd.) et al.*, No. 2-22-CV-0122-JRG (W.D. Tx. Filed 14th Oct 2022);
- *Amazon.com Inc., v. Epistar Corp.*, No. 6-22-CV-00526-ADA (W.D. Tx. Filed 24th May 2022)
- *Certain integrated circuits, and electronic devices and products containing the same*, No. 337-TA-1287 (ITC Filed 1st Dec 2021);
- *LedComm LLC., v. IKEA US Retail LLC et al.*, No. 6-22-CV-00302-ADA (W.D. Tx. Filed 21st Mar 2022);
- *Jiaxing Super Lighting Electric Appliance Co., LTD and Obert Inc. v. Maxlite Inc.*, No. 19-CV-04047 (C.D. Cal. Filed 8th May 2019); and
- *Cree Lighting, Wolfspeed, Ideal Industries Lighting, v. CAO Lighting*, No. IPR2022-00848 (PTAB Filed 8th April 2022).

2.5 Expertise

41. Based on my education and experience, I consider myself to be an expert in the fields of LED and LED packaging related to the technologies described and claimed in the '126 patent.

3. Person of Ordinary Skill in the Art (POSITA)

42. I understand that validity/invalidity are determined from the perspective of a person of ordinary skill in the art, or POSITA, at the time of the alleged invention. I understand the alleged invention date to be the earliest effective filing date of the application that issued as the '126 patent, which I understand to be September 22, 2005.

43. In determining the appropriate level of ordinary skill for a POSITA, my understanding is that the following factors can be considered: the inventor's educational background and experience, the types of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made in the art, the sophistication of the technology, the educational background and experience of those working in the art, and the like.

44. After a review of the '126 patent, I am of the opinion that a POSITA at the relevant time of the alleged invention of the '126 patent would have had (1) a Bachelor's degree in electrical engineering, physics, or a comparable field of study, and (2) at least three years of professional experience with semiconductor optoelectronic devices that includes designing/analysis, mounting, manufacturing, and packaging. This description is approximate, and a higher level of education or skill might make up for less experience, and additional experience could make up

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for a lower education level (for example, an M.S. in any of the above fields and two years of practical experience would qualify one as a POSITA).

45. I consider myself to be a person of at least ordinary skill in the art for the '126 patent. As of 1988, I had a Bachelor's degree in electrical engineering and at least three years of professional experience with semiconductor optoelectronics devices and packaging, including LED leadframe manufacturing and design. I received a Bachelor's degree in electrical engineering in 1984 and by no later than 1988, had at least three years of professional experience with semiconductor optoelectronics devices and packaging through my Ph.D. and post-doctoral research performed at Bell Labs (thesis related to the characterization and fabrication of optoelectronic and electronic semiconductor devices).

4. Materials Considered

46. I have considered information from various sources in forming my opinions. Besides drawing from more than forty-year career in optoelectronics, I have also reviewed the '126 patent, its file history, IKEA's Petition for *inter partes* review ("Petition"), each exhibit attached to the Petition, and any other documents or references discussed in this declaration.

5. Legal Standards Applied in the Report

47. I am not an attorney and will not offer opinions on the law. I was asked to apply the following legal standards in forming my opinions.

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48. I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made. My understanding of the legal standards for anticipation and obviousness are set forth below.

49. I was instructed that IKEA has the burden of proving that the Challenged Claims of the '126 patent are anticipated by or obvious in view of the prior art by a preponderance of the evidence in this proceeding. I was instructed that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not. I used that standard in my analysis.

50. I was instructed to evaluate whether an invention is new and not obvious in view of the legal standards below and what is referred to as “prior art.” I understand that “prior art” generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.) that existed before the earliest filing date (the “effective filing date”) of the claims in the '126 patent. I understand that whether a printed document qualifies as prior art to the '126 patent is a legal conclusion, so I was asked to assume for my analysis that the documents applied in my report are prior art to the Challenged Claims.

51. I was instructed that in my anticipation and obvious analysis, I should compare the Challenged Claims to the prior art. I was instructed that in this analysis, the '126 patent claims must be interpreted in accordance with certain standards of

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claim construction. I was instructed that claim construction is a question of law for the Court to decide. The claim construction I was asked to use is provided below.

5.1 Anticipation

52. I was instructed that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art. I have applied these standards in my evaluation of whether the claims of the patent would have been anticipated by the prior art.

53. I was instructed that, for a patent claim to be “anticipated” by the prior art, each and every limitation of a claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that a prior art reference inherently discloses a claim limitation if the claim limitation is necessarily present or the natural result of the combination of elements explicitly disclosed in the prior art reference. I understand that the inherency inquiry is distinct from the question of obviousness.

54. I was instructed that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

5.2 Obviousness

55. I was instructed that a claimed invention is not patentable if it would have been obvious to a POSITA at the time the invention was made.

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56. I was instructed that a patent may not be obtained even though the invention is not identically disclosed or anticipated by the prior art, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which said subject matter pertains.

57. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the patent at issue here would have been considered obvious as of the relevant priority date. I have been asked to assume that the priority date for the claims at issue here is September 27, 2004.

58. I understand that to find a claim in a patent obvious, one must consider certain factual questions regarding the claimed invention and the prior art. Specifically, I understand that the question of whether an alleged invention is obvious requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The level of ordinary skill in the art/knowledge of a POSITA; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case (commonly referred to as “secondary considerations of non-obviousness”).

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59. In addition, I understand that the obviousness inquiry should not be done based on hindsight, but must be done using the perspective of a POSITA as of the priority date of the patent claim.

60. I was instructed that the secondary considerations of non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors” suggesting the claimed subject matter is not obvious, and reserve my right to address any such evidence if it is identified in the future. I understand that objective factors of obviousness include near simultaneous invention by another.

61. I understand that an indication of obviousness is the combination of familiar elements according to known techniques to yields predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or

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design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product, not of innovation, but of ordinary skill and common sense

62. I also understand that if a POSITA can implement a predictable variation, that variation may be considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using that technique to improve the other device is an indication that the technique would have been obvious unless its actual application yields unexpected results or challenges in implementation.

63. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can consider the “ordinary innovation” and experimentation that yields predictable results, which include inferences and creative steps that a POSITA would employ.

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64. I understand that, to make an obviousness determination, it will sometimes be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. It is my understanding that motivation to combine prior art to form the claimed invention includes motivation or suggestions in a reference, common sense, the level of ordinary skill, and motivation derived from the nature of the problem to be solved.

65. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

5.3 Claim Construction

66. I understand that the claim construction is for the USPTO. I understand that a claim construction order was recently issued in the Walmart-Everlight Litigation (Ex-1015). I have applied those constructions here (Ex-1015). To the extent that the claim is definite, I apply the plain and ordinary meaning of the claims to a POSITA.

6. Technical Background

67. In this section, I describe engineering that was well-known to a POSITA prior to 2004.

6.1. Light Emitting Diodes (LEDs)

68. A light-emitting diode (LED) is a semiconductor die that emits light when electric current flows through it. LEDs are well-known semiconductors dating back to as early as 1907.

69. LEDs can be made from a variety of semiconductor materials to emit different colors of visible light. For example, red LEDs, which were first introduced in the 1970s, can be made from Gallium Arsenide Phosphide (GaAsP), Gallium Phosphide (GaP), and Aluminum Gallium Arsenide (AlGaAs). Yellow LEDs, also demonstrated as early as 1972, can be made from GaAsP, GaP, and Aluminum Indium Gallium Phosphide (AlInGaP). Blue LEDs were made commercially available in 1989.

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70. The '126 patent teaches that n-electrodes can be fabricated with larger electrode surface areas to ease the alignment and placement accuracy needed to flip-chip the LED chip to a printed circuit board or substate (*see e.g.*, Ex-1001 at 5:48-56). The '126 patent accomplishes a larger n-electrode by the use of a dielectric layer, which was a well-known technique in the semiconductor industry. Easing the alignment and placement of flip-chip bumping whether the technique uses solder or anisotropic conductive silver paste is similar, yields will increase, and costs will reduce. This was a well-known technique used by the semiconductor industry in general that has been matured since the 1960s since IBM introduced the 'C4' process of flip-chip bumping using solder.

71. Before the '126 patent (*e.g.*, before 2004), the LED industry has successfully adopted surface mount packaging for LED chips, and in particular flip-chip techniques as developed by the semiconductor industry. The '126 patent noted that if the high precision of flip-chip bump placement and alignment is not eased, this will lead to “a reduction in the productivity” (Ex-1001 at 2:39-40). The LED industry addressed this issue in a couple of directions before the '126 patent including by: a) using higher accuracy pick and place robots that can accept smaller LED chip electrodes; and b) larger electrode pads. Higher accuracy pick and place robots that pick up LED chips and, place them more accurately onto printed circuit boards tend to be more expensive than silicon semiconductor pick and place robots

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that have lower precision for picking and placing chips. An alternative philosophy of increasing electrode pads (*e.g.*, surface area) resulted from many LED packaging and assembly companies choosing a lower precision tool that is more economic to purchase, and which has the benefit of being utilized with high yields and huge volumes in the silicon semiconductor industry. Thus, increasing an electrode pad size (*e.g.*, surface area) to lower manufacturing costs is a concept that has been addressed by pick and place tool manufacturers and chip package designers for many years in the silicon semiconductor industry.

72. The type of LED element described in the '126 patent was well-known and widely used prior to 2004.

7. The '126 Patent

73. U.S. Patent No. 7,554,126 issued on June 30, 2009 and matured from a patent application filed on March 12, 2007, which is the national phase entry of PCT application filed on September 22, 2005. The '126 patent claims the benefit of Japanese Patent Application No. JP2004279049, filed on September 27, 2004, and PCT/JP2005/017467, filed on September 22, 2005 (Ex-1001 at Cover Page).

7.1. The Relevant Technical Field

74. The '126 patent includes thirteen claims. Claims 1 and 2 are independent device claims. Claims 9 and 10 are independent methods of manufacturing claims that correspond to claims 1 and 2, respectively. Claims 4-8

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and 11-13 are dependent claims. Claims 1-2 and 4-13 are the Challenged Claims. The Challenged Claims generally relate to an LED and LED attachment to generic circuit boards, as well as methods of manufacturing/mounting the same.

75. The relevant technical field of the '126 patent is in the manufacturing and mounting of a semiconductor light emitting element, a manufacturing method and a mounting and forming a light-emitting device by mounting the semiconductor light-emitting elements on a circuit board. (Ex-1001 at 1:8-12).

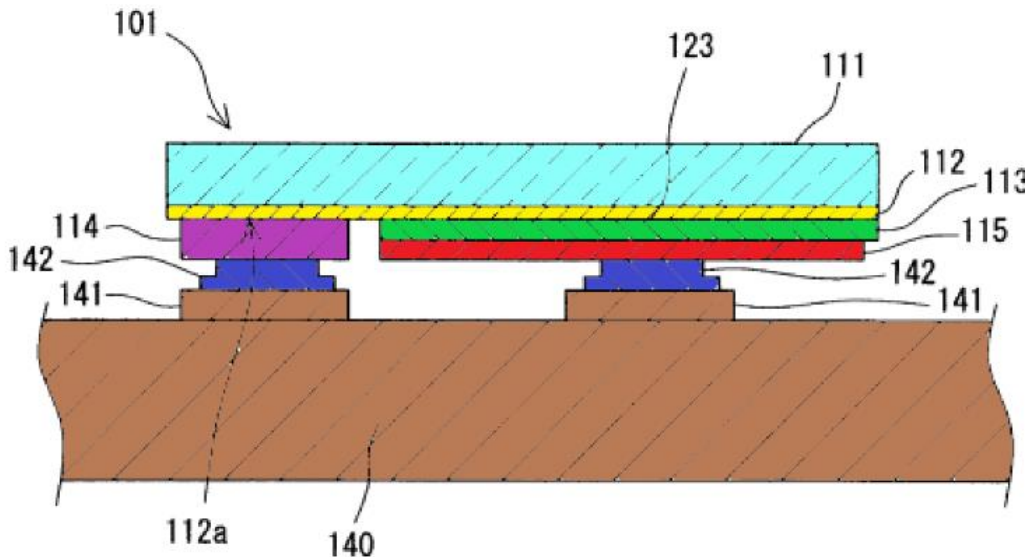
7.2. The '126 Patent's Alleged Invention

76. The alleged problem can be understood with reference to the “Issue to be Improved by the Invention” and FIGs. 16 and 17 (Ex-1001 at 1:24-2:49). The '126 patent describes a “typically conventional structure” in FIGs. 16-17 (Ex-1001 at 1:26-28). FIG. 16 illustrates an LED chip 101 having a “light-transmitting substrate 111,” (blue) an n-type semiconductor layer 112 (yellow) formed on the substrate 111, and a p-type semiconductor layer 113 (green) formed so as to cover part of the n-type semiconductor layer 112 (Ex-1001 at 1:32-37). An n-electrode 114 (purple) is formed on the n-type semiconductor layer 112 (yellow) (Ex-1001 at 1:36-37). A p-electrode 115 (red) is formed on the p-type semiconductor layer 113 (Ex-1001 at 1:41-42). LED 100 is connected to a circuit board 140 with bumps (e.g., indigo) 142 that connect the LED n-electrode 114 and the LED p-electrode 115 to

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corresponding circuit board (e.g., printed circuit board or “PCB”) electrodes 141 (brown).

'126 Patent FIG. 16 (Annotated)



77. The '126 patent explains that mounting a chip on a circuit board is usually carried out at low costs by using a conductive bonding material (e.g., solder or silver paste) (Ex-1001 at 2:12-16). According to the '126 patent, because an LED emits light from the p-type semiconductor material and the junction between the chip n-electrode and the circuit board n-electrode can block light from being emitted, the n-chip/circuit board junction needs to be small (Ex-1001 at 2:17-21). Also, the p-type semiconductor layer needs to be large to maximize the light-emitting area (Ex-1001 at 2:22-24). In order to maximize light extraction, the n-electrode is not always made bigger (Ex-1001 at 2:24-26). Therefore, the '126 patent further states that it may be difficult to use a conductive bonding material (e.g., solder and bumps) to

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join a relatively small n-electrode 114 area to a large circuit board joining area (Ex-1001 at 2:27-40). Against this backdrop, the '126 patent states that its “main objective is to provide a semiconductor light-emitting element which can be mounted on a circuit board by using a conductive bonding material, typically represented by solder, at low costs” (Ex-1001 at 2:41-45).

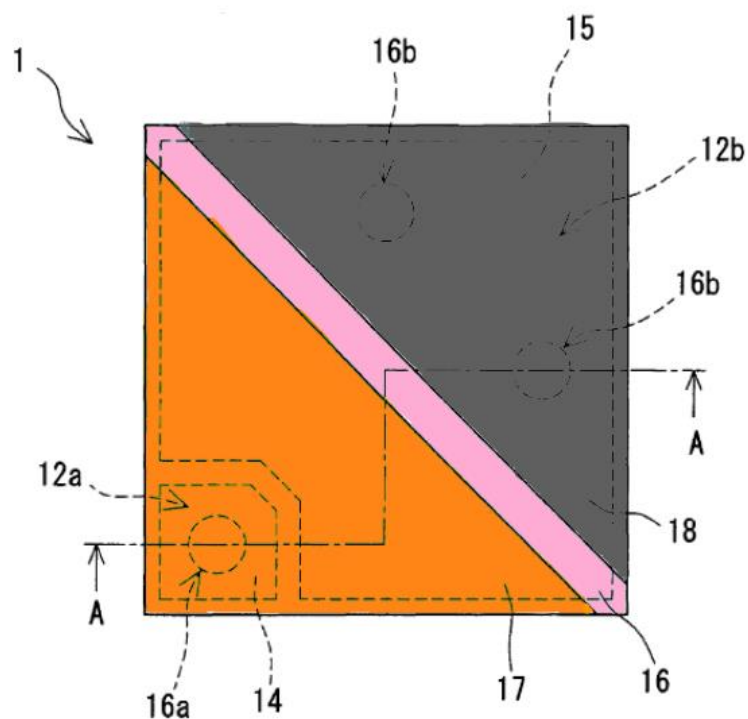
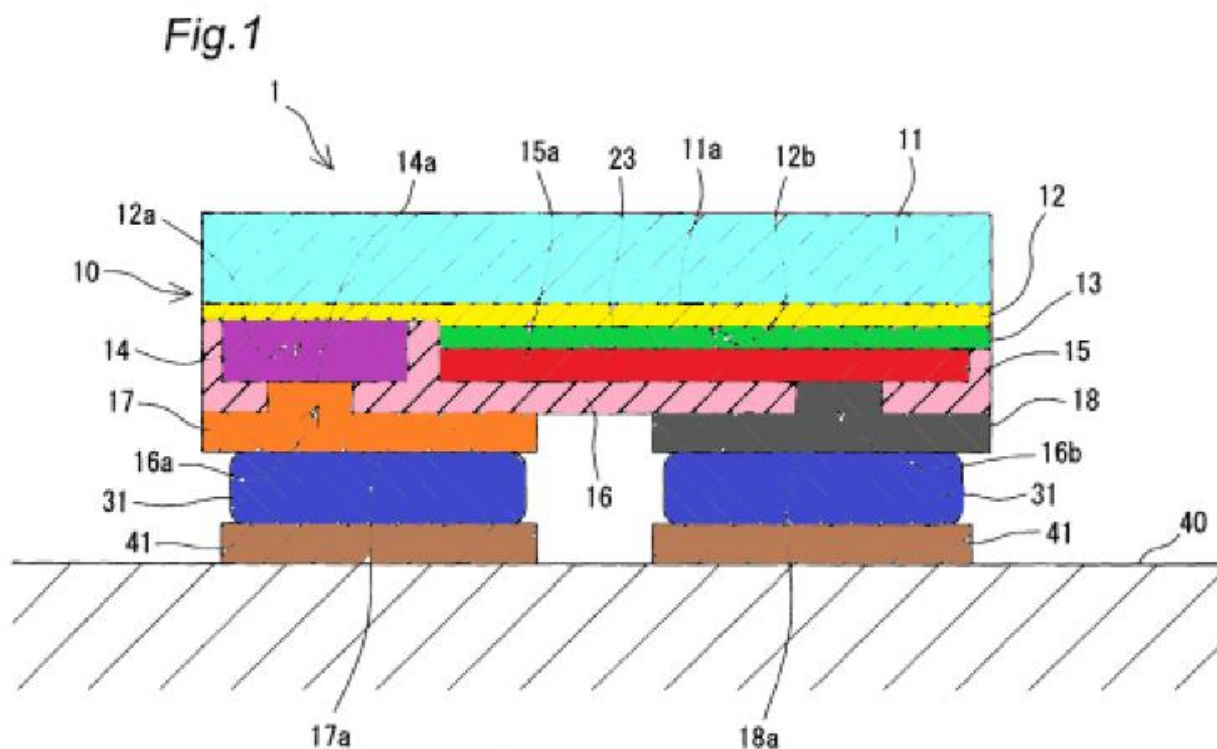
78. The '126 patent describes a light emitting device that is similar to the conventional LED described above but has a second n-electrode, a second p-electrode, and an insulating layer (*see e.g.*, Ex-1001 at 2:55-3:12). The '126 patent illustrates a first embodiment of “the invention” in FIGs. 1 and 2 (Ex-1001 at 6:61-64). FIG. 2 is a bottom view of a light emitting device taken without the solder and the circuit board as shown by the annotated arrows added in FIG. 1 (Ex-1001 at 6:6-7). FIG. 1 is a cross-section taken along the lines A-A in FIG. 2, so that the n and p electrodes can be seen in the same cross section (Ex-1001 at 6:3-7; 6:67-7-1). These figures are “exaggerated” for illustration (Ex-1001 at 7:1-4).

79. Similar to the described conventional LED, the '126 patent describes a light emitting device having a light emitting substrate 11 (*e.g.*, sapphire) (blue), an n-semiconductor layer 12 (yellow), a p-semiconductor layer 13 (green), a first n-electrode 12a (purple), and a first p-electrode 15 (red) (Ex-1001 at 7:7-15; 7:25-31). The first electrodes are described as thin film electrodes (Ex-1001 at 7:32; 7:41).

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80. The '126 patent discloses a first insulating layer 16 (pink) that insulates the first n-electrode (purple) and the first p-electrodes (red) from each other (Ex-1001 at 7:16-20). The '126 patent describes a second n-electrode 17 (orange) and a second p-electrode 18 (gray) (Ex-1001 at 7:19-24). The second n-electrode 17 (orange) is “formed on the first insulating layer 16” (pink) and “penetrates the first insulating layer 14 to be electrically connected to the first n-electrode 14” (purple) (Ex-1001 at 7:21-23). The second p-electrode 18 (gray) is electrically connected to the first p-electrode (red) (Ex-1001 at 7:23-24). The second electrodes are referred to as “thin films” (Ex-1001 at 7:65-8:1). However, the '126 patent states that different electrode sizes (areas) can be used (Ex-1001 at 9:16-17). As shown by the solid lines in FIG. 2, the second n-electrode 17 (orange) and the second p-electrode (gray) are shown to be “isosceles triangles that have virtually the same size,” but the patent states that different sizes (areas) can be used (Ex-1001 at 9:5-20). The '126 patent states that the second electrodes can be bonded to electrodes 41 of a circuit board 40 (brown) (FIG. 1) with a conductive bonding material layer, such as solder 31 (indigo) (Ex-1001 at 8:37-41).

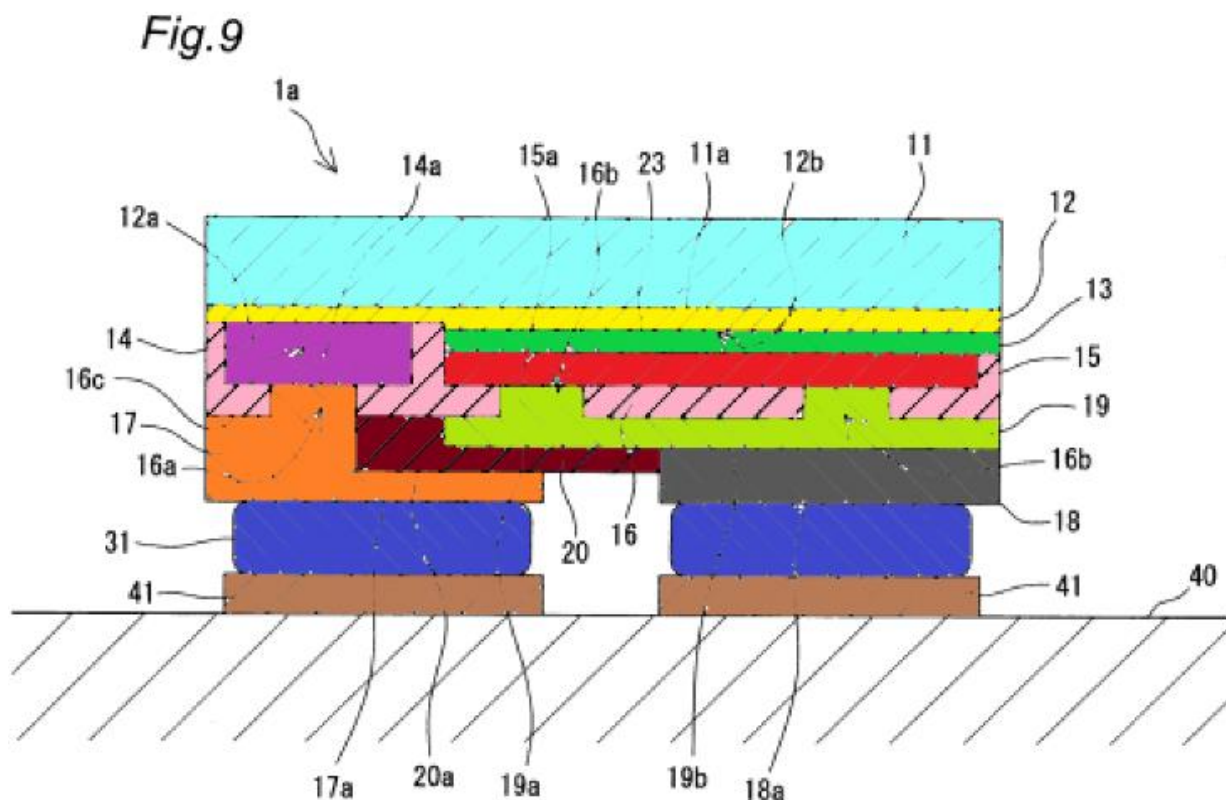
'126 Patent FIGs. 1 & 2 (Annotated)

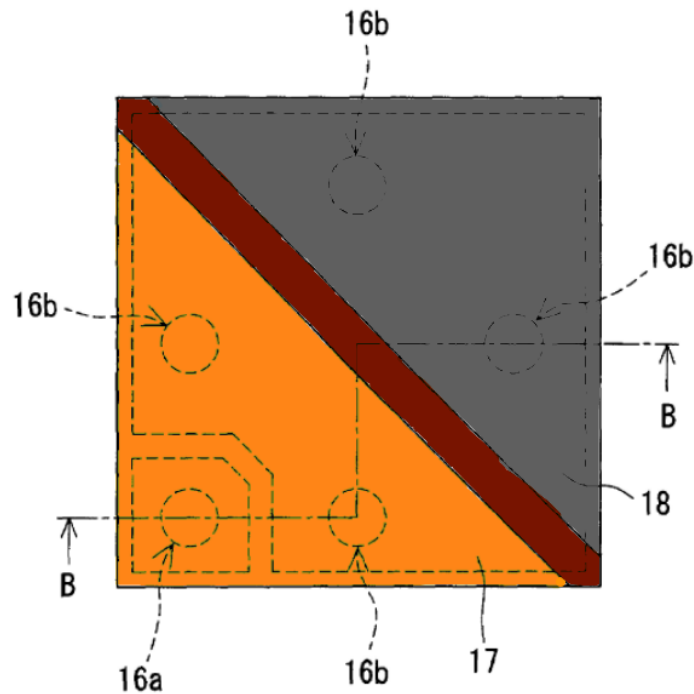


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81. The '126 patent describes a second embodiment in FIGs. 9 and 10 (Ex-1001 at 6:25-29; 11:26-49). The second embodiment adds a conductive layer 19 (lime) and a second insulating layer 20 (dark red) to the first embodiment (Ex-1001 at 11:43-49). The conductive layer 19 is formed on the first insulating layer 16 and is electrically connected to the first and second p-electrodes 15, 18 (Ex-1001 at 11:49-56). The second insulating layer 20 insulates the second n-electrode 17 from the conductive layer 19 (Ex-1001 at 11:60-64).

'126 Patent Figs. 9 & 10 Annotated





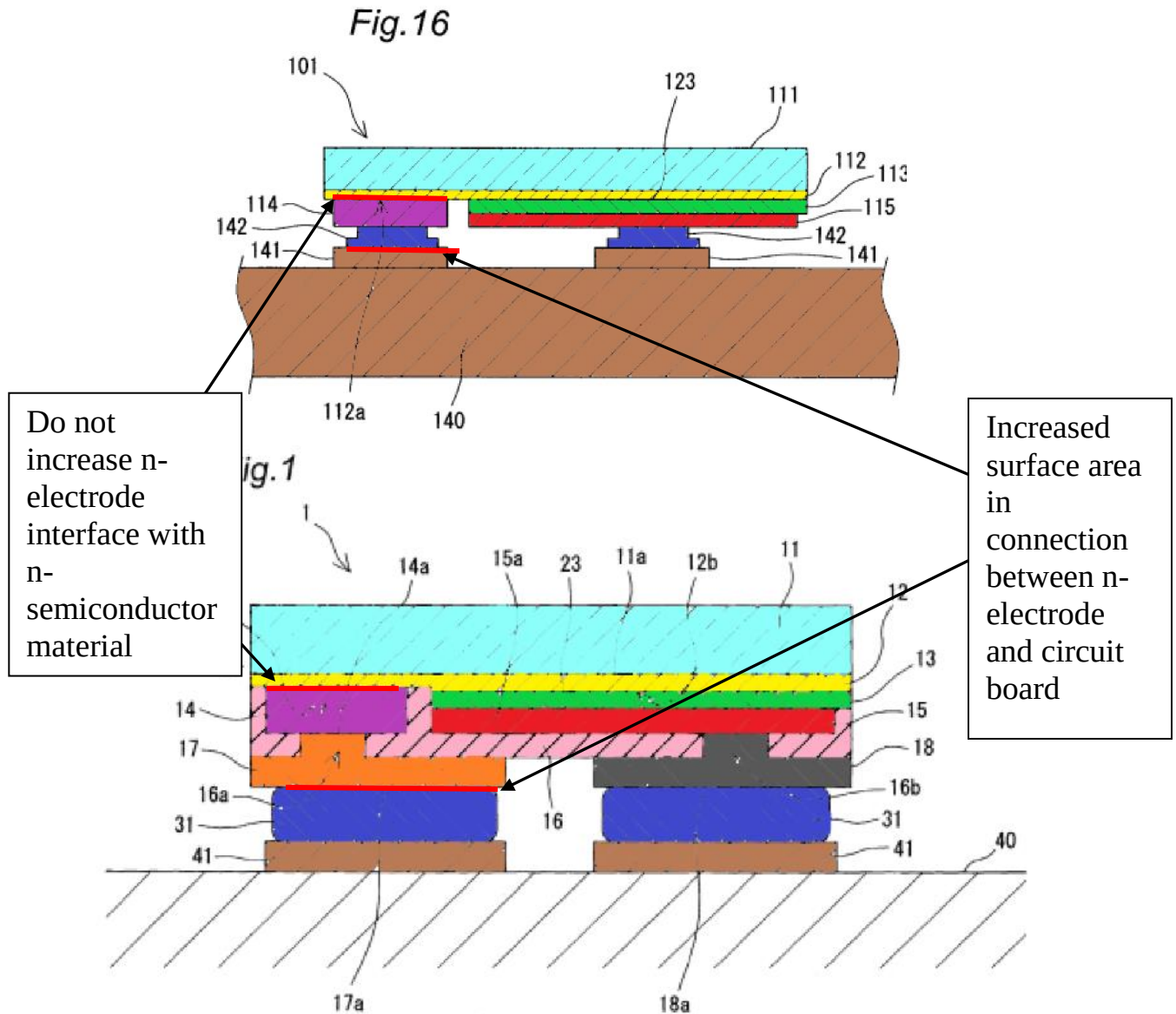
82. According to the '126 patent, by connecting the LED to a circuit board 40 with a second n-electrode, the joining strength and heat dissipation is increased (Ex-1001 at 10:63-11:3). The described structure seemed to be aimed at simply determining how to strengthen the mechanical and thermal connection between the n-electrode and a circuit board without increasing the area that the n-electrode covers the n-semiconductor layer, so that the interface between the n-semiconductor layer and the p-semiconductor layer can be maximized, thereby maximizing the light generating junction between the n-semiconductor layer and the p-semiconductor layer and the heat dissipation. This is understood with reference to the '126 patent's conventional with the LED in FIG. 1 below. As shown with the red lines in the Figures below on the n-electrode interfaces, the '126 patent increased the red

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interface between the second n-electrode and the circuit board electrode without increasing the red interface between the first n-electrode and the n-semiconductor layer.

83. The '126 patent solved this alleged problem by simply increasing the n-electrode surface area that is in contact with the circuit board (i.e., by attaching a second n-electrode with more surface area than the n-electrode/n semiconductor layer interface). The goal of creating a stronger connection was simply and straightforwardly (allegedly) solved by providing more surface area.

Comparison of Conventional LED of FIG. 16 and FIG. 1 Embodiment



7.3. The Prosecution History

84. In preparing my report, I have reviewed the file history of the '126 patent (“’126 patent file history”) (Ex-1002). I discuss only portions of the file

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history herein, but I reserve the right to rely on any other portion of the file history for my opinions as this matter proceeds.

85. The '126 patent was filed as U.S. App. No. 11/662,547 on September 22, 2005 (Ex-1001 at Cover). The '126 patent claims were allowed quickly without even a single office action and with limited art considered (Ex. 1002). The examiner did not cite any references (Ex. 1002). The applicant cited all references considered (Ex. 1002 at p. 22).

7.4. The Claims of the '126 Patent

86. Claim 1 of the '126 patent is directed to a “semiconductor light-emitting element” and has a “substrate,” an “n-type semiconductor layer,” a “p-type semiconductor layer,” a “first n-electrode,” a “first p-electrode,” a “first insulating layer,” “second n-electrode,” and a “second p-electrode.” (Exhibit 1001 at 13:46-14:7). Claim 9 is directed to the same embodiment as Claim 1.

87. The first six elements of claims 2 and 10 are the same as claims 1 and 9, respectively, but otherwise the claims differ insofar as claims 2 and 20 have limitations relating to “openings” for the first claimed electrodes and the second claimed electrodes being “formed on the first insulating layer” (Ex-1001 at 14:47-15:38). Claim 2 claims a “semiconductor light-emitting element” and has a “substrate,” an “n-type semiconductor layer,” a “p-type semiconductor layer,” a “first n-electrode,” a “first p-electrode,” a “first insulating layer,” “second n-

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electrode,” and a “second p-electrode” (Exhibit 1001 at 14:8-14:38). Claim 10 is directed to the same embodiment as Claim 2.

88. U.S. Patent No. 7,554,126 issued on June 30, 2009 and matured from a patent application filed on March 12, 2007, which is the national phase entry of PCT application filed on September 22, 2005, and claims priority to foreign Japanese application filed on September 27, 2004.

8. Overview of the Prior Art

89. The main focus of the '126 patent is the sizing of the n-electrode and p-electrode. But these sizing concepts were known as were the other standard LED structures and manufacturing techniques. In general the '126 patent dependent claims merely recite known LED structures or techniques, some that are quite old (*e.g.*, solder, sputtering, plating, LED relative sizing and placement). All of my opinions are expressed from the perspective of a POSITA at the alleged invention date, the earliest alleged priority date of the '126 patent.

8.1. Sizing of N-electrodes and P-Electrodes

90. The '126 patent did not invent second n- and p-electrodes or insulating layers. The '126 patent did not invent increasing the surface area connection for an n-electrode by attaching a second n-electrode, with a larger surface area, to a first n-electrode that has a smaller joined face between the first n-electrode and n-semiconductor layer.

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8.1.1. Terashima

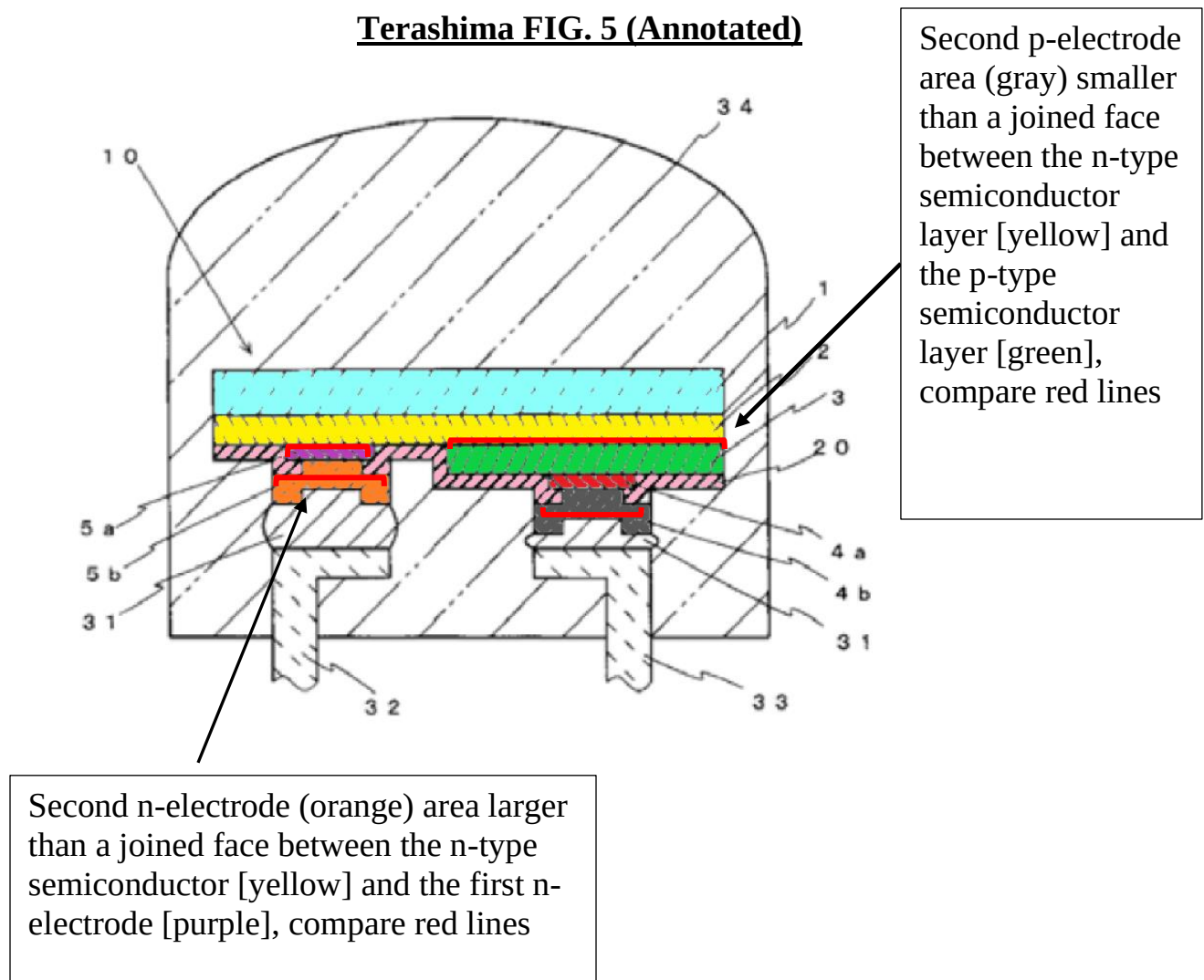
91. Japanese Patent Publication No. 2004-103975 (“Terashima”) (Ex-1004) published on April 2, 2004 (Ex.-1010 at “(43) Publication Date”). A certified translation of Terashima – including a declaration by the translator in accordance with 37 CFR 1.68 attesting to its accuracy – is attached as Ex-1010. Terashima was used to reject versions of the claims present in PCT/JP2005/017467 (*i.e.*, the PCT application from which the ’126 patent was a national phase filing) as indicated in the International Preliminary Report on Patentability (Ex-1009). Given that the PCT application does not issue as a patent, it appears that the patentee never attempted to rebut the rejections based on Terashima. Although Terashima was considered by the Patent Examiner during the prosecution of the ’126 patent (Ex-1002 at FH_000041), the only portion of Terashima that was provided to the Examiner in the English language was the Abstract, as the specification, figures, and claims of Terashima were only provided in Japanese (Ex-1002 at FH_000041; FH_000226-000229; FH_000239-000253).

92. As shown in annotated FIG. 5 below, Terashima discloses a “semiconductor light-emitting element” (Ex-1004 at ¶ [0050]) having a “transparent insulating substrate 1” (blue), an “n-type nitride semiconductor layer 2” (yellow) formed on the substrate, a “p-type nitride semiconductor layer 3” (green) formed on the n-semiconductor layer, a first “plating growth film” n-electrode 5a (purple) and

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a second, larger n-electrode 5b (orange), a first “plating growth film” p-electrode 4a (red) and a second, larger p-electrode 4b (grey) p-electrode, and an insulating layer in the form of “protective film 20” (pink) (Ex-1010 at ¶¶ [0003], [0029], [0032]-[0036], [0061], Explanation of symbols]). As shown below in FIG. 5, Terashima discloses that: (i) the second n-electrode has an “area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode;” and (i) the second p-electrode has an area that is smaller than the interface between the n-semiconductor layer and the p-semiconductor layer, as claimed in the ’126 patent. Thus, the ’126 patent claims and the ’126 patent’s alleged inventive concepts are not novel.

Terashima FIG. 5 (Annotated)



8.1.2. Sugimoto

93. United States Patent Application Publication no. US 2004/0159836 (“Sugimoto”) published on August 19, 2004 from an application filed on February 19, 2004, and is prior art to the ’126 patent under 35 U.S.C. §§ 102(a)&(e) (pre-AIA).

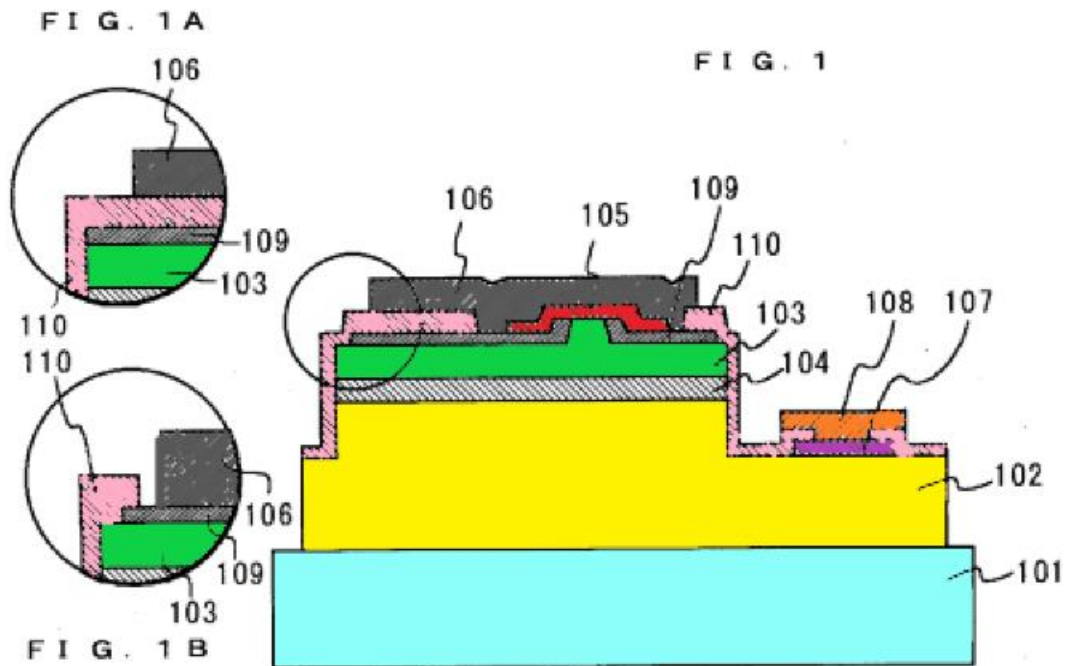
94. Sugimoto further discloses a light emitting device having an n-type semiconductor layer 102 (yellow) formed on a sapphire substrate 101 (blue) and a

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p-type semiconductor layer 103 (green) formed on the n-type semiconductor layer 102 (yellow) with an active layer between the n and p layers (Ex-1006 at ¶ [0072], *see* [0005] “sapphire” substrate). In addition, Sugimoto discloses a first p-electrode 105 (red) connected to a second p-electrode 106 (gray) (Ex-1006 at ¶ [0073]). Sugimoto discloses a first n-electrode 107 (purple) connected to a second n-electrode 108 (orange) (Ex-1006 at ¶ [0073]). As shown in FIG. 1, Sugimoto also discloses a first and a second insulation layer 109, 110 that insulate the electrodes (Ex-1006 at ¶¶ [0073], [0075]).

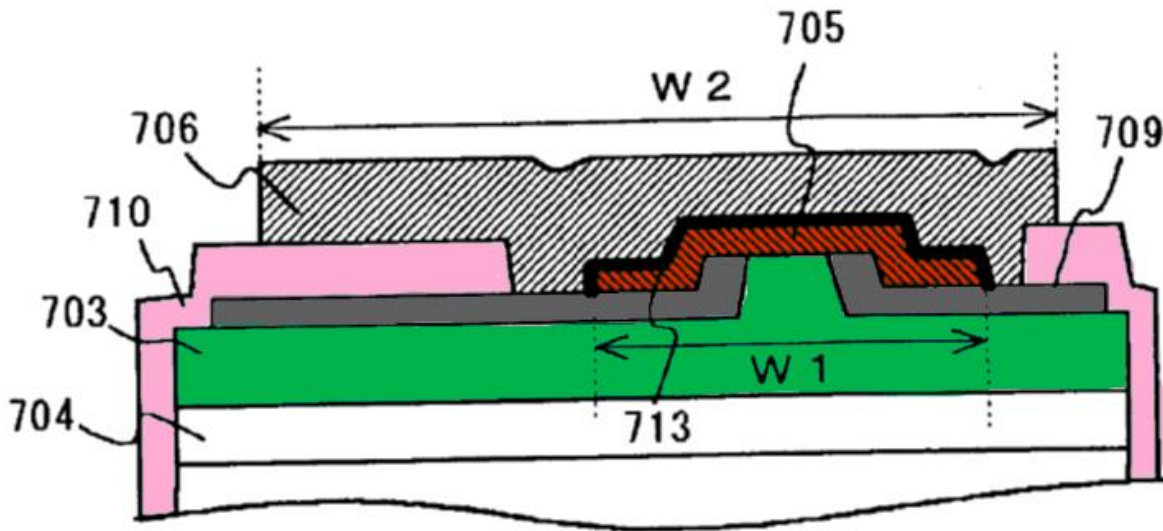
95. Sugimoto’s second n-electrode 108 has an area larger than a joined face between the n-type semiconductor (102) and the first n-electrode (107), so that the second n-electrode is electrically connected to the first n-electrode (Ex-1006 at ¶ [0073]). Also, as shown in Fig. 5, Sugimoto’s second p-electrode 106 has an area smaller than a joined face between the n-type semiconductor layer (102) and the p-type semiconductor layer (103) (Ex-1006 at Fig. 1). Thus, like Terashima, Sugimoto discloses the alleged inventive concepts to which the ’126 patent claims are directed.

Sugimoto Fig. 1



96. Sugimoto teaches what the '126 patent claim to have invented regarding the relationship between the n-electrode sizes in Figure 7A. Sugimoto states that preferably “the width W2 of the second electrode 706 is larger than the width W1 of the first electrode 705” (Ex-1006 at ¶¶ [0058]-[0059]).

Sugimoto Fig. 7A



8.1.3. Shin

97. U.S. Publication No. 2004/0256631 (“Shin”) published on December 23, 2004 from an application filed on November 6, 2003 (Ex-1005 at Cover).

98. Shin’s FIG. 5 illustrates a top view and a cross-section taken along line B-B (Ex-1005 at ¶ [0060]). Shin discloses a flip-chip light emitting element (Ex-1005 at ¶¶ [0002], [0019], [0038]). Shin describes that the light emitting element has a sapphire substrate 41 (blue), a n-semiconductor layer (yellow) that includes the n-sublayer 43a and buffer layer 42, and a p-semiconductor layer 43c (green) formed on the n-semiconductor layer with an exposed area for a first n-electrode 46a (purple) on the n-semiconductor layer (Ex-1005 at ¶¶ [0040], [0044]). A first p-electrode 45 (red) is formed on the p-semiconductor layer 43c (Ex-1005 at ¶ [0044]). First n-electrode 46a, 46b are formed on n-layer 43a/buffer layer 42 (Ex-1005 at ¶

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[0045]). Shin discloses a “passivation” or “insulation” layer 47 (Ex-1005 at ¶ [0048]-[0050]).

Shin FIG. 5 (Annotated)

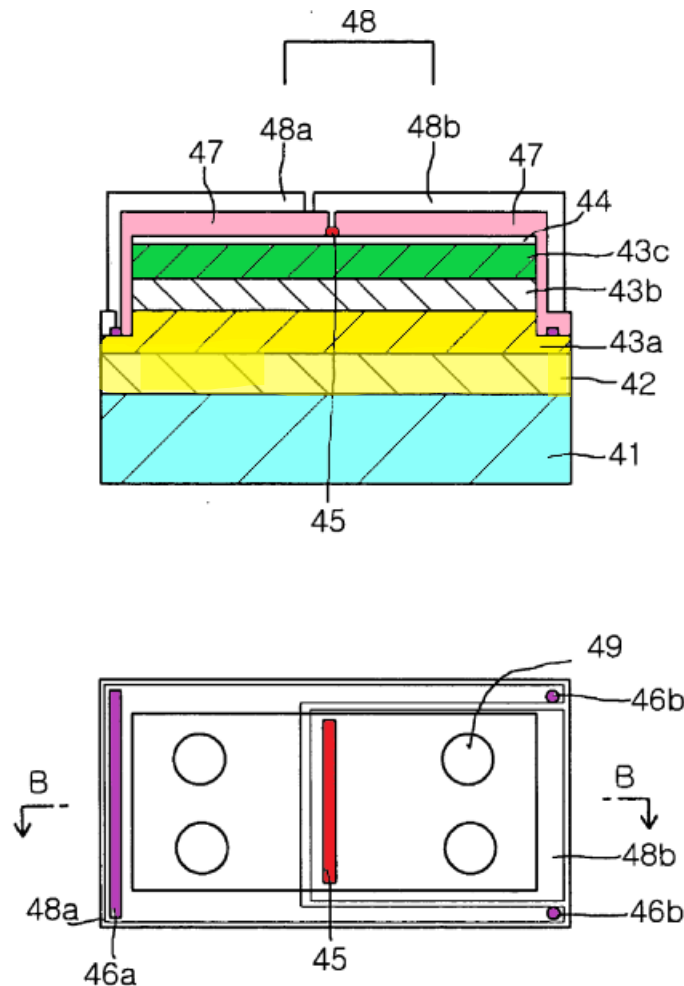


FIG. 5

99. Shin also discloses a second n-electrode 48a (orange) and a second p-electrode 48b (grey) formed on the insulation layer 47, as shown in FIG. 4E below (Ex-1005 at ¶¶ [0047], [0051]). FIG. 4E illustrates a top and cross-section views of

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the LED (Ex-1005 at ¶¶ [0034], [0050]). As is shown by comparing FIG. 4E with FIG. 5 above, the second n-electrode 48a (orange) has an area larger than a joined face between the n-type semiconductor and the first n-electrode (*i.e.*, the area associated with 46a) first n-electrode (Ex-1005 at ¶ [0051]). Also, as shown in FIGs. 4E and 5, the second p-electrode 48b has an area smaller than a joined face between the n-type semiconductor layer/buffer layer (43a/42 - yellow) and the p-type semiconductor layer (43c – green) (Ex-1005 at ¶ [0051]). Again, the '126 patent's alleged inventive concept is disclosed.

Shin Fig. 4E (Annotated)

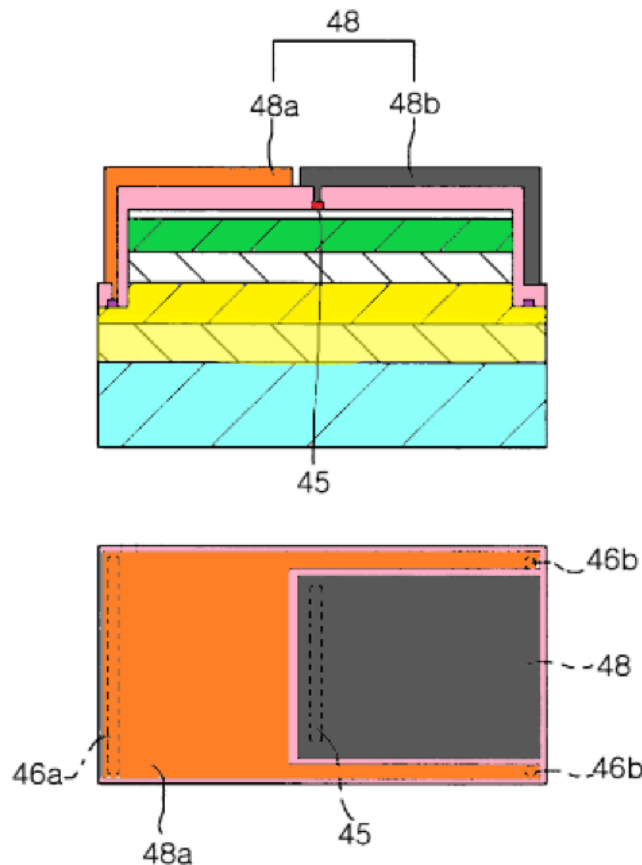


FIG. 4E

8.2. Thin Film Art

100. The '126 patent does not claim to have invented “thin film” electrodes. Thin film electrodes were common to a POSITA and well-known before the '126 patent particularly for use in gallium nitride LEDs.

101. The '126 patent provides examples, but not limits, on what constitutes a “thin film.” The '126 patent specification provides that: the first n-electrode is formed as a thin film “having a thickness, for example, in a range of 0.1 micrometers

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to 0.3 micrometers” (Ex-1001 at 7:32-34; 7:42-42); the first p-electrode is formed as a thin film “having a thickness, for example, in a range of 0.1 micrometers to 1.0 micrometers” (Ex-1001 at 7:32-34; 7:42-42); and the second n- and p-electrode have “a thickness, for example, in a range of 0.1 micrometers to 0.3 micrometers” (Ex-1001 at 7:65-8:1). Thus, while the ’126 patent provides different example dimensions (*e.g.*, 0.1-0.3 & 0.1-1.0 micrometers) for what constitutes “thin,” the ’126 patent claims do not specify any dimensions for a “thin film.”

102. Thin film electrodes were well-known prior to the ’126 patent. For example, U.S. Patent No. 6,989,598 (“Song”) (Ex-1017) describes how prior to the filing date of the ’126 patent, in 2004, “thin film electrodes based on nickel (Ni), *e.g.*, a thin metal film of nickel/gold (Ni/Au), have been widely used as thin film electrode structures for ohmic contact” (Ex-1023 at 1:32-34). These LED thin film electrodes have “very thin thickness ($<\sim 100$ Å) and a transmittance of 80% or more” (Ex-1017 at 1:61-63). Song was filed in the United States on March 17, 2004 and claims priority to a foreign application filed on March 7, 2003 (Ex-1017).

103. The prior art discloses “thin film” electrodes. For example, Sugimoto discloses that the prior art to Sugimoto included LED electrodes made as a single or multi-layer film (Ex-1006 at ¶¶ [0006], [0008]). Sugimoto also discloses thin “film” electrodes, where the first electrodes preferably have a thickness in the range of about 100 to 30,000 angstroms (0.01 to 3 micrometers), and the second electrodes

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preferably have a thickness in the range of 3,000 to 20,000 angstroms (0.3 to 2 micrometers) (Ex-1006 at ¶¶ [0065]-[0068]). While Sugimoto does not precisely state that the first p-electrode has the same dimensions as the first n-electrode, that is the understanding that a POSITA would have based on Sugimoto. Sugimoto describes at some length the materials and manufacturing of the first n and p electrodes together, and therefore a POSITA would understand that the first n and p-electrodes would have the same range of dimensions (Ex-1006 at ¶¶ [0065]-[0068]). In fact, it is often typical to manufacture the first electrodes at the same time with the same thickness as this simplifies the manufacturing process (Ex-1006 at ¶¶ [0014]-[0018]; [0020]-[0034], [0053], [0055], [0059]).

104. Similarly, Terashima describes the first n-electrode 5a and first p-electrode as each being a “plated growth film,” “thin,” and formed by either a “film deposition method, such as vacuum deposition, sputtering, or printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]). Film deposition method, such as vacuum deposition, sputtering, or printing were processes known to a POSITA to make thin film electrodes. Terashima describes the second p-electrode as a “film” or “single layer film” (*e.g.*, “thin”) (Ex-1010 at ¶ [0038], [0059]).

105. Shin likewise describes that the “n-electrode 46” is formed as a “lane electrode” 46a having “as narrow width as possible” with example widths of 10 to 20 micrometers (Ex-1005 at ¶¶ [0045]-[0046]). Shin describes thin film electrodes.

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In describing a “conventional” LED, Shin refers to U.S. Patent No. 6,333,522 (Ex-1021) (“Inoue”) (Ex-1005 at ¶ [0014]). Inoue discloses thin film electrodes. Inoue describes the electrodes as “metal films” (Ex-1021 at 3:35-4:17). Inoue further describes that the electrodes can be formed with a titanium film with a thickness of about 0.2 microns, a gold film having a thickness of about 0.5 microns stacked by a lift-off method or an etching method resulting in a multilayer film, forming a Ni film with a thickness of about 0.2 microns over the entire surface of the wafer, followed by an Au film with a thickness of about 1 um formed thereon by vapor deposition, and forming a resist mask with openings corresponding to the respective regions, in which microbumps are formed over the Ni/Au multilayer film by a photolithography process. (Ex-1021 at 13:13-29). A POSITA understands this disclosed electrode to be a thin film. Further, although the specific sentence describing this electrode construction refers to the n-side electrode 6 (Ex-1021 at 13:17), a POSITA understands that this electrode description applies to both n and p electrodes because (i) Inoue introduces this description by stating that “the description will be given next to an exemplary procedure for forming the p-side electrode 5, the n-side electrode 6, and the microbumps 22 and 23 (Ex-1021 at 13:13-15); (ii) after describing the construction Inoue states that microbumps are attached through openings in the resist mask are plated to overlies the n and p electrodes 6 and 5, thereby stating that the construction also applies to the p-electrode (Ex-1021 at 29-

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34), and (iii) another description of constructing a p-electrode is not provided in this section. Inoue also discloses that it is “possible to provide” a thick film p-electrode can be used in that particular application (Ex-1021 at 14:52-57).

106. United States patent publication US 2003/0160259 (“Uemura ’259”) published on August 28, 2003. United States patent publication US 2004/0149999 (“Uemura ’999”) published on August 5, 2004. Uemura ’259 discloses a film thickness of 0.3 micrometers for a p-electrode provides sufficient strength and stability for general purposes and the upper limit for thickness can be based on cost (Ex-1007 at ¶ [0049]). Likewise, Uemura ’999 discloses n and p electrode film thicknesses in the range of 0.1 to 50 micrometers (Ex-1008 at ¶ [0032]). The Uemura references disclose thin film electrodes.

107. I refer to Terashima, Sugimoto, Inoue, Uemura ’259, and Uemura ’999 collectively as the “Thin Film Art.” A POSITA would have been motivated to use the thin film electrodes as described in any of the Thin Film Art. As I described, thin film electrodes were common place in 2003. Thin film electrodes were known to provide good electrical and mechanical connections while maximizing light extraction by reducing reflection and absorption. The results were predictable and well-known with the level of ordinary skill in the art.

108. A reason a POSITA used thin film electrodes in LEDs is to enhance light extraction from an LED package. A primary goal of an LED package is to

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maximize the amount of light emitted by an LED from the LED package. Metal electrodes can be used to provide the electrical path for electricity to reach the LED because metals are excellent electrical conductors as well as thermal conductors to dissipate heat. However, metals also reflect light and can absorb light. If light is reflected back into the LED package or absorbed, this can decrease light extraction. Thin film electrodes were developed as a way to provide the benefits of a metal electrode but minimize the detrimental impact on light extraction. Techniques for manufacturing thin film electrodes such as sputtering and plating are described below and were developed well before the '126 patent. Thin film electrodes can be single layer or multilayer. Generally, thin film electrodes are formed by depositing very small amounts of metal and building a layer of a desired thickness. The thickness is application dependent based on the size of the LED and the intended LED purpose. Based on the known acceptance and benefits of thin film electrodes, a POSITA would have been motivated to use thin film electrodes in LEDs, particularly those related to gallium nitride LEDs before the earliest claimed priority date of the '126 patent.

8.3. Electrode Spacing

109. The '126 patent describes uniformly spacing the p-electrodes to promote the uniformity of light emitted from the p-semiconductor layer (Ex-1001 at 8:63-9:4). This concept was not invented by the '126 patent. A POSITA knew that it was beneficial to provide a uniform current to the p-semiconductor layer. By applying a uniform current to the p-semiconductor layer, light is more efficiently produced. Further, a uniform current induces less stress into the p-semiconductor layer, which prevents the LED from degrading. A POSITA knew prior to the earliest priority date for the '126 patent that one way to provide a uniform current to the p-semiconductor layer was to provide uniformly spaced p-electrodes that uniformly provide the current to the p-semiconductor layer.

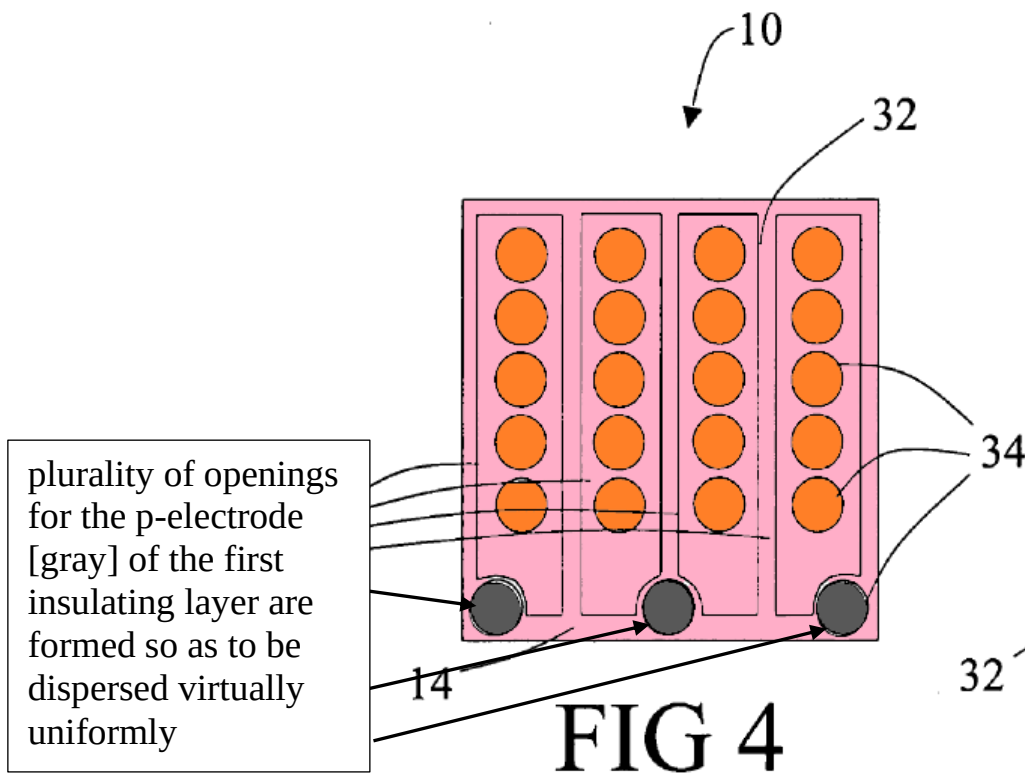
110. Shin describes a p-electrode positioned at the “center of the light emitting structure” (Ex-1004 at ¶ [0021]). Shin describes this positioning to be advantageous because “current uniformly flows” through the LED, thereby preventing the LED life span from being shortened due to concentration of current at a predetermined position (Ex-1004 at ¶ [0021]). Thus, Shin recognized the importance of uniform current flow.

111. U.S. Application Publication No. 2005/0194605 (“Shelton”) likewise provides for uniform current flow by providing uniformly spaced openings for a plurality of p-electrodes. Shelton discloses “a plurality of openings for the p-

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electrode of the first insulating layer are formed so as to be dispersed virtually uniformly.” As shown below, Shelton’s n-electrode 12 [orange] and p-electrode 14 [gray] are sealed by a dielectric layer 32 [pink], which is an insulating layer (Ex-1011 at [0038]). The dielectric layer 32 includes several vias 34 or “openings.” For example, Shelton describes that the “vias 34 provide access to the p-type and n-type electrodes 12 [gray], 14 [orange]. Shelton discloses several vias 34 for each of the electrodes 12 [gray], 14 [orange] that are distributed virtually uniformly across the “lateral area of the light emitting diode 10 to promote current spreading across the light emitting diode 10” (Ex-1011 at ¶ [0039]). Shelton’s current spreading was known to enhance LED light extraction and prevent LED degradation. This was known and a POSITA would have been motivated to use uniform spaced p-electrodes to provide uniform current to the p-semiconductor layer to prevent LED degradation.

Shelton, Figure 4 (annotated)



8.4. Manufacturing Film Electrodes & Insulation Layers

112. The '126 patent refers to the electrodes and insulation layer being formed through sputtering (Ex-1001 at 7:40-43; 7:65-67; 10:6-7). The '126 patent also states that the electrodes can be formed by “plating” (Ex-1001 at 7:40-43; 7:65-67; 10:20-23). The '126 patent does not claim to have invented sputtering or plating. The '126 patent does not provide any details about sputtering and plating and assumes that sputtering and plating were known to a POSITA. I agree that sputtering and plating were known to a POSITA and within the level of ordinary skill in the art. Sputtering and plating are manufacturing techniques that were well-established,

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predictable, and known for manufacturing LED electrodes and insulation layers, particularly thin film electrodes. Using sputtering and plating to form electrodes and insulation layers was predictable.

113. Sputtering can generally be described as the process by which ionized atoms are accelerated into a surface in order to eject atoms from that surface. The ejected atoms can be condensed onto a sample to nucleate a thin film of the ejected material. This is often referred to as sputter deposition. A metric to characterize the sputtering event is the sputter yield. Sputtering yield is a measure of the number of atoms ejected from the target for each bombardment ion.

114. One type of sputtering is known as CD diode sputtering. Generally, DC diode sputtering uses two plates, a vacuum supply, and a power supply. A sputtering gas, such as argon, is introduced under pressure and voltage is applied across the two plates. Another type of sputtering is known as RF Plasma sputtering. RF Plasma sputtering uses an alternating-current radio frequency source instead of a DC power source.

115. Other techniques for forming electrodes include evaporation, plating, e-beam processes, and chemical vapor deposition.

116. Plating or electroplating is used to form electrodes by depositing for example copper. The plating metal is connected to a positively charged electrode or anode of an electrical circuit. A work piece, or substrate, is placed at the negatively

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charged electrode, called the cathode. Both the plating metal and the substrate are immersed in an electrolytic solution called a bath. After submersion, a DC current is supplied to the anode, oxidizing the atoms of the plating metal and dissolving them into the bath. At the cathode, the negative charge reduces the atoms, causing them to plate the substrate.

117. Terashima describes the first n-electrode 5a and the first p-electrode can be a “plated growth film,” “thin,” and formed with by either a “film deposition method, such as vacuum deposition, sputtering, or printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]). Terashima discloses that n and p electrodes 4b, 5b respectively, can be formed by “plating” (Ex-1010 at ¶ [0034]) .

118. Terashima teaches that the protective film 20, which is an “insulating layer,” “is formed by a film forming means such as vacuum deposition or sputtering” (Ex-1010 at ¶ [0036]).

119. Sugimoto teaches that electrodes are formed” by “sputtering (Ex-1006 at ¶¶ [0155]; [0019]; *see also* ¶¶ [0020], [0021], [0024]).

8.5. Attaching an LED to a Circuit Board

120. Connecting an LED to a circuit board by using solder is very old. Solder, such as lead or tin, can be melted and flowed to create a connection between an electrode LED and a circuit board LED. This was common knowledge to a POSITA.

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121. The '126 patent refers to solder reflow. The '126 patent did not invent Solder reflow. Solder reflow was a common process known to a POSITA. Solder reflow involves applying solder paste to a circuit board and applying controlled heat in a controlled oven to melt and harden the solder to connect an LED to a circuit board. Solder reflow is consistent and repeatable and was widely adopted prior to the '126 patent. A POSITA knew that solder reflow created reliable connections between an LED and a circuit board.

122. As an example, Shelton discloses that LED p and n electrodes can be bonded with solder, a “conductive material,” and “reflow alloy bonding” to “mechanically secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]).

8.6. Epitaxial LED Growth

123. Epitaxial growth was a known method of making an LED at the relevant time period. Epitaxial growth involves growing layers of an LED on top of each other. Growing a layer of one material on another material can introduce strain. This strain is due to the lattice mismatch between the two layers. Lattice mismatch refers to the lattice constant of two materials being different. The lattice constant describes the spacing between adjacent cells in a crystal structure. Because different materials, such as sapphire and an n-semiconductor layer have different lattice constants, when an n-semiconductor layer is grown on a sapphire substrate it is

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common for the n-semiconductor layer to have sublayers for lattice matching and reducing strain. For example, the n and p semiconductor layers may have a buffer layer that is proximal to the sapphire substrate. An example of this is provided in U.S. Patent No. 7,154,125 (Ex-1020). The '125 patent describes that the n-semiconductor layer and p-type semiconductor layers have multiple layers (Ex-1020 at 7:48-61; 9:50-60; 10:47-62).

124. Similarly, Sugimoto describes that the n-semiconductor layer and p-type semiconductor layers can have multiple sublayers (Ex-1006 at ¶ [0005]). Sugimoto describes that a “typical nitride semiconductor device has a multilayer structure” including the (i) “a buffer layer, an n-type contact layer, a crack-free layer, an n-type cladding layer, an n-type light guide layer,” that form an n-semiconductor layer; (ii) an active layer; and (iii) “a p-type electron confinement layer, a p-type light guide layer, a p-type cladding layer, and a p-type contact layer,” that form a p-semiconductor layer.

9. The Challenged Claims are Unpatentable

9.1. Terashima Anticipates Claims 1, 2, and 5-12

125. It is my opinion that Terashima anticipates claims 1, 2, and 5-12 of the '126 patent. Terashima teaches each limitation in these claims. Terashima's structure that satisfies claim 1 is set forth with reference to the following color coding.

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Claim 1 Element	Terashima Disclosure
Preamble	“optical semiconductor device (LED component)”
substrate	“transparent insulating substrate 1” [blue]
n-type layer	“n-type nitride semiconductor layer 2” [yellow]
p-type layer	“p-type nitride semiconductor layer 3” [green]
first n-electrode	“plated growth film 5a” [purple]
first p-electrode	“plated growth film 4a” [red]
first insulating layer	“protective film 20” [pink]
second n-electrode	“n electrode 5b” [orange]
second p-electrode	“p electrode 4b” [gray]

9.1.1. Terashima Anticipates Independent Claim 1

126. It is my opinion Terashima anticipates claim 1 of the '126 patent for at least the following reasons.

9.1.1.1. Terashima Discloses the Preamble

127. Terashima discloses “[a] A semiconductor light-emitting element,” recited in claim 1 of the '126 patent.

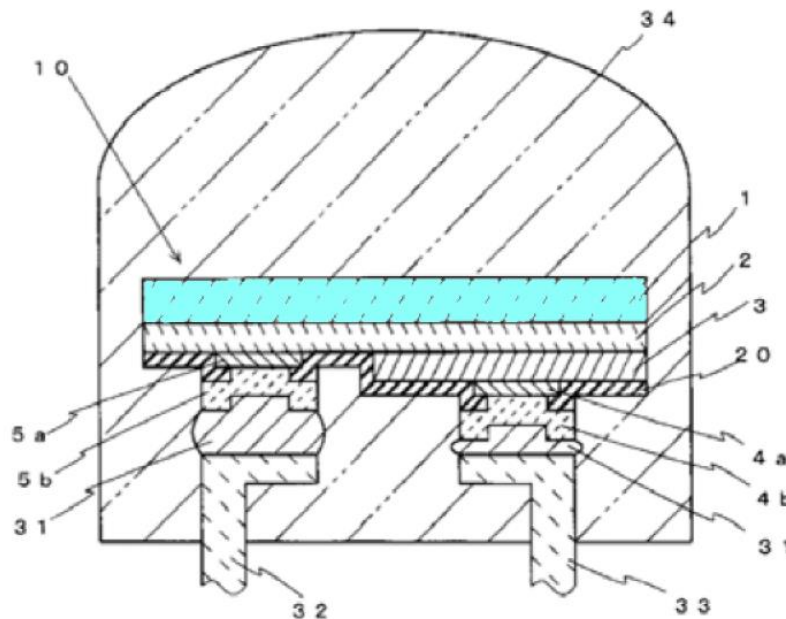
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128. The “LED component” illustrated in Terashima FIG. 5 (Ex-1004 at ¶¶ [0001], [0062], [0070], Claim 10), which is reproduced below, is the “semiconductor light-emitting element” claimed in claim 1’s preamble. The Terashima disclosure includes a flip-chip LED component which satisfies claim 1’s preamble (Ex-1010 at ¶ [0062]).

9.1.1.2. Terashima Discloses the Substrate Limitation

129. It is my opinion that Terashima discloses “a light-transmitting element substrate.” For example, Terashima discloses a “transparent insulating substrate 1” [blue] which is the claimed “light-transmitting element substrate,” as shown in the below annotated Terashima FIG. 5 (Ex-1010 at ¶¶ [0032], [0061], “Description of Reference Numerals” at “1”). Terashima discloses that the substrate 1 can be sapphire, which is transparent and is light-transmissive, and is described as “transparent” (Ex-1010 at ¶¶ [0032], [0061]).

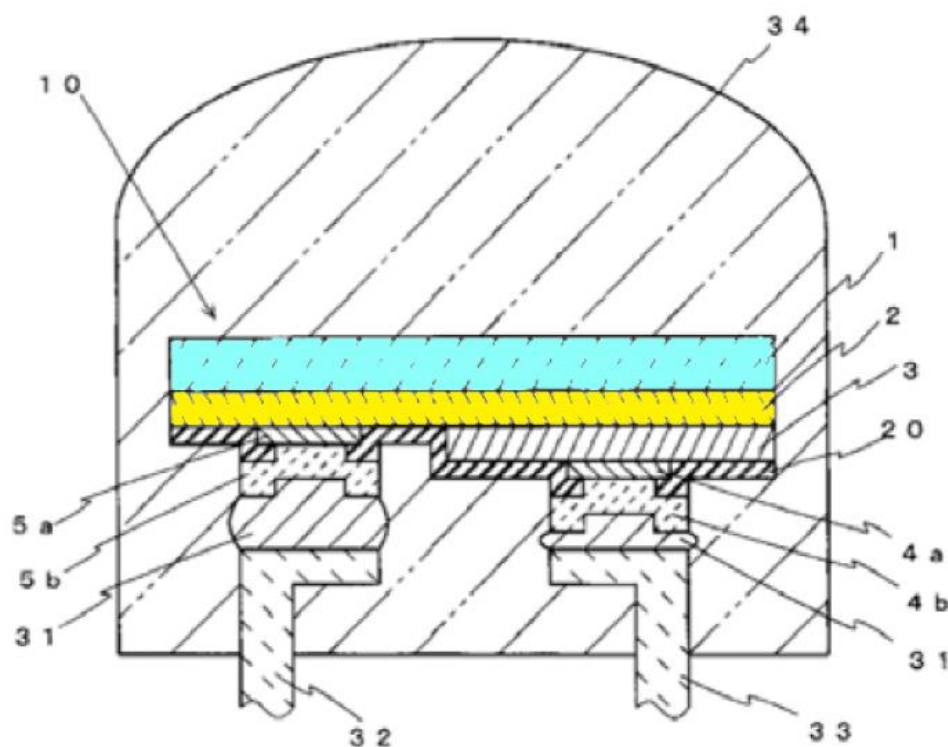
Terashima, FIG. 5 (Annotated)



9.1.1.3 Terashima Discloses the N-type Layer Limitation

130. It is my opinion that Terashima’s “n-type nitride semiconductor layer 2” [yellow] is the claimed “n-type semiconductor layer formed on the element substrate so as to cover the element substrate” (Ex-1010 at ¶¶ [0017], [0032], [0061], “Description of Reference Numerals” at “2”). As shown in FIG. 5, Terashima’s n-type nitride semiconductor layer 2 [yellow] is formed on and covers the transparent substrate 1 [blue] (e.g., the claimed “light-transmitting element substrate”) (Ex-1010 at ¶ [0062]). Terashima explains that the n-type semiconductor layer is “formed” on “the entire surface of a transparent insulating substrate 1” (Ex-1010 at ¶¶ [0032], [0061]).

Terashima FIG. 5 (Annotated)



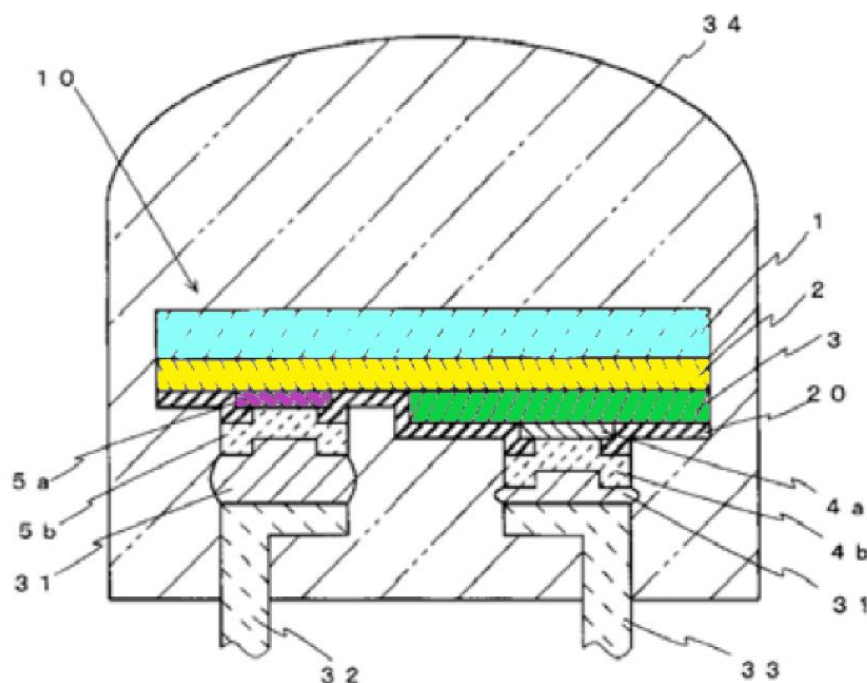
9.1.1.4. Terashima Discloses the P-type Layer Limitation

131. It is my opinion that Terashima's "p-type nitride semiconductor layer 3" is the claimed "p-type semiconductor layer formed so as to cover an area on the n-type semiconductor layer from which an area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer." Terashima's "metal plating film 5a" is the claimed "n-electrode." As shown in FIG. 5, the p-type nitride semiconductor layer 3 [green] is "formed so as to cover an area on the n-type semiconductor layer" 2 [yellow] (Ex-1010 at ¶¶ [0032], [0061]). As is also shown below, the p-type nitride semiconductor

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layer 3 [green] is “excluded” from the areas where the first n-electrode [purple] is in contact with the n-type semiconductor layer 2 [yellow] and the areas where the first n-electrode and the p-type semiconductor layer do not cover the n-type semiconductor layer. As Terashima explains, after the p-type semiconductor layer is formed, a portion of the p-type semiconductor layer is “removed” to expose a portion of the underlying n-type semiconductor layer for an n-electrode to be formed on the n-type semiconductor layer (Ex-1001 at ¶¶ [0033]-[0035]). Terashima further describes that when “a predetermined voltage between the p-electrode 4b and the n-electrode 5b, holes from the p-electrode 4b and electrons from the n-electrode 5b [become light that can] be emitted by recombination near the junction interface between the [n]-type nitride semiconductor layer 2 [yellow] and the p-type nitride semiconductor layer 3 [green]” (Ex-1010 at ¶ [0030]).

Terashima FIG. 5 (Annotated)



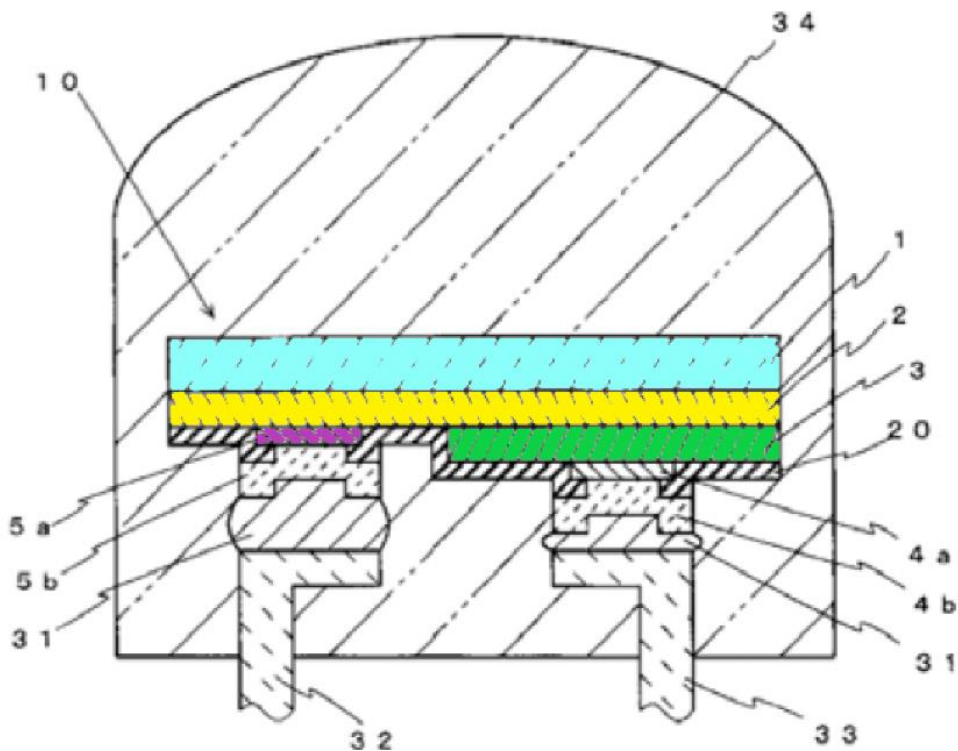
9.1.1.5. Terashima Discloses the First N-electrode Limitation

132. It is my opinion that Terashima’s “plated growth film” 5a [purple], with “metal as the main component” is the claimed “first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer.” Terashima describes the first n-electrode 5a as a “plated growth film,” “thin,” and formed by a “film deposition method, such as vacuum deposition, sputtering, or printing” (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]), which are processes known for making thin film electrodes. Terashima also explains that the film 4a or first n-

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electrode must be “thin enough to maintain transparency” (Ex-1010 at ¶ [0035]). Terashima further describes that the first n-electrode 5a is “provided on a portion of the n-type nitride semiconductor material” 2 [yellow] (FIG 5. below) (Ex-1010 at ¶ [0034]).

Terashima FIG. 5 (Annotated)



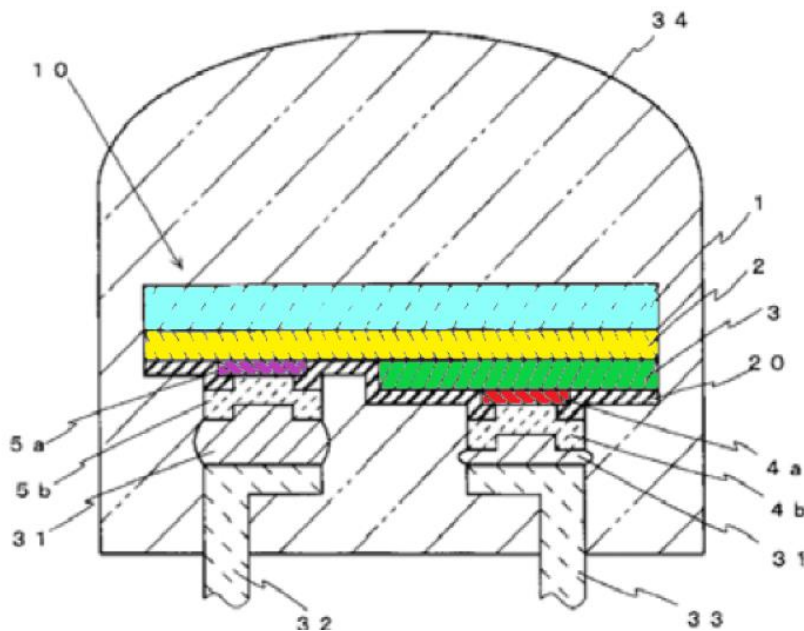
9.1.1.6. Terashima Discloses the First P-electrode Limitation

133. It is my opinion that Terashima’s “plated growth film 4a” [red] is the claimed “first p-electrode that is a thin film formed on the p-type semiconductor layer.” Terashima describes the first p-electrode 5a is a “plated growth film,” “thin,” and formed with a “film deposition method, such as vacuum deposition, sputtering,

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or printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]), which are processes known for making thin film electrodes. The metal plating film 4a [red] is “provided on an upper layer of the p-type nitride semiconductor 3” [green] (FIG 5. below) (Ex-1010 at ¶ [0034]).

Terashima FIG. 5 (Annotated)



9.1.1.7. Terashima Discloses the First Insulating Layer Limitation

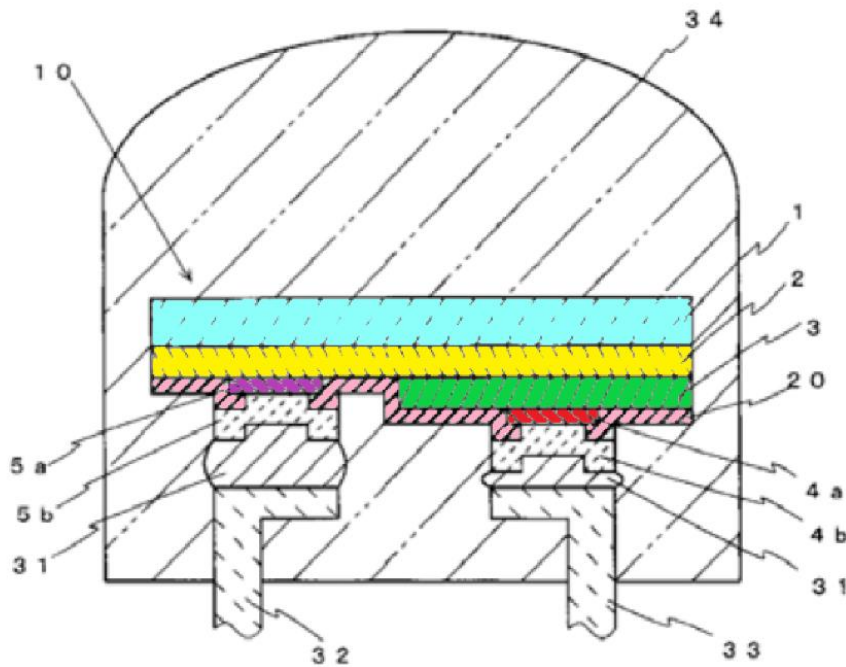
134. It is my opinion that Terashima’s “protective film 20” [pink] is the claimed “first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other.” Terashima’s “protective film 20” [pink] is made from a “material having good insulating properties such as silicon oxide

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(SiO₂) or silicon nitride (Si₃N₄)” (Ex-1010 at ¶¶ [0036], [0061]; *see also* ¶ [0037]).

As shown in FIG. 5, the protective film 20 [pink] “is formed so as to insulate the first n-electrode and the first p-electrode from each other.”

Terashima FIG. 5 (Annotated)



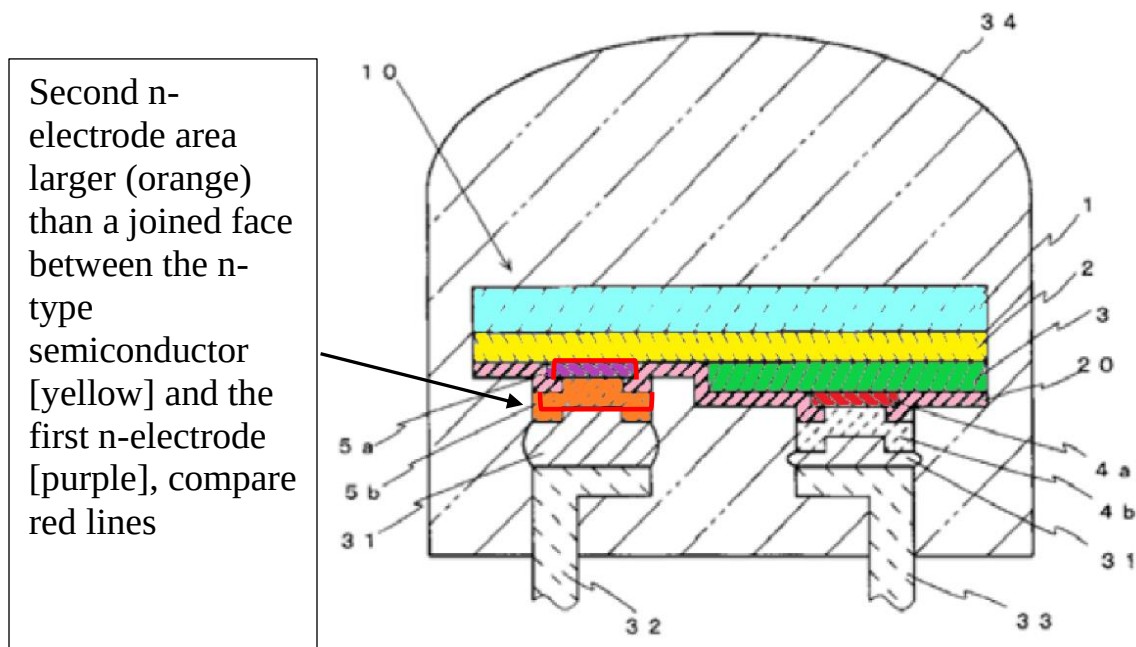
9.1.1.8. Terashima Discloses the Second N-electrode Limitation

135. It is my opinion that Terashima’s “n electrode 5b” [orange] is the claimed “second n-electrode formed on the first n-electrode and the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode, the second n-electrode being insulated from the first p-electrode by the first insulating layer.” As shown in FIG. 5, the “n electrode

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5b” [orange] is provided on or “formed” on the first n-electrode (*i.e.*, Terashima’s “metal film 5a” [purple]) and the first insulating layer (*i.e.*, Terashima’s “protective layer 20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0037], [0046], [0053], [0051], [0059], [0061]). Terashima describes the second n-electrode is a “film” or “single layer film” (e.g., “thin”) (Ex-1010 at ¶ [0038], [0059]). As shown in FIG. 5, the “n electrode 5b” [orange] has “an area larger than a joined face between the n-type semiconductor” (*i.e.*, “n-type nitride semiconductor layer 2” [yellow]) and the first n-electrode,” (*i.e.*, “metal film 5a” [purple]).

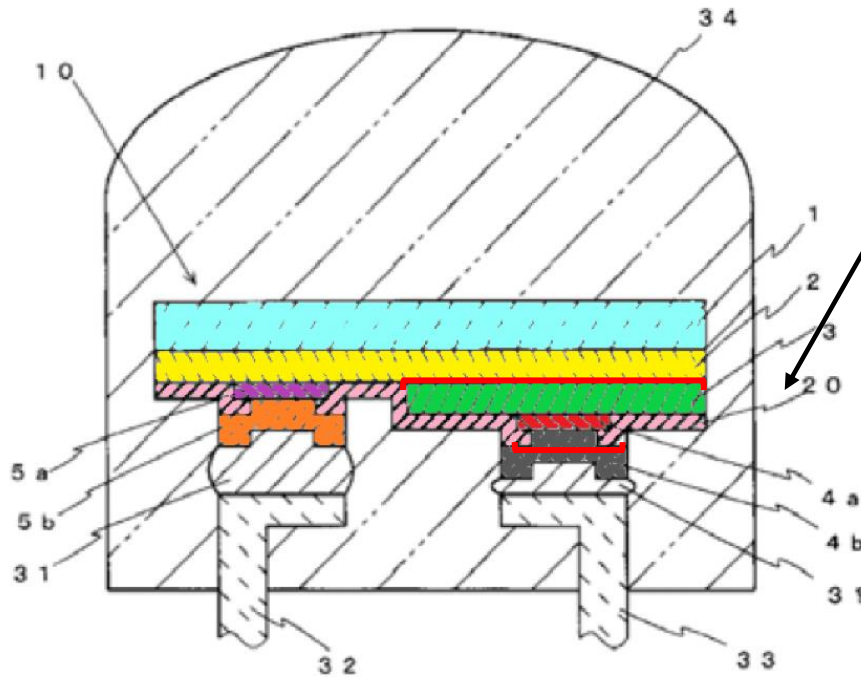
Terashima FIG. 5 (Annotated)



9.1.1.9. Terashima Discloses the Second P-electrode Limitation

136. For the below reasons, it is my opinion that Terashima’s “p electrode 4b” [gray] is the claimed “second p-electrode formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode.” Terashima describes the second p-electrode as a “film” or “single layer film” (*e.g.*, “thin”) (Ex-1010 at ¶ [0038], [0059]). Further, Terashima FIG. 5 shows the “p electrode 4b” [gray] is “provided on” or “formed on” the first p-electrode (*i.e.*, Terashima’s “metal film 4a” [red]) and the first insulating layer (*i.e.*, Terashima’s “protective layer 20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0038], [0046], [0053], [0059], [0061]). As shown in FIG. 5, Terashima’s second “p electrode 4b” [gray] also has “an area smaller than a joined face between the n-type semiconductor layer” (*i.e.*, “n-type nitride semiconductor layer 2” [yellow]) and the p-type semiconductor layer” (*i.e.*, “p-type nitride semiconductor layer 3” [green]).

Terashima FIG. 5 (Annotated)



9.1.2. Terashima Anticipates Independent Claim 2

137. For the below reasons, it is my opinion that Terashima discloses claim 2’s preamble and the first five elements as described above with reference to claim 1.

138. Terashima’s structure that satisfies the remaining claim 2 limitations is provided below with the following color references.

Reference	Claim 2 Limitations
Preamble	“optical semiconductor device (LED component)”

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Substrate	“transparent insulating substrate 1” [blue]
n-type layer	“n-type nitride semiconductor layer 2” [yellow]
p-type layer	“p-type nitride semiconductor layer 3” [green]
first n-electrode	“plated growth film 5a” [purple]
first p-electrode	“plated growth film 4a” [red]
first insulating layer (2)	“protective film 20” [pink]
second n-electrode (2)	“n electrode 5b” [orange]
second p-electrode (2)	“p electrode 4b” [gray]

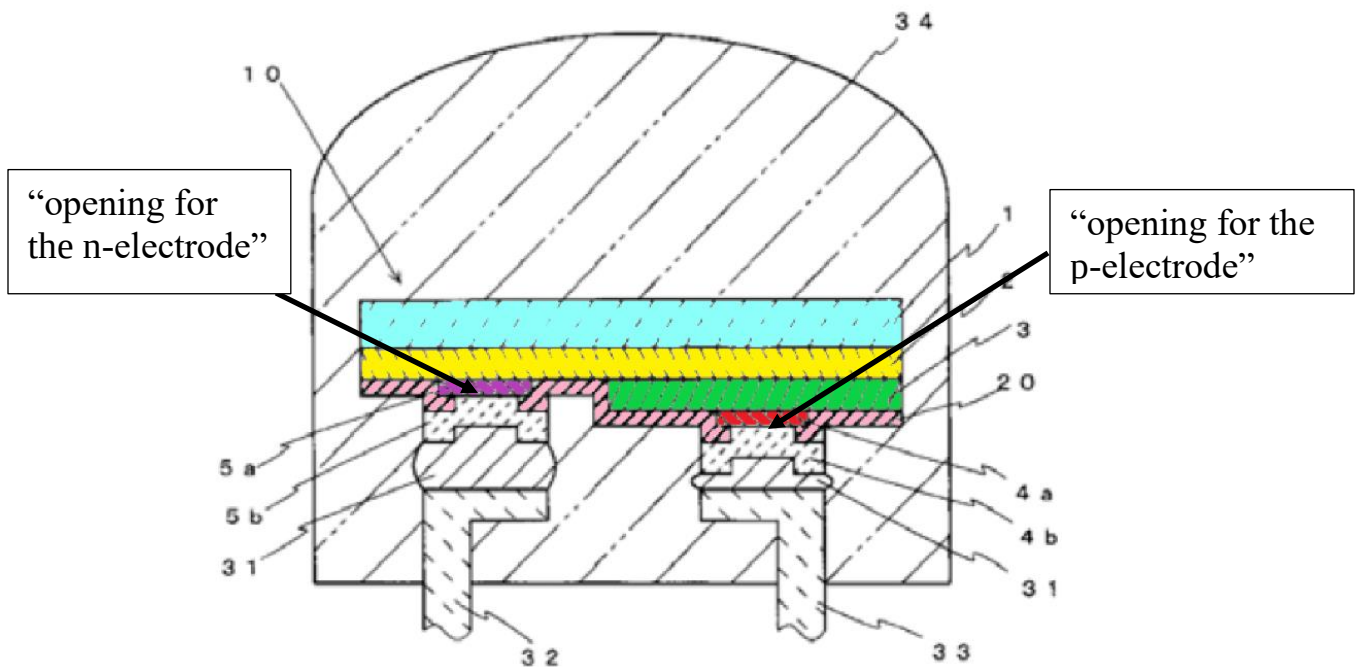
9.1.2.1 Terashima Discloses Claim 2’s First Insulating Layer Limitation

139. Terashima’s “protective film 20” [pink] is the claimed “a first insulating layer having at least one opening for the n-electrode and one opening for the p-electrode formed therein, which covers the first n-electrode and the first p-electrode so as to insulate the first n-electrode and the first p-electrode from each other, except for the opening for the n-electrode and the opening for the p-electrode.” Terashima’s “protective film 20” [pink] is made from a “material having good insulating properties such as silicon oxide (SiO₂) or silicon nitride (Si₃N₄)” (Ex-1010 at ¶¶ [0036], [0061]; *see also* ¶ [0037]). As shown in FIG. 5, the protective film 20 [pink]

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covers the first n-electrode and first p-electrode and is formed so as to insulate the first n-electrode and the first p-electrode from each other. The protective film 20 [pink] is also described to have an “opening for the n-electrode” and an “opening for the p-electrode” (Ex-1010 at ¶¶ [0020], [0029]) to allow for electrical connections to the n-type semiconductor layer 2 [yellow] and p-type semiconductor layer 3, respectively.

Terashima FIG. 5 (Annotated)



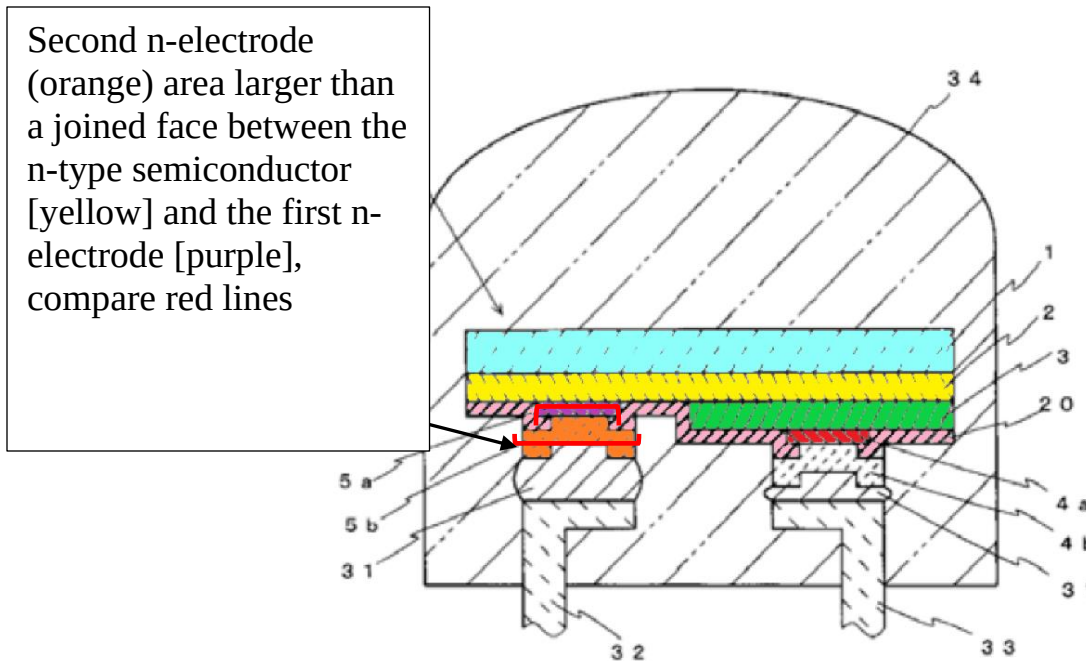
9.1.2.2 Terashima Discloses Claim 2’s Second N-Electrode Limitation

140. Terashima’s “n electrode 5b” [orange] is the claimed “a second n-electrode formed on the first insulating layer as a thin film having an area larger than

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a joined face between the n-type semiconductor layer and the first n-electrode, the second n-electrode being electrically connected to the first n-electrode through the opening for the n-electrode of the first insulating layer.” FIG. 5 shows that the “n electrode 5b” [orange] is provided on or “formed” on the first insulating layer (*i.e.*, Terashima’s “protective layer 20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0037], [0046], [0053], [0051], [0059], [0061]). Terashima describes the second n-electrode as a “film” or “single layer film” (*e.g.*, “thin”) (Ex-1010 at ¶ [0038], [0059]). Terashima also shows in FIG. 5, the “n electrode 5b” [orange] has “an area larger than a joined face between the n-type semiconductor” (*i.e.*, n-type nitride semiconductor layer 2 [yellow]) and “the first n-electrode,” (*i.e.*, “metal film 5a” [purple]) and is “electrically connected to the first n-electrode through the opening for the n-electrode of the first insulating layer” (*see* Ex-1010 at ¶ [0062] describing electrical connections).

Terashima FIG. 5 (Annotated)



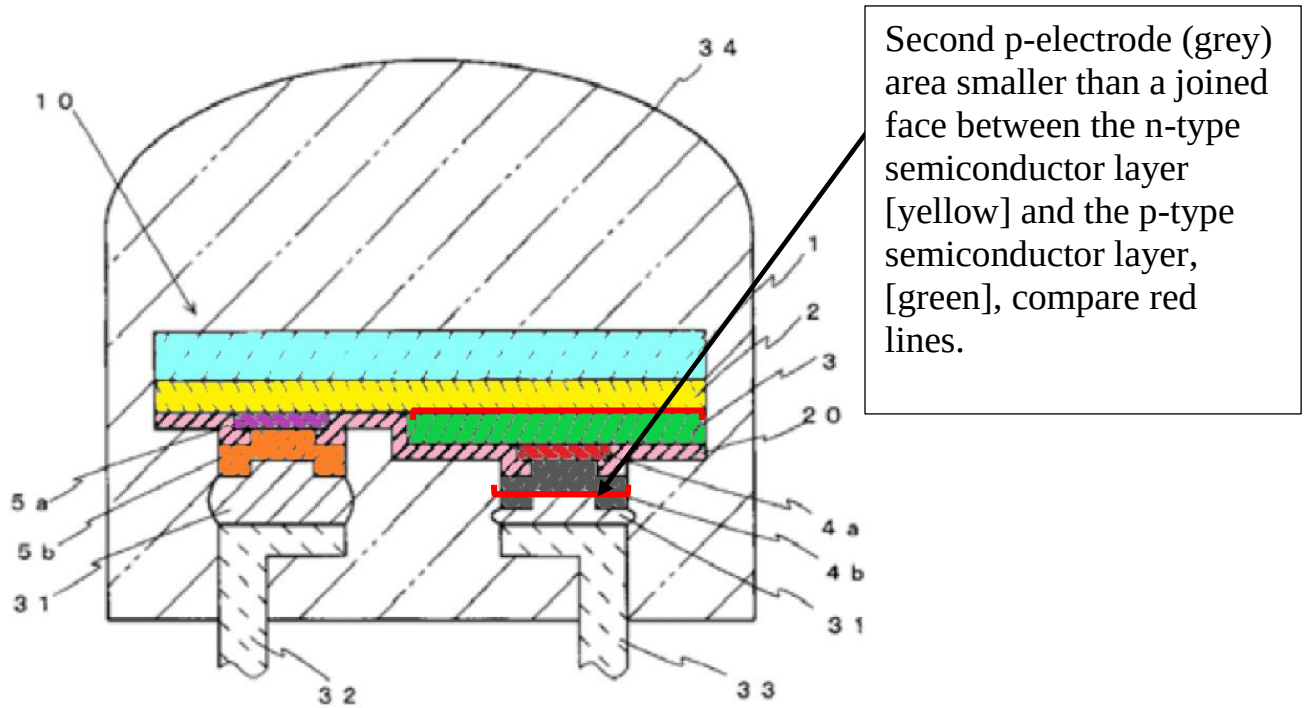
9.1.2.3 Terashima Discloses Claim 2's Second P-Electrode Limitation

141. Terashima's "p electrode 4b" [gray] is the claimed "a second p-electrode formed on the first insulating layer as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode through the opening for the p-electrode of the first insulating layer." Terashima describes the second p-electrode as a "film" or "single layer film" (*e.g.*, "thin") (Ex-1010 at ¶¶ [0038], [0059]). Further, FIG. 5 shows the "p electrode 4b" [gray] is "provided on" or "formed on" the first insulating layer (*i.e.*, Terashima's "protective layer 20" [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0038], [0046], [0053], [0059], [0061]). Terashima's second "p electrode 4b" [gray] also has "an area

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smaller than a joined face between the n-type semiconductor layer” (*i.e.*, n-type nitride semiconductor layer 2 [yellow]) and “the p-type semiconductor layer” (*i.e.*, p-type nitride semiconductor layer 3 [green])” and is “electrically connected to the first p-electrode through the opening for the p-electrode of the first insulating layer” (*see* Ex-1010 at ¶ [0062] describing electrical connections).

Terashima FIG. 5 (Annotated)



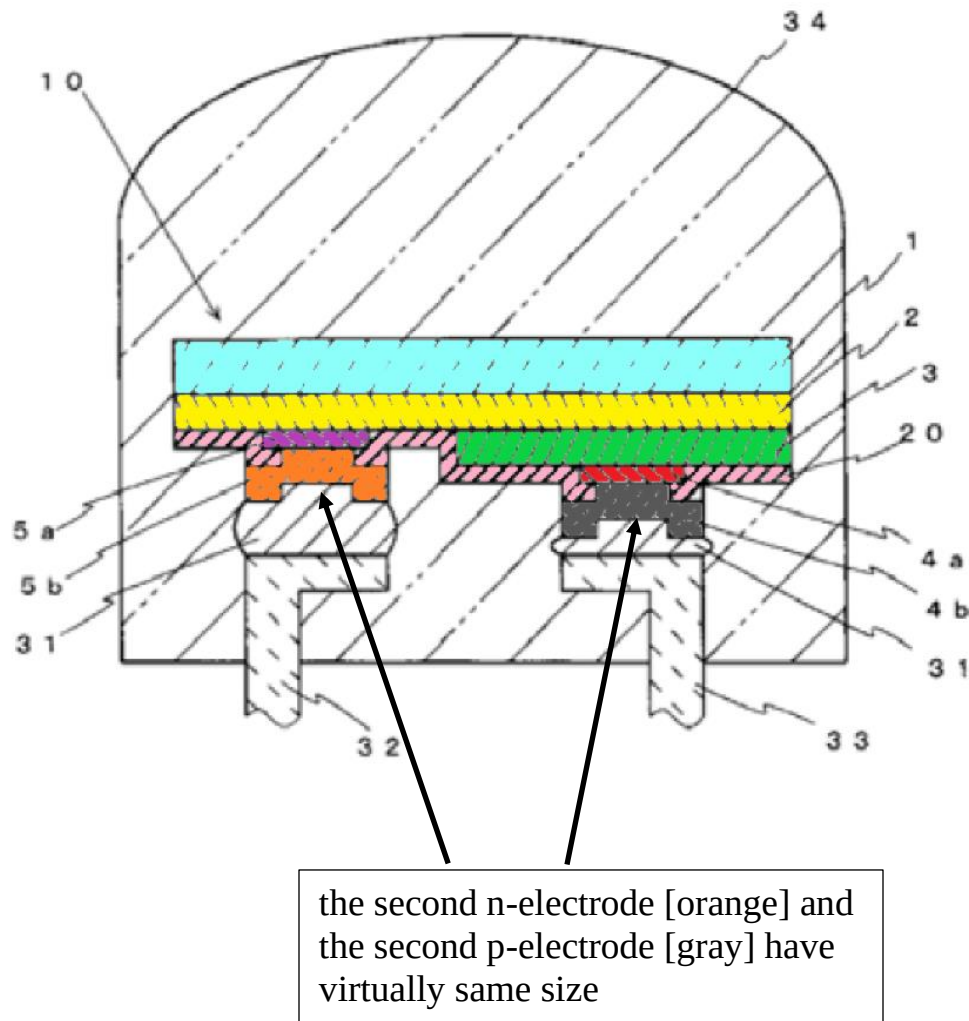
9.1.3. Terashima Anticipates Claim 5

142. Terashima discloses that “the second n-electrode” (*i.e.*, n electrode 5b [orange]) and the second p-electrode (*i.e.*, p electrode 4b [orange]) have virtually same size.” For example, FIG. 5 shows that the n-electrode 5b [orange] and the p-electrode 4b [gray] “have virtually same size.” Terashima provides an example

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where the second n and p electrodes 4b, 5b “can be “formed to a desired thickness” (e.g., virtually the same thickness) (Ex-1010 at ¶ [0038]).

Terashima, FIG. 5 (Annotated)

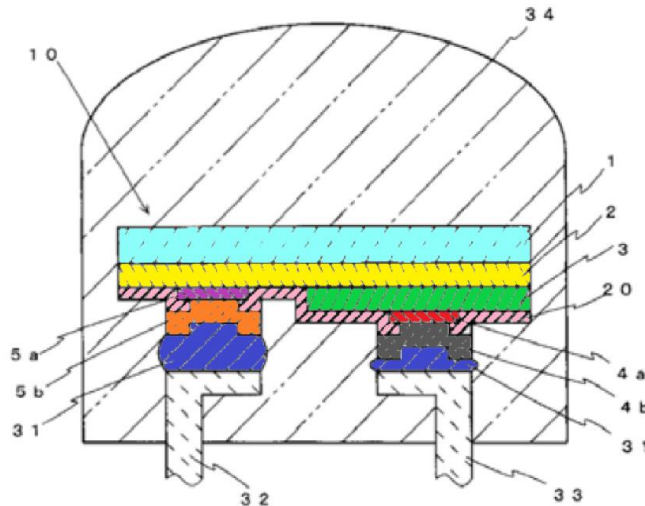


9.1.4. Terashima Anticipates Claim 6

143. Terashima discloses (FIG. 5) solder 31 [indigo] which is “used to fuse” electrodes 5b [orange] and 4b [gray] “to the lead frames 32, 33” for “electrical connection” (Ex-1010 at [0062]). Solder is the claimed “conductive layer.”

Terashima, FIG. 5 (Annotated)

[Figure 5]



9.1.5. Terashima Anticipates Claim 7

144. Claim 7 recites a “light-emitting device comprising: the semiconductor light-emitting element according to claim 1; a circuit board having a plurality of electrodes; and a conductive bonding material layer that electrically connects and fixes the second n-electrode and the second p-electrode to the electrodes on the circuit board.”

145. Terashima discloses solder 31 [indigo] which is “used to fuse” electrodes 5b [orange] and 4b [gray] “to the lead frames 32, 33 [brown]” for electrical connection (Ex-1010 at [0062]). A POSITA would have understood that the lead frames 32, 33 [brown] are a “plurality of electrodes” that are inherently connected to a circuit board or other electrical component. In my opinion, it was

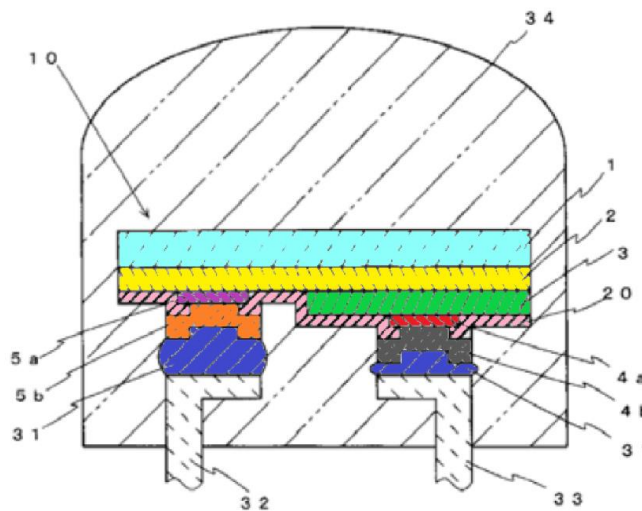
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well known that “flip-chip mounted” LEDs, such as the “semiconductor element” of Terashima (Ex-1010 at [0062]) were mounted on circuit boards.

9.1.6. Terashima Anticipates Claim 8

146. Terashima anticipates claim 8. For example, Terashima discloses (FIG. 5) solder 31 [indigo] which is “used to fuse” electrodes 5b [orange] and 4b [gray] “to the lead frames 32, 33” for electrical connection (Ex-1010 at ¶ [0062]). Solder is the claimed “conductive layer.”

Terashima, FIG. 5 (Annotated)



9.1.7. Terashima Anticipates Claim 9

147. Claim 9 is the corresponding method recited in claim 1. Thus, Terashima anticipates claim 9 for the reasons described with respect to claim 1 (*see supra* §9.1.1.).

9.1.8. Terashima Anticipates Claim 10

148. Claim 10 is the corresponding method recited in claim 2. Thus, Terashima anticipates claim 10 for the reasons described with respect to claim 2 (*see supra* § 9.1.2).

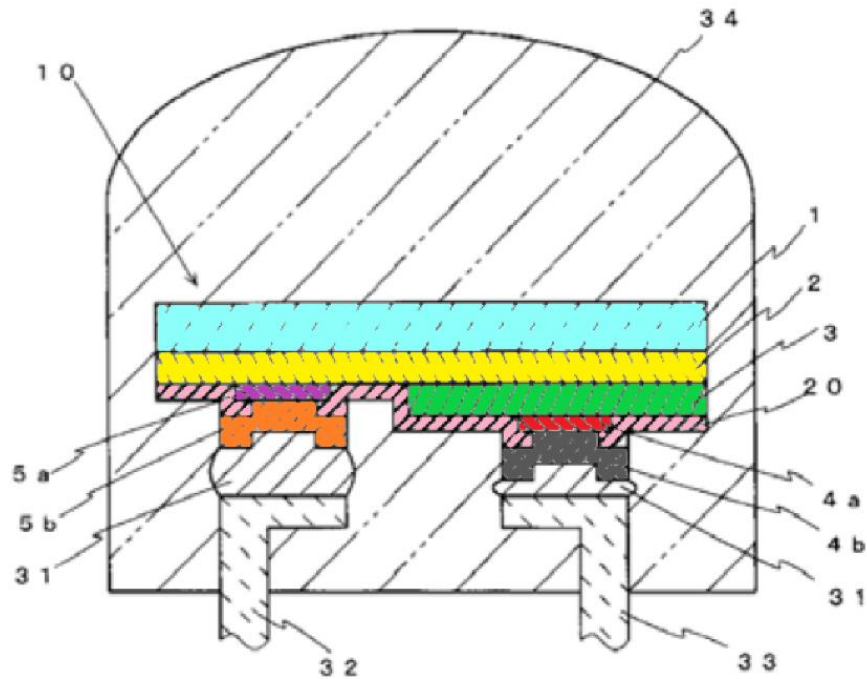
9.1.9. Terashima Anticipates Claim 11

149. Claim 11 reads: “[t]he method for manufacturing a semiconductor light-emitting element according to claim 10, wherein the first insulating layer is formed through sputtering is the corresponding method recited in claim 1.” Terashima anticipates claim 11. For example, Terashima teaches that the protective film 20, which is the claimed “first insulating layer,” “is formed by a film forming means such as vacuum deposition or sputtering” (Ex-1010 at ¶ [0036]).

9.1.10. Terashima Anticipates Claim 12

150. Claim 12 reads: “[t]he method for manufacturing a semiconductor light-emitting element according to claim 9, wherein the second n-electrode and the second p-electrode are formed through sputtering or plating.” Terashima anticipates claim 12. For example, Terashima discloses that electrodes 4b, 5b, which are the claimed second n- and p-electrodes, respectively, can be formed by “plating” (Ex-1010 at ¶ [0034]).

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9.2. Sugimoto Anticipates Claims 1, 5, 6, 9, & 12

151. It is my opinion that Sugimoto (Ex-1006) anticipates claims 1, 5, 6, 9, and 12. Sugimoto discloses each limitation in these claims.

9.2.1. Sugimoto Anticipates Claim 1

152. Sugimoto discloses each element of claim 1 as described below. Sugimoto references that satisfy claim 1 are set forth with reference to the colors below.

Claim 1 Element	Sugimoto Disclosure
Preamble	“nitride semiconductor device”
substrate	“substrate 101” [blue]

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n-type layer	“n-type nitride semiconductor layer 102” [yellow]
p-type layer	“p-type nitride semiconductor layer 103” [green]
first n-electrode	“first n electrode 107” [purple]
first p-electrode	“first p electrode 105” [red]
first insulating layer	“insulating layer 110” [pink]
second n-electrode	“second n electrode 108” [orange]
second p-electrode	“second p electrode 106” [gray]

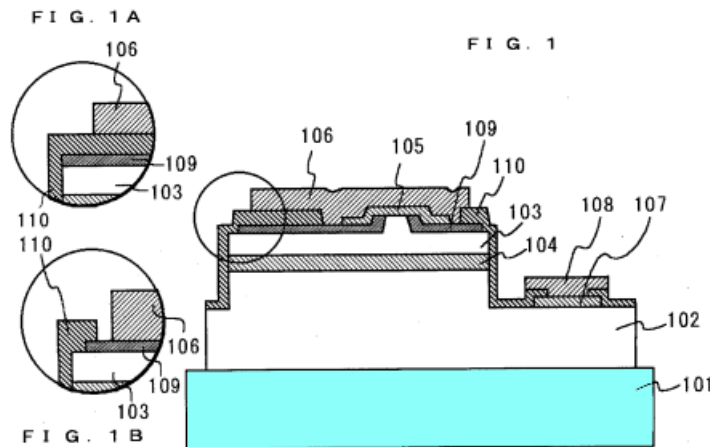
9.2.1.1. Sugimoto Discloses Claim 1’s Preamble

153. Sugimoto discloses “a semiconductor light-emitting element.” For example, Sugimoto describes a “nitride semiconductor device” that emits light (Ex-1006 at ¶¶ [0005]; [0012]; [0074]; [0086]; [0103]).

9.2.1.2. Sugimoto Discloses the Substrate Limitation

154. Sugimoto discloses “a light-transmitting element substrate.” For example, Sugimoto FIGs. 1A and 1B disclose a nitride semiconductor device having “substrate 101” [blue] (Ex-1006 at ¶ [0072]; *see also* ¶¶ [0005], [0107], [0108]). Sapphire is used as a substrate (Ex-1006 at ¶ [0018]), which is light-transmitting.

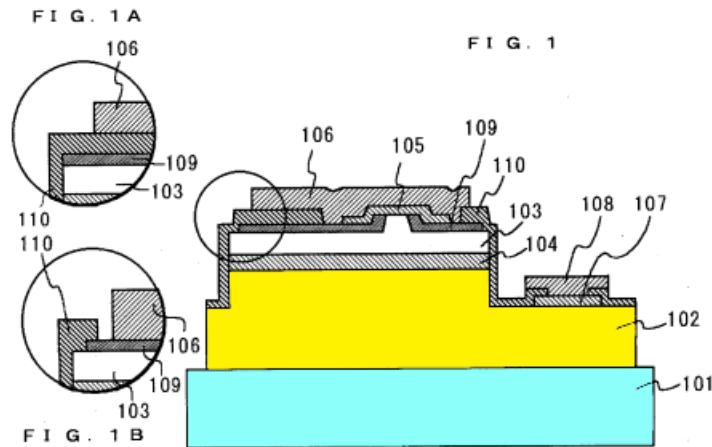
Sugimoto Figs. 1, 1A, 1B (Annotated)



9.2.1.3. Sugimoto Discloses the N-Type Layer Limitation

155. Sugimoto discloses “an n-type semiconductor layer formed on the element substrate so as to cover the element substrate.” For example, Sugimoto discloses a nitride semiconductor device having “n-type semiconductor layer 102” [yellow] (Ex-1006 at ¶¶ [0072]-[0073]). Sugimoto Figs. 1, 1A, and 1B disclose the “an n-type semiconductor layer 102” [yellow] is “formed on the element substrate 101 [blue] so as to cover the element substrate 101 [blue].”

Sugimoto Figs. 1, 1A, & 1B (Annotated)



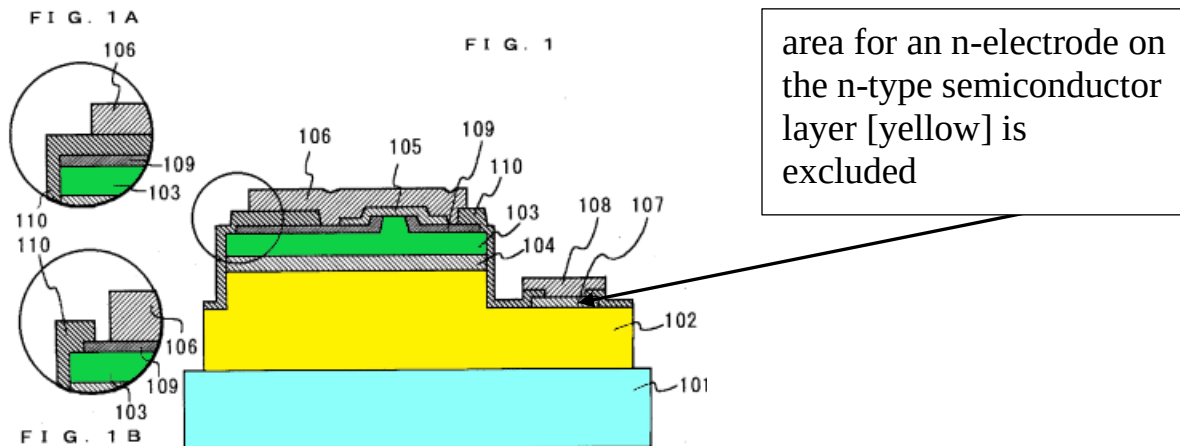
9.2.1.4. Sugimoto Discloses the P-Type Layer Limitation

156. Sugimoto discloses a “p-type semiconductor layer” (*i.e.*, “p-type nitride semiconductor layer 103” [green]) formed so as to cover an area on the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]) from which an area for an n-electrode (*i.e.*, “first n electrode 107” [purple]) on the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]) is excluded, for emitting light in cooperation with the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]). For example, Sugimoto discloses a nitride semiconductor device having “p-type nitride semiconductor layer 103” [green] (Ex-1006 at ¶¶ [0072]-[0073]). Sugimoto FIGs. 1, 1A, and 1B disclose that the p-type layer 103 [green] covers the n-type semiconductor layer 102 [yellow] and has an “area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer.” P-type nitride

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semiconductor layer 103 [green]) emits light in cooperation with n-type semiconductor layer 102 [yellow] via their junction at active layer 104 (Ex-1006 at ¶¶ [0072]-[0074]). While Sugimoto discloses an active layer 104 between the p-type nitride semiconductor layer 103 and the n-type semiconductor layer 102, there is always an active layer between these layers in an LED, so “formed on” in this context must mean there is an active layer between the p-type nitride semiconductor layer 103 and the n-type semiconductor layer 102.

Sugimoto Fig. 1, 1A, & 1B (Annotated)



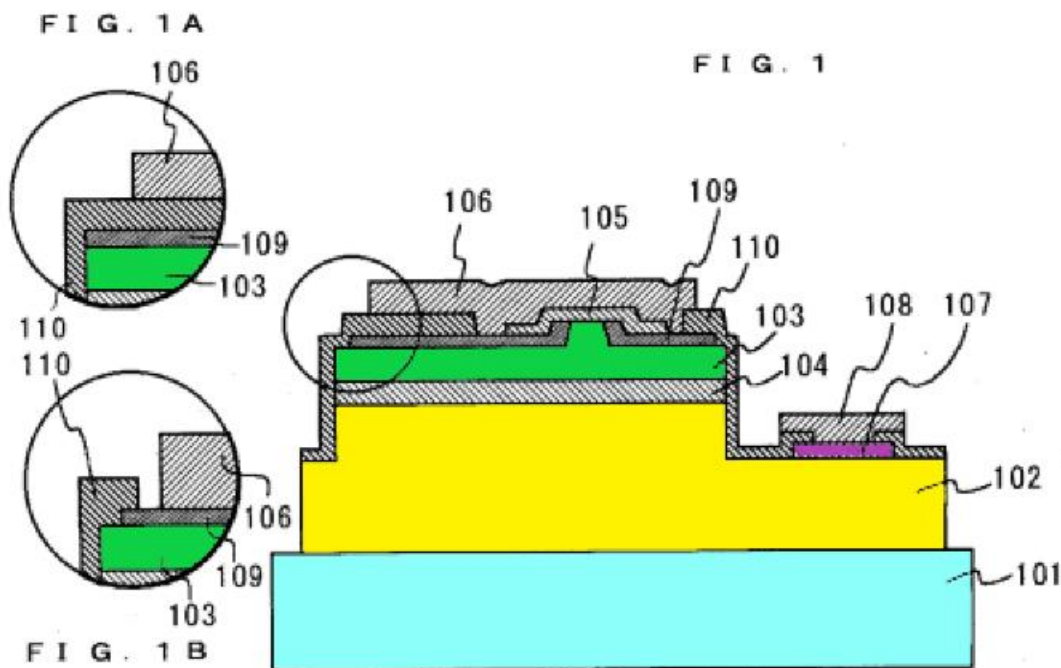
9.2.1.5. Sugimoto Discloses the First N-electrode Limitation

157. Sugimoto discloses “a first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer.” For example, Sugimoto discloses a first n-type electrode 107 [purple] that is a thin film formed on the area of the n-electrode of the n-type semiconductor layer (Ex-1006 at ¶ [0073]).

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Sugimoto discloses “thin film” electrodes and describes that the first n-electrode preferably has a thickness in the range of about 100 to 30,000 angstroms (0.01 to 3 micrometers) (Ex-1006 at ¶¶ [0061]-[0064]).

Sugimoto Fig. 1, 1A, & 1B (Annotated)



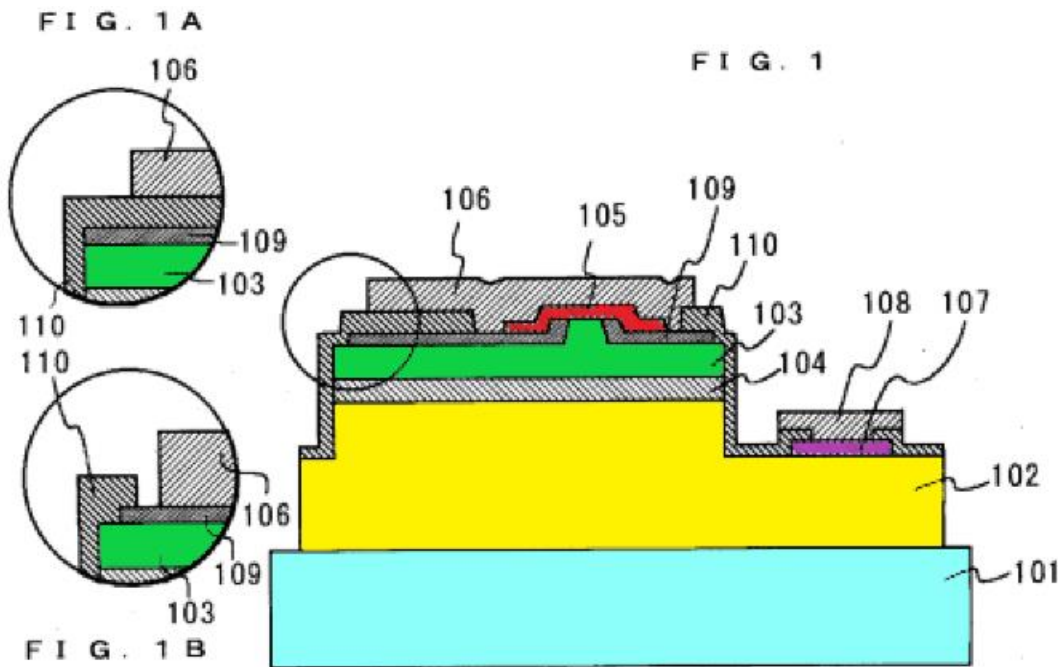
9.2.1.6. Sugimoto Discloses the First P-Electrode Limitation

158. Sugimoto discloses “a first p-electrode that is a thin film formed on the p-type semiconductor layer.” For example, Sugimoto discloses a nitride semiconductor device having “a first p electrode 105” [red] (Ex-1006 at ¶¶ [0073], [0075]). Sugimoto discloses that the first p-electrode is a thin “film” electrode (Ex-1006 at ¶¶ [0061]-[0064], [0067]). Sugimoto discloses “thin film” electrodes and describes that the first n-electrode preferably has a thickness in the range of about

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100 to 30,000 angstroms (0.01 to 3 micrometers) (Ex-1006 at ¶¶ [0061]-[0064]). A POSITA would understand that Sugimoto discloses that the first p-electrode has the same preferable dimensions as the first n-electrode because the two first electrodes are extensively described together regarding layers, materials, and manufacturing (Ex-1006 at ¶¶ [0014]-[0018]; [0020]-[0034], [0053], [0055], [0059]).

Sugimoto Figs. 1, 1A, & 1B (Annotated)



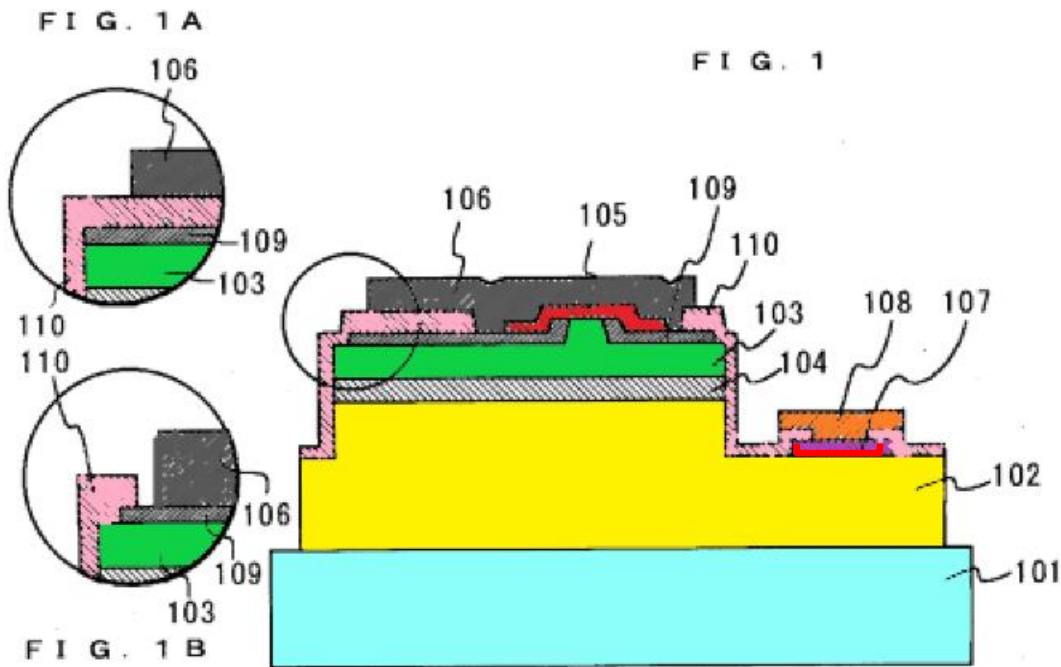
9.2.1.7. Sugimoto Discloses the First Insulating Layer Limitation

159. Sugimoto discloses “a first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other.” For example, Sugimoto discloses a nitride semiconductor device having “second insulating layer 110” [pink] (Ex-1006 at ¶¶ [0073], [0075]). Although Sugimoto’s “second

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insulating layer 110” is referred to as a “second” layer, Sugimoto’s “second insulating layer 110” satisfies the claimed “first insulating layer” limitations. Sugimoto explains that the insulating layer 110 prevents “short circuit between the p-side electrodes and the n-side electrodes” and “is provided over the entire surface of the composite structure except the upper surface of the [second electrodes] (Ex-1006 at ¶¶ [0075], [0081]). As shown in FIG. 1, Sugimoto’s “insulating layer” 110 electrically insulates current from flowing between the first n-electrode 107 (purple) and the first and second p-electrodes 105, 106 (red, grey).

Sugimoto Figs. 1, 1A, & 1B (Annotated)

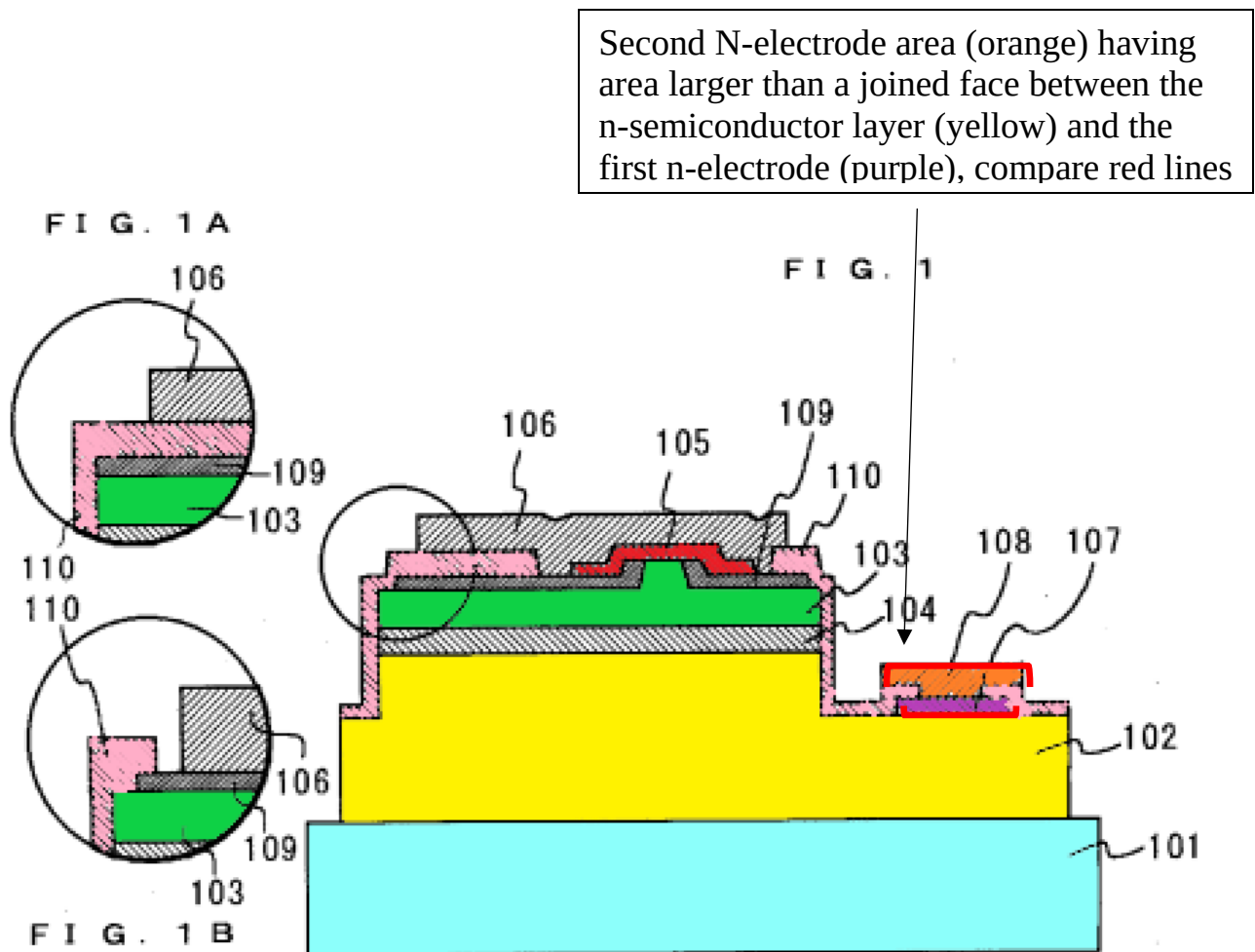


9.2.1.8. Sugimoto Discloses the Second N-Electrode Limitation

160. As shown in FIG. 1, Sugimoto discloses “a second n-electrode” (*i.e.*, second n electrode 108 [orange]) formed on the first n-electrode (*i.e.*, first n electrode 107 [purple]) and the first insulating layer (*i.e.*, insulating layer 110 [pink]) as a thin film having an area larger than a joined face between the n-type semiconductor (*i.e.*, n-type semiconductor layer 102 [yellow]) and the first n-electrode (*i.e.*, first n electrode 107 [purple]) so that the second n-electrode (*i.e.*, second n electrode 108 [orange]) is electrically connected to the first n-electrode (*i.e.*, first n electrode 107 [purple]), the second n-electrode (*i.e.*, second n electrode 108 [orange]) being insulated from the first p-electrode (*i.e.*, first p electrode 105 [red]) by the first insulating layer (*i.e.*, insulating layer 110 [pink]).

161. Sugimoto discloses that the claimed second n-electrode 108 [orange] is a “thin film” preferably having a thickness in the range of about 3,000 to 20,000 angstroms (0.03 to 0.2 micrometers) (Ex-1006 at ¶¶ [0061]-[0063], [0066]). Sugimoto states that second n-electrode 108 is provided “on first n electrode” (Ex-1006 at ¶ [0073], FIG. 1). In my opinion, Sugimoto discloses a “thin film” for the second n-electrode.

Sugimoto Figs. 1, 1A, & 1B (Annotated)



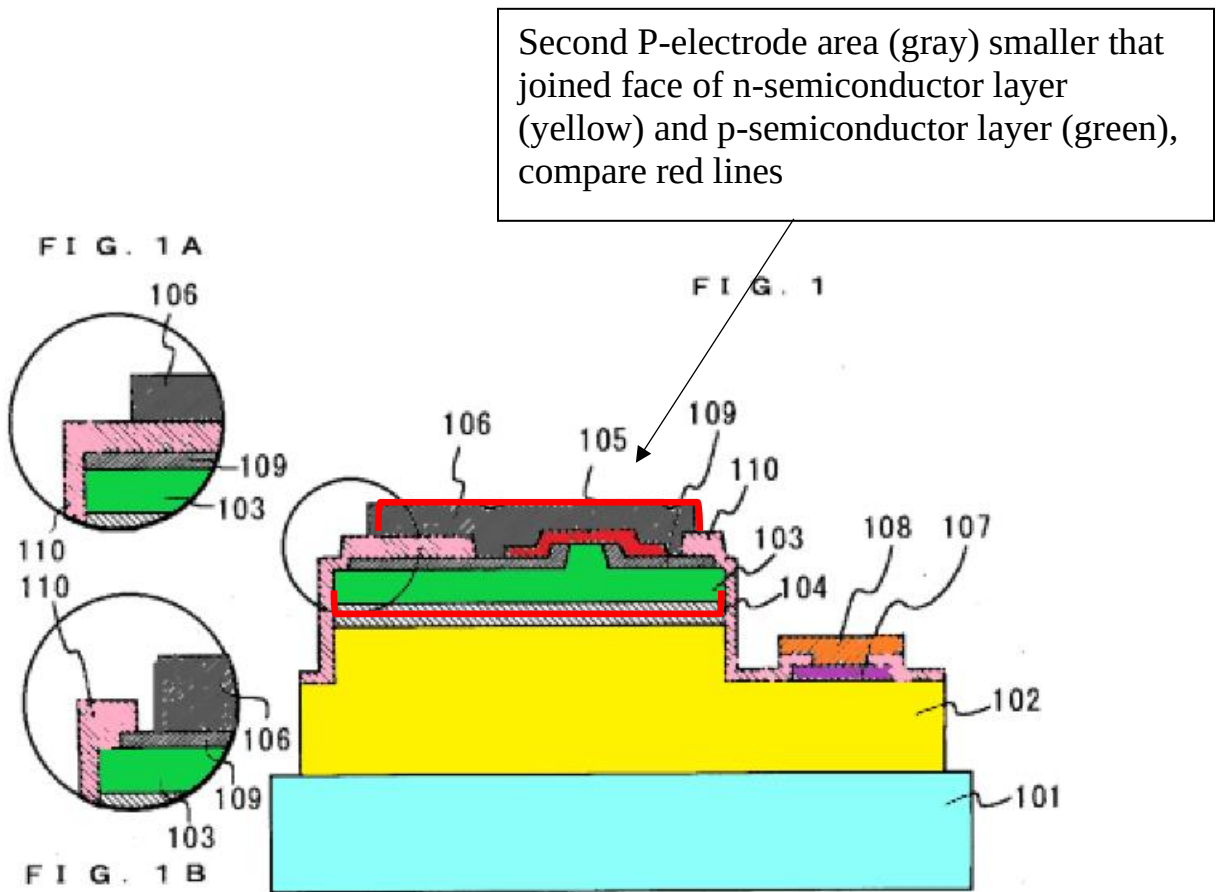
9.2.1.9. Sugimoto Discloses the Second P-Electrode Layer Limitation

162. Sugimoto discloses in FIG. 1 “a second p-electrode” (*i.e.*, second p electrode 106) formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer (*i.e.*, n-type semiconductor layer 102 [yellow]) and the p-type semiconductor layer (*i.e.*, p-type semiconductor layer 103 [green]), the second p-electrode (*i.e.*, second p electrode 106) being electrically

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connected to the first p-electrode (*i.e.*, first p electrode 105). Sugimoto discloses “film” electrodes, and that the second n-electrode preferably has a thickness in the range of about 3,000 to 20,000 angstroms (0.03 to 0.2 micrometers) (Ex-1006 at ¶¶ [0061]-[0063], [0068]). In my opinion, Sugimoto discloses a “thin film” for the second p-electrode.

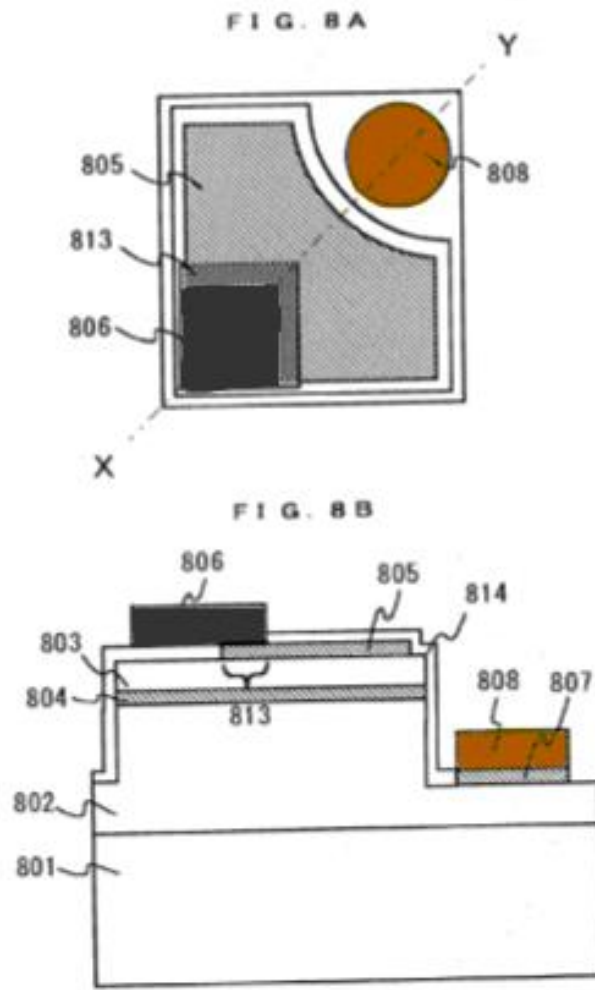
Sugimoto Fig. 1, 1A, & 1B Annotated



9.2.2. Sugimoto Anticipates Claim 5

163. Claim 5 recites that “semiconductor light-emitting element according to claim 1, wherein the second n-electrode and the second p-electrode have virtually same size.” Sugimoto discloses an embodiment in Figure 8 that meets this limitation showing that second p-electrode 806 (gray) and the second n-electrode (orange) 808 have the same thickness and are “virtually the same size” even though they have different shapes (Ex-1006 at ¶ [0103]; Figs. 8A, 8B).

Sugimoto Figs. 8A & 8B



9.2.3. Sugimoto Anticipates Claim 6

164. To the extent that claim 6 has any meaning, Sugimoto anticipates claim 6. Claim 6 recites “where the conductive bonding material layer is any one of members selected from the group consisting of solder, silver paste, and anisotropic resin.” Sugimoto Figure 3 is similar to Figure 1. However, Sugimoto add an adhesion layer 311 “that further enhances the adhesion” between the first and the

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second p electrodes to Figure 1 (Ex-1006 at ¶ [0087]). Sugimoto discloses that “the adhesion layer 311 may be conductive” (Ex-1006 at ¶ [0088]). Sugimoto also discloses that the upper layer of the adhesion layer may be made of silver or gold and the lower layer may be tin (Ex-1006 at ¶ [0089]). Thus, Sugimoto anticipates claim 6.

9.2.4. Sugimoto Anticipates Claim 9

165. Claim 9 is a manufacturing claim that corresponds to claim 1. Sugimoto anticipates claim 1 for the same reasons as described above regarding claim 1.

9.2.5. Sugimoto Anticipates Claim 12

166. Claim 12 recites the “method for manufacturing a semiconductor light-emitting element according to claim 9, wherein the second n-electrode and the second p-electrode are formed through sputtering or plating.” Sugimoto teaches that “second electrodes are formed” by “sputtering” and the “second electrode is deposited by, for example, sputtering” (Ex-1006 at ¶¶ [0155]; [0019]; *see also* ¶¶ [0020], [0021], [0024]).

9.3. Claims 1, 2, & 5-10 are Obvious over Shin Plus One or More of the Thin Film Art

167. Claim 1 is obvious over Shin (Ex-1005) and one or more of Terashima, Sugimoto, Uemura '259, Uemura '999, and/or Inoue (Collectively the “Thin Film Art”). Shin describes all of the limitations of claim 1 with the exception of possibly

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the claimed electrodes being “thin films.” While Shin discloses thin film electrodes to a POSITA, Shin does not use the precise words “thin film.” Therefore, the Thin Film Art is cited as prior art disclosing thin film electrodes. It would have been obvious to a POSITA to combine Shin with one or more of Terashima, Sugimoto, Uemura '259, Uemura '999, and/or Inoue at the time of the alleged invention to form the alleged invention of claim 1.

9.3.1. Claim 1 is Obvious over Shin Plus One or More of the Thin Film Art

168. Shin plus one or more of the Thin Film Art discloses each element of claim 1 as described below. Below I compared the scope and content of the prior art and any differences between the prior art and claim 1. I found no differences. I am not aware of any secondary factors of nonobviousness. I considered the level of ordinary skill in the art particularly that thin film electrodes were well-known and in common use. Based on my analysis and these considerations, it is my opinion that claim 1 is obvious over Shin in view of one or more of the Thin Film Art.

169. Shin and the Thin Film Art disclose each element of claim 1 as described below. Example references that satisfy claim 1 are provided with reference to the colors below.

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Claim 1 Element	Shin Disclosure
Preamble	“GaN light emitting diode”
substrate	“sapphire substrate 41” [blue]
n-type layer	“n-type GaN clad layer 43a” [yellow]
p-type layer	“p-type GaN clad layer 43c” [green]
first n-electrode	“n-electrode 46” [purple]
first p-electrode	“p-electrode 45” [red]
first insulating layer	“passivation layer 47” [pink]
second n-electrode	“second bonding electrode 48a” [orange]
second p-electrode	“second bonding electrode 48b” [grey]

9.3.1.1. Shin Discloses Claim 1’s Preamble

170. Shin states that “the present invention pertains, in general, to a light emitting diode (LED), which is a “semiconductor light-emitting element” (Ex-1005 at ¶¶ [0002]; [0004]; [0020]; [0074]; [0019]).

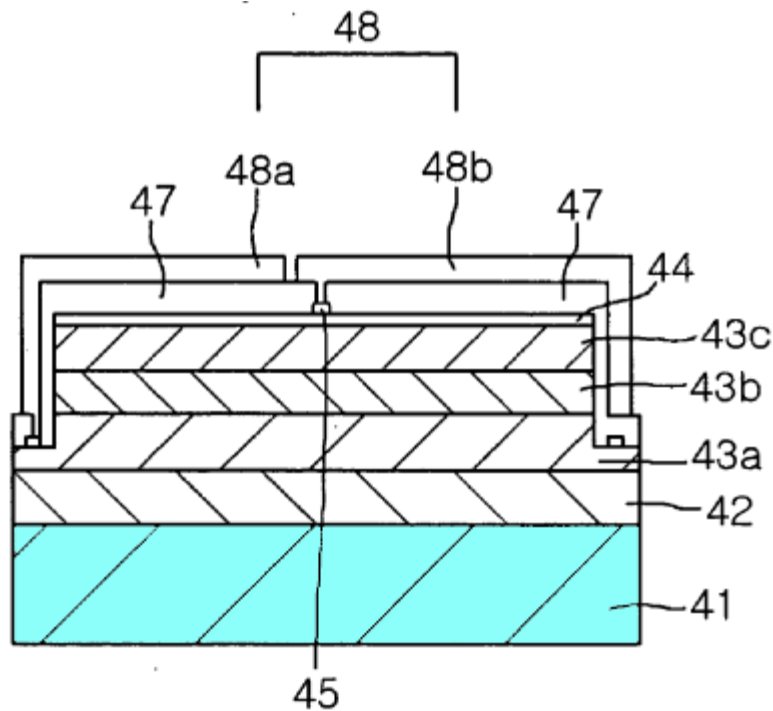
9.3.1.2. Shin Discloses the Substrate Limitation

171. Shin discloses “sapphire substrate 41” (blue, Ex-1005 at ¶¶ [0020] [0039]; 0040]; *see also* ¶¶ [0005], [0107], [0108]; FIGs. 3, 4A, 5), which satisfies

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claim 1's "substrate" limitation. Shin's sapphire substrate 41 is transparent and light transmitting as it is well-known that sapphire is considered transparent.

Shin Fig. 5 (Annotated)



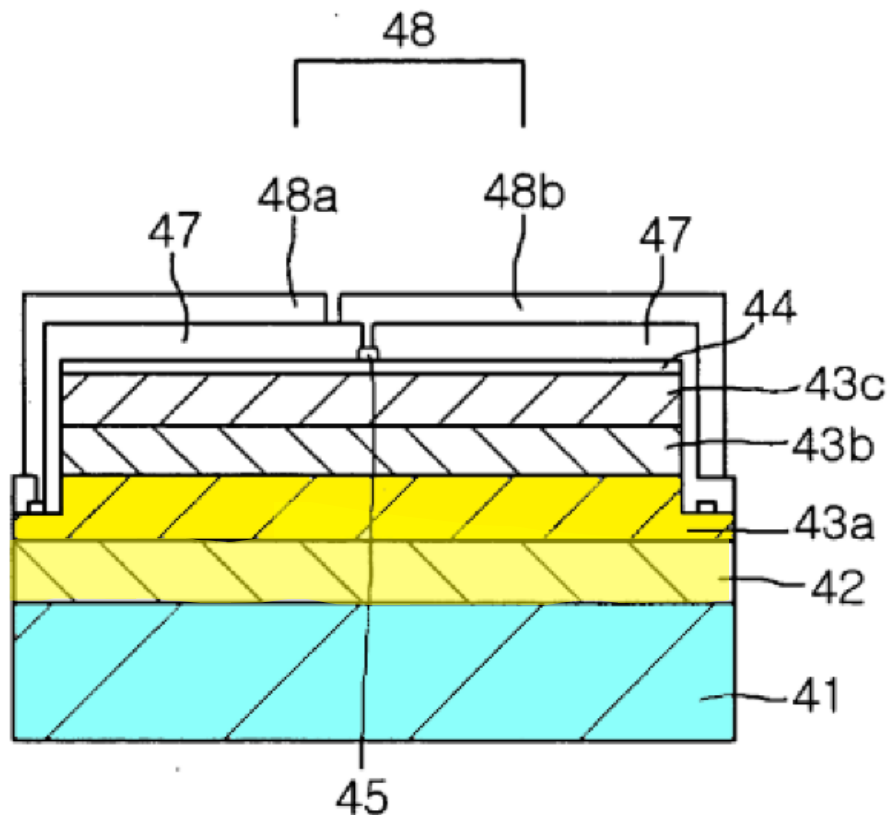
9.3.1.3. Shin Discloses the n-type Layer Limitation

172. Shin discloses an “n-type GaN clad layer 43a” and “buffer layer” 42 [yellow] which together are the claimed “an n-type semiconductor layer” (Ex-1005 at ¶ [0040]). As I describe above in the background section regarding epitaxial growth, an LED n-type or p-type semiconductor layer is often described as having sublayers including buffer or clad layers (*see supra* ¶ 123). For example, n or p layers may include a “buffer layer” in a standard LED epitaxial growth process to

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improve lattice matching between a layer and another material, such as the sapphire substrate, to reduce strain at the interface of different materials (*see supra* ¶ 123; Ex-1005 at ¶ [0040]). Shin’s “n-type GaN clad layer 43a” and “buffer layer” 42 [yellow] are “formed on” and cover the sapphire substrate 41” [blue] (FIG. 5 yellow) (Ex-1005 at ¶ [0040]).

Shin Fig. 5 (Annotated)



9.3.1.4. Shin Discloses the p-type Layer Limitation

173. Shin discloses “p-type GaN clad layer 43c,” [green] which is the claimed “p-type semiconductor layer” (Ex-1005 at ¶ [0040]). As shown in FIG. 5, Shin’s p-type semiconductor layer 43c [green] covers an area on the n-type GaN clad

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layer 43c, buffer layer 42 [yellow] (*e.g.*, the claimed “n-type semiconductor layer”). The top-down view of FIG. 5 shows that the n-electrodes 46a-b [purple] are visible and thus an area for an n-electrode (*i.e.*, n-electrodes 46a-b [purple]) on the n-type semiconductor layer (*i.e.*, n-type GaN clad layer/buffer layer 43a, 42 [yellow]) is excluded from the cover of the p-type semiconductor layer (*i.e.*, “a p-type GaN clad layer 43c [green]”).

Shin Fig. 5 (Annotated)

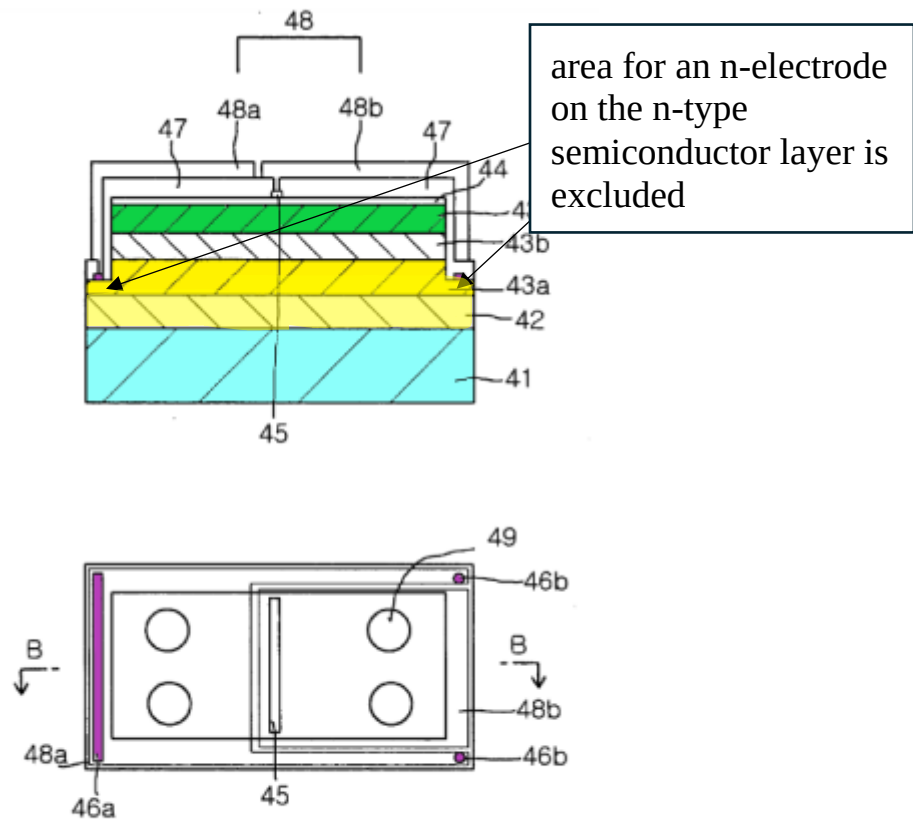


FIG. 5

9.3.1.5. Shin Plus One or More of the Thin Film Art Disclose the First n-Electrode Limitation

174. Shin discloses a first “n-electrode 46” [purple] “formed on the n-type GaN clad layer 43/buffer layer 42 [yellow] (Ex-1005 at ¶ [0044]; Fig. 4C). Shin’s n-electrode 46 is the claimed “first n-electrode.”

Shin Fig. 4C (Annotated)

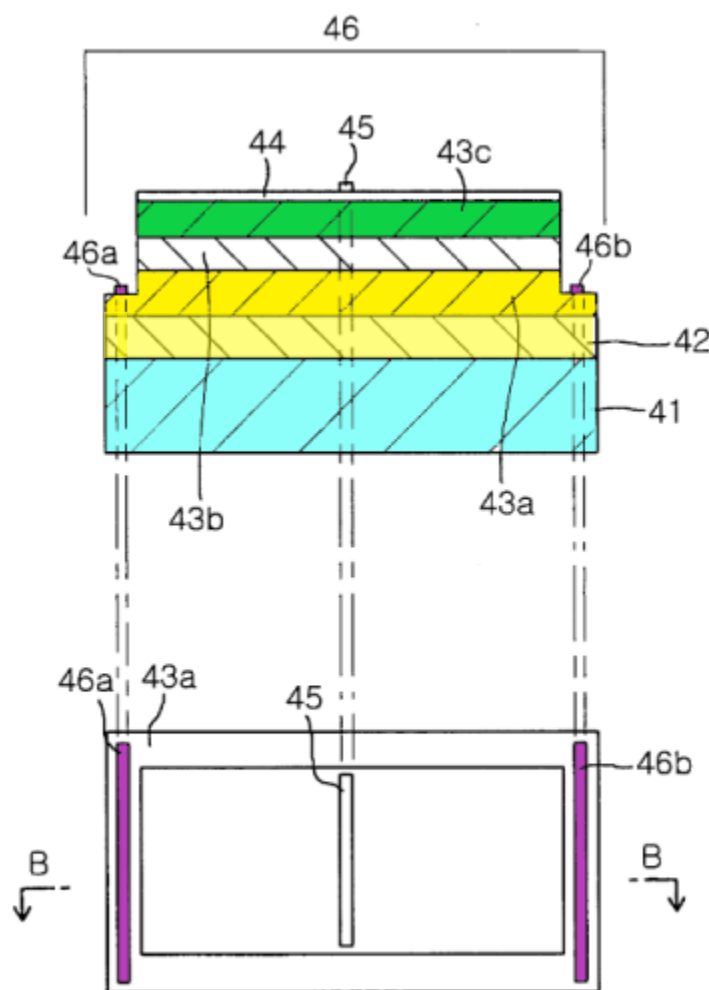


FIG. 4C

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175. A POSITA understands that Shin discloses thin film electrodes based on Shin’s disclosure. For example, Shin describes that the invention pertains to a gallium nitride LEDs diode for flip-chip bonding (Ex-1005 at ¶ [0002]). Because Shin’s disclosure is for GaN LEDS in 2003, this informs a POSITA that thin film electrodes are used in Shin (*see supra* § 8.2). For example, in describing a “conventional” LED, Shin refers to Inoue (“Inoue”). Inoue discloses thin film electrodes. Inoue describes the electrodes as “metal films” (Ex-1021 at 3:35-4:17). Inoue further describes that the n and p electrodes can be formed with a titanium film with a thickness of about 0.2 microns and a gold film having a thickness of about 0.5 microns are stacked by a lift-off method or an etching method resulting in a multilayer film (Ex-1021 at 13:13-20). Inoue also discloses that a thick film p-electrode can be used in that particular application instead of thin films (Ex-1021 at 14:52-57). Shin’s reference to Inoue’s conventional thin film electrodes informs a POSITA that Shin’s electrodes are thin film electrodes.

176. Further, Shin describes the state of GaN LED art as having electrodes that are “formed on” or “layered” on the LED semiconductor layers (Ex-1005 at ¶ [0015]). Shin also discloses that the electrodes in the disclosed Figures are “formed on” the semiconductor layers or other electrodes to specific shapes and widths (Ex-1005 at ¶¶ [0044], [0045], [0051]). For example, Shin describes that the “n-electrode 46” is formed as a “lane electrode” 46a having “as narrow width as possible” with

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example widths of 10 to 20 micrometers (Ex-1005 at ¶¶ [0026], [0045]-[0046]). This description informs a POSITA that the electrodes are thin film electrodes because the language informs a POSITA that conventional sputtering, plating, or other processes are used to “form” the electrodes by depositing metal and forming thin films.

177. Also, Shin discloses that the LED is attached to a circuit board with gold bumps (Ex-1005 at ¶ [0061]). A POSITA understands the gold bumps are on the order of 10 microns thick. A POSITA knows that Shin’s gold bumps would be used with thin film electrodes based on the thickness of gold bumps.

178. Nevertheless, Shin does not use the words “thin film.” As described (*see supra* § 8.2) each of the Thin Film Art discloses thin film electrodes. It would have been obvious to a POSITA to use a thin film electrode as disclosed in one or more of the Thin Film Art as the electrodes in Shin. There are no differences between the claim and the art because Shin discloses the limitations of claim 1 and each of the Thin Film Art discloses thin film electrodes. Using thin film electrodes was well within the level of ordinary skill in the art as described (*see supra* § 8.2). In fact, Shin describes a GaN LED and the state of the art included using thin film electrodes with reference to Inoue (*see supra* §8.2). Using thin film electrodes as taught in each of the Thin Film Art was well-understood, common knowledge, predictable, and routine in 2003 (*see supra* §8.2). Song for example recognized the

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wide-spread use of thin film electrodes. Song states describes how in 2004 “thin film electrodes based on nickel (Ni), e.g., a thin metal film of nickel/gold (Ni/Au), have been widely used as thin film electrode structures for ohmic contact” (Ex-1017 at 1:32-34). Song states that these LED thin film electrodes have “very thin thickness ($<\sim 100 \text{ \AA}$) and a transmittance of 80% or more Using a thin film electrode as disclosed in each of the Thin Film Art in Shin yields an operational LED and predictable results because Shin is directed to GaN LEDs where thin film electrodes were common (Ex-1017 at 1:61-63). Further, the sputtering and other processes for manufacturing thin films were known and within the level of ordinary skill in the art (*see supra* § 8.4).

179. A POSITA would have been motivated to use thin film electrodes from one or more of the Thin Film Art in Shin to enhance light extraction from an LED package. A primary goal of an LED package is to maximize the amount of light emitted by an LED from the LED package. Metal electrodes can be used to provide the electrical path for electricity to reach the LED because metals are excellent electrical conductors as well as thermal conductors to dissipate heat. However, metals also reflect light and can absorb light. If light is reflected back into the LED package or absorbed, this can decrease light extraction. Thin film electrodes were developed as a way to provide the benefits of a metal electrode but minimize the impact on light extraction. Generally, thin film electrodes are formed by depositing

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very small amounts of metal and building a layer of a desired thickness. The thickness is application dependent based on the size of the LED and the intended LED purpose. A POSITA would have been motivated to use the thin film electrodes in one or more of the Thin Film Art in Shin to maximize light extraction as is known in the art. Further, a POSITA knew that thin film electrodes had wide-spread acceptance particularly in gallium-nitride LEDs.

180. A POSITA would have been further motivated to use thin film electrodes in one or more of the Thin Film Art in Shin because a POSITA knew that thin film electrodes provided good reliability, good adhesion/bonding, and good conductance, so that the applied LED voltage can be minimized to prevent LED degradation (Ex-1006 at ¶¶ [0014], [0016]], [0021]-[0034]) (*see supra* § 8.2). Also, a POSITA would have been motivated to use any of the thin film electrodes in the Thin Film art by combining one or more of the Thin Film Art with Shin because Shin references thin film electrodes in Inoue as conventional. Moreover, the thin film electrodes in the Thin Film art fits with Shin's disclosure of forming "lane" electrodes, with widths as narrow width as possible" and with example widths of 10 to 20 micrometers (Ex-1005 at ¶¶ [0026], [0045]-[0046]). Film electrodes were predictable. Use of one or more of the electrodes described in the Thin Film Art in Shin would result in an operable invention.

9.3.1.6. Shin Plus One or More of the Thin Film Art Disclose the First P-Electrode Limitation

181. Shin discloses “a first p-electrode that is a thin film formed on the p-type semiconductor layer.” For example, Shin discloses a nitride semiconductor device having a first “p-electrode” 45 (red, Fig. 3 below) (Ex-1005 at ¶¶ [0044]). While the below annotated version of Shin FIG. 4C shows a transparent electrode 44 between the p-type GaN clad layer 43 c [green] and the p electrode 45 [red], Shin describes that the transparent electrode 44 “may be omitted” (Ex-1005 at ¶ [0043]) Thus, Shin discloses that p electrode 45 [red] is “formed on” p-type GaN clad layer 43c [green].

Shin Fig. 4C (Annotated)

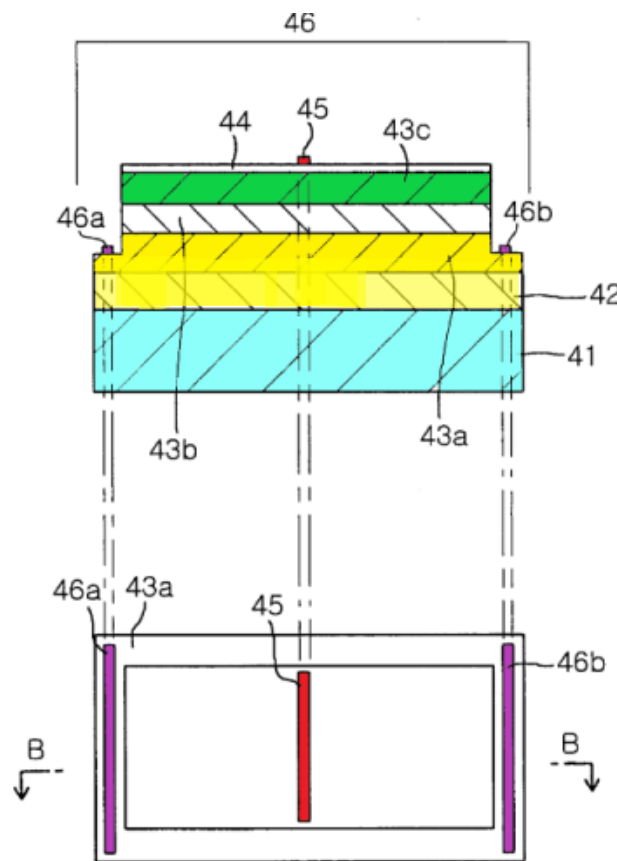


FIG. 4C

182. A POSITA understands that Shin discloses thin film electrodes based on Shin's disclosure. Shin's p-electrode is described as having as "narrow width as possible" and for example having a width of 10-20 micrometers (Ex-1005 at ¶¶ [0026], [0046]. For the reasons described above with reference to the first n-electrode, Shin plus one or more of the Thin Film Art discloses a thin film as the first

p-electrode and a POSITA would have been motivated to use a thin film as disclosed in one more of the Thin Film Art for the first p-electrode in Shin (*see supra* § 9.3.1.5).

9.3.1.7. Shin Discloses the First Insulating Layer Limitation

183. Shin discloses “a transparent, nonconductive passivation layer 47” [pink] that is the claimed “first insulation layer” (Ex-1005 at ¶ [0046]). Shin describes that passivation layer electrically insulates electrodes (Ex-1005 at ¶ [0020]). As shown in Fig. 4C, Shin’s “passivation layer 47” electrically insulates the first n-electrode [purple] and the first p-electrode [red] from each other (*see* Ex-1005 at ¶ [0046]). Shin further describes that after the first n and p electrodes are formed, the “nonconductive passivation layer is formed on the resulting structure” (*e.g.*, on both first n and p electrodes), thereby insulating the first n and p electrodes from each other (Ex-1005 at ¶ [0047], *see also* ¶ [0020]). Portions of the passivation layer are punched to expose portions of the first n and p electrodes as shown in FIG. 4D (purple first n-electrodes, and red first p-electrode) (Ex-1005 at ¶ [0047]).

Shin Fig. 4D (Annotated)

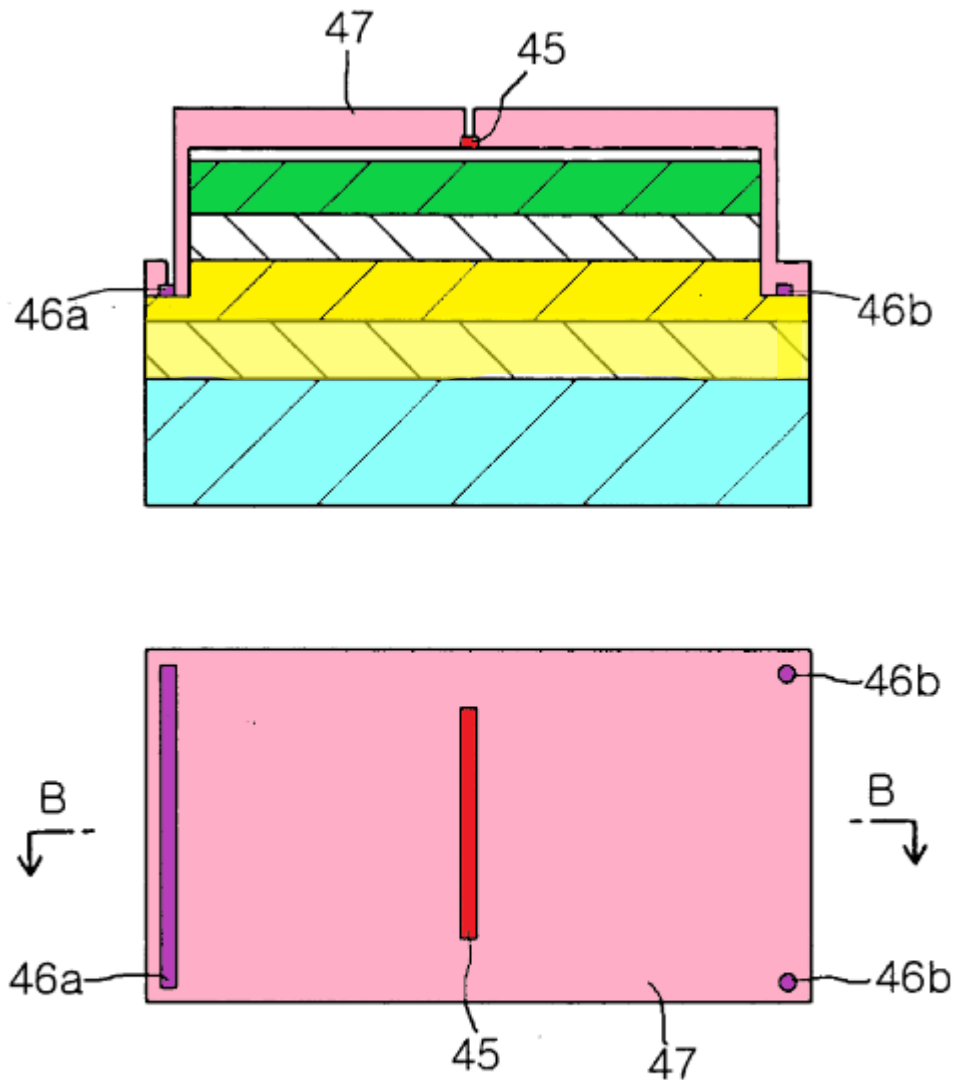


FIG. 4D

9.3.1.8. Shin Plus One or More of the Thin Film Art Discloses the Second N-Electrode Limitation

184. Shin discloses “a second n-electrode” (*i.e.*, second bonding electrode 48a [orange]) formed on the first n-electrode (*i.e.*, n-electrode 46 [purple]) and the first insulating layer as a thin film (*i.e.*, passivation layer 47 [pink]) having an area larger than a joined face between the n-type semiconductor layer (*i.e.*, n-type GaN clad layer 43a/buffer layer 42 [yellow]) and the first n-electrode (*i.e.*, “n-electrode 46” [purple]) so that the second n-electrode (*i.e.*, second bonding electrode 48a [orange]) is electrically connected to the first n-electrode (*i.e.*, “n-electrode 46” [purple]), the second n-electrode (*i.e.*, “n-electrode 48” [orange]) being insulated from the first p-electrode p (*i.e.*, electrode 45 [red]) by the first insulating layer (*i.e.*, passivation layer 47 [pink]).

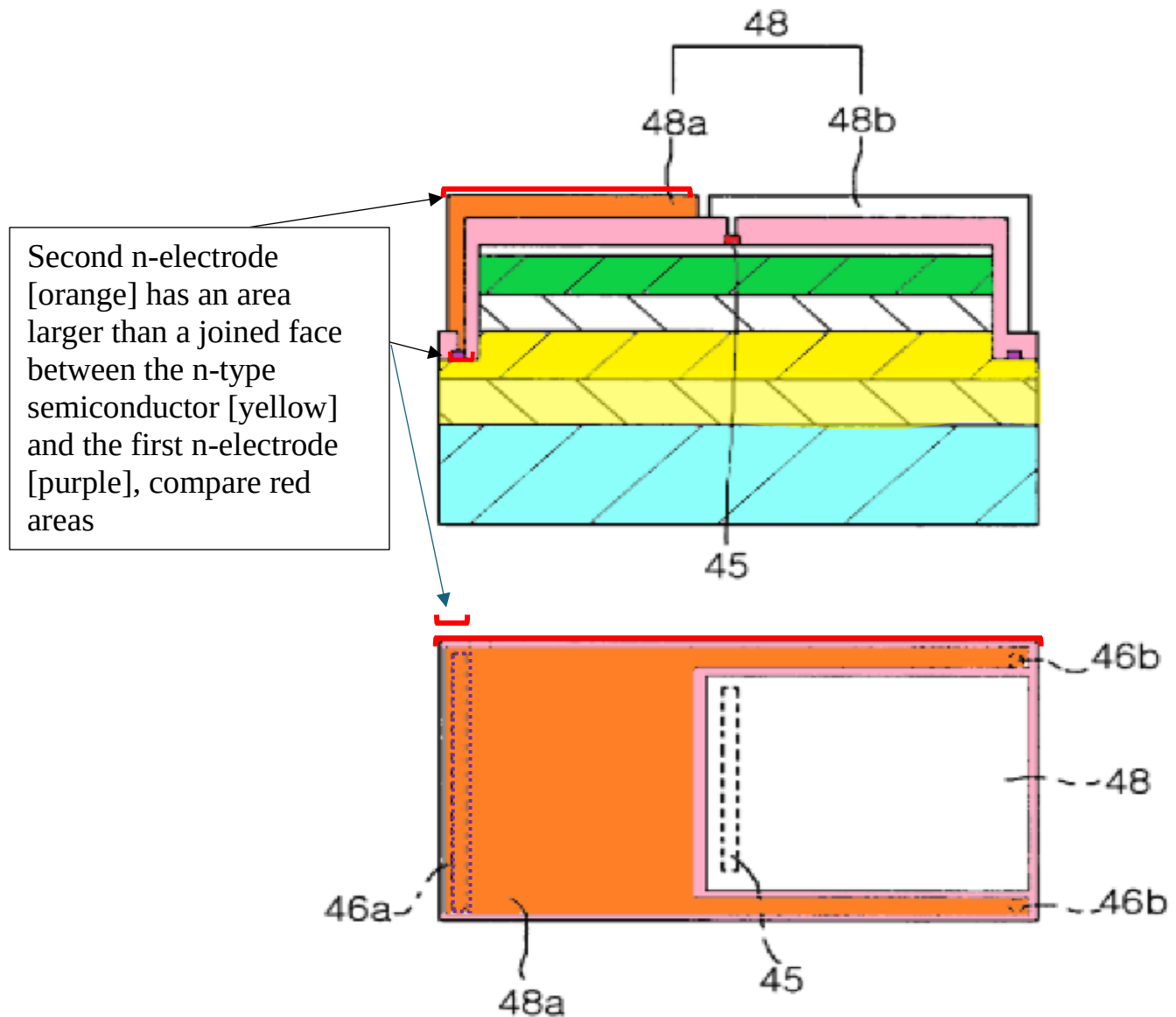
185. For example, Shin discloses a “second bonding electrode 48a” [orange] “formed on the passivation layer” [pink] as a thin film to “come into contact with the n-electrode 46” [purple] (FIG. 5 below) (Ex-1005 at [0051]). Second bonding electrode 48a is formed as a thin film given that it is described as being shaped with a lane, with a width of 10-20 micrometers, and “formed in a shape of ‘[’” on passivation layer 47 (Ex-1005 at ¶¶ [0020], [0026], [0051]). Shin’s second n-electrode covers a significant portion of the passivation insulation layer (Ex-1005 at ¶¶ [0045], [0051]). Thus, Shin’s second n-electrode (orange) has an area that is

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larger than the “joined face between the n-type semiconductor material” (yellow) and the first n-electrode (purple) because the second n-electrode covers a significant area of the passivation or insulation layer.

186. Shin further describes that the first n-electrode 46 has a “minimized area” and the second n-electrode has “sufficient bonding area” (Ex-1005 at ¶¶ [0052], [0055]). A POSITA understands that Shin discloses thin film electrodes based on Shin’s disclosure. For the reasons described above with reference to the first n-electrode, Shin plus one or more of the Thin Film Art discloses the second n-electrode limitation and a POSITA would have been motivated to use a thin film as disclosed in one more of the Thin Film Art for the second n-electrode in Shin (*see supra* § 9.3.1.5).

Shin Fig. 4E (Annotated)



9.3.1.9. Shin and the Thin Film Art Disclose the Second P-Electrode Limitation

187. Shin discloses “a second p-electrode” (*i.e.*, second bonding electrode 48b [grey]) “formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer” (*i.e.*, n-type GaN clad layer 43a/buffer layer [yellow]) “and the p-type semiconductor layer” (*i.e.*, p-type GaN clad layer 43c [green]), “the second p-electrode” (*i.e.*, second bonding electrode 48b [grey]) “being electrically connected to the first p-electrode” (*i.e.*, p electrode 45 [red]).

188. Shin discloses a second bonding electrode 48b [gray] which is the claimed “second p-electrode” that covers the first p-lane electrode (Ex-1005 at ¶ [0050]; FIGS. 4C& 4D above). Shin also discloses that the second p-electrode 48a is “formed on the passivation layer” [pink] as a thin film to “cover a portion of the passivation layer 47 corresponding in position to the p-electrode 45” (FIG. 5 below) (Ex-1005 at ¶ [0051]). Shin’s second p-electrode covers a significant portion of the passivation insulation layer (Ex-1005 at ¶¶ [0045], [0051]). Thus, Shin’s second p-electrode 48a has an area smaller than joined face between the n-type semiconductor layer (*i.e.*, n-type GaN clad layer 43a/buffer layer 42 [yellow]) and the p-type semiconductor layer (*i.e.*, p-type GaN clad layer 43c [green]).

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189. A POSITA understands that Shin discloses thin film electrodes based on Shin's disclosure. For example, second bonding electrode 48b is formed as a thin film given that it is described as being shaped as a "lane" with a width of 10-20 micrometers (Ex-1005 at ¶¶ [0020], [0026], [0051]). For the reasons described above with reference to the first n-electrode, Shin plus one or more of the Thin Film Art discloses the second p-electrode limitation and a POSITA would have been motivated to use a thin film as disclosed in one more of the Thin Film Art for the second p-electrode in Shin (*see supra* ¶ 9.3.1.5).

Shin Fig. 4E Annotated

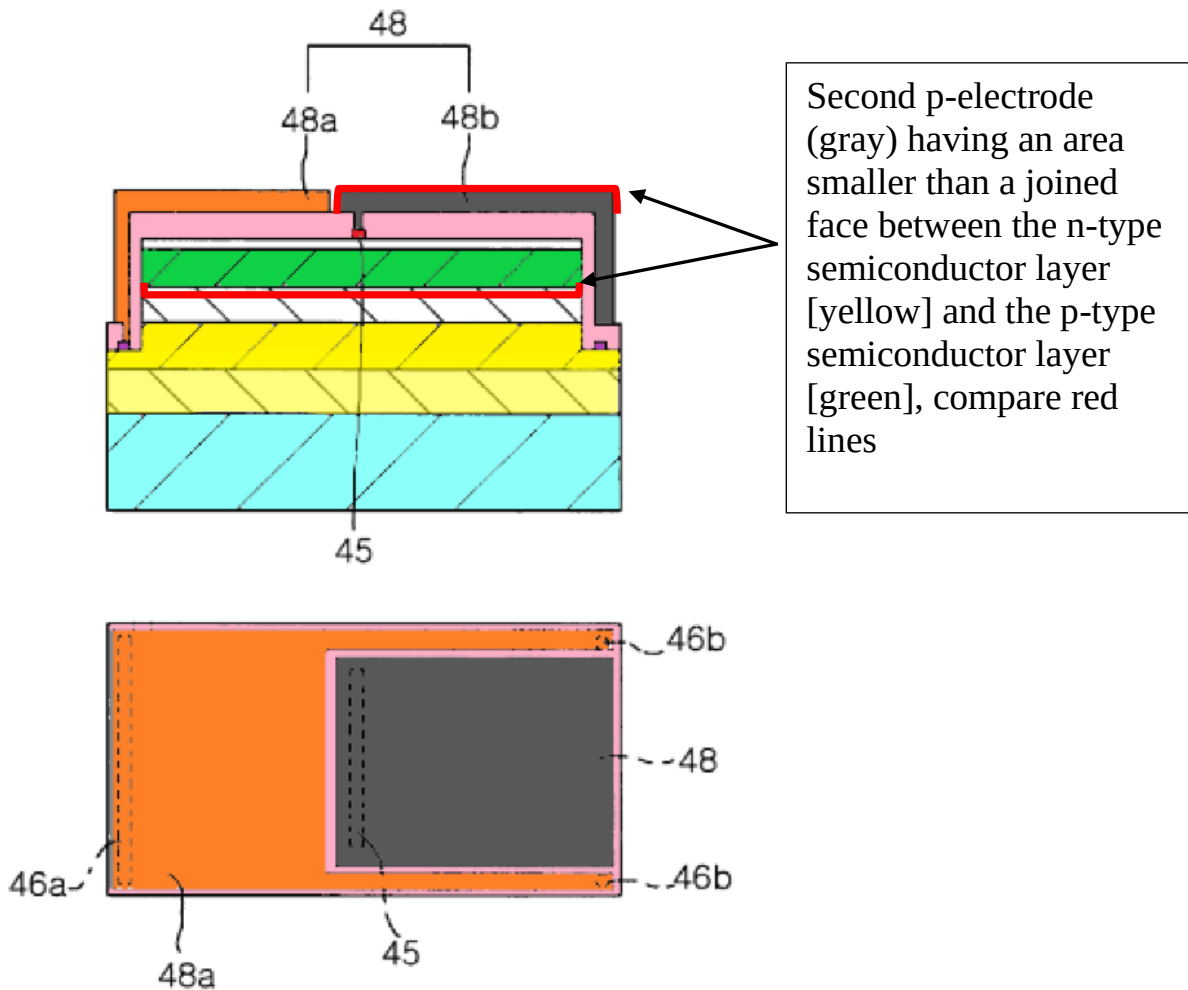


FIG. 4E

9.3.1.10. Obviousness Conclusion

190. Thin film electrodes were well within the level of ordinary skill in the art (*see supra* § 8.2). There are no known second factors of nonobviousness. Thus, claim 1 is obvious over Shin in view of one or more of the Thin Film Art.

9.3.2. Claim 2 is Obvious over Shin Plus One or more of the Thin Film Art

191. Claim 2 is independent. Claim 2's preamble and first five elements are the same as claim 1. Therefore, Shin alone or in combination with one or more of the Thin Film Art discloses claim 2's preamble and the first five elements as described above with reference to claim 1.

192. Claim 2 is obvious over Shin (Ex-1005) and one or more of Terashima, Sugimoto, Uemura '259, Uemura '999, and/or Inoue (Collectively the "Thin Film Art"). Shin described all of the limitations of claim 2 with the possible exception of the claimed electrodes being "thin films." While Shin discloses thin film electrodes to a POSITA, Shin does not use the precise words "thin film." Therefore, the Thin Film Art is cited as prior art disclosing thin film electrodes. It would have been obvious to a POSITA to combine Shin with one or more of Terashima, Sugimoto, Uemura '259, Uemura '999, and/or Inoue at the time of the alleged invention to form the alleged invention of claim 2.

**9.3.2.1. Shin Plus One or More of the Thin Film Art
Render Claim 2 Obvious**

193. Shin plus one or more of the Thin Film Art discloses each element of claim 2 as described below. Below I compared the scope and content of the prior art and any differences between the prior art and claim 2. I found no differences. I am not aware of any secondary factors of nonobviousness. I considered the level of

ordinary skill in the art particularly that thin film electrodes were well-known and in common use. Based on my analysis and these considerations, it is my opinion that claim 2 is obvious over Shin in view of one or more of the Thin Film Art.

9.3.2.2. Shin discloses Claim 2's First Insulating Layer

194. Shin discloses “a first insulating layer” (*i.e.*, passivation layer 47 [pink]) having at least one opening for the n-electrode (*i.e.*, “n-electrode 46” [purple]) and one opening for the p-electrode (*i.e.*, p electrode 45 [red]) formed therein, which covers the first n-electrode (*i.e.*, “n-electrode 46” [purple]) and the first p-electrode (*i.e.*, p electrode 45 [red]) so as to insulate the first n-electrode (*i.e.*, “n-electrode 46” [purple]) and the first p-electrode (*i.e.*, p electrode 45 [red]) from each other, except for the opening for the n-electrode and the opening for the p-electrode. Shin’s “passivation layer 47” or “first insulating layer” has an opening for the n-electrode 46 and an opening for the p-electrode 45 (*see* Ex-1005 at ¶ [0046]). For example, Shin describes that the “portion of the passivation layer 47 [pink] corresponding in position to one electrode 46 a [purple] of the two n-electrodes is punched (a shape of the portion of the passivation layer which is punched is a lane with a predetermined length and width, like the shape of the electrode 46a), and other portions of the passivation layer 47 corresponding in position to the other electrode 46b [purple] are punched in a shape of two holes at portions of the passivation layer 47 corresponding in position to both ends of the lane-shaped electrode 46b” (Ex-

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1005 at ¶ [0048]). Likewise, the “portion of the passivation layer 47 [pink] corresponding in position to the p-electrode 45 [red] is punched in the same shape as the p-electrode 45 (*i.e.* lane with the same width and length as the p-electrode)” (*id.*). The “punched” portions of the passivation layer 47 are the claimed “openings.” Shin’s passivation layer 47 also covers the first n-electrode and the first p-electrode to as to insulate them from each other except for the openings as shown in Fig. 4C.

Shin Fig. 4C (Annotated)

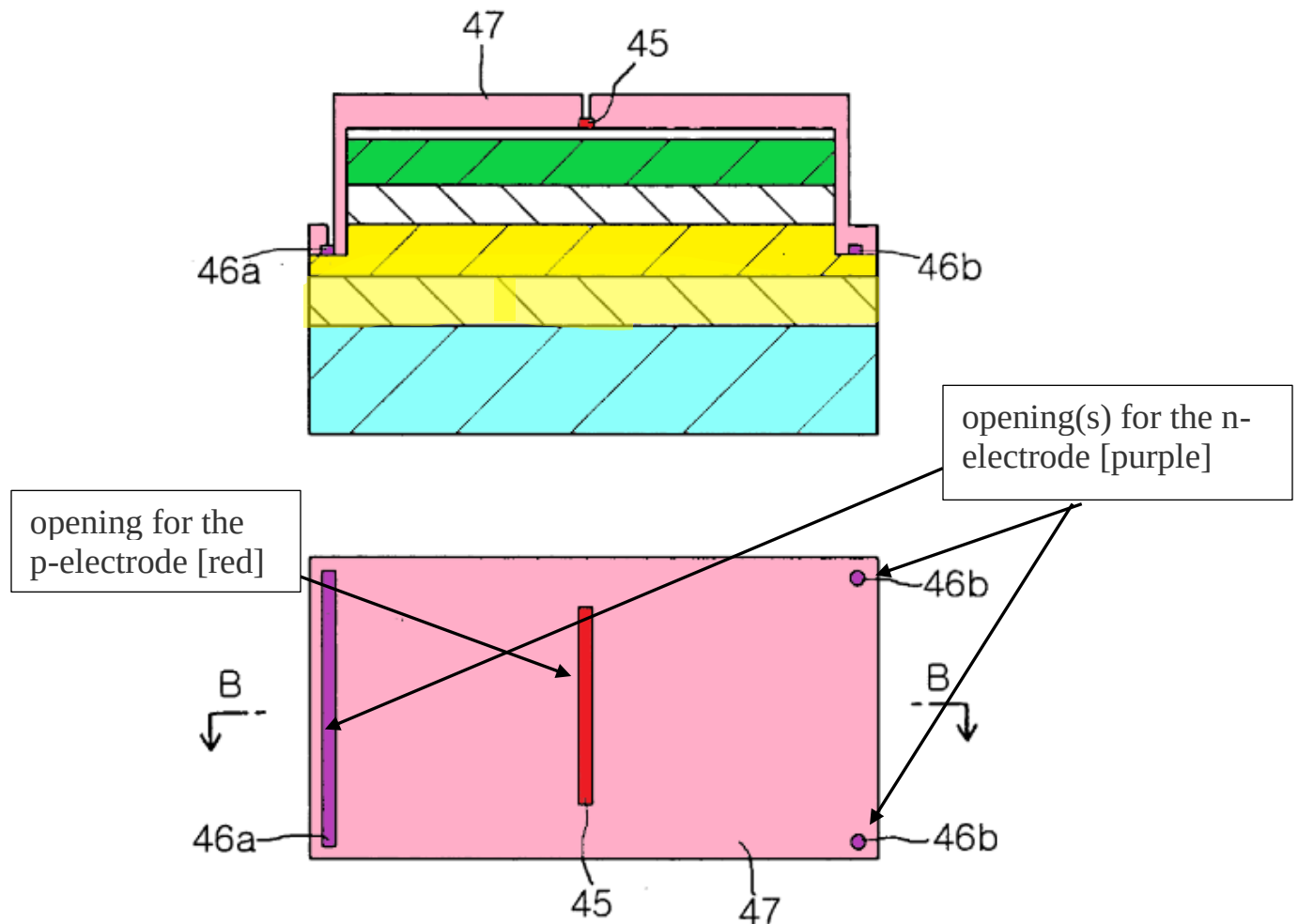


FIG. 4D

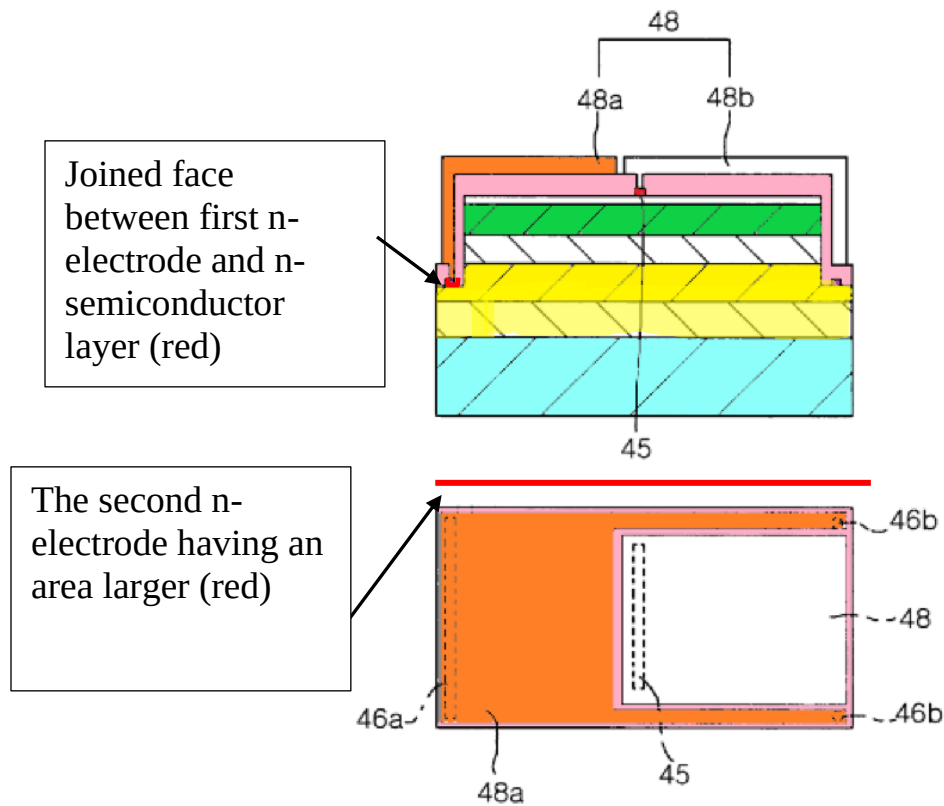
9.3.2.3. Shin and the Thin Film Art Disclose Claim 2's Second N-Electrode

195. Shin discloses “a second n-electrode” (*i.e.*, second bonding electrode 48a [orange]) formed on the first insulating layer (*i.e.*, passivation layer 47 [pink]) as a thin film having an area larger than a joined face between the n-type

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semiconductor layer (*i.e.*, n-type GaN clad layer 43a/buffer layer 42 [yellow]) and the first n-electrode (*i.e.*, n-electrode 46 [purple]), the second n-electrode (*i.e.*, second bonding electrode 48a [orange]) being electrically connected to the first n-electrode (*i.e.*, n-electrode 46 [purple]) through the opening for the n-electrode of the first insulating layer (*i.e.*, passivation layer 47 [pink]). Shin FIG. 4E discloses the second n-electrode 48a [orange] that has an area that is larger than the joined face between the n-type layer 43a/buffer layer 42 [yellow] and the first n-electrode 46a [purple] (Ex-1005 at ¶¶ [0087]-[0088]). Shin also describes that the second n-electrode 48a [orange] is “formed on the passivation layer 47 [pink] as a way to come into contact with the n-electrode 46 [purple]” (Ex-1005 at ¶ [0050]). Shin in view of one or more of the Thin Film Art discloses that that the second n-electrode is formed as a thin film (*see supra* § 9.3.1.5). For the reasons described above with reference to the first n-electrode in claim 1, Shin plus one or more of the Thin Film Art discloses a thin film as the second n-electrode and a POSITA would have been motivated to use a thin film as disclosed in one or more of the Thin Film Art for the second n-electrode in Shin (*see supra* § 9.3.1.5).

Shin Fig. 4E (Annotated)



9.3.2.4. Shin and the Thin Film Art Disclose Claim 2's Second P-Electrode

196. Shin discloses “a second p-electrode” (*i.e.*, p-electrode 48b [gray]) formed on the first insulating layer (*i.e.*, passivation layer 47 [pink]) as a thin film having an area smaller than a joined face between the n-type semiconductor layer (*i.e.*, n-type GaN clad layer 43a/buffer layer 42 [yellow]) and the p-type semiconductor layer (*i.e.*, p-type GaN clad layer 43c [green]), the second p-electrode being electrically connected to the first p-electrode through the opening

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for the p-electrode of the first insulating layer. Shin FIG. 4E discloses that the second p-electrode 48b is formed on the insulating layer 47 and has an area smaller than the joined face between the n-type semiconductor layer 43a/buffer layer 42 and the p-type semiconductor layer 43c. Shin also discloses that the second p-electrode 48b [gray] is “formed on the passivation layer 47 [pink] as a way to come into contact with” the first p-electrode 45 [red], as shown in Figure 4E (Ex-1005 at ¶ [0050]). Shin in view of one or more of the Thin Film Art discloses that that the second p-electrode is formed as a thin film (*see supra* § 9.3.1.5). For the reasons described above with reference to the first n-electrode in claim 1, Shin plus one or more of the Thin Film Art discloses a thin film as the second n-electrode and a POSITA would have been motivated to use a thin film as disclosed in one or more of the Thin Film Art as the second p-electrode in Shin (*see supra* § 9.3.1.5).

Shin Fig. 4E (Annotated)

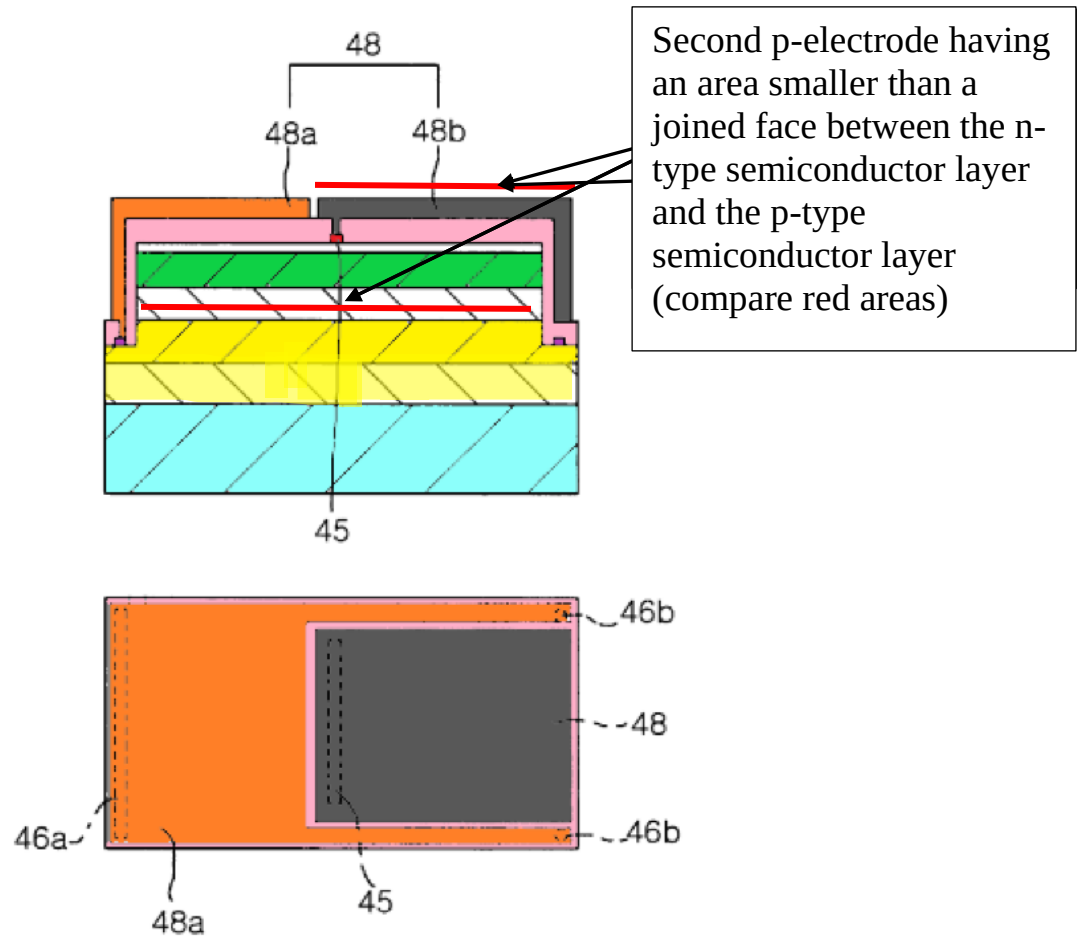


FIG. 4E

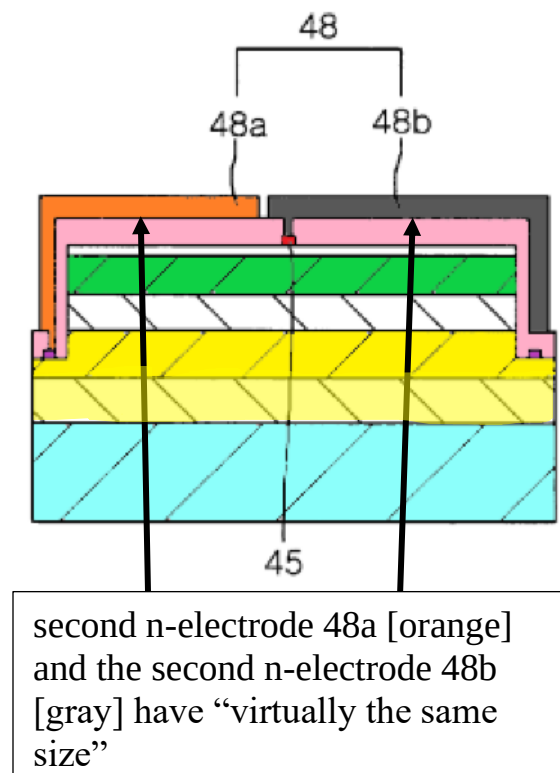
9.3.2.5. Obviousness Conclusion

197. There are no differences between claim 2 and Shin and the Thin Film Art. For the reasons provided above with respect to Shin and claims 1 and 2, claim 2 is obvious over Shin in view of one or more of the Thin Film Art.

9.3.3. Claim 5 is Obvious over Shin Plus One or More of the Thin Film Art

198. Claim 5 recites that “semiconductor light-emitting element according to claim 1, wherein the second n-electrode (orange) and the second p-electrode (gray) have virtually same size.” Shin states that both second electrodes are 10-20 micrometers in width and are “lane” electrodes with virtually the same size as shown in FIG. 4E (Ex-1005 at ¶¶ [0020], [0021], [0026]). Thus, Shin discloses the limitation added in claim 5 and claim 5 is obvious as described above with reference to claim 1.

Shin Fig. 4E (Annotated)



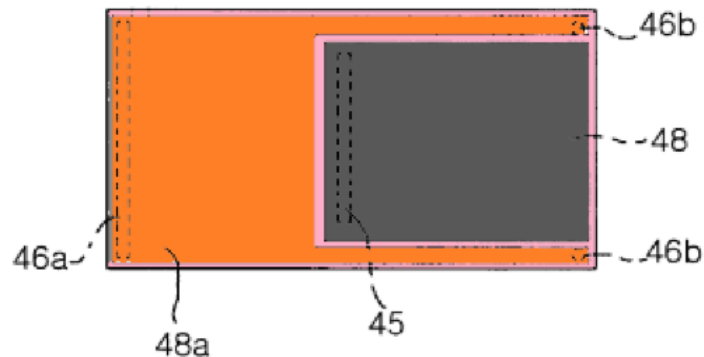


FIG. 4E

9.3.4. Claim 7 is Obvious over Shin Plus One or More of the Thin Film Art

199. Claim 7 recites a “light-emitting device comprising: the semiconductor light-emitting element according to claim 1; a circuit board having a plurality of electrodes; and a conductive bonding material layer that electrically connects and fixes the second n-electrode and the second p-electrode to the electrodes on the circuit board.”

200. Shin’s “Si substrate 61” [brown] is the claimed circuit board (Ex-1005 at ¶ [0049]. Shin’s circuit board has “signal patterns 62” or electrodes to attach to an LED. Shin’s “Au bumps 63” [indigo] are the claimed “conductive bonding material layer” (Ex-1005 at ¶¶ [0013], [0061]-[0063]). Shin discloses that “light emitting diode 40 bonded to the Si substrate according [brown] to a flip-chip bonding technology (Ex-1005 at ¶ [0061]). As shown in FIG. 6, Au bumps 63 [indigo] are formed on the Si substrate 61 [brown] on which signal patterns 62 are formed, and

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after Au is deposited on the first and second bonding electrode 48a [orange], 48b [gray] of the light emitting diode 40, Au portions of the first and second bonding electrode 48a, 48b are bonded to the Au portions of the Si substrate 61” (Ex-1005 at ¶ [0061]). Thus, Shin discloses the limitation added in claim 5 and claim 5 is obvious as described above with reference to claim 1.

Shin Fig. 6 (Annotated)

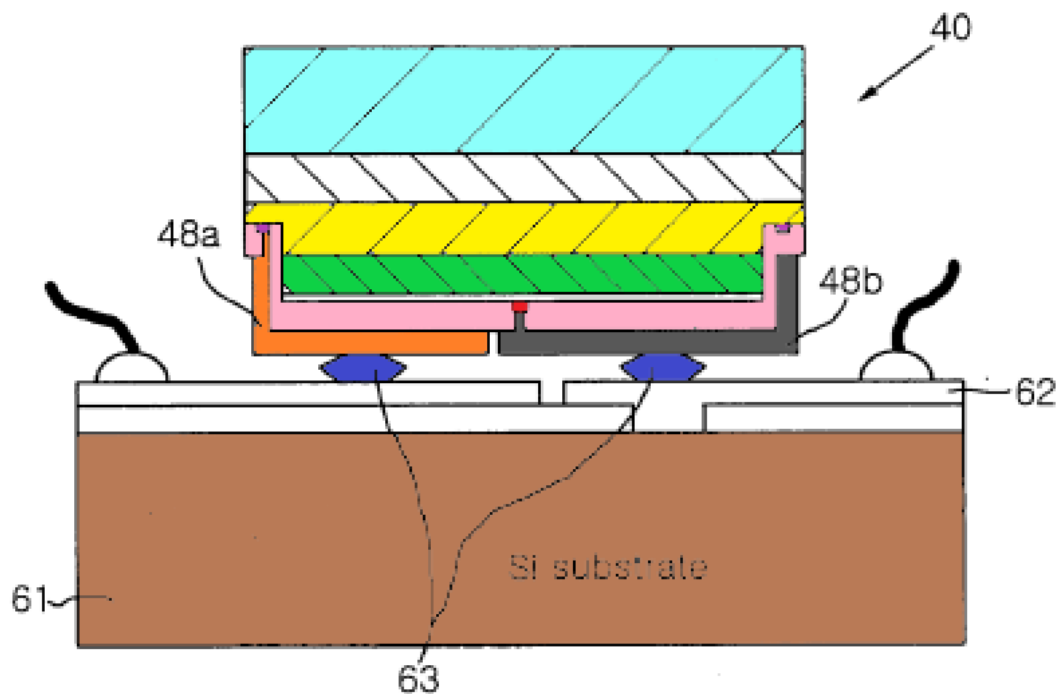


FIG. 6

9.3.5. Claim 9 is Obvious over Shin Plus One or More of the Thin Film Art

201. Claim 9 is a method of manufacturing claim that corresponds to claim

1. Claim 9 is obvious over Shin and one or more of the Thin Film Art for the reasons explained above with reference to claim 1.

9.3.6. Claim 10 is Obvious over Shin Plus One or More of the Thin Film Art

202. Claim 10 is a method of manufacturing claim that corresponds to claim

2. Claim 10 is obvious over Shin and one or more of the Thin Film Art for the reasons explained above with reference to claim 2.

9.4. Claim 4 is Obvious over Terashima or Shin and the Thin Film Art in view of Shelton or Inoue

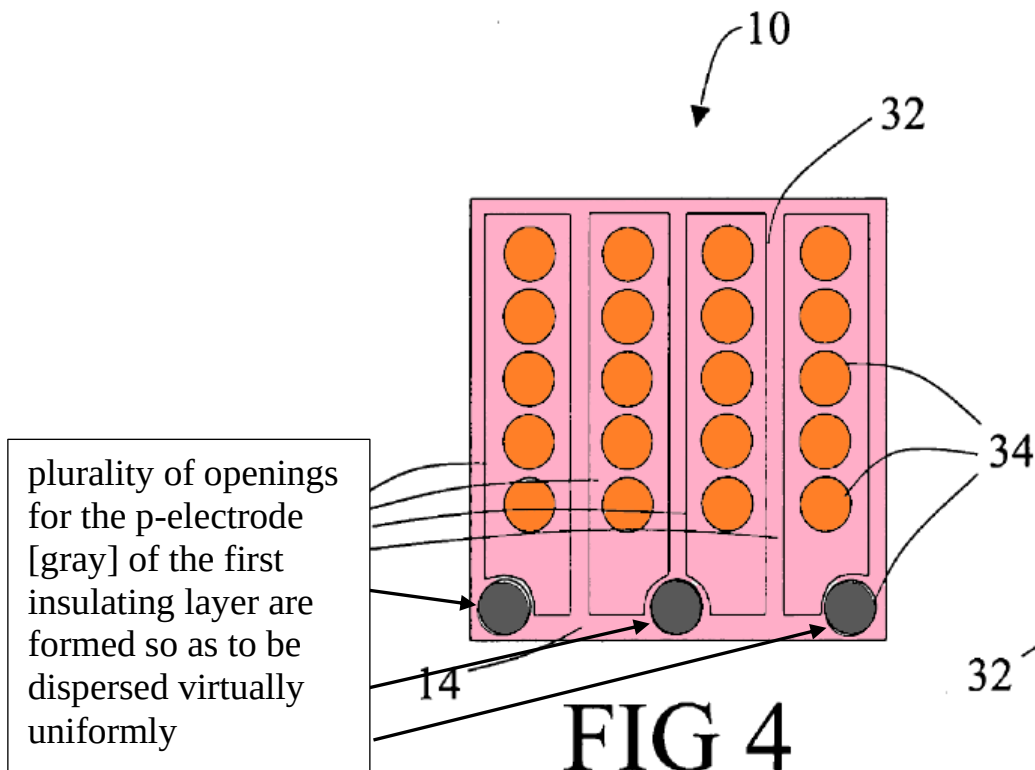
203. Claim 4 recites: “The semiconductor light-emitting element according to claim 2, wherein a plurality of openings for the p-electrode of the first insulating layer are formed so as to be dispersed virtually uniformly.” It would have been obvious to a POSITA to modify (i) Terashima or (ii) Shin and one or more of the Thin Film Art in view of Shelton to form the alleged invention of claim 4.

204. Shelton discloses “a plurality of openings for the p-electrode of the first insulating layer are formed so as to be dispersed virtually uniformly.” As shown below, Shelton’s n-electrode 12 [orange] and p-electrode 14 [gray] are sealed by a dielectric layer 32 [pink], which is an insulating layer (Ex-1011 at [0038]). The

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dielectric layer 32 includes several vias 34 or “openings.” For example, Shelton describes that the “vias 34 provide access to the p-type and n-type electrodes 12 [gray], 14 [orange]. Shelton discloses several vias 34 contacting each of the electrodes 12 [gray], 14 [orange] that are distributed virtually uniformly across the “lateral area of the light emitting diode 10 to promote current spreading across the light emitting diode 10” (Ex-1011 at ¶ [0039]).

Shelton, Figure 4 (annotated)



205. Terashima does not expressly describe how openings for the p-electrode are disposed. It would have been obvious to modify Terashima to have a plurality of openings for the p-electrode in the first insulating layer that are disposed

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uniformly in view of Shelton to promote uniform current spreading in the p-semiconductor layer or Inoue to provide sufficient brightness. Providing uniform current spreading can prevent deteriorating the LED and maximize light extraction. How to create uniform openings and the results were known and predictable (*see supra* § 8.5).

206. Shin describes a p-electrode positioned at the “center of the light emitting structure” (Ex-1004 at ¶ [0021]). Shin describes this positioning to be advantageous because “current uniformly flows” through the LED, thereby preventing the LED life span from being shortened due to concentration of current at a predetermined position (Ex-1004 at ¶ [0021]). Thus, Shin recognizes the importance of uniform current flow. Shelton likewise provides for uniform current flow by providing uniformly spaced openings for a plurality of p-electrodes. A POSITA knew that uniform spacing helps achieve sufficient brightness (Ex-1025 at 18:50-53). A POSITA would have been motivated to modify Shin to have multiple p-electrode openings because the p-semiconductor layer only covers part of the n-semiconductor layer and therefore multiple openings as described by Shelton or Inoue to provide even more uniform current flow and prevent life-shortening because the multiple opening can be more uniformly dispersed than an LED in the center of the device, which is not in the center of the p-semiconductor layer as in Shin. The results are predictable and an operable device results by combining

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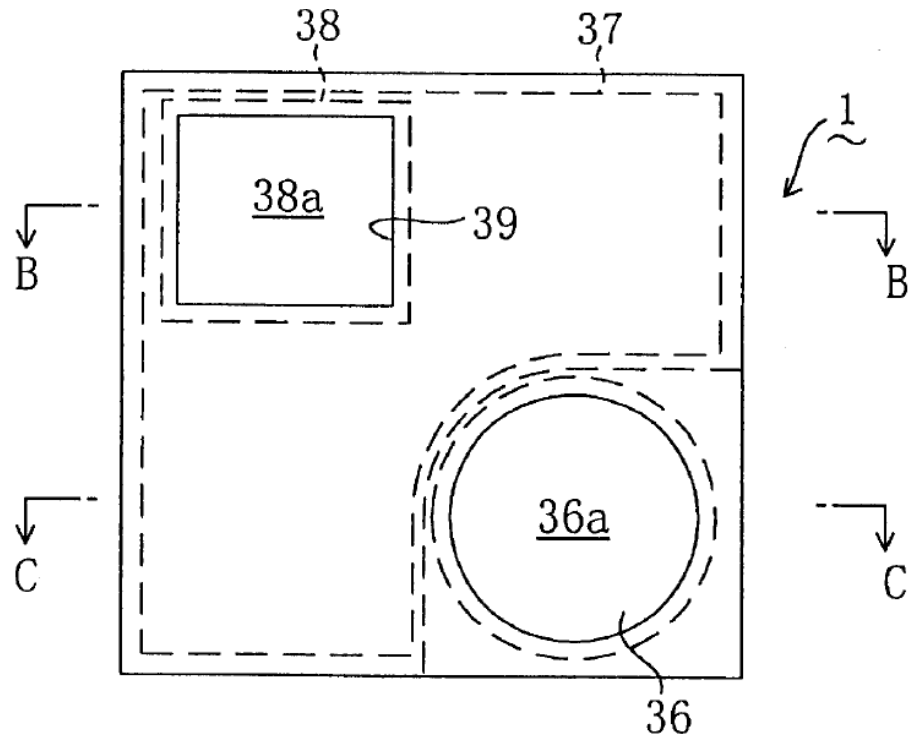
Shelton's virtually uniform spacing with Terashima or Shin plus one or more of the Thin Film Art. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 4 is obvious over Terashima or Shin as applied to claim 2 and Shelton and/or the level of ordinary skill in the art.

9.5. Claim 5 is Obvious over Terashima in view of Shin, Sugimoto, Inoue and/or the OLSA

207. To the extent that Terashima does not anticipate claim 5, claim 5 is obvious over Terashima in view of Shin, Sugimoto, Inoue, and/or the OLSA. Shin and Sugimoto disclose the second n-electrode and the second p-electrode having virtually the same size as recited in claim 5 (*see supra* ¶¶ 81, 164, 200). Inoue further discloses an n electrode 36 and a p electrode 38 having virtually the same size in Fig. 4A (Ex-1021 at Fig. 4A & 1:58).

Inoue Fig. 4A

Fig. 4A
PRIOR ART



208. To the extent that Terashima does not disclose the second n-electrode and the second p-electrode having virtually the same size, it would have been obvious (and a POSITA would have been motivated) to have Terashima's second n-electrode and the second p-electrode have the virtually the same size (*see supra* § 8.2). Each electrode needs to be of sufficient size to mechanically connect to electrodes, provide electricity, and thermal heat dissipation. Both electrodes have similar requirements (Ex-1006 at ¶ [0103]; Ex-1006 at Figs. 8A, 8B; Ex-1005 at ¶¶ [0020], [0021], [0026]; Ex-1021 at Fig. 4A & 1:58). Therefore, it would have been obvious to a POSITA for Terashima's second n-electrode and second p-electrode to have virtually the same size (Ex-1006 at ¶ [0103]; Ex-1006 at Figs. 8A, 8B; Ex-1005

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at ¶¶ [0020], [0021], [0026]; Ex-1021 at Fig. 4A & 1:58). This was well-known and predictable (Ex-1006 at ¶ [0103]; Ex-1006 at Figs. 8A, 8B; Ex-1005 at ¶¶ [0020], [0021], [0026]; Ex-1021 at Fig. 4A & 1:58). Further, this simplifies the manufacturing process because the electrodes can be similarly formed. The results are predictable and an operable device results by combining Shin's, Sugimoto's, and/or Inoue's virtually the same size electrodes with Terashima.

209. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 5 is obvious.

9.6. Claim 6 is Obvious over Terashima, Sugimoto or Shin + Thin Film Art in view of Shelton and/or the OLSA

210. Claim 6 recites “wherein the conductive bonding material layer is any one of the members selected from a group consisting of solder, silver paste, and anisotropic conductive resin.” To the extent that this claim is definite and Terashima, Shin + Thin Film Art, and Sugimoto do not disclose this limitation, this claim is obvious over either (i) Terashima; (ii) Sugimoto, or (iii) Shin + Thin Film Art in view of Shelton and/or the OLSA. Shelton discloses that LED p and n electrodes can be bonded with solder to “mechanically secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at

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[0044]). Shelton's solder constitutes the claimed "conductive bonding material layer."

211. It was rudimentary for a POSITA to attach an LED to a circuit board with solder. For example, the '126 patent states that the prior art includes "in general, a mounting process onto a circuit board is carried out at low costs by using a conductive bonding material such as solder and silver paste" (Ex-1001 at 2:14-16). Shin discloses that a flip-chip of the type described by Terashima can be bonded to a printed circuit board or lead frame (Ex-1005 at ¶ [0013]). A POSITA was well-aware of circuit boards connecting lead frames to circuit boards (*see supra* § 8.5).

212. It would have been obvious to bond and of the LEDs in (i) Terashima; (ii) Sugimoto, or (iii) Shin + Thin Film Art to a circuit board with solder. Solder was the routine way to connect LED electrodes with circuit board electrodes. The results were predictable and the combination is operational. A POSITA would have been motivated to use known, proven techniques such as solder and silver paste.

213. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 6 is obvious.

9.7. Claim 7 is Obvious over Terashima, Sugimoto, or Shin + Thin Film Art in view of Shelton and/or the OLSA

214. To the extent that either Terashima or Sugimoto do not anticipate claim 7 and claim 7 is not obvious over Shin + Thin Film Art, claim 7 is obvious over Terashima, Shin + Thin Film Art, or Sugimoto in view of Shelton and/or OLSA. Shelton discloses that LED p and n electrodes can be bonded with solder, a “conductive material,” and “reflow alloy bonding” to “mechanically secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]). It was rudimentary for a POSITA to attach LED p and n electrodes to a circuit board with solder (*see supra* § 8.5, Ex-1011 at [0044]). The APA admits that “in general, a mounting process onto a circuit board is carried out at low costs by using a conductive bonding material such as solder and silver paste” (Ex-1001 at 2:14-16). Moreover, Shin discloses that a flip-chip of the type described by Terashima, Shin, and Sugimoto can be bonded to a circuit board (Ex-1005 at ¶ [0013]). Solder, conductive bumps, and silver paste were routine ways to connect LED electrodes with circuit board electrodes. The results were predictable, and the combination is operational. A POSITA would have been motivated to use known, proven techniques such as solder and silver paste.

215. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art,

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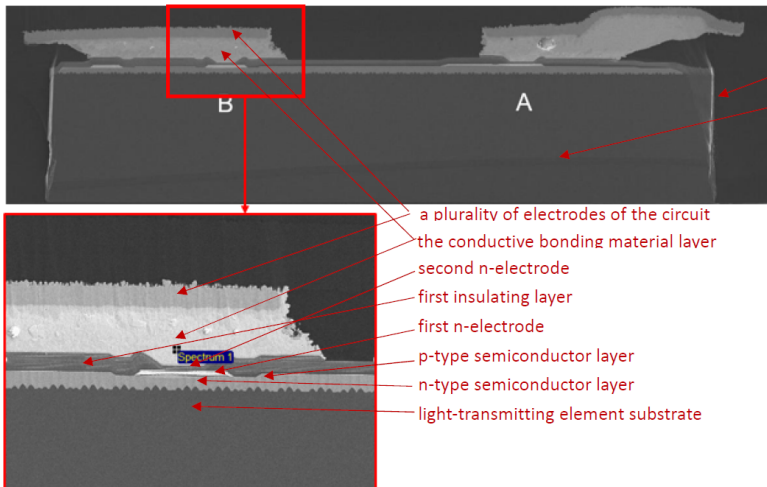
and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 7 is obvious.

9.8. Claim 8 is Obvious over Terashima, Shin + Thin Film Art, or Sugimoto in view of Shelton and/or the OLSA

216. Claim 8 recites “wherein the conductive bonding material layer is any one of the members selected from a group consisting of solder, silver paste, and anisotropic conductive resin. To the extent that this claim is definite and Terashima, Shin + Thin Film Art, and Sugimoto do not disclose this limitation, claim 8 is obvious over either (i) Terashima; (ii) Shin plus Thin Film Art; and (iii) Sugimoto in view of Shelton and/or the OLSA. Shelton discloses that LED p and n electrodes can be bonded with solder to “mechanically secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at [0044]). Shelton’s solder constitutes the claimed “conductive bonding material layer.” This comports with Everlight’s infringement contentions which contend that solder attaching an LED to a circuit board satisfy claim 6 as shown below (Ex-1016 at p. 32).

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Everlight's Infringement Contentions (Ex-1016)

6.1 The semiconductor light-emitting element according to claim 1, wherein the conductive bonding material layer is any one of the members selected from a group consisting of solder, silver paste and anisotropic conductive resin.	In the Accused Filament Product, the conductive bonding material layer is any one of the members selected from a group consisting of solder, silver paste and anisotropic conductive resin. See, e.g., EDX Analysis of <u>the second p-electrode of ROLLSBO LED BULB E26 140 LUMEN</u>: Spectrum 1 (below panel) shows the conductive bonding material layer (below panel) as obtained from SEM-EDX analysis. As shown in Spectrum 1 (below panel), the elements Tin (Sn) are present in the conductive bonding material layer (below panel), which is consistent with the conductive bonding material layer comprising solder.  The figure consists of two SEM-EDX analysis panels, A and B, showing cross-sections of an LED flip chip. Panel A is a larger cross-section showing the LED flip chip mounted on a light-transmitting element substrate. Labels point to the LED Flip Chip, light-transmitting element substrate, a plurality of electrodes of the circuit, the conductive bonding material layer, second n-electrode, first insulating layer, first n-electrode, p-type semiconductor layer, n-type semiconductor layer, and light-transmitting element substrate. Panel B is a smaller, magnified cross-section of the conductive bonding material layer, showing the presence of Tin (Sn) as indicated by Spectrum 1.
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217. It was rudimentary for a POSITA to attach an LED lead frame to a circuit board with solder. The '126 patent describes that “in general, a mounting process onto a circuit board is carried out at low costs by using a conductive bonding material such as solder and silver paste” (Ex-1001 at 2:14-16). Shin discloses that a flip-chip of the type described by Terashima can be bonded to a printed circuit board or lead frame (Ex-1005 at ¶ [0013]). A POSITA was well-aware of circuit boards connecting lead frames to circuit boards. Solder was the routine way to connect LED electrodes with circuit board electrodes. The results were predictable, and the combination is operational. A POSITA would have been motivated to use known, proven techniques such as solder and silver paste.

218. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 8 is obvious.

9.9. Claim 11 is Obvious over Sugimoto or Shin + Thin Film Art in view of Terashima and/or the OLSA

219. Claim 11 recites the “method for manufacturing a semiconductor light-emitting element according to claim 10, wherein the first insulating layer is formed through sputtering.” Neither Shin nor Sugimoto expressly state that the “first insulating layer is formed through sputtering.” However, Terashima teaches that the protective film 20, which is the claimed “first insulating layer,” “is formed by a film forming means such as vacuum deposition or sputtering” (Ex-1010 at ¶ [0036]). Sputtering to form insulation layers was well-known, predictable, and within the ordinary level of skill in the art (*see supra* § 8.5). A POSITA would have been motivated to use known sputtering techniques to form the claimed insulation layer (*see supra* § 8.5). The results were predictable, and the combination is operational. The ’126 patent did not invent a sputtering process. In fact, Everlight admits in its infringement contentions that “sputtering is commonly applied to the formation of electrode films or insulating later in the technical field of light emitting diode manufacturing” (Ex-1016 at p. 71; *see also* p. 74).

220. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 11 is obvious.

9.10 Claim 12 is Obvious over Shin + Thin Film Art in view of Terashima, Sugimoto, and/or the OLSA

221. Claim 12 provides the “method for manufacturing a semiconductor light emitting element according to claim 9, wherein the second n-electrode and the second p-electrode are formed through sputtering or plating.”

222. While Shin does not expressly state that Shin’s second n and p electrodes were formed through “sputtering or plating,” Terashima and Sugimoto disclose the limitations of claim 12 (*see supra* ¶¶ 9.1.10, 9.2.5). Sputtering or plating were common techniques for forming the claimed electrodes and well within the ordinary level of skill in the art (*see supra* § 8.5) (Ex-1010 at ¶¶ [0034]-[0035]; Ex-1010 at ¶¶ [0038], [0061]; Ex-1006 at ¶¶ [0155]; [0019]; Ex-1006 at ¶¶ [0020], [0021], [0024]). Sputtering and plating were predictable and routine techniques. The ’126 patent did not invent a sputtering a plating technique. Everlight admits in its infringement contentions that “sputtering is commonly applied to the formation of electrode films or insulating layer in the technical field of light emitting diode manufacturing” and “sputtering or plating is commonly applied to the formation

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electrode films in the technical field of light emitting diode manufacturing” (Ex-1011 at p. 71, 74). Therefore, a POSITA would have been motivated to use the known sputtering and plating techniques to form the claimed electrodes.

223. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 12 is obvious.

9.11 Claim 13 is Obvious over Terashima, Sugimoto, or Shin + Thin Film Art, in view of Shelton and/or the OLSA

224. Claim 13 recites a “method for mounting semiconductor light-emitting elements, comprising: placing solder between the second n-electrode as well as the second p-electrode of the semiconductor light-emitting element according to claim 1 and a plurality of electrodes on a circuit board, and then carrying out a reflow treatment thereon, thereby the semiconductor light-emitting elements are mounted on the circuit board through solder.”

225. Terashima discloses using “solder” 31 to attach its LED to a circuit board (Ex-1010 at [0062]). Sugimoto discloses using an adhesion layer having an upper of silver or gold and a lower layer that may be tin to mount an LED to a circuit board (Ex-1006 at ¶ [0089] (*see supra* ¶ 164). Shin discloses using gold bumps (Ex-1005 at ¶ [1061]). The references do not explicitly mention reflow treatments.

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226. Shelton discloses that an LED with n and p electrodes that can be bonded with solder and “reflow alloy bonding” to “mechanically secure” a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]). Further, this was common knowledge, within the level of ordinary skill in the art, predictable to a POSITA, and the benefits of reflow treatments were known (*see supra* § 8.6). Reflow ensures that the solder flows and good connections are obtained between the electrodes. Reflow involves using controlled heat, in for example an oven, to the solder, causing the solder to reflow and provide a better connection. Typically, solder and solder paste are applied to the electrodes. Heat is then applied generally with hot air or with heat radiation. The solder paste melts and after heat is removed solidifies to form a stable connection. The results were predictable, and the combination is operational. Therefore, a POSITA would have been motivated to use the routine known techniques claimed to mount an LED on a circuit board. A POSITA would have been motivated to use a common solder attachment process with known reflow treatments to achieve the benefits of reflow and because solder can be cheaper than gold or silver (*see supra* § 8.6).

227. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art, and the lack of any known secondary factors of nonobviousness. My conclusion is that claim 13 is obvious.

9.12 Claim 1, 2, and 4-13 are Obvious over Terashima in view of the Thin Film Art and the Other Art Applied with Tersashima

228. To the extent that Patent Owner claims that Terashima does not teach the “thin film” claim limitations, I disagree. However, even if Patent Owner were correct, claims 1, 2, and 4-13 would be invalid as obvious over Terashima in view of one or more of the Thin Film Art which discloses thin films and the other art as combined with Terashima as explained above for each respective claim.

229. Terashima discloses Terashima describes the first n-electrode 5a as a “plated growth film,” “thin,” and formed by a “film deposition method, such as vacuum deposition, sputtering, or printing” (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]), which are processes known for making thin film electrodes. Terashima also explains that the film 4a or first n-electrode must be “thin enough to maintain transparency” (Ex-1010 at ¶ [0035]).

230. Terashima’s “plated growth film 4a” [red] is the claimed “first p-electrode that is a thin film formed on the p-type semiconductor layer.” Terashima describes the first p-electrode 5a is a “plated growth film,” “thin,” and formed with a “film deposition method, such as vacuum deposition, sputtering, or printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]), which are processes known for making thin film electrodes.

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231. Terashima describes the second n-electrode is a “film” or “single layer film” (e.g., “thin”) (Ex-1010 at ¶¶ [0038], [0059]).

232. Terashima describes the second p-electrode as a “film” or “single layer film” (e.g., “thin”) (Ex-1010 at ¶¶ [0038], [0059]).

233. To the extent that Patent Owner contends that any of these disclosures are not thin films, I disagree. Each of the Thin Film Art discloses thin film electrodes (*see supra* § 8.2).

234. A POSITA would have been motivated to use the Thin Film Art as taught by each reference as thin film electrodes for the electrodes in Terashima as described above with reference to Shin (*see supra* § 8.2). Terashima describes that the first electrodes are thin film and make with thin film manufacturing techniques (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0049], [0061]). Terashima describes that the second electrodes are films or single layer films (Ex-1010 at ¶¶ [0038], [0059]). A POSITA would have been motivated to use thin film from any of the Thin Film Art based on Terashima’s disclosure, the known benefits of using thin film electrodes, the widespread use of thin film electrodes, the known manufacturing processes, and the predictability (*see supra* § 8.2) and as described above with reference to Shin.

235. I have considered the scope and content of the prior art, that there are no differences between the claims and the art, the level of ordinary skill in the art,

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and the lack of any known secondary factors of nonobviousness. My conclusion is that claims 1, 2, and 4-13 are obvious.

10. Secondary Considerations of Non-Obviousness

236. I am not aware of any secondary considerations of nonobviousness.

11. Use of Demonstratives

237. I reserve the right to make demonstratives (including product demonstrations, product usage, and videos thereof), charts, graphs, or other similar visual aids for trial based upon the opinions expressed in this report, the data contained in this report, the exhibits or other things cited in this report and/or attached as exhibits to this report.

12. Sworn Statement

238. I, Dr. Michael S. Lebby, do hereby declare and state, that: (1) all statements made herein of my own knowledge are true; (2) all statements made herein on information and belief are believed to be true; and (3) these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: May 31, 2024



Dr. Michael S. Lebby

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