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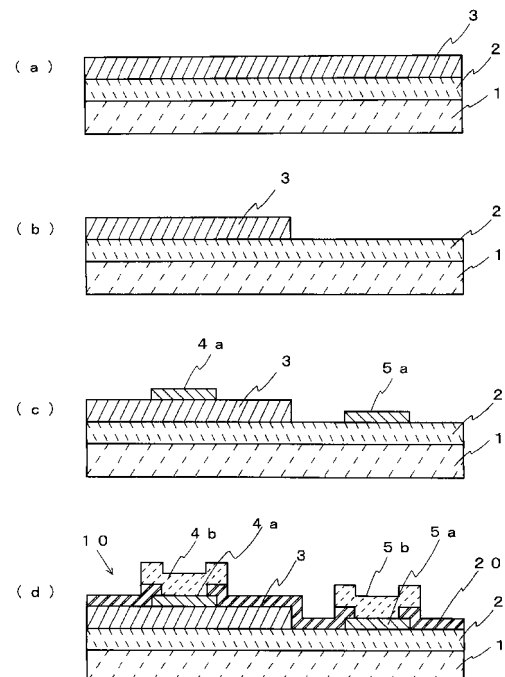
(54) [Title of Invention] OPTICAL SEMICONDUCTOR ELEMENT MANUFACTURING METHOD, OPTICAL SEMICONDUCTOR ELEMENT, AND OPTICAL SEMICONDUCTOR DEVICE EQUIPPED WITH OPTICAL SEMICONDUCTOR ELEMENT

(57) [Abstract]

[Problem] In the configuration and manufacturing method of conventional optical semiconductor elements, a lift-off method is used as means for forming connection electrodes consisting of an n-electrode and a p-electrode made of the same material, which requires large-scale equipment, increases manufacturing costs, and creates problems with manufacturing yields.

[Resolution Means] A manufacturing method is adopted that includes a step for providing a plating growth film mainly composed of a metal on which an electroless plating film can be deposited on at least a portion of the surface of one of the p-type and n-type semiconductor layers, and a step for simultaneously forming one connection electrode that covers the plating growth film by electroless plating, and the other connecting electrode on the surface of the other semiconductor layer.

[Selected Drawing] FIG. 1



[Scope of Patent Claims]

[Claim 1]

A manufacturing method of an optical semiconductor element having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode formed from the same metal material on upper layers of the p-type and n-type semiconductor layers, respectively, the manufacturing method comprising:

a step for forming the p-type and n-type semiconductor layers; a step for providing, on at least a portion of the surface of each of the semiconductor layers, a plating growth film mainly composed of a metal on which an electroless plating film can be deposited; and a step for simultaneously forming a pair of connection electrodes covering the plating growth film by electroless plating.

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[Claim 2]

A optical semiconductor element manufacturing method having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode formed from the same metal material on upper layers of the p-type and n-type semiconductor layers, respectively, the manufacturing method comprising:

a step for forming the p-type and n-type semiconductor layers; a step for providing, on at least a portion of the surface of each of the semiconductor layers, a plating growth film mainly composed of a metal on which an electroless plating film can be deposited; and a step for simultaneously forming one connection electrode covering the plating growth film, and another connection electrode on the surface of the semiconductor layer, by electroless plating.

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[Claim 3]

The manufacturing method of an optical semiconductor device according to claim 1 or 2, further comprising a step for forming a protective film that exposes at least a portion of each of the p-type and n-type semiconductor layers or the plating growth film before the step for simultaneously forming the pair of connection electrodes.

[Claim 4]

The manufacturing method of an optical semiconductor device according to claim 3, wherein the thickness of the connection electrode is controlled by adjusting the size of an opening in the exposed portion of the protective film.

[Claim 5]

The optical semiconductor element manufacturing method according to claim 1 or 2, further comprising a step for forming a separating partition wall for separating the pair of connection electrodes on a surface of the semiconductor layer before the step for simultaneously forming the pair of connecting electrodes.

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[Claim 6]

The optical semiconductor element manufacturing method according to claim 5, wherein the connection electrodes are formed by covering the plating growth film and covering the entire surface of the semiconductor layer exposed at the surface.

[Claim 7]

The optical semiconductor element manufacturing method according to any one of claims 1 to 6, wherein the connection electrodes are formed at a thickness that functions as a barrier metal layer, and a protruding electrode is further provided on an upper layer thereof.

[Claim 8]

The optical semiconductor element manufacturing method according to any one of claims 1 to 7, wherein the film thickness of the connection electrode is controlled by the film thickness of the plating growth film.

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[Claim 9]

An optical semiconductor, being formed by the optical semiconductor element manufacturing method according to any one of claims 1 to 8.

[Claim 10]

An optical semiconductor device in which the optical semiconductor element according to claim 9 is flip chip mounted.

[Detailed Description of Invention]

[0001]

[Technical Field of Invention]

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The present invention relates to: a manufacturing method of an optical semiconductor element having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode respectively formed from the same metal material on the p-type and n-type semiconductor layers, and having respective functions of a light-emitting element that converts electricity into light and emits such, and a light-receiving element that receives incident light and converts such into electricity; an optical semiconductor element; and an optical semiconductor device in which the optical semiconductor element is

mounted.

[0002]

[Conventional Art]

In recent years, optical semiconductor elements in which p-type and n-type nitride semiconductor layers made of gallium nitride compounds are formed on an insulating transparent circuit board, and a pair of positive and negative connection electrodes are provided on the same plane have attracted attention. The structure of an optical semiconductor element that is conventional art is illustrated in FIG. 6.

[0003]

FIG. 6(d) is a structural cross-sectional view illustrating the configuration of an optical semiconductor element formed by conventional art.

This optical semiconductor element 111 has a p-n junction in which an n-type nitride semiconductor layer 102 and a p-type nitride semiconductor layer 103 composed of a gallium nitride compound are laminated on a transparent insulating circuit board 101 composed of a material such as sapphire, and a p-electrode 104 and an n-electrode 105 composed of the same metal material are formed on the surfaces of the p-type nitride semiconductor layer 103 and the n-type nitride semiconductor layer 102, respectively (for example, see patent document 1).

This n-electrode 105 is formed on the surface of the n-type nitride semiconductor layer 102 exposed by selectively etching a portion of the p-type nitride semiconductor layer 103 of the p-n junction. By configuring as such, an optical semiconductor element 111 is obtained that has a pair of positive and negative connection electrodes, consisting of a p-electrode and an n-electrode, on the same plane of each of the nitride semiconductor layers described above.

[0004]

In the optical semiconductor element 111 having the foregoing structure, when a predetermined voltage is applied across the p-electrode 104 and the n-electrode 105, electron holes from the p-electrode 104 side and electrons from the n-electrode 105 side recombine near an interface across the n-type nitride semiconductor layer 102 and the p-type nitride semiconductor layer 103, resulting in light emission.

[0005]

Here, a method for manufacturing the optical semiconductor element 111 will be described with reference to FIGS. 6(a) to (d).

First, as illustrated in FIG. 6(a), a p-n junction is formed by stacking the n-type nitride semiconductor layer 102 made of n-GaN and the p-type nitride semiconductor layer 103 made of p-GaN on the insulating transparent insulating substrate 101 by means of metal-organic chemical vapor deposition or the like.

[0006]

Next, as illustrated in FIG. 6(b), a portion of the p-type nitride semiconductor layer 103 is selectively etched away from the p-n junction to expose the n-type nitride semiconductor layer 102.

[0007]

Subsequently, as illustrated in FIG. 6(c), in order to simultaneously form the p-electrode 104 and the n-electrode 105, which are a pair of connection electrodes, by a single lift-off, a resist is applied to the surfaces of the nitride semiconductor layers 102 and 103 to form a mask pattern 121, and Ni, Ti, and Au are further sequentially stacked on the surface of the mask pattern 121 by a vacuum deposition method to form a metal layer 122.

[0008]

Then, by removing the mask pattern 121, the optical semiconductor element 111 having the pair of connection electrodes (the p-electrode 104 and the n-electrode 105) on the surfaces of the nitride semiconductor layers 102 and 103 is obtained as illustrated in FIG. 6(d).

[0009]

Here, the metal materials used for the p-electrode and the n-electrode are required to have good ohmic contact with both the p-type nitride semiconductor layer 103 and the n-type nitride semiconductor layer 102, and therefore, elemental metals such as Au, Pd, Ti, Pt, Mo, Cr, Al, Co, Rh, Ir, Mn, V, Sc, Mg, and Zr, or laminated films made of alloys are used.

[0010]

[Patent Document 1]

JP H9-232632 A (Pages 3 to 4, FIG. 1, FIG. 2)

[0011]

[Problem to Be Solved by Invention]

In this manner, in order to form the connection electrodes consisting of the n-electrode 105 and the p-electrode 104 made of the same material as in the optical semiconductor element 111 of the conventional art described above, a lift-off method is employed as the means therefor.

[0012]

As described above, this lift-off method requires a large-scale deposition apparatus such as a vacuum deposition apparatus or a sputtering apparatus in order to deposit the metal layer 122 over the entire surface of the resist, including the openings formed by the mask pattern 121. 10

[0013]

Furthermore, according to this method, the openings formed in the mask pattern 121 occupy only a small portion of the resist surface area, and thus most of the metal layer is removed by this process. Therefore, the material cost of the metal layer 122 is wasted, inflating manufacturing costs.

[0014]

Furthermore, when the resist and the overlying metal layer 122 are removed, leaving only the metal layer 123 in the opening illustrated in FIG. 6(c), the portions in the opening that are to be left as connection electrodes may also be peeled off, resulting in portions where the pair of connection electrodes is not formed.

[0015]

Due to the foregoing reasons, the lift-off method has poor productivity as a technique for forming electrodes applied to optical semiconductor elements and cannot be said to be a preferable manufacturing method when the mass production of optical semiconductor elements is taken into consideration. 20

[0016]

An object of the present invention is to solve the foregoing problems and to provide: a method for manufacturing an optical semiconductor element having good element characteristics and a simple manufacturing process; an optical semiconductor element; and an optical semiconductor device in which the optical semiconductor element is mounted.

[0017]

[Means for Solving Problem]

In order to solve the foregoing problems, the following configurations and manufacturing methods are adopted. 30
The method for manufacturing an optical semiconductor element according to claim 1 of the present invention is a method for manufacturing an optical semiconductor element having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode formed from the same metal material on upper layers of the p-type and n-type semiconductor layers, respectively, including: a step for forming the p-type and n-type semiconductor layers; a step for providing, on at least a portion of the surface of each of the semiconductor layers, a plating growth film mainly composed of a metal on which an electroless plating film can be deposited; and a step for simultaneously forming a pair of connection electrodes covering the plating growth film by electroless plating.

[0018]

Furthermore, the method for manufacturing an optical semiconductor element according to claim 2 of the present invention is a method for manufacturing an optical semiconductor element having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode formed from the same metal material on upper layers of the p-type and n-type semiconductor layers, respectively, including: a step for forming the p-type and n-type semiconductor layers; a step for providing, on at least a portion of the surface of each of the semiconductor layers, a plating growth film mainly composed of a metal on which an electroless plating film can be deposited; and a step for simultaneously forming one connection electrode covering the plating growth film, and another connection electrode on the surface of the semiconductor layer, by electroless plating. 40

[0019]

Furthermore, the optical semiconductor element manufacturing method according to claim 3 of the present invention includes, before the step for simultaneously forming the pair of connection electrodes, a step for forming a protective film that exposes at least a portion of each of the p-type and n-type semiconductor layers or the plating growth film. 50

[0020]

Furthermore, the optical semiconductor element manufacturing method according to claim 4 of the present invention controls the film thickness of the connection electrode based on the size of the opening diameter of the exposed

portion of the protective film.

[0021]

Furthermore, the optical semiconductor element manufacturing method according to claim 5 of the present invention includes, before the step for simultaneously forming the pair of connection electrodes, a step for forming a separating partition wall for separating the pair of connection electrodes on the surface of the semiconductor layer.

[0022]

Furthermore, in the optical semiconductor element manufacturing method according to claim 6 of the present invention, the connection electrodes are formed by covering the plating growth film and covering the entire surface of the semiconductor layer exposed on the surface.

[0023]

Furthermore, in the optical semiconductor element manufacturing method according to claim 7 of the present invention, the connection electrode is formed at a thickness that functions as a barrier metal layer, and a protruding electrode is further provided on an upper layer thereof.

[0024]

Furthermore, the optical semiconductor element manufacturing method according to claim 8 of the present invention controls the film thickness of the connection electrode based on the film thickness of the plating growth film.

[0025]

Furthermore, the optical semiconductor element according to claim 9 of the present invention is formed by one of the manufacturing methods of optical semiconductor elements described above.

[0026]

Furthermore, in the optical semiconductor device according to claim 10 of the present invention, the optical semiconductor element described above formed by flip chip mounting.

[0027]

[Embodiments of Invention]

Embodiments will be described below with reference to the following drawings.

The optical semiconductor element described below refers to a semiconductor element having a light emitting or light receiving function and specifically indicates a light emitting diode, a semiconductor laser, a photodetector, a solar cell, and the like.

Furthermore, in the following embodiments of the optical semiconductor element of the present invention, the configuration and manufacturing method of a single element will be described, but it should be understood that in actual production, a large number of optical semiconductor elements are formed at once and then cut into individual elements.

[0028]

(First Embodiment)

First, the configuration of an optical semiconductor element formed according to the present invention will be described. FIG. 1(d) is a structural cross-sectional view illustrating an optical semiconductor element according to the first embodiment of the present invention.

Similarly to the conventional configuration, this optical semiconductor element 10 has an n-type nitride semiconductor layer 2 on a transparent insulating substrate 1, and a p-type nitride semiconductor layer 3 electrically connected to the upper layer thereof is provided. Furthermore, the underlying n-type nitride semiconductor layer 2 is exposed from a portion of a junction surface between the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3, providing a p-n junction on the same plane.

[0029]

Furthermore, plating growth films 4a and 5a are provided on exposed upper layers of the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3. The plating growth film 4a provided on the upper layer of this p-type nitride semiconductor layer 3 is provided at a location where a p-electrode 4b is to be formed, and the plating growth film 5a provided on the upper layer of the n-type nitride semiconductor layer 2 is provided at a location where an n-electrode 5b is to be formed.

Also, a protective film 20 is provided by forming an opening in a portion of the plating growth films 4a and 5a, the p-electrode 4b is provided on the plating growth film 4a exposed from the opening of the protective film 20, and the n-electrode 5b on the plating growth film 5a, and these electrodes 4b and 5b are connected to respective nitride semiconductor layers 3 and 2.

[0030]

In this optical semiconductor device 10, similarly to the conventional configuration, by applying a predetermined voltage across the p-electrode 4b and the n-electrode 5b, electron holes from the p-electrode 4b and electrons from

the n-electrode 5b are recombined near the junction interface across the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3, thereby emitting light.

[0031]

Furthermore, it is needless to say that this optical semiconductor element 10 can be used as a light receiving element that detects a degree of light irradiation from the potential difference generated across the electrodes.

[0032]

Here, the optical semiconductor element manufacturing method according to the present invention will be described in detail with reference to FIGS. 1(a) to (d)

First, as illustrated in FIG. 1(a), a gallium nitride-based semiconductor layer is formed as the n-type nitride semiconductor layer 2 on the entire surface of a transparent insulating substrate 1 made of a material such as cleaned sapphire (Al₂O₃), spinel (MgAl₂O₄), silicon carbide (SiC), silicon (Si), zinc oxide (ZnO), or gallium nitride (GaN) by means of such a CVD method or the like. Next, the gallium nitride semiconductor layer is doped with a p-type dopant such as Zn, Mg, Be, Ca, Sr, or Ba to form the upper layer portion of the n-type nitride semiconductor layer 2 into the p-type nitride semiconductor layer 3. 10

[0033]

Subsequently, as illustrated in FIG. 1(b), a portion of the p-type nitride semiconductor layer 3 is removed by a combination of means such as photolithography and etching, and the underlying n-type nitride semiconductor layer 2 is exposed from a portion of the junction surface between the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3.

[0034]

Furthermore, as illustrated in FIG. 1(c), plating growth films 4a and 5a containing, as a main component, a metal that enables growth by electroless plating are provided on a portion of the n-type nitride semiconductor 2 and the upper layer of the p-type nitride semiconductor 3, respectively, by a film deposition method such as vacuum deposition, sputtering, or printing. Metals that can be used here include Ni, Pd, Au, and the like. Instead of this metal, a conductive resin such as a conductive paste may be formed by a printing method. Furthermore, although any of the metal materials listed here can be used to form the p-electrode 4b and the n-electrode 5b to be described later by electroless plating, other metals may be used insofar long as they undergo a precipitation reaction with the metal in the electroless plating bath. Among these, the most desirable metals are Ni and Pd, which have excellent oxidation resistance and electrical conductivity, and metal compositions containing these metal elements as main components. 30

[0035]

Furthermore, although not illustrated in the figure, the plating growth films 4a and 5a may be formed to cover as wide an area as possible of the surface of each of the nitride semiconductor layers 2 and 3. By configuring as such, a voltage can be efficiently applied to each of the nitride semiconductor layers 2 and 3, which are active layers, and stronger light emission can be obtained. In particular, the p-type nitride semiconductor layer 3 tends to have a relatively high resistance value compared to the n-type, and thus it is preferable to have a configuration in which the plating growth film 4a is thin and disposed over the entire surface of at least the upper layer of the p-type nitride semiconductor layer 3. However, in the case of an optical semiconductor device (LED component) configured to externally extract light emitted from an optical semiconductor element 10 through a transparent insulating substrate 1, this plating growth film must be formed thin enough to maintain transparency. This is because the plating growth films 4a and 5a hinder the light emission of the optical semiconductor element 10. 40

[0036]

Subsequently, as illustrated in FIG. 1(d), a protective film 20 that forms an opening in at least a portion of the plating growth films 4a and 5a is formed. A material having good insulating properties, such as silicon oxide (SiO₂) or silicon nitride (Si₃N₄) is used as the material of this protective film 20, which is formed by a film forming means such as vacuum deposition or sputtering. Subsequently, the opening is formed by a photolithographic etching process.

[0037]

Then, the foregoing structure is immersed in an electroless plating solution to form the p-electrode 4b and an n-electrode 5b on the portions of the plating growth films 4a and 5a exposed from the protective film 20, respectively. At such time, the plating growth films 4a and 5a are made of a material mainly composed of metal such as Ni, Pd, or Au, but when the p-electrode 4b and the n-electrode 5b are formed using a metal element that is the same as or more base than the elements in the plating growth films 4a and 5a, the desired electrode structure can be formed by electroless plating. A desirable material for the p-electrode 4b and the n-electrode 5b used here is Ni, which has excellent electrical conductivity and corrosion resistance. Furthermore, as the electroless Ni plating solution, a plating solution that supplies Ni ions through sulfuric acid or a Ni chloride salt and uses NaH₂PO₂, KH₂PO₃, NaBH₄, 50

KBH₄, hydrazine, formalin, or the like as a reducing agent.

Through the above steps, the optical semiconductor element of the present invention is completed.

[0038]

Note that the inventors have also found that the start time of electroless plating and the growth rate of the plating metal can be controlled according to the exposed area of the surfaces of the plating growth films 4a and 5a or the film thicknesses of the plating growth films 4a and 5a.

That is, by increasing the opening diameter of the protective film 20 and increasing the exposed area of the surfaces of the plating growth films 4a and 5a, the time when the plated metal begins to adhere after immersion in the plating solution is earlier and the rate at which this plating grows is faster. In contrast, by decreasing the opening diameter of the protective film 20 and increasing the exposed area of the surface of the plating growth film 4a, the time when the plated metal begins to adhere after immersion in the plating solution is later and the rate at which this plating grows is slower.

Furthermore, when the plating growth films 4a and 5a are thick, the time when the plating metal begins to adhere after immersion in the plating solution tends to be earlier and the growth rate of the plating metal tends to be faster.

By utilizing the foregoing phenomenon, it becomes possible to control the film thickness of the p-electrode 4b and the n-electrode 5b, and the p-electrode 4b and the n-electrode 5b can be formed to a desired thickness.

[0039]

As above, a p-n junction has been described as the junction form of the optical semiconductor element 10 of the present invention, but the art of the present invention can also be used for MIS junctions and PIN junctions, and can also be applied to optical semiconductor elements with single heterostructures and double heterostructures.

[0040]

Furthermore, an example has been illustrated in which plating growth films 4a and 5a are provided on the upper layers of the nitride semiconductor layers 2 and 3, respectively, and a protective film 20 is provided so that parts of the plating growth films are exposed; however, although not illustrated in the drawing, after forming the structure of FIG. 1(c), it is also possible to form the protective film 20 exposing parts of the nitride semiconductor layers 2 and 3, form a plating growth film in the location where the connection electrode is to be formed, and then deposit a connection electrode covering the plating growth film by electroless plating.

[0041]

(Second Embodiment)

FIG. 2 is a structural cross-sectional view for describing a second embodiment.

The optical semiconductor element illustrated in the second embodiment is the same as that of the first embodiment in that it has a pair of connection electrodes on each of the upper layers of an n-type nitride semiconductor layer 2 and a p-type nitride semiconductor layer 3 formed on a transparent insulating substrate 1, but differs in that one of the connection electrodes is connected to one of the nitride semiconductor layers via a plating growth film, and the other connection electrode is directly connected to the other nitride semiconductor layer.

An optical semiconductor element 11 illustrated here has a configuration in which the plating growth film 4a is provided only on the surface of the p-type nitride semiconductor layer 3, as one example.

[0042]

According to the present embodiment, forming the plating growth film 4a only on the surface of the p-type nitride semiconductor layer 3 illustrated in FIG. 2(e) by means of, for example, mask deposition or printing has an advantage in terms of manufacturing in that it can be performed more easily than forming on the exposed portion (the lower surface of a step portion) of the n-type nitride semiconductor layer 2. In other words, a step is formed in the n-type nitride semiconductor layer 2 where at least a portion of the surface is exposed, and due to this step, a gap is created between the mask for the above-mentioned mask deposition, printing, or the like, and the surface of the n-type nitride semiconductor layer 2 corresponding to the bottom of the step. When mask deposition or printing is performed in this state, it will be impossible to precisely form a plating growth film 5a. In order to avoid this, the plating growth film 5a must be formed in a photolithographic etching step. In this way, when considering improvement in productivity, it is desirable to form the plating growth film 4a on the surface of the p-type nitride semiconductor layer 2.

[0043]

Next, a method for manufacturing the optical semiconductor device 11 will be described with reference to FIGS. 1(a) and (b) and FIGS. 2(c) to (e).

First, similarly to the first embodiment, the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3 are laminated on the transparent insulating substrate 1 by the steps illustrated in FIGS. 1(a) and (b), and a structure is further formed in which at least a portion of the n-type nitride semiconductor layer 2 is exposed.

[0044]

Furthermore, as illustrated in FIG. 2(c), one of plating growth films 4a and 5a is formed on the upper surface of either one of the nitride semiconductor layers 2 and 3 at least at a location where a connection electrode is to be formed. 10

[0045]

Subsequently, as illustrated in FIG. 2(d), the protective film 20 is formed such that at least a portion of both nitride semiconductor layers of the structure illustrated in FIG. 2(c) is exposed. The material of the protective film 20 is the same as that of the first embodiment.

[0046]

Subsequently, as illustrated in FIG. 2(e), the structure illustrated in FIG. 2(d) is immersed in the electroless plating solution used in the first embodiment. Then, an electroless plating film is deposited on the surface of the plating growth film 4a to form the p-electrode 4b. At this time, the p-type nitride semiconductor layer 3 is directly connected to the lower layer of the plating growth film 4a and the n-type nitride semiconductor layer 2 is further 20 connected to the p-type nitride semiconductor layer 2, and thus the potential of both nitride semiconductor layers 2 and 3 relative to the electroless plating bath (the state for transferring electrons to and from the metal in the electroless plating bath) changes, and the n-electrode 5b can be deposited not only on the p-electrode 4b, which is an electroless plating film, but also on the n-type nitride semiconductor layer 2, on which it is generally considered impossible to directly form an electroless plating film. Thus, the electroless plating film precipitated from the plating growth film 4a is formed up to the opening of the protective film 20 where the n-type nitride semiconductor layer is exposed, and the p-electrode 4b and the n-electrode 5b connected to both nitride semiconductor layers 2 and 3 can be formed as illustrated in FIG. 2(e), thereby completing the optical semiconductor element 11. When the nitride semiconductor layers 2 and 3 are materials that cannot be electroless plated, this plating growth film 4a is preferably formed from Ni, which is highly effective in preventing diffusion of material components of 30 a pair of connection electrodes disposed above the nitride semiconductor layers into the nitride semiconductor layers, but this is not particularly limited to Ni.

[0047]

Note that in the present embodiment, an example has been described in which only the plating growth film 4a is disposed on the upper layer of the p-type nitride semiconductor layer 3 to form the p-electrode 4b and the n-electrode 5b, but the plating growth film 5a may be disposed on the surface of the n-type nitride semiconductor layer 2 to form both electrodes.

[0048]

Furthermore, in the method described above for manufacturing the optical semiconductor element 10 in FIG. 1, the plating growth film 4a is formed after at least a portion of the n-type nitride semiconductor layer 2 is exposed, 40 but the plating growth film 4a may be provided before the n-type nitride semiconductor layer 2 is exposed.

[0049]

(Third Embodiment)

FIG. 3 is a structural cross-sectional view for describing a third embodiment.

As illustrated in FIG. 3(e), an optical semiconductor element 12 of the third embodiment differs from the first embodiment in that, instead of the arrangement structure of the protective film 20 illustrated in the first embodiment, a separating partition wall 21 is provided for electrically isolating the p-electrode 4b and the n-electrode 5b, the p-electrode 4b is formed not only on the surface of the plating growth film 4a but also on the p-type nitride semiconductor layer 3 exposed on the surface, and similarly, the n-electrode 4c is formed not only on the surface of the plating growth film 5a but also on the n-type nitride semiconductor layer 2 exposed on the 50 surface.

[0050]

In this manner, by disposing a thin metal film on the exposed surface portions of the nitride semiconductor layers 2 and 3 excluding the plating growth films 4a and 5a portions, the voltage applied from the p-electrode 4b and the n-electrode 5b can be efficiently transmitted to the p-type nitride semiconductor layer 3 and the n-type nitride semiconductor layer 2, which are active layers, thereby enabling the optical semiconductor element 12 to emit

stronger light.

[0051]

Here, the optical semiconductor element manufacturing method according to the present invention will be described in detail using FIGS. 1(a) to (c) and FIGS. 3(d) and (e).

First, similarly to the first embodiment, the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3 are laminated on the transparent insulating substrate 1 by the steps illustrated in FIGS. 1(a) to (c), a structure is further formed in which at least a portion of the n-type nitride semiconductor layer 2 is exposed, and the plating growth films 4a and 5a are formed on the upper surfaces of the nitride semiconductor layers 2 and 3 at locations where the p-electrode 4b and the n-electrode 5b are formed.

[0052]

Next, as illustrated in FIG. 3(d), the separating partition wall 21 is formed to cover at least the boundary portion across the p-type nitride semiconductor layer 3 and the n-type nitride semiconductor layer 2 exposed on the surface of the structure illustrated in FIG. 1(c). The separating partition wall 21 can be formed by applying an insulating resin such as polyimide to the boundary surface by means of screen printing or the like, and then curing the resin. Note that the insulating resin may be applied to the entire surface by spin coating, and then the separating partition wall 21 may be formed by a photolithography etching process that leaves only necessary areas.

[0053]

Subsequently, as illustrated in FIG. 3(e), the structure illustrated in FIG. 3(d) is immersed in the electroless plating solution used in the first embodiment. Then, an electroless plating film is deposited on the surfaces of the plating growth films 4a and 5a. At this time, the plating growth films 4a and 5a are in contact with both nitride semiconductor layers 2 and 3, and thus the potential of the nitride semiconductor layers 2 and 3 with respect to the electroless plating bath changes, enabling the p-electrode 4b and the n-electrode 5b, which are electroless plating films, to be deposited, and this electroless plating film can be formed on the surfaces of both nitride semiconductor layers 2 and 3 that are exposed at the surface.

Through the above steps, the p-electrode 4b and the n-electrode 5b having uniform thicknesses can be formed over the entire surfaces of both nitride semiconductor layers 2 and 3 and the plating growth films 4b and 5b except for the portion of separating partition wall 21 illustrated in FIG. 3(e), completing the optical semiconductor element 12 of the present invention.

[0054]

These plating growth films 4a and 5a are preferably formed from Ni, which is highly effective in preventing diffusion of material components of a pair of connection electrodes disposed above the nitride semiconductor layers 2 and 3 into the nitride semiconductor layers, but are not particularly limited to Ni.

[0055]

(Fourth Embodiment)

FIG. 4 is a structural cross-sectional view for describing the configuration of the optical semiconductor element of a fourth embodiment.

An optical semiconductor device 13 illustrated in FIG. 4 differs from the first embodiment only in that protruding electrodes 6 composed of solder or the like are provided on the upper stages of the p-electrode 4b and n-electrode 5b, and the configuration is otherwise the same.

[0056]

In the fourth embodiment, the p-electrode 4b and the n-electrode 5b need only function as a barrier metal to suppress diffusion of the material of the plating growth films 4a and 5a located below and the protruding electrode 6 located above them, and also to maintain adhesion to the members arranged above and below them, and thus a thickness of at least a few microns achieved by electroless plating is sufficient.

[0057]

This optical semiconductor element 13 is provided with the p-electrode 4b and the n-electrode 5b, and is further provided with the protruding electrode 6 composed of solder or the like provided on the upper layer thereof, and thus the height of the electrodes themselves can be increased, making this an effective configuration for such applications.

[0058]

Here, the method for manufacturing the optical semiconductor element 13 according to the present invention will be described in detail using FIGS. 1(a) to (c) and FIG. 4(d).

First, similarly to the first embodiment, the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3 are laminated on the transparent insulating substrate 1 by the steps illustrated in FIGS. 1(a) to (c), a structure is further formed in which at least a portion of the n-type nitride semiconductor layer 2 is exposed, and the plating growth films 4a and 5a are formed on the upper surfaces of the nitride semiconductor

layers 2 and 3 at locations where the p-electrode 4b and the n-electrode 5b are formed.

[0059]

Furthermore, as illustrated in FIG. 4, after forming the protective film 20 exposing at least a portion of each of the plating growth films 4a and 5a, the p-electrode 4b and the n-electrode 5b composed of Ni, Pd, Pt, or the like are simultaneously formed by electroless plating. This formation method and plating solution are the same as those in the first embodiment. The materials for the p-electrode 4b and n-electrode 5b used here are not limited to the above Ni, Pd, and Pt, but may be a metal single layer film, a laminated film combining multiple materials, or an alloy that has a barrier metal function to suppress diffusion of the material of the plating growth films 4a and 5a located in the lower layer and the protruding electrode 6 formed on the upper layer, and that is expected to provide good connection between the two components.

[0060]

Subsequently, the protruding electrodes 6 composed of a brazing material such as solder are formed on the p-electrode 4b and the n-electrode 5b, completing the optical semiconductor element 13 of the present invention. Note that one example of a method for forming the protruding electrodes 6 is to supply brazing material onto the p-electrode 4b and the n-electrode 5b by printing a brazing material paste or mounting brazing material balls, or the like, and then melt the brazing material to form the protruding electrodes 6. At this time, by plating the surfaces of the p-electrode 4b and the n-electrode 5b with gold and further using flux, good adhesion between the protruding electrodes 6 and the p-electrode 4b and n-electrode 5b can be obtained.

[0061]

(Fifth Embodiment)

An optical semiconductor device (LED component) on which the optical semiconductor elements 10 to 13 formed according to the first to fourth embodiments are mounted will be described below.

First, a plurality of semiconductor elements are simultaneously formed on the transparent insulating substrate 1 by the series of steps explained in the first to fourth embodiments. Then, the p-electrode 4b and the n-electrode 5b connected to the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3 formed on the transparent insulating substrate 1 are cut as a pair to obtain individual optical semiconductor elements 10 to 13. The LED component in which the optical semiconductor element 10 is mounted will be described below by using the element as an example.

[0062]

FIG. 5 is a cross-sectional view of the structure of an LED component formed using optical semiconductor element 10 of the first embodiment.

This configuration illustrates a configuration in which light is externally extracted from the transparent insulating substrate 1. That is, the mounting of the optical semiconductor element 10 of the present invention is performed by the flip chip method, namely, the back surface of the transparent insulating substrate 1 is facing upward and face-down, and the p-electrode 4b and the n-electrode 5b of the optical semiconductor element 10 are fused to the lead frames 32 and 33, respectively, using solder (for example, In or PbSn) 31 for electrical connection. Then, by covering the entire optical semiconductor element 10 and molding such from a lens-shaped resin 34, the structure illustrated in FIG. 5 can be obtained.

[0063]

By configuring as such, light emitted from the active layer can be extracted more effectively. In particular, the p-electrode 4b and the n-electrode 5b are composed of the same material, and thus uniform reflection characteristics can be obtained, resulting in an LED component having excellent light distribution.

[0064]

Furthermore, regardless of the configuration of the LED component described above, although not illustrated in the drawings, it is of course also possible to fix the optical semiconductor element 10 face-up with the nitride semiconductor layers 2 and 3 formed on the transparent insulating substrate 1 facing up, and to electrically connect the p-electrode 4b and the n-electrode 5b to each of the lead frames 32 and 33 by wires.

[0065]

Furthermore, it goes without saying that optical semiconductor elements 11 to 13 formed according to other embodiments can be applied to the LED component having the above configuration.

[0066]

[Effect of Invention]

As described above, according to the present invention, a pair of positive and negative connection electrodes can be easily formed by a single immersion in an electroless plating solution. Therefore, there is no need for a large-scale film forming apparatus such as a vacuum deposition apparatus or a sputtering apparatus for forming electrodes as in the conventional technology.

Also, metal is deposited in an electroless plating bath only on the portions where the connection electrodes are to be formed, and thus waste of material is minimized, and manufacturing costs can be kept to a minimum. Additionally, there is no occurrence of electrode defects due to peeling of the connection electrode portion, which is unique to the lift-off method, and the productivity of optical semiconductor elements is improved.

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[0067]

Furthermore, in the optical semiconductor element according to the second embodiment, a plating growth film is formed only on the surface of one of the nitride semiconductor layers, and connection electrodes can be formed simultaneously on the upper layers of both nitride semiconductor layers in a single electroless plating process, and thus in addition to the effects of the optical semiconductor element of the first embodiment, it is possible to obtain the unique effect of the present invention of further simplifying the process.

[0068]

Moreover, in the optical semiconductor element according to the third embodiment, the surface of the nitride semiconductor layer other than the portion where the plating growth film is formed is also covered with the connection electrode, so that a voltage can be efficiently applied to the nitride semiconductor layer, which is the active layer, and stronger light emission can be expected as compared to the other embodiments.

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[0069]

What is more, in the optical semiconductor element according to the fourth embodiment, the connection electrodes are formed to a thickness sufficient to function as a barrier metal, and protruding electrodes composed of solder or the like are provided on the upper layer, and thus the height of the electrodes formed on the optical semiconductor element can be increased. Therefore, in this embodiment, the configuration is effective when such an application is required.

[0070]

The connection electrodes of the optical semiconductor element of the present invention are formed by electroless plating, and thus the composition of the electrode material is stable, and the reliability of an optical semiconductor device incorporating this optical semiconductor element is improved significantly over conventional optical semiconductor devices.

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[Brief Description of Drawings]

[FIG. 1] A cross-sectional view for describing the structure and manufacturing method of the optical semiconductor element in the first embodiment of the present invention.

[FIG. 2] A cross-sectional view for describing the structure and manufacturing method of the optical semiconductor element in the second embodiment of the present invention.

[FIG. 3] A cross-sectional view for describing the structure and manufacturing method of the optical semiconductor element in the third embodiment of the present invention.

[FIG. 4] A cross-sectional view for describing the structure of the optical semiconductor element in the fourth embodiment of the present invention.

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[FIG. 5] A structural cross-sectional view illustrating an LED component in which the optical semiconductor element of the present invention is flip chip mounted.

[FIG. 6] A cross-sectional view for describing the structure and manufacturing method of the optical semiconductor element in conventional art.

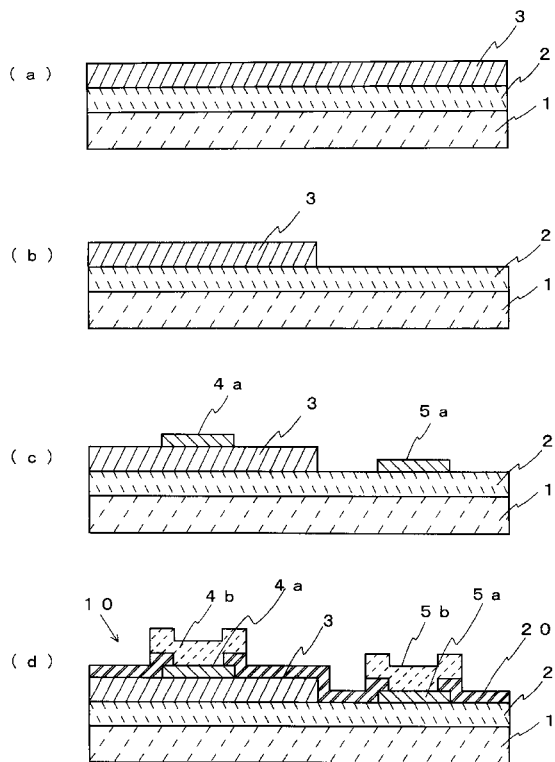
[Description of Reference Numerals]

- 1, 101 Transparent insulating substrate
- 2, 102 n-type nitride semiconductor layer
- 3, 103 p-type nitride semiconductor layer
- 4a, 5a Plating growth film
- 4b, 104 p-electrode
- 5b, 105 n-electrode
- 6 Protruding electrode
- 10 to 13, 111 Optical semiconductor elements
- 20 Protective film

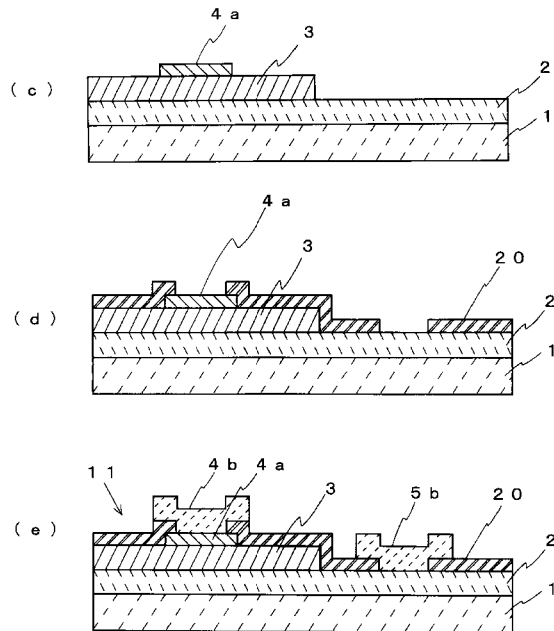
50

21 Separating partition wall
 31 Solder
 32, 33 Lead frame
 34 Resin
 121 Mask pattern
 122, 123 Metal film

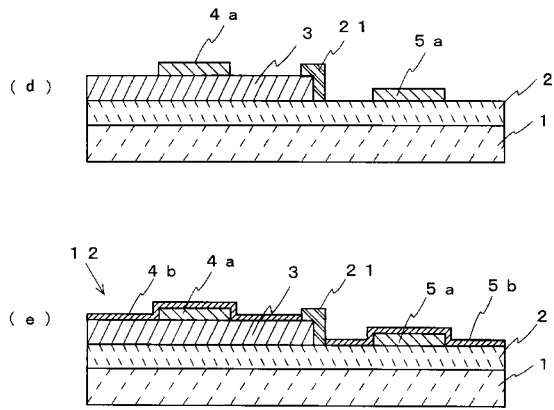
[FIG. 1]



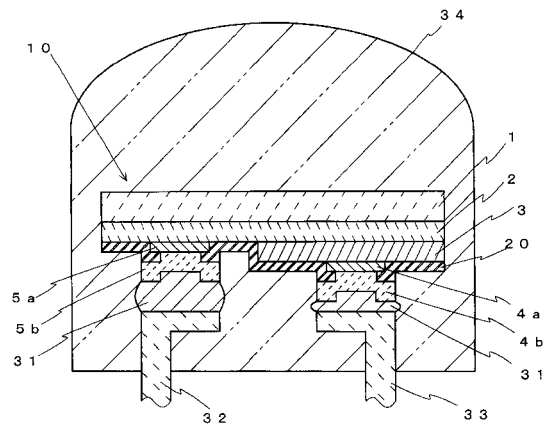
[FIG. 2]



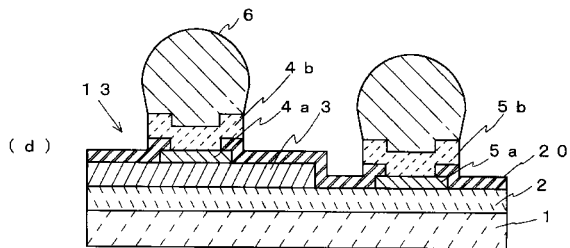
[FIG. 3]



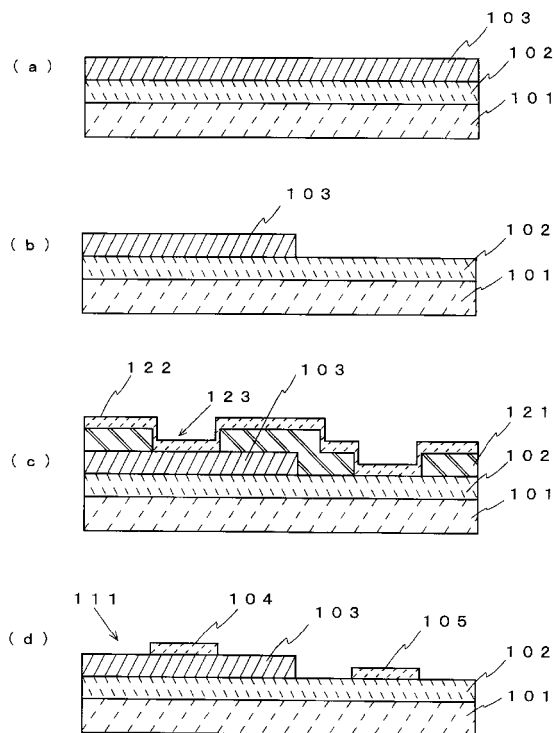
[FIG. 5]



[FIG. 4]



[FIG. 6]



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H01L 21/288	H01L 21/28 301B	
	H01L 21/288 E	



May 22, 2024

Certification

Welocalize Translations

TRANSLATOR'S DECLARATION:

I, Eric Vance, hereby declare:

1. I personally prepared the attached translation, from Japanese into English, of Japanese Patent Publication No. JP2004103975A.
2. The attached translation is, to the best of my knowledge and ability, a true, full, and accurate translation of the attached Japanese document.
3. I am competent to perform this translation, because I have advanced knowledge of the Japanese and English languages as a professional Japanese-to-English patent translator.
4. All statements made of my own knowledge are true.
5. All statements made on information and belief are believed to be true.
6. I declare under the penalty of perjury under the laws of the United States that the foregoing is true and correct.
7. I further declare that I am aware that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

A handwritten signature in black ink, appearing to read "Eric Vance", is written over a horizontal line.

Eric Vance

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