

**UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE
THE PATENT TRIAL AND APPEAL BOARD**

IKEA Supply AG

Petitioner

v.

Everlight Electronics Co., Ltd.,

Patent Owner

Patent No. 7,554,126 to Higashi *et al.* IPR Case No.: IPR2024-00988

**PETITION FOR *INTER PARTES* REVIEW OF
CLAIMS 1-2 & 4-13 OF U.S. PATENT No. 7,554,126
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§42.100 *ET SEQ.***

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Mandatory Notices Under 37 C.F.R. §42.8(a)(1) for <i>Inter Partes</i> Review	1
A.	Real Party in Interest Under 37 C.F.R. § 42.8(b)(1)	1
B.	Related Matters Under 37 C.F.R. §42.8(b)(2)	2
C.	Lead and Backup Counsel Under 37 C.F.R. §42.8(b)(3) and Service Information under 37 C.F.R. §42.8(b)(4)	3
III.	Payment of Fees Under 37 C.F.R. §42.15.....	4
IV.	Certification of Word Count under 37 C.F.R. § 42.24(D).....	4
V.	IPR Requirements Under 37 C.F.R. §42.104.....	4
A.	Grounds for Standing Under 37 C.F.R. §42.104(a).....	4
B.	Identification of Challenge Under 37 C.F.R. §42.104(b) and Relief Requested	4
VI.	Overview of the '126 Patent.....	7
A.	The Challenged Claims.....	7
B.	Priority and Effective Filing Date	7
C.	The '126 Patent's Description of the Alleged Problem in the Art.....	7
D.	The '126 Patent's Description of the Alleged Invention	9
E.	The '126 Patent Claims	16
F.	Prosecution History	18
VII.	Person of Ordinary Skill in the art ("POSITA")	19
VIII.	Overview of the Prior Art.....	19
A.	Terashima	20

B.	Sugimoto.....	22
C.	Shin.....	25
D.	The Thin Film Art	28
E.	Shelton.....	31
IX.	No Basis Exists for Discretionary Denial Under §§ 314(a) and 325(d).....	31
X.	Claim Construction	34
XI.	Specific Grounds for Petition	35
A.	Ground 1: Anticipation of Claims 1, 2, 5-8, & 9-12 by Terashima.....	37
1.	Terashima Anticipates Claim 1.....	37
2.	Terashima Anticipates Claim 2.....	45
3.	Terashima Anticipates Claim 5.....	50
4.	Terashima Anticipates Claim 6.....	51
5.	Terashima Anticipates Claim 7.....	52
6.	Terashima Anticipates Claim 8.....	53
7.	Terashima Anticipates Claims 9 & 10.....	53
8.	Terashima Anticipates Claim 11.....	53
9.	Terashima Anticipates Claim 12.....	54
B.	Ground 2: Sugimoto Anticipates Claims 1, 6, 9, & 12	54
1.	Sugimoto Anticipates Claim 1	54
2.	Sugimoto Anticipates Claim 5	63
3.	Sugimoto Anticipates Claim 6.....	64
4.	Sugimoto Anticipates Claim 9.....	65

5. Sugimoto Anticipates Claim 12	65
C. Ground 3: Obvious Over Shin in view of any of the Thin Film Art.....	65
1. Shin Plus the Thin Film Art Renders Claim 1 Obvious	66
2. Shin Plus One or more of the Thin Film Art Renders Claim 2 Obvious.....	81
3. Shin and the Thin Film Art Renders Claim 5 Obvious.....	83
4. Shin Plus the Thin Film Art Renders Claim 7 Obvious	85
5. Shin Plus the Thin Film Art Renders Claims 9 & 10 Obvious.....	86
D. Ground 4: Claim 4 is Obvious over Terashima or Ground 3 in view of Shelton.....	87
E. Ground 5: Claims 5 is Obvious over Terashima in view of Shin, Sugimoto, Inoue, and/or the OLSA	89
F. Ground 6: Claims 6 is Obvious over Terashima, Sugimoto, or Ground 3 in view of Shelton and/or the OLSA.....	90
G. Ground 7: Claim 7 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA.....	91
H. Ground 8: Claim 8 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA.....	92
I. Ground 9: Claim 11 is Obvious over Ground 3 or Sugimoto in view of Terashima and/or the OLSA	92
J. Ground 10: Claim 12 is Obvious over Ground 3 in view of Terashima, Sugimoto, and/or the OLSA.....	93
K. Ground 11: Claim 13 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA.....	93
L. Ground 12: Any of Grounds 1, 4-8, and 11 with respect to Terashima in view of the Thin Film Art	94
XII. Secondary Considerations	94

XIII. Conclusion	94
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TABLE OF AUTHORITIES

Cases

<i>Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH,</i> IPR2019-01469 (PTAB. Feb. 13, 2020).....	34
<i>Apple Inc. v. Fintiv, Inc.,</i> IPR2020-00019 (PTAB March 20, 2020)	34
<i>General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha,</i> IPR2016-01357 (PTAB Sept. 6, 2017)	32
<i>Medtronic, Inc. v. Barry,</i> 891 F.3d 1368 (Fed. Cir. 2018)	7
<i>PowerOasis, Inc. v. T-Mobile USA, Inc.,</i> 522 F.3d 1299 (Fed. Cir. 2008).....	7
<i>Sony Interactive Entertainment LLC v. Bot M8, LLC, IPR2020-00726,</i> (PTAB Oct. 6, 2020).....	34
<i>Tokai Corp. v. Easton Enters., Inc.,</i> 632 F.3d 1358 (Fed. Cir. 2011)	94
<i>Vibrant Media Corp. v. General Electric Co.,</i> IPR2013-00172 (PTAB July 29, 2013).....	47

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 7,554,126 (“’126 patent”)
1002	File history of U.S. Patent No. 7,554,126 (“’126 FH”)
1003	Declaration of Michael Lebby Regarding Invalidity of U.S. Patent No. 7,554,126
1004	Japanese Published Unexamined Patent Application JP2004-103975 (“Terashima”)
1005	U.S. Application Publication No. 2004/0256631 (“Shin”)
1006	U.S. Application Publication No. US 2004/0159836 (“Sugimoto”)
1007	U.S. Application Publication No. US 2003/0160259 (“Uemura ’259”)
1008	U.S. Application Publication No. US 2004/0149999 (“Uemura ’999”)
1009	English translation of the International Preliminary Report on Patentability issued by the International Bureau for International Patent Application No. PCT/JP2005/017467
1010	Certified Translation of Ex-1004, Japanese Published Unexamined Patent Application JP2004-103975 (“Terashima”)
1011	U.S. Application Publication No. 2005/0194605 (“Shelton”)
1012	Preliminary Opinion in German Nullity Proceeding for EP2947705
1013	English Translation of Preliminary Opinion in German Nullity Proceeding for EP2947705
1014	Scheduling Order issued in <i>Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al.</i> , N 6:23-cv-00481-AM-DTG (W.D. Tx. Jul. 5, 2023).

Exhibit	Description
1015	Claims Construction Order issued in <i>Everlight Electronic Co., Ltd. v. Walmart Inc.</i> , No. 23-cv-000439-AM-DTG (W.D. Tx. Jun. 9, 2023).
1016	Patent Owner’s Infringement Contentions – Claim Chart of the ’126 Patent to IKEA Rollsbo LED BULB E26 140 lumen in <i>Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al.</i> , No. 6:23-cv-00481-AM-DTG (W.D. Tx. Jul. 5, 2023).
1017	U.S. Patent No. 6,989,598 (Ex-1017) (“Song”)
1018	Curriculum Vitae of Dr. Michael S. Lebby
1019	Attorney Declaration of Joseph R. Klinicki
1020	U.S. Patent No. 7,154,125 (“Koide”)
1021	U.S. Patent No. 6,333,522 (“Inoue”).
1022	Joint Motion to Amend Claim Construction Deadlines filed in <i>Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al.</i> , No. 6:23-cv-00481-AM-DTG (W.D. Tx. Jul. 5, 2023)

I. Introduction

IKEA Supply AG (collectively “Petitioner” or “ISAG”) hereby petitions for *inter partes* review of Claims 1-2 & 4-13 (“Challenged Claims”) of U.S. Patent No. 7,554,126 (Ex-1001). The Challenged Claims should be canceled because they do not claim anything new or inventive; they claim a previously known light emitting diode (LED) configuration.

II. Mandatory Notices Under 37 C.F.R. §42.8(a)(1) for *Inter Partes* Review

A. Real Party in Interest Under 37 C.F.R. § 42.8(b)(1)

A real-party-in-interest in this petition is ISAG. ISAG is a subsidiary of Inter IKEA Holding BV (“Inter IKEA”), which has a place of business at Olof Palmestraat 1, Delft, Zuid-Holland, 2616. IKEA US Retail LLC and IKEA North America Services, LLC, of Conshohocken, Pennsylvania, are real-parties-in-interest as they are currently named as Defendants in the district court proceeding identified in §II(b), *infra*, and related through contracts and/or related company’s contracts by franchise agreements and/or indemnification agreements with Inter IKEA and/or ISAG. OSRAM Opto Semiconductors Gmbh, of Regensburg, Germany, Samsung Electronics Co., Ltd., of Suwon-si, South Korea, Seoul Semiconductor Co., Ltd, of Ansan-si, South Korea, Philips Lumileds Lighting LLC, of San Jose, California, Bridgelux, Inc. of Fremont, California, Shenzhen Smalite Semiconductor Co., Ltd., of Shenzhen, China, and/or Intematix, Inc., of Fremont, California, may be real-

parties-in-interest insofar as they supply components to ISAG that Patent Owner has accused of infringement and have certain contractual and/or indemnification obligations to ISAG in relation to those accused products.

B. Related Matters Under 37 C.F.R. §42.8(b)(2)

This petition is related to three complaints filed by Patent Owner involving the '126 patent:

1) *Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al*, No. 2:23-cv-00126-JRG) (E.D. Tex.), complaint served June 1, 2023, and subsequently voluntarily dismissed on July 5, 2023;

2) *Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al*, No. 6:23-cv-00481-AM) (W.D. Tex.), complaint served July 6, 2023, which is pending (“IKEA-Everlight Litigation”).

3) *Everlight Electronics Co., Ltd. v. Walmart Inc.*, No. 6:23-cv-00439-AM-DTG) (W.D. Tex.), which is pending (“Walmart-Everlight Litigation”).

In the IKEA-Everlight litigation, Everlight asserts the '126 patent, U.S. Patent Nos. 9,640,733 (“’733 patent”), and 9,905,742 (“’742 patent”). ISAG’s has challenged the '733 patent in IPR2024-00972 and the '742 patent in IPR2024-00987. Everlight asserted EP2947705, a foreign counterpart to the '733 patent, against IKEA Deutschland GmbH & Co. KG and IKEA of Sweden AB in Germany in the District Court of Dusseldorf Civil Chamber. That case is pending. Two nullity proceedings

have been filed against EP2947705 with the German Federal Patent Court by SLV GmbH (2 Ni 16/23 (EP)) and IKEA Deutschland GmbH & Co. KG (2 Ni 1/24 (EP)).

A copy of the initial preliminary opinion finding that the claims of EP2947705 likely lack novelty and/or inventive step is attached as Ex-1012 (Ex-1013, English machine translation of Ex-1012).

The undersigned is unaware of any other pending judicial or administrative matters that would affect, or be affected by, a decision in this proceeding.

C. Lead and Backup Counsel Under 37 C.F.R. §42.8(b)(3) and Service Information under 37 C.F.R. §42.8(b)(4)

Petitioner designates the following lead and backup counsel:

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Service on Petitioner may be made by mail or hand delivery to: Flaster Greenberg P.C., 1717 Arch Street, Suite 3300, Philadelphia, PA 19103. Petitioner also consents to and prefers electronic service by emailing IKEA-Everlight-IPRs@flastergreenberg.com and counsel of record (shown above).

III. Payment of Fees Under 37 C.F.R. §42.15

Petitioner submits that the fee set forth in 37 C.F.R. §42.15(a) was properly paid using the USPTO Financial Manager.

IV. Certification of Word Count under 37 C.F.R. § 42.24(D)

Petitioner certifies that the word count in this Petition is 13,608 words, as counted by the word-processing program (Microsoft Word for Office 365) used to generate this Petition, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, table of exhibits, and this certificate of word count. This Petition is in compliance with the 14,000-word limit set forth in 37 C.F.R. §42.24(a)(1)(i).

V. IPR Requirements Under 37 C.F.R. §42.104

A. Grounds for Standing Under 37 C.F.R. §42.104(a)

Petitioner certifies that the '126 patent is available for *inter partes* review on the grounds identified in this petition. Petitioner is not barred or estopped from requesting *inter partes* review.

B. Identification of Challenge Under 37 C.F.R. §42.104(b) and Relief

Requested

Petitioner requests that the Challenged Claims be cancelled based on the following grounds:

Ground of Unpatentability	'126 Patent Claim(s)	Basis for Rejection under 35 U.S.C. §§ 102/103
Ground 1	1, 2, and 5-12	Anticipated by Terashima
Ground 2	1, 5-6, 9 and 12	Anticipated by Sugimoto
Ground 3	1, 2, 5, and 7-10	Obvious over Shin in view of one or more of the Thin Film Art (<i>i.e.</i> , Sugimoto, Terashima, Uemura '259, Uemura '999, and/or Inoue)
Ground 4	4	Obvious over Terashima or Ground 3 in view of Shelton or Inoue
Ground 5	5	Obvious over Terashima in view of Shin, Sugimoto, or Inoue

Ground 6	6	Obvious over Terashima, Sugimoto. or Ground 3 in view of Shelton and/or the ordinary level of skill in the art (“OLSA”)
Ground 7	7	Obvious over Terashima, Sugimoto. or Ground 3 in view of Shelton, and/or the OLSA
Ground 8	8	Obvious over Terashima, Sugimoto, or Ground 3 in view of Shelton and/or the OLSA
Ground 9	11	Obvious over Sugimoto or Ground 3 in view of Terashima or the OLSA
Ground 10	12	Obvious over Ground 3 in view of Terashima, Sugimoto, or the OLSA
Ground 11	13	Obvious over either Terashima, Sugimoto, or Ground 3 in view of Shelton and/or the OLSA
Ground 12	1, 2, and 4-13	Obvious over Grounds 1, 4-8, and 11 regarding Terashima in view of Sugimoto, Uemura ’259, Uemura ’999 and/or the OLSA

VI. Overview of the '126 Patent

A. The Challenged Claims

The Challenged Claims generally relate to an LED, LED attachment to generic circuit boards, and methods of manufacturing/mounting the same. Claims 1-2 and 4-13 are the Challenged Claims. Claims 1 and 2 are independent device claims. Claims 9 and 10 are independent methods of manufacturing claims that correspond to claims 1 and 2, respectively. Claim 4-8 and 11-13 are dependent claims.

B. Priority and Effective Filing Date

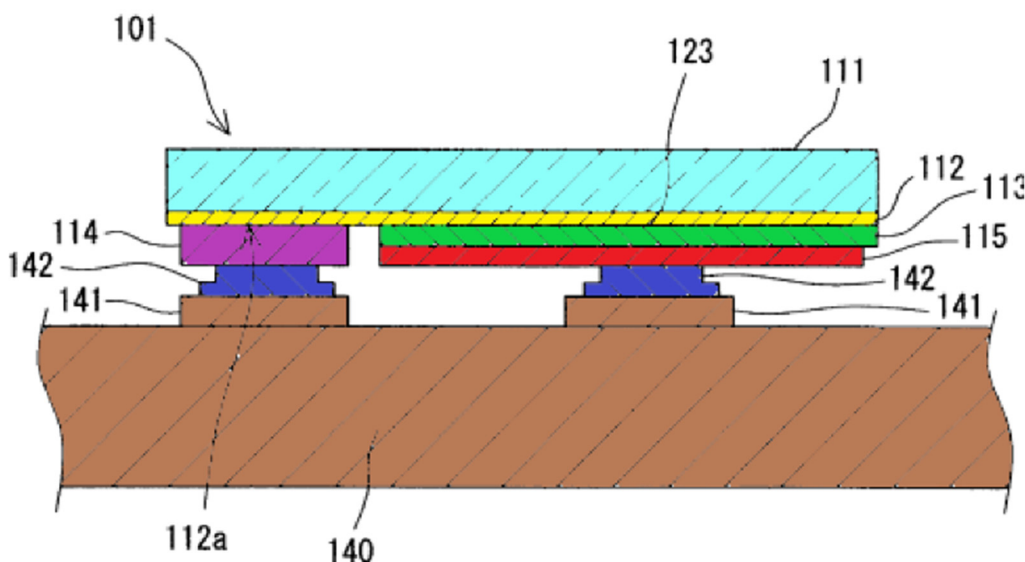
The '126 patent claims the benefit of Japanese Patent Application No. JP2004279049, filed on September 27, 2004, and PCT/JP2005/017467, filed on September 22, 2005 (Ex-1001 at Cover Page). Petitioner applies September 27, 2004 as the effective filing date here, without conceding that the '126 patent is entitled to it. *See PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1303-06 (Fed. Cir. 2008). As the effective filing date of the '126 patent is before March 16, 2013, pre-AIA 35 U.S.C. §§ 102 & 103 apply. *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1375 (Fed. Cir. 2018).

C. The '126 Patent's Description of the Alleged Problem in the Art

The alleged problem can be understood with reference to the "Issue to be Improved by the Invention" and FIGs. 16 and 17 (Ex-1001 at 1:24-2:49). The '126

patent describes a “typically conventional structure” in FIGs. 16-17 (Ex-1001 at 1:26-28). FIG. 16 illustrates an LED chip 101 having a “light-transmitting substrate 111,” (blue) an n-type semiconductor layer 112 (yellow) formed on the substrate 111, and a p-type semiconductor layer 113 (green) formed so as to cover part of the n-type semiconductor layer 112 (Ex-1001 at 1:32-37). An n-electrode 114 (purple) is formed on the n-type semiconductor layer 112 (yellow) (Ex-1001 at 1:36-37). A p-electrode 115 (red) is formed on the p-type semiconductor layer 113 (Ex-1001 at 1:41-42). LED 100 is connected to a circuit board 140 with bumps (e.g., indigo) 142 that connect the n-electrode 114 and the p-electrode 115 to corresponding circuit board (e.g., printed circuit board or “PCB”) electrodes 141 (brown).

'126 Patent FIG. 16 (Annotated)



The '126 patent explains that mounting a chip on a circuit board is usually

carried out at low costs by using a conductive bonding material (*e.g.*, solder or silver paste) (Ex-1001 at 2:12-16). According to the '126 patent, the p-type semiconductor layer needs to be large to maximize the light-emitting area (Ex-1001 at 2:22-24). Because an LED emits light from the p-type semiconductor material and the junction between the LED and circuit board n-electrodes can block light from being emitted, the n-chip/circuit board junction should be small (Ex-1001 at 2:17-21; 2:24-26). The '126 patent further states that it may be difficult to use a conductive bonding material (*e.g.*, solder and bumps) to join a relatively small n-electrode 114 area to a large circuit board joining area (Ex-1001 at 2:27-40). Against this backdrop, the '126 patent states that its “main objective is to provide a semiconductor light-emitting element which can be mounted on a circuit board by using a conductive bonding material, typically represented by solder, at low costs” (Ex-1001 at 2:41-45).

D. The '126 Patent's Description of the Alleged Invention

The '126 patent describes a light emitting device that is similar to the conventional LED described above but has a second n-electrode, a second p-electrode, and an insulating layer. The '126 patent illustrates a first embodiment of “the invention” in FIGs. 1-2 (Ex-1001 at 6:61-64). FIG. 2 is a bottom view of a light emitting device taken without the solder and the circuit board as shown by the annotated arrows added in FIG. 1 (Ex-1001 at 6:6-7). FIG. 1 is a cross-section taken along the lines A-A in FIG. 2, so that the n and p electrodes can be seen in the same

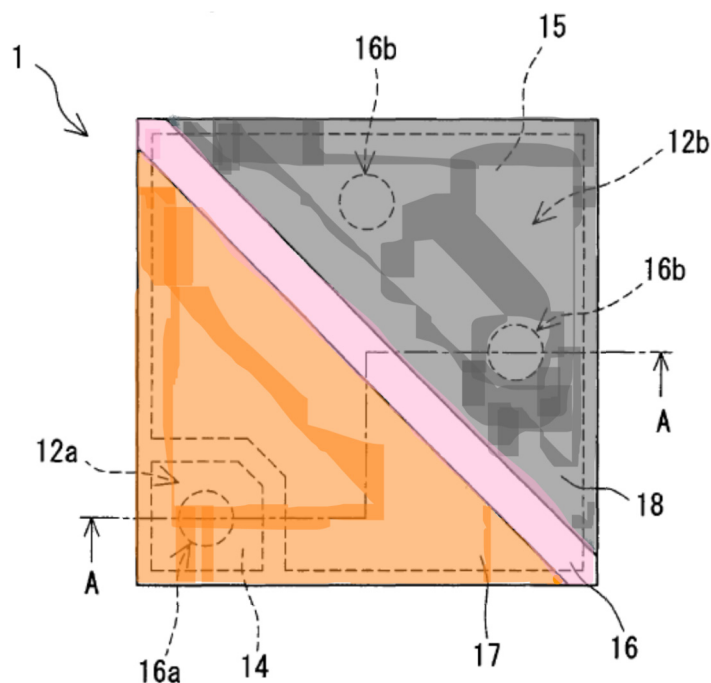
cross section (Ex-1001 at 6:3-7; 6:67-7-1).

Similar to the described conventional LED, the '126 patent describes a light emitting device having a light emitting substrate 11 (*e.g.*, sapphire) (blue), an n-semiconductor layer 12 (yellow), a p-semiconductor layer 13 (green), a first n-electrode 12a (purple), and a first p-electrode 15 (red) (Ex-1001 at 7:7-15; 7:25-31). The first electrodes are described as thin film electrodes (Ex-1001 at 7:32; 7:41).

The '126 patent discloses a first insulating layer 16 (pink) that insulates the first n-electrode (purple) and the first p-electrodes (red) from each other (Ex-1001 at 7:16-20). The '126 patent describes a second n-electrode 17 (orange) and a second p-electrode 18 (gray) (Ex-1001 at 7:19-24). The second n-electrode 17 (orange) is “formed on the first insulating layer 16” (pink) and “penetrates the first insulating layer 14 to be electrically connected to the first n-electrode 14” (purple) (Ex-1001 at 7:21-23). The second p-electrode 18 (gray) is electrically connected to the first p-electrode (red) (Ex-1001 at 7:23-24). The second electrodes are referred to as “thin films” (Ex-1001 at 7:65-8:1). As shown by the solid lines in FIG. 2, the second n-electrode 17 (orange) and the second p-electrode (gray) are shown to be “isosceles triangles that have virtually the same size,” (Ex-1001 at 9:5-12). However, the '126 patent states that different electrode sizes (areas) can be used (Ex-1001 at 9:16-17). The '126 patent states that the second electrodes can be bonded to electrodes 41 of a

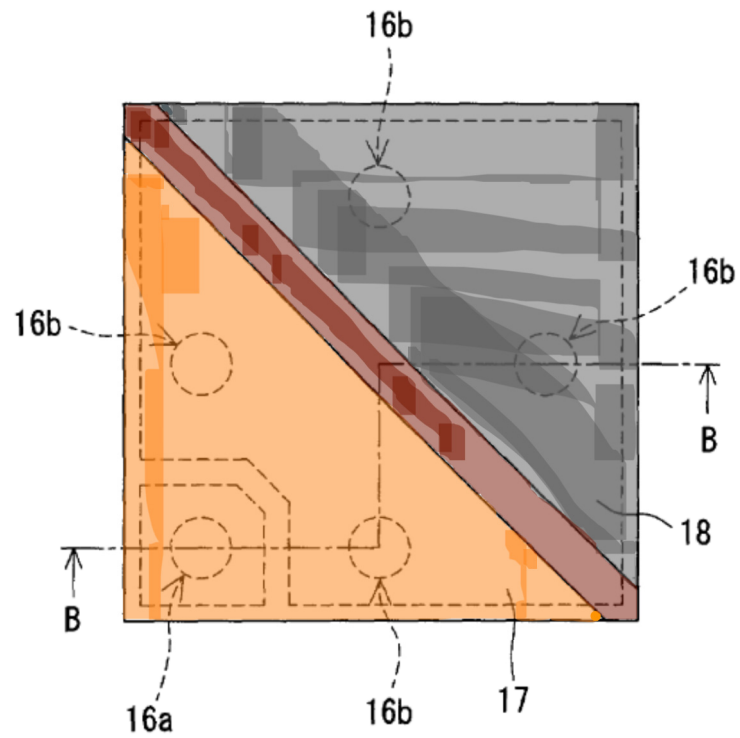
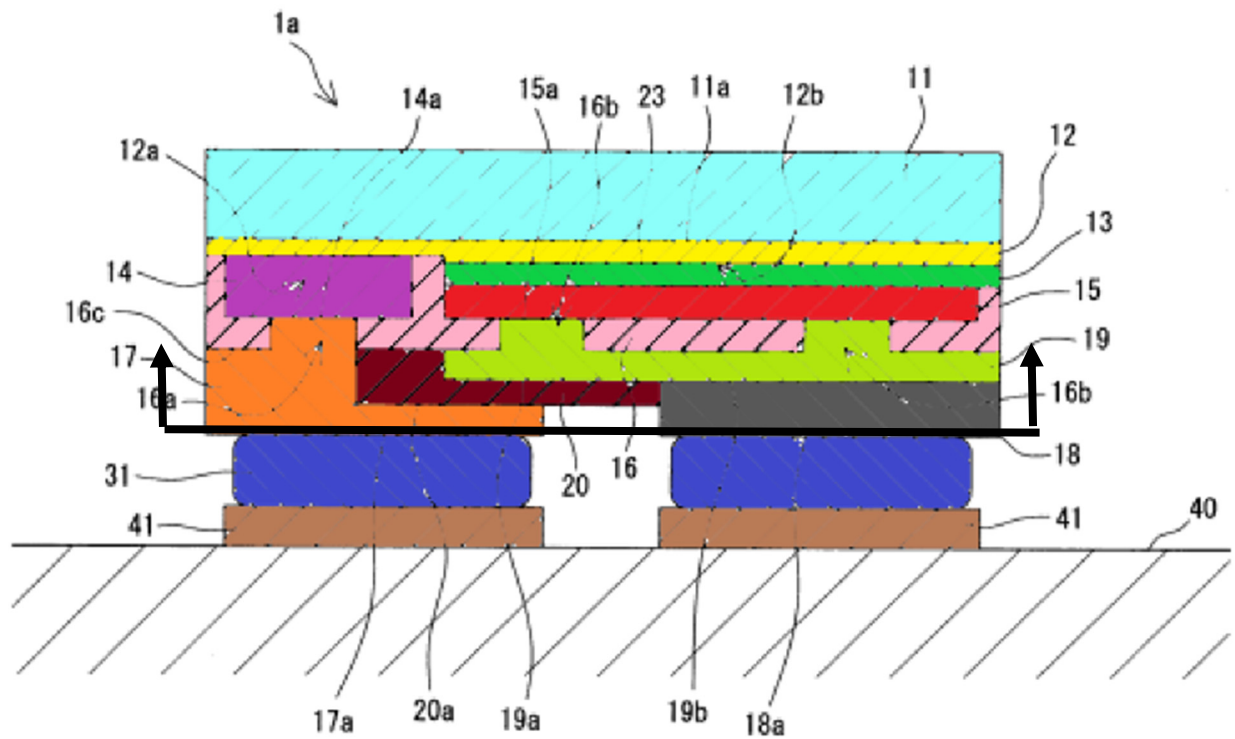
'126 Patent FIGs. 1 & 2 (Annotated)





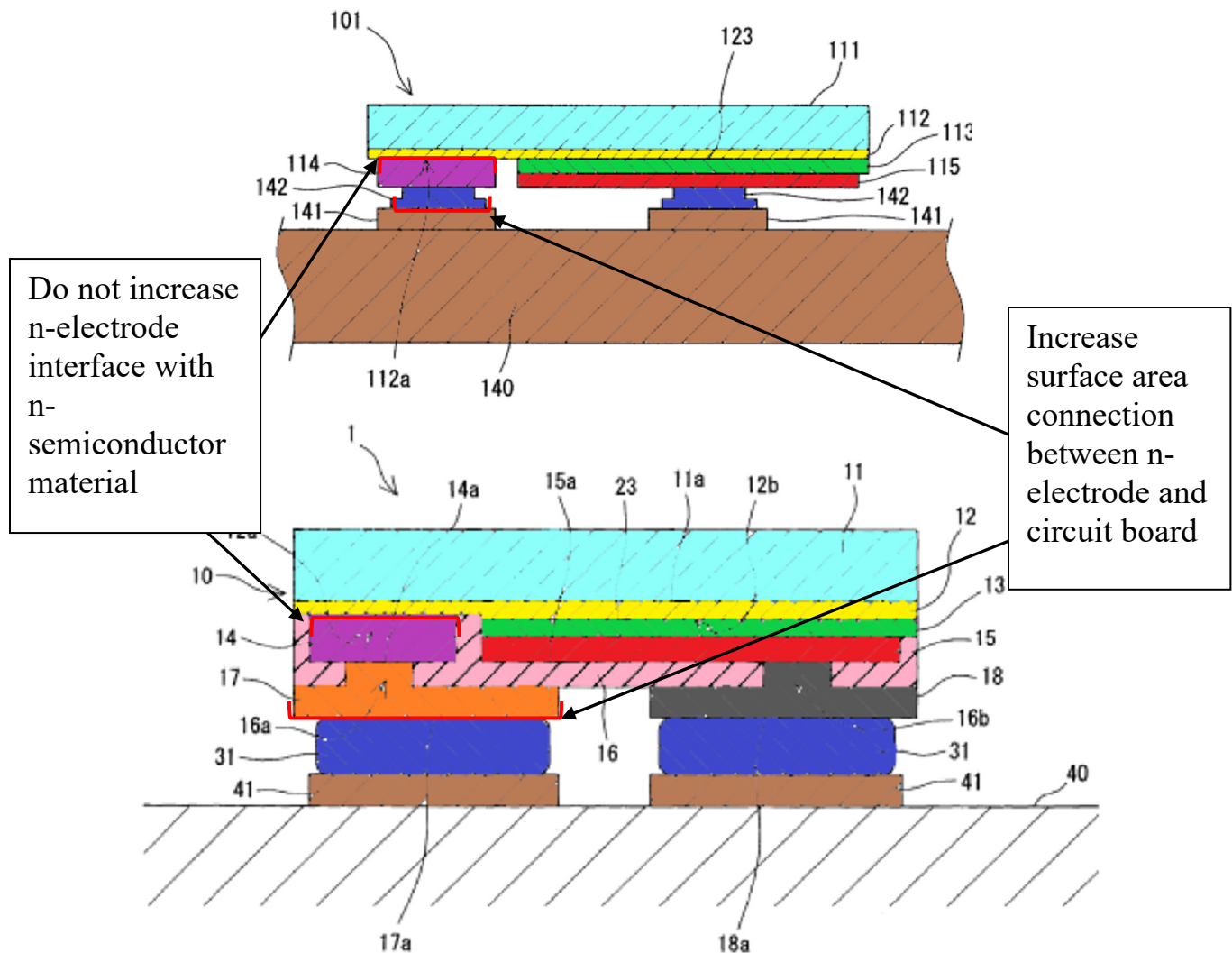
The '126 patent describes a second embodiment in FIGs. 9 and 10 (Ex-1001 at 6:25-29; 11:26-49). The second embodiment adds a conductive layer 19 (lime) and a second insulating layer 20 (dark red) to the first embodiment (Ex-1001 at 11:43-49). The conductive layer 19 is formed on the first insulating layer 16 and is electrically connected to the first and second p-electrodes 15, 18 (Ex-1001 at 11:49-56). The second insulating layer 20 insulates the second n-electrode 17 from the conductive layer 19 (Ex-1001 at 11:60-64).

'126 Patent Figs. 9 & 10 Annotated



According to the '126 patent, by connecting the LED to a circuit board 40 with a second n-electrode, the joining strength and heat dissipation is increased (Ex-1001 at 10:63-11:3). The described structure seemed to be aimed at simply strengthening the mechanical and thermal connection between the n-electrode and a circuit board without increasing the area that the n-electrode covers the n-semiconductor layer, so that the interface between the n-semiconductor layer and the p-semiconductor layer can be maximized, thereby maximizing the light generating junction between the n-semiconductor layer and the p-semiconductor layer. This is understood by comparing FIG. 1's embodiment with FIG. 16's conventional LED where the red lines show the increased surface area for the second n-electrode/circuit board connection.

Comparison of Conventional LED of FIG. 16 and FIG. 1 Embodiment



All the '126 patent did to solve its alleged problem was to increase the n-electrode surface area that is in contact with the circuit board (*i.e.*, by attaching a second n-electrode with more surface area than the n-electrode/n semiconductor layer interface). The goal of creating a stronger connection was simply and

straightforwardly (allegedly) solved by providing more surface area.

E. The '126 Patent Claims

In view of this disclosure, claims 1 (device claim) and 9 (manufacturing method claim) are directed to the first embodiment. Claim 1 is provided below with a reference identifier for each limitation.

Reference	Claim Limitation
Preamble	1. A semiconductor light-emitting element comprising:
substrate	a light-transmitting element substrate;
n-type layer	an n-type semiconductor layer formed on the element substrate so as to cover the element substrate;
p-type layer	a p-type semiconductor layer formed so as to cover an area on the n-type semiconductor layer from which an area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer;
first n-electrode	a first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer;
first p-electrode	a first p-electrode that is a thin film formed on the p-type semiconductor layer;
first insulating layer	a first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other;
second n-electrode	a second n-electrode formed on the first n-electrode and the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode, the second n-electrode being insulated from the first p-electrode by the first insulating layer; and

second p-electrode	a second p-electrode formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode.
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Claim 2 (claim 10 is a corresponding manufacturing method claim) is provided below with a reference identifier for each limitation. The first six elements of claims 2 are the same as claim 1. Claims 2 and 10 differ from claims 1 and 9 by claiming insulation layer “openings” for the claimed electrodes and the second claimed electrodes being “formed on the first insulating layer” (Ex-1001 at 14:21-14:38; 16:10-26).

Reference	Claim 2 Limitations
Preamble	2. A semiconductor light-emitting element comprising:
substrate	a light-transmitting element substrate;
n-type layer	an n-type semiconductor layer formed on the element substrate so as to cover the element substrate;
p-type layer	a p-type semiconductor layer formed so as to cover an area on the n-type semiconductor layer from which an area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer;
first n-electrode	a first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer;
first p-electrode	a first p-electrode that is a thin film formed on the p-type semiconductor layer;
first insulating layer (2)	a first insulating layer having at least one opening for the n-electrode and one opening for the p-electrode

	formed therein, which covers the first n-electrode and the first p-electrode so as to insulate the first n-electrode and the first p-electrode from each other, except for the opening for the n-electrode and the opening for the p-electrode,
second n-electrode (2)	a second n-electrode formed on the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor layer and the first n-electrode, the second n-electrode being electrically connected to the first n-electrode through the opening for the n-electrode of the first insulating layer; and
second p-electrode (2)	a second p-electrode formed on the first insulating layer as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode through the opening for the p-electrode of the first insulating layer.

Dependent claims 4-6 relate to additional device features (Ex-1001 at 14:59-15:2). Dependent claims 7-8 and 13 relate to attachment to a circuit board (Ex-1001 at 14:66-15:13; 16:34-42). Claims 11 and 12 relates to a method of manufacturing the insulation layer/electrodes (Ex-1001 at 16:27-29).

F. Prosecution History

The '126 patent claims were allowed without a single office action (Ex-1001 at "References Cited," Ex-1002). The examiner did not cite any references (Ex-1002).

VII. Person of Ordinary Skill in the art (“POSITA”)

A POSITA in the field of the ’126 patent at the time of the effective filing date would have had: (1) a Bachelor’s degree in electrical engineering, physics, or a comparable field of study, and (2) at least three years of professional experience with semiconductor optoelectronic devices that includes designing/analysis, mounting, manufacturing, and packaging (Ex-1003 at ¶ 44). This description is approximate, and a higher level of education or skill might make up for less experience, and additional experience could make up for a lower education level (Ex-1003 at ¶ 44).

VIII. Overview of the Prior Art

The ’126 patent did not invent increasing the surface area of the junction between the n-electrode and a circuit board. The ’126 patent did not invent second n- and p-electrodes or insulating layers. The ’126 patent did not invent increasing the surface area connection for an n-electrode by attaching a second n-electrode, with a larger surface area, to a first n-electrode that has a smaller joined face between the first n-electrode and n-semiconductor layer. It was of course known that a stronger connection can be created by increasing surface area with a larger second n-electrode (Ex-1003 at §§ 8.1-8.6).

Nor did the ’126 patent invent a second p-electrode that is smaller than the junction between the n-semiconductor layer and the p-semiconductor layer (Ex-1003

at §§ 8.1-8.6). This is, of course, not surprising because the light emits from the p-semiconductor layer, so a POSITA preferred not to cover the p-semiconductor layer with a p-electrode and inhibit light extraction.

A. Terashima

Japanese Patent Publication No. 2004103975 (“Terashima”) (Ex-1004) published on April 2, 2004 (Ex.-1010 at “(43) Publication Date”). A certified translation of Terashima in accordance with 37 CFR 1.68 is attached (Ex-1010). Terashima is prior art under 35 U.S.C. § 102 (pre-AIA). Terashima was cited in an international preliminary examination report (Ex-1009) and is listed as considered by the USPTO in the ’126 patent’s list of “Foreign Patent Documents” section of the references cited (Ex-1001). However, it does not appear that an English translation of Terashima was ever provided to the USPTO (Ex-1002 at pp. 228-229, 239-253 translation as “Terajima”).

As shown in FIG. 5 below, Terashima discloses a “semiconductor light-emitting element” (Ex-1001 at ¶ [0050]) having a “transparent insulating substrate 1” (blue), an “n-type nitride semiconductor layer 2” (yellow) formed on the substrate, a “p-type nitride semiconductor layer 3” (green) formed on the n-semiconductor layer, a first “plating growth film” n-electrode 5a (purple) and a second, larger n-electrode 5b (orange), a first “plating growth film” p-electrode 4a (red) and a second, larger p-electrode 4b (grey) p-electrode, and an insulating layer in the form of

“protective film 20” (pink) (Ex-1010 at ¶¶ [0003], [0029], [0032]-[0036], [0061], Explanation of symbols)). Terashima (FIG. 5) discloses that: (i) the second n-electrode has an “area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode”; and (ii) the second p-electrode has an area that is smaller than the interface between the n-semiconductor layer and the p-semiconductor layer, as claimed in the ’126 patent (Ex-1003 at ¶ 92). Thus, the ’126 patent claims and the ’126 patent’s alleged inventive concepts are not novel (Ex-1003 at § 8.1.1).

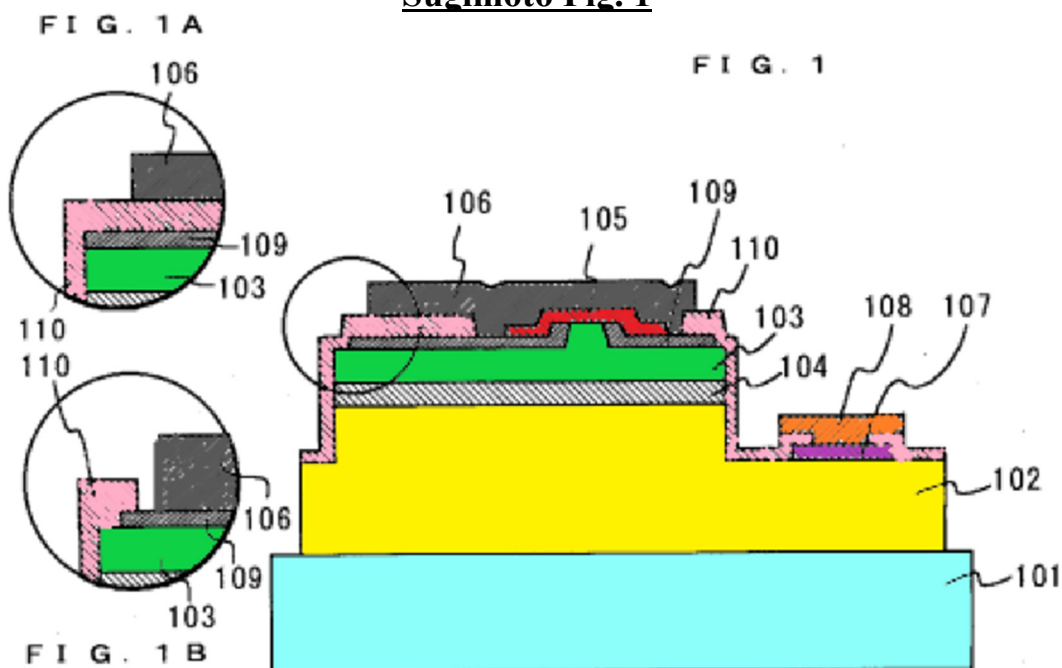
United States Patent Application Publication no. US 2004/0159836

Sugimoto discloses a light emitting device having an n-type semiconductor layer 102 (yellow) formed on a sapphire substrate 101 (blue) and a p-type

semiconductor layer 103 (green) formed on the n-type semiconductor layer 102 (yellow) with an active layer between the n and p layers (Ex-1006 at ¶ [0072], *see* [0005] “sapphire” substrate). In addition, Sugimoto discloses a first p-electrode 105 (red) connected to a second p-electrode 106 (gray) (Ex-1006 at ¶ [0073]). Sugimoto discloses a first n-electrode 107 (purple) connected to a second n-electrode 108 (orange) (Ex-1006 at ¶ [0073]). As shown in FIG. 1, Sugimoto also discloses a first and a second insulation layer 109, 110 that insulate the electrodes (Ex-1006 at ¶¶ [0073], [0075]).

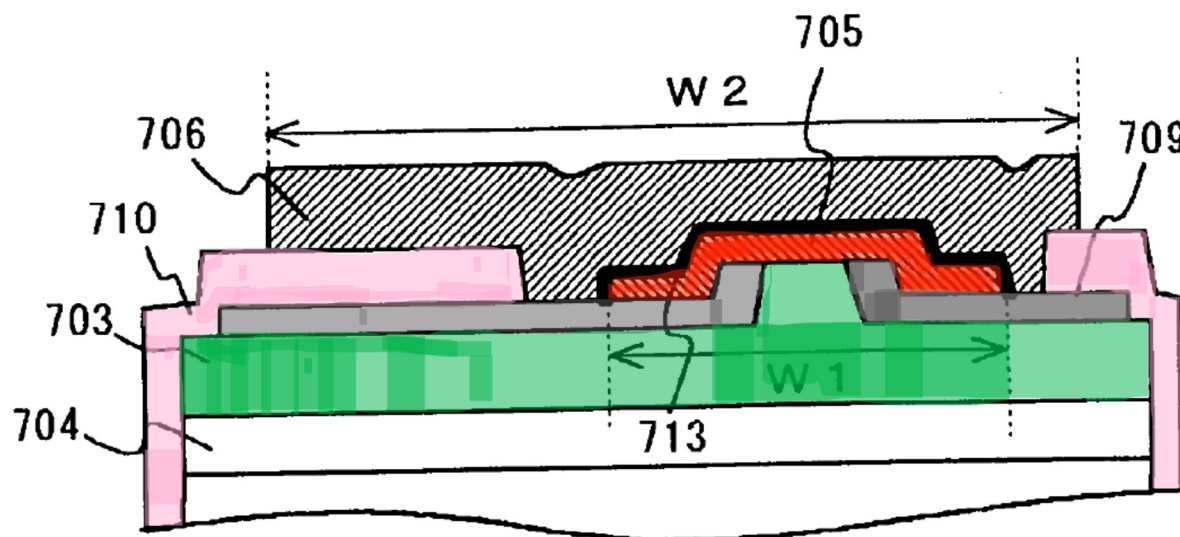
Sugimoto’s second n-electrode 108 has an area larger than a joined face between the n-type semiconductor (102) and the first n-electrode (107), so that the second n-electrode is electrically connected to the first n-electrode (Ex-1006 at ¶ [0073]; Ex-1003 at § 8.1.2). Also, as shown in Fig. 5, Sugimoto’s second p-electrode 106 has an area smaller than a joined face between the n-type semiconductor layer (102) and the p-type semiconductor layer (103) (Ex-1006 at Fig. 1; Ex-1003 at § 8.1.2).

Sugimoto Fig. 1



Sugimoto further expressly teaches what the '126 patent claim to have invented regarding the relationship between the n-electrode sizes (Ex-1003 at ¶ 96). Sugimoto states that preferably “the width W2 of the second electrode 706 is larger than the width W1 of the first electrode 705 (Ex-1006 at ¶¶ [0058]-[0059]).

Sugimoto Fig. 7A



C. Shin

U.S. Publication No. 2004/0256631 (“Shin”) published on December 23, 2004 from an application filed on November 6, 2003 (Ex-1005 at Cover). Shin is prior art to the ’126 patent under 35 U.S.C. 102(e) (pre-AIA). Shin’s FIG. 5 illustrates a top view and a cross-section taken along line B-B (Ex-1005 at ¶ [0060]). Shin discloses a flip-chip light emitting element (Ex-1005 at ¶¶ [0002], [0019], [0038]). Shin describes that the light emitting element has a sapphire substrate 41 (blue), a n-semiconductor layer 43a/42 (yellow) formed on the substrate using a buffer layer 42, a p-semiconductor layer 43c (green) formed on

the n-semiconductor layer with an exposed area for a first n-electrode 46a (purple) on the n-semiconductor layer (Ex-1005 at ¶¶ [0040], [0044]; Ex-1003 at § 8.1.3).

A first p-electrode 45a (red) is formed on the p-semiconductor layer 43c (Ex-1005 at ¶ [0044]). Shin discloses a “passivation” or the claimed insulation layer 47 (Ex-1005 at ¶¶ [0048]-[0050]; Ex-1003 at ¶ 98).

Shin FIG. 5 (Annotated)

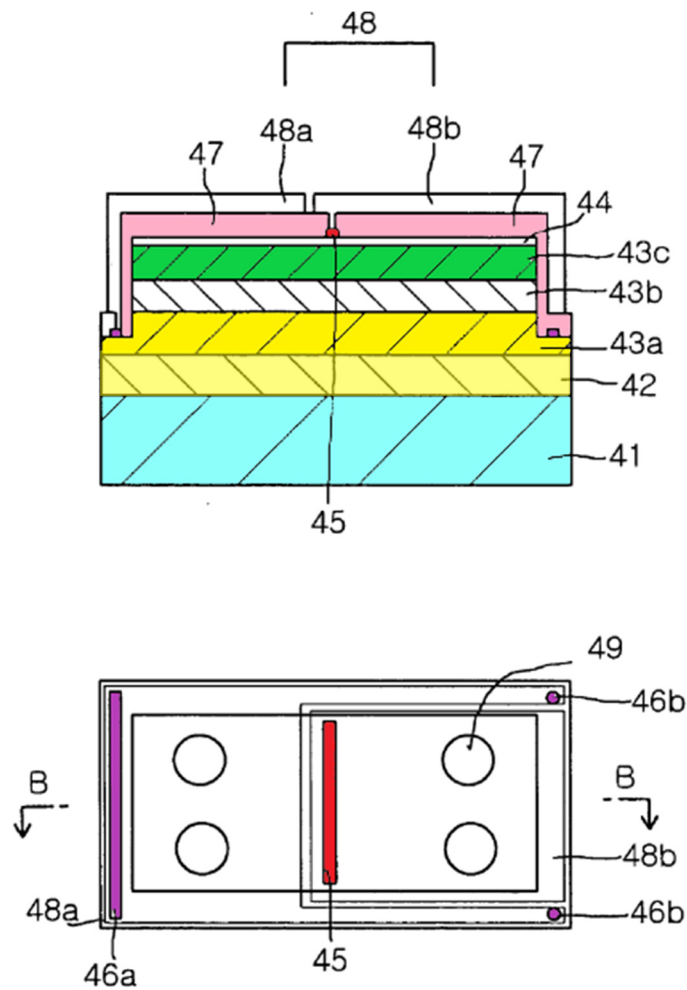


FIG. 5

FIG. 4E illustrates a top and cross-section views of the LED (Ex-1005 at ¶¶ [0034], [0050]). Shin also discloses a second n-electrode 48a (orange) and a second p-electrode 48b (grey) formed on the insulation layer 47, (FIG. 4E) (Ex-1005 at ¶¶ [0047], [0051]). As is shown by comparing FIG. 4E with FIG. 5, the second n-electrode 48a (orange) has an area larger than a joined face between the n-type semiconductor and the first n-electrode (*i.e.*, the area associated with 46a), so that the second n-electrode is electrically connected to the first n-electrode (Ex-1005 at ¶ [0051]; Ex-1003 at ¶ 99). Also, as shown in FIG. 5, the second p-electrode 48b has an area smaller than a joined face between the n-type semiconductor layer (43a/42 - yellow) and the p-type semiconductor layer (43c – green) (Ex-1005 at ¶ [0051]; Ex-1003 at ¶ 99). Again, the '126 patent's alleged inventive concept is disclosed (Ex-1003 at ¶ 99).

Shin Fig. 4E (Annotated)

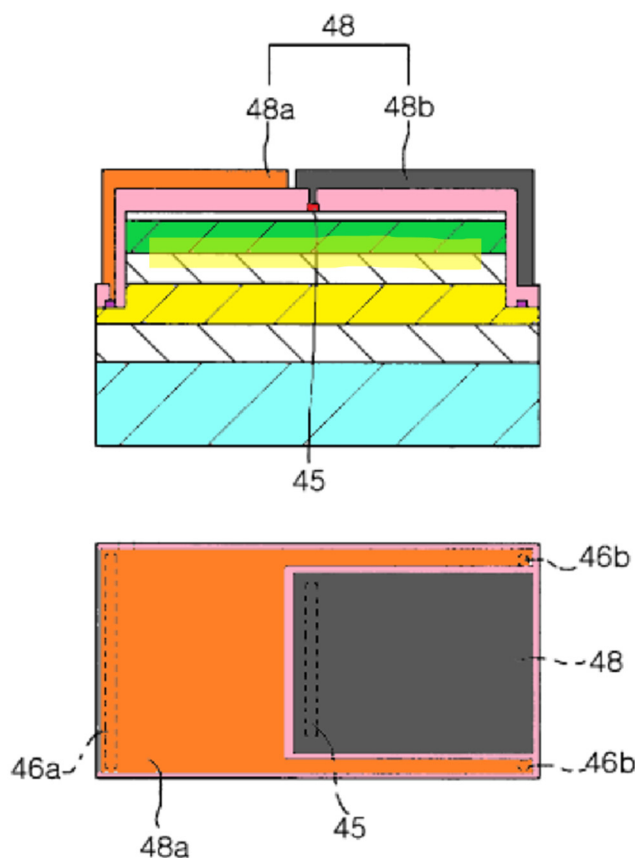


FIG. 4E

D. The Thin Film Art

The '126 patent does not claim to have invented “thin film” electrodes. The '126 patent provides examples of what constitutes a “thin film.” The '126 patent specification states that: the first n-electrode, the second n-electrode, and the second p-electrode are each formed as a thin film “having a thickness, for example, in a range of 0.1 micrometers to 0.3 micrometers” (Ex-1001 at 7:32-34; 7:42-42; 7:65-8:1) and the first p-electrode is formed as a thin film “having a thickness, for

example, in a range of 0.1 micrometers to 1.0 micrometers” (Ex-1001 at 7:32-34; 7:42-42). While the ’126 patent provides different example dimensions (*e.g.*, 0.1-0.3 & 0.1-1.0 micrometers) for what constitutes “thin,” the ’126 patent claims does not claim any dimensions associated with the claimed “thin film.”

Dr. Lebby explains that thin film electrodes were well-known and the state of the art in 2003 (Ex-1003 at § 8.2). Dr. Lebby’s opinion is supported by U.S. Patent No. 6,989,598 (Ex-1017) (“Song”), which states that “prior to the filing date of the ’126 patent, in 2004, thin film electrodes based on nickel (Ni), *e.g.*, a thin metal film of nickel/gold (Ni/Au), have been widely used as thin film electrode structures for ohmic contact” (Ex-1017 at 1:32-34). These LED thin film electrodes have “very thin thickness ($<\sim 100 \text{ \AA}$) and a transmittance of 80% or more” (Ex-1017 at 1:61-63; Ex-1003 at ¶ 102).

Sugimoto discloses that the prior art to Sugimoto included LED electrodes made as a single or multi-layer film (Ex-1006 at ¶¶ [0006], [0008]). Sugimoto also discloses “film” electrodes, where the first electrodes preferably have a thickness in the range of about 100 to 30,000 angstroms (0.01 to 3 micrometers), and the second electrodes preferably have a thickness in the range of 3,000 to 20,000 angstroms (0.3 to 2 micrometers) (Ex-1006 at ¶¶ [0065]-[0068]), which are “thin film” electrodes (Ex-1003 at ¶ 103).

Similarly, Terashima describes the first n-electrode 5a as a “plated growth film,” “thin,” and formed by either a “film deposition method, such as vacuum deposition, sputtering, or printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* Ex-1010 at ¶¶ [0038], [0061]). Shin likewise describes that the “n-electrode 46” is formed as a “lane electrode” 46a having “as narrow width as possible” with example widths of 10 to 20 micrometers (Ex-1005 at ¶¶ [0045]-[0046]).

While Shin itself does not use the words “thin film,” a POSITA understands that Shin discloses thin film electrodes based on Shin’s disclosure (Ex-1003 at ¶ 105). In describing a “conventional” LED, Shin refers to U.S. Patent No. 6,333,522 (Ex-1021) (“Inoue”). Inoue discloses thin film electrodes (Ex-1003 at ¶ 105). Inoue describes the electrodes as “metal films” (Ex-1021 at 3:35-4:17). Inoue describes that the electrodes can be formed with a titanium film with a thickness of about 0.2 microns, a gold film having a thickness of about 0.5 microns stacked by a lift-off method or an etching method resulting in a multilayer film, forming a Ni film with a thickness of about 0.2 microns over the entire surface of the wafer, followed by an Au film with a thickness of about 1 um formed thereon by vapor deposition, and forming a resist mask with openings corresponding to the respective regions, in which microbumps are formed over the Ni/Au multilayer film by a photolithography process (Ex-1021 at 13:13-29).

In addition, United States patent publication US 2003/0160259 (“Uemura ’259”) published on August 28, 2003 discloses a film thickness of 0.3 micrometers for a p-electrode provides sufficient strength and stability for general purposes and the upper limit for thickness can be based on cost and discloses n and p electrode film thicknesses in the range of 0.1 to 50 micrometers (Ex-1007 at ¶¶ [0049]; [0032]). Also, United States patent publication US 2004/0149999 (“Uemura ’999”) published on August 5, 2004 discloses a film thickness of 0.3 micrometers for a p-electrode provides sufficient strength and stability for general purposes and the upper limit for thickness can be based on cost (Ex-1007 at ¶ [0049]). The Uemura prior art disclose thin film electrodes (Ex-1003 at ¶ 106).

E. Shelton

U.S. patent application publication no. US 2005/0194605 (“Shelton”) is prior art to the ’126 patent under 35 U.S.C. § 102(a) and (e). Shelton describes subject matter set forth in some of the ’126 patent dependent claims such as dispersing “virtually uniformly” openings in an insulation layer for p-electrodes and bonding an LED to circuit board electrodes with solder and using a reflow treatment (Ex-1011 at ¶¶ [0038], [0039], [0044], FIG. 4; Ex-1003 at ¶¶ 111, 122).

IX. No Basis Exists for Discretionary Denial Under §§ 314(a) and 325(d)

Each factor regularly considered under § 314(a) weighs in favor of institution or is neutral. *General Plastics* does not apply, as this is the only IPR filed against the

'126 patent, so the Board can satisfy the requirements of 35 U.S.C. § 316(a)(11). *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential: §II.B.4.i).

Factors considered under § 314(a) related to parallel district court litigations weigh in favor of institution. Each of factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (March 20, 2020) (precedential) are addressed below:

1. **District Court Stay:** Favors institution. On May 30, 2024, a joint motion for a 30-day delay/stay of pending deadlines was filed in the Everlight-IKEA litigation (Ex-1007), which favors institution. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020).
2. **Proximity of Trial Date:** Favors Institution. Jury selection/trial has been scheduled for November 10, 2025 in the IKEA-Everlight Litigation (Ex-1014), which is close to the projected statutory deadline for this IPR. It is unlikely that Court would hold the trial if this IPR is instituted and a final written decision is imminent. This is particularly true since Everlight's other asserted patents were found invalid.
3. **Investment in Parallel Proceedings:** Favors Institution. Although the IKEA-Everlight Litigation was filed in July 2023, due to jurisdictional

disputes and related briefing, a schedule was not set until March 6, 2024 (Ex-1014). IKEA and Everlight recently submitted a request to postpone the claim construction schedule (Ex-1022). The only scheduled dates that have passed are initial contention disclosures (Ex-1014). Claim construction exchanges have just begun. Fact discovery is not open and does not open until the claim construction hearing, which has not been scheduled, and closes on April 2025 (Ex-1014). Expert discovery is from May to June 2025 (Ex-1014). Based on the initial nature of the litigation, this factor favors institution.

4. **Overlap in Issues:** This factor is neutral.
5. **Same Party:** Favors Institution. ISAG is not a party to any of the pending litigations involving the '126 patent, though ISAG has contractual relations with IKEA companies in the IKEA-Everlight Litigation.
6. **Other Circumstances:** Favors Institution. This Petition is strong on the merits. Further, while the Tashima was cited during prosecution, the USPTO appears to have only been provided with a translation of Tashima's Abstract (Ex-1002 at pp. 228-229, 239-253).

Factors considered under §325(d) favor of institution. Although Terashima

was used to reject versions of the claims during the PCT stage (Ex-1009 at pp. 4-6), Patent Owner never rebutted the rejections based on Terashima. The only portion of Terashima that was cited to the Examiner in the English language was the Abstract, while the specification, figures, and claims of Terashima were only provided in Japanese (Ex-1002 at pp. 228-229, 239-253). Thus, it is not clear that the Examiner considered the full scope of Terashima's disclosure when allowing the '126 patent. As is demonstrated in detail in § XI(A), *infra*, the strength of the challenge based on Terashima is strong enough to demonstrate an error by the Office in a manner material to the claims regarding its consideration of the non-English version of Terashima. *Sony Interactive Entertainment LLC v. Bot M8, LLC*, IPR2020-00726, Paper 13, at 11-13 (PTAB Oct. 6, 2020).

Further, neither Sugimoto nor Shin was considered by the Examiner (See Ex-1001 at References Cited; Ex-1002), which favors institution. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6 (PTAB. Feb. 13, 2020) (precedential).

X. Claim Construction

A claim construction order was recently issued in the Walmart-Everlight Litigation construing one term from the '126 patent (Ex-1016). Petition applies that construction for the “forming a first insulating layer” (Ex-1016 at 2-3). Given that the prior art is nearly identical to the structures disclosed in the '126 patent, additional

constructions do not appear necessary and plain meaning is applied. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

XI. Specific Grounds for Petition

The twelve petition grounds are provided below. Exemplary citations to the applied art are provided below. Dr. Lebby describes where each limitation is taught by a reference (Ex-1003 at § 9). However, citations are generally to the reference itself. How the references figures match up to the claims is explained with the color scheme below.

Claim 1 Element	Terashima Disclosure
Preamble	“optical semiconductor device (LED component)”
substrate	“transparent insulating substrate 1” [blue]
n-type layer	“n-type nitride semiconductor layer 2” [yellow]
p-type layer	“p-type nitride semiconductor layer 3” [green]
first n-electrode	“plated growth film 5a” [purple]
first p-electrode	“plated growth film 4a” [red]
first insulating layer	“protective film 20” [pink]
second n-electrode	“n electrode 5b” [orange]
second p-electrode	“p electrode 4b” [gray]

Reference	Claim 2 Limitations
Preamble	“optical semiconductor device (LED component)”
Substrate	“transparent insulating substrate 1” [blue]
n-type layer	“n-type nitride semiconductor layer 2” [yellow]
p-type layer	“p-type nitride semiconductor layer 3” [green]
first n-electrode	“plated growth film 5a” [purple]
first p-electrode	“plated growth film 4a” [red]
first insulating layer (2)	“protective film 20” [pink]
second n-electrode (2)	“n electrode 5b” [orange]
second p-electrode (2)	“p electrode 4b” [gray]

A. Ground 1: Anticipation of Claims 1, 2, 5-8, & 9-12 by Terashima

For Ground 1, the prior art consists of Terashima (Ex-1004; Translation at Ex-1010). The challenged claims are claims 1, 2, 5-8, & 9-12.

1. Terashima Anticipates Claim 1

Terashima teaches each claim limitation (Ex-1003 at § 9.1.1).

a. Terashima Discloses Claim 1’s Preamble

The “LED component” illustrated in Terashima FIG. 5 (Ex-1004 at ¶¶ [0001], [0062] disclosing a “flip-chip”, [0070], Claim 10), which is reproduced below, is the “semiconductor light-emitting element” claimed in claim 1’s preamble.

b. Terashima Discloses the Substrate Limitation

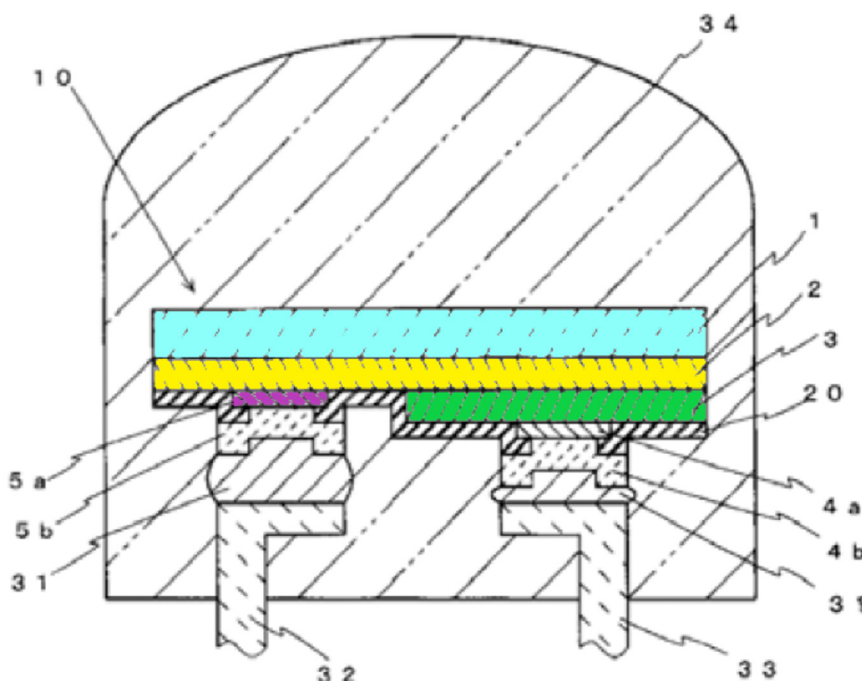
In FIG. 5, Terashima discloses a “transparent insulating substrate 1” [blue] which is the claimed “light-transmitting element substrate” (Ex-1010 at ¶¶ [0032], [0061], “Description of Reference Numerals” at “1”). Terashima discloses that the substrate 1 can be sapphire, which is “transparent” and light-transmissive” (Ex-1010 at ¶¶ [0032], [0061]; Ex-1003 at ¶ 129).

Terashima's "n-type nitride semiconductor layer 2" [yellow] is the claimed "n-type semiconductor layer formed on the element substrate so as to cover the element substrate" (Ex-1010 at ¶¶ [0017], [0032], [0061], "Description of Reference Numerals" at "2"). As shown in FIG. 5, Terashima's n-type nitride semiconductor layer 2 [yellow] is formed on "the entire surface of a transparent insulating substrate 1" [blue] (e.g., the claimed "light-transmitting element substrate) (Ex-1010 at ¶¶ [0032]) [0061], [0062]; Ex-1003 at ¶ 130).

Terashima's "p-type nitride semiconductor layer 3" is the claimed "p-type semiconductor layer formed so as to cover an area on the n-type semiconductor layer from which an area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer" (Ex-1003 at ¶ 131). Terashima's "metal plating film 5a" is the claimed "n-electrode." As shown in FIG. 5, the p-type nitride semiconductor layer 3 [green] is "formed so as to cover an area on the n-type semiconductor layer" 2 [yellow], and the p-type nitride

semiconductor layer 3 [green] is “excluded” from the area where the first n-electrode [purple] is in contact with the n-type semiconductor layer 2 [yellow] (Ex-1010 at ¶¶ [0032], [0033]-[0035]; [0061]; Ex-1003 at ¶ 131).

Terashima FIG. 5 (Annotated)

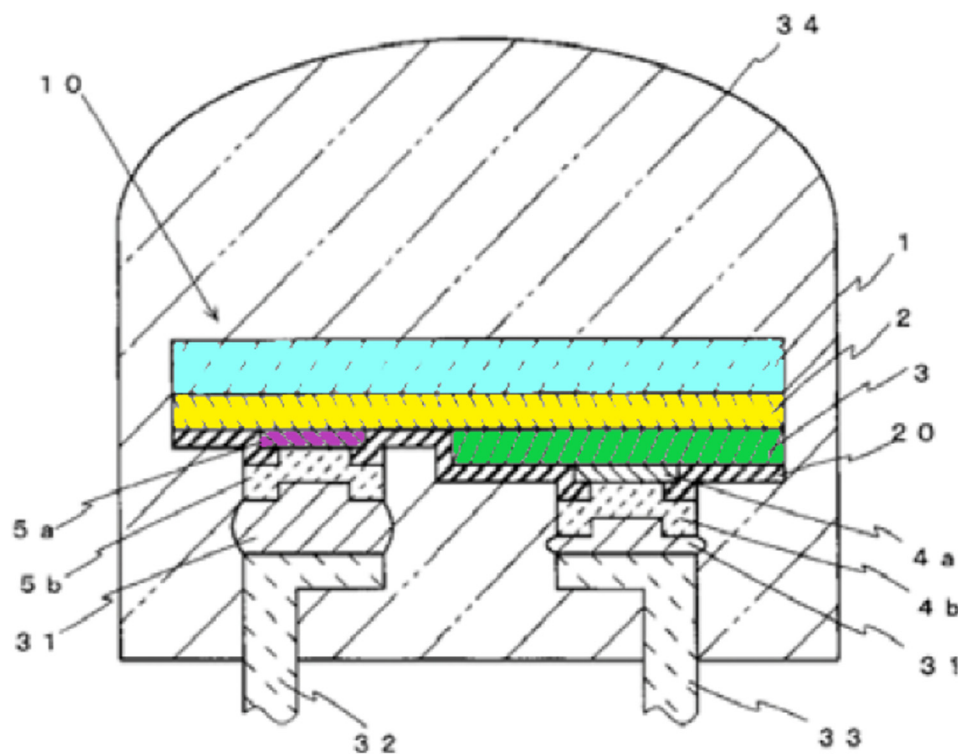


e. Terashima Discloses the first N-Electrode Limitation

Terashima’s “plated growth film” 5a [purple], with “metal as the main component” is the claimed “first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer” (Ex-1003 at ¶ 132). Terashima describes the first n-electrode 5a as a “plated growth film,” “thin,” and formed by a “film deposition method, such as vacuum deposition, sputtering, or printing” (Ex-1010 at ¶¶ [0034]-[0035]; *see also* ¶¶ [0038], [0061]), which are processes known for making thin film electrodes (Ex-1003 at ¶ 132). Terashima also explains that the film

4a or first n-electrode must be “thin enough to maintain transparency” (Ex-1010 at ¶ [0035]). Terashima further describes that the first n-electrode 5a is “provided on a portion of the n-type nitride semiconductor material” 2 [yellow] (FIG 5. below) (Ex-1010 at ¶ [0034]).

Terashima FIG. 5 (Annotated)

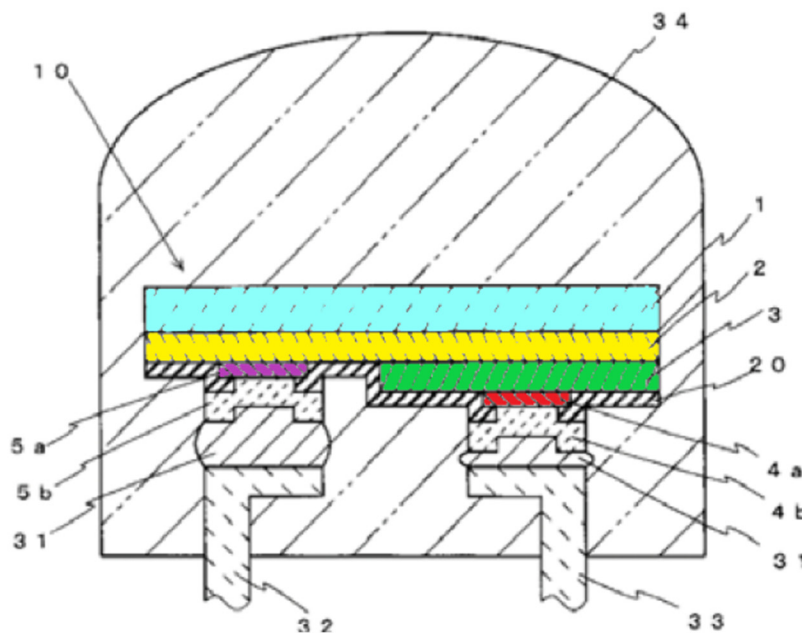


f. Terashima Discloses the First P-Electrode Limitation

Terashima’s “plated growth film 4a” [red] is the claimed “first p-electrode that is a thin film formed on the p-type semiconductor layer” (Ex-1003 at ¶ 133). Terashima describes the first p-electrode 5a is a “plated growth film,” “thin,” and formed with a “film deposition method, such as vacuum deposition, sputtering, or

printing (Ex-1010 at ¶¶ [0034]-[0035]; *see also* Ex-1010 at ¶¶ [0038], [0061]), which are processes known for making thin film electrodes (Ex-1003 at ¶ 133). The metal plating film 4a [red] is “provided on an upper layer of the p-type nitride semiconductor 3” [green] (FIG 5. below) (Ex-1010 at ¶ [0034]).

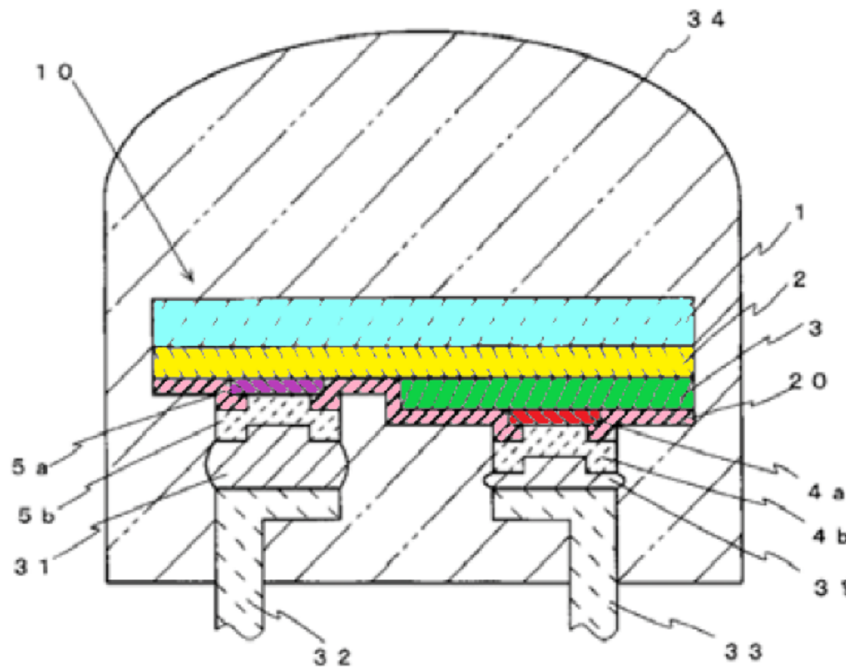
Terashima FIG. 5 (Annotated)



g. Terashima Discloses the First Insulating Layer Limitation

Terashima’s “protective film 20” [pink] is the claimed “first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other” (Ex-1003 at ¶ 134). Terashima’s “protective film 20” [pink] is made from a “material having good insulating properties such as silicon oxide (SiO₂) or silicon nitride (Si₃N₄)” (Ex-1010 at ¶¶ [0036], [0061]; *see also* Ex-1010 at ¶ [0037]). As

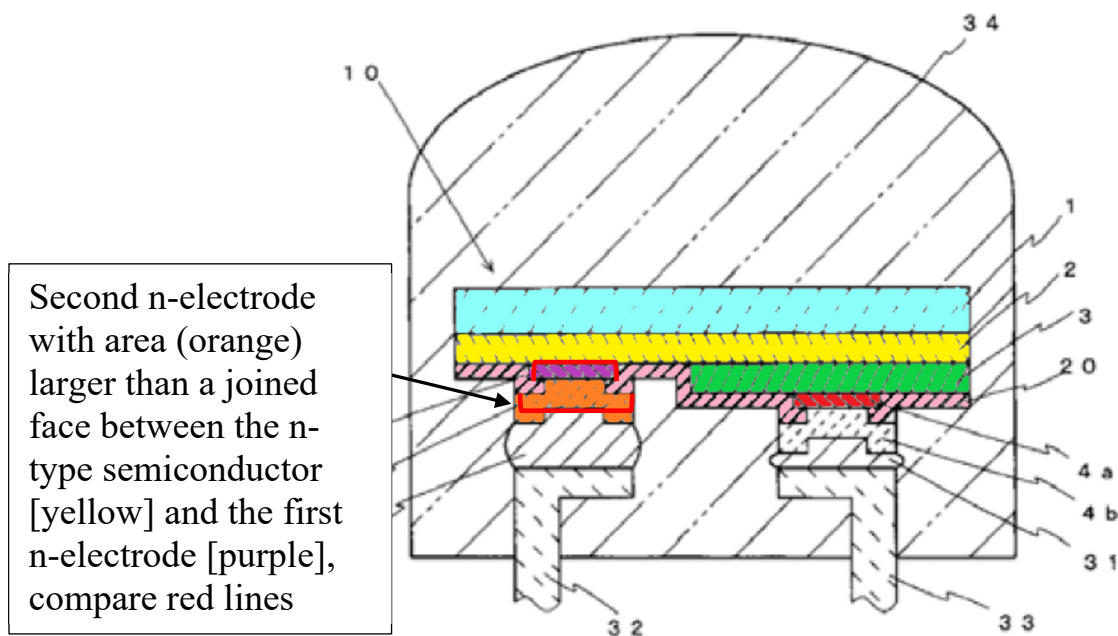
Terashima FIG. 5 (Annotated)



Terashima's "n electrode 5b" [orange] is the claimed "second n-electrode formed on the first n-electrode and the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode, the second n-electrode being insulated from the first p-electrode by the first insulating layer" (Ex-1003 at ¶ 135). As shown in FIG. 5, the "n electrode 5b" [orange] is provided on or "formed" on the first n-electrode (*i.e.*, Terashima's "metal film 5a" [purple]) and the first insulating layer (*i.e.*, Terashima's "protective layer

20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0037], [0046], [0053], [0051], [0059], [0061]). Terashima describes the second n-electrode is a “film” or “single layer film” (e.g., “thin”) (Ex-1010 at ¶¶ [0038], [0059]). As shown in FIG. 5, the “n electrode 5b” [orange] has “an area larger than a joined face” between the n-type semiconductor layer 2 [yellow] and the first n-electrode 5a [purple]) (Ex-1003 at ¶ 135).

Terashima FIG. 5 (Annotated)

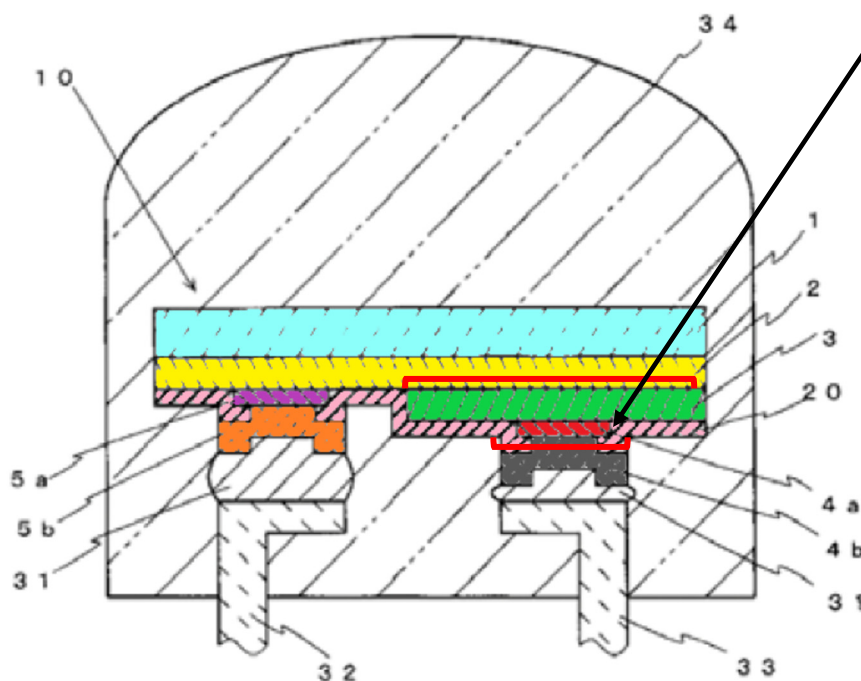


i. Terashima Discloses the Second P-Electrode Limitation

Terashima’s “p electrode 4b” [gray] is the claimed “second p-electrode formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode” (Ex-1003 at ¶ 136) Terashima describes the second p-electrode as a “film” or “single layer film” (e.g., “thin”) (Ex-

1010 at ¶¶ [0038], [0059]). Further, Terashima FIG. 5 shows the “p electrode 4b” [gray] is “provided on” or “formed on” the first p-electrode (*i.e.*, Terashima’s “metal film 4a” [red]) and the first insulating layer (*i.e.*, Terashima’s “protective layer 20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0038], [0046], [0053], [0059], [0061]). As shown in FIG. 5, Terashima’s second “p electrode 4b” [gray] has “an area smaller than a joined face” between the n-type semiconductor layer 2 [yellow] and the p-type semiconductor layer 3 [green]) (Ex-1003 at ¶ 136).

Terashima FIG. 5 (Annotated)



2. Terashima Anticipates Claim 2

Claim 2’s preamble and first five elements are the same as claim 1. Therefore, Terashima discloses claim 2’s preamble and the first five elements as described above

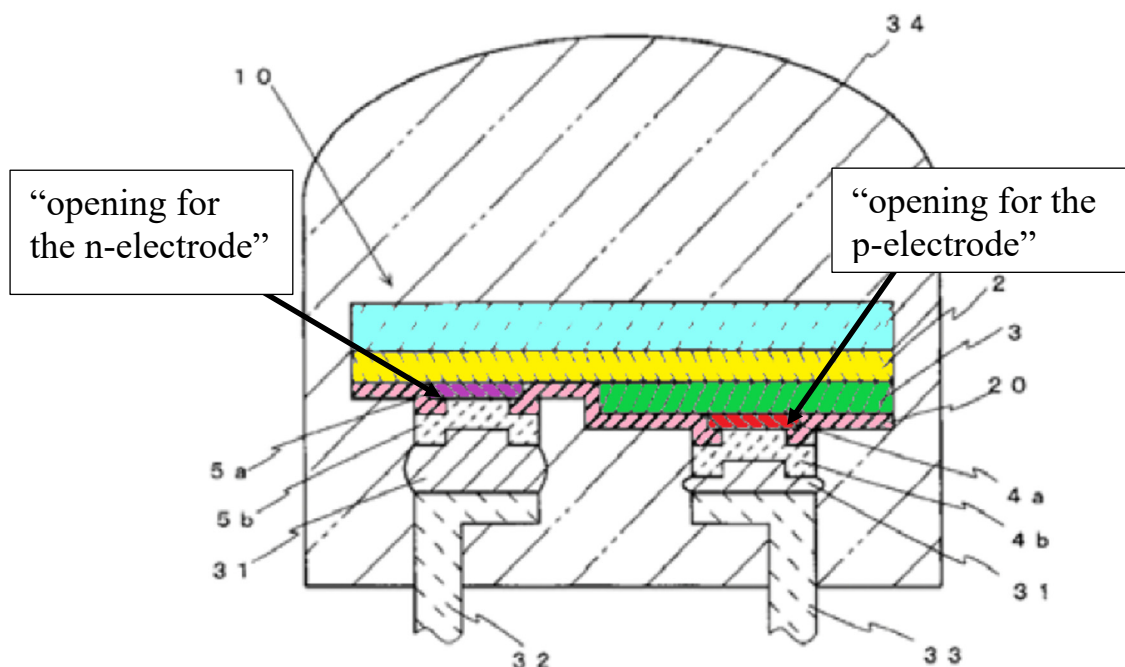
with reference to claim 1 (*see supra* §XI.A.1.). Terashima anticipates claim 2 (Ex-1003 at § 9.1.2)

a. Terashima Discloses Claim 2’s First Insulating Layer Limitation

Terashima’s “protective film 20” [pink] is the claimed “a first insulating layer having at least one opening for the n-electrode and one opening for the p-electrode formed therein, which covers the first n-electrode and the first p-electrode so as to insulate the first n-electrode and the first p-electrode from each other, except for the opening for the n-electrode and the opening for the p-electrode” (Ex-1003 at ¶ 139). Terashima’s “protective film 20” [pink] is made from a “material having good insulating properties such as silicon oxide (SiO₂) or silicon nitride (Si₃N₄)” (Ex-1010 at ¶¶ [0036], [0061]; *see also* ¶ [0037]). As shown in FIG. 5, the protective film 20 [pink] covers the first n-electrode and first p-electrode and is formed so as to insulate the first n-electrode and the first p-electrode from each other (Ex-1003 at ¶ 139). The protective film 20 [pink] is also described to have an “opening for the n-electrode” and an “opening for the p-electrode” (Ex-1010 at ¶¶ [0020], [0029]) to allow for electrical connections to the n-type semiconductor layer 2 [yellow] and p-type semiconductor layer 3, respectively (Ex-1003 at ¶ 139).

Terashima FIG. 5 (Annotated)

[Figure 5]



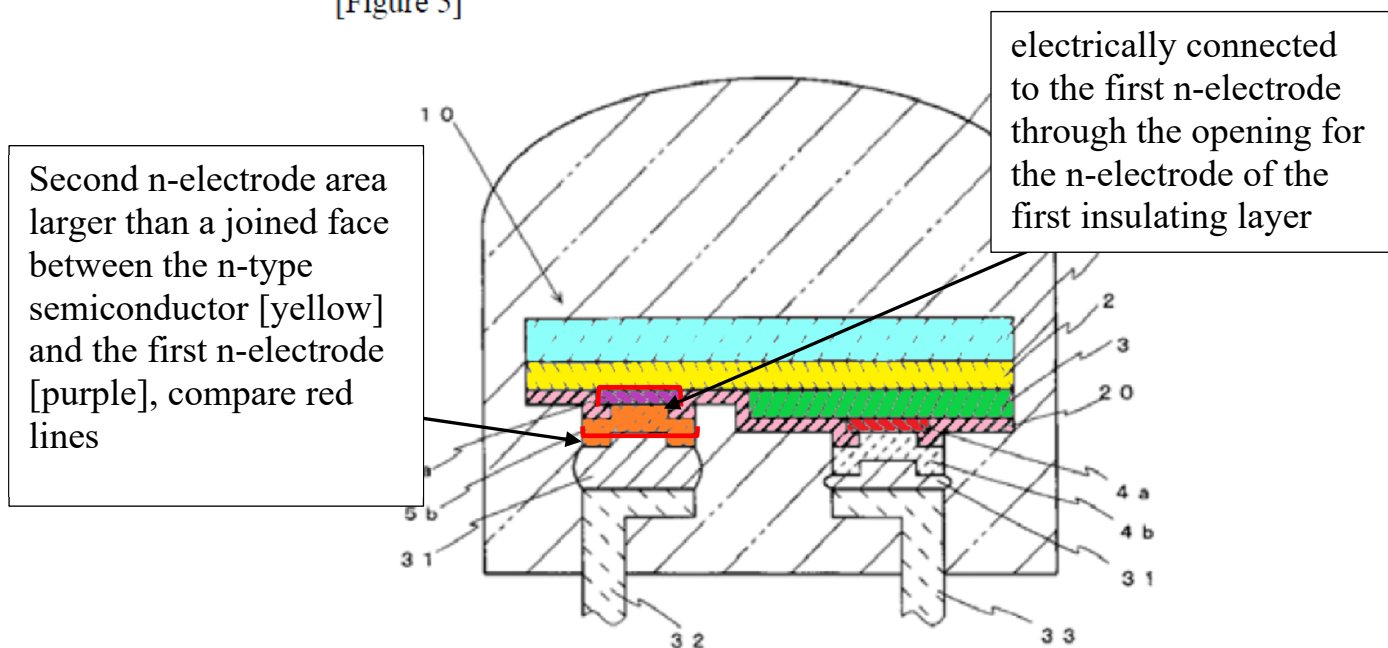
b. Terashima Discloses Claim 2’s Second N-Electrode Limitation

Terashima’s “n electrode 5b” [orange] is the claimed “a second n-electrode formed on the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor layer and the first n-electrode, the second n-electrode being electrically connected to the first n-electrode through the opening for the n-electrode of the first insulating layer” (Ex-1003 at ¶ 140). FIG. 5 shows that the “n electrode 5b” [orange] is provided on or “formed” on the first insulating layer

(i.e., Terashima's "protective layer 20" [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0037], [0046], [0053], [0051], [0059], [0061]). Terashima describes the second n-electrode as a "film" or "single layer film" and therefore a "thin" film (Ex-1010 at ¶ [0038], [0059]; Ex-1003 at ¶ 140). Terashima also shows in FIG. 5, the "n electrode 5b" [orange] has "an area larger than a joined face" between the n-type semiconductor layer 2 [yellow] and the first n-electrode 5a [purple]) and is "electrically connected to the first n-electrode through the opening for the n-electrode of the first insulating layer" (see Ex-1010 at ¶ [0062] describing electrical connections) (Ex-1003 at ¶ 140).

Terashima FIG. 5 (Annotated)

[Figure 5]

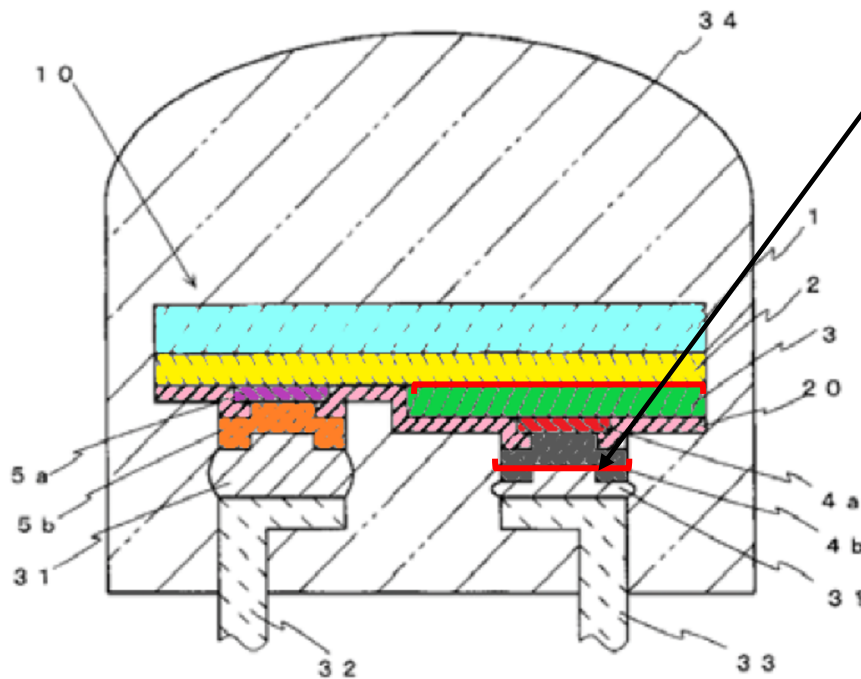


c. Terashima Discloses Claim 2's Second P-Electrode Limitation

Terashima's "p electrode 4b" [gray] is the claimed "a second p-electrode

formed on the first insulating layer as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode through the opening for the p-electrode of the first insulating layer” (Ex-1003 at ¶ 141). Terashima describes the second p-electrode as a “film” or “single layer film” and therefore a “thin film” (Ex-1010 at ¶¶ [0038], [0059]; Ex-1003 at ¶ 141). Further, FIG. 5 shows the “p electrode 4b” [gray] is “provided on” or “formed on” the first insulating layer (*i.e.*, Terashima’s “protective layer 20” [pink]) (Ex-1010 at ¶¶ [0029], [0034], [0038], [0046], [0053], [0059], [0061]). Terashima’s second “p electrode 4b” [gray] also has “an area smaller than a joined face” between the n-type semiconductor layer 2 [yellow] and the p-type semiconductor layer [green] and is “electrically connected to the first p-electrode through the opening for the p-electrode of the first insulating layer” (*see* Ex-1010 at ¶ [0062] describing electrical connections; (Ex-1003 at ¶ 141).

Terashima FIG. 5 (Annotated)

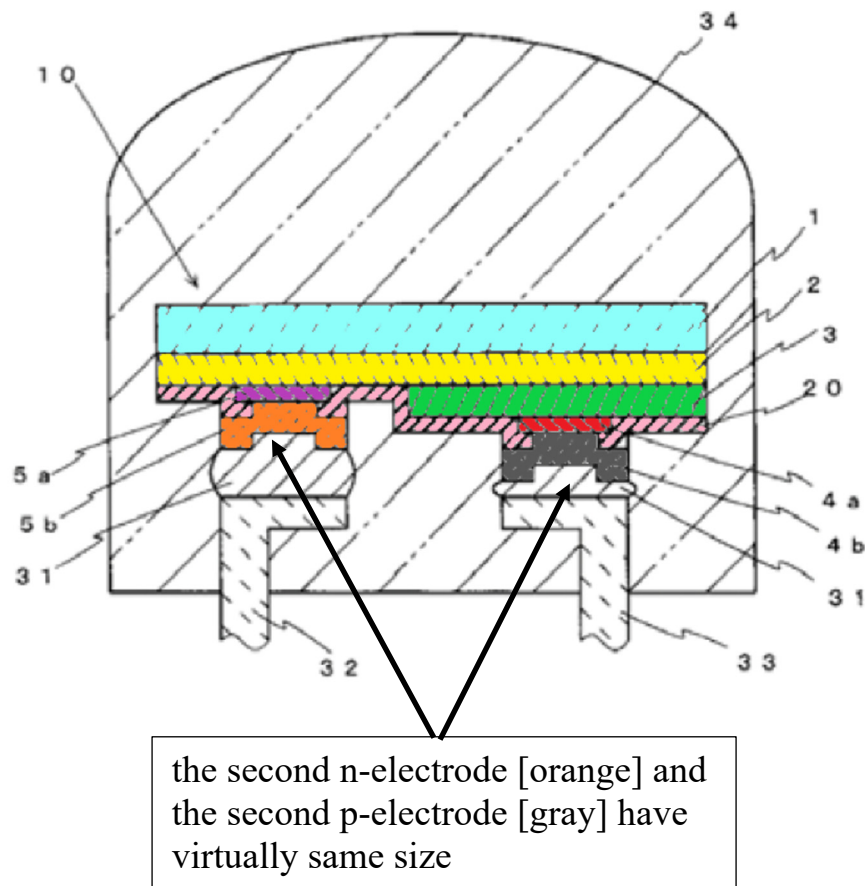


Second -electrode area smaller than a red joined face between the n-type semiconductor layer [yellow] and the p-type semiconductor layer [green], compare red lines

3. Terashima Anticipates Claim 5

Terashima discloses in Fig. 5 that “the second n-electrode” (*i.e.*, n electrode 5b [orange]) and the second p-electrode (*i.e.*, p electrode 4b [orange]) have virtually same size” (Ex-1003 at ¶ 142). Terashima provides an example where the second n and p electrodes 4b, 5b “can be “formed to a desired thickness” (*e.g.*, virtually the same thickness) (Ex-1010 at ¶ [0038]).

Terashima, FIG. 5 (Annotated)

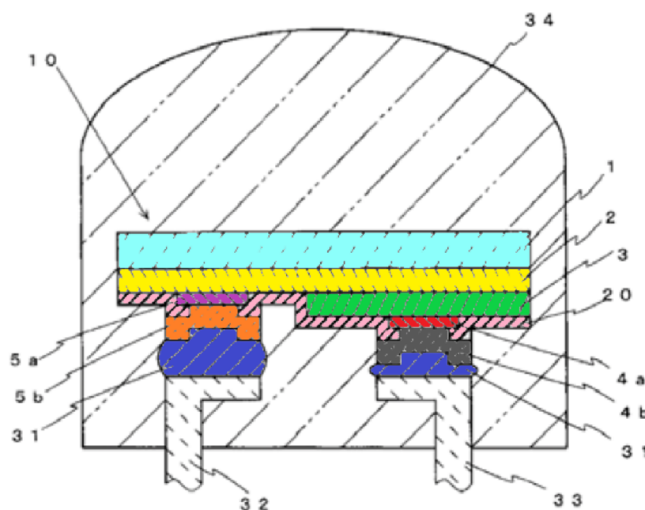


4. Terashima Anticipates Claim 6

To the extent that claim 6 has any meaning, Terashima anticipates claim 6. For example, Terashima discloses (FIG. 5) solder 31 [indigo] which is “used to fuse” electrodes 5b [orange] and 4b [gray] “to the lead frames 32, 33” for “electrical connection” (Ex-1010 at ¶ [0062]); (Ex-1003 at ¶ 143). Solder is the claimed “conductive layer” (Ex-1003 at ¶ 143).

Terashima, FIG. 5 (Annotated)

[Figure 5]



5. Terashima Anticipates Claim 7

Claim 7 recites a “light-emitting device comprising: the semiconductor light-emitting element according to claim 1; a circuit board having a plurality of electrodes; and a conductive bonding material layer that electrically connects and fixes the second n-electrode and the second p-electrode to the electrodes on the circuit board.”

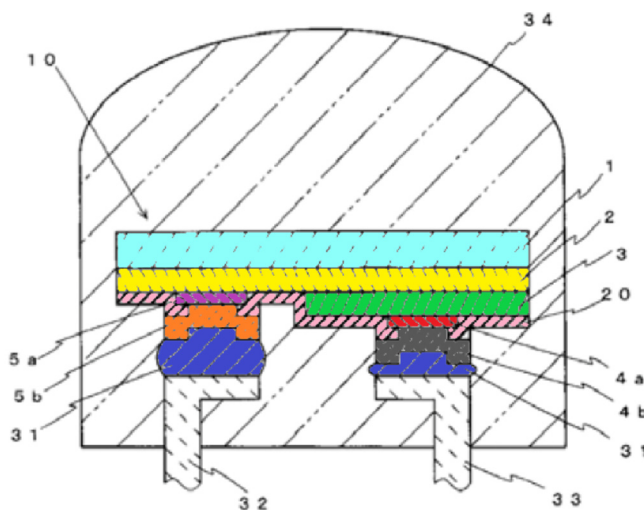
Terashima discloses solder 31 [indigo] (“a conductive bonding layer”) which is “used to fuse” electrodes 5b [orange] and 4b [gray] of a semiconductor light emitting device “to the lead frames 32, 33 [brown]” for electrical connection (Ex-1010 at [0062]; Ex-1003 at ¶ 145). A POSITA would have understood that the lead frames 32, 33 [brown] are a “plurality of electrodes” that are inherently connected to

a circuit board or other electrical component (Ex-1003 at ¶ 145).

6. Terashima Anticipates Claim 8

Terashima anticipates claim 8 (Ex-1003 at ¶ 146). Terashima discloses (FIG. 5) solder 31 [indigo] which is a “conductive bonding layer” to fuse electrodes 5b [orange] and 4b [gray] “to the lead frames 32, 33” for electrical connection (Ex-1010 at ¶ [0062]; Ex-1003 at ¶ 146).

Terashima, FIG. 5 (Annotated)



7. Terashima Anticipates Claims 9 & 10

Claims 9 and 10 are methods corresponding respectively to the devices in claims 1 and 2. Terashima anticipates claims 9 and 10 for the reasons described with respect to claims 1 and 2 (*see supra* §XI.A.1-X.A.2).

8. Terashima Anticipates Claim 11

Claim 11 reads: “[t]he method for manufacturing a semiconductor light-emitting element according to claim 10, wherein the first insulating layer is formed

through sputtering is the corresponding method recited in claim 1.” Terashima anticipates claim 11 (Ex-1003 at ¶ 149). Terashima teaches that the protective film 20, which is the claimed “first insulating layer,” “is formed by a film forming means such as vacuum deposition or sputtering” (Ex-1010 at ¶ [0036]).

9. Terashima Anticipates Claim 12

Claim 12 reads: “[t]he method for manufacturing a semiconductor light-emitting element according to claim 9, wherein the second n-electrode and the second p-electrode are formed through sputtering or plating.” Terashima anticipates claim 12 (Ex-1003 at ¶ 150). Terashima discloses that electrodes 4b, 5b, which are the claimed second n- and p-electrodes, respectively, can be formed by “plating” (Ex-1010 at ¶ [0034]).

B. Ground 2: Sugimoto Anticipates Claims 1, 6, 9, & 12

For Ground 2, the prior art consists of Sugimoto (Ex-1006). Sugimoto anticipates claims 1, 5, 6, 9, and 12 (Ex-1003 at § 9.2).

1. Sugimoto Anticipates Claim 1

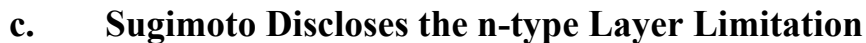
Sugimoto discloses each element of claim 1 as described below (Ex-1003 at § 9.2.1).

a. Sugimoto Discloses Claim 1’s Preamble

Sugimoto discloses “a semiconductor light-emitting element.” For example, Sugimoto describes a “nitride semiconductor device” that emits light (Ex-1006 at ¶¶

b. Sugimoto Discloses the Substrate Limitation

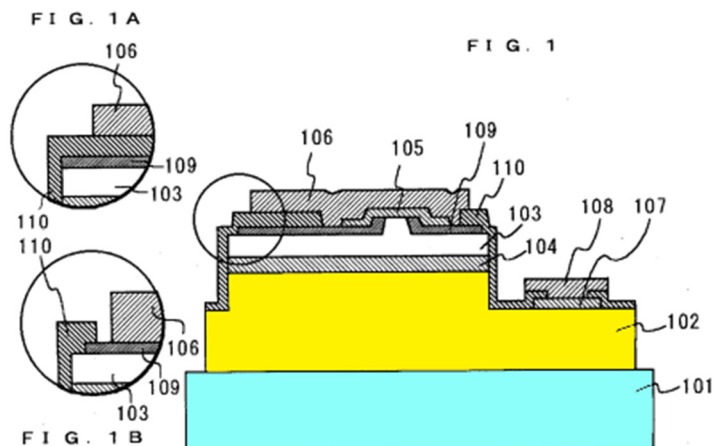
Sugimoto Figs. 1, 1A, 1B (Annotated)



55

substrate 101 [blue] so as to cover the element substrate 101 [blue].”

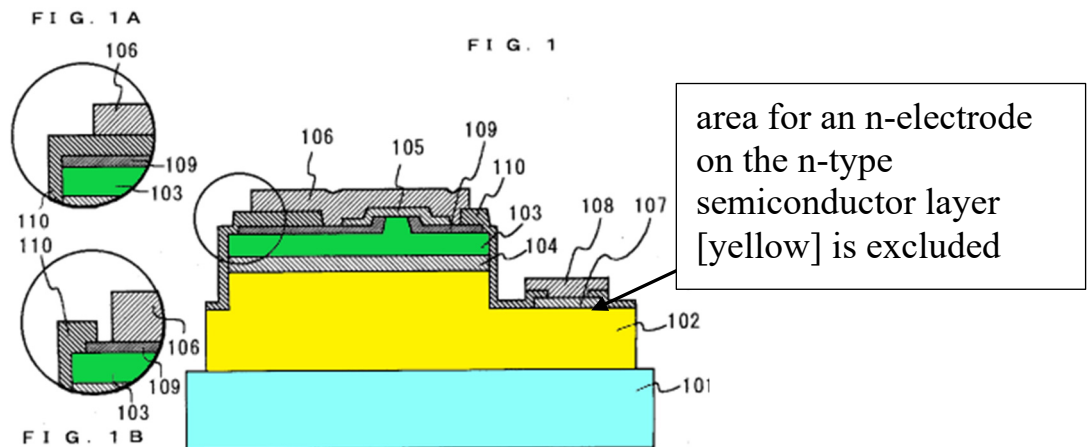
Sugimoto Figs. 1, 1A, & 1B (Annotated)



d. Sugimoto Discloses the P-Type Layer Limitation

Sugimoto discloses a “p-type semiconductor layer” (*i.e.*, “p-type nitride semiconductor layer 103” [green]) formed so as to cover an area on the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]) from which an area for an n-electrode (*i.e.*, “first n electrode 107” [purple]) on the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]) is excluded, for emitting light in cooperation with the n-type semiconductor layer (*i.e.*, “n-type semiconductor layer 102” [yellow]) (Ex-1003 at ¶ 156; Ex-1006 at ¶¶ [0072]-[0074]).

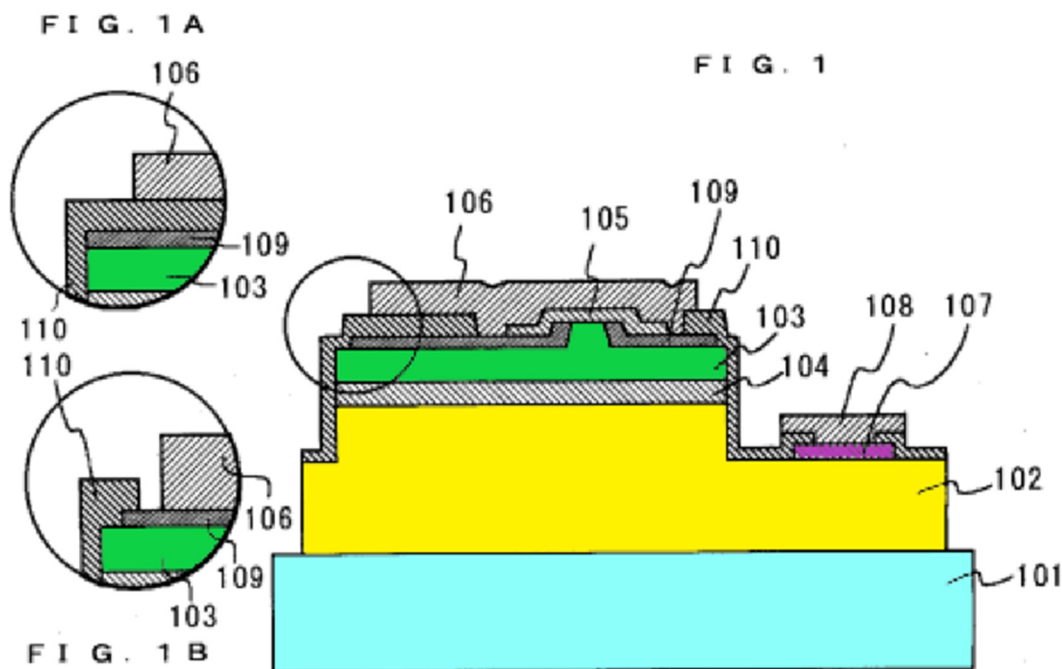
Sugimoto Fig. 1, 1A, & 1B (Annotated)



e. Sugimoto Discloses the first n-electrode Limitation

Sugimoto discloses “a first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer” (Ex-1003 at ¶ 157). For example, Sugimoto discloses a first n-type electrode 107 [purple] that is a thin film formed on the area of the n-electrode of the n-type semiconductor layer (Ex-1006 at ¶ [0073]). Sugimoto discloses “thin film” electrodes and describes that the first n-electrode is a thin film preferably having a thickness in the range of about 100 to 30,000 angstroms (0.01 to 3 micrometers) (Ex-1006 at ¶¶ [0061]-[0064]; Ex. 1003 at ¶ 157).

Sugimoto Fig. 1, 1A, & 1B (Annotated)

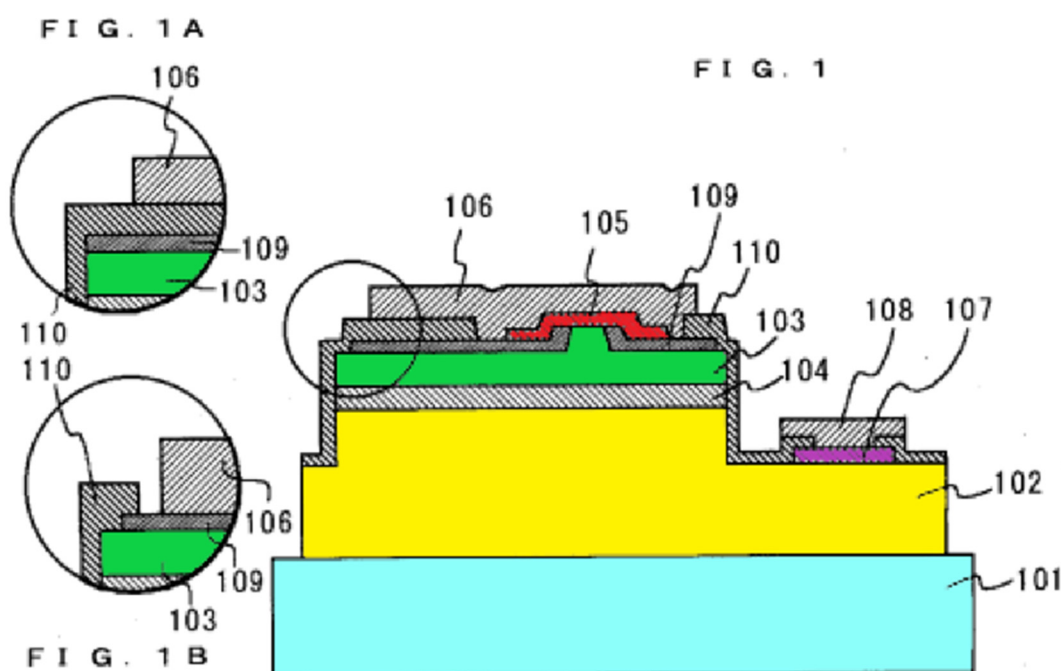


f. Sugimoto Discloses the First P-Electrode Limitation

Sugimoto discloses “a first p-electrode that is a thin film formed on the p-type semiconductor layer” (Ex. 1003 at ¶ 158). For example, Sugimoto discloses a nitride semiconductor device having “a first p electrode 105” [red] (Ex-1006 at ¶¶ [0073], [0075]). Sugimoto discloses that the first p-electrode is a thin “film” electrode (Ex-1006 at ¶¶ [0061]-[0064], [0067]). Sugimoto discloses “thin film” electrodes and describes that the first n-electrode preferably has a thickness in the range of about 100 to 30,000 angstroms (0.01 to 3 micrometers) (Ex-1006 at ¶¶ [0061]-[0064]). A POISTA would understand that Sugimoto discloses that the first

p-electrode has the same preferable dimensions as the first n-electrode because the two first electrodes are extensively described together regarding layers, materials, and manufacturing (Ex-1006 at ¶¶ [0014]-[0018]; [0020]-[0034], [0053], [0055], [0059]; Ex. 1003 at ¶¶ 103, 158).

Sugimoto Figs. 1, 1A, & 1B (Annotated)

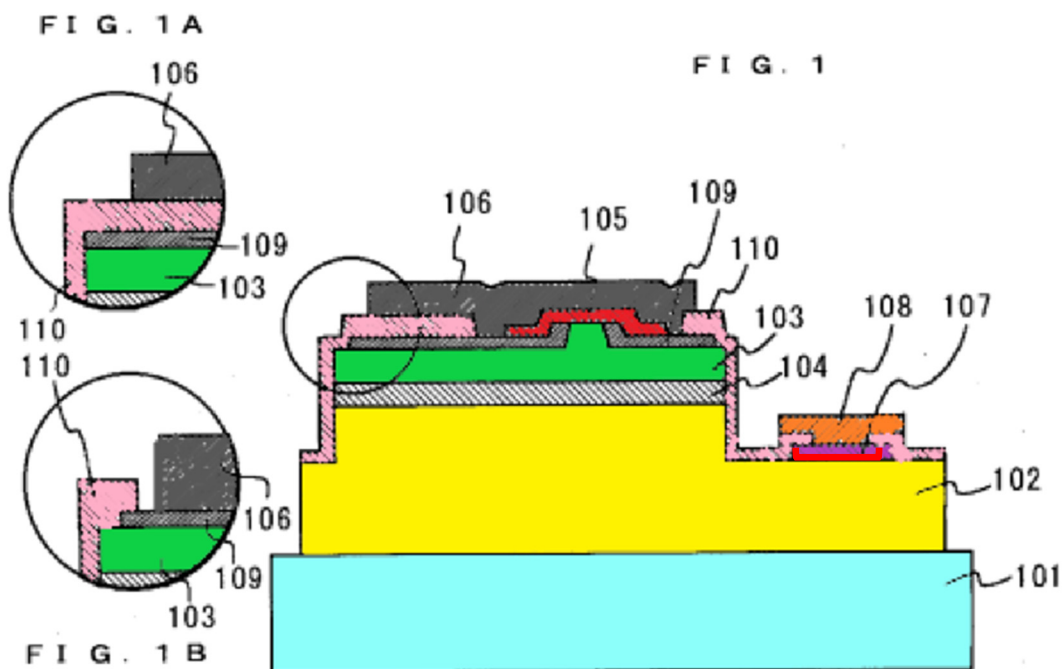


g. Sugimoto Discloses the First Insulating Layer Limitation

Sugimoto discloses “a first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other” (Ex. 1003 at ¶ 159). For example, Sugimoto discloses a nitride semiconductor device having “second insulating layer 110” [pink] (Ex-1006 at ¶¶ [0073], [0075]). Although Sugimoto’s “second insulating layer 110” is referred to as a “second” layer, Sugimoto’s “second

insulating layer 110” satisfies the claimed “first insulating layer” limitations (Ex. 1003 at ¶ 159). Sugimoto explains that the insulating layer 110 prevents “short circuit between the p-side electrodes and the n-side electrodes” and “is provided over the entire surface of the composite structure except the upper surface of the [second electrodes] (Ex-1006 at ¶¶ [0075], [0081]). As shown in FIG. 1, Sugimoto’s “insulating layer” 110 electrically insulates current from flowing between the first n-electrode 107 (purple) and the first and second p-electrodes 105, 106 (red, grey).

Sugimoto Figs. 1, 1A, & 1B (Annotated)



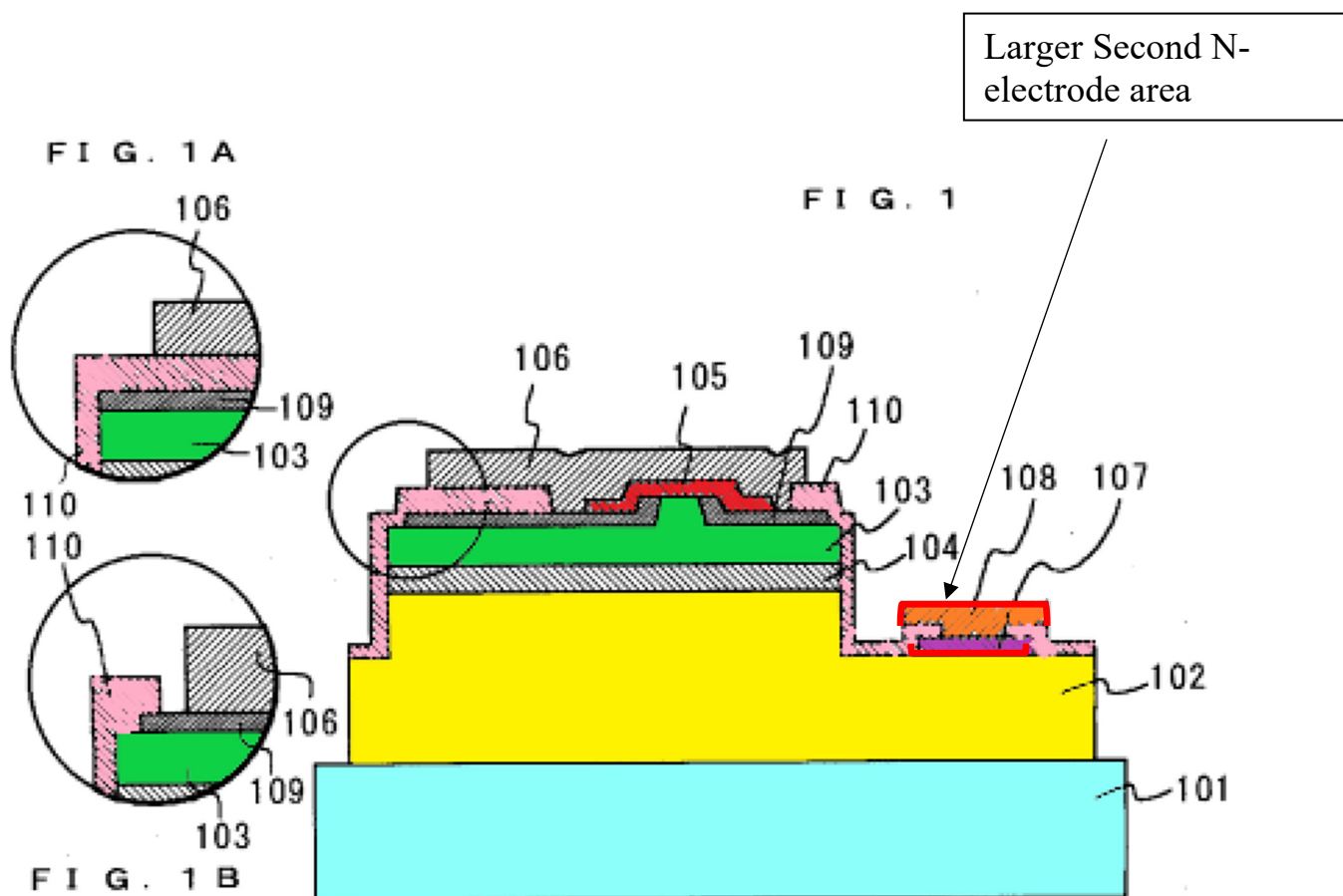
h. Sugimoto Discloses the Second N-Electrode Limitation

As shown in FIG. 1, Sugimoto discloses “a second n-electrode” (*i.e.*, second n electrode 108 [orange]) formed on the first n-electrode 107 [purple] and the first

insulating layer 110 [pink] as a thin film having an area larger than a joined face between the n-type semiconductor layer 102 [yellow]) and the first n-electrode 107 [purple], so that the second n-electrode 108 [orange] is electrically connected to the first n-electrode 107 [purple]), the second n-electrode 108 [orange] being insulated from the first p-electrode 105 [red] by the first insulating layer 110 [pink]) (Ex. 1003 at ¶ 161).

Sugimoto discloses that the claimed second n-electrode 108 [orange] is a “thin film” preferably having a thickness in the range of about 3,000 to 20,000 angstroms (0.03 to 0.2 micrometers) (Ex-1006 at ¶¶ [0061]-[0063], [0066]; Ex. 1003 at ¶¶ 103, 160). Sugimoto states that second n-electrode 108 is provided “on first n electrode” (Ex-1006 at ¶ [0073], FIG. 1).

Sugimoto Figs. 1, 1A, & 1B (Annotated)

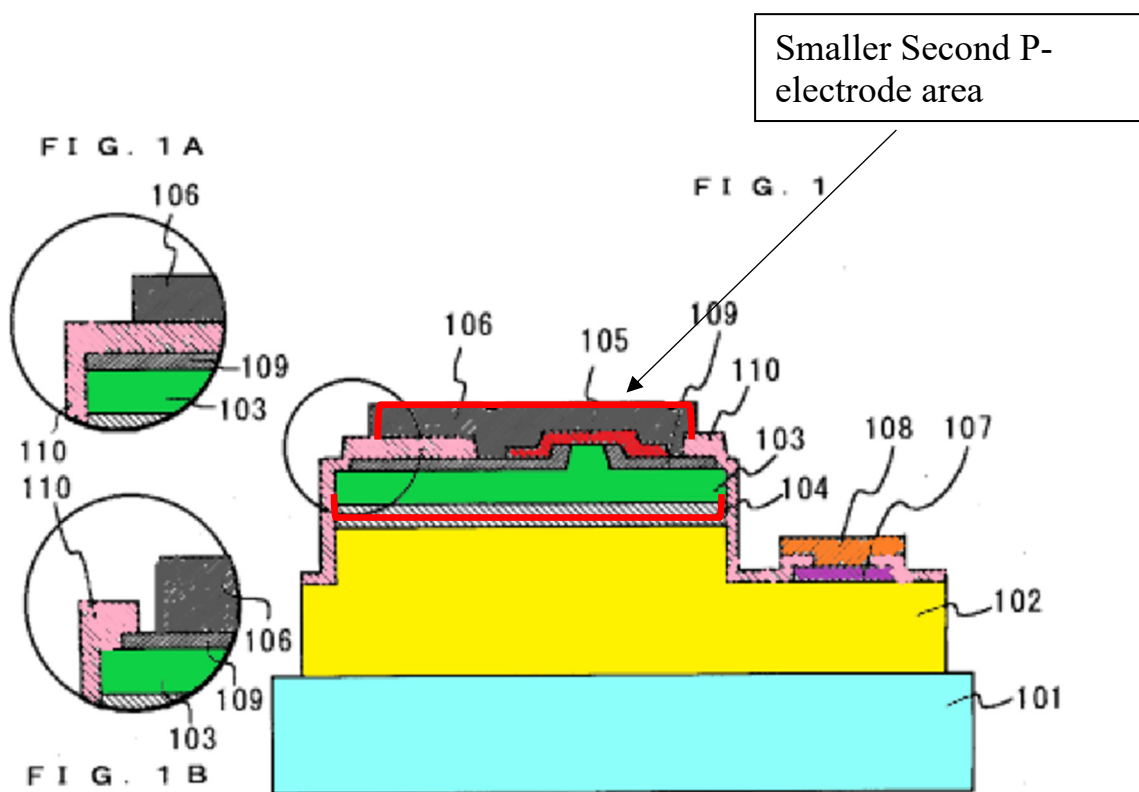


i. Sugimoto discloses the Second P-Electrode Layer Limitation

Sugimoto discloses in FIG. 1 “a second p-electrode” 106 formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer 102 [yellow] and the p-type semiconductor layer 103 [green], the second p-electrode 106 being electrically connected to the first p-electrode 105) (Ex. 1003 at ¶ 161). Sugimoto discloses a thin film second p-electrode because Sugimoto describes “film” electrodes and that the second n-electrode preferably has a thickness in the range of

about 3,000 to 20,000 angstroms (0.03 to 0.2 micrometers) (Ex-1006 at ¶¶ [0061]-[0063], [0068]; Ex. 1003 at ¶¶ 103, 162).

Sugimoto Fig. 1, 1A, & 1B Annotated

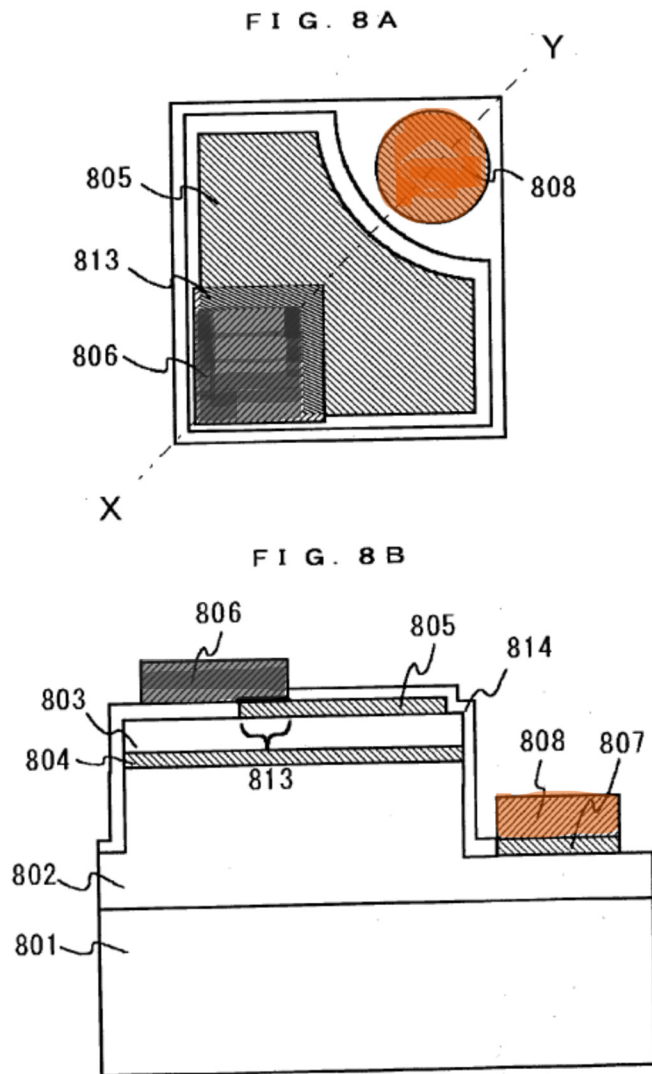


2. Sugimoto Anticipates Claim 5

Claim 5 recites that “semiconductor light-emitting element according to claim 1, wherein the second n-electrode and the second p-electrode have virtually same size.” Sugimoto discloses an embodiment in Figure 8 that meets this limitation showing that second p-electrode 806 (gray) and the second n-electrode (orange) 808 have the same thickness and are “virtually the same size” even though

they have different shapes (Ex-1006 at ¶ [0103]; Figs. 8A, 8B; Ex. 1003 at ¶ 163).

Sugimoto Figs. 8A & 8B



That Sugimoto discloses claim 5 is supported by the '126 patent's description and Everlight's infringement contentions (*see supra* §V.D.).

3. Sugimoto Anticipates Claim 6

To the extent that claim 6 has any meaning, Sugimoto anticipates claim 6.

Sugimoto Figure 3 is similar to Figure 1. However, Sugimoto add an adhesion layer 311 “that further enhances the adhesion” between the first and the second p electrodes to Figure 1 (Ex-1006 at ¶ [0087]). Sugimoto discloses that “the adhesion layer 311 may be conductive” (Ex-1006 at ¶ [0088]). Sugimoto also discloses that the upper layer of the adhesion layer may be made of silver or gold and the lower layer may be tin (Ex-1006 at ¶ [0089]).

4. Sugimoto Anticipates Claim 9

Claim 9 is a manufacturing claim that corresponds to claim 1. Sugimoto anticipates claim 1 for the reasons described above regarding claim 1.

5. Sugimoto Anticipates Claim 12

Claim 12 recites the “method for manufacturing a semiconductor light-emitting element according to claim 9, wherein the second n-electrode and the second p-electrode are formed through sputtering or plating.” Sugimoto teaches that “second electrodes are formed” by “sputtering” and the “second electrode is deposited by, for example, sputtering” (Ex-1006 at ¶¶ [0155]; Ex-1006 at [0019]; *see also* Ex-1006 at ¶¶ [0020], [0021], [0024]; Ex-1003 at ¶ 166).

C. Ground 3: Obvious Over Shin in view of any of the Thin Film Art

For Ground 3, the prior art consists of Shin (Ex-1005) and one or more of Terashima, Sugimoto, Uemura '259, Uemura '999, and/or Inoue (Collectively the “Thin Film Art”). Shin described all of the limitations of claim 1, 2, 5, and 7-10 with

the exception of possibly the claimed electrodes being “thin films.” While Shin discloses thin film electrodes to a POSITA, Shin does not use the precise words “thin film.” Therefore, the Thin Film Art is cited as prior art disclosing thin film electrodes. Claims 1, 2, 5, and 7-10 are obvious over the Shin plus one or more of the Thin Film Art (Ex-1003 at § 9.3).

1. Shin Plus the Thin Film Art Renders Claim 1 Obvious

Shin plus the Thin Film Art discloses each element of claim 1 as described below (Ex-1003 at § 9.3.1). The scope and content of the prior art compared to the claims is provided below.

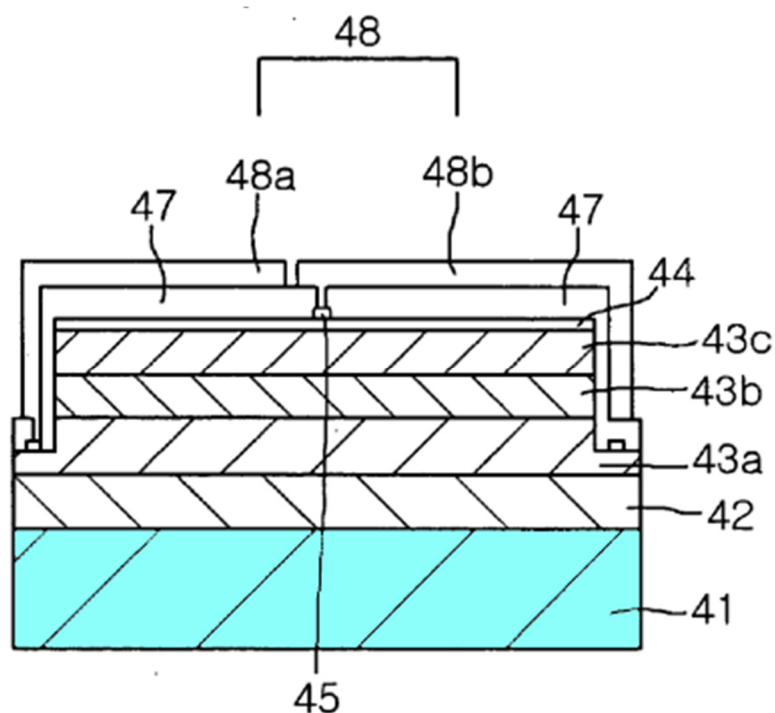
a. Shin Discloses Claim 1’s Preamble

Shin states that “the present invention pertains, in general, to a light emitting diode (LED), which is a “semiconductor light-emitting element” (Ex-1005 at ¶¶ [0002]; [0004]; [0020]; [0074]; [0019]).

b. Shin Discloses the Substrate Limitation

Shin discloses “sapphire substrate 41” (blue, Ex-1005 at ¶¶ [0020] [0039]; [0040]; *see also* ¶¶ [0005], [0107], [0108]; FIGs. 3, 4A, 5), which satisfies claim 1’s “substrate” limitation. Shin’s sapphire substrate 41 is transparent and light transmitting (Ex-1003 at ¶ 171).

Shin Fig. 5 (Annotated)

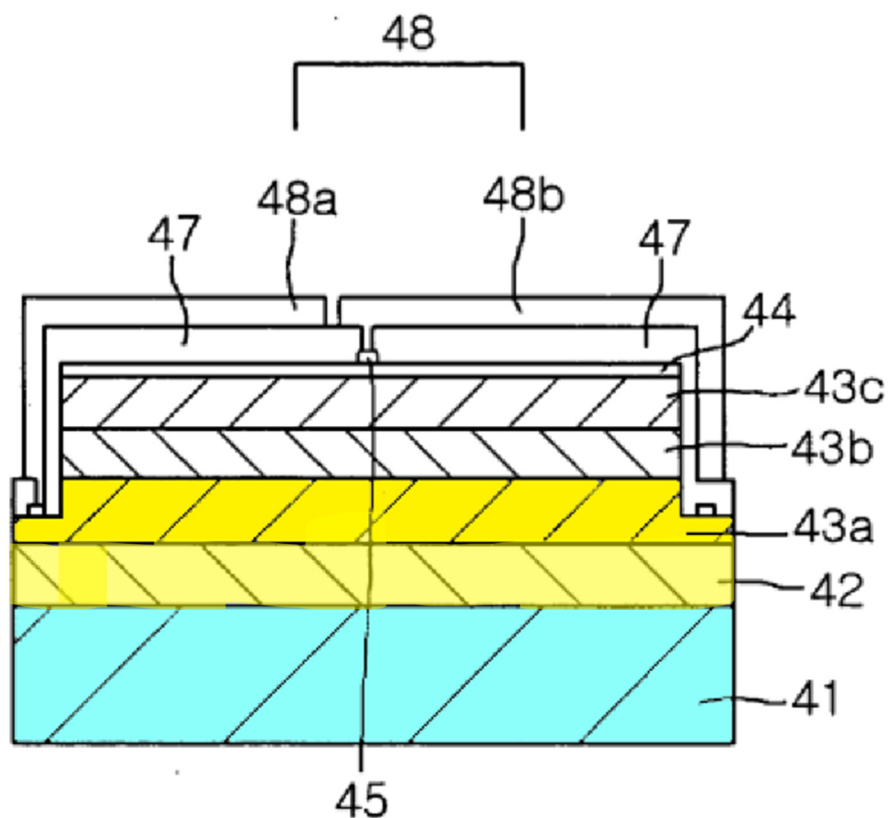


c. Shin Discloses the N-type Layer Limitation

Shin discloses an “n-type GaN clad layer 43a” and “buffer layer” 42 [yellow] which together are the claimed “an n-type semiconductor layer” (Ex-1005 at ¶ [0040]; Ex-1003 at ¶ 172). Dr. Lebby explains that an LED n-type or p-type semiconductor layer is often described as having sublayers including buffer or clad layers (Ex-1003 at ¶¶ 123, 172). For example, as Dr. Lebby and Shin describe, n or p layers may include a “buffer layer” in a standard LED epitaxial growth process to improve lattice matching between a layer and another material, such as the sapphire substrate, to reduce strain at the interface of different materials (Ex-1003 at ¶ 172 ; Ex-1005 at ¶

[0040]). Shin's "n-type GaN clad layer 43a" and "buffer layer" 42 [yellow] are "formed on" and cover the sapphire substrate 41" [blue] (FIG. 5 yellow) (Ex-1005 at ¶ [0040]).

Shin Fig. 5 (Annotated)



d. Shin Discloses the p-type Layer Limitation

Shin discloses "p-type GaN clad layer 43c," [green] which is the claimed "p-type semiconductor layer" (Ex-1005 at ¶ [0040]; Ex-1003 at ¶ 173). As shown in FIG. 5, Shin's p-type semiconductor layer 43c [green] covers an area on the n-type semiconductor layer 42/43a. FIG. 5 shows an area for the n-electrodes 46a-b [purple] is excluded from the cover of the p-type semiconductor layer 43c [green] (Ex-1003

at ¶ 173).

Shin Fig. 5 (Annotated)

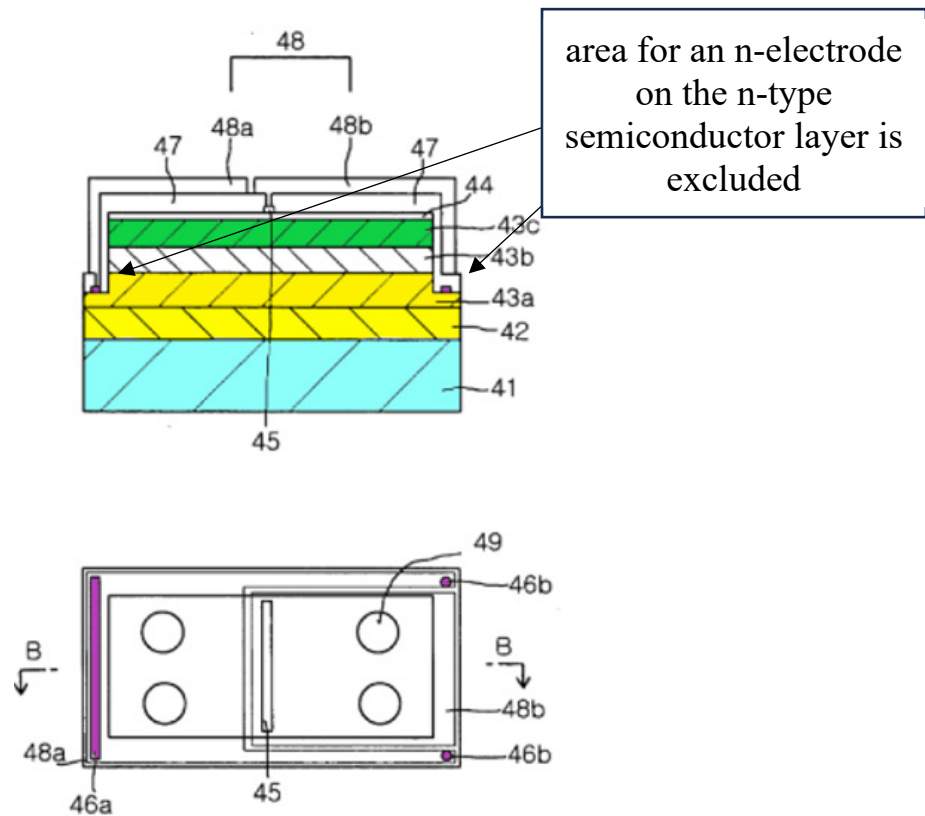


FIG. 5

e. Shin and The Thin Film Art Disclose the First n-Electrode Limitation

Shin discloses a first “n-electrode 46” [purple] “formed on Shin’s n-type semiconductor layer 43a/42 [yellow] (Ex-1005 at ¶ [0044]; Fig. 4C), which is the claimed “first n-electrode.”

Shin Fig. 4C (Annotated)

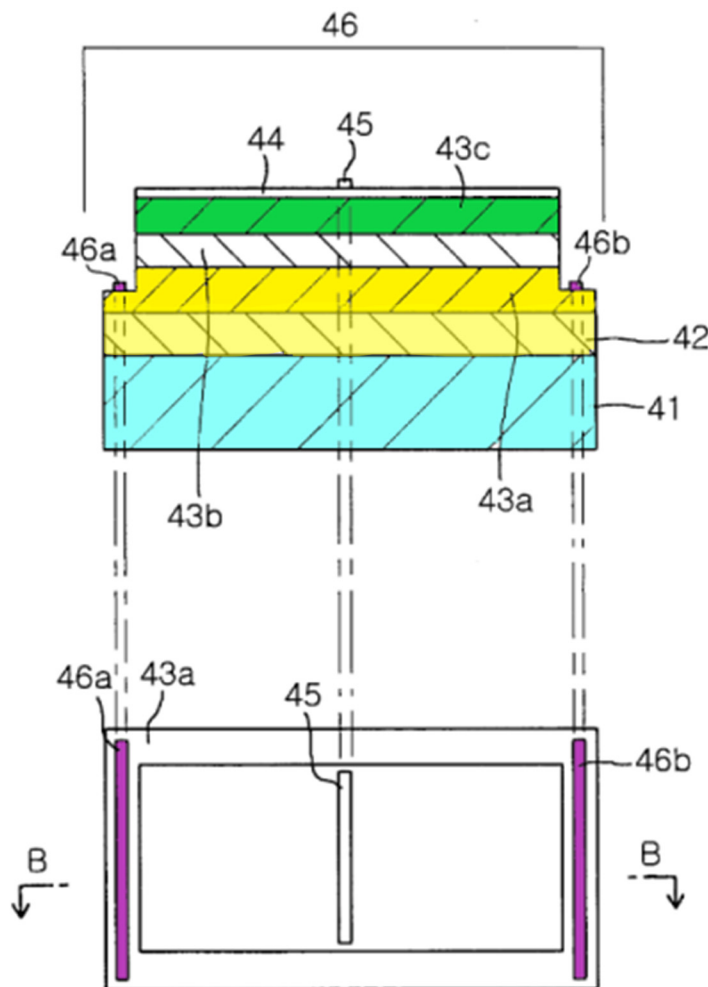


FIG. 4C

As Dr. Lebby explains, a POSITA understands that Shin discloses thin film electrodes because: (i) Shin describes that the invention pertains to a gallium nitride LEDs diode for flip-chip bonding (Ex-1005 at ¶ [0002]), which primarily used thin film electrodes by 2003, (Ex-1003 at ¶ 175); (ii) the disclosed electrodes are “formed

on” the semiconductor layers or other electrodes to specific shapes and widths (e.g., “lane electrodes having widths of 10 to 20 microns (Ex-1005 at ¶¶ [0015], [0026] [0044],-[0046] [0051]) thereby informing a POSITA that conventional sputtering, plating, or other processes are used to “form” the electrodes by depositing metal and forming thin films (Ex-1003); and (iii) Shin discloses that the LED is attached to a circuit board with gold bumps (Ex-1005 at []) (Ex-1003 at ¶¶ 105, 175-177). A POSITA understands the gold bumps are on the order of 10 microns thick (Ex-1003). A POSITA knows that Shin’s gold bumps would be used with thin film electrodes based on the thickness of the gold bumps (Ex-1003 at ¶ 177). Shin also describes a “conventional” LED by referring to Inoue (Ex-1021 at 3:35-4:17), which describes thin metal film electrodes of about a micron thick (Ex-1021 at 13:13-20; Ex-1003 at ¶¶ 105, 175).

Nevertheless, Shin does not use the words “thin film.” As described by Dr. Lebby, each of the Thin Film Art discloses thin film electrodes (Ex-1003 at § 8.2). It would have been obvious to a POSITA (and a POSITA would have been motivated) to use a thin film electrode as disclosed in one or more of the Thin Film Art as the electrodes in Shin because Shin describes a GaN LED where the state of the art included using thin film electrodes (Ex-1003 at ¶ 178). Using thin film electrodes as taught in each of the Thin Film Art was well-understood, common knowledge,

predictable, and routine in 2003 (Ex-1003 at § 8.2, ¶ 178). Song describes that thin film electrodes were in “wide-spread” use (Ex-1017 at 1:32-34). Using a thin film electrode as disclosed in each of the Thin Film Art in Shin yields an operational LED and predictable results because Shin is directed to GaN LEDs where thin film electrodes were common (Ex-1003 at ¶ 178). Further, the sputtering and other processes for manufacturing thin films were known and predictable ways to make thin film electrodes and enhance light extraction (Ex-1003 at § 8.2, 9.3.1.5).

A POSITA would have further been motivated to use thin film electrodes from one or more of the Thin Film Art in Shin to enhance light extraction from an LED package (Ex-1003 at § 8.2, 9.3.1.5). A primary goal of an LED package is to maximize the amount of light emitted by an LED from the LED package (Ex-1003 at ¶¶ 107-108, 179). Metal electrodes can be used to provide the electrical path for electricity to reach the LED because metals are excellent electrical conductors as well as thermal conductors to dissipate heat (Ex-1003 at ¶¶ 107-108, 179). However, metals also reflect light and can absorb light (Ex-1003 at ¶¶ 107-108, 179). If light is reflected back into the LED package or absorbed, this can decrease light extraction (Ex-1003 at ¶¶ 107-108, 179). Thin film electrodes were developed as a way to provide the benefits of a metal electrode but minimize the impact on light extraction (Ex-1003 at ¶¶ 107-108, 179). Thus, a POSITA would have been motivated to use

one or more of the Thin Film Art electrodes as the electrodes in Shin.

A POSITA would have been further motivated to use thin film electrodes in one or more of the Thin Film Art in Shin because a POSITA knew that thin film electrodes provided good reliability, good adhesion/bonding, and good conductance, so that the applied LED voltage can be minimized to prevent LED degradation (Ex-1003 at ¶ 180; Ex-1006 at [0014], [0016], [0021]-[0034]). Moreover, Inoue describes thin films as conventional and a POSITA would have been motivated to use conventional thin films (Ex-1003 at ¶ 180; § 8.2).

Moreover, a POSITA would have been motivated to use one or more of the Thin Film Art electrodes for Shin's electrodes because each of those electrodes fits within Shin's description of using "lane electrodes," having as narrow a width as possible" and "widths of 10-20 microns" (Ex-1003 at ¶ 180; Ex-1005 at ¶¶ [0026], [0045]-[0046]).

f. Shin and The Thin Film Art Disclose the First P-Electrode Limitation

Shin discloses "a first p-electrode that is a thin film formed on the p-type semiconductor layer" (Ex-1003 at ¶¶ 105, 181, 182). For example, Shin discloses a nitride semiconductor device having a first "p-electrode" 45 (red, Fig. 3 below) (Ex-1005 at ¶¶ [0044]). While the below annotated version of Shin FIG. 4C shows a transparent electrode 44 between the p-type GaN clad layer 43 c [green] and the p

electrode 45 [red], Shin describes that the transparent electrode 44 “may be omitted” (Ex-1005 at ¶ [0043]). Thus, Shin discloses that p electrode 45 [red] is “formed on” p-type GaN clad layer 43c [green].

Shin Fig. 4C (Annotated)

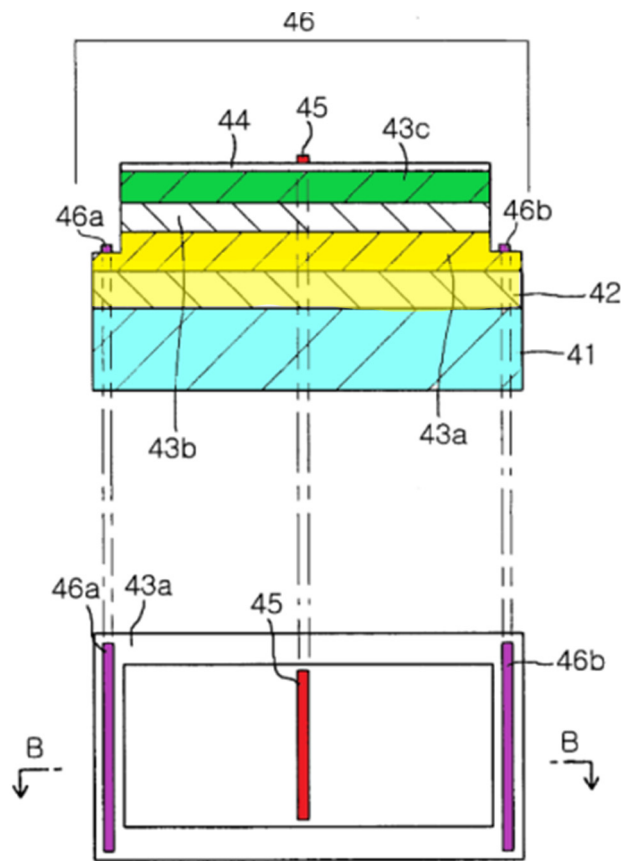


FIG. 4C

A POSITA understands that Shin discloses thin film electrodes based on Shin’s disclosure (Ex-1003 at ¶ 182; Ex-1003 at ¶ 173). Shin’s p-electrode is described as having as “narrow width as possible” and for example having a width of 10-20

micrometers (Ex-1005 at ¶¶ [0026], [0046]; (Ex-1003 at ¶¶ 105, 182). For the reasons described above with reference to the first n-electrode, Shin plus one or more of the Thin Film Art discloses a thin film as the first p-electrode and a POSITA would have been motivated to use a thin film from one or more of the Thin Film Art as the first p-electrode in Shin (*see supra* §XI.C.1.e; Ex-1003 at ¶¶ 182; §§ 8.2; 9.3.1.5-9.3.1.6).

g. Shin Discloses the First Insulating Layer Limitation

Shin discloses “a transparent, nonconductive passivation layer 47” [pink] that is the claimed “first insulation layer” for electrically insulates electrodes (Ex-1005 at ¶¶ [0020], [0046]; Ex-1003 at ¶ 183). As shown in Fig. 4C, Shin’s “passivation layer 47” electrically insulates the first n-electrode [purple] and the first p-electrode [red] from each other (*see* Ex-1005 at ¶ [0046]). Shin further describes that after the first n and p electrodes are formed, the “nonconductive passivation layer is formed on the resulting structure” (*e.g.*, on both first n and p electrodes), thereby insulating the first n and p electrodes from each other (Ex-1005 at ¶ [0047], *see also* ¶ [0020]). Portions of the passivation layer are punched to expose portions of the first n and p electrodes as shown in FIG. 4D (purple first n-electrodes, and red first p-electrode) (Ex-1005 at ¶ [0047]).

Shin Fig. 4D (Annotated)

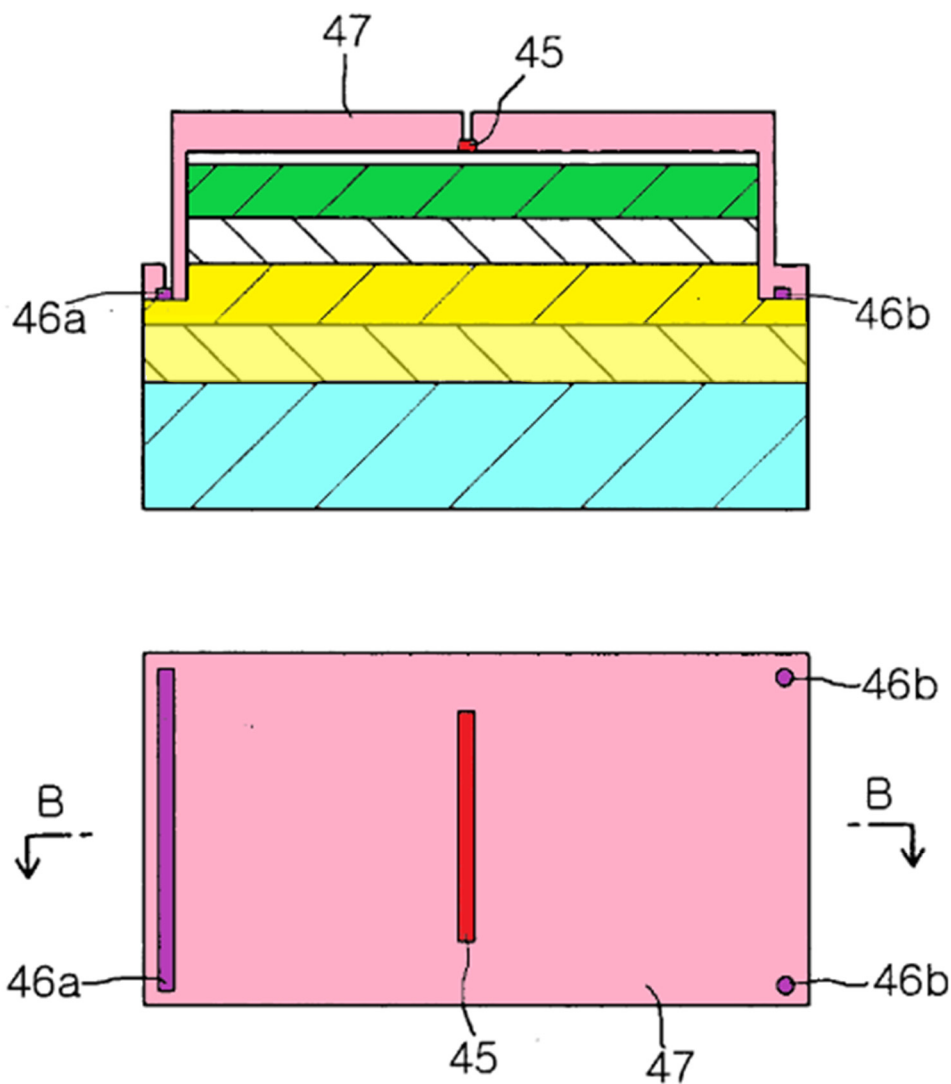


FIG. 4D

h. Shin and the Thin Film Art Disclose the Second N-Electrode Layer Limitation

Shin discloses “a second n-electrode” 48a [orange] formed as a thin film on the

first n-electrode 46a [purple] and the first insulating layer 47 [pink]) and having an area larger than a joined face between the n-type semiconductor layer 43a/42 [yellow] and the first n-electrode 46 [purple], so that the second n-electrode 48a [orange] is electrically connected to the first n-electrode 46 [purple], the second n-electrode 46 [purple] being insulated from the first p-electrode 45 [red] by the first insulating layer 47 [pink] (Ex-1003 at ¶ 183; Ex-1005 at ¶ [0051], FIG. 5). Shin's second n-electrode covers a significant portion of the passivation insulation layer (Ex-1003 at ¶¶ [0045], [0051]). Thus, Shin's second n-electrode (orange) has an area that is larger than the "joined face between the n-type semiconductor material" (yellow) and the first n-electrode (purple (Ex-1005 at ¶¶ [0052], [0055]; Ex-1003 at ¶ 185).

As Dr. Lebby testifies, second bonding electrode 48a is formed as a thin film given that it is described as being shaped with a lane, with a width of 10-20 micrometers, and "formed in a shape of '['" on passivation layer 47 (Ex-1003 at ¶¶ 184-186; Ex-1005 at ¶¶ [0020], [0026], [0051]). For the reasons described above with reference to the first n-electrode, Shin plus one or more of the Thin Film Art discloses the second n-electrode limitation and a POSITA would have been motivated to use a thin film from one or more of the Thin Film Art as the second n-electrode in Shin (*see supra* §XI.C.1.e; Ex-1003 at ¶¶ 186; §§ 8.2, 9.3.1.5, 9.3.1.8).

Shin Fig. 4E (Annotated)

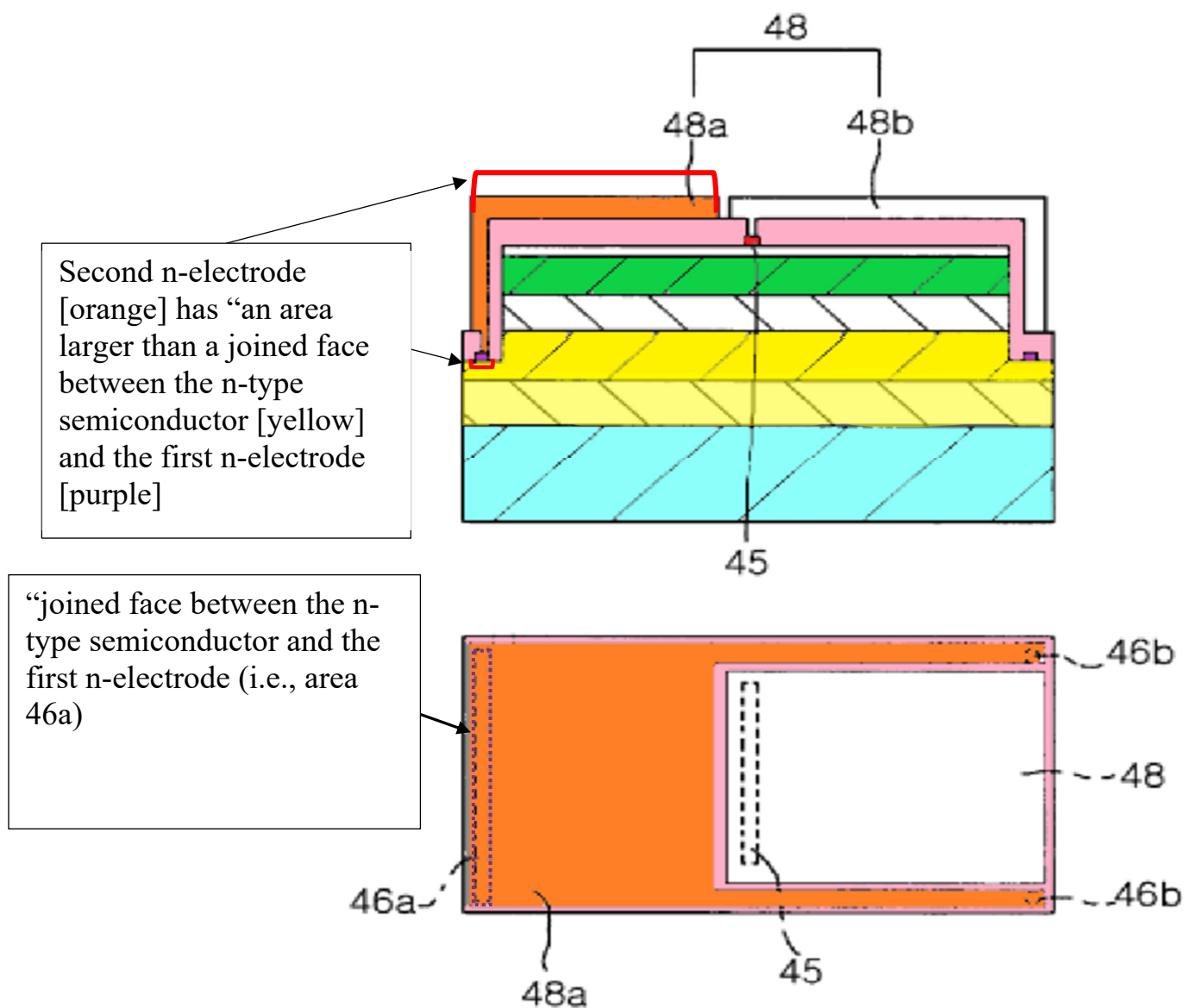


FIG. 4E

i. Shin and the Thin Film Art Disclose the Second P-Electrode Layer Limitation

Shin discloses “a second p-electrode” (*i.e.*, second bonding electrode 48b)

[grey]) “formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer” 43a/42 [yellow] and the p-type semiconductor layer 43c [green], the second p-electrode 48b [grey] “being electrically connected to the first p-electrode” 45 [red] (Ex-1003 at § 9.3.1.9). Shin’s second p-electrode 48a has an area smaller than joined face between the n-type semiconductor layer 43a/42 and the p-type semiconductor layer 43c [green] (Ex-1005 at ¶ [0045], [0050], [0051]; FIGS. 4C& 4D, 5 above; Ex-1003 at § 9.3.1.9).

A POSITA understands that Shin discloses thin film electrodes based on Shin’s disclosure (Ex-1003 at §§ 8.2, 9.3.1.9). For example, As Dr. Lebby testifies, second bonding electrode 48b is formed as a thin film given that it is described as being shaped as a “lane” with a width of 10-20 micrometers (Ex-1003 at §§ 8.2, 9.3.1.9; Ex-1005 at ¶¶ [0020], [0026], [0051]). For the reasons described above with reference to the first p-electrode, Shin plus one or more of the Thin Film Art discloses the second p-electrode limitation and a POSITA would have been motivated to use a thin film from one or more of the Thin Film Art as the second p-electrode in Shin (*see supra* §XI.C.1.e; Ex-1003 at ¶¶ 186; §§ 8.2; 9.3.1.5, 9.3.1.9).

Shin Fig. 4E Annotated

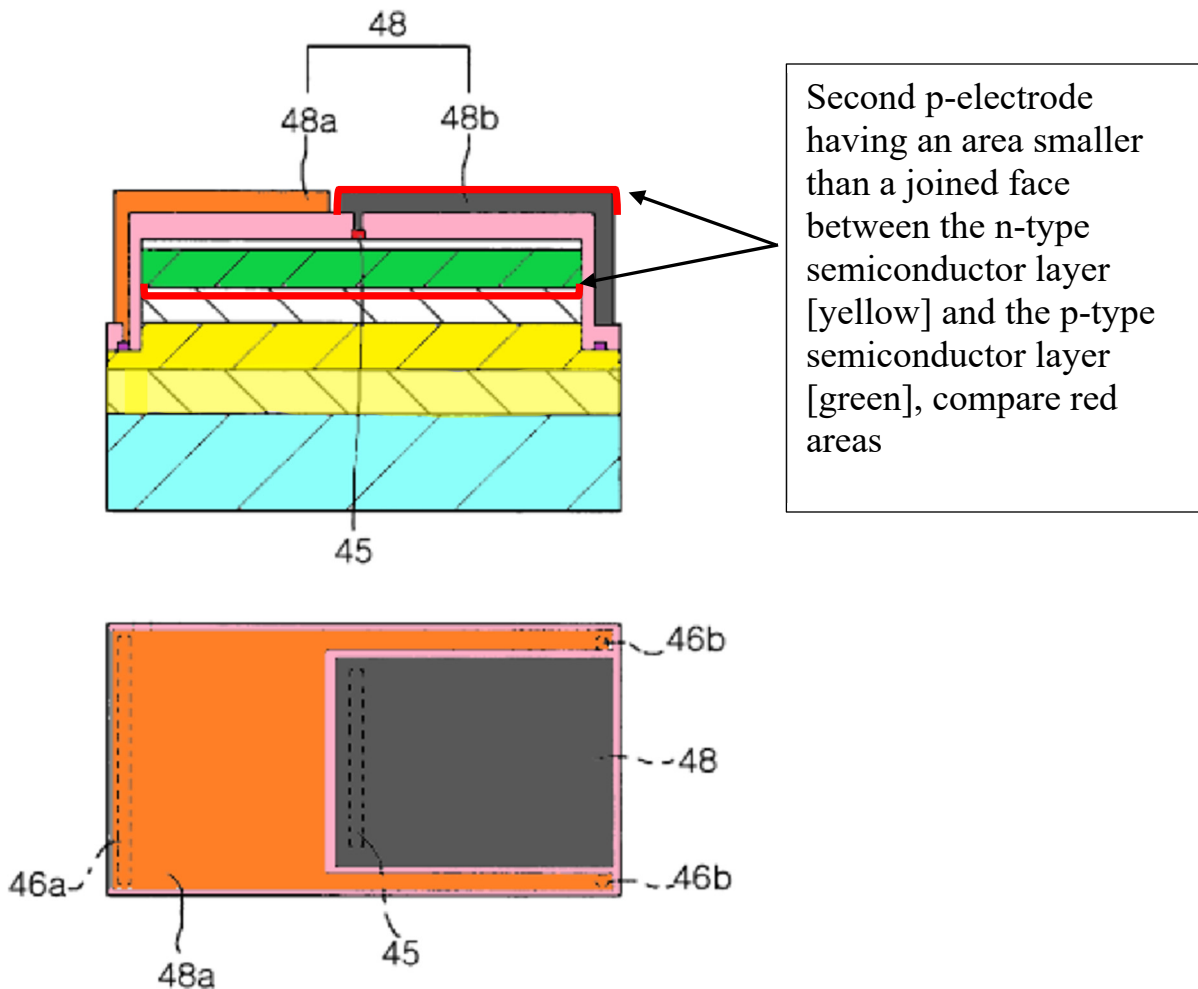


FIG. 4E

j. Obviousness Conclusion

As Dr. Lebby explains, thin film electrodes were well within the level of ordinary skill in the art. There are no known second factors of nonobviousness. Thus, claim 1 is obvious over Shin in view of one or more of the Thin Film Art (Ex-1003 at ¶ 190).

2. Shin Plus One or more of the Thin Film Art Renders Claim 2 Obvious

Claim 2 is independent. Claim 2's preamble and first five elements are the same as claim 1. Therefore, Shin discloses claim 2's preamble and the first five elements as described above with reference to claim 1 (*see supra* §XI.B.1.). The differences between claim 1 and 2 related to the “the first insulation layer” having “openings” electrodes and the “second p-electrode” being formed on the “first insulation layer” (Ex-1001 at 13:63-14:7; 14:21-38). These limitations are shown in Shin's FIGS. 4E and 5 above and are described as satisfied by Dr. Lebbby (Ex-1003 at § 9.3.2).

Shin discloses the claimed “openings” in FIGs 4C, 4D (Ex-1005 at Fig. 4C, 4D; Ex-1003 at § 9.3.2.2).

Shin Fig. 4C (Annotated)

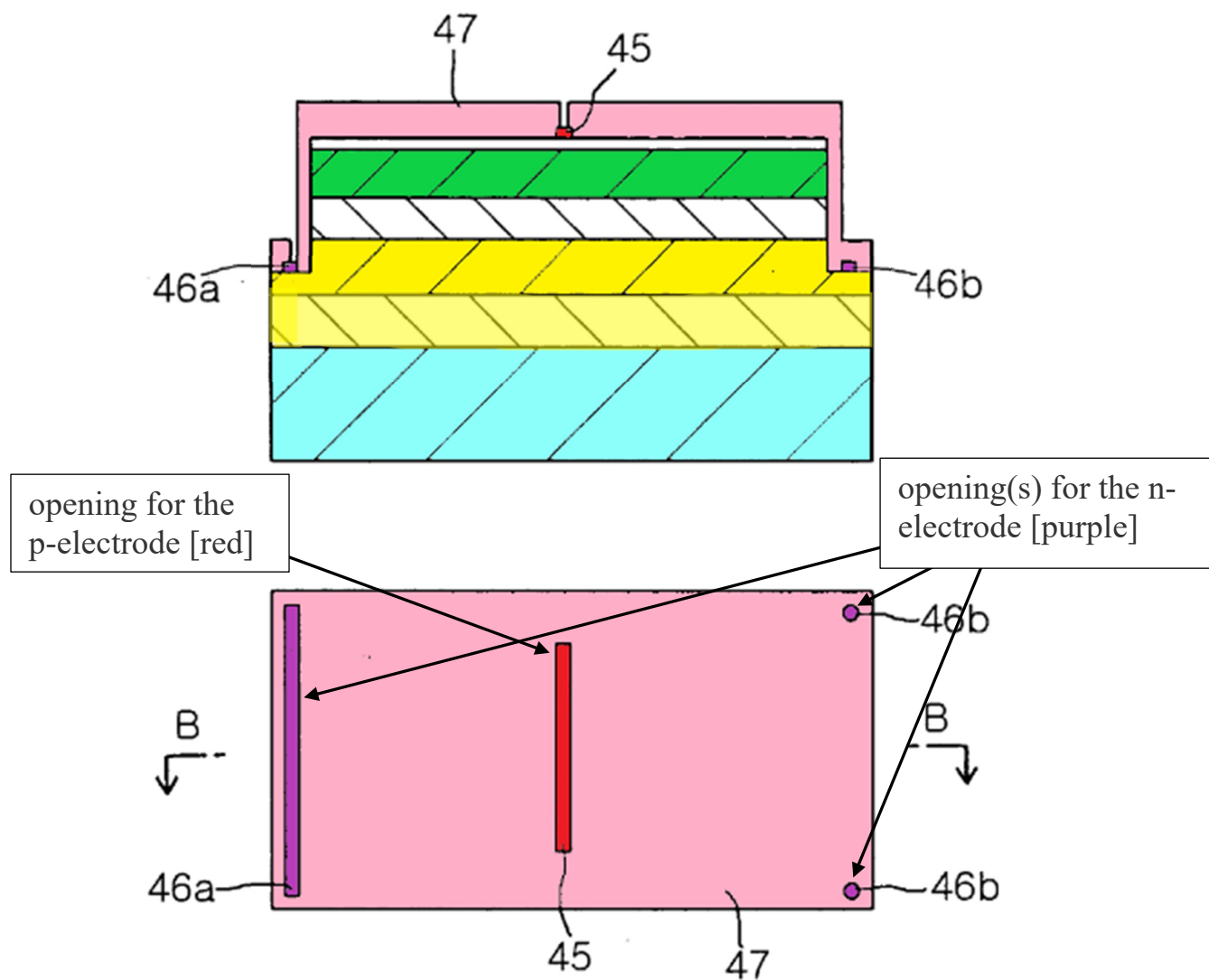


FIG. 4D

Shin's "passivation layer 47" or "first insulating layer" (pink) is punched to create an opening for the n-electrode 46 and an opening for the p-electrode 45 (*see*

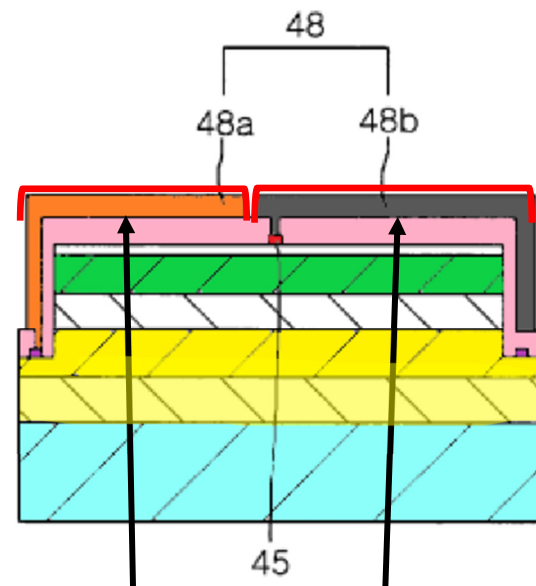
Ex-1005 at ¶¶ [0046] [0048]). Further, Shin discloses in FIG. 4E that the second n-electrode 48a [orange]) is electrically connected to the first n-electrode 46 [purple]) through the opening for the n-electrode in the first insulating layer 47 [pink] (Ex-1003 at § 9.3.2.3). In addition, as shown in Fig. 4E above, Shin discloses a second p-electrode 48b [gray] formed on the first insulating layer 47 [pink], as a thin film and being electrically connected to the first p-electrode 45 through the opening for the p-electrode in the first insulating layer (Ex-1003 at § 9.3.2.4). As Dr. Lebby describes, Shin discloses the limitations of claim 2 that differ from claim 1 (Ex-1003 at § 9.3.2).

There are no differences between claim 2 and Shin and the Thin Film Art. Considering the level of ordinary skill in the art and the lack of secondary factors, claim 2 is obvious over Shin in view of one or more of the Thin Film Art (Ex-1003 at § 9.3.2).

3. Shin and the Thin Film Art Renders Claim 5 Obvious

Claim 5 recites that “semiconductor light-emitting element according to claim 1, wherein the second n-electrode and the second p-electrode have virtually same size.” Shin states that both second electrodes are 10-20 micrometers in width and are “lane” electrodes with virtually the same size as shown in FIG. 4E (Ex-1005 at ¶¶ [0020], [0021], [0026]; Ex-1003 at ¶ 198). Thus, Shin discloses claim 5’s limitations and claim 5 is obvious over Shin plus one or more of the Thin Film Art (Ex-1003 at ¶ 198)

Shin Fig. 4E (Annotated)



second n-electrode 48a [orange]
and the second n-electrode 48b
[gray] have “virtually the same
size”

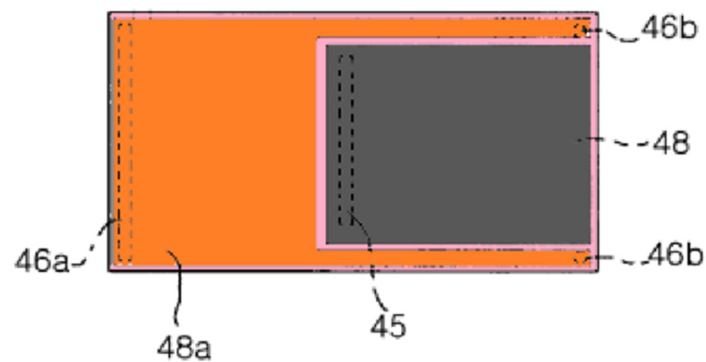


FIG. 4E

4. Shin Plus the Thin Film Art Renders Claim 7 Obvious

Claim 7 recites a “light-emitting device comprising: the semiconductor light-emitting element according to claim 1; a circuit board having a plurality of electrodes; and a conductive bonding material layer that electrically connects and fixes the second n-electrode and the second p-electrode to the electrodes on the circuit board.”

Shin’s “Si substrate 61” [brown] is the claimed circuit board having “signal patterns 62” or electrodes to attach to an LED ((Ex-1005 at ¶ [0049]; Ex-1003 at ¶ 200). Shin’s Au bumps 63 [indigo] are the claimed conductive bonding layer that electrically connects the LED second n and p electrodes to the signal patterns (Ex-1005 at ¶¶ [0013], [0061]-[0063]; Ex-1003 at ¶ 200). Thus, Shin discloses claim 7’s limitations and claim 7 is obvious over Shin plus one or more of the Thin Film Art (Ex-1003 at ¶ 200).

Shin Fig. 6 (Annotated)

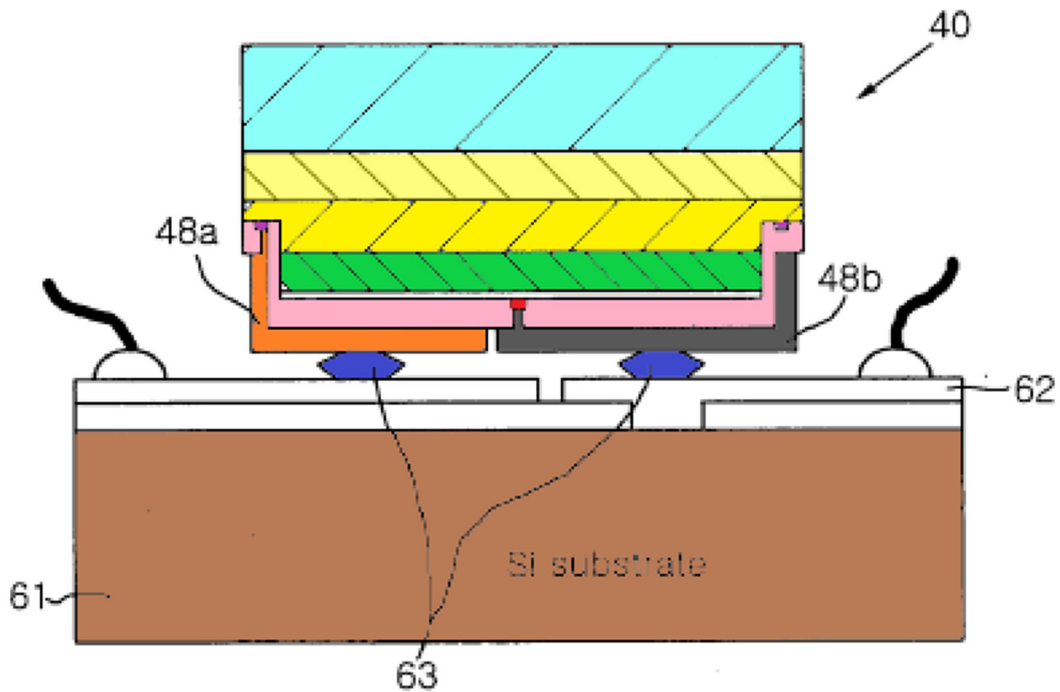


FIG. 6

5. Shin Plus the Thin Film Art Renders Claims 9 & 10 Obvious

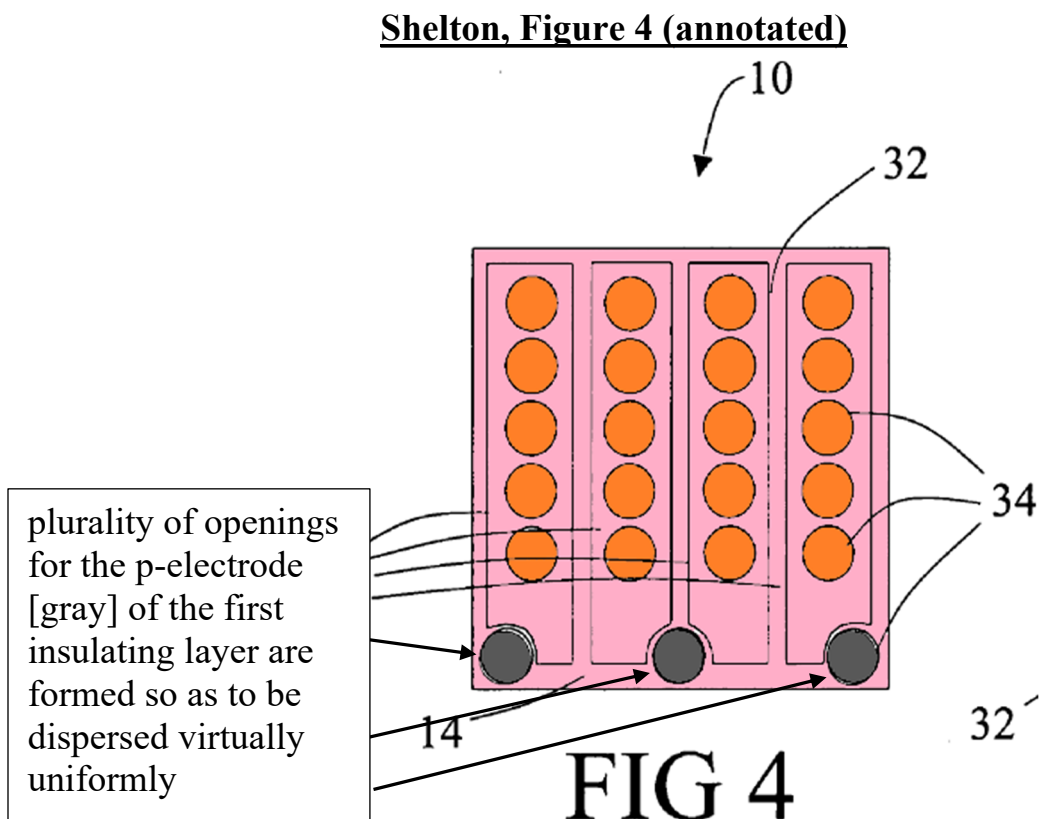
Claims 9 and 10 are methods of manufacturing claims that corresponds to claims 1 and 2. Shin anticipates claims 9 and 10 for the reasons explained above with reference to claims 1 and 2 (Ex-1003 at §§ 9.3.5-9.3.6).

D. Ground 4: Claim 4 is Obvious over Terashima or Ground 3 in view of Shelton

Claim 4 recites: “The semiconductor light-emitting element according to claim 2, wherein a plurality of openings for the p-electrode of the first insulating layer are formed so as to be dispersed virtually uniformly.” It would have been obvious to a POSITA to modify Terashima or Shin in view of Shelton to form the alleged invention of claim 4 (Ex-1003 at § 9.4).

Shelton discloses “a plurality of openings for the p-electrode of the first insulating layer are formed so as to be dispersed virtually uniformly.” As shown below, Shelton’s n-electrode 12 [orange] and p-electrode 14 [gray] are sealed by a dielectric layer 32 [pink], which is an insulating layer (Ex-1011 at ¶ [0038]).

Shelton’s dielectric layer 32 includes several vias 34 or “openings to “provide access to the p-type and n-type electrodes” (12 [gray], 14 [orange]), which are distributed virtually uniformly across the “lateral area of the light emitting diode 10 to promote current spreading across the light emitting diode 10” (Ex-1011 at ¶ [0039]; Ex-1003 at §9.4).



Terashima does not expressly describe how openings for the p-electrode are disposed. It would have been obvious to modify Terashima to have a plurality of openings for the p-electrode in the first insulating layer that are disposed uniformly in view of Shelton to promote uniform current spreading in the p-semiconductor layer or Inoue to achieve sufficient brightness (Ex-1003 at ¶¶ 205, § 8.5).

Providing uniform current spreading can prevent deteriorating the LED and

maximize light extraction (Ex-1003 at ¶ 205, § 8.5). How to create uniform openings and the results were known and predictable (Ex-1003 at ¶ 205, § 8.5).

Shin describes a p-electrode positioned at the “center of the light emitting structure” (Ex-1004 at ¶ [0021]). Shin describes this positioning to be advantageous because “current uniformly flows” through the LED, thereby preventing the LED life span from being shortened due to concentration of current at a predetermined position (Ex-1004 at ¶ [0021]). Thus, Shin recognizes the importance of uniform current flow. A POSITA would have been motivated to modify Shin to have multiple p-electrode openings because the p-semiconductor layer only covers part of the n-semiconductor layer and therefore multiple openings as described by Shelton can provide even more uniform current flow and prevent life-shortening because the multiple opening can be more uniformly dispersed than an LED in the center of the device, which is not in the center of the p-semiconductor layer (Ex-1003 at ¶ 206). As Dr. Lebby describes, the techniques were known and predictable (Ex-1003 at ¶ 206).

E. Ground 5: Claims 5 is Obvious over Terashima in view of Shin, Sugimoto, Inoue, and/or the OLSA

To the extent that Terashima does not anticipate claim 5, claim 5 is obvious over Terashima in view of Shin, Sugimoto, and/or the OLSA (Ex-1003 at § 9.5). Shin and Sugimoto disclose the second n-electrode and the second p-electrode having

virtually the same size as recited in claim 5 (Ex-1003 at ¶¶ 81, 164, 200, 207). Inoue further discloses n electrode 36 and p electrode 38 having virtually the same size in Fig. 4A (Ex-1021 at Fig. 4A & 1:58; Ex-1003 at ¶ 207).

To the extent that Terashima does not disclose claim 5's limitations, it would have been obvious to have Terashima's second n-electrode and the second p-electrode have virtually the same size (Ex-1021 at Fig. 4A & 1:58; Ex-1003 at § 9.5). Each electrode needs to be of sufficient size to mechanically connect to electrodes, provide electricity, and thermal heat dissipation. Both electrodes have similar requirements (Ex-1021 at Fig. 4A & 1:58). Therefore, it would have been obvious to a POSITA for Terashima's second n-electrode and second p-electrode to have virtually the same size (Ex-1021 at Fig. 4A & 1:58; Ex-1003 at § 9.5). This was well-known and predictable (Ex-1021 at Fig. 4A & 1:58; Ex-1003 at § 9.5).

F. Ground 6: Claims 6 is Obvious over Terashima, Sugimoto, or Ground 3 in view of Shelton and/or the OLSA

Claim 6 recites “wherein the conductive bonding material layer is any one of the members selected from a group consisting of solder, silver paste, and anisotropic conductive resin. To the extent that this claim is definite and Terashima, Shin, and Sugimoto do not disclose this limitation, this claim is obvious over Terashima, Shin, and Sugimoto in view of Shelton and/or the OLSA (Ex-1003 at § 9.6). Shelton discloses that LED p and n electrodes can be bonded with solder to “mechanically

secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]). Shelton’s solder constitutes the claimed “conductive bonding material layer.”

Moreover, citing APA and Shin, Dr. Lebby testifies that it was rudimentary for a POSITA to attach an LED to a circuit board with solder (Ex-1003 at ¶ 211, § 8.5). The APA admits that “in general, a mounting process onto a circuit board is carried out at low costs by using a conductive bonding material such as solder and silver paste” (Ex-1003 at ¶ 211 citing to Ex-1001 at 2:14-16).

G. Ground 7: Claim 7 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA

To the extent that either Terashima, Shin, or Sugimoto do not anticipate claim 7, claim 7 is obvious over Terashima, Shin + one or more of the Thin Film Art, or Sugimoto in view of Shelton and/or OLSA (Ex-1003 at § 9.7). Shelton discloses that LED p and n electrodes can be bonded with solder, a “conductive material,” and “reflow alloy bonding” to “mechanically secure” and electrically connect a light emitting diode to bonding bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]). Moreover, citing the ’126 patent admissions, Dr. Lebby testifies that it was rudimentary for a POSITA to attach LED p and n electrodes to a circuit board (Ex-1003 at §§ 9.7, 8.5; Ex-1001 at 2:14-16).

H. Ground 8: Claim 8 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA

To the extent that Terashima does not anticipate claim 8, claim is obvious over Terashima in view of Shelton and/or the level of skill because Shelton discloses claim 8's limitations and a POSITA was aware of claim 8's limitations which are rudimentary as described above (Ex-1003 at §§ 9.8, 8.5).

I. Ground 9: Claim 11 is Obvious over Ground 3 or Sugimoto in view of Terashima and/or the OLSA

Claim 11 recites the “method for manufacturing a semiconductor light-emitting element according to claim 10, wherein the first insulating layer is formed through sputtering.” Neither Shin nor Sugimoto expressly state that the “first insulating layer is formed through sputtering.” However, Terashima teaches that the protective film 20, which is the claimed “first insulating layer,” “is formed by a film forming means such as vacuum deposition or sputtering” (Ex-1010 at ¶ [0036]). As Dr. Lebby explains, sputtering to form insulation layers was well-known, predictable, and within the ordinary level of skill in the art and a POSITA would have been motivated to use known sputtering techniques to form the claimed insulation layer (Ex-1003 at §§ 9.9, 8.4). The '126 patent did not invent a sputtering process (Ex-1003 at §§ 8.4, 9.9). In fact, Everlight admits in its infringement contentions that “sputtering is commonly applied to the formation of electrode films or insulating later in the technical field of light emitting diode

manufacturing” (Ex-1016 at p. 71; *see also* p. 74).

J. Ground 10: Claim 12 is Obvious over Ground 3 in view of Terashima, Sugimoto, and/or the OLSA

While Shin does not expressly state that Shin’s second n and p electrodes were formed through “sputtering or plating,” Terashima and Sugimoto disclose the limitations of claim 12 (Ex-1003 at ¶ 222, §§ 9.1.10, 9.2.5). Dr. Lebby further explains that claim 12 is obvious because, *inter alia*, sputtering and plating were common techniques for forming the claimed electrodes and well within the ordinary level of skill in the art, predictable, and routine (Ex-1003 at §§ 8.4, 9.10; *see also* Ex-1016 at pp. 71, 74).

K. Ground 11: Claim 13 is Obvious over Terashima, Ground 3, or Sugimoto in view of Shelton and/or the OLSA

Claim 13 recites a “method for mounting semiconductor light-emitting elements, comprising: placing solder between the second n-electrode as well as the second p-electrode of the semiconductor light-emitting element according to claim 1 and a plurality of electrodes on a circuit board, and then carrying out a reflow treatment thereon, thereby the semiconductor light-emitting elements are mounted on the circuit board through solder.” Claim 13 is obvious over Terashima, Shin, or Sugimoto in view of Shelton and/or the OLSA (Ex-1003 at § 8.6, 9.11). Shelton discloses that an LED with n and p electrodes that can be bonded with solder and “reflow alloy bonding” to “mechanically secure” a light emitting diode to bonding

bumps or electrodes of a “printed circuit board” (Ex-1011 at ¶ [0044]). Further, reflow was common knowledge, within the level of ordinary skill in the art, and predictable to a POSITA (Ex-1003 at §§ 8.6, 9.11). Therefore, a POSITA would have been motivated to use the routine known techniques claimed to mount an LED on a circuit board.

L. Ground 12: Any of Grounds 1, 4-8, and 11 with respect to Terashima in view of the Thin Film Art

Terashima discloses thin film electrodes. To the extent Patent Owner contends otherwise, it would have been obvious to a POSITA to combine Terashima with one or more of the Thin Film Art to form the claimed inventions for substantially the reasons set forth with respect to Shin (Ex-1003 at § 9.12).

XII. Secondary Considerations

Petitioners are not aware of any secondary considerations that would overcome the strong showing of obviousness provided by the Petition. Further, any attempt by Patent Owner to rely on alleged secondary considerations cannot overcome the showing of obviousness detailed above. *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1370 (Fed. Cir. 2011).

XIII. Conclusion

For the foregoing reasons, Petitioners respectfully request that the *inter partes* review of the '126 patent be instituted, as the Petition establishes a reasonable

likelihood of prevailing with respect to the Challenged Claims. Petitioners further respectfully request cancellation of the Challenged Claims.

Respectfully submitted,

FLASTER GREENBERG P.C.

Date: May 31, 2024

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Certificate of Service

Pursuant to 37 C.F.R. §§ 42.6 and 42.106, the undersigned certifies that a true and correct copy of the foregoing Petition for *Inter Partes Review* of U.S. Patent No. 7,554,126, together with Petitioner's exhibits identified in the above Table of Exhibits, and Petitioner's Powers of Attorney, have been served on the Patent Owner via Federal Express service for overnight delivery, a means at least as fast and reliable as Priority Mail Express, on the below date, at the following correspondence address of record for the '126 patent:

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